A Two Chip PCM Voice CODEC with Filters

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Abstract—**Architecture and design of a monolithic voice CODEC is described.**

The CODEC consists of 2 chips—the transmit chip includes the companding coder (nonlinear A/D) along with filtering functions, and the receive chip consists of the expanding decoder (nonlinear D/A) chip with its smoothing filter.

Experimental results show the circuit to meet accepted requirements.

I. Introduction

FOR MORE THAN a decade analog-to-digital (A/D) and digital-to-analog (D/A) conversion, i.e., the coder-decoder (CODEC) function has been required in the telephone system for transmission of voiceband signals. This involved the use of a high-speed CODEC multiplexed over 24, 32, or 96 channels using pulse amplitude modulation techniques. Technological advances have allowed the use of time division multiplexed digital switching networks to replace older space division analog switching networks. This has created yet another market for CODEC's (in addition to the channel bank application) for use in PBX's and local switching networks. The large volumes involved, coupled with the economics of LSI circuits, make the development of monolithic per channel CODEC's viable.

The CODEC to be described uses pulse-code modulation (PCM) for voice digitization. PCM is widely used in commercial telephony switching and is deeply entrenched in world networks for short haul transmission. In order to achieve the required greater than 70 dB dynamic range with an 8 bit digital word, compression/expansion technique is performed by using coding laws, the two internationally recognized laws for 8 bit PCM being the segmented $\mu 255$ law and the A Law [1]. The $\mu 255$ version has been implemented here and the A Law version is a metal mask option.

The standard sampling rate for PCM coding is 8 kHz. This requires that the signals applied to the coder be band-limited to below 4 kHz (Nyquist frequency) to prevent aliasing. In the decoder direction, after the digital word is decoded and is applied to the sample-and-hold, a smoothing filter is required to remove the high-frequency components from the sample-and-hold signal. These filtering functions have also been integrated on the same chip with the associated data converters.

II. Selection of Process Technology

Silicon gate CMOS technology was chosen to fabricate the CODEC. This choice was motivated by the availability of low-power digital circuitry and by the superior analog capability of CMOS compared to single channel MOS. The CODEC with filters has a large mix of analog and digital circuitry on the same chip. Thus digital feedthrough and noise can be coupled onto analog signal paths (for instance, through operational amplifier power supplies). Single channel operational amplifiers do not have a comparable power supply rejection from both supplies compared to CMOS operational amplifiers. This allows for a smaller decoupling requirement on CMOS analog circuitry power supply lines and also allows a wider operating voltage range. In addition, CMOS has vertical n-p-n bipolar transistors which provides low output impedance devices with high current drive capability.

Thin oxide voltage invariant capacitors were used for the CODEC. The polysilicon-to-aluminum capacitors are thermally grown using a double contact process. The first contact mask is used to define normal diffusion or polysilicon-to-metal contact openings and capacitor areas. A second contact mask is used after the wafer goes through a reflow process to remove oxide from normal contact areas. This mask is identical to the first contact mask if no capacitors are present. Thus, capacitors are fabricated without the need for additional masking steps.

III. Chip Architecture

The encoder and decoder with their corresponding filtering functions were integrated on two separate chips. This configuration guarantees good isolation between the transmit and receive functions. Integrating both functions on the same chip makes such isolation difficult to achieve, especially under an asynchronous mode of operation. In addition, each chip of such a pair is smaller than a single chip version and, as such, yields are higher and costs are lower. Further, many applications exist where either the transmit or receive functions are separately required.

Fig. 1(a), and (b) show the block diagram of the transmit and receive chip, respectively. In the transmit chip the voice signal is applied to a switched capacitor active low-pass filter through an uncommitted operational amplifier. The uncommitted operational amplifier is required for constructing an antialiasing filter with external passive components. These components can also be used for gain trimming. The low-pass filter is followed by a high-pass filter which also acts as a sample-and-hold for the encoder. The encoder performs the A/D conversion using a binary area ratioed capacitor array and a linear resistor string. An auto zero loop is also included to cancel any dc offset in the encoder/filter combination.

The phase-locked loop (PLL) synchronizes to an externally supplied strobe, typically 8 kHz, and provides all internal timing. In addition, the PLL powers down the chip during the ab-

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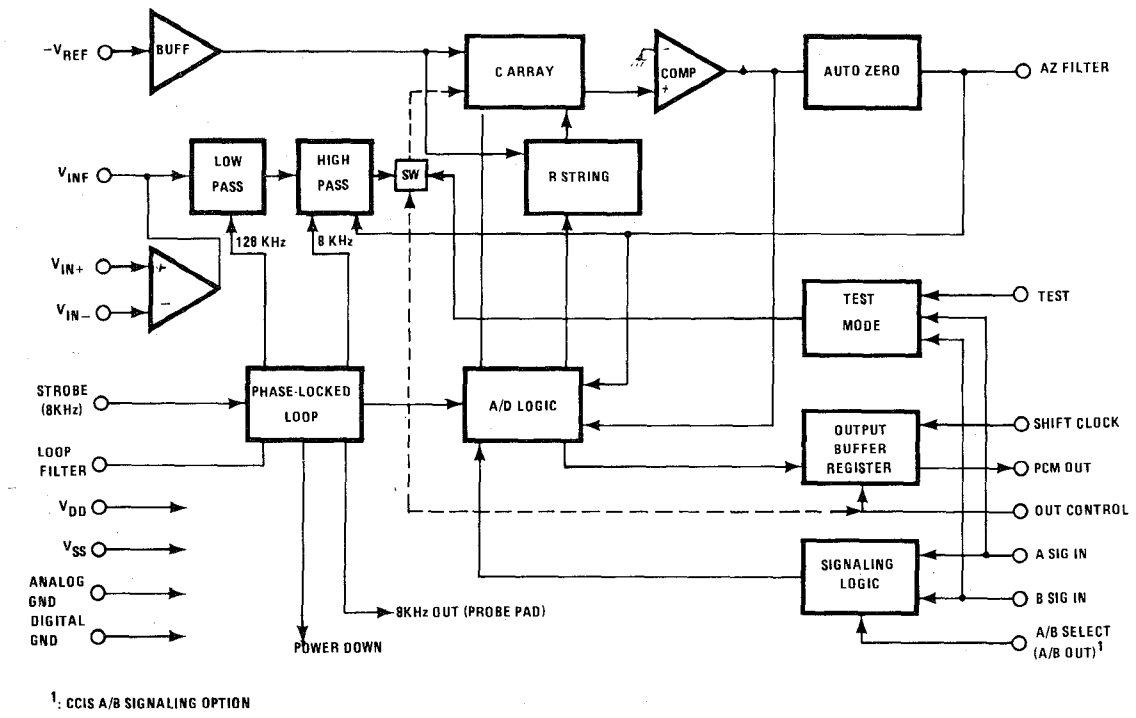
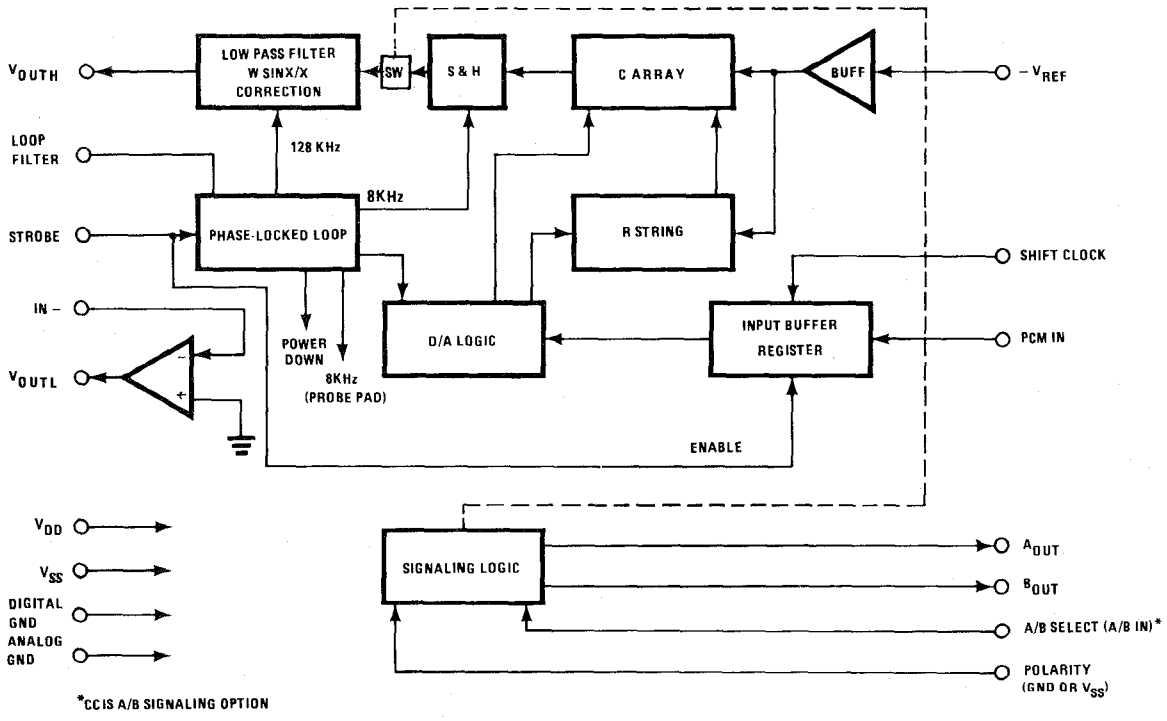


S3501 ENCODER WITH FILTER BLOCK DIAGRAM (18 PIN PKG)

(a)



S3502 DECODER WITH FILTER BLOCK DIAGRAM (16 PIN PKG)

(b)

Fig. 1. (a) Block diagram for the transmit chip. (b) Block diagram for the receive chip.

sence of the 8 kHz strobe by driving a power-on reset (POR) circuit. The converted 8 bit PCM word is shifted out by a shift clock using a tristate output driver. This facilitates tying the PCM outputs of multiplexed CODEC's on a time shared bus. Th

conversion. The output of the decoder is sampled and held and introduced into a switched-capacitor active low-pass reconstruction filter. A separate uncommitted-low output-impedance operational amplifier is provided in this chip capable of

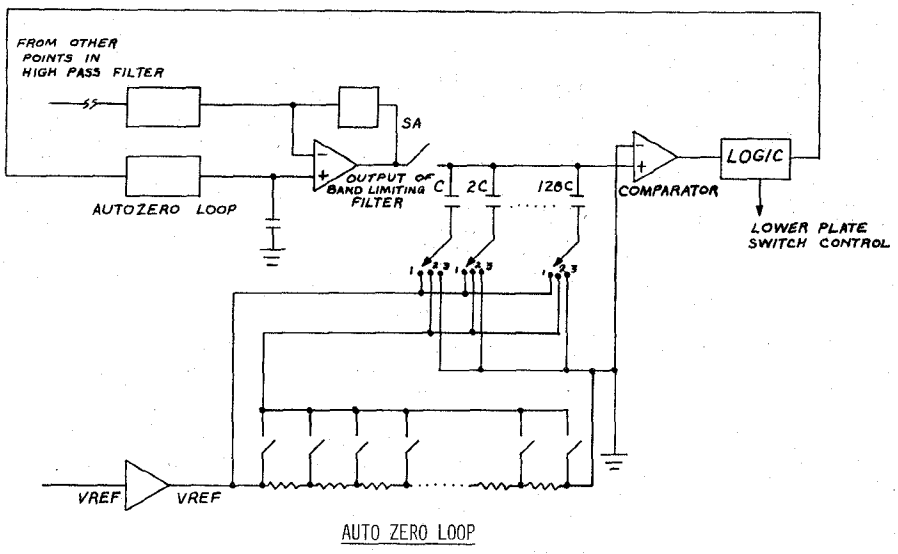


Fig. 2. Block diagram representation of the key section of A/D.

tion the operational amplifier can be effectively turned off to save power.

Both chips include functions required for supervision and signaling in telephone systems. Both in band signaling (where the LSB of the processed word is replaced every sixth frame by *A* signal and *B* signal inputs) and common channel interoffice signaling (CCIS) schemes (where a separate signaling highway exists) are implemented. In addition, noninverted and inverted (for relay drive applications) signaling options are available.

The use of the PLL makes the system very flexible, since the 8 kHz strobe (an internationally accepted standard) fixes all internal timing independent of the shift clock rate which is used to shift out the converted PCM data. The shift clock rate of the chip can be arbitrary to 3.1 MHz. The architecture of these chips was aimed at minimizing overall cost of the system where the CODEC will be used. This was achieved by integrating the described features and by making the chip requirements flexible. Hence, the operating power supplies are allowed to vary from ±4.75 to ±7.5 V. In addition, only one common reference is required which can be shared among several CODEC's (i.e., 24 or 32 in a channel bank). This is achieved by buffering the reference on-chip. Also power supply and reference voltage decoupling were kept minimal (i.e., 0.1 μF capacitor). The use of the PLL (which eliminates the need for extra clock inputs) and the use of multiplexing on certain pins enabled the chips to be packaged in an 18 pin (16 pins for the receive chip) 300 mil wide package. The narrow packages have lower cost, are machine insertable, and result in a compact printed circuit board layout. To fit the package, the chip dimensions were tailored to be narrow on one side.

IV. Circuit Design

A. A/D and D/A Conversion Schemes

The CODEC design is based on charge redistribution in a binary weighted array of capacitors [2]. In the present work, a capacitor array is used to define the decision levels corresponding to the end points of the companding segments. To generate the linearly spaced decision levels within the segments, however, a resistor array is used instead of another capacitor array and buffer amplifier. Use of a resistor array for this application has been reported in previous work [3]. However, the configuration of the array used here is different.

The design approach to be described here differs from other designs based on the charge redistribution principle in that it uses state sequencing of switches to achieve data conversion of bipolar signals with a single polarity reference. This is achieved by switching the capacitors in the capacitor array from analog ground to V_{ref} (reference voltage) for a $+V_{ref}$ increment, and from V_{ref} to analog ground for a $-V_{ref}$ increment. Apart from the fact that only one reference is needed, this scheme has the advantage that the two reference swings achieved at the capacitor array are identical in magnitude, i.e., no mismatch occurs.

Fig. 2. shows a simplified schematic of the analog portion of the transmit circuit. Initially, the input analog voltage from the band-limiting filter is sampled on the top plate of the capacitor array with the bottom plate being connected to V_{ref} (normally -3 V). This corresponds to position 1 for the lower plate switches. The sign of the signal is then determined and if the signal is positive the lower plates are connected to position 3 (i.e., ground) with switch S_A still being on. If the signal is negative, the lower plates are left connected in position 1 and switch S_A is turned off. The segment bits (i.e., chords) are found by a sequential technique where, starting with the smallest capacitor, the voltage on the lower plate of the array is changed by $-V_{ref}$ (for a negative signal) by switching the lower plate connection from position 1 to 3, or by $+V_{ref}$ (for a positive signal) by changing the lower plate switch from position 3 to 1 until the comparator changes sign. This determines the chord. The linear resistor string with 32 taps is then used to present $(V_{ref}/32)$ k V ($k = 0$ to 32) to the lower plate of one capacitor (selected by the sequential search for the chords) in the capacitor array. A successive approximation technique is then used to determine the 4 bits corresponding to the linear division of the chords (this technique was not used for the

chords because for coding of the smallest signal more than one capacitor needs to be switched simultaneously, as opposed to only one in the sequential scheme, thus increasing the risk of disturbing the sensing node during a critical phase of the conversion). The decoder uses similar principles to achieve the data conversion. The linear resistor string has 32 equal taps on the transmit chip to implement the half-step shift adjacent to the origin. In the decoder, 32 equal taps are used to implement half-step shifts corresponding to the signaling frames (where the LSB of the processed word is replaced by signaling bits) and information frames (where the unaltered 8 bit PCM word is available).

B. Offset Compensation

In order to meet stringent system requirements, it is necessary to cancel any offset voltage in the encoder. The offset is caused by comparator and filter offset voltages and by clock feedthrough on the top plates of the capacitor array through the parasitic capacitance of the switch driving it. Offset cancellation is achieved by integrating the PCM sign bit (using an on-chip resistor and an external capacitor) and feeding back the result into the last stage of the high-pass filter, as shown in Fig. 2. The time constant of the auto zero loop is several seconds. For faster acquisition of offsets immediately after power-up, a dual bandwidth loop was implemented. The auto zero loop is powered up immediately on application of the strobe signal. The loop starts with a large bandwidth by selecting a smaller on-chip integrating resistance. The PLL in the meantime acquires lock and drives a POR circuit to enable the chip. As soon as the chip is enabled, the auto zero loop switches to a lower bandwidth. This feature not only improves circuit performance immediately after power-up but also eases automated testing of these chips.

C. Operational Amplifiers

The transmit and receive chips required 20 operational amplifiers, out of which three had to have low-impedance outputs capable of driving 600 Ω loads. Due to the large number of amplifiers, the power dissipation of each amplifier had to be minimized. In addition, due to the large mix of digital and analog circuitry, the power supply rejection had to be acceptable to limit noise from power supply lines getting coupled onto analog signal paths.

Figs. 3 and 4 show the schematic of a high and low output impedance operational amplifier. A key feature of the circuits is the class A-B operation of the output stage which results in significantly reduced power dissipation and higher open loop gain. Further reduction in power dissipation is obtained by using a frequency compensation scheme which does not use a buffer amplifier (normally used to prevent the feedforward of the signal through the compensation capacitor which creates a low-frequency zero in the transfer function [4]). Instead, the compensation capacitor is introduced through a resistor (using $Q10$, $Q11$). This creates a zero in the position of the second dominant pole and helps stabilize the amplifier. In principle, the operational amplifier can be stabilized using C_1 only. Use of C_2 along with C_1, however, improves the power supply rejection ratio (PSRR) as follows: node 1 (in Fig. 3) is a high-

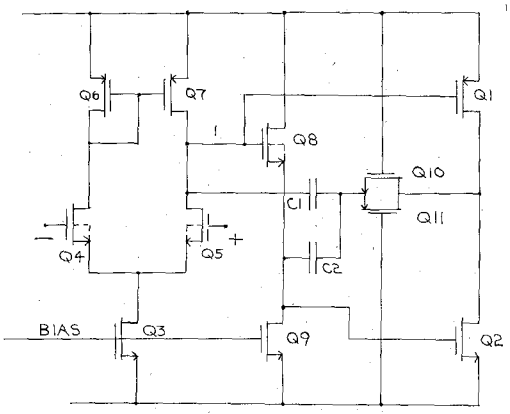


Fig. 3. Schematic of high-output impedance operational amplifier.

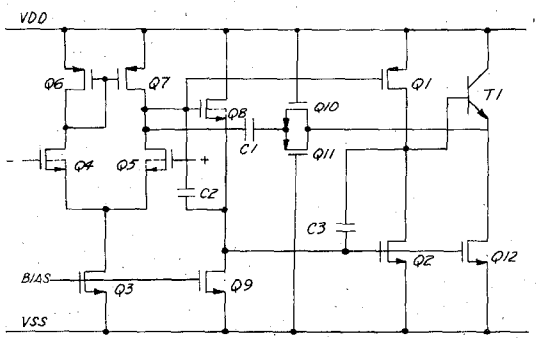


Fig. 4. Schematic of the low-output impedance operational amplifier.

impedance point and any noise on V_{DD} appears essentially unattenuated on it at low frequencies. Thus, at low frequencies transistor Q_1 does not amplify any noise on V_{DD} (due to essentially zero gate source noise voltage). At higher frequencies, however, node 1 starts rolling off due to the pole created by C_1, thus creating an increasing gate source noise voltage and thus noise amplification into the amplifier through Q_1. This effect can be alleviated by making C_1 smaller. Use of C_2 makes this possible. Table I shows the performance data for the high output impedance operational amplifier. The low output impedance operational amplifier has similar performance, except that the minimum open loop gain is 60 dB and the power dissipation is higher (approximately 20 mW).

D. Comparator

The comparator used in the transmit chip is capable of resolving 300 μV in less than 2 μs. It consists of (Fig. 5) a diode clamped preamplifier (Q_{13}, Q_{14}, Q_{15}, Q_{16}, Q_{17}) driving another differential amplifier stage (Q_3, Q_4, Q_5, Q_6, Q_7) which drives the output gain stage (Q_{10}, Q_{11}, Q_{12}). The output of a nondiode clamped differential stage undergoes large voltage excursions and under sufficient input voltage it drives the output devices out of the saturation region of operation. Therefore, in switching from one state to another, the comparator initially starts with a low gain resulting in a slow response time. Diode clamps on the output nodes (node 2) limits the voltage excursion of the output nodes and thus improves the transient response. The stage was broad-banded by using source follower buffers (Q_{18}, Q_{19}, Q_{20}, Q_{21}) to drive the second stage (the input capacitance of this stage is large due to the Miller multiplication of the gate drain overlap capacitance).

TABLE I
HIGH-OUTPUT IMPEDANCE OPERATIONAL AMPLIFIER

Low Frequency Gain	= 90dB
Unity Gain Bandwidth	= 2.5MHz
Offset Voltage	= 10mv (standard deviation) = +0.4mv (mean)
CMRR	= 73dB
PSRR	= 70dB (DC) to VSS / 76dB (DC), 74dB (3.16KHz) to VSS 68dB (DC) to VDD / 74dB (DC), 67dB (3.16KHz) to VDD (measured) (computer simulation)
Slew Rate	= 2V/μsec
Power Dissipation	= 1.6mW
Noise	= 26μV rms (integrated over a band 10Hz-1MHz.)
Area	= 270mil^2

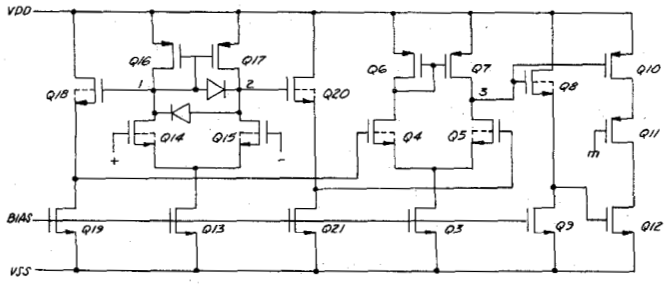


Fig. 5. Schematic of comparator used in the transmit chip.

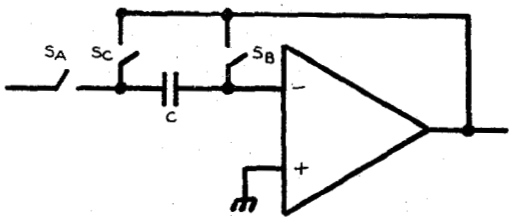


Fig. 6. Offset canceled reference buffer.

The second differential amplifier has a cascoded gain stage for its load. This reduces Miller multiplication of the gate capacitance of Q_{10}, as seen on node 3. A push-pull drive has been implemented for the output stage to reduce power dissipation and increase gain. The comparator has an open loop gain greater than 120 dB with a bandwidth of 25 MHz.

E. Reference Buffer

An on-chip reference buffer is required for both chips to reduce decoupling and current supply requirements of the external reference (which can be common to many CODEC's). The offset voltage of this reference buffer is canceled to eliminate gain variation in the channel. This is accomplished by using the circuit shown on Fig. 6. Initially, switches S_A and S_B are turned on and the reference voltage is sampled onto one plate of the capacitor C, with the offset of the amplifier being stored on the other plate. Next, S_A and S_B are turned off and S_C is turned on. This forces the output to be equal to the reference voltage. Clock feedthrough does not have any effect since the feedthrough is not signal dependent (the refer-

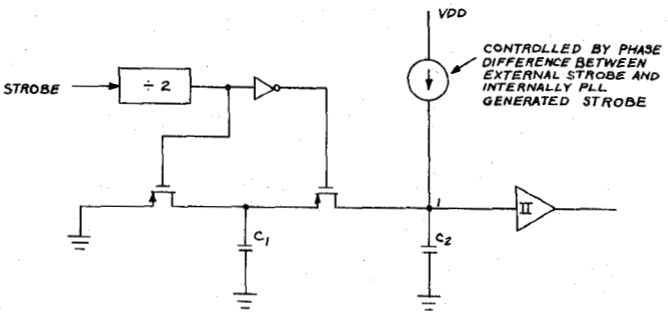


Fig. 7. Schematic of power-on reset circuit.

F. PLL and POR Circuitry

The PLL consists of an edge sensitive phase detector, a loop filter (lead-lag), a voltage-controlled oscillator (VCO), and a divider chain. The loop filter uses on-chip resistors and an external capacitor. The loop filter has dual bandwidth. During the power-up period the loop filter starts with a small time-constant, thus enabling the PLL to achieve lock in less than 20 ms. In normal operation, however, the loop switches to a narrow bandwidth filter to reduce phase jitter.

A POR circuit controls the power-up/down function on both chips, and is shown in Fig. 7. In the absence of the strobe signal, the lock detector in the PLL turns on a current source and charges the capacitor C_2 to V_{DD}, and forces the Schmitt trigger to V_{DD}. In the presence of the strobe this capacitor is discharged to ground through S_A and S_B which eventually powers up the circuit by forcing the Schmitt trigger output to ground. Capacitors C_1, C_2 act as an RC filter with the time constant given by $(C_1/C_2)\,T$, where T is the clocking period. The time constant of the POR is selected to allow sufficient time for the PLL to acquire lock before the circuit is powered up.

G. Signaling

Two different types of signaling functions have been incorporated. In the common channel interoffice signaling (CCIS) scheme, a separate signaling highway is created. Two bits (A_{sig}, B_{sig}) are multiplexed on this line and transmitted every frame. In the inband signaling scheme implemented, the

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