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Washington, D.C. 20231

Box Patent Application

Re: U.S. Non-Provisional Utility Patent Application under 37 C.F.R. § 1.53(b)
Appl. No. To be assigned; Filed: August 4, 2000
For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations**
Inventors: David F. Sorrells, Michael J. Bultman, Robert W. Cook, Richard C. Looke, Charley D. Moses, Jr., Gregory S. Rawlins, and Michael W. Rawlins
Our Ref: 1744.0630003

Sir:

The following documents are forwarded herewith for appropriate action by the U.S. Patent and Trademark Office:

1. USPTO Utility Patent Application Transmittal Form PTO/SB/05;

2. U.S. Utility Patent Application entitled:

   Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations

   and naming as inventors:

   David F. Sorrells, Michael J. Bultman, Robert W. Cook, Richard C. Looke, Charley D. Moses, Jr., Gregory S. Rawlins, and Michael W. Rawlins

the application comprising:

a. specification containing:

i. 98 pages of description prior to the claims;

ii. 7 pages of claims (40 claims);

iii. a one (1) page abstract;

b. Two-hundred and eight (208) sheets of drawings: (Figures 1A-D, 2A, 2B, 3-14, 15A-F, 16-19, 20A, 20A-1, 20B-F, 21, 22A-F, 23A, 24A-J, 25-45, 46A, 46B, 47, 48, 49A, 49B,50, 51, 52A-C, 53-55, 56A, 56B, 57-60, 61A, 61B, 62-66, 67A, 67B, 68A, 68B, 69A, 69B, 70A-S, 71A-D, 72A-J, 73A, 73B, 74, 75A-C, 76A, 76B, 77, 78, 79A-D, 80, 81A-C, 82-88, 89A-E, 90A-D, 91-94, 95A-C, 96-161);

3. 37 C.F.R. § 1.136(a)(3) Authorization to Treat a Reply As Incorporating An Extension of Time (in duplicate); and

4. Two (2) return postcards.

It is respectfully requested that, of the two attached postcards, one be stamped with the filing date of these documents and returned to our courier, and the other, prepaid postcard, be stamped with the filing date and unofficial application number and returned as soon as possible.

This patent application is being submitted under 37 C.F.R. § 1.53(b) without Declaration and without filing fee.

This application claims priority to U.S. Provisional Application No. 60/147,129, filed August 4, 1999; U.S. Application No. 09/525,615, filed on March 14, 2000; and U.S. Application No. 09/526,041, filed on March 14, 2000.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR § 1.53(b))

Attorney Docket No	*1744.0630003*
First Inventor or Application Identifier	*David F. Sorrells*
Title	*Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations*
Express Mail Label No.	

JC882 U.S. PTO 09/632056 08/04/00

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO. Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☐ * Fee Transmittal Form (*e.g.*, PTO/SB/17)
(Submit an original, and a duplicate for fee processing)
2. ☒ Specification [Total Pages 106]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings *(if filed)*
- Detailed Description
- Claim(s)
- Abstract of the Disclosure
3. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets 208]
4. ☐ Oath or Declaration [Total Pages ____]
   a. ☐ Newly executed (original or copy)
   b. ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)*
   [Note Box 5 below]
      i. ☐ DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR §§ 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation By Reference *(useable if Box 4b is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. ☐ Computer Readable Copy
   b. ☐ Paper Copy (identical to computer copy)
   c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ☐ Assignment Papers (cover sheet & document(s))
9. ☐ 37 CFR 3.73(b) Statement (when there is an assignee) ☐ Power of Attorney
10. ☐ English Translation Document *(if applicable)*
11. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
14. ☐ *Small Entity Statement(s) *(PTO/SB/09-12)* ☐ Statement filed in prior application, Status still proper and desired
15. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)
16. ☒ Other: 37 C F R. § 1.136(a)(3) Authorization
☐ Other:

**NOTE FOR ITEMS 1 & 14 IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. §1.28)*

17. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment:*

☐ Continuation ☐ Divisional ☐ Continuation-in-Part (CIP) of prior application No: ____/____________

Prior application information: *Examiner* ____________ *Group/Art Unit:* ____________

18. CORRESPONDENCE ADDRESS

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Burden Hour Statement this form is estimated to take 0.2 hours to complete Time will vary depending upon the needs of the individual case Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

SKGF Rev 8/99 ...

Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations

David F. Sorrells
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Robert W. Cook
Richard C. Looke
Charley D. Moses, Jr.
Gregory S. Rawlins
Michael W. Rawlins

This application claims the benefit of the following: U.S. Provisional Application No.60/147,129, filed on August 4, 1999; U.S. Application No. 09/525,615, filed on March 14, 2000; and U.S. Application No. 09/526,041, filed on March 14, 2000, all of which are incorporated herein by reference in their entireties.

Cross-Reference to Other Applications

The following applications of common assignee are related to the present application, and are herein incorporated by reference in their entireties:

"Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed October 21, 1998, issued as U.S. Patent No. 6,061,551 on May 9, 2000.

"Method and System for Down-Converting Electromagnetic Signals Having Optimized Switch Structures," Ser. No. 09/293,095, filed April 16, 1999.

"Method and System for Down-Converting Electromagnetic Signals Including Resonant Structures for Enhanced Energy Transfer," Ser. No. 09/293,342, filed April 16, 1999.

"Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, filed October 21, 1998, issued as U.S. Patent No. 6,091,940 on July 18, 2000.

"Method and System for Frequency Up-Conversion Having Optimized Switch Structures," Ser. No. 09/293,097, filed April 16, 1999.

"Method and System for Ensuring Reception of a Communications Signal," Ser. No. 09/176,415, filed October 21, 1998, issued as U.S. Patent No. 6,061,555 on May 9, 2000.

"Integrated Frequency Translation And Selectivity,"Ser. No. 09/175,966, filed October 21, 1998, issued as U.S. Patent No. 6,049,706 on April 11, 2000.

"Integrated Frequency Translation and Selectivity with a Variety of Filter Embodiments," Ser. No. 09/293,283, filed April 16, 1999.

"Applications of Universal Frequency Translation," Ser. No. 09/261,129, filed March 3, 1999.

"Method and System for Down-Converting an Electromagnetic Signal, Transforms For Same, and Aperture Relationships", Ser. No. 09/550,644, filed on April 14, 2000.

"Wireless Local Area Network (WLAN) Technology and Applications Including Techniques of Universal Frequency Translation", Attorney Docket No. 1744.0630002, filed on August 4, 2000.

Background of the Invention

Field of the Invention

The present invention is generally related to wireless local area networks (WLANs), and more particularly, to WLANs that utilize universal frequency translation technology for frequency translation, and applications of same.

Related Art

Wireless LANs exist for receiving and transmitting information to/from mobile terminals using electromagnetic (EM) signals. Conventional wireless communications circuitry is complex and has a large number of circuit parts. This complexity and high parts count increases overall cost. Additionally, higher part counts result in higher power consumption, which is undesirable, particularly in battery powered wireless units. Additionally, various communication components exist for performing frequency down-conversion, frequency up-conversion, and filtering. Also, schemes exist for signal reception in the face of potential jamming signals.

Summary of the Invention

The present invention is directed to a wireless local area network (WLAN) that includes one or more WLAN devices (also called stations, terminals, access points, client devices, or infrastructure devices) for effecting wireless communications over the WLAN. The WLAN device includes at least an antenna, a receiver, and a transmitter for effecting wireless communications over the WLAN. Additionally, the WLAN device may also include a LNA/PA module, a control signal generator, a demodulation/modulation facilitation module, and a media access control (MAC) interface. The WLAN receiver includes at least one universal frequency translation module that frequency down-converts a received electromagnetic (EM) signal. In embodiments, the UFT based receiver is configured in a multi-phase embodiment to reduce or eliminate re-radiation that is caused by DC offset. The WLAN transmitter includes at least one universal frequency translation module that frequency up-converts a baseband signal in preparation for transmission over the WLAN. In embodiments, the UFT based transmitter is configured in a differential and/or multi-phase embodiment to reduce carrier insertion and spectral growth in the transmitted signal.

WLANs exhibit multiple advantages by using UFT modules for frequency translation. These advantages include, but are not limited to: lower power consumption, longer battery life, fewer parts, lower cost, less tuning, and more effective signal transmission and reception. These advantages are possible because the UFT module enables direct frequency conversion in an efficient manner with minimal signal distortion.

The structure and operation of embodiments of the UFT module, and various applications of the same are described in detail in the following sections.

Further features and advantages of the invention, as well as the structure and operation of various embodiments of the invention, are described in detail below with reference to the accompanying drawings. The drawing in which an element first appears is typically indicated by the leftmost character(s) and/or digit(s) in the corresponding reference number.

Brief Description of the Figures

The present invention will be described with reference to the accompanying drawings, wherein:

FIG. 1A is a block diagram of a universal frequency translation (UFT) module according to an embodiment of the invention;

FIG. 1B is a more detailed diagram of a universal frequency translation (UFT) module according to an embodiment of the invention;

FIG. 1C illustrates a UFT module used in a universal frequency down-conversion (UFD) module according to an embodiment of the invention;

FIG. 1D illustrates a UFT module used in a universal frequency up-conversion (UFU) module according to an embodiment of the invention;

FIG. 2A-2B illustrate block diagrams of universal frequency translation (UFT) modules according to an embodiment of the invention;

FIG. 3 is a block diagram of a universal frequency up-conversion (UFU) module according to an embodiment of the invention;

FIG. 4 is a more detailed diagram of a universal frequency up-conversion (UFU) module according to an embodiment of the invention;

FIG. 5 is a block diagram of a universal frequency up-conversion (UFU) module according to an alternative embodiment of the invention;

FIGS. 6A-6I illustrate example waveforms used to describe the operation of the UFU module;

FIG. 7 illustrates a UFT module used in a receiver according to an embodiment of the invention;

FIG. 8 illustrates a UFT module used in a transmitter according to an embodiment of the invention;

FIG. 9 illustrates an environment comprising a transmitter and a receiver, each of which may be implemented using a UFT module of the invention;

FIG. 10 illustrates a transceiver according to an embodiment of the invention;

FIG. 11 illustrates a transceiver according to an alternative embodiment of the invention;

FIG. 12 illustrates an environment comprising a transmitter and a receiver, each of which may be implemented using enhanced signal reception (ESR) components of the invention;

FIG. 13 illustrates a UFT module used in a unified down-conversion and filtering (UDF) module according to an embodiment of the invention;

FIG. 14 illustrates an example receiver implemented using a UDF module according to an embodiment of the invention;

FIGS. 15A-15F illustrate example applications of the UDF module according to embodiments of the invention;

FIG. 16 illustrates an environment comprising a transmitter and a receiver, each of which may be implemented using enhanced signal reception (ESR) components of the invention, wherein the receiver may be further implemented using one or more UFD modules of the invention;

FIG. 17 illustrates a unified down-converting and filtering (UDF) module according to an embodiment of the invention;

FIG. 18 is a table of example values at nodes in the UDF module of FIG. 19;

FIG. 19 is a detailed diagram of an example UDF module according to an embodiment of the invention;

FIGS. 20A and 20A-1 are example aliasing modules according to embodiments of the invention;

FIGS. 20B-20F are example waveforms used to describe the operation of the aliasing modules of FIGS. 20A and 20A-1;

FIG. 21 illustrates an enhanced signal reception system according to an embodiment of the invention;

FIGS. 22A-22F are example waveforms used to describe the system of FIG. 21;

FIG. 23A illustrates an example transmitter in an enhanced signal reception system according to an embodiment of the invention;

FIGS. 23B and 23C are example waveforms used to further describe the enhanced signal reception system according to an embodiment of the invention;

FIG. 23D illustrates another example transmitter in an enhanced signal reception system according to an embodiment of the invention;

FIGS. 23E and 23F are example waveforms used to further describe the enhanced signal reception system according to an embodiment of the invention;

FIG. 24A illustrates an example receiver in an enhanced signal reception system according to an embodiment of the invention;

FIGS. 24B-24J are example waveforms used to further describe the enhanced signal reception system according to an embodiment of the invention;

FIG. 25 illustrates a block diagram of an example computer network;

FIG. 26 illustrates a block diagram of an example computer network;

FIG. 27 illustrates a block diagram of an example wireless interface;

FIG. 28 illustrates an example heterodyne implementation of the wireless interface illustrated in FIG. 27;

FIG. 29 illustrates an example in-phase/quadrature-phase (I/Q) heterodyne implementation of the interface illustrated in FIG. 27;

FIG. 30 illustrates an example high level block diagram of the interface illustrated in FIG. 27, in accordance with the present invention;

FIG. 31 illustrates a example block diagram of the interface illustrated in FIG. 29, in accordance with the invention;

FIG. 32 illustrates an example I/Q implementation of the interface illustrated in FIG.31;

FIGS. 33-38 illustrate example environments encompassed by the invention;

FIG. 39 illustrates a block diagram of a WLAN interface according to an embodiment of the invention;

FIG. 40 illustrates a WLAN receiver according to an embodiment of the invention;

FIG. 41 illustrates a WLAN transmitter according to an embodiment of the invention;

FIGS. 42-44 are example implementations of a WLAN interface;

FIGS. 45, 46A, and 46B relate to an example MAC interface for an example WLAN interface embodiment;

FIGS. 47, 48, 49A, and 49B relate to an example demodulator/modulator facilitation module for an example WLAN interface embodiment;

FIGS. 50, 51, 52A, 52B, and 52C relate to an example alternate demodulator/modulator facilitation module for an example WLAN interface embodiment;

FIGS. 53 and 54 relate to an example receiver for an example WLAN interface embodiment;

FIGS. 55, 56A, and 56B relate to an example synthesizer for an example WLAN interface embodiment;

FIGS. 57, 58, 59, 60, 61A, and 61B relate to an example transmitter for an example WLAN interface embodiment;

FIGS. 62 and 63 relate to an example motherboard for an example WLAN interface embodiment;

FIGS. 64-66 relate to example LNAs for an example WLAN interface embodiment;

FIGS. 67A-B illustrate IQ receivers having UFT modules in a series and shunt configurations, according to embodiments of the invention;

FIGS. 68A-B illustrate IQ receivers having UFT modules with delayed control signals for quadrature implementation, according to embodiments of the present invention;

FIGS. 69A-B illustrate IQ receivers having FET implementations, according to embodiments of the invention;

FIG. 70A illustrates an IQ receiver having shunt UFT modules according to embodiments of the invention;

FIG. 70B illustrates control signal generator embodiments for receiver 7000 according to embodiments of the invention;

FIGS. 70C-D illustrate various control signal waveforms according to embodiments of the invention;

FIG. 70E illustrates an example IQ modulation receiver embodiment according to embodiments of the invention;

FIGS. 70F-P illustrate example waveforms that are representative of the IQ receiver in FIG. 70E;

FIGS. 70Q-R illustrate single channel receiver embodiments according to embodiments of the invention;

FIG. 70S illustrates a FET configuration of an IQ receiver embodiment according to embodiments of the invention;

FIG. 71A illustrate a balanced transmitter 7102, according to an embodiment of the present invention;

FIGs. 71B-C illustrate example waveforms that are associated with the balanced transmitter 7102, according to an embodiment of the present invention;

FIG. 71D illustrates example FET configurations of the balanced transmitter 7102, according to embodiments of the present invention;

FIGs. 72A-I illustrate various example timing diagrams that are associated with the transmitter 7102, according to embodiments of the present invention;

FIG. 72J illustrates an example frequency spectrum that is associated with a modulator 7104, according to embodiments of the present invention;

FIG. 73A illustrate a transmitter 7302 that is configured for carrier insertion, according to embodiments of the present invention;

FIG. 73B illustrates example signals associated with the transmitter 7302, according to embodiments of the invention;

FIG. 74 illustrates an IQ balanced transmitter 7420, according to embodiments of the present invention;

FIGs. 75A-C illustrate various example signal diagrams associated with the balanced transmitter 7420 in FIG. 74;

FIG. 76A illustrates an IQ balanced transmitter 7608 according to embodiments of the invention;

FIG. 76B illustrates an IQ balanced modulator 7618 according to embodiments of the invention;

FIG. 77 illustrates an IQ balanced modulator 7702 configured for carrier insertion according to embodiments of the invention;

FIG. 78 illustrates an IQ balanced modulator 7802 configured for carrier insertion according to embodiments of the invention;

FIG. 79A illustrate a transmitter 7900, according to embodiments of the present invention;

FIGs. 79B-C illustrate various frequency spectrums that are associated with the transmitter 7900;

FIG. 79D illustrates a FET configuration for the transmitter 7900, according to embodiments of the present invention;

FIG. 80 illustrates an IQ transmitter 8000, according to embodiments of the present invention;

FIGs. 81A-C illustrate various frequency spectrums that are associated with the IQ transmitter 8000, according to embodiments of the present invention;

FIG. 82 illustrates an IQ transmitter 8200, according to embodiments of the present invention;

FIG. 83 illustrates an IQ transmitter 8300, according to embodiments of the invention;

FIG. 84 illustrates a flowchart 8400 that is associated with the transmitter 7102 in the FIG. 71A, according to embodiments of the invention;

FIG. 85 illustrates a flowchart 8500 that further defines the flowchart 8400 in the FIG. 84, and is associated with the transmitter 7102 according to embodiments of the invention;

FIG. 86 illustrates a flowchart 8600 that is associated with the transmitter 7900 and further defines the flowchart 8400 in the FIG. 84, according to embodiments of the invention;

FIG. 87 illustrates a flowchart 8700, that is associated with the transmitter 7420 in the FIG. 74, according to embodiments of the invention;

FIG. 88 illustrates a flowchart 8800 that is associated with the transmitter 8000, according to embodiments of the invention;

FIG. 89A illustrate a pulse generator according to embodiments of the invention;

FIGS. 89B-C illustrate various example signal diagrams associated with the pulse generator in FIG. 89A, according to embodiments of the invention;

FIG. 89D-E illustrate various example pulse generators according to embodiments of the present invention;

FIGS. 90A-D illustrates various implementation circuits for the modulator 7410, according to embodiments of the present invention;

FIG. 91 illustrates an IQ transceiver 9100 according to embodiments of the present invention;

FIG. 92 illustrates direct sequence spread spectrum according to embodiments of the present invention;

FIG. 93 illustrates the LNA/PA module 3904 according to embodiments of the present invention;

FIG. 94 illustrates a WLAN device 9400, according to embodiments of the invention of the present invention; and

FIGs. 95A-C, and FIGs. 96-161 illustrate schematics for an integrated circuit implementation example of the present invention.

Detailed Description of the Preferred Embodiments

Table of Contents

1. Universal Frequency Translation

The present invention is related to frequency translation, and applications of same. Such applications include, but are not limited to, frequency down-conversion, frequency up-conversion, enhanced signal reception, unified down-conversion and filtering, and combinations and applications of same.

FIG. 1A illustrates a universal frequency translation (UFT) module 102 according to embodiments of the invention. (The UFT module is also sometimes called a universal frequency translator, or a universal translator.)

As indicated by the example of FIG. 1A, some embodiments of the UFT module 102 include three ports (nodes), designated in FIG. 1A as Port 1, Port 2, and Port 3. Other UFT embodiments include other than three ports.

Generally, the UFT module 102 (perhaps in combination with other components) operates to generate an output signal from an input signal, where the frequency of the output signal differs from the frequency of the input signal. In other words, the UFT module 102 (and perhaps other components) operates to generate the output signal from the input signal by translating the frequency (and perhaps other characteristics) of the input signal to the frequency (and perhaps other characteristics) of the output signal.

An example embodiment of the UFT module 103 is generally illustrated in FIG. 1B. Generally, the UFT module 103 includes a switch 106 controlled by a control signal 108. The switch 106 is said to be a controlled switch.

As noted above, some UFT embodiments include other than three ports. For example, and without limitation, FIG. 2 illustrates an example UFT module 202. The example UFT module 202 includes a diode 204 having two ports, designated as Port 1 and Port 2/3. This embodiment does not include a third port, as indicated by the dotted line around the "Port 3" label.

The UFT module is a very powerful and flexible device. Its flexibility is illustrated, in part, by the wide range of applications in which it can be used. Its power is illustrated, in part, by the usefulness and performance of such applications.

For example, a UFT module 115 can be used in a universal frequency down-conversion (UFD) module 114, an example of which is shown in FIG. 1C. In this capacity, the UFT module 115 frequency down-converts an input signal to an output signal.

As another example, as shown in FIG. 1D, a UFT module 117 can be used in a universal frequency up-conversion (UFU) module 116. In this capacity, the UFT module 117 frequency up-converts an input signal to an output signal.

These and other applications of the UFT module are described below. Additional applications of the UFT module will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. In some applications, the UFT module is a required component. In other applications, the UFT module is an optional component.

2. Frequency Down-Conversion

The present invention is directed to systems and methods of universal frequency down-conversion, and applications of same.

In particular, the following discussion describes down-converting using a Universal Frequency Translation Module. The down-conversion of an EM signal by aliasing the EM signal at an aliasing rate is fully described in co-pending U.S. Patent Application entitled "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed October 21, 1998, issued as U.S. Patent No. 6,061,551 on May 9, 2000, the full disclosure of which is incorporated herein by reference. A relevant portion of the above mentioned patent application is summarized below to describe down-converting an input signal to produce a down-converted signal that exists at a lower frequency or a baseband signal.

FIG. 20A illustrates an aliasing module 2000 (also called a universal frequency down-conversion module) for down-conversion using a universal frequency translation (UFT) module 2002 which down-converts an EM input signal 2004. In particular embodiments, aliasing module 2000 includes a switch 2008 and a capacitor 2010. The electronic alignment of the circuit components is flexible. That is, in one implementation, the switch 2008 is in series with input signal 2004 and capacitor 2010 is shunted to ground (although it may be other than ground in configurations such as differential mode). In a second implementation (see FIG. 20A-1), the capacitor 2010 is in series with the input signal 2004 and the switch 2008 is shunted to ground (although it may be other than ground in configurations such as differential mode). Aliasing module 2000 with UFT module 2002 can be easily tailored to down-convert a wide variety of electromagnetic signals using aliasing frequencies that are well below the frequencies of the EM input signal 2004.

In one implementation, aliasing module 2000 down-converts the input signal 2004 to an intermediate frequency (IF) signal. In another implementation, the aliasing module 2000 down-converts the input signal 2004 to a demodulated baseband signal. In yet another implementation, the input signal 2004 is a frequency modulated (FM) signal, and the aliasing module 2000 down-converts it to a non-FM signal, such as a phase modulated (PM) signal or an amplitude modulated (AM) signal. Each of the above implementations is described below.

In an embodiment, the control signal 2006 includes a train of pulses that repeat at an aliasing rate that is equal to, or less than, twice the frequency of the input signal 2004. In this embodiment, the control signal 2006 is referred to herein as an aliasing signal because it is below the Nyquist rate for the frequency of the input signal 2004. Preferably, the frequency of control signal 2006 is much less than the input signal 2004.

A train of pulses 2018 as shown in FIG. 20D controls the switch 2008 to alias the input signal 2004 with the control signal 2006 to generate a down-converted output signal 2012. More specifically, in an embodiment, switch 2008 closes on a first edge of each pulse 2020 of FIG. 20D and opens on a second edge of each pulse. When the switch 2008 is closed, the input signal 2004 is coupled to the capacitor 2010, and charge is transferred from the input signal to the capacitor 2010. The charge stored during successive pulses forms down-converted output signal 2012.

Exemplary waveforms are shown in FIGS. 20B-20F.

FIG. 20B illustrates an analog amplitude modulated (AM) carrier signal 2014 that is an example of input signal 2004. For illustrative purposes, in FIG. 20C, an analog AM carrier signal portion 2016 illustrates a portion of the analog AM carrier signal 2014 on an expanded time scale. The analog AM carrier signal portion 2016 illustrates the analog AM carrier signal 2014 from time t_0 to time t_1.

FIG. 20D illustrates an exemplary aliasing signal 2018 that is an example of control signal 2006. Aliasing signal 2018 is on approximately the same time scale as the analog AM carrier signal portion 2016. In the example shown in FIG. 20D, the aliasing signal 2018 includes a train of pulses 2020 having negligible apertures that tend towards zero (the invention is not limited to this embodiment, as discussed below). The pulse aperture may also be referred to as the pulse width as will be understood by those skilled in the art(s). The pulses 2020 repeat at an aliasing rate, or pulse repetition rate of aliasing signal 2018. The aliasing rate is determined as described below, and further described in co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," Application No. 09/176,022, Attorney Docket Number 1744.0010000, issued as U.S. Patent No. 6,061,551 on May 9, 2000.

As noted above, the train of pulses 2020 (i.e., control signal 2006) control the switch 2008 to alias the analog AM carrier signal 2016 (i.e., input signal 2004) at the aliasing rate of the aliasing signal 2018. Specifically, in this embodiment, the switch 2008 closes on a first edge of each pulse and opens on a second edge of each pulse. When the switch 2008 is closed, input signal 2004 is coupled to the capacitor 2010, and charge is transferred from the input signal 2004 to the capacitor 2010. The charge transferred during a pulse is referred to herein as an under-sample. Exemplary under-samples 2022 form down-converted signal portion 2024 (FIG. 20E) that corresponds to the analog AM carrier signal portion 2016 (FIG. 20C) and the train of pulses 2020 (FIG. 20D). The charge stored during successive under-samples of AM carrier signal 2014 form the down-converted signal 2024 (FIG. 20E) that is an example of down-converted output signal 2012 (FIG. 20A). In FIG. 20F, a demodulated baseband signal 2026 represents the demodulated baseband signal 2024 after filtering on a compressed time scale. As illustrated, down-converted signal 2026 has substantially the same "amplitude envelope" as AM carrier signal 2014. Therefore, FIGS. 20B-20F illustrate down-conversion of AM carrier signal 2014.

The waveforms shown in FIGS. 20B-20F are discussed herein for illustrative purposes only, and are not limiting. Additional exemplary time domain and frequency domain drawings, and exemplary methods and systems of the invention relating thereto, are disclosed in co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," Application No. 09/176,022, Attorney Docket Number 1744.0010000, issued as U.S. Patent No. 6,061,551 on May 9, 2000.

The aliasing rate of control signal 2006 determines whether the input signal 2004 is down-converted to an IF signal, down-converted to a demodulated baseband signal, or down-converted from an FM signal to a PM or an AM signal. Generally, relationships between the input signal 2004, the aliasing rate of the control signal 2006, and the down-converted output signal 2012 are illustrated below:

$$\text{(Freq. of input signal 2004)} = n\bullet\text{(Freq. of control signal 2006)} \pm \text{(Freq. of down-converted output signal 2012)}$$

For the examples contained herein, only the "+" condition will be discussed. The value of n represents a harmonic or sub-harmonic of input signal 2004 (e.g., $n = 0.5, 1, 2, 3, \ldots$).

When the aliasing rate of control signal 2006 is off-set from the frequency of input signal 2004, or off-set from a harmonic or sub-harmonic thereof, input signal 2004 is down-converted to an IF signal. This is because the under-sampling pulses occur at different phases of subsequent cycles of input signal 2004. As a result, the under-samples form a lower frequency oscillating pattern. If the input signal 2004 includes lower frequency changes, such as amplitude, frequency, phase, etc., or any combination thereof, the charge stored during associated under-samples reflects the lower frequency changes, resulting in similar changes on the down-converted IF signal. For example, to down-convert a 901 MHZ input signal to a 1 MHZ IF signal, the frequency of the control signal 2006 would be calculated as follows:

$$(\text{Freq}_{\text{input}} - \text{Freq}_{\text{IF}})/n = \text{Freq}_{\text{control}}$$

$$(901 \text{ MHZ} - 1 \text{ MHZ})/n \quad = 900/n$$

For $n = 0.5, 1, 2, 3, 4$, etc., the frequency of the control signal 2006 would be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc.

Exemplary time domain and frequency domain drawings, illustrating down-conversion of analog and digital AM, PM and FM signals to IF signals, and exemplary methods and systems thereof, are disclosed in co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," Application No. 09/176,022, Attorney Docket Number 1744.0010000, issued as U.S. Patent No. 6,061,551 on May 9, 2000.

Alternatively, when the aliasing rate of the control signal 2006 is substantially equal to the frequency of the input signal 2004, or substantially equal to a harmonic or sub-harmonic thereof, input signal 2004 is directly down-converted to a demodulated baseband signal. This is because, without modulation, the under-sampling pulses occur at the same point of subsequent cycles of the input signal 2004. As a result, the under-samples form a constant output baseband signal. If the input signal 2004 includes lower frequency changes, such as amplitude, frequency, phase, etc., or any combination thereof, the charge stored during associated under-samples reflects the lower frequency changes, resulting in similar changes on the demodulated baseband signal. For example, to directly down-convert a 900 MHZ input signal to a demodulated baseband signal (i.e., zero IF), the frequency of the control signal 2006 would be calculated as follows:

$$(\text{Freq}_{\text{input}} - \text{Freq}_{\text{IF}})/n = \text{Freq}_{\text{control}}$$
$$(900 \text{ MHZ} - 0 \text{ MHZ})/n \quad = 900 \text{ MHZ}/n$$

For $n = 0.5, 1, 2, 3, 4$, etc., the frequency of the control signal 2006 should be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc.

Exemplary time domain and frequency domain drawings, illustrating direct down-conversion of analog and digital AM and PM signals to demodulated baseband signals, and exemplary methods and systems thereof, are disclosed in the co-pending U.S. Patent

Application entitled "Method and System for Down-converting Electromagnetic Signals," Application No. 09/176,022, issued as U.S. Patent No. 6,061,551 on May 9, 2000.

Alternatively, to down-convert an input FM signal to a non-FM signal, a frequency within the FM bandwidth must be down-converted to baseband (i.e., zero IF). As an example, to down-convert a frequency shift keying (FSK) signal (a sub-set of FM) to a phase shift keying (PSK) signal (a subset of PM), the mid-point between a lower frequency F_1 and an upper frequency F_2 (that is, $[(F_1 + F_2) \div 2]$) of the FSK signal is down-converted to zero IF. For example, to down-convert an FSK signal having F_1 equal to 899 MHZ and F_2 equal to 901 MHZ, to a PSK signal, the aliasing rate of the control signal 2006 would be calculated as follows:

$$\begin{aligned} \text{Frequency of the input} &= (F_1 + F_2) \div 2 \\ &= (899 \text{ MHZ} + 901 \text{ MHZ}) \div 2 \\ &= 900 \text{ MHZ} \end{aligned}$$

Frequency of the down-converted signal = 0 (i.e., baseband)

$$\begin{aligned} (\text{Freq}_{\text{input}} - \text{Freq}_{\text{IF}})/n &= \text{Freq}_{\text{control}} \\ (900 \text{ MHZ} - 0 \text{ MHZ})/n &= 900 \text{ MHZ}/n \end{aligned}$$

For $n = 0.5, 1, 2, 3$, etc., the frequency of the control signal 2006 should be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc. The frequency of the down-converted PSK signal is substantially equal to one half the difference between the lower frequency F_1 and the upper frequency F_2.

As another example, to down-convert a FSK signal to an amplitude shift keying (ASK) signal (a subset of AM), either the lower frequency F_1 or the upper frequency F_2 of the FSK signal is down-converted to zero IF. For example, to down-convert an FSK signal having F_1 equal to 900 MHZ and F_2 equal to 901 MHZ, to an ASK signal, the aliasing rate of the control signal 2006 should be substantially equal to:

(900 MHZ - 0 MHZ)/n = 900 MHZ/*n*, or

(901 MHZ - 0 MHZ)/n = 901 MHZ/*n*.

For the former case of 900 MHZ/*n*, and for $n = 0.5, 1, 2, 3, 4$, etc., the frequency of the control signal 2006 should be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc. For the latter case of 901 MHZ/*n*, and for $n = 0.5, 1, 2, 3, 4$, etc., the frequency of the control signal 2006 should be substantially equal to 1.802 GHz, 901 MHZ, 450.5 MHZ, 300.333 MHZ, 225.25 MHZ, etc. The frequency of the down-converted AM signal is substantially equal to the difference between the lower frequency F_1 and the upper frequency F_2 (i.e., 1 MHZ).

Exemplary time domain and frequency domain drawings, illustrating down-conversion of FM signals to non-FM signals, and exemplary methods and systems thereof, are disclosed in the co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," Application No. 09/176,022, issued as U.S. Patent No. 6,061,551 on May 9, 2000.

In an embodiment, the pulses of the control signal 2006 have negligible apertures that tend towards zero. This makes the UFT module 2002 a high input impedance device. This configuration is useful for situations where minimal disturbance of the input signal may be desired.

In another embodiment, the pulses of the control signal 2006 have non-negligible apertures that tend away from zero. This makes the UFT module 2002 a lower input impedance device. This allows the lower input impedance of the UFT module 2002 to be substantially matched with a source impedance of the input signal 2004. This also improves the energy transfer from the input signal 2004 to the down-converted output signal 2012, and hence the efficiency and signal to noise (s/n) ratio of UFT module 2002.

Exemplary systems and methods for generating and optimizing the control signal 2006, and for otherwise improving energy transfer and s/n ratio, are disclosed in the co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," Application No. 09/176,022, issued as U.S. Patent No. 6,061,551 on May 9, 2000.

3. Frequency Up-Conversion

The present invention is directed to systems and methods of frequency up-conversion, and applications of same.

An example frequency up-conversion system 300 is illustrated in FIG. 3. The frequency up-conversion system 300 is now described.

An input signal 302 (designated as "Control Signal" in FIG. 3) is accepted by a switch module 304. For purposes of example only, assume that the input signal 302 is a FM input signal 606, an example of which is shown in FIG. 6C. FM input signal 606 may have been generated by modulating information signal 602 onto oscillating signal 604 (FIGS. 6A and 6B). It should be understood that the invention is not limited to this embodiment. The information signal 602 can be analog, digital, or any combination thereof, and any modulation scheme can be used.

The output of switch module 304 is a harmonically rich signal 306, shown for example in FIG. 6D as a harmonically rich signal 608. The harmonically rich signal 608 has a continuous and periodic waveform.

FIG. 6E is an expanded view of two sections of harmonically rich signal 608, section 610 and section 612. The harmonically rich signal 608 may be a rectangular wave, such as a square wave or a pulse (although, the invention is not limited to this embodiment). For ease of discussion, the term "rectangular waveform" is used to refer to waveforms that are substantially rectangular. In a similar manner, the term "square wave" refers to those waveforms that are substantially square and it is not the intent of the present invention that a perfect square wave be generated or needed.

Harmonically rich signal 608 is comprised of a plurality of sinusoidal waves whose frequencies are integer multiples of the fundamental frequency of the waveform of the harmonically rich signal 608. These sinusoidal waves are referred to as the harmonics of the underlying waveform, and the fundamental frequency is referred to as the first harmonic. FIG. 6F and FIG. 6G show separately the sinusoidal components making up the first, third, and fifth harmonics of section 610 and section 612. (Note that in theory there may be an infinite number of harmonics; in this example, because harmonically rich signal 608 is shown as a square wave, there are only odd harmonics). Three harmonics are shown simultaneously (but not summed) in FIG. 6H.

The relative amplitudes of the harmonics are generally a function of the relative widths of the pulses of harmonically rich signal 306 and the period of the fundamental frequency, and can be determined by doing a Fourier analysis of harmonically rich signal 306. According to an embodiment of the invention, the input signal 606 may be shaped to ensure that the amplitude of the desired harmonic is sufficient for its intended use (e.g., transmission).

A filter 308 filters out any undesired frequencies (harmonics), and outputs an electromagnetic (EM) signal at the desired harmonic frequency or frequencies as an output signal 310, shown for example as a filtered output signal 614 in FIG. 6I.

FIG. 4 illustrates an example universal frequency up-conversion (UFU) module 401. The UFU module 401 includes an example switch module 304, which comprises a bias signal 402, a resistor or impedance 404, a universal frequency translator (UFT) 450, and a ground 408. The UFT 450 includes a switch 406. The input signal 302 (designated as "Control Signal" in FIG. 4) controls the switch 406 in the UFT 450, and causes it to close and open. Harmonically rich signal 306 is generated at a node 405 located between the resistor or impedance 404 and the switch 406.

Also in FIG. 4, it can be seen that an example filter 308 is comprised of a capacitor 410 and an inductor 412 shunted to a ground 414. The filter is designed to filter out the undesired harmonics of harmonically rich signal 306.

The invention is not limited to the UFU embodiment shown in FIG. 4.

For example, in an alternate embodiment shown in FIG. 5, an unshaped input signal 501 is routed to a pulse shaping module 502. The pulse shaping module 502 modifies the unshaped input signal 501 to generate a (modified) input signal 302 (designated as the "Control Signal" in FIG. 5). The input signal 302 is routed to the switch module 304, which operates in the manner described above. Also, the filter 308 of FIG. 5 operates in the manner described above.

The purpose of the pulse shaping module 502 is to define the pulse width of the input signal 302. Recall that the input signal 302 controls the opening and closing of the switch 406 in switch module 304. During such operation, the pulse width of the input signal 302 establishes the pulse width of the harmonically rich signal 306. As stated above, the relative amplitudes of the harmonics of the harmonically rich signal 306 are a function of at least the pulse width of the harmonically rich signal 306. As such, the pulse width of the input signal 302 contributes to setting the relative amplitudes of the harmonics of harmonically rich signal 306.

Further details of up-conversion as described in this section are presented in pending U.S. application "Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, filed October 21, 1998, incorporated herein by reference in its entirety.

4. Enhanced Signal Reception

The present invention is directed to systems and methods of enhanced signal reception (ESR), and applications of same.

Referring to FIG. 21, transmitter 2104 accepts a modulating baseband signal 2102 and generates (transmitted) redundant spectrums 2106a-n, which are sent over communications medium 2108. Receiver 2112 recovers a demodulated baseband signal 2114 from (received) redundant spectrums 2110a-n. Demodulated baseband signal 2114 is representative of the modulating baseband signal 2102, where the level of similarity between the modulating baseband signal 2114 and the modulating baseband signal 2102 is application dependent.

Modulating baseband signal 2102 is preferably any information signal desired for transmission and/or reception. An example modulating baseband signal 2202 is illustrated in FIG. 22A, and has an associated modulating baseband spectrum 2204 and image spectrum 2203 that are illustrated in FIG. 22B. Modulating baseband signal 2202 is illustrated as an analog signal in FIG. 22a, but could also be a digital signal, or combination thereof. Modulating baseband signal 2202 could be a voltage (or current) characterization of any number of real world occurrences, including for example and without limitation, the voltage (or current) representation for a voice signal.

Each transmitted redundant spectrum 2106a-n contains the necessary information to substantially reconstruct the modulating baseband signal 2102. In other words, each redundant spectrum 2106a-n contains the necessary amplitude, phase, and frequency information to reconstruct the modulating baseband signal 2102.

FIG. 22C illustrates example transmitted redundant spectrums 2206b-d. Transmitted redundant spectrums 2206b-d are illustrated to contain three redundant spectrums for illustration purposes only. Any number of redundant spectrums could be generated and transmitted as will be explained in following discussions.

Transmitted redundant spectrums 2206b-d are centered at f_1, with a frequency spacing f_2 between adjacent spectrums. Frequencies f_1 and f_2 are dynamically adjustable in real-time as will be shown below. FIG. 22D illustrates an alternate embodiment, where redundant spectrums 2208c,d are centered on unmodulated oscillating signal 2209 at f_1 (Hz). Oscillating signal 2209 may be suppressed if desired using, for example, phasing techniques or filtering techniques. Transmitted redundant spectrums are preferably above baseband frequencies as is represented by break 2205 in the frequency axis of FIGS. 22C and 22D.

Received redundant spectrums 2110a-n are substantially similar to transmitted redundant spectrums 2106a-n, except for the changes introduced by the communications medium 2108. Such changes can include but are not limited to signal attenuation, and signal interference. FIG. 22E illustrates example received redundant spectrums 2210b-d. Received redundant spectrums 2210b-d are substantially similar to transmitted redundant spectrums 2206b-d, except that redundant spectrum 2210c includes an undesired jamming signal spectrum 2211 in order to illustrate some advantages of the present invention. Jamming signal spectrum 2211 is a frequency spectrum associated with a jamming signal. For purposes of this invention, a "jamming signal" refers to any unwanted signal, regardless of origin, that may interfere with the proper reception and reconstruction of an intended signal. Furthermore, the jamming signal is not limited to tones as depicted by spectrum 2211, and can have any spectral shape, as will be understood by those skilled in the art(s).

As stated above, demodulated baseband signal 2114 is extracted from one or more of received redundant spectrums 2210b-d. FIG. 22F illustrates example demodulated baseband signal 2212 that is, in this example, substantially similar to modulating baseband signal 2202 (FIG. 22A); where in practice, the degree of similarity is application dependent.

An advantage of the present invention should now be apparent. The recovery of modulating baseband signal 2202 can be accomplished by receiver 2112 in spite of the fact that high strength jamming signal(s) (e.g. jamming signal spectrum 2211) exist on the communications medium. The intended baseband signal can be recovered because multiple redundant spectrums are transmitted, where each redundant spectrum carries the necessary information to reconstruct the baseband signal. At the destination, the redundant spectrums are isolated from each other so that the baseband signal can be recovered even if one or more of the redundant spectrums are corrupted by a jamming signal.

Transmitter 2104 will now be explored in greater detail. FIG. 23A illustrates transmitter 2301, which is one embodiment of transmitter 2104 that generates redundant spectrums configured similar to redundant spectrums 2206b-d. Transmitter 2301 includes generator 2303, optional spectrum processing module 2304, and optional medium interface module 2320. Generator 2303 includes: first oscillator 2302, second oscillator 2309, first stage modulator 2306, and second stage modulator 2310.

Transmitter 2301 operates as follows. First oscillator 2302 and second oscillator 2309 generate a first oscillating signal 2305 and second oscillating signal 2312, respectively. First stage modulator 2306 modulates first oscillating signal 2305 with modulating baseband signal 2202, resulting in modulated signal 2308. First stage modulator 2306 may implement any type of modulation including but not limited to: amplitude modulation, frequency modulation, phase modulation, combinations thereof, or any other type of modulation. Second stage modulator 2310 modulates modulated signal 2308 with second oscillating signal 2312, resulting in multiple redundant spectrums 2206a-n shown in FIG. 23B. Second stage modulator 2310 is preferably a phase modulator, or a frequency modulator, although other types of modulation may be implemented including but not limited to amplitude modulation. Each redundant spectrum

2206a-n contains the necessary amplitude, phase, and frequency information to substantially reconstruct the modulating baseband signal 2202.

Redundant spectrums 2206a-n are substantially centered around f_1, which is the characteristic frequency of first oscillating signal 2305. Also, each redundant spectrum 2206a-n (except for 2206c) is offset from f_1 by approximately a multiple of f_2 (Hz), where f_2 is the frequency of the second oscillating signal 2312. Thus, each redundant spectrum 2206a-n is offset from an adjacent redundant spectrum by f_2 (Hz). This allows the spacing between adjacent redundant spectrums to be adjusted (or tuned) by changing f_2 that is associated with second oscillator 2309. Adjusting the spacing between adjacent redundant spectrums allows for dynamic real-time tuning of the bandwidth occupied by redundant spectrums 2206a-n.

In one embodiment, the number of redundant spectrums 2206a-n generated by transmitter 2301 is arbitrary and may be unlimited as indicated by the "a-n" designation for redundant spectrums 2206a-n. However, a typical communications medium will have a physical and/or administrative limitations (i.e. FCC regulations) that restrict the number of redundant spectrums that can be practically transmitted over the communications medium. Also, there may be other reasons to limit the number of redundant spectrums transmitted. Therefore, preferably, the transmitter 2301 will include an optional spectrum processing module 2304 to process the redundant spectrums 2206a-n prior to transmission over communications medium 2108.

In one embodiment, spectrum processing module 2304 includes a filter with a passband 2207 (FIG. 23C) to select redundant spectrums 2206b-d for transmission. This will substantially limit the frequency bandwidth occupied by the redundant spectrums to the passband 2207. In one embodiment, spectrum processing module 2304 also up converts redundant spectrums and/or amplifies redundant spectrums prior to transmission over the communications medium 2108. Finally, medium interface module 2320 transmits redundant spectrums over the communications medium 2108. In one embodiment, communications medium 2108 is an over-the-air link and medium interface module 2320 is an antenna. Other embodiments for communications medium 2108 and medium interface module 2320 will be understood based on the teachings contained herein.

FIG. 23D illustrates transmitter 2321, which is one embodiment of transmitter 2104 that generates redundant spectrums configured similar to redundant spectrums 2208c-d and unmodulated spectrum 2209. Transmitter 2321 includes generator 2311, spectrum processing module 2304, and (optional) medium interface module 2320. Generator 2311 includes: first oscillator 2302, second oscillator 2309, first stage modulator 2306, and second stage modulator 2310.

As shown in FIG. 23D, many of the components in transmitter 2321 are similar to those in transmitter 2301. However, in this embodiment, modulating baseband signal 2202 modulates second oscillating signal 2312. Transmitter 2321 operates as follows. First stage modulator 2306 modulates second oscillating signal 2312 with modulating baseband signal 2202, resulting in modulated signal 2322. As described earlier, first stage modulator 2306 can effect any type of modulation including but not limited to: amplitude modulation frequency modulation, combinations thereof, or any other type of modulation. Second stage modulator 2310 modulates first oscillating signal 2304 with modulated signal 2322, resulting in redundant spectrums 2208a-n, as shown in FIG. 23E. Second stage modulator 2310 is preferably a phase or frequency modulator, although other modulators could used including but not limited to an amplitude modulator.

Redundant spectrums 2208a-n are centered on unmodulated spectrum 2209 (at f_1 Hz), and adjacent spectrums are separated by f_2 Hz. The number of redundant spectrums 2208a-n generated by generator 2311 is arbitrary and unlimited, similar to spectrums 2206a-n discussed above. Therefore, optional spectrum processing module 2304 may also include a filter with passband 2325 to select, for example, spectrums 2208c,d for transmission over communications medium 2108. In addition, optional spectrum processing module 2304 may also include a filter (such as a bandstop filter) to attenuate unmodulated spectrum 2209. Alternatively, unmodulated spectrum 2209 may be attenuated by using phasing techniques during redundant spectrum generation. Finally, (optional) medium interface module 2320 transmits redundant spectrums 2208c,d over communications medium 2108.

Receiver 2112 will now be explored in greater detail to illustrate recovery of a demodulated baseband signal from received redundant spectrums. FIG. 24A illustrates receiver 2430, which is one embodiment of receiver 2112. Receiver 2430 includes optional medium interface module 2402, down-converter 2404, spectrum isolation module 2408, and data extraction module 2414. Spectrum isolation module 2408 includes filters 2410a-c. Data extraction module 2414 includes demodulators 2416a-c, error check modules 2420a-c, and arbitration module 2424. Receiver 2430 will be discussed in relation to the signal diagrams in FIGS. 24B-24J.

In one embodiment, optional medium interface module 2402 receives redundant spectrums 2210b-d (FIG. 22E, and FIG. 24B). Each redundant spectrum 2210b-d includes the necessary amplitude, phase, and frequency information to substantially reconstruct the modulating baseband signal used to generated the redundant spectrums. However, in the present example, spectrum 2210c also contains jamming signal 2211, which may interfere with the recovery of a baseband signal from spectrum 2210c. Down-converter 2404 down-converts received redundant spectrums 2210b-d to lower intermediate frequencies, resulting in redundant spectrums 2406a-c (FIG. 24C). Jamming signal 2211 is also down-converted to jamming signal 2407, as it is contained within redundant spectrum 2406b. Spectrum isolation module 2408 includes filters 2410a-c that isolate redundant spectrums 2406a-c from each other (FIGS. 24D-24F, respectively). Demodulators 2416a-c independently demodulate spectrums 2406a-c, resulting in demodulated baseband signals 2418a-c, respectively (FIGS. 24G-24I). Error check modules 2420a-c analyze demodulate baseband signal 2418a-c to detect any errors. In one embodiment, each error check module 2420a-c sets an error flag 2422a-c whenever an error is detected in a demodulated baseband signal. Arbitration module 2424 accepts the demodulated baseband signals and associated error flags, and selects a substantially error-free demodulated baseband signal (FIG. 24J). In one embodiment, the substantially error-free demodulated baseband signal will be substantially similar to the modulating baseband signal used to generate the received redundant spectrums, where the degree of similarity is application dependent.

Referring to FIGS. 24G-I, arbitration module 2424 will select either demodulated baseband signal 2418a or 2418c, because error check module 2420b will set the error flag 2422b that is associated with demodulated baseband signal 2418b.

The error detection schemes implemented by the error detection modules include but are not limited to: cyclic redundancy check (CRC) and parity check for digital signals, and various error detections schemes for analog signal.

Further details of enhanced signal reception as described in this section are presented in pending U.S. application "Method and System for Ensuring Reception of a Communications Signal," Ser. No. 09/176,415, filed October 21, 1998, issued as U.S. Patent No. 6,061,555 on May 9, 2000.

5. Unified Down-Conversion and Filtering

The present invention is directed to systems and methods of unified down-conversion and filtering (UDF), and applications of same.

In particular, the present invention includes a unified down-converting and filtering (UDF) module that performs frequency selectivity and frequency translation in a unified (i.e., integrated) manner. By operating in this manner, the invention achieves high frequency selectivity prior to frequency translation (the invention is not limited to this embodiment). The invention achieves high frequency selectivity at substantially any frequency, including but not limited to RF (radio frequency) and greater frequencies. It should be understood that the invention is not limited to this example of RF and greater frequencies. The invention is intended, adapted, and capable of working with lower than radio frequencies.

FIG. 17 is a conceptual block diagram of a UDF module 1702 according to an embodiment of the present invention. The UDF module 1702 performs at least frequency translation and frequency selectivity.

The effect achieved by the UDF module 1702 is to perform the frequency selectivity operation prior to the performance of the frequency translation operation. Thus, the UDF module 1702 effectively performs input filtering.

According to embodiments of the present invention, such input filtering involves a relatively narrow bandwidth. For example, such input filtering may represent channel select filtering, where the filter bandwidth may be, for example, 50 KHz to 150 KHz. It should be understood, however, that the invention is not limited to these frequencies. The invention is intended, adapted, and capable of achieving filter bandwidths of less than and greater than these values.

In embodiments of the invention, input signals 1704 received by the UDF module 1702 are at radio frequencies. The UDF module 1702 effectively operates to input filter these RF input signals 1704. Specifically, in these embodiments, the UDF module 1702 effectively performs input, channel select filtering of the RF input signal 1704. Accordingly, the invention achieves high selectivity at high frequencies.

The UDF module 1702 effectively performs various types of filtering, including but not limited to bandpass filtering, low pass filtering, high pass filtering, notch filtering, all pass filtering, band stop filtering, etc., and combinations thereof.

Conceptually, the UDF module 1702 includes a frequency translator 1708. The frequency translator 1708 conceptually represents that portion of the UDF module 1702 that performs frequency translation (down conversion).

The UDF module 1702 also conceptually includes an apparent input filter 1706 (also sometimes called an input filtering emulator). Conceptually, the apparent input filter 1706 represents that portion of the UDF module 1702 that performs input filtering.

In practice, the input filtering operation performed by the UDF module 1702 is integrated with the frequency translation operation. The input filtering operation can be viewed as being performed concurrently with the frequency translation operation. This is a reason why the input filter 1706 is herein referred to as an "apparent" input filter 1706.

The UDF module 1702 of the present invention includes a number of advantages. For example, high selectivity at high frequencies is realizable using the UDF module 1702. This feature of the invention is evident by the high Q factors that are attainable. For example, and without limitation, the UDF module 1702 can be designed with a filter center frequency f_C on the order of 900 MHZ, and a filter bandwidth on the order of 50 KHz. This represents a Q of 18,000 (Q is equal to the center frequency divided by the bandwidth).

It should be understood that the invention is not limited to filters with high Q factors. The filters contemplated by the present invention may have lesser or greater Qs, depending on the application, design, and/or implementation. Also, the scope of the invention includes filters where Q factor as discussed herein is not applicable.

The invention exhibits additional advantages. For example, the filtering center frequency f_C of the UDF module 1702 can be electrically adjusted, either statically or dynamically.

Also, the UDF module 1702 can be designed to amplify input signals.

Further, the UDF module 1702 can be implemented without large resistors, capacitors, or inductors. Also, the UDF module 1702 does not require that tight tolerances be maintained on the values of its individual components, i.e., its resistors, capacitors, inductors, etc. As a result, the architecture of the UDF module 1702 is friendly to integrated circuit design techniques and processes.

The features and advantages exhibited by the UDF module 1702 are achieved at least in part by adopting a new technological paradigm with respect to frequency selectivity and translation. Specifically, according to the present invention, the UDF module 1702 performs the frequency selectivity operation and the frequency translation operation as a single, unified (integrated) operation. According to the invention, operations relating to frequency translation also contribute to the performance of frequency selectivity, and vice versa.

According to embodiments of the present invention, the UDF module generates an output signal from an input signal using samples/instances of the input signal and samples/instances of the output signal.

More particularly, first, the input signal is under-sampled. This input sample includes information (such as amplitude, phase, etc.) representative of the input signal existing at the time the sample was taken.

As described further below, the effect of repetitively performing this step is to translate the frequency (that is, down-convert) of the input signal to a desired lower frequency, such as an intermediate frequency (IF) or baseband.

Next, the input sample is held (that is, delayed).

Then, one or more delayed input samples (some of which may have been scaled) are combined with one or more delayed instances of the output signal (some of which may have been scaled) to generate a current instance of the output signal.

Thus, according to a preferred embodiment of the invention, the output signal is generated from prior samples/instances of the input signal and/or the output signal. (It is noted that, in some embodiments of the invention, current samples/instances of the input signal and/or the output signal may be used to generate current instances of the output signal.). By operating in this manner, the UDF module preferably performs input filtering and frequency down-conversion in a unified manner.

FIG. 19 illustrates an example implementation of the unified down-converting and filtering (UDF) module 1922. The UDF module 1922 performs the frequency translation operation and the frequency selectivity operation in an integrated, unified manner as described above, and as further described below.

In the example of FIG. 19, the frequency selectivity operation performed by the UDF module 1922 comprises a band-pass filtering operation according to EQ. 1, below, which is an example representation of a band-pass filtering transfer function.

$$VO = \alpha_1 z^{-1} VI - \beta_1 z^{-1} VO - \beta_0 z^{-2} VO \qquad \text{EQ. 1}$$

It should be noted, however, that the invention is not limited to band-pass filtering. Instead, the invention effectively performs various types of filtering, including but not limited to bandpass filtering, low pass filtering, high pass filtering, notch filtering, all pass filtering, band stop filtering, etc., and combinations thereof. As will be appreciated, there are many representations of any given filter type. The invention is applicable to these filter representations. Thus, EQ. 1 is referred to herein for illustrative purposes only, and is not limiting.

The UDF module 1922 includes a down-convert and delay module 1924, first and second delay modules 1928 and 1930, first and second scaling modules 1932 and 1934, an output sample and hold module 1936, and an (optional) output smoothing module

1938. Other embodiments of the UDF module will have these components in different configurations, and/or a subset of these components, and/or additional components. For example, and without limitation, in the configuration shown in FIG. 19, the output smoothing module 1938 is optional.

As further described below, in the example of FIG. 19, the down-convert and delay module 1924 and the first and second delay modules 1928 and 1930 include switches that are controlled by a clock having two phases, ϕ_1 and ϕ_2. ϕ_1 and ϕ_2 preferably have the same frequency, and are non-overlapping (alternatively, a plurality such as two clock signals having these characteristics could be used). As used herein, the term "non-overlapping" is defined as two or more signals where only one of the signals is active at any given time. In some embodiments, signals are "active" when they are high. In other embodiments, signals are active when they are low.

Preferably, each of these switches closes on a rising edge of ϕ_1 or ϕ_2, and opens on the next corresponding falling edge of ϕ_1 or ϕ_2. However, the invention is not limited to this example. As will be apparent to persons skilled in the relevant art(s), other clock conventions can be used to control the switches.

In the example of FIG. 19, it is assumed that α_1 is equal to one. Thus, the output of the down-convert and delay module 1924 is not scaled. As evident from the embodiments described above, however, the invention is not limited to this example.

The example UDF module 1922 has a filter center frequency of 900.2 MHZ and a filter bandwidth of 570 KHz. The pass band of the UDF module 1922 is on the order of 899.915 MHZ to 900.485 MHZ. The Q factor of the UDF module 1922 is approximately 1879 (i.e., 900.2 MHZ divided by 570 KHz).

The operation of the UDF module 1922 shall now be described with reference to a Table 1802 (FIG. 18) that indicates example values at nodes in the UDF module 1922 at a number of consecutive time increments. It is assumed in Table 1802 that the UDF module 1922 begins operating at time t-1. As indicated below, the UDF module 1922 reaches steady state a few time units after operation begins. The number of time units necessary for a given UDF module to reach steady state depends on the configuration of the UDF module, and will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

At the rising edge of ϕ_1 at time t-1, a switch 1950 in the down-convert and delay module 1924 closes. This allows a capacitor 1952 to charge to the current value of an input signal, VI_{t-1}, such that node 1902 is at VI_{t-1}. This is indicated by cell 1804 in FIG. 18. In effect, the combination of the switch 1950 and the capacitor 1952 in the down-convert and delay module 1924 operates to translate the frequency of the input signal VI to a desired lower frequency, such as IF or baseband. Thus, the value stored in the capacitor 1952 represents an instance of a down-converted image of the input signal VI.

The manner in which the down-convert and delay module 1924 performs frequency down-conversion is further described elsewhere in this application, and is additionally described in pending U.S. application "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed October 21, 1998, issued as U.S. Patent No. 6,061,551 on May 9, 2000, which is herein incorporated by reference in its entirety.

Also at the rising edge of ϕ_1 at time t-1, a switch 1958 in the first delay module 1928 closes, allowing a capacitor 1960 to charge to VO_{t-1}, such that node 1906 is at VO_{t-1}. This is indicated by cell 1806 in Table 1802. (In practice, VO_{t-1} is undefined at this point. However, for ease of understanding, VO_{t-1} shall continue to be used for purposes of explanation.)

Also at the rising edge of ϕ_1 at time t-1, a switch 1966 in the second delay module 1930 closes, allowing a capacitor 1968 to charge to a value stored in a capacitor 1964. At this time, however, the value in capacitor 1964 is undefined, so the value in capacitor 1968 is undefined. This is indicated by cell 1807 in table 1802.

At the rising edge of ϕ_2 at time t- 1, a switch 1954 in the down-convert and delay module 1924 closes, allowing a capacitor 1956 to charge to the level of the capacitor 1952. Accordingly, the capacitor 1956 charges to VI_{t-1}, such that node 1904 is at VI_{t-1}. This is indicated by cell 1810 in Table 1802.

The UDF module 1922 may optionally include a unity gain module 1990A between capacitors 1952 and 1956. The unity gain module 1990A operates as a current source to enable capacitor 1956 to charge without draining the charge from capacitor 1952. For a similar reason, the UDF module 1922 may include other unity gain modules 1990B-1990G. It should be understood that, for many embodiments and applications of the invention, these unity gain modules 1990A-1990G are optional. The structure and operation of the unity gain modules 1990 will be apparent to persons skilled in the relevant art(s).

Also at the rising edge of ϕ_2 at time t−1, a switch 1962 in the first delay module 1928 closes, allowing a capacitor 1964 to charge to the level of the capacitor 1960. Accordingly, the capacitor 1964 charges to VO_{t-1}, such that node 1908 is at VO_{t-1}. This is indicated by cell 1814 in Table 1802.

Also at the rising edge of ϕ_2 at time t-1, a switch 1970 in the second delay module 1930 closes, allowing a capacitor 1972 to charge to a value stored in a capacitor 1968. At this time, however, the value in capacitor 1968 is undefined, so the value in capacitor 1972 is undefined. This is indicated by cell 1815 in table 1802.

At time t, at the rising edge of ϕ_1, the switch 1950 in the down-convert and delay module 1924 closes. This allows the capacitor 1952 to charge to VI_t, such that node 1902 is at VI_t. This is indicated in cell 1816 of Table 1802.

Also at the rising edge of ϕ_1 at time t, the switch 1958 in the first delay module 1928 closes, thereby allowing the capacitor 1960 to charge to VO_t. Accordingly, node 1906 is at VO_t. This is indicated in cell 1820 in Table 1802.

Further at the rising edge of ϕ_1 at time t, the switch 1966 in the second delay module 1930 closes, allowing a capacitor 1968 to charge to the level of the capacitor 1964. Therefore, the capacitor 1968 charges to VO_{t-1}, such that node 1910 is at VO_{t-1}. This is indicated by cell 1824 in Table 1802.

At the rising edge of ϕ_2 at time t, the switch 1954 in the down-convert and delay module 1924 closes, allowing the capacitor 1956 to charge to the level of the capacitor 1952. Accordingly, the capacitor 1956 charges to VI_t, such that node 1904 is at VI_t. This is indicated by cell 1828 in Table 1802.

Also at the rising edge of ϕ_2 at time t, the switch 1962 in the first delay module 1928 closes, allowing the capacitor 1964 to charge to the level in the capacitor 1960. Therefore, the capacitor 1964 charges to VO_t, such that node 1908 is at VO_t. This is indicated by cell 1832 in Table 1802.

Further at the rising edge of ϕ_2 at time t, the switch 1970 in the second delay module 1930 closes, allowing the capacitor 1972 in the second delay module 1930 to charge to the level of the capacitor 1968 in the second delay module 1930. Therefore, the capacitor 1972 charges to VO_{t-1}, such that node 1912 is at VO_{t-1}. This is indicated in cell 1836 of FIG. 18.

At time t+1, at the rising edge of ϕ_1, the switch 1950 in the down-convert and delay module 1924 closes, allowing the capacitor 1952 to charge to VI_{t+1}. Therefore, node 1902 is at VI_{t+1}, as indicated by cell 1838 of Table 1802.

Also at the rising edge of ϕ_1 at time t+1, the switch 1958 in the first delay module 1928 closes, allowing the capacitor 1960 to charge to VO_{t+1}. Accordingly, node 1906 is at VO_{t+1}, as indicated by cell 1842 in Table 1802.

Further at the rising edge of ϕ_1 at time t+1, the switch 1966 in the second delay module 1930 closes, allowing the capacitor 1968 to charge to the level of the capacitor 1964. Accordingly, the capacitor 1968 charges to VO_t, as indicated by cell 1846 of Table 1802.

In the example of FIG. 19, the first scaling module 1932 scales the value at node 1908 (i.e., the output of the first delay module 1928) by a scaling factor of -0.1. Accordingly, the value present at node 1914 at time t+1 is $-0.1 * VO_t$. Similarly, the second scaling module 1934 scales the value present at node 1912 (i.e., the output of the second scaling module 1930) by a scaling factor of -0.8. Accordingly, the value present at node 1916 is $-0.8 * VO_{t-1}$ at time t+1.

At time t+1, the values at the inputs of the summer 1926 are: VI_t at node 1904, $-0.1 * VO_t$ at node 1914, and $-0.8 * VO_{t-1}$ at node 1916 (in the example of FIG. 19, the values at nodes 1914 and 1916 are summed by a second summer 1925, and this sum is presented to the summer 1926). Accordingly, at time t+1, the summer generates a signal equal to $VI_t - 0.1 * VO_t - 0.8 * VO_{t-1}$.

At the rising edge of ϕ_1 at time t+1, a switch 1991 in the output sample and hold module 1936 closes, thereby allowing a capacitor 1992 to charge to VO_{t+1}. Accordingly, the capacitor 1992 charges to VO_{t+1}, which is equal to the sum generated by the adder 1926. As just noted, this value is equal to: $VI_t - 0.1 * VO_t - 0.8 * VO_{t-1}$. This is indicated in cell 1850 of Table 1802. This value is presented to the optional output smoothing module 1938, which smooths the signal to thereby generate the instance of the output signal VO_{t+1}. It is apparent from inspection that this value of VO_{t+1} is consistent with the band pass filter transfer function of EQ. 1.

Further details of unified down-conversion and filtering as described in this section are presented in pending U.S. application "Integrated Frequency Translation And Selectivity," Ser. No. 09/175,966, filed October 21, 1998, issued as U.S. Patent No. 6,049,706 on April 11, 2000, incorporated herein by reference in its entirety.

6. *Example Application Embodiments of the Invention*

As noted above, the UFT module of the present invention is a very powerful and flexible device. Its flexibility is illustrated, in part, by the wide range of applications in which it can be used. Its power is illustrated, in part, by the usefulness and performance of such applications.

Example applications of the UFT module were described above. In particular, frequency down-conversion, frequency up-conversion, enhanced signal reception, and unified down-conversion and filtering applications of the UFT module were summarized above, and are further described below. These applications of the UFT module are discussed herein for illustrative purposes. The invention is not limited to these example applications. Additional applications of the UFT module will be apparent to persons skilled in the relevant art(s), based on the teachings contained herein.

For example, the present invention can be used in applications that involve frequency down-conversion. This is shown in FIG. 1C, for example, where an example UFT module 115 is used in a down-conversion module 114. In this capacity, the UFT module 115 frequency down-converts an input signal to an output signal. This is also shown in FIG. 7, for example, where an example UFT module 706 is part of a down-conversion module 704, which is part of a receiver 702.

The present invention can be used in applications that involve frequency up-conversion. This is shown in FIG. 1D, for example, where an example UFT module 117 is used in a frequency up-conversion module 116. In this capacity, the UFT module 117 frequency up-converts an input signal to an output signal. This is also shown in FIG. 8, for example, where an example UFT module 806 is part of up-conversion module 804, which is part of a transmitter 802.

The present invention can be used in environments having one or more transmitters 902 and one or more receivers 906, as illustrated in FIG. 9. In such environments, one or more of the transmitters 902 may be implemented using a UFT module, as shown for example in FIG. 8. Also, one or more of the receivers 906 may be implemented using a UFT module, as shown for example in FIG. 7.

The invention can be used to implement a transceiver. An example transceiver 1002 is illustrated in FIG. 10. The transceiver 1002 includes a transmitter 1004 and a receiver 1008. Either the transmitter 1004 or the receiver 1008 can be implemented using a UFT module. Alternatively, the transmitter 1004 can be implemented using a UFT module 1006, and the receiver 1008 can be implemented using a UFT module 1010. This embodiment is shown in FIG. 10.

Another transceiver embodiment according to the invention is shown in FIG. 11. In this transceiver 1102, the transmitter 1104 and the receiver 1108 are implemented using a single UFT module 1106. In other words, the transmitter 1104 and the receiver 1108 share a UFT module 1106.

As described elsewhere in this application, the invention is directed to methods and systems for enhanced signal reception (ESR). Various ESR embodiments include an ESR module (transmit) in a transmitter 1202, and an ESR module (receive) in a receiver 1210. An example ESR embodiment configured in this manner is illustrated in FIG. 12.

The ESR module (transmit) 1204 includes a frequency up-conversion module 1206. Some embodiments of this frequency up-conversion module 1206 may be implemented using a UFT module, such as that shown in FIG. 1D.

The ESR module (receive) 1212 includes a frequency down-conversion module 1214. Some embodiments of this frequency down-conversion module 1214 may be implemented using a UFT module, such as that shown in FIG. 1C.

As described elsewhere in this application, the invention is directed to methods and systems for unified down-conversion and filtering (UDF). An example unified down-conversion and filtering module 1302 is illustrated in FIG. 13. The unified down-conversion and filtering module 1302 includes a frequency down-conversion module 1304 and a filtering module 1306. According to the invention, the frequency down-conversion module 1304 and the filtering module 1306 are implemented using a UFT module 1308, as indicated in FIG. 13.

Unified down-conversion and filtering according to the invention is useful in applications involving filtering and/or frequency down-conversion. This is depicted, for example, in FIGS. 15A-15F. FIGS. 15A-15C indicate that unified down-conversion and filtering according to the invention is useful in applications where filtering precedes, follows, or both precedes and follows frequency down-conversion. FIG. 15D indicates that a unified down-conversion and filtering module 1524 according to the invention can be utilized as a filter 1522 (i.e., where the extent of frequency down-conversion by the down-converter in the unified down-conversion and filtering module 1524 is minimized). FIG. 15E indicates that a unified down-conversion and filtering module 1528 according to the invention can be utilized as a down-converter 1526 (i.e., where the filter in the unified down-conversion and filtering module 1528 passes substantially all frequencies). FIG. 15F illustrates that the unified down-conversion and filtering module 1532 can be used as an amplifier. It is noted that one or more UDF modules can be used in applications that involve at least one or more of filtering, frequency translation, and amplification.

For example, receivers, which typically perform filtering, down-conversion, and filtering operations, can be implemented using one or more unified down-conversion and filtering modules. This is illustrated, for example, in FIG. 14.

The methods and systems of unified down-conversion and filtering of the invention have many other applications. For example, as discussed herein, the enhanced signal reception (ESR) module (receive) operates to down-convert a signal containing a plurality of spectrums. The ESR module (receive) also operates to isolate the spectrums in the down-converted signal, where such isolation is implemented via filtering in some embodiments. According to embodiments of the invention, the ESR module (receive) is implemented using one or more unified down-conversion and filtering (UDF) modules. This is illustrated, for example, in FIG. 16. In the example of FIG. 16, one or more of the UDF modules 1610, 1612, 1614 operates to down-convert a received signal. The UDF modules 1610, 1612, 1614 also operate to filter the down-converted signal so as to isolate the spectrum(s) contained therein. As noted above, the UDF modules 1610, 1612, 1614 are implemented using the universal frequency translation (UFT) modules of the invention.

The invention is not limited to the applications of the UFT module described above. For example, and without limitation, subsets of the applications (methods and/or structures) described herein (and others that would be apparent to persons skilled in the relevant art(s) based on the herein teachings) can be associated to form useful combinations.

For example, transmitters and receivers are two applications of the UFT module. FIG. 10 illustrates a transceiver 1002 that is formed by combining these two applications of the UFT module, i.e., by combining a transmitter 1004 with a receiver 1008.

Also, ESR (enhanced signal reception) and unified down-conversion and filtering are two other applications of the UFT module. FIG. 16 illustrates an example where ESR and unified down-conversion and filtering are combined to form a modified enhanced signal reception system.

The invention is not limited to the example applications of the UFT module discussed herein. Also, the invention is not limited to the example combinations of applications of the UFT module discussed herein. These examples were provided for illustrative purposes only, and are not limiting. Other applications and combinations of such applications will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such applications and combinations include, for example and without limitation, applications/combinations comprising and/or involving one or more of: (1) frequency translation; (2) frequency down-conversion; (3) frequency up-conversion;

(4) receiving; (5) transmitting; (6) filtering; and/or (7) signal transmission and reception in environments containing potentially jamming signals.

Additional example applications are described below.

6.1 Data Communication

The invention is directed to data communication among data processing devices. For example, and without limitation, the invention is directed to computer networks such as, for example, local area networks (LANs), wide area networks (WANs), including wireless LANs (WLANs) and wireless WANs, modulator/demodulators (modems), including wireless modems, etc.

FIG. 25 illustrates an example environment 2502 wherein computers 2504, 2512, and 2526 communicate with one another via a computer network 2534. It is noted that the invention is not limited to computers, but encompasses any data processing and/or communications device or other device where communications with external devices is desired. Also, the invention includes but si not limited to WLAN client (also called mobile terminals, and/or stations) and infrastructure devices (also called access points). In the example of FIG. 25, computer 2504 is communicating with the network 2534 via a wired link, whereas computers 2512 and 2526 are communicating with the network 2534 via wireless links.

In the teachings contained herein, for illustrative purposes, a link may be designated as being a wired link or a wireless link. Such designations are for example purposes only, and are not limiting. A link designated as being wireless may alternatively be wired. Similarly, a link designated as being wired may alternatively be wireless. This is applicable throughout the entire application.

The computers 2504, 2512 and 2526 each include an interface 2506, 2514, and 2528, respectively, for communicating with the network 2534. The interfaces 2506, 2514, and 2528 include transmitters 2508, 2516, and 2530 respectively. Also, the interfaces 2506, 2514 and 2528 include receivers 2510, 2518, and 2532 respectively. In embodiments of the invention, the transmitters 2508, 2516 and 2530 are implemented using UFT modules for performing frequency up-conversion operations (see, for example, FIG. 8). In embodiments, the receivers 2510, 2518 and 2532 are implemented using UFT modules for performing frequency down-conversion operations (see, for example, FIG. 7).

As noted above, the computers 2512 and 2526 interact with the network 2534 via wireless links. In embodiments of the invention, the interfaces 2514, 2528 in computers 2512, 2526 represent modulator/demodulators (modems).

In embodiments, the network 2534 includes an interface or modem 2520 for communicating with the modems 2514, 2528 in the computers 2512, 2526. In embodiments, the interface 2520 includes a transmitter 2522, and a receiver 2524. Either or both of the transmitter 2522, and the receiver 2524 are implemented using UFT modules for performing frequency translation operations (see, for example, FIGS. 7 and 8).

In alternative embodiments, one or more of the interfaces 2506, 2514, 2520, and 2528 are implemented using transceivers that employ one or more UFT modules for performing frequency translation operations (see, for example, FIGS. 10 and 11).

FIG. 26 illustrates another example data communication embodiment 2602. Each of a plurality of computers 2604, 2612, 2614 and 2616 includes an interface, such as an interface 2606 shown in the computer 2604. It should be understood that the other computers 2612, 2614, 2616 also include an interface such as an interface 2606. The computers 2604, 2612, 2614 and 2616 communicate with each other via interfaces 2606 and wireless or wired links, thereby collectively representing a data communication network.

The interfaces 2606 may represent any computer interface or port, such as but not limited to a high speed internal interface, a wireless serial port, a wireless PS2 port, a wireless USB port, PCMCIA port, etc.

The interface 2606 includes a transmitter 2608 and a receiver 2610. In embodiments of the invention, either or both of the transmitter 2608 and the receiver 2610 are implemented using UFT modules for frequency up-conversion and down-conversion (see, for example, FIGS. 7 and 8). Alternatively, the interfaces 2806 can be implemented using a transceiver having one or more UFT modules for performing frequency translation operations (see, for example, FIGS. 10 and 11).

FIGS. 33-38 illustrate other scenarios envisioned and encompassed by the invention. FIG. 33 illustrates a data processing environment 3302 wherein a wired network, such as an Ethernet network 3304, is linked to another network, such as a WLAN 3306, via a wireless link 3308. The wireless link 3308 is established via interfaces 3310, 3312 which are preferably implemented using universal frequency translation modules.

FIGS 35-38 illustrate that the present invention supports WLANs that are located in one or more buildings or over any defined geographical area, as shown in FIGs. 35-38.

The invention includes multiple networks linked together. The invention also envisions wireless networks conforming to any known or custom standard or specification. This is shown in FIG. 34, for example, where any combination of WLANs conforming to any WLAN standard or configuration, such as IEEE 802.11 and Bluetooth (or other relatively short range communication specification or standard), any WAN cellular or telephone standard or specification, any type of radio links, any custom standard or specification, etc., or combination thereof, can be implemented using the universal frequency translation technology described herein. Also, any combination of these networks may be coupled together, as illustrated in FIG. 34.

The invention supports WLANs that are located in one or multiple buildings, as shown in FIGS. 35 and 36. The invention also supports WLANs that are located in an area including and external to one or more buildings, as shown in FIG. 37. In fact, the invention is directed to networks that cover any defined geographical area, as shown in FIG. 38. In the embodiments described above, wireless links are preferably established using WLAN interfaces as described herein.

More generally, the invention is directed to WLAN client devices and WLAN infrastructure devices. "WLAN Client Devices" refers to, for example, any data processing and/or communication devices in which wired or wireless communication functionality is desired, such as but not limited to computers, personal data assistants (PDAs), automatic identification data collection devices (such as bar code scanners/readers, electronic article surveillance readers, and radio frequency identification readers), telephones, network devices, etc., and combinations thereof. "WLAN Infrastructure Devices" refers to, for example, Access Points and other devices used to provide the ability for WLAN Client Devices (as well as potentially other devices) to connect to wired and/or wireless networks and/or to provide the network functionality of a WLAN. "WLAN" refers to, for example, a Wireless Local Area Network that is implemented according to and that operates within WLAN standards and/or specifications, such as but not limited to IEEE 802.11, IEEE 802.11a, IEEE 802.11b, HomeRF, Proxim Range LAN, Proxim Range LAN2, Symbol Spectrum 1, Symbol Spectrum 24 as it existed prior to adoption of IEEE 802.11, HiperLAN1, or HiperLAN2. WLAN client devices and/or WLAN infrastructure devices may operate in a multi-mode capacity. For example, a device may include WLAN and WAN functionality. Another device may include WLAN and short range communication (such as but not limited to Blue Tooth) functionality. Another device may include WLAN and WAN and short range communication functionality. It is noted that the above definitions and examples are provided for illustrative purposes, and are not limiting. Equivalents to that described above will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

6.1.1. Example Implementations: Interfaces, Wireless Modems, Wireless LANs, etc.

The present invention is now described as implemented in an interface, such as a wireless modem or other device (such as client or infrastructure device) , which can be utilized to implement or interact with a wireless local area network (WLAN) or wireless wide area network (WWAN), for example. In an embodiment, the present invention is implemented in a WLAN to support IEEE WLAN Standard 802.11, but this embodiment is mentioned for illustrative purposes only. The invention is not limited to this standard.

Conventional wireless modems are described in, for example, U.S. Patent 5,764,693, titled, "Wireless Radio Modem with Minimal Inter-Device RF Interference," incorporated herein by reference in its entirety. The present invention replaces a substantial portion of conventional wireless modems with one or more universal frequency translators (UFTs). The resultant improved wireless modem consumes less power that conventional wireless modems and is easier and less expensive to design and build. A wireless modem in accordance with the present invention can be implemented in a PC-MCIA card or within a main housing of a computer, for example.

FIG. 27 illustrates an example block diagram of a computer system 2710, which can be wirelessly coupled to a LAN, as illustrated in FIGS. 25 and 26. The computer system 2710 includes an interface 2714 and an antenna 2712. The interface 2714 includes a transmitter module 2716 that receives information from a digital signal processor (DSP) 2720, and modulates and up-converts the information for transmission from the antenna 2712. The interface 2714 also includes a receiver module 2718 that receives modulated carrier signals via the antenna 2712. The receiver module 2718 down-converts and demodulates the modulated carrier signals to baseband information, and provides the baseband information to the DSP 2720. The DSP 2720 can include a central processing unit (CPU) and other components of the computer 2712. Conventionally, the interface 2714 is implemented with heterodyne components.

FIG. 28 illustrates an example interface 2810 implemented with heterodyne components. The interface 2810 includes a transmitter module 2812 and a receiver module 2824. The receiver module 2824 includes an RF section 2830, one or more IF sections 2828, a demodulator section 2826, an optional analog to digital (A/D) converter 2834, and a frequency generator/synthesizer 2832. The transmitter module 2812 includes an optional digital to analog (D/A) converter 2822, a modulator \section 2818, one or more IF sections 2816, an RF section 2814, and a frequency generator/synthesizer 2820. Operation of the interface 2810 will be apparent to one skilled in the relevant art(s), based on the description herein.

FIG. 29 illustrates an example in-phase/quadrature-phase (I/Q) interface 2910 implemented with heterodyne components. I/Q implementations allow two channels of information to be communicated on a carrier signal and thus can be utilized to increase data transmission.

The interface 2910 includes a transmitter module 2912 and a receiver module 2934. The receiver module 2934 includes an RF section 2936, one or more IF sections 2938, an I/Q demodulator section 2940, an optional A/D converter 2944, and a frequency generator/synthesizer 2942. The I/Q demodulator section 2940 includes a signal splitter 2946, mixers 2948, and a phase shifter 2950. The signal splitter 2946 provides a received signal to the mixers 2948. The phase shifter 2950 operates the mixers 2948 ninety degrees out of phase with one another to generate I and Q information channels 2952 and 2954, respectively, which are provided to a DSP 2956 through the optional A/D converter 2944.

The transmitter module 2912 includes an optional D/A converter 2922, an I/Q modulator section 2918, one or more IF sections 2916, an RF section 2914, and a frequency generator/synthesizer 2920. The I/Q modulator section 2918 includes mixers 2924, a phase shifter 2926, and a signal combiner 2928. The phase shifter 2926 operates the mixers 2924 ninety degrees out of phase with one another to generate I and Q modulated information signals 2930 and 2932, respectively, which are combined by the signal combiner 2928. The IF section(s) 2916 and RF section 2914 up-convert the combined I and Q modulated information signals 2930 and 2932 to RF for transmission by the antenna, in a manner well known in the relevant art(s).

Heterodyne implementations, such as those illustrated in FIGS. 28 and 29, are expensive and difficult to design, manufacture and tune. In accordance with the present invention, therefore, the interface 2714 (FIG. 27) is preferably implemented with one or more universal frequency translation (UFT) modules, such as the UFT module 102 (FIG. 1A). Thus previously described benefits of the present invention are obtained in wireless modems, WLANs, etc.

FIG. 30 illustrates an example block diagram embodiment of the interface 2714 that is associated with a computer or any other data processing and/or communications device. In FIG. 30, the receiver module 2718 includes a universal frequency down-converter (UFD) module 3014 and an optional analog to digital (A/D) converter 3016, which converts an analog output from the UFD 3014 to a digital format for the DSP 2720. The transmitter module 2716 includes an optional modulator 3012 and a universal frequency up-converter (UFU) module 3010. The optional modulator 3012 can be a variety of types of modulators, including conventional modulators. Alternatively, the UFU module 3010 includes modulator functionality. The example implementation of FIG. 30 operates substantially as described above and in co-pending U.S. Patent Applications titled, "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed October 21, 1998, issued as U.S. Patent No. 6,061,551 on May 9, 2000, and "Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, filed October 21, 1998, issued as U.S. Patent No. 6,091,940 on July 18, 2000, as well as other cited documents.

FIG. 31 illustrates an example implementation of the interface 2714 illustrated in FIG. 30, wherein the receiver UFD 3014 includes a UFT module 3112, and the transmitter UFU 3010 includes a universal frequency translation (UFT) module 3110. This example implementation operates substantially as described above and in co-pending U.S. Patent Applications titled, "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed October 21, 1998,issued as U.S. Patent No. 6,061,551 on May 9, 2000, and "Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, filed October 21, 1998, "Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, filed October 21, 1998, issued as U.S. Patent No. 6,091,940 on July 18, 2000, as well as other cited documents.

FIG. 32 illustrates an example I/Q implementation of the interface module 2710. Other I/Q implementations are also contemplated and are within the scope of the present invention.

In the example of FIG. 32, the receiver UFD module 3014 includes a signal divider 3228 that provides a received I/Q modulated carrier signal 3230 between a third UFT module 3224 and a fourth UFT module 3226. A phase shifter 3232, illustrated here as a 90 degree phase shifter, controls the third and fourth UFT modules 3224 and 3226 to operate 90 degrees out of phase with one another. As a result, the third and fourth UFT modules 3224 and 3226 down-convert and demodulate the received I/Q modulated carrier signal 3230, and output I and Q channels 3234 and 3236, respectively, which are provided to the DSP 2720 through the optional A/D converter 3016.

In the example of FIG. 32, the transmitter UFU module 3010 includes first and second UFT modules 3212 and 3214 and a phase shifter 3210, which is illustrated here as a 90 degree phase shifter. The phase shifter 3210 receives a lower frequency modulated carrier signal 3238 from the modulator 3012. The phase shifter 3210 controls the first and second UFT modules 3212 and 3214 to operate 90 degrees out of phase with one another. The first and second UFT modules 3212 and 3214 up-convert the lower frequency modulated carrier signal 3238, which are output as higher frequency modulated I and Q carrier channels 3218 and 3220, respectively. A signal combiner 3216 combines the higher frequency modulated I and Q carrier channels 3218 and 3220 into a single higher frequency modulated I/Q carrier signal 3222 for transmitting by the antenna 2712.

The example implementations of the interfaces described above, and variations thereof, can also be used to implement network interfaces, such as the network interface 2520 illustrated in FIG. 25.

6.1.2. Example Modifications

The RF modem applications, WLAN applications, etc., described herein, can be modified by incorporating one or more of the enhanced signal reception (ESR) techniques described herein. Use of ESR embodiments with the network embodiments described herein will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

The RF modem applications, WLAN applications, etc., described herein can be enhanced by incorporating one or more of the unified down-conversion and filtering (UDF) techniques described herein. Use of UDF embodiments with the network embodiments described herein will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

6.2. Other Example Applications

The application embodiments described above are provided for purposes of illustration. These applications and embodiments are not intended to limit the invention. Alternate and additional applications and embodiments, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. For example, such alternate and additional applications and embodiments include combinations of those described above. Such combinations will be apparent to persons skilled in the relevant art(s) based on the herein teachings.

7.0. Example WLAN Implementation Embodiments

7.1 Architecture

FIG. 39 is a block diagram of a WLAN interface 3902 (also referred to as a WLAN modem herein) according to an embodiment of the invention. The WLAN interface/modem 3902 includes an antenna 3904, a low noise amplifier or power amplifier (LNA/PA) 3904, a receiver 3906, a transmitter 3910, a control signal generator 3908, a demodulator/modulator facilitation module 3912, and a media access controller (MAC) interface 3914. Other embodiments may include different elements. The MAC interface 3914 couples the WLAN interface/modem 3902 to a computer 3916 or other data processing device. The computer 3916 preferably includes a MAC 3918.

The WLAN interface/modem 3902 represents a transmit and receive application that utilizes the universal frequency translation technology described herein. It also represents a zero IF (or direct-to-data) WLAN architecture.

The WLAN interface/modem 3902 also represents a vector modulator and a vector demodulator using the universal frequency translation (UFT) technology described herein. Use of the UFT technology enhances the flexibility of the WLAN application (i.e., makes it universal).

In the embodiment shown in FIG. 39, the WLAN interface/modem 3902 is compliant with WLAN standard IEEE 802.11. However, the invention is not limited to this standard. The invention is applicable to any communication standard or specification, as will be appreciated by persons skilled in the relevant art(s) based on the teachings contained herein. Any modifications to the invention to operate with other standards or specifications will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

In the embodiment shown in FIG. 39, the WLAN interface/modem 3902 provides half duplex communication. However, the invention is not limited to this communication mode. The invention is applicable and directed to other communication modes, as will be appreciated by persons skilled in the relevant art(s) based on the teachings contained herein.

In the embodiment shown in FIG. 39, the modulation/demodulation performed by the WLAN interface/modem 3902 is preferably direct sequence spread spectrum QPSK (quadrature phase shift keying) with differential encoding. However, the invention is not limited to this modulation/demodulation mode. The invention is applicable and directed to other modulation and demodulation modes, such as but not limited to those described herein, as well as frequency hopping according to IEEE 802.11, OFDM (orthogonal frequency division multiplexing), as well as others. These modulation/demodulation modes will be appreciated by persons skilled in the relevant art(s) based on the teachings contained herein.

The operation of the WLAN interface/modem 3902 when receiving shall now be described.

Signals 3922 received by the antenna 3903 are amplified by the LNA/PA 3904. The amplified signals 3924 are down-converted and demodulated by the receiver 3906. The receiver 3906 outputs I signal 3926 and Q signal 3928.

FIG. 40 illustrates an example receiver 3906 according to an embodiment of the invention. It is noted that the receiver 3906 shown in FIG. 40 represents a vector modulator. The "receiving" function performed by the WLAN interface/modem 3902 can be considered to be all processing performed by the WLAN interface/modem 3902 from the LNA/PA 3904 to generation of baseband information.

Signal 3924 is split by a 90 degree splitter 4001 to produce an I signal 4006A and Q signal 4006B that are preferably 90 degrees apart in phase. I and Q signals 4006A, 4006B are down-converted by UFD (universal frequency down-conversion) modules 4002A, 4002B. The UDF modules 4002A, 4002B output down-converted I and Q signals 3926, 3928. The UFD modules 4002A, 4002B each includes at least one UFT (universal frequency translation) module 4004A. UFD and UFT modules are described above. An example implementation of the receiver 3906 (vector demodulator) is shown in FIG. 53. An example BOM list for the receiver 3906 of FIG. 53 is shown in FIG. 54.

The demodulator/modulator facilitation module 3912 receives the I and Q signals 3926, 3928. The demodulator/modulator facilitation module 3912 amplifies and filters the I and Q signals 3926, 3928. The demodulator/modulator facilitation module 3912 also performs automatic gain control (AGC) functions. The AGC function is coupled with the universal frequency translation technology described herein. The demodulator/modulator facilitation module 3912 outputs processed I and Q signals 3930, 3932.

The MAC interface 3914 receives the processed I and Q signals 3930, 3932. The MAC interface 3914 preferably includes a baseband processor. The MAC interface 3914 preferably performs functions such as combining the I and Q signals 3930, 3932, and arranging the data according to the protocol/file formal being used. Other functions performed by the MAC interface 3914 and the baseband processor contained therein will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The MAC interface 3914 outputs the baseband information signal, which is received and processed by the computer 3916 in an implementation and application specific manner.

In the example embodiment of FIG. 39, the demodulation function is distributed among the receiver 3906, the demodulator/modulator facilitation module 3912, and a baseband processor contained in the MAC interface 3914. The functions collectively performed by these components include, but are not limited to, despreading the information, differentially decoding the information, tracking the carrier phase, descrambling, recreating the data clock, and combining the I and Q signals. The invention is not limited to this arrangement. These demodulation-type functions can be centralized in a single component, or distributed in other ways.

The operation of the WLAN interface/modem 3902 when transmitting shall now be described.

A baseband information signal 3936 is received by the MAC interface 3914 from the computer 3916. The MAC interface 3914 preferably performs functions such as splitting the baseband information signal to form I and Q signals 3930, 3932, and arranging the data according to the protocol/file formal being used. Other functions performed by the MAC interface 3914 and the baseband processor contained therein will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

The demodulator/modulator facilitation module 3912 filters and amplifies the I and Q signals 3930, 3932. The demodulator/modulator facilitation module 3912 outputs processed I and Q signals 3942, 3944. Preferably, at least some filtering and/or amplifying components in the demodulator/modulator facilitation module 3912 are used for both the transmit and receive paths.

The transmitter 3910 up-converts the processed I and Q signals 3942, 3944, and combines the up-converted I and Q signals. This up-converted/combined signal is amplified by the LNA/PA 3904, and then transmitted via the antenna 3904.

FIG. 41 illustrates an example transmitter 3910 according to an embodiment of the invention. The device in FIG. 41 can also be called a vector modulator. In an embodiment, the "transmit" function performed by the WLAN interface/modem 3902 can be considered to be all processing performed by the WLAN interface/modem 3902 from receipt of baseband information through the LNA/PA 3904. An example implementation of the transmitter 3910 (vector modulator) is shown in FIGS. 57-60. The data conditioning interfaces 5802 in FIG. 58 effectively pre-process the I and Q signals 3942, 3944 before being received by the UFU modules 4102. An example BOM list for the transmitter 3910 of FIGS. 57-60 is shown in FIGS. 61A and 61B.

I and Q signals 3942, 3944 are received by UFU (universal frequency up-conversion) modules 4102A, 4102B. The UFU modules 4102A, 4102B each includes at least one UFT module 4104A, 4104B. The UFU modules 4102A, 4102B up-convert I and Q signals 3942, 3944. The UFU modules 4102A, 4102B output up-converted I and Q signals 4106, 4108. The 90 degree combiner 4110 effectively phase shifts either the I signal 4106 or the Q signal 4108 by 90 degrees, and then combines the phase shifted signal with the unshifted signal to generate a combined, up-converted I/Q signal 3946.

In the example embodiment of FIG. 39, the modulation function is distributed among the transmitter 3910, the demodulator/modulator facilitation module 3912, and a baseband processor contained in the MAC interface 3914. The functions collectively performed by these components include, but are not limited to, differentially encoding data, splitting the baseband information signal into I and Q signals, scrambling data, and data spreading. The invention is not limited to this arrangement. These modulation-type functions can be centralized in a single component, or distributed in other ways.

An example implementation of the transmitter 3910 (vector modulator) is shown in FIGS. 57-60. The data conditioning interfaces 5802 in FIG. 58 effectively pre-process the I and Q signals 3942, 3944 before being received by the UFU modules 4102. An example BOM list for the transmitter 3910 of FIGS. 57-60 is shown in FIGS. 61A and 61B.

The components in the WLAN interface/modem 3902 are preferably controlled by the MAC interface 3914 in operation with the MAC 3918 in the computer 3916. This is represented by the distributed control arrow 3940 in FIG. 39. Such control includes setting the frequency, data rate, whether receiving or transmitting, and other communication characteristics/modes that will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. In embodiments, control signals are sent over the corresponding wireless medium and received by the antenna 3904, and sent to the MAC 3918.

FIG. 42 illustrates an example implementation of the WLAN interface/modem 3902. It is noted that in this implementation example, the MAC interface 3914 is located on a different board. FIG. 62 is an example motherboard corresponding to FIG. 42. FIG.

63 is an example bill-of-materials (BOM) list for the motherboard of FIG. 62. This and other implementations are provided herein for example purposes only. Other implementations will be apparent to persons skilled in the relevant art(s), and the invention is directed to such other implementations.

FIG. 102 illustrates an alternate example PCMCIA test bed assembly for a WLAN interface/modem 3902 according to an embodiment of the invention. In this embodiment, the baseband processor 10202 is separate from the MAC interface 3914.

In some applications, it is desired to separate the receive path and the transmit path. FIG. 43 illustrates an example receive implementation, and FIG. 44 illustrates an example transmit implementation.

7.2 Receiver

Example embodiments and implementations of the IQ receiver 3906 will be discussed as follows. The example embodiments and implementations include multi-phase embodiments that are useful for reducing or eliminating unwanted DC offsets and circuit re-radiation. The invention is not limited to these example receiver embodiments. Other receiver embodiments will be understood by those skilled in the relevant arts based on the discussion given herein. These other embodiments are within the scope and spirit of the present invention.

7.2.1 IQ Receiver

An example embodiment of the receiver 3906 is shown in FIG. 67A. Referring to FIG. 67A, the UFD module 4002A (FIG. 40) is configured so that the UFT module 4004A is coupled to a storage module 6704A. The UFT module 4004A is a controlled switch 6702A that is controlled by the control signal 3920A. The storage module 6704A is a capacitor 6706A. However, other storage modules could be used including an inductor, as will be understood by those skilled in the relevant arts. Likewise, the UFD module 4002B (FIG. 40) is configured so that the UFT module 4004B is coupled to a storage module 6704B. The UFT module 4004B is a controlled switch 6702B that is controlled by the control signal 3920B. The storage module 6704B is a capacitor 6706B. However, other storage modules could be used including an inductor, as will be understood by those skilled in the relevant arts. The operation of the receiver 3906 is discussed as follows.

The 90 degree splitter 4001 receives the received signal 3924 from the LNA/PA module 3904. The 90 degree splitter 4001 divides the signal 3924 into an I signal 4006A and a Q signal 4006B.

The UFD module 4002A receives the I signal 4006A and down-converts the I signal 4006A using the control signal 3920A to a lower frequency signal I 3926. More specifically, the controlled switch 6702A samples the I signal 4006A according to the control signal 3920A, transferring charge (or energy) to the storage module 6704A. The charge stored during successive samples of the I signal 4006A, results in the down-converted signal I signal 3926. Likewise, UFD module 4002B receives the Q signal 4006B and down-converts the Q signal 4006B using the control signal 3920B to a lower frequency signal Q 3928. More specifically, the controlled switch 6702B samples the Q signal 4006B according to the control signal 3920B, resulting in charge (or energy) that is stored in the storage module 6704B. The charge stored during successive samples of the I signal 4006A, results in the down-converted signal Q signal 3928.

Down-conversion utilizing a UFD module (also called an aliasing module) is further described in the above referenced applications, such as "Method and System for Down-converting Electromagnetic Signals," Ser. No. 09/176,022, now U.S. Patent No. 6,061,551. As discussed in the '551 patent, the control signals 3920A,B can be configured as a plurality of pulses that are established to improve energy transfer from the signals 4006A,B to the down-converted signals 3926 and 3928, respectively. In other words, the pulse widths of the control signals 3920 can be adjusted to increase and/or optimize the energy transfer from the signals 4006 to the down-converted output signals 3926 and 3938, respectively. Additionally, matched filter principles can be implemented to shape the sampling pulses of the control signal 3920, and therefore further improve energy transfer to the down-converted output signal 3106. Matched filter principle and energy transfer are further described in the above referenced applications, such as U.S. patent application titled, "Method and System for Down-Converting an Electromagnetic Signal, Transforms For Same, and Aperture Relationships", Ser. No. 09/550,644, filed on April 14, 2000.

The configuration of the UFT based receiver 3906 is flexible. In FIG. 67A, the controlled switches 6702 are in a series configuration relative to the signals 4006. Alternatively, FIG 67B illustrates the controlled switches 6702 in a shunt configuration so that the switches 6702 shunt the signals 4006 to ground.

Additionally in FIGs. 67A-B, the 90 degree phase shift between the I and Q channels is realized with the 90 degree splitter 4001. Alternatively, FIG. 68A illustrates a receiver 6806 in series configuration, where the 90 degree phase shift is realized by shifting the control signal 3920B by 90 degrees relative to the control signal 3920A. More specifically, the 90 degree shifter 6804 is added to shift the control signal 3920B by 90 degrees relative to the control signal 3920A. As such, the splitter 6802 is an in-phase (i.e. 0 degree) signal splitter. FIG. 68B illustrates an embodiment of the receiver 3906 of the receiver 3906 in a shunt configuration with 90 degree delays on the control signal.

Furthermore, the configuration of the controlled switch 6702 is also flexible. More specifically, the controlled switches 6702 can be implemented in many different ways, including transistor switches. FIG. 69A illustrates the UFT modules 6702 in a series configuration and implemented as FETs 6902, where the gate of each FET 6902 is controlled by the respective control signal 3920. As such, the FET 6902 samples the respective signal 4006, according to the respective control signal 3920. FIG. 69B illustrates the shunt configuration.

7.2.2 Multi-Phase IQ Receiver

FIG. 70A illustrates an exemplary I/Q modulation receiver 7000, according to an embodiment of the present invention. I/Q modulation receiver 7000 has additional advantages of reducing or eliminating unwanted DC offsets and circuit re-radiation. As will be apparent, the IQ receiver 7000 can be described as a multi-phase receiver to those skilled in the arts.

I/Q modulation receiver 7000 comprises a first UFD module 7002, a first optional filter 7004, a second UFD module 7006, a second optional filter 7008, a third UFD module 7010, a third optional filter 7012, a fourth UFD module 7014, a fourth filter 7016, an optional LNA 7018, a first differential amplifier 7020, a second differential amplifier 7022, and an antenna 7072.

I/Q modulation receiver 7000 receives, down-converts, and demodulates a I/Q modulated RF input signal 7082 to an I baseband output signal 7084, and a Q baseband output signal 7086. I/Q modulated RF input signal 7082 comprises a first information signal and a second information signal that are I/Q modulated onto an RF carrier signal. I baseband output signal 7084 comprises the first baseband information signal. Q baseband output signal 7086 comprises the second baseband information signal.

Antenna 7072 receives I/Q modulated RF input signal 7082. I/Q modulated RF input signal 7082 is output by antenna 7072 and received by optional LNA 7018. When present, LNA 7018 amplifies I/Q modulated RF input signal 7082, and outputs amplified I/Q signal 7088.

First UFD module 7002 receives amplified I/Q signal 7088. First UFD module 7002 down-converts the I-phase signal portion of amplified input I/Q signal 7088 according to an I control signal 7090. First UFD module 7002 outputs an I output signal 7098.

In an embodiment, first UFD module 7002 comprises a first storage module 7024, a first UFT module 7026, and a first voltage reference 7028. In an embodiment, a switch contained within first UFT module 7026 opens and closes as a function of I control signal 7090. As a result of the opening and closing of this switch, which respectively couples and de-couples first storage module 7024 to and from first voltage reference 7028, a down-converted signal, referred to as I output signal 7098, results. First voltage reference 7028 may be any reference voltage, and is preferably ground. I output signal 7098 is stored by first storage module 7024.

In an embodiment, first storage module 7024 comprises a first capacitor 7074. In addition to storing I output signal 7098, first capacitor 7074 reduces or prevents a DC offset voltage resulting from charge injection from appearing on I output signal 7098.

I output signal 7098 is received by optional first filter 7004. When present, first filter 7004 is in some embodiments a high pass filter to at least filter I output signal 7098 to remove any carrier signal "bleed through". In a preferred embodiment, when present, first filter 7004 comprises a first resistor 7030, a first filter capacitor 7032, and a first filter voltage reference 7034. Preferably, first resistor 7030 is coupled between I output signal 7098 and a filtered I output signal 7007, and first filter capacitor 7032 is coupled between filtered I output signal 7007 and first filter voltage reference 7034. Alternately, first filter 7004 may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant art(s). First filter 7004 outputs filtered I output signal 7007.

Second UFD module 7006 receives amplified I/Q signal 7088. Second UFD module 7006 down-converts the inverted I-phase signal portion of amplified input I/Q signal 7088 according to an inverted I control signal 7092. Second UFD module 7006 outputs an inverted I output signal 7001.

In an embodiment, second UFD module 7006 comprises a second storage module 7036, a second UFT module 7038, and a second voltage reference 7040. In an embodiment, a switch contained within second UFT module 7038 opens and closes as a function of inverted I control signal 7092. As a result of the opening and closing of this switch, which respectively couples and de-couples second storage module 7036 to and from second voltage reference 7040, a down-converted signal, referred to as inverted I output signal 7001, results. Second voltage reference 7040 may be any reference voltage, and is preferably ground. Inverted I output signal 7001 is stored by second storage module 7036.

In an embodiment, second storage module 7036 comprises a second capacitor 7076. In addition to storing inverted I output signal 7001, second capacitor 7076 reduces or prevents a DC offset voltage resulting from charge injection from appearing on inverted I output signal 7001.

Inverted I output signal 7001 is received by optional second filter 7008. When present, second filter 7008 is a high pass filter to at least filter inverted I output signal 7001 to remove any carrier signal "bleed through". In a preferred embodiment, when present, second filter 7008 comprises a second resistor 7042, a second filter capacitor

7044, and a second filter voltage reference 7046. Preferably, second resistor 7042 is coupled between inverted I output signal 7001 and a filtered inverted I output signal 7009, and second filter capacitor 7044 is coupled between filtered inverted I output signal 7009 and second filter voltage reference 7046. Alternately, second filter 7008 may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant art(s). Second filter 7008 outputs filtered inverted I output signal 7009.

First differential amplifier 7020 receives filtered I output signal 7007 at its non-inverting input and receives filtered inverted I output signal 7009 at its inverting input. First differential amplifier 7020 subtracts filtered inverted I output signal 7009 from filtered I output signal 7007, amplifies the result, and outputs I baseband output signal 7084. Because filtered inverted I output signal 7009 is substantially equal to an inverted version of filtered I output signal 7007, I baseband output signal 7084 is substantially equal to filtered I output signal 7009, with its amplitude doubled. Furthermore, filtered I output signal 7007 and filtered inverted I output signal 7009 may comprise substantially equal noise and DC offset contributions from prior down-conversion circuitry, including first UFD module 7002 and second UFD module 7006, respectively. When first differential amplifier 7020 subtracts filtered inverted I output signal 7009 from filtered I output signal 7007, these noise and DC offset contributions substantially cancel each other.

Third UFD module 7010 receives amplified I/Q signal 7088. Third UFD module 7010 down-converts the Q-phase signal portion of amplified input I/Q signal 7088 according to an Q control signal 7094. Third UFD module 7010 outputs an Q output signal 7003.

In an embodiment, third UFD module 7010 comprises a third storage module 7048, a third UFT module 7050, and a third voltage reference 7052. In an embodiment, a switch contained within third UFT module 7050 opens and closes as a function of Q control signal 7094. As a result of the opening and closing of this switch, which respectively couples and de-couples third storage module 7048 to and from third voltage reference 7052, a down-converted signal, referred to as Q output signal 7003, results.

Third voltage reference 7052 may be any reference voltage, and is preferably ground. Q output signal 7003 is stored by third storage module 7048.

In an embodiment, third storage module 7048 comprises a third capacitor 7078. In addition to storing Q output signal 7003, third capacitor 7078 reduces or prevents a DC offset voltage resulting from charge injection from appearing on Q output signal 7003.

Q output signal 7003 is received by optional third filter 7012. When present, in an embodiment, third filter 7012 is a high pass filter to at least filter Q output signal 7003 to remove any carrier signal "bleed through". In an embodiment, when present, third filter 7012 comprises a third resistor 7054, a third filter capacitor 7056, and a third filter voltage reference 7058. Preferably, third resistor 7054 is coupled between Q output signal 7003 and a filtered Q output signal 7011, and third filter capacitor 7056 is coupled between filtered Q output signal 7011 and third filter voltage reference 7058. Alternately, third filter 7012 may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant art(s). Third filter 7012 outputs filtered Q output signal 7011.

Fourth UFD module 7014 receives amplified I/Q signal 7088. Fourth UFD module 7014 down-converts the inverted Q-phase signal portion of amplified input I/Q signal 7088 according to an inverted Q control signal 7096. Fourth UFD module 7014 outputs an inverted Q output signal 7005.

In an embodiment, fourth UFD module 7014 comprises a fourth storage module 7060, a fourth UFT module 7062, and a fourth voltage reference 7064. In an embodiment, a switch contained within fourth UFT module 7062 opens and closes as a function of inverted Q control signal 7096. As a result of the opening and closing of this switch, which respectively couples and de-couples fourth storage module 7060 to and from fourth voltage reference 7064, a down-converted signal, referred to as inverted Q output signal 7005, results. Fourth voltage reference 7064 may be any reference voltage, and is preferably ground. Inverted Q output signal 7005 is stored by fourth storage module 7060.

In an embodiment, fourth storage module 7060 comprises a fourth capacitor 7080. In addition to storing inverted Q output signal 7005, fourth capacitor 7080 reduces or prevents a DC offset voltage resulting from charge injection from appearing on inverted Q output signal 7005.

Inverted Q output signal 7005 is received by optional fourth filter 7016. When present, fourth filter 7016 is a high pass filter to at least filter inverted Q output signal 7005 to remove any carrier signal "bleed through". In a preferred embodiment, when present, fourth filter 7016 comprises a fourth resistor 7066, a fourth filter capacitor 7068, and a fourth filter voltage reference 7070. Preferably, fourth resistor 7066 is coupled between inverted Q output signal 7005 and a filtered inverted Q output signal 7013, and fourth filter capacitor 7068 is coupled between filtered inverted Q output signal 7013 and fourth filter voltage reference 7070. Alternately, fourth filter 7016 may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant art(s). Fourth filter 7016 outputs filtered inverted Q output signal 7013.

Second differential amplifier 7022 receives filtered Q output signal 7011 at its non-inverting input and receives filtered inverted Q output signal 7013 at its inverting input. Second differential amplifier 7022 subtracts filtered inverted Q output signal 7013 from filtered Q output signal 7011, amplifies the result, and outputs Q baseband output signal 7086. Because filtered inverted Q output signal 7013 is substantially equal to an inverted version of filtered Q output signal 7011, Q baseband output signal 7086 is substantially equal to filtered Q output signal 7013, with its amplitude doubled. Furthermore, filtered Q output signal 7011 and filtered inverted Q output signal 7013 may comprise substantially equal noise and DC offset contributions of the same polarity from prior down-conversion circuitry, including third UFD module 7010 and fourth UFD module 7014, respectively. When second differential amplifier 7022 subtracts filtered inverted Q output signal 7013 from filtered Q output signal 7011, these noise and DC offset contributions substantially cancel each other.

Additional embodiments relating to addressing DC offset and re-radiation concerns, applicable to the present invention, are described in co-pending Patent Application No. 09/526,041,entitled "DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," Attorney Docket No. 1744.0880000, which is herein incorporated by reference in its entirety.

1744.0630003

7.2.2.1 Example I/Q Modulation Control Signal Generator Embodiments

FIG. 70B illustrates an exemplary block diagram for I/Q modulation control signal generator 7023, according to an embodiment of the present invention. I/Q modulation control signal generator 7023 generates I control signal 7090, inverted I control signal 7092, Q control signal 7094, and inverted Q control signal 7096 used by I/Q modulation receiver 7000 of FIG. 70A. I control signal 7090 and inverted I control signal 7092 operate to down-convert the I-phase portion of an input I/Q modulated RF signal. Q control signal 7094 and inverted Q control signal 7096 act to down-convert the Q-phase portion of the input I/Q modulated RF signal. Furthermore, I/Q modulation control signal generator 7023 has the advantage of generating control signals in a manner such that resulting collective circuit re-radiation is radiated at one or more frequencies outside of the frequency range of interest. For instance, potential circuit re-radiation is radiated at a frequency substantially greater than that of the input RF carrier signal frequency.

I/Q modulation control signal generator 7023 comprises a local oscillator 7025, a first divide-by-two module 7027, a 180 degree phase shifter 7029, a second divide-by-two module 7031, a first pulse generator 7033, a second pulse generator 7035, a third pulse generator 7037, and a fourth pulse generator 7039.

Local oscillator 7025 outputs an oscillating signal 7015. FIG. 70C shows an exemplary oscillating signal 7015.

First divide-by-two module 7027 receives oscillating signal 7015, divides oscillating signal 7015 by two, and outputs a half frequency LO signal 7017 and a half frequency inverted LO signal 7041. FIG. 70C shows an exemplary half frequency LO signal 7017. Half frequency inverted LO signal 7041 is an inverted version of half frequency LO signal 7017. First divide-by-two module 7027 may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant art(s).

180 degree phase shifter 7029 receives oscillating signal 7015, shifts the phase of oscillating signal 7015 by 180 degrees, and outputs phase shifted LO signal 7019. 180 degree phase shifter 7029 may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant art(s). In alternative embodiments, other amounts of phase shift may be used.

Second divide-by two module 7031 receives phase shifted LO signal 7019, divides phase shifted LO signal 7019 by two, and outputs a half frequency phase shifted LO signal 7021 and a half frequency inverted phase shifted LO signal 7043. FIG. 70C shows an exemplary half frequency phase shifted LO signal 7021. Half frequency inverted phase shifted LO signal 7043 is an inverted version of half frequency phase shifted LO signal 7021. Second divide-by-two module 7031 may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant art(s).

First pulse generator 7033 receives half frequency LO signal 7017, generates an output pulse whenever a rising edge is received on half frequency LO signal 7017, and outputs I control signal 7090. FIG. 70C shows an exemplary I control signal 7090.

Second pulse generator 7035 receives half frequency inverted LO signal 7041, generates an output pulse whenever a rising edge is received on half frequency inverted LO signal 7041, and outputs inverted I control signal 7092. FIG. 70C shows an exemplary inverted I control signal 7092.

Third pulse generator 7037 receives half frequency phase shifted LO signal 7021, generates an output pulse whenever a rising edge is received on half frequency phase shifted LO signal 7021, and outputs Q control signal 7094. FIG. 70C shows an exemplary Q control signal 7094.

Fourth pulse generator 7039 receives half frequency inverted phase shifted LO signal 7043, generates an output pulse whenever a rising edge is received on half frequency inverted phase shifted LO signal 7043, and outputs inverted Q control signal 7096. FIG. 70C shows an exemplary inverted Q control signal 7096.

In an embodiment, control signals 7090, 7021, 7041 and 7043 include pulses having a width equal to one-half of a period of I/Q modulated RF input signal 7082. The invention, however, is not limited to these pulse widths, and control signals 7090, 7021, 7041, and 7043 may comprise pulse widths of any fraction of, or multiple and fraction of, a period of I/Q modulated RF input signal 7082.

First, second, third, and fourth pulse generators 7033, 7035, 7037, and 7039 may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant art(s).

As shown in FIG. 70C, in an embodiment, control signals 7090, 7021, 7041, and 7043 comprise pulses that are non-overlapping in other embodiments the pulses may overlap. Furthermore, in this example, pulses appear on these signals in the following order: I control signal 7090, Q control signal 7094, inverted I control signal 7092, and inverted Q control signal 7096. Potential circuit re-radiation from I/Q modulation receiver 7000 may comprise frequency components from a combination of these control signals.

For example, FIG. 70D shows an overlay of pulses from I control signal 7090, Q control signal 7094, inverted I control signal 7092, and inverted Q control signal 7096. When pulses from these control signals leak through first, second, third, and/or fourth UFD modules 7002, 7006, 7010, and 7014 to antenna 7072 (shown in FIG. 70A), they may be radiated from I/Q modulation receiver 7000, with a combined waveform that appears to have a primary frequency equal to four times the frequency of any single one of control signals 7090, 7021, 7041, and 7043. FIG. 70 shows an example combined control signal 7045.

FIG. 70D also shows an example I/Q modulation RF input signal 7082 overlaid upon control signals 7090, 7094, 7092, and 7096. As shown in FIG. 70D, pulses on I control signal 7090 overlay and act to down-convert a positive I-phase portion of I/Q modulation RF input signal 7082. Pulses on inverted I control signal 7092 overlay and act to down-convert a negative I-phase portion of I/Q modulation RF input signal 7082. Pulses on Q control signal 7094 overlay and act to down-convert a rising Q-phase portion of I/Q modulation RF input signal 7082. Pulses on inverted Q control signal 7096 overlay and act to down-convert a falling Q-phase portion of I/Q modulation RF input signal 7082.

As FIG. 70D further shows in this example, the frequency ratio between the combination of control signals 7090, 7021, 7041, and 7043 and I/Q modulation RF input signal 7082 is approximately 4:3. Because the frequency of the potentially re-radiated signal, i.e., combined control signal 7045, is substantially different from that of the signal being down-converted, i.e., I/Q modulation RF input signal 7082, it does not interfere with signal down-conversion as it is out of the frequency band of interest, and hence may be filtered out. In this manner, I/Q modulation receiver 7000 reduces problems due to circuit re-radiation. As will be understood by persons skilled in the relevant art(s) from the teachings herein, frequency ratios other than 4:3 may be implemented to achieve similar reduction of problems of circuit re-radiation.

It should be understood that the above control signal generator circuit example is provided for illustrative purposes only. The invention is not limited to these embodiments. Alternative embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) for I/Q modulation control signal generator 7023 will be apparent to persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the present invention.

FIG. 70S illustrates the receiver 7000, where the UFT modules 7028, 7038, 7050, and 7062 are configured with FETs 7099a-d.

Additional embodiments relating to addressing DC offset and re-radiation concerns, applicable to the present invention, are described in co-pending patent application no. 09/526, 041, entitled "DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," which is herein incorporated by reference in its entirety.

7.2.2.2 Implementation of Multi-phase I/Q Modulation Receiver Embodiment with Exemplary Waveforms

FIG. 70E illustrates a more detailed example circuit implementation of I/Q modulation receiver 7000, according to an embodiment of the present invention. FIGS.

70F-P show example waveforms related to an example implementation of I/Q modulation receiver 7000 of FIG. 70E.

FIGS. 70F and 70G show first and second input data signals 7047 and 7049 to be I/Q modulated with a RF carrier signal frequency as the I-phase and Q-phase information signals, respectively.

FIGS. 70I and 70J show the signals of FIG. 70F and 70G after modulation with a RF carrier signal frequency, respectively, as I-modulated signal 7051 and Q-modulated signal 7053.

FIG. 70H shows an I/Q modulation RF input signal 7082 formed from I-modulated signal 7051 and Q-modulated signal 7053 of FIGS. 70I and 70J, respectively.

FIG. 70O shows an overlaid view of filtered I output signal 7007 and filtered inverted I output signal 7009.

FIG. 70P shows an overlaid view of filtered Q output signal 7011 and filtered inverted Q output signal 7013.

FIGS. 70K and 70L show I baseband output signal 7084 and Q baseband output signal 7086, respectfully. A data transition 7055 is indicated in both I baseband output signal 7084 and Q baseband output signal 7086. The corresponding data transition 7055 is indicated in I-modulated signal 7051 of FIG. 70I, Q-modulated signal 7053 of FIG. 70J, and I/Q modulation RF input signal 7082 of FIG. 70H.

FIGS. 70M and 70N show I baseband output signal 7084 and Q baseband output signal 7086 over a wider time interval.

7.2.2.3 Example Single Channel Receiver Embodiment

FIG. 70Q illustrates an example single channel receiver 7091, corresponding to either the I or Q channel of I/Q modulation receiver 7000, according to an embodiment of the present invention. Single channel receiver 7091 can down-convert an input RF signal 7097 modulated according to AM, PM, FM, and other modulation schemes. Refer to section 7.2.1 above for further description on the operation of single channel receiver

7091. In other words, the single channel receiver 7091 is a one channel of the IQ receiver 7000 that was discussed in section 7.2.1.

7.2.2.4 Alternative Example I/Q Modulation Receiver Embodiment

FIG. 70R illustrates an exemplary I/Q modulation receiver 7089, according to an embodiment of the present invention. I/Q modulation receiver 7089 receives, down-converts, and demodulates an I/Q modulated RF input signal 7082 to an I baseband output signal 7084, and a Q baseband output signal 7086. I/Q modulation receiver 7089 has additional advantages of reducing or eliminating unwanted DC offsets and circuit re-radiation, in a similar fashion to that of I/Q modulation receiver 7000 described above.

7.3 Transmitter

Example embodiments and implementations of the IQ transmitter 3910 will be discussed as follows. The example embodiments and implementations include multi-phase embodiments that are useful for reducing or eliminating unwanted DC offsets that can result in unwanted carrier insertion.

7.3.1 Universal Transmitter with 2 UFT Modules

FIG. 71A illustrates a transmitter 7102 according to embodiments of the present invention. Transmitter 7102 includes a balanced modulator/up-converter 7104, a control signal generator 7142, an optional filter 7106, and an optional amplifier 7108. Transmitter 7102 up-converts a baseband signal 7110 to produce an output signal 7140 that is conditioned for wireless or wire line transmission. In doing so, the balanced modulator 7104 receives the baseband signal 7110 and samples the baseband signal in a differential and balanced fashion to generate a harmonically rich signal 7138. The harmonically rich signal 7138 includes multiple harmonic images, where each image contains the baseband information in the baseband signal 7110. The optional bandpass filter 7106 may be included to select a harmonic of interest (or a subset of harmonics) in the signal 7138 for transmission. The optional amplifier 7108 may be included to amplify the selected harmonic prior to transmission. The universal transmitter is further described at a high level by the flowchart 8400 that is shown in FIG. 84. A more detailed structural and operational description of the balanced modulator follows thereafter.

Referring to flowchart 8400, in step 8402, the balanced modulator 7104 receives the baseband signal 7110.

In step 8404, the balanced modulator 7104 samples the baseband signal in a differential and balanced fashion according to a first and second control signals that are phase shifted with respect to each other. The resulting harmonically rich signal 7138 includes multiple harmonic images that repeat at harmonics of the sampling frequency, where each image contains the necessary amplitude and frequency information to reconstruct the baseband signal 7110.

In embodiments of the invention, the control signals include pulses having pulse widths (or apertures) that are established to improve energy transfer to a desired harmonic of the harmonically rich signal 7138. In further embodiments of the invention, DC offset voltages are minimized between sampling modules as indicated in step 8406, thereby minimizing carrier insertion in the harmonic images of the harmonically rich signal 7138.

In step 8408, the optional bandpass filter 7106 selects the desired harmonic of interest (or a subset of harmonics) in from the harmonically rich signal 7138 for transmission.

In step 8410, the optional amplifier 7108 amplifies the selected harmonic(s) prior to transmission.

In step 8412, the selected harmonic(s) is transmitted over a communications medium.

7.3.1.1 Balanced Modulator Detailed Description

Referring to the example embodiment shown in FIG. 71A, the balanced modulator 7104 includes the following components: a buffer/inverter 7112; summer amplifiers 7118, 7119; UFT modules 7124 and 7128 having controlled switches 7148 and 7150, respectively; an inductor 7126; a blocking capacitor 7136; and a DC terminal 7111. As stated above, the balanced modulator 7104 differentially samples the baseband signal 7110 to generate a harmonically rich signal 7138. More specifically, the UFT modules 7124 and 7128 sample the baseband signal in differential fashion according to control signals 7123 and 7127, respectively. A DC reference voltage 7113 is applied to terminal 7111 and is uniformly distributed to the UFT modules 7124 and 7128. The distributed DC voltage 7113 prevents any DC offset voltages from developing between the UFT modules, which can lead to carrier insertion in the harmonically rich signal 7138. The operation of the balanced modulator 7104 is discussed in greater detail with reference to flowchart 8500 (FIG. 85), as follows.

In step 8402, the buffer/inverter 7112 receives the input baseband signal 7110 and generates input signal 7114 and inverted input signal 7116. Input signal 7114 is substantially similar to signal 7110, and inverted signal 7116 is an inverted version of signal 7114. As such, the buffer/inverter 7112 converts the (single-ended) baseband signal 7110 into differential input signals 7114 and 7116 that will be sampled by the UFT modules. Buffer/inverter 7112 can be implemented using known operational amplifier (op amp) circuits, as will be understood by those skilled in the arts, although the invention is not limited to this example.

In step 8504, the summer amplifier 7118 sums the DC reference voltage 7113 applied to terminal 7111 with the input signal 7114, to generate a combined signal 7120. Likewise, the summer amplifier 7119 sums the DC reference voltage 7113 with the inverted input signal 7116 to generate a combined signal 7122. Summer amplifiers 7118 and 7119 can be implemented using known op amp summer circuits, and can be designed to have a specified gain or attenuation, including unity gain, although the invention is not limited to this example. The DC reference voltage 7113 is also distributed to the outputs of both UFT modules 7124 and 7128 through the inductor 7126 as is shown.

In step 8506, the control signal generator 7142 generates control signals 7123 and 7127 that are shown by way of example in FIG. 72B and FIG. 72C, respectively. As illustrated, both control signals 7123 and 7127 have the same period T_S as a master clock signal 7145 (FIG.72A), but have a pulse width (or aperture) of T_A. In the example, control signal 7123 triggers on the rising pulse edge of the master clock signal 7145, and control signal 7127 triggers on the falling pulse edge of the master clock signal 7145. Therefore, control signals 7123 and 7127 are shifted in time by 180 degrees relative to each other. In embodiments of invention, the master clock signal 7145 (and therefore the control signals 7123 and 7127) have a frequency that is a sub-harmonic of the desired output signal 7140. The invention is not limited to the example of FIGs. 72A-72C.

In one embodiment, the control signal generator 7142 includes an oscillator 7146, pulse generators 7144a and 7144b, and an inverter 7147 as shown. In operation, the oscillator 7146 generates the master clock signal 7145, which is illustrated in FIG. 72A as a periodic square wave having pulses with a period of T_S. Other clock signals could be used including but not limited to sinusoidal waves, as will be understood by those skilled in the arts. Pulse generator 7144a receives the master clock signal 7145 and triggers on the rising pulse edge, to generate the control signal 7123. Inverter 7147 inverts the clock signal 7145 to generate an inverted clock signal 7143. The pulse generator 7144b receives the inverted clock signal 7143 and triggers on the rising pulse edge (which is the falling edge of clock signal 7145), to generate the control signal 7127.

FIG 89A-E illustrate example embodiments for the pulse generator 7144. FIG. 89A illustrates a pulse generator 8902. The pulse generator 8902 generates pulses 8908 having pulse width T_A from an input signal 8904. Example input signals 8904 and pulses 8908 are depicted in FIGs 89B and 89C, respectively. The input signal 8904 can be any type of periodic signal, including, but not limited to, a sinusoid, a square wave, a saw-tooth wave etc. The pulse width (or aperture) T_A of the pulses 8908 is determined by delay 8906 of the pulse generator 8902. The pulse generator 8902 also includes an optional inverter 8910, which is optionally added for polarity considerations as understood by those skilled in the arts. The example logic and implementation shown for the pulse generator 8902 is provided for illustrative purposes only, and is not limiting. The actual logic employed can take many forms. Additional examples of pulse generation logic are shown in FIGs. 89D and 89E. FIG. 89D illustrates a rising edge pulse generator 8912 that triggers on the rising edge of input signal 8904. FIG. 89E illustrates a falling edge pulse generator 8916 that triggers on the falling edge of the input signal 8904.

In step 8508, the UFT module 7124 samples the combined signal 7120 according to the control signal 7123 to generate harmonically rich signal 7130. More specifically, the switch 7148 closes during the pulse widths T_A of the control signal 7123 to sample the combined signal 7120 resulting in the harmonically rich signal 7130. FIG. 71B illustrates an exemplary frequency spectrum for the harmonically rich signal 7130 having harmonic images 7152a-n. The images 7152 repeat at harmonics of the sampling frequency $1/T_S$, at infinitum, where each image 7152 contains the necessary amplitude, frequency, and phase information to reconstruct the baseband signal 7110. As discussed further below, the relative amplitude of the frequency images is generally a function of the harmonic number and the pulse width T_A. As such, the relative amplitude of a particular harmonic 7152 can be increased (or decreased) by adjusting the pulse width T_A of the control signal 7123. In general, shorter pulse widths of T_A shift more energy into the higher frequency harmonics, and longer pulse widths of T_A shift energy into the lower frequency harmonics. The generation of harmonically rich signals by sampling an input signal according to a controlled aperture have been described earlier in this application in the section titled, "Frequency Up-conversion Using Universal Frequency Translation", and is illustrated by FIGs. 3-6. A more detailed discussion of frequency up-conversion using a switch with a controlled sampling aperture is discussed in the co-pending patent application titled, "Method and System for Frequency Up-Conversion," Ser. No./09/176,154, field on October 21, 1998, and incorporated herein by reference.

In step 8510, the UFT module 7128 samples the combined signal 7122 according to the control signal 7127 to generate harmonically rich signal 7134. More specifically, the switch 7150 closes during the pulse widths T_A of the control signal 7127 to sample the combined signal 7122 resulting in the harmonically rich signal 7134. The harmonically rich signal 7134 includes multiple frequency images of baseband signal 7110 that repeat at harmonics of the sampling frequency ($1/T_S$), similar to that for the harmonically rich signal 7130. However, the images in the signal 7134 are phase-shifted compared to those in signal 7130 because of the inversion of signal 7116 compared to signal 7114, and because of the relative phase shift between the control signals 7123 and 7127.

In step 8512, the node 7132 sums the harmonically rich signals 7130 and 7134 to generate harmonically rich signal 7133. FIG. 71C illustrates an exemplary frequency spectrum for the harmonically rich signal 7133 that has multiple images 7154a-n that repeat at harmonics of the sampling frequency $1/T_S$. Each image 7154 includes the necessary amplitude, frequency and phase information to reconstruct the baseband signal 7110. The capacitor 7136 operates as a DC blocking capacitor and substantially passes the harmonics in the harmonically rich signal 7133 to generate harmonically rich signal 7138 at the output of the modulator 7104.

In step 8408, the optional filter 7106 can be used to select a desired harmonic image for transmission. This is represented for example by a passband 7156 that selects the harmonic image 7154c for transmission in FIG. 71C.

An advantage of the modulator 7104 is that it is fully balanced, which substantially minimizes (or eliminates) any DC voltage offset between the two UFT modules 7124 and 7128. DC offset is minimized because the reference voltage 7113 contributes a consistent DC component to the input signals 7120 and 7122 through the summing amplifiers 7118 and 7119, respectively. Furthermore, the reference voltage 7113 is also directly coupled to the outputs of the UFT modules 7124 and 7128 through the inductor 7126 and the node 7132. The result of controlling the DC offset between the UFT modules is that carrier insertion is minimized in the harmonic images of the harmonically rich signal 7138. As discussed above, carrier insertion is substantially wasted energy because the information for a modulated signal is carried in the sidebands of the modulated signal and not in the carrier. Therefore, it is often desirable to minimize the energy at the carrier frequency by controlling the relative DC offset.

7.3.1.2 Balanced Modulator Example Signal Diagrams and Mathematical Description

In order to further describe the invention, FIGs. 72D-72I illustrate various example signal diagrams (vs. time) that are representative of the invention. These signal diagrams are meant for example purposes only and are not meant to be limiting. FIG. 72D illustrates a signal 7202 that is representative of the input baseband signal 7110 (FIG. 71A). FIG. 72E illustrates a step function 7204 that is an expanded portion of the signal 7202 from time t_0 to t_1, and represents signal 7114 at the output of the buffer/inverter 7112. Similarly, FIG. 72F illustrates a signal 7206 that is an inverted version of the signal 7204, and represents the signal 7116 at the inverted output of buffer/inverter 7112. For analysis purposes, a step function is a good approximation for a portion of a single bit of data (for the baseband signal 7110) because the clock rates of the control signals 7123 and 7127 are significantly higher than the data rates of the baseband signal 7110. For example, if the data rate is in the KHz frequency range, then the clock rate will preferably be in MHZ frequency range in order to generate an output signal in the Ghz frequency range.

Still referring to FIGs. 72D-I, FIG. 72G illustrates a signal 7208 that an example of the harmonically rich signal 7130 when the step function 7204 is sampled according to the control signal 7123 in FIG. 72B. The signal 7208 includes positive pulses 7209 as referenced to the DC voltage 7113. Likewise, FIG. 72H illustrates a signal 7210 that is an example of the harmonically rich signal 7134 when the step function 7206 is sampled according to the control signal 7127. The signal 7210 includes negative pulses 7211 as referenced to the DC voltage 7113, which are time-shifted relative the positive pulses 7209 in signal 7208.

Still referring to FIGs. 72D-I, the FIG. 72I illustrates a signal 7212 that is the combination of signal 7208 (FIG. 72G) and the signal 7210 (FIG. 72H), and is an example of the harmonically rich signal 7133 at the output of the summing node 7132. As illustrated, the signal 7212 spends approximately as much time above the DC reference voltage 7113 as below the DC reference voltage 7113 over a limited time period. For example, over a time period 7214, the energy in the positive pulses 7209a-b is canceled out by the energy in the negative pulses 7211a-b. This is indicative of minimal (or zero) DC offset between the UFT modules 7124 and 7128, which results in minimal carrier insertion during the sampling process.

Still referring to FIG. 72I, the time axis of the signal 7212 can be phased in such a manner to represent the waveform as an odd function. For such an arrangement, the Fourier series is readily calculated to obtain:

$$I_c(t) = \sum_{n=1}^{\infty} \left(\frac{4\sin\left(\frac{n\pi T_A}{T_s}\right) \cdot \sin\left(\frac{n\pi}{2}\right)}{n\pi} \right) \cdot \sin\left(\frac{2n\pi t}{T_s}\right) \qquad \textbf{\textit{Equation 1.}}$$

where: T_S = period of the master clock 7145

T_A = pulse width of the control signals 7123 and 7127

n= harmonic number

As shown by Equation 1, the relative amplitude of the frequency images is generally a function of the harmonic number *n,* and the ratio of T_A/T_S. As indicated, the T_A/T_S ratio represents the ratio of the pulse width of the control signals relative to the period of the sub-harmonic master clock. The T_A/T_S ratio can be optimized in order to maximize the amplitude of the frequency image at a given harmonic. For example, if a passband waveform is desired to be created at 5x the frequency of the sub-harmonic clock, then a baseline power for that harmonic extraction may be calculated for the fifth harmonic (n=5) as:

$$I_c(t) = \left(\frac{4 \sin\left(\frac{5\pi T_A}{T_s} \right)}{5\pi} \right) \cdot \sin(5\omega_s t) \qquad \textbf{\textit{Equation 2.}}$$

As shown by Equation 2, $I_C(t)$ for the fifth harmonic is a sinusoidal function having an amplitude that is proportional to the sin $(5\pi T_A/T_S)$. The signal amplitude can be maximized by setting $T_A = (1/10 \cdot T_S)$ so that $\sin(5\pi T_A/T_S) = \sin(\pi/2) = 1$. Doing so results in the equation:

$$I_c(t)\big|_{n=5} = \frac{4}{5\pi}\left(\sin\left(5\omega_s t\right)\right) \qquad \textbf{\textit{Equation 3.}}$$

This component is a frequency at 5x of the sampling frequency of sub-harmonic clock, and can be extracted from the Fourier series via a bandpass filter (such as bandpass filter 7106) that is centered around $5f_S$. The extracted frequency component can then be optionally amplified by the amplifier 7108 prior to transmission on a wireless or wire-line communications channel or channels.

Equation 3 can be extended to reflect the inclusion of a message signal as illustrated by equation 4 below:

$$m(t) \cdot I_c(t)\big|_{\substack{n=5 \\ \theta=\theta(t)}} = \frac{4 \cdot m(t)}{5\pi}\left(\sin\left(5\omega_s t + 5\theta(t)\right)\right) \qquad \textbf{\textit{Equation 4.}}$$

Equation 4 illustrates that a message signal can be carried in harmonically rich signals 7133 such that both amplitude and phase can be modulated. In other words, m(t) is modulated for amplitude and $\theta(t)$ is modulated for phase. In such cases, it should be noted that $\theta(t)$ is augmented modulo *n* while the amplitude modulation *m(t)* is simply scaled.

Therefore, complex waveforms may be reconstructed from their Fourier series with multiple aperture UFT combinations.

As discussed above, the signal amplitude for the 5th harmonic was maximized by setting the sampling aperture width T_A= 1/10 T_S, where T_S is the period of the master clock signal. This can be restated and generalized as setting T_A= ½ the period (or π radians) at the harmonic of interest. In other words, the signal amplitude of any harmonic *n* can be maximized by sampling the input waveform with a sampling aperture of T_A= ½ the period of the harmonic of interest (*n*). Based on this discussion, it is apparent that varying the aperture changes the harmonic and amplitude content of the output waveform. For example, if the sub-harmonic clock has a frequency of 200 MHZ, then the fifth harmonic is at 1Ghz. The amplitude of the fifth harmonic is maximized by setting the aperture width T_A= 500 picoseconds, which equates to ½ the period (or π radians) at 1 Ghz.

FIG. 72J depicts a frequency plot 7216 that graphically illustrates the effect of varying the sampling aperture of the control signals on the harmonically rich signal 7133 given a 200 MHZ harmonic clock. The frequency plot 7216 compares two frequency spectrums 7218 and 7220 for different control signal apertures given a 200 MHZ clock. More specifically, the frequency spectrum 7218 is an example spectrum for signal 7133 given the 200 MHZ clock with the aperture T_A = 500 psec (where 500 psec is π radians at the 5th harmonic of 1GHz). Similarly, the frequency spectrum 7220 is an example spectrum for signal 7133 given a 200 MHZ clock that is a square wave (so T_A = 5000 psec). The spectrum 7218 includes multiple harmonics 7218a-I, and the frequency spectrum 7220 includes multiple harmonics 7220a-e. [It is noted that spectrum 7220 includes only the odd harmonics as predicted by Fourier analysis for a square wave.] At 1 Ghz (which is the 5th harmonic), the signal amplitude of the two frequency spectrums 7218e and 7220c are approximately equal. However, at 200 MHZ, the frequency spectrum 7218a has a much lower amplitude than the frequency spectrum 7220a, and therefore the frequency spectrum 7218 is more efficient than the frequency spectrum 7220, assuming the desired harmonic is the 5th harmonic. In other words, assuming 1 Ghz is the desired harmonic, the frequency spectrum 7218 wastes less energy at the 200 MHZ fundamental than does the frequency spectrum 7218.

7.3.1.3 Balanced Modulator Having a Shunt Configuration

FIG. 79A illustrates a universal transmitter 7900 that is a second embodiment of a universal transmitter having two balanced UFT modules in a shunt configuration. (In contrast, the balanced modulator 7104 can be described as having a series configuration based on the orientation of the UFT modules.) Transmitter 7900 includes a balanced modulator 7901, the control signal generator 7142, the optional bandpass filter 7106, and the optional amplifier 7108. The transmitter 7900 up-converts a baseband signal 7902 to produce an output signal 7936 that is conditioned for wireless or wire line transmission. In doing so, the balanced modulator 7901 receives the baseband signal 7902 and shunts the baseband signal to ground in a differential and balanced fashion to generate a harmonically rich signal 7934. The harmonically rich signal 7934 includes multiple harmonic images, where each image contains the baseband information in the baseband signal 7902. In other words, each harmonic image includes the necessary amplitude, frequency, and phase information to reconstruct the baseband signal 7902. The optional bandpass filter 7106 may be included to select a harmonic of interest (or a subset of harmonics) in the signal 7934 for transmission. The optional amplifier 7108 may be included to amplify the selected harmonic prior to transmission, resulting in the output signal 7936.

The balanced modulator 7901 includes the following components: a buffer/inverter 7904; optional impedances 7910, 7912; UFT modules 7916 and 7922 having controlled switches 7918 and 7924, respectively; blocking capacitors 7928 and 7930; and a terminal 7920 that is tied to ground. As stated above, the balanced modulator 7901 differentially shunts the baseband signal 7902 to ground, resulting in a harmonically rich signal 7934. More specifically, the UFT modules 7916 and 7922 alternately shunts the baseband signal to terminal 7920 according to control signals 7123 and 7127, respectively. Terminal 7920 is tied to ground and prevents any DC offset voltages from developing between the UFT modules 7916 and 7922. As described above, a DC offset voltage can lead to undesired carrier insertion. The operation of the balanced modulator 7901 is described in greater detail according to the flowchart 8600 (FIG. 86) as follows.

In step 8402, the buffer/inverter 7904 receives the input baseband signal 7902 and generates I signal 7906 and inverted I signal 7908. I signal 7906 is substantially similar to the baseband signal 7902, and the inverted I signal 7908 is an inverted version of signal 7902. As such, the buffer/inverter 7904 converts the (single-ended) baseband signal 7902 into differential signals 7906 and 7908 that are sampled by the UFT modules. Buffer/inverter 7904 can be implemented using known operational amplifier (op amp) circuits, as will be understood by those skilled in the arts, although the invention is not limited to this example.

In step 8604, the control signal generator 7142 generates control signals 7123 and 7127 from the master clock signal 7145. Examples of the master clock signal 7145, control signal 7123, and control signal 7127 are shown in FIGs. 72A-C, respectively. As illustrated, both control signals 7123 and 7127 have the same period T_S as a master clock signal 7145, but have a pulse width (or aperture) of T_A. Control signal 7123 triggers on the rising pulse edge of the master clock signal 7145, and control signal 7127 triggers on the falling pulse edge of the master clock signal 7145. Therefore, control signals 7123 and 7127 are shifted in time by 180 degrees relative to each other. A specific embodiment of the control signal generator 7142 is illustrated in FIG. 71A, and was discussed in detail above.

In step 8606, the UFT module 7916 shunts the signal 7906 to ground according to the control signal 7123, to generate a harmonically rich signal 7914. More specifically, the switch 7918 closes and shorts the signal 7906 to ground (at terminal 7920) during the aperture width T_A of the control signal 7123, to generate the harmonically rich signal 7914. FIG. 79B illustrates an exemplary frequency spectrum for the harmonically rich signal 7918 having harmonic images 7950a-n. The images 7950 repeat at harmonics of the sampling frequency $1/T_S$, at infinitum, where each image 7950 contains the necessary amplitude, frequency, and phase information to reconstruct the baseband signal 7902. The generation of harmonically rich signals by sampling an input signal according to a controlled aperture have been described earlier in this application in the section titled, "Frequency Up-conversion Using Universal Frequency Translation", and is illustrated by FIGs. 3-6. A more detailed discussion of frequency up-conversion using a switch with a controlled sampling aperture is discussed in the co-pending patent application titled, "Method and System for Frequency Up-Conversion," Ser. No./09/176,154, field on October 21, 1998, and incorporated herein by reference.

The relative amplitude of the frequency images 7950 are generally a function of the harmonic number and the pulse width T_A. As such, the relative amplitude of a particular harmonic 7950 can be increased (or decreased) by adjusting the pulse width T_A of the control signal 7123. In general, shorter pulse widths of T_A shift more energy into the higher frequency harmonics, and longer pulse widths of T_A shift energy into the lower frequency harmonics, as described by equations 1-4 above. Additionally, the relative amplitude of a particular harmonic 7950 can also be adjusted by adding/tuning an optional impedance 7910. Impedance 7910 operates as a filter that emphasizes a particular harmonic in the harmonically rich signal 7914.

In step 8608, the UFT module 7922 shunts the inverted signal 7908 to ground according to the control signal 7127, to generate a harmonically rich signal 7926. More specifically, the switch 7924 closes during the pulse widths T_A and shorts the inverted I signal 7908 to ground (at terminal 7920), to generate the harmonically rich signal 7926. At any given time, only one of input signals 7906 or 7908 is shorted to ground because the pulses in the control signals 7123 and 7127 are phase shifted with respect to each other, as shown in FIGs. 72B and 72C.

The harmonically rich signal 7926 includes multiple frequency images of baseband signal 7902 that repeat at harmonics of the sampling frequency ($1/T_S$), similar to that for the harmonically rich signal 7914. However, the images in the signal 7926 are phase-shifted compared to those in signal 7914 because of the inversion of the signal 7908 compared to the signal 7906, and because of the relative phase shift between the control signals 7123 and 7127. The optional impedance 7912 can be included to emphasis a particular harmonic of interest, and is similar to the impedance 7910 above.

In step 8610, the node 7932 sums the harmonically rich signals 7914 and 7926 to generate the harmonically rich signal 7934. The capacitors 7928 and 7930 operate as blocking capacitors that substantially pass the respective harmonically rich signals 7914 and 7926 to the node 7932. (The capacitor values may be chosen to substantially block baseband frequency components as well.) FIG. 79C illustrates an exemplary frequency spectrum for the harmonically rich signal 7934 that has multiple images 7952a-n that repeat at harmonics of the sampling frequency $1/T_S$. Each image 7952 includes the necessary amplitude, frequency, and phase information to reconstruct the baseband signal 7902. The optional filter 7106 can be used to select the harmonic image of interest for transmission. This is represented by a passband 7956 that selects the harmonic image 7932c for transmission.

An advantage of the modulator 7901 is that it is fully balanced, which substantially minimizes (or eliminates) any DC voltage offset between the two UFT modules 7912 and 7914. DC offset is minimized because the UFT modules 7916 and 7922 are both connected to ground at terminal 7920. The result of controlling the DC offset between the UFT modules is that carrier insertion is minimized in the harmonic images of the harmonically rich signal 7934. As discussed above, carrier insertion is substantially wasted energy because the information for a modulated signal is carried in the sidebands of the modulated signal and not in the carrier. Therefore, it is often desirable to minimize the energy at the carrier frequency by controlling the relative DC offset.

7.3.1.4 Balanced Modulator FET Configuration

As described above, the balanced modulators 7104 and 7901 utilize two balanced UFT modules to sample the input baseband signals to generate harmonically rich signals that contain the up-converted baseband information. More specifically, the UFT modules include controlled switches that sample the baseband signal in a balanced and differential fashion. FIGs. 71D and 79D illustrate embodiments of the controlled switch in the UFT module.

FIG. 71D illustrates an example embodiment of the modulator 7104 (FIG. 71B) where the controlled switches in the UFT modules are field effect transistors (FET). More specifically, the controlled switches 7148 and 7128 are embodied as FET 7158 and FET 7160, respectively. The FET 7158 and 7160 are oriented so that their gates are controlled by the control signals 7123 and 7127, so that the control signals control the FET conductance. For the FET 7158, the combined baseband signal 7120 is received at the source of the FET 7158 and is sampled according to the control signal 7123 to produce the harmonically rich signal 7130 at the drain of the FET 7158. Likewise, the combined baseband signal 7122 is received at the source of the FET 7160 and is sampled according to the control signal 7127 to produce the harmonically rich signal 7134 at the drain of FET 7160. The source and drain orientation that is illustrated is not limiting, as the source and drains can be switched for most FETs. In other words, the combined baseband signal can be received at the drain of the FETs, and the harmonically rich signals can be taken from the source of the FETs, as will be understood by those skilled in the relevant arts.

FIG. 79D illustrates an embodiment of the modulator 7900 (FIG. 79A) where the controlled switches in the UFT modules are field effect transistors (FET). More specifically, the controlled switches 7918 and 7924 are embodied as FET 7936 and FET 7938, respectively. The FETs 7936 and 7938 are oriented so that their gates are controlled by the control signals 7123 and 7127, respectively, so that the control signals determine FET conductance. For the FET 7936, the baseband signal 7906 is received at the source of the FET 7936 and shunted to ground according to the control signal 7123, to produce the harmonically rich signal 7914. Likewise, the baseband signal 7908 is received at the source of the FET 7938 and is shunted to grounding according to the control signal 7127, to produce the harmonically rich signal 7926. The source and drain orientation that is illustrated is not limiting, as the source and drains can be switched for most FETs, as will be understood by those skilled in the relevant arts.

7.3.1.5 Universal Transmitter Configured for Carrier Insertion

As discussed above, the transmitters 7102 and 7900 have a balanced configuration that substantially eliminates any DC offset and results in minimal carrier insertion in the output signal 7140. Minimal carrier insertion is generally desired for most applications because the carrier signal carries no information and reduces the overall transmitter efficiency. However, some applications require the received signal to have sufficient carrier energy for the receiver to extract the carrier for coherent demodulation. In support thereof, the present invention can be configured to provide the necessary carrier insertion by implementing a DC offset between the two sampling UFT modules.

FIG. 73A illustrates a transmitter 7302 that up-converts a baseband signal 7306 to an output signal 7322 having carrier insertion. As is shown, the transmitter 7302 is similar to the transmitter 7102 (FIG. 71A) with the exception that the up-converter/modulator 7304 is configured to accept two DC references voltages. In contrast, modulator 7104 was configured to accept only one DC reference voltage. More specifically, the modulator 7304 includes a terminal 7309 to accept a DC reference voltage 7308, and a terminal 7313 to accept a DC reference voltage 7314. Vr 7308 appears at the UFT module 7124 though summer amplifier 7118 and the inductor 7310. Vr 7314 appears at UFT module 7128 through the summer amplifier 7119 and the inductor 7316. Capacitors 7312 and 7318 operate as blocking capacitors. If Vr 7308 is different from Vr 7314 then a DC offset voltage will be exist between UFT module 7124 and UFT module 7128, which will be up-converted at the carrier frequency in the harmonically rich signal 7320. More specifically, each harmonic image in the harmonically rich signal 7320 will include a carrier signal as depicted in FIG. 73B.

FIG. 73B illustrates an exemplary frequency spectrum for the harmonically rich signal 7320 that has multiple harmonic images 7324a-n. In addition to carrying the baseband information in the sidebands, each harmonic image 7324 also includes a carrier signal 7326 that exists at respective harmonic of the sampling frequency $1/T_S$. The amplitude of the carrier signal increases with increasing DC offset voltage. Therefore, as the difference between Vr 7308 and Vr 7314 widens, the amplitude of each carrier signal 7326 increases. Likewise, as the difference between Vr 7308 and Vr 7314 shrinks, the amplitude of each carrier signal 7326 shrinks. As with transmitter 7302, the optional bandpass filter 7106 can be included to select a desired harmonic image for transmission. This is represented by passband 7328 in FIG. 73B.

7.3.2 Universal Transmitter In I Q Configuration:

As described above, the balanced modulators 7104 and 7901 up-convert a baseband signal to a harmonically rich signal having multiple harmonic images of the baseband information. By combining two balanced modulators, IQ configurations can be formed for up-converting I and Q baseband signals. In doing so, either the (series type) balanced modulator 7104 or the (shunt type) balanced modulator 7901 can be utilized. IQ modulators having both series and shunt configurations are described below.

7.3.2.1 IQ Transmitter Using Series-Type Balanced Modulator

FIG. 74 illustrates an IQ transmitter 7420 with an in-phase (I) and quadrature (Q) configuration according to embodiments of the invention. The transmitter 7420 includes an IQ balanced modulator 7410, an optional filter 7414, and an optional amplifier 7416. The transmitter 7420 is useful for transmitting complex I Q waveforms and does so in a balanced manner to control DC offset and carrier insertion. In doing so, the modulator 7410 receives an I baseband signal 7402 and a Q baseband signal 7404 and up-converts these signals to generate a combined harmonically rich signal 7412. The harmonically rich signal 7412 includes multiple harmonics images, where each image contains the baseband information in the I signal 7402 and the Q signal 7404. The optional bandpass filter 7414 may be included to select a harmonic of interest (or subset of harmonics) from the signal 7412 for transmission. The optional amplifier 7416 may be included to amplify the selected harmonic prior to transmission, to generate the IQ output signal 7418.

As stated above, the balanced IQ modulator 7410 up-converts the I baseband signal 7402 and the Q baseband signal 7404 in a balanced manner to generate the combined harmonically rich signal 7412 that carriers the I and Q baseband information. To do so, the modulator 7410 utilizes two balanced modulators 7104 from FIG. 71A, a signal combiner 7408, and a DC terminal 7407. The operation of the balanced modulator 7410 and other circuits in the transmitter is described according to the flowchart 8700 in FIG. 87, as follows.

In step 8702, the IQ modulator 7410 receives the I baseband signal 7402 and the Q baseband signal 7404.

In step 8704, the I balanced modulator 7104a samples the I baseband signal 7402 in a differential fashion using the control signals 7123 and 7127 to generate a harmonically rich signal 7411a. The harmonically rich signal 7411a contains multiple harmonic images of the I baseband information, similar to the harmonically rich signal 7130 in FIG. 71B.

In step 8706, the balanced modulator 7104b samples the Q baseband signal 7404 in a differential fashion using control signals 7123 and 7127 to generate harmonically rich signal 7411b, where the harmonically rich signal 7411b contains multiple harmonic images of the Q baseband signal 7404. The operation of the balanced modulator 7104 and the generation of harmonically rich signals was fully described above and illustrated in FIGs. 71A-C, to which the reader is referred for further details.

In step 8708, the DC terminal 7407 receives a DC voltage 7406 that is distributed to both modulators 7104a and 7104b. The DC voltage 7406 is distributed to both the input and output of both UFT modules 7124 and 7128 in each modulator 7104. This minimizes (or prevents) DC offset voltages from developing between the four UFT modules, and thereby minimizes or prevents any carrier insertion during the sampling steps 8704 and 8706.

In step 8710, the 90 degree signal combiner 7408 combines the harmonically rich signals 7411a and 7411b to generate IQ harmonically rich signal 7412. This is further illustrated in FIGs. 75A-C. FIG. 75A depicts an exemplary frequency spectrum for the harmonically rich signal 7411a having harmonic images 7502a-n. The images 7502 repeat at harmonics of the sampling frequency $1/T_S$, where each image 7502 contains the necessary amplitude and frequency information to reconstruct the I baseband signal 7402. Likewise, FIG. 75B depicts an exemplary frequency spectrum for the harmonically rich signal 7411b having harmonic images 7504a-n. The harmonic images 7504a-n also repeat at harmonics of the sampling frequency $1/T_S$, where each image 7504 contains the necessary amplitude, frequency, and phase information to reconstruct the Q baseband signal 7404. FIG.75C illustrates an exemplary frequency spectrum for the combined harmonically rich signal 7412 having images 7506. Each image 7506 carries the I baseband information and the Q baseband information from the corresponding images 7502 and 7504, respectively, without substantially increasing the frequency bandwidth occupied by each harmonic 7506. This can occur because the signal combiner 7408 phase shifts the Q signal 7411b by 90 degrees relative to the I signal 7411a. The result is that the images 7502a-n and 7504a-n effectively share the signal bandwidth do to their orthogonal relationship. For example, the images 7502a and 7504a effectively share the frequency spectrum that is represented by the image 7506a.

In step 8712, the optional filter 7414 can be included to select a harmonic of interest, as represented by the passband 7508 selecting the image 7506c in FIG. 75c.

In step 8714, the optional amplifier 7416 can be included to amplify the harmonic (or harmonics) of interest prior to transmission.

In step 8716, the selected harmonic (or harmonics) is transmitted over a communications medium.

FIG. 76A illustrates a transmitter 7608 that is a second embodiment for an I Q transmitter having a balanced configuration. Transmitter 7608 is similar to the transmitter 7420 except that the 90 degree phase shift between the I and Q channels is achieved by phase shifting the control signals instead of using a 90 degree signal combiner to combine the harmonically rich signals. More specifically, delays 7604a and 7604b delay the control signals 7123 and 7127 for the Q channel modulator 7104b by 90 degrees relative the control signals for the I channel modulator 7104a. As a result, the Q modulator 7104b samples the Q baseband signal 7404 with 90 degree delay relative to the sampling of the I baseband signal 7402 by the I channel modulator 7104a. Therefore, the Q harmonically rich signal 7411b is phase shifted by 90 degrees relative to the I harmonically rich signal.

Since the phase shift is achieved using the control signals, an in-phase signal combiner 7606 combines the harmonically rich signals 7411a and 7411b, to generate the harmonically rich signal 7412.

FIG. 76B illustrates a transmitter 7618 that is similar to transmitter 7608 in FIG. 76A. The difference being that the transmitter 7618 has a modulator 7620 that utilizes a summing node 7622 to sum the signals 7411a and 7411b instead of the in-phase signal combiner 7606 that is used in modulator 7602 of transmitter 7608.

FIG. 90A-90D illustrate various detailed circuit implementations of the transmitter 7420 in FIG. 74. These circuit implementations are meant for example purposes only, and are not meant to be limiting.

FIG. 90A illustrates I input circuitry 9002a and Q input circuitry 9002b that receive the I and Q input signals 7402 and 7404, respectively.

FIG. 90B illustrates the I channel circuitry 9006 that processes an I data 9004a from the I input circuit 9002a.

FIG. 90C illustrates the Q channel circuitry 9008 that processes the Q data 9004b from the Q input circuit 9002b.

FIG. 90D illustrates the output combiner circuit 9012 that combines the I channel data 9007 and the Q channel data 9010 to generate the output signal 7418.

7.3.2.2 IQ Transmitter Using Shunt-Type Balanced Modulator

FIG. 80 illustrates an IQ transmitter 8000 that is another IQ transmitter embodiment according to the present invention. The transmitter 8000 includes an IQ balanced modulator 8001, an optional filter 8012, and an optional amplifier 8014. During operation, the modulator 8001 up-converts an I baseband signal 8002 and a Q baseband signal 8004 to generate a combined harmonically rich signal 8011. The harmonically rich signal 8011 includes multiple harmonics images, where each image contains the baseband information in the I signal 8002 and the Q signal 8004. The optional bandpass filter 8012 may be included to select a harmonic of interest (or subset of harmonics) from the harmonically rich signal 8011 for transmission. The optional amplifier 8014 may be included to amplify the selected harmonic prior to transmission, to generate the IQ output signal 8016.

The IQ modulator 8001 includes two shunt balanced modulators 7901 from FIG. 79A, and a 90 degree signal combiner 8010 as shown. The operation of the IQ modulator 8001 is described in reference to the flowchart 8800 (FIG. 88), as follows. The order of the steps in flowchart 8800 is not limiting.

In step 8802, the balanced modulator 8001 receives the I baseband signal 8002 and the Q baseband signal 8004.

In step 8804, the balanced modulator 7901a differentially shunts the I baseband signal 8002 to ground according the control signals 7123 and 7127, to generate a harmonically rich signal 8006. More specifically, the UFT modules 7916a and 7922a alternately shunt the I baseband signal 8002 and an inverted version of the I baseband signal 8002 to ground according to the control signals 7123 and 7127, respectively. The operation of the balanced modulator 7901 and the generation of harmonically rich signals was fully described above and is illustrated in FIGs. 79A-C, to which the reader is referred for further details. As such, the harmonically rich signal 8006 contains multiple harmonic images of the I baseband information as described above.

In step 8806, the balanced modulator 7901b differentially shunts the Q baseband signal 8004 to ground according to control signals 7123 and 7127, to generate harmonically rich signal 8008. More specifically, the UFT modules 7916b and 7922b alternately shunt the Q baseband signal 8004 and an inverted version of the Q baseband signal 8004 to ground, according to the control signals 7123 and 7127, respectively. As such, the harmonically rich signal 8008 contains multiple harmonic images that contain the Q baseband information.

In step 8808, the 90 degree signal combiner 8010 combines the harmonically rich signals 8006 and 8008 to generate IQ harmonically rich signal 8011. This is further illustrated in FIGs. 81A-C. FIG. 81A depicts an exemplary frequency spectrum for the harmonically rich signal 8006 having harmonic images 8102a-n. The harmonic images 8102 repeat at harmonics of the sampling frequency $1/T_S$, where each image 8102 contains the necessary amplitude, frequency, and phase information to reconstruct the I baseband signal 8002. Likewise, FIG. 81B depicts an exemplary frequency spectrum for the harmonically rich signal 8008 having harmonic images 8104a-n. The harmonic images 8104a-n also repeat at harmonics of the sampling frequency $1/T_S$, where each image 8104 contains the necessary amplitude, frequency, and phase information to reconstruct the Q baseband signal 8004. FIG.81C illustrates an exemplary frequency spectrum for the IQ harmonically rich signal 8011 having images 8106a-n. Each image 8106 carries the I baseband information and the Q baseband information from the corresponding images 8102 and 8104, respectively, without substantially increasing the frequency bandwidth occupied by each image 8106. This can occur because the signal combiner 8010 phase shifts the Q signal 8008 by 90 degrees relative to the I signal 8006.

In step 8810, the optional filter 8012 may be included to select a harmonic of interest, as represented by the passband 8108 selecting the image 8106c in FIG. 81C.

In step 8812, the optional amplifier 8014 can be included to amplify the selected harmonic image 8106 prior to transmission.

In step 8814, the selected harmonic (or harmonics) is transmitted over a communications medium.

FIG. 82 illustrates a transmitter 8200 that is another embodiment for an IQ transmitter having a balanced configuration. Transmitter 8200 is similar to the transmitter 8000 except that the 90 degree phase shift between the I and Q channels is achieved by phase shifting the control signals instead of using a 90 degree signal combiner to combine the harmonically rich signals. More specifically, delays 8204a and 8204b delay the control signals 7123 and 7127 for the Q channel modulator 7901b by 90 degrees relative the control signals for the I channel modulator 7901a. As a result, the Q modulator 7901b samples the Q baseband signal 8004 with a 90 degree delay relative to the sampling of the I baseband signal 8002 by the I channel modulator 7901a. Therefore, the Q harmonically rich signal 8008 is phase shifted by 90 degrees relative to the I harmonically rich signal 8006. Since the phase shift is achieved using the control signals, an in-phase signal combiner 8206 combines the harmonically rich signals 8006 and 8008, to generate the harmonically rich signal 8011.

FIG.83 illustrates a transmitter 8300 that is similar to transmitter 8200 in FIG. 82. The difference being that the transmitter 8300 has a balanced modulator 8302 that utilizes a summing node 8304 to sum the I harmonically rich signal 8006 and the Q harmonically rich signal 8008 instead of the in-phase signal combiner 8206 that is used in the modulator 8202 of transmitter 8200. The 90 degree phase shift between the I and Q channels is implemented by delaying the Q clock signals using 90 degree delays 8204, as shown.

7.3.2.3 IQ Transmitters Configured for Carrier Insertion

The transmitters 7420 (FIG. 74) and 7608 (FIG. 76A) have a balanced configuration that substantially eliminates any DC offset and results in minimal carrier insertion in the IQ output signal 7418. Minimal carrier insertion is generally desired for most applications because the carrier signal carries no information and reduces the overall transmitter efficiency. However, some applications require the received signal to have sufficient carrier energy for the receiver to extract the carrier for coherent demodulation. In support thereof, FIG. 77 illustrates a transmitter 7702 to provide any necessary carrier insertion by implementing a DC offset between the two sets of sampling UFT modules.

Transmitter 7702 is similar to the transmitter 7420 with the exception that a modulator 7704 in transmitter 7702 is configured to accept two DC reference voltages so that the I channel modulator 7104a can be biased separately from the Q channel modulator 7104b. More specifically, modulator 7704 includes a terminal 7706 to accept a DC voltage reference 7707, and a terminal 7708 to accept a DC voltage reference 7709. Voltage 7707 biases the UFT modules 7124a and 7128a in the I channel modulator 7104a. Likewise, voltage 7709 biases the UFT modules 7124b and 7128b in the Q channel modulator 7104b. When voltage 7707 is different from voltage 7709, then a DC offset will appear between the I channel modulator 7104a and the Q channel modulator 7104b, which results in carrier insertion in the IQ harmonically rich signal 7412. The relative amplitude of the carrier frequency energy increases in proportion to the amount of DC offset.

FIG. 78 illustrates a transmitter 7802 that is a second embodiment of an IQ transmitter having two DC terminals to cause DC offset, and therefore carrier insertion. Transmitter 7802 is similar to transmitter 7702 except that the 90 degree phase shift between the I and Q channels is achieved by phase shifting the control signals, similar to that done in transmitter 7608. More specifically, delays 7804a and 7804b phase shift the control signals 7123 and 7127 for the Q channel modulator 7104b relative to those of the I channel modulator 7104a. As a result, the Q modulator 7104b samples the Q baseband signal 7404 with 90 degree delay relative to the sampling of the I baseband signal 7402 by the I channel modulator 7104a. Therefore, the Q harmonically rich signal 7411b is phase shifted by 90 degrees relative to the I harmonically rich signal 7411a, which are combined by the in-phase combiner 7806.

7.4 Transceiver Embodiments

Referring to FIG. 39, in embodiments the receiver 3906, transmitter 3910, and LNA/PA 3904 are configured as a transceiver, such as but not limited to transceiver 9100, that is shown in FIG. 91.

Referring to FIG. 91, the transceiver 9100 includes a diplexer 9108, the IQ receiver 7000, and the IQ transmitter 8000. Transceiver 9100 up-converts an I baseband signal 9114 and a Q baseband signal 9116 using the IQ transmitter 8000 (FIG. 80) to generate an IQ RF output signal 9106. A detailed description of the IQ transmitter 8000 is included for example in section 7.3.2.2, to which the reader is referred for further details. Additionally, the transceiver 9100 also down-converts a received RF signal 9104 using the IQ Receiver 7000, resulting in I baseband output signal 9110 and a Q baseband output signal 9112. A detailed description of the IQ receiver 7000 is included in section 7.2.2, to which the reader is referred for further details.

7.5 Demodulator/Modulator Facilitation Module

An example demodulator/modulator facilitation module 3912 is shown in FIGS. 47 and 48. A corresponding BOM list is shown in FIGS. 49A and 49B.

An alternate example demodulator/modulator facilitation module 3912 is shown in FIGS. 50 and 51. A corresponding BOM list is shown in FIGS. 52A and 52B.

FIG. 52C illustrates an exemplary demodulator/modulator facilitation module 5201. Facilitation module 5201 includes the following: de-spread module 5204, spread module 5206, de-modulator 5210, and modulator 5212.

For receive, the de-spread module 5204 de-spreads received spread signals 3926 and 3928 using a spreading code 5202. Separate spreading codes can be used for the I and Q channels as will be understood by those skilled in the arts. The demodulator 5210 uses a signal 5208 to demodulate the de-spread received signals from the de-spread module 5204, to generate the I baseband signal 3930a and the Q baseband signal 3932a.

For transmit, the modulator 5212 modulates the I baseband signal 3930b and the Q baseband signal 3932b using a modulation signal 5208. The resulting modulated signals are then spread by the spread module 5206, to generate I spread signal 3942 and Q spread signal 3944.

In embodiments, the modulation scheme that is utilized is differential binary phase shift keying (DBPSK) or differential quadrature phase shift keying (DQPSK), and is compliant with the various versions of IEEE 802.11. Other modulation schemes could be utilized besides DBPSK or DQPSK, as will understood by those skilled in arts based on the discussion herein.

In embodiments, the spreading code 5202 is a Barker spreading code, and is compliant with the various versions of IEEE 802.11. More specifically, in embodiments, an 11-bit Barker word is utilized for spreading/de-spreading. Other spreading codes could be utilized as will be understood by those skilled in the arts based on the discussion herein.

7.6 MAC Interface

An example MAC interface 3914 is shown in FIG. 45. A corresponding BOM list is shown in FIGS. 46A and 46B.

In embodiments, the MAC 3918 and MAC interface 3914 supply the functionality required to provide a reliable delivery mechanism for user data over noisy, and unreliable wireless media. This is done this while also providing advanced LAN services, equal to or beyond those of existing wired LANs.

The first functionality of the MAC is to provide a reliable data delivery service to users of the MAC. Through a frame exchange protocol at the MAC level, the MAC significantly improves on the reliability of data delivery services over wireless media, as compared to earlier WLANs. More specifically, the MAC implements a frame exchange protocol to allow the source of a frame to determine when the frame has been successfully received at the destination. This frame exchange protocol adds some overhead beyond that of other MAC protocols, like IEEE 802.3, because it is not sufficient to simply transmit a frame and expect that the destination has received it correctly on the wireless media. In addition, it cannot be expected that every station in the WLAN is able to communicate with every other station in the WLAN. If the source does not receive this acknowledgment, then the source will attempt to transmit the frame again. This retransmission of frame by the source effectively reduces the effective error rate of the medium at the cost of additional bandwidth consumption.

The minimal MAC frame exchange protocol consists of two frames, a frame sent from the source to the destination and an acknowledgment from the destination that the frame was received correctly. The frame and its acknowledgment are an atomic unit of the MAC protocol. As such, they cannot be interrupted by the transmission from any other station. Additionally, a second set of frames may be added to the minimal MAC frame exchange. The two added frames are a request to send frame and a clear to send frame. The source sends a request to send to the destination. The destination returns a clear to send to the source. Each of these frames contains information that allows other stations receiving them to be notified of the upcoming frame transmission, and therefore to delay any transmission their own. The request to send and clear frames serve to announce to all stations in the neighborhood of both the source and the destination about the pending transmission from the source to the destination. When the source receives the clear to send from the destination, the real frame that the source wants delivered to the destination is sent. If the frame is correctly received at the destination, then the destination will return an acknowledgment. completing the frame exchange protocol. While this four way frame exchange protocol is a required function of the MAC, it may be disabled by an attribute in the management information base.

The second functionality of the MAC is to fairly control access to the shared wireless medium. It performs this function through two different access mechanisms: the basic access mechanism, call the distribution coordination system function, and a centrally controlled access mechanism, called the point coordination function.

The basic access mechanism is a carrier sense multiple access with collision avoidance (CSMA/CA) with binary exponential backoff.. This access mechanism is similar to that used for IEEE 802.3, with some variations. CSMA/CA is a "listen before talk" (LBT) access mechanism. In this type of access mechanism, a station will listen to the medium before beginning a transmission. If the medium is already carrying a transmission, then the station that listening will not begin its own transmission. More specifically , if a listening station detects an existing transmission in progress, the listening station enters a transmit deferral period determined by the binary exponential backoff algorithm. The binary exponential backoff mechanism chooses a random number which represents the amount of time that must elapse while there are not any transmission. In other words, the medium is idle before the listening station may attempt to begin its transmission again. The MAC may also implement a network allocation vector (NAV). The NAV is the value that indicates to a station that amount of time that remains before a medium becomes available. The NAV is kept current through duration values that are transmitted in all frames. By examining the NAV, a station may avoid transmitting, even when the medium does not appear to be carrying a transmission in the physical sense.

The centrally controlled access mechanism uses a poll and response protocol to eliminate the possibility of contention for the medium. This access mechanism is called the point coordination function (PCF). A point coordinator (PC) controls the PCF. The PC is always located in an AP. Generally, the PCF operates by stations requesting that the PC register them on a polling list, and the PC then regularly polls the stations for traffic while also delivering traffic to the stations. With proper planning, the PCF is able to deliver near isochronous service to the stations on the polling list.

The third function of the MAC is to protect the data that it delivers. Because it is difficult to contain wireless WLAN signals to a particular physical area, the MAC provides a privacy service, called Wired Equivalent Privacy (WEP), which encrypts the data sent over the wireless medium. The level of encryption chosen approximates the level of protection data might have on a wireless LAN in a building with controlled access that prevents physically connecting to the LAN without authorization.

7.7 Control Signal Generator - Synthesizer

In an embodiment, the control signal generator 3908 is preferably implemented using a synthesizer. An example synthesizer is shown in FIG. 55. A corresponding BOM list is shown in FIGS. 56A and 56B.

7.8 LNA/PA

An example LNA/PA 3904 is shown in FIGS. 64 and 65. A corresponding BOM list is shown in FIG. 66.

Additionally, FIG. 93 illustrates a LNA/PA module 9301 that is another embodiment of the LNA/PA 3904. LNA/PA module 9301 includes a switch 9302, a LNA 9304, and a PA 9306. The switch 9302 connects either the LNA 9304 or the PA 9306 to the antenna 3903, as shown. The switch 9302 can be controlled by an on -board processor that is not shown.

8.0 802.11 Physical Layer Configurations

The 802.11 WLAN standard specifies two RF physical layers: frequency hopped spread spectrum (FHSS) and direct sequence spread spectrum (DSSS). The invention is not limited to these specific examples. Both DSSS and FHSS support 1 Mbps and 2 Mbps data rates and operate in the 2.400-2.835 GHz band for wireless communications in accordance to FCC part 15 and ESTI-300 rules. Additionally, 802.11 has added an 11 Mbps standard that operates at 5 GHz and utilizes OFDM modulation.

The DSSS configuration supports the 1 MBPS data rate utilizing differential binary phase shift keying (DBPSK) modulation, and supports 2 MBPS utilizing differential quadrature phase shift keying modulation. In embodiments, an 11-bit Barker word is used as the spreading sequence that is utilized by the stations in the 802.11 network. A Barker word has a relatively short sequence, and is known to have very good correlation properties, and includes the following sequence: +1, -1, +1, +1, -1, +1, +1, +1, -1, -1, -1. The Barker word used for 802.11 is not to be confused with the spreading codes used for code division multiple access (CDMA) and global positioning system (GPS). CDMA and GPS use orthogonal spreading codes, which allow multiple users to operate on the same channel frequency. Generally, CDMA codes have longer sequences and have richer correlation properties.

During transmission, the 11-bit barker word is exclusive-ored (EX-OR) with each of the information bits using a modulo-2 adder, as illustrated by modulo-2 adder 9202 in FIG. 92 . Referring to FIG. 92, the11-bit (at 11 MBPS) Barker word is applied to a modulo-2 adder together with each one (at 1 MBPS) of the information bits (in the PPDU data). The Ex-OR function combines both signals by performing a modulo-2 addition of each information bit with each Barker bit (or chip). The output of the modulo-2 adder results in a signal with a data rate that is 10x higher than the information rate. The result in the frequency domain signal is a signal that is spread over a wider bandwidth at a reduced RF power level. At the receiver, the DSSS signal is convolved with an 11-bit Barker word and correlated. As shown in FIG. 92, the correlation recovers the information bits at the transmitted information rate, and the undesired interfering in-band signals are spread out-of-band. The spreading and despreading of narrowband to wideband signal is commonly referred to as processing gain and is measured in decibels (dB). Processing gain is the ratio of DSSS signal rate information rate. In embodiments, the minimum requirement for processing gain is 10 dB.

The second RF physical layer that is specified by the IEEE 802.11 standard is frequency hopping spread spectrum (FHSS). A set of hop sequences is defined in IEEE 802.11 for use in the 2.4 GHz frequency band. The channels are evenly spaced across the band over a span of 83.5 MHz. During the development of IEEE 802.11, the hop sequences listed in the standard were pre-approved for operation in North America, Europe, and Japan. In North America and Europe (excluding Spain and France), the required number of hop channels is 79. The number of hopped channels for Spain and France is 23 and 35, respectively. In Japan, the required number of hopped channels is 23. The hopped center channels are spaced uniformly across the 2.4 GHz frequency band occupying a bandwidth of 1MHz. In North America and Europe (excluding Spain and France), the hopped channels operate from 2.402 GHz to 2.480 GHz. In Japan, the hopped channels operate from 2.447 GHz to 2.473 GHz. The modulation scheme called out for FHSS by 802.11 is 2-level Gaussian Phase Shift Keying (GFSK) for the 1 MBps data rate, and 4-level GFSK for the 2 MBps data rate.

In addition to DSSS and FHSS RF layer standards, the IEEE 802.11 Executive Committee approved two projects for higher rate physical layer extensions. The first extension, IEEE 802.11a defines requirements for a physical layer operating in the 5.0 GHz frequency band, and data rates ranging from 6 MBps to 54 MBps. This 802.11a draft standard is based on Orthogonal Frequency Division Multiplexing (OFDM) and uses 48 carriers as a phase reference (so coherent), with 20 MHZ spacing between the channels. The second extension, IEEE 802.11b, defines a set of physical layer specifications operating in the 2.4 GHz ISM frequency band. This 802.11b utilizes complementary code keying (CCK), and extends the data rate up to 5.5 Mbps and 11 Mbps.

The transmitter and receiver circuits described herein can be operated in all of the WLAN physical layer embodiments described herein, including the DSSS and FHSS embodiments described herein. However, the present invention is not limited to being operated in WLAN physical layer embodiments that were described herein, as the invention could be configured in other physical layer embodiments.

Figure 94 illustrates a block diagram of an IEEE 802.11 DSSS radio transceiver 9400 using UFT Zero IF technology. DSSS transceiver 9400 includes: antenna 9402, switch 9404, amplifiers 9406 and 9408, transceivers 9410, baseband processor 9412, MAC 9414, bus interface unit 9416, and PCMCIA connector 9418. The DSSS transceiver 9400 includes an IQ receiver 7000 and an IQ transmitter 8000, which are described herein. UFT technology interfaces directly to the baseband processor 9412 of the physical layer. In the receive path, the IQ receiver 7000 transforms a 2.4GHz RF signal-of-interest into I/Q analog baseband signals in a single step and passes the signals to the baseband processor 9412, where the baseband processor is then responsible for de-spreading and demodulating the signal. In embodiments, the IQ receiver 7000 includes all of the circuitry necessary for accommodating AGC, baseband filtering and baseband amplification. In the transmit path, the transmitter 8000 transforms the I/Q analog baseband signals to a 2.4GHz RF carrier directly in a single step. The signal conversion clock is derived from a single synthesized local oscillator (LO) 9420. The selection of the clock frequency is determined by choosing a sub-harmonic of the carrier frequency. For example, a 5th harmonic of 490 MHZ was used, which corresponds to a RF channel frequency of 2.450GHz. Using UFT technology simplifies the requirements and complexity of the synthesizer design.

9. Appendix

The attached Appendix contained in FIGS. 95A-C, 96-161, which forms part of this patent application, includes schematics of an integrated circuit (IC) implementation example of the present invention. This example embodiment is provided solely for illustrative purposes , and is not limiting. Other embodiments will be apparent to persons skilled in the relevant art(s) based on the teachings herein. FIG. 95A illustrates a schematic for a WLAN modulator/demodulator IC according to embodiments of the invention. FIGs. 95B and 95C illustrate an expanded view of the circuit in FIG. 95A. FIGs. 96-161 further illustrate detailed circuit schematics of the WLAN modulator/demodulator integrated circuit.

10. Conclusions

Example implementations of the systems and components of the invention have been described herein. As noted elsewhere, these example implementations have been described for illustrative purposes only, and are not limiting. Other implementation embodiments are possible and covered by the invention, such as but not limited to software and software/hardware implementations of the systems and components of the invention. Such implementation embodiments will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

While various application embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

What Is Claimed Is:

1. A wireless modem apparatus, comprising:

a balanced transmitter for up-converting a baseband signal, including,

an inverter, to receive said baseband signal and generate an inverted baseband signal;

a first controlled switch, coupled to a non-inverting output of said inverter, said first controlled switch to sample said baseband signal according to a first control signal, resulting in a first harmonically rich signal;

a second controlled switch, coupled to an inverting output of said inverter, said second controlled switch to sample said inverted baseband signal according to a second control signal, resulting in a second harmonically rich signal; and

a combiner, coupled to an output of said first controlled switch and an output of said second controlled switch, said combiner to combine said first harmonically rich signal and said second harmonically rich signal, resulting in a third harmonically rich signal.

2. The apparatus of claim 1, wherein said second control signal is phase shifted with respect to said first control signal.

3. The apparatus of claim 1, wherein said second control signal is phase shifted by 180 degrees with respect to said first control signal.

4. The apparatus of claim 1, wherein said first control signal and said second control signal each comprise a plurality of pulses having an associated pulse width T_A that operates to improve energy transfer to a desired harmonic image in said harmonically rich signal.

5. The apparatus of claim 4, wherein said pulse width T_A is approximately ½ of a period of said desired harmonic.

6. The apparatus of claim 1, further comprising a filter attached to an output of said combiner, wherein said filter selects a desired harmonic from said third harmonically rich signal.

7. The apparatus of claim 1, further comprising:

a balanced receiver, coupled to said balanced modulator, said receiver including,

a first universal frequency down-conversion module to down-convert an input signal, wherein said first universal frequency down-conversion module down-converts said input signal according to a third control signal and outputs a first down-converted signal;

a second universal frequency down-conversion module to down-convert said input signal, wherein said second universal frequency down-conversion module down-converts said input signal according to a fourth control signal and outputs a second down-converted signal; and

a subtractor module that subtracts said second down-converted signal from said first down-converted signal and outputs a down-converted signal.

8. The apparatus of claim 7, wherein said fourth control signal is delayed relative to said third control signal by .5 + n cycles of said input signal, wherein n may be any integer greater than or equal to 1.

9. The apparatus of claim 7, wherein said first universal frequency down-conversion module under-samples said input signal according to said third control signal, and said second universal frequency down-conversion module under-samples said input signal according to said fourth control signal.

10. The apparatus of claim 7, wherein said third and said fourth control signals each comprise a train of pulses having pulse widths that are established to improve energy transfer from said input signal to said first and said second down-converted signals, respectively.

11. The apparatus of claim 10, wherein said train of pulses have a pulse width that is approximately a fraction of a period of said input signal.

12. The apparatus of claim 10, wherein said train of pulses have pulse width that is approximately multiple periods and a fraction of a period of said input signal.

13. The apparatus of claim 10, wherein said first and said second universal frequency down-conversion modules each comprise a switch and a storage element.

14. The apparatus of claim 13, wherein said storage element comprises a capacitor that reduces a DC offset voltage in said first down-converted signal and said second down-converted signal.

15. The apparatus of claim 7, wherein said subtractor module comprises a differential amplifier.

16. The apparatus of claim 7, further comprising an antenna coupled to said balanced transmitter and said balanced receiver.

17. The apparatus of claim 16, further comprising a switch, said switch connecting either said transmitter or said receiver to said antenna.

18. The apparatus of claim 7, further comprising a baseband processor coupled to said transmitter and said receiver.

19. The apparatus of claim 7, further comprising a media access controller (MAC) coupled to said transmitter and said receiver.

20. The apparatus of claim 19, wherein said MAC comprises a means for controlling accessing to a WLAN medium.

21. The apparatus of claim 20, wherein said means for controlling includes carrier sense multiple access with collision avoidance (CSMA/CA).

22. The apparatus of claim 7, further comprising a demodulator/modulator facilitation module coupled to said transmitter and receiver.

23. The apparatus of claim 22, wherein said demodulator/modulator facilitation module comprises a means for modulating said baseband signal using differential binary phase shift keying (DBPSK).

24. The apparatus of claim 22, wherein said demodulator/modulator facilitation module comprises a means for de-modulating said down-converted signal using differential binary phase shift keying (DBPSK).

25. The apparatus of claim 22, wherein said demodulator/modulator facilitation module comprises a means for spreading said baseband signal.

26. The apparatus of claim 25, wherein said means for spreading comprises a means for spreading said baseband signal using a Barker code.

27. The apparatus of claim 22, wherein said demodulator/modulator facilitation module comprises a means for de-spreading said down-converted signal.

28. The apparatus of claim 27, wherein said means for de-spreading comprises a means for de-spreading said down-converted signal using a Barker code.

29. The apparatus of claim 1, wherein said apparatus is an infrastructure device.

30. The apparatus of claim 1, wherein said apparatus is a client device.

31. The apparatus of claim 1, wherein said first controlled switch shunts said baseband signal to a reference potential according to said first control signal, and wherein said second controlled switch shunts said inverted baseband signal to said reference potential according to said second control signal.

32. A method of transmitting a baseband signal over a wireless LAN, comprising the steps of:

(1) spreading the baseband signal using a spreading code, resulting in a spread baseband signal; and

(2) differentially sampling the spread baseband signal according to a first control signal and a second control signal resulting in a plurality of harmonic images that are each representative of the baseband signal, wherein said first and second control signals have pulse widths that improve energy transfer to a desired harmonic image of said plurality of harmonics.

33. The method of claim 32, further comprising the step of:

(3) modulating the baseband signal using phase shift keying prior to step (1).

34. The method of claim 32, further comprising the steps of:

(3) determining availability of a WLAN medium; and

(4) transmitting said desired harmonic over said WLAN medium if said medium is available.

35. The method of claim 34, wherein step (3) comprises the step of determining availability of said WLAN medium using carrier sense multiple access (CSMA) protocol.

36. The method of claim 32, wherein said step (2) comprises the step of:

(a) converting said baseband signal into a differential baseband signal having a first differential baseband component and a second differential baseband component;

(b) sampling said first differential component according to said first control signal to generate a first harmonically rich signal, and sampling said second differential component according to said second control signal to generate a second harmonically rich signal, wherein said second control signal is phase shifted relative to said first control signal; and

(c) combining said first harmonically rich signal and said second harmonically rich signal to generate said harmonic images.

37. The method of claim 32, further comprising the step of:

(3) minimizing DC offset voltages between sampling modules during step (2), and thereby minimizing carrier insertion in said harmonic images.

38. The method of claim 32, wherein said pulse widths are approximately ½ of a period of said desired harmonic.

39. In a wireless LAN device, a method of down-converting a received RF signal, comprising the steps of:

down-converting said received RF signal according to a first control signal and a second control signal, resulting in a down-converted signal, wherein said second control signal is delayed relative to said first control signal by .5 + n cycles of said received RF signal, wherein n may be any integer greater than or equal to 1;

de-spreading said down-converted signal using a spreading code, resulting in a de-spread signal; and

de-modulating said de-spread signal, resulting in a de-modulated signal;

wherein said first and said second control signals each comprise a train of pulses having pulse widths that are established to improve energy transfer from said received RF signal to said down-converted signal.

40. The method of claim 39, wherein said pulse widths are approximately ½ of a period of said received RF signal.

Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations

Abstract

Frequency translation and applications of the same are described herein, including RF modem and wireless local area network (WLAN) applications. In embodiments, the WLAN invention includes an antenna, an LNA/PA module, a receiver, a transmitter, a control signal generator, a demodulation/modulation facilitation module, and a MAC interface. The WLAN receiver includes at least one universal frequency translation module that frequency down-converts a received EM signal. In embodiments, the UFT based receiver is configured in a multi-phase embodiment to reduce or eliminate re-radiation that is caused by DC offset. The WLAN transmitter includes at least one universal frequency translation module that frequency up-converts a baseband signal in preparation for transmission over the wireless LAN. In embodiments, the UFT based transmitter is configured in a differential and multi-phase embodiment to reduce carrier insertion and spectral growth.

A278-54.wpd

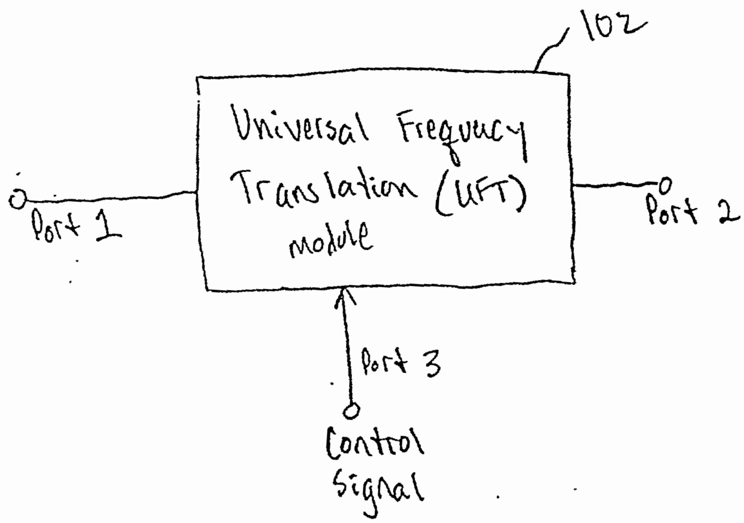

102
Universal Frequency Translation (UFT) module
Port 1
Port 2
Port 3
Control Signal

FIG. 1A

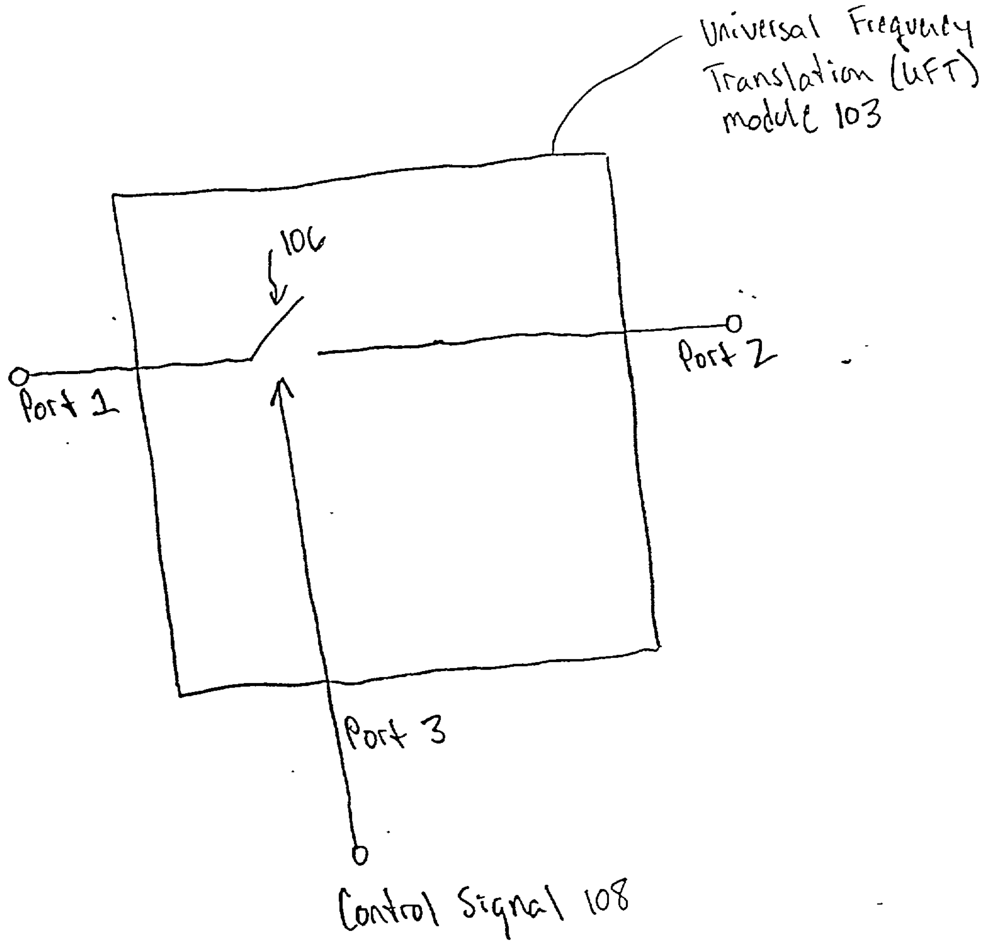

Universal Frequency Translation (UFT) module 103
106
Port 1
Port 2
Port 3
Control Signal 108

FIG. 1B

m

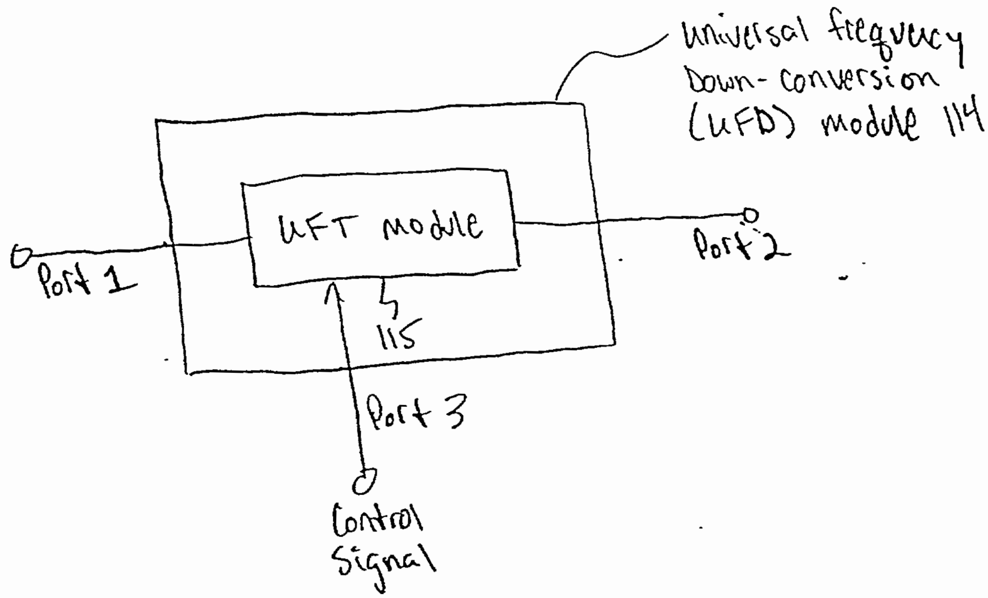

universal frequency
Down-conversion
(UFD) module 114
UFT module
Port 1
Port 2
115
Port 3
Control
Signal

FIG. 1C

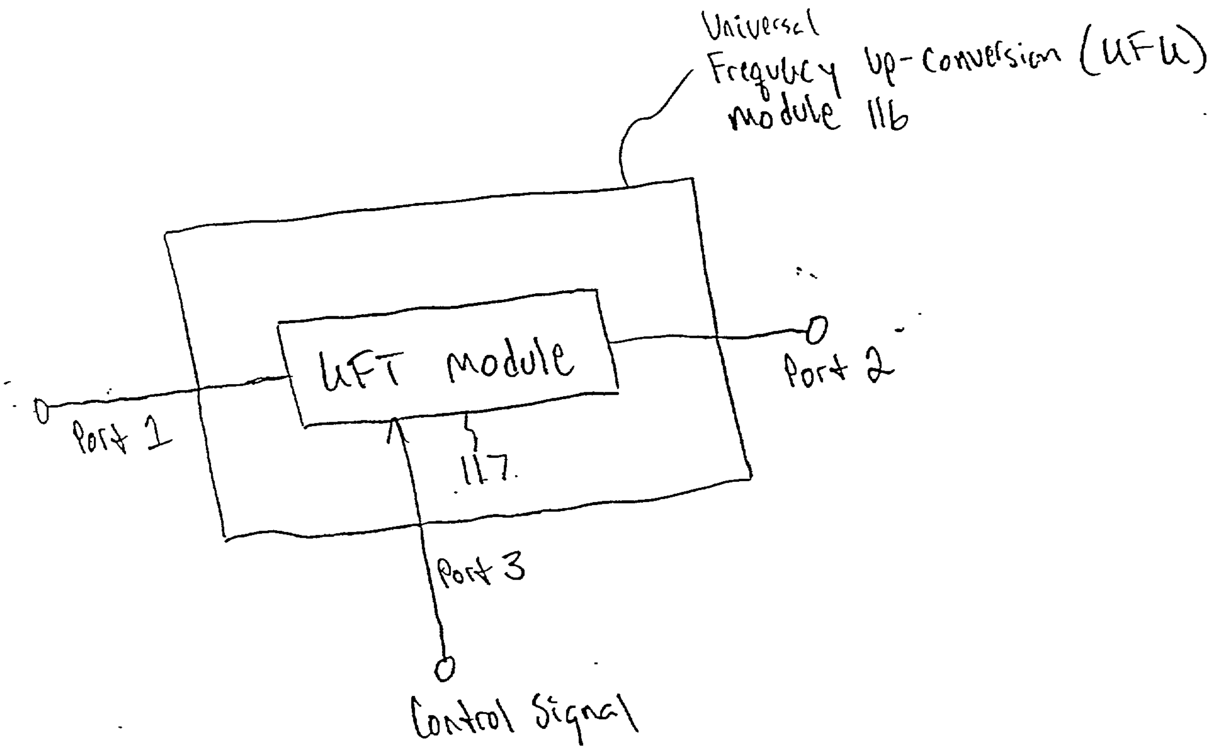

Universal
Frequency Up-Conversion (UFU)
module 116
UFT Module
Port 1
Port 2
117
Port 3
Control Signal

FIG. 1D

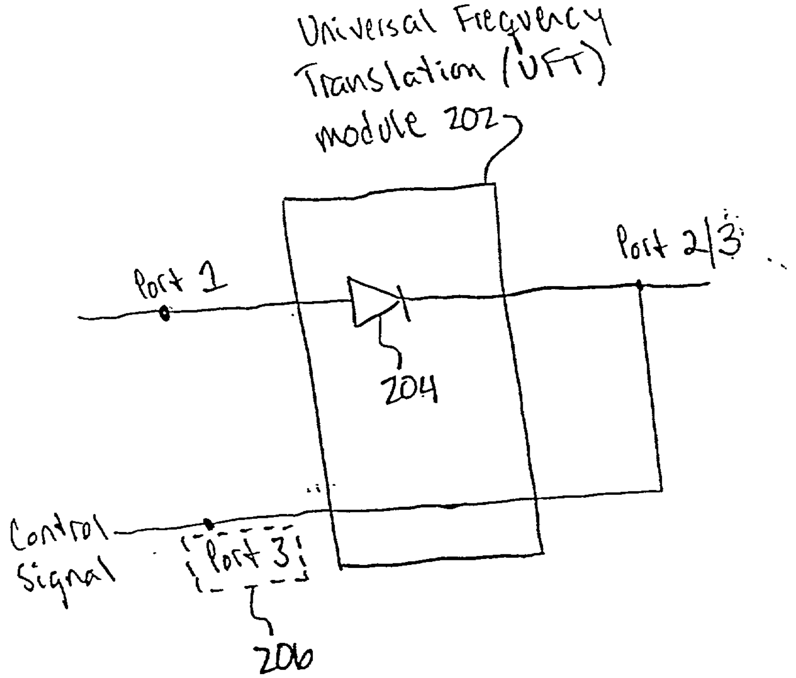

Universal Frequency
Translation (UFT)
module 202
Port 1
Port 2/3
204
Control
Signal
Port 3
206

FIG. 2A

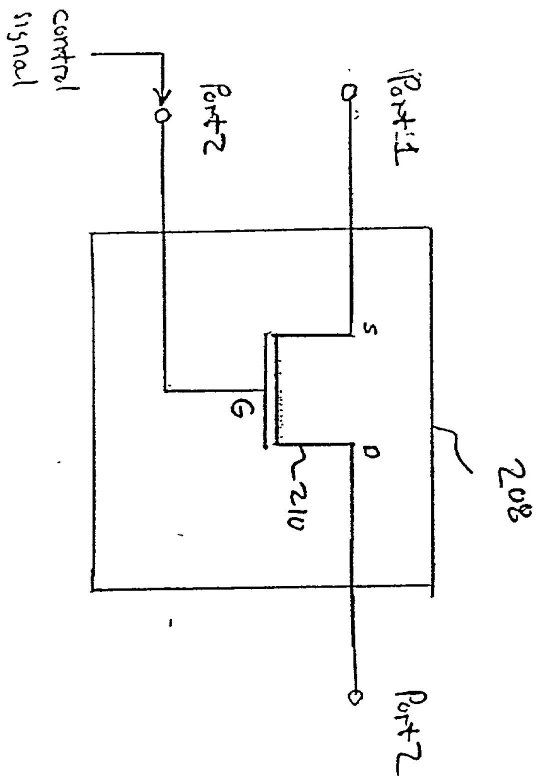


FIG. 2B

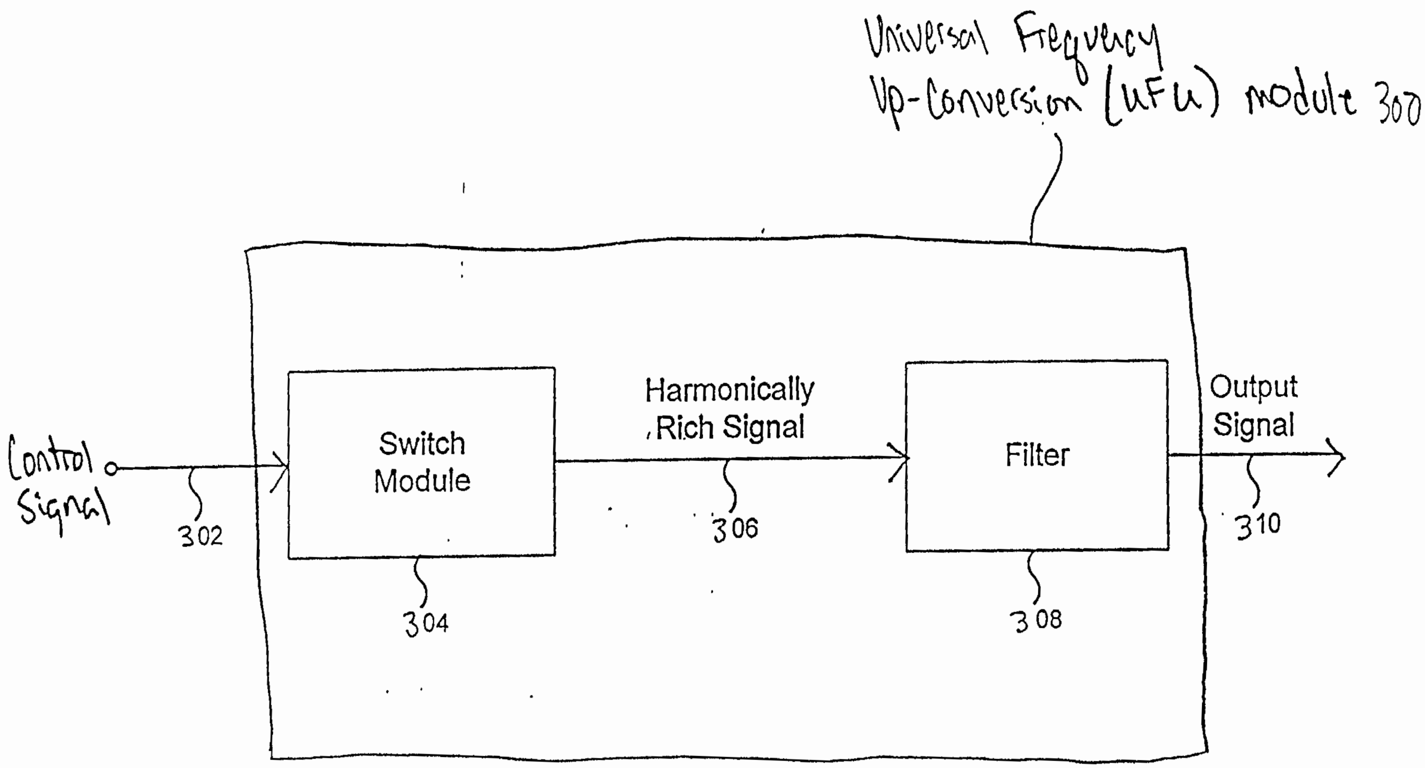

Universal Frequency Up-Conversion (UFU) module 300
Control Signal
302
Switch Module
304
Harmonically Rich Signal
306
Filter
308
Output Signal
310

FIG. 3

3

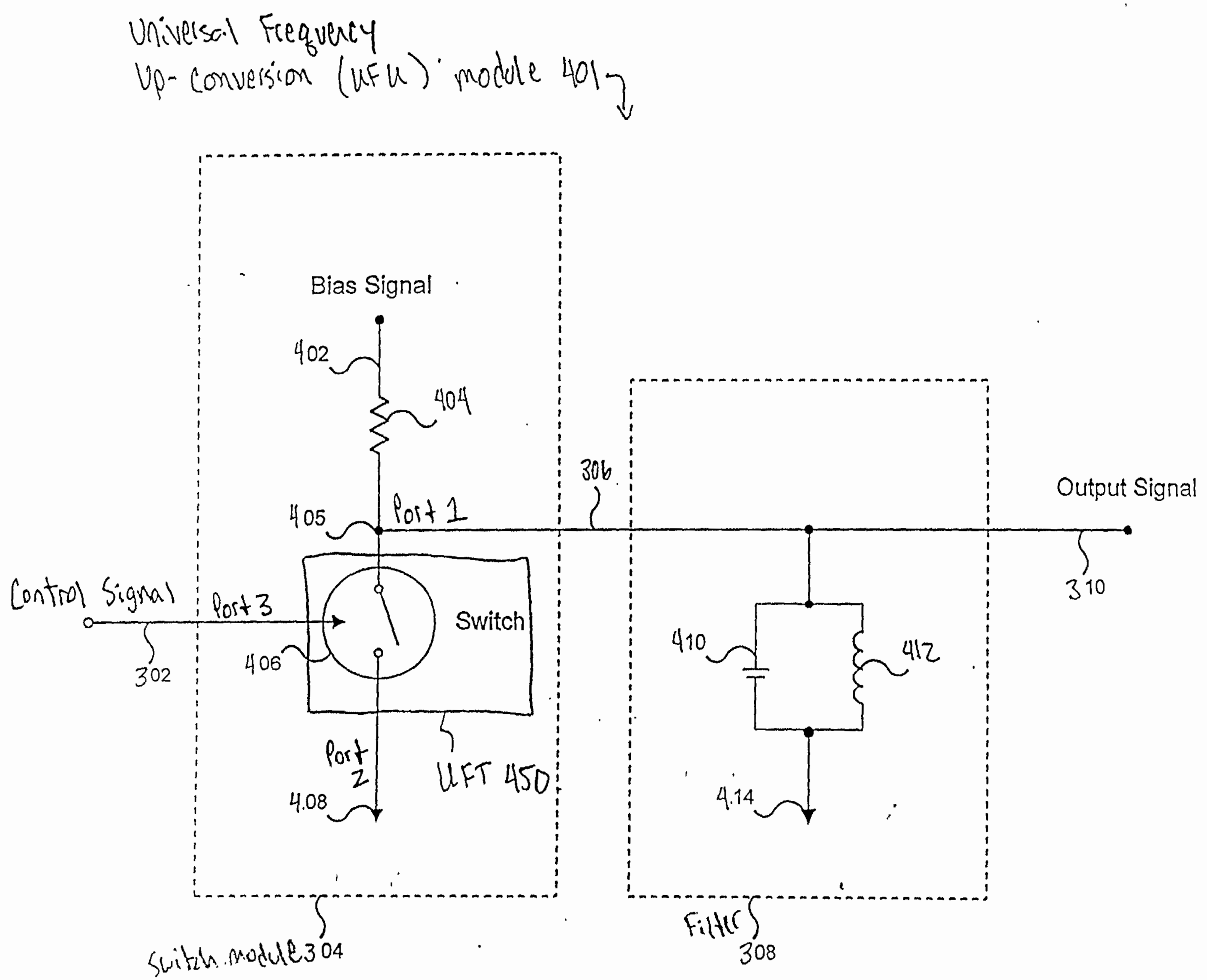


FIG. 4

09632856 .080400

9809.02.vsd/47

3

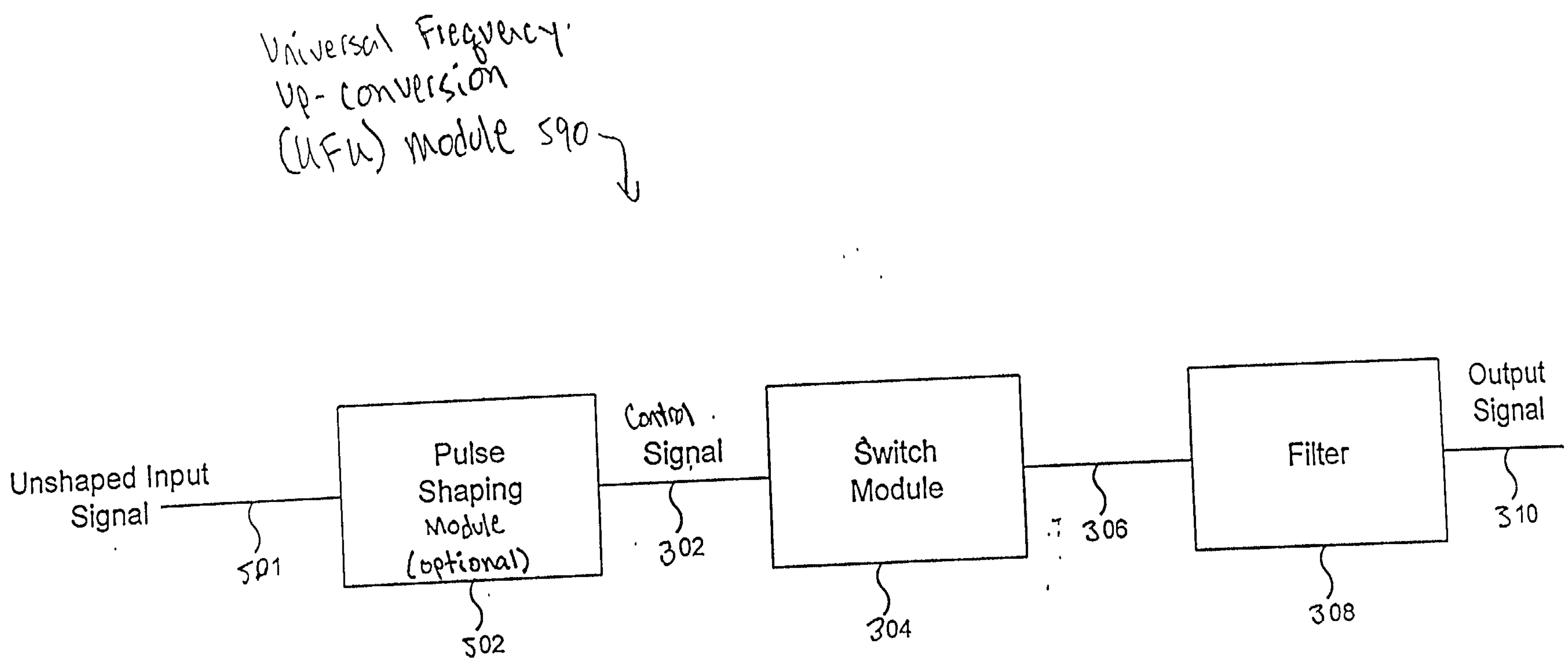


FIG. 5

09632856.080400

3609-02.vsd/48

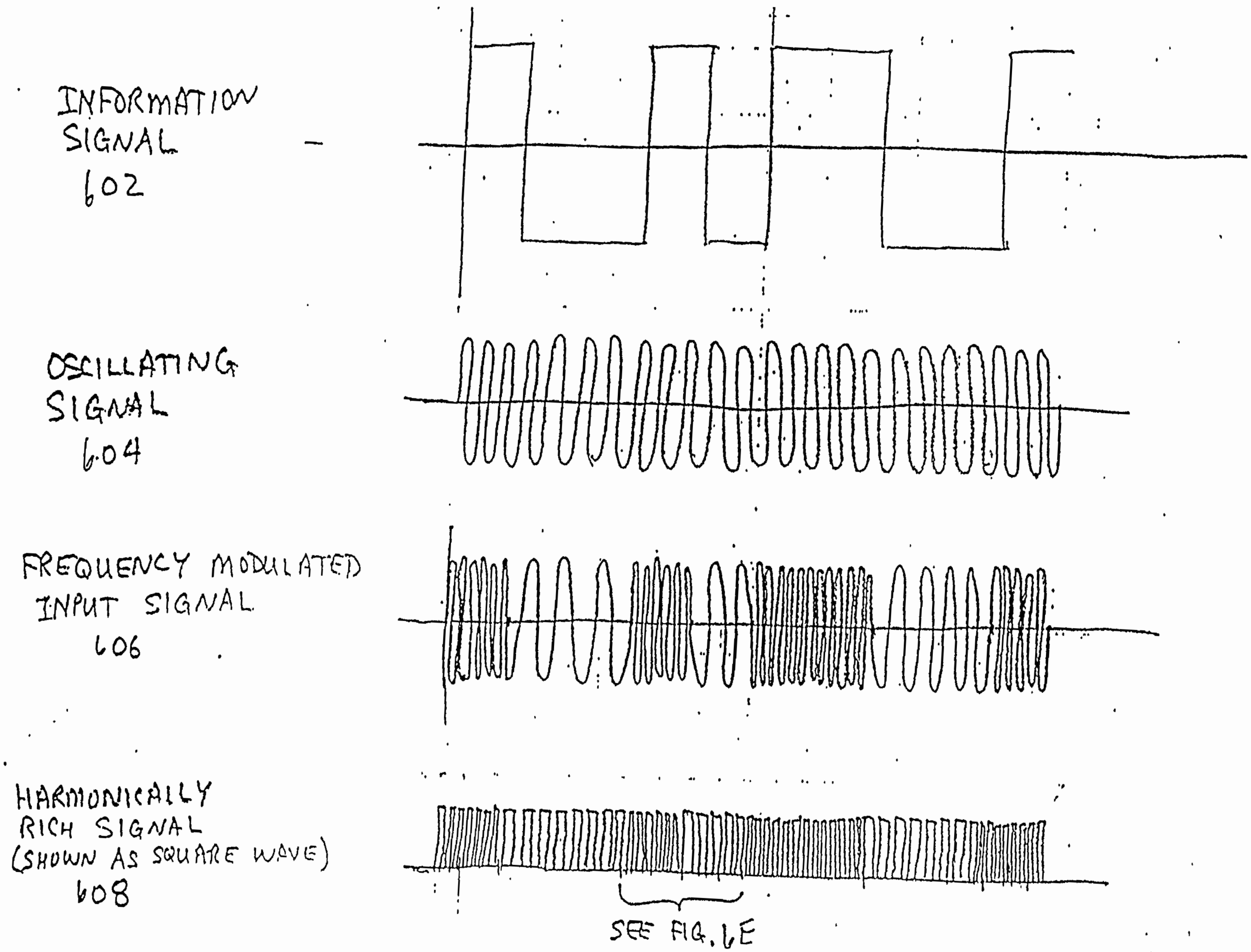


FIG. 6A

FIG. 6B

FIG. 6C

FIG. 6D

FIG. 6

EXPANDED VIEW OF HARMONICALLY RICH SIGNAL 608

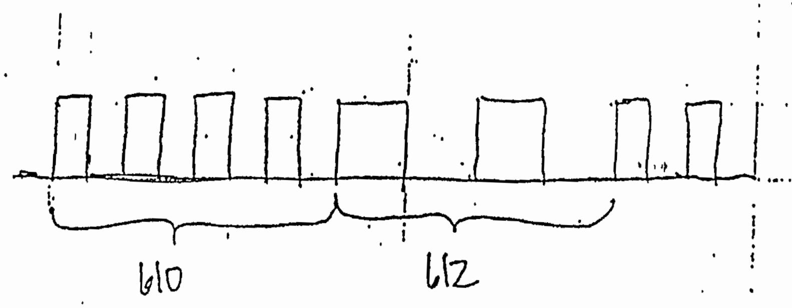


FIG 6E

HARMONICS OF SIGNAL 610 (SHOWN SEPARATELY)

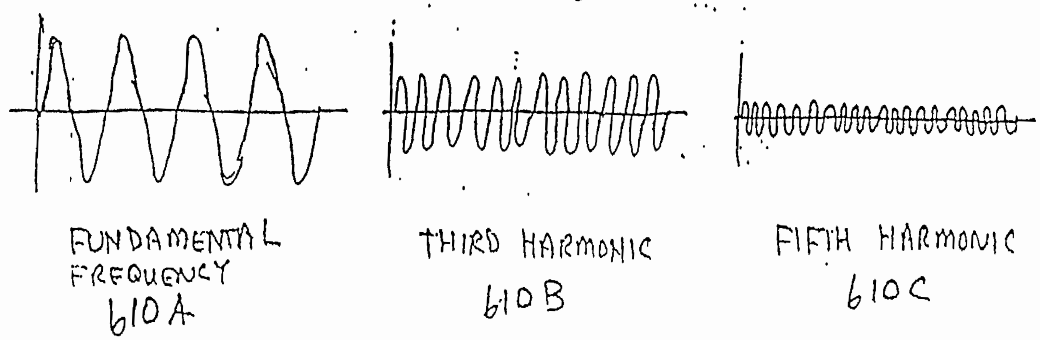


FIG. 6F

HARMONICS OF SIGNAL 612 (SHOWN SEPARATELY)

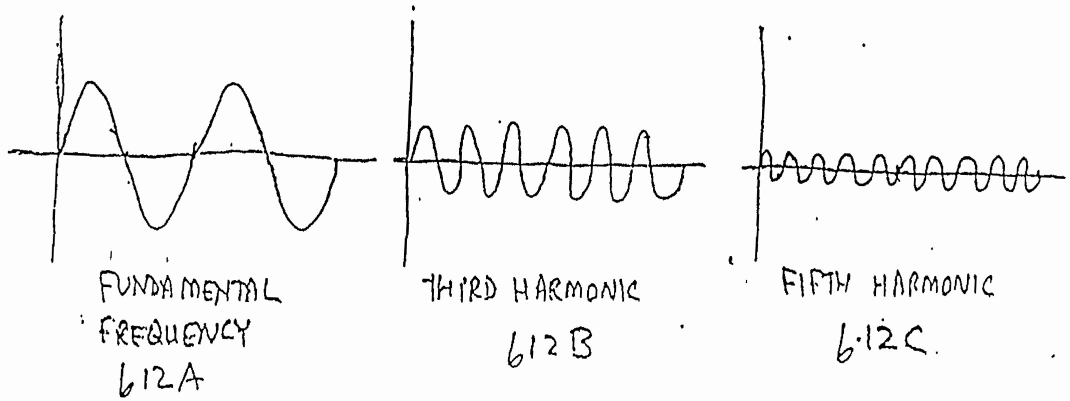


FIG. 6G

FIG. 6 (cont.)

HARMONICS OF SIGNALS 610 AND 612. (SHOWN SIMULTANEOUSLY BUT NOT SUMMED)

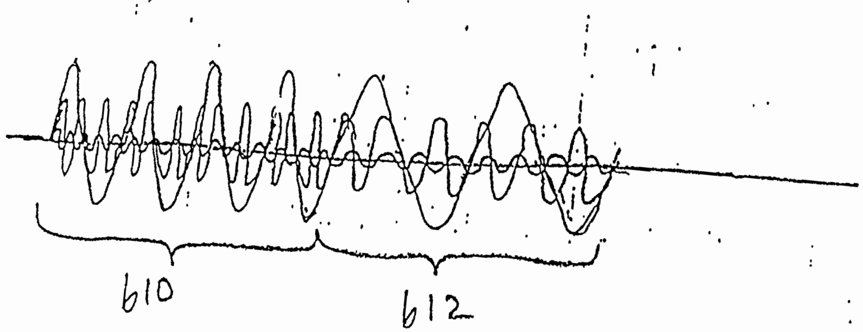


FIG 6H

FILTERED OUTPUT SIGNAL 614

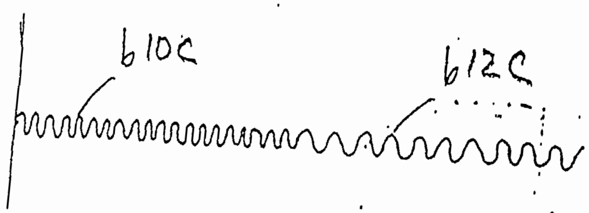


FIG. 6I

FIG 6 (cont.)

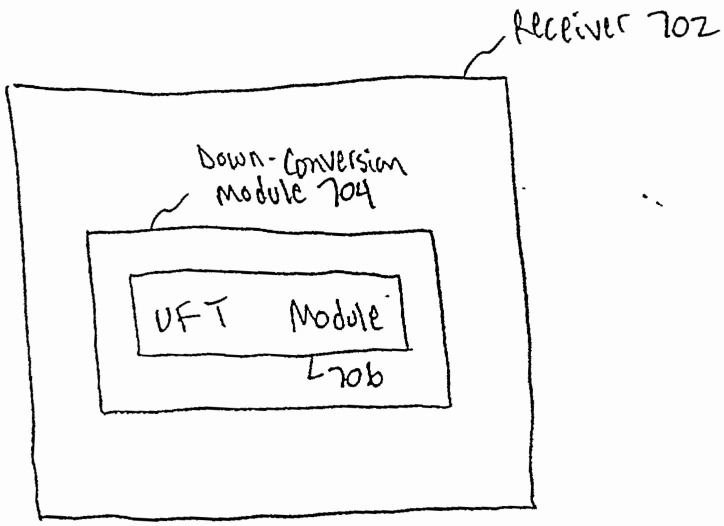


FIG. 7

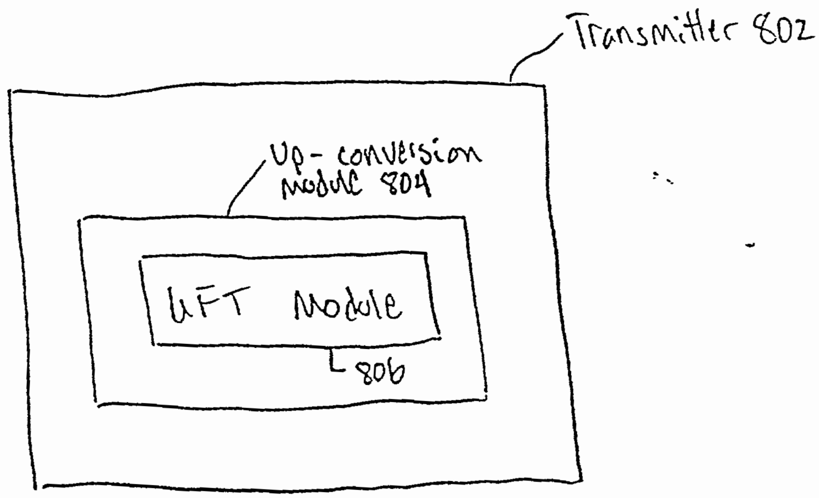


FIG. 8

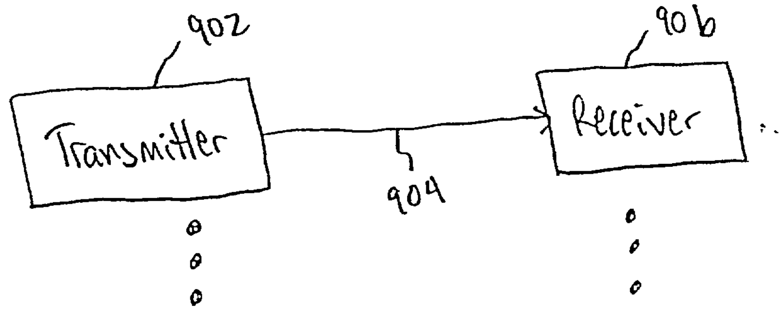
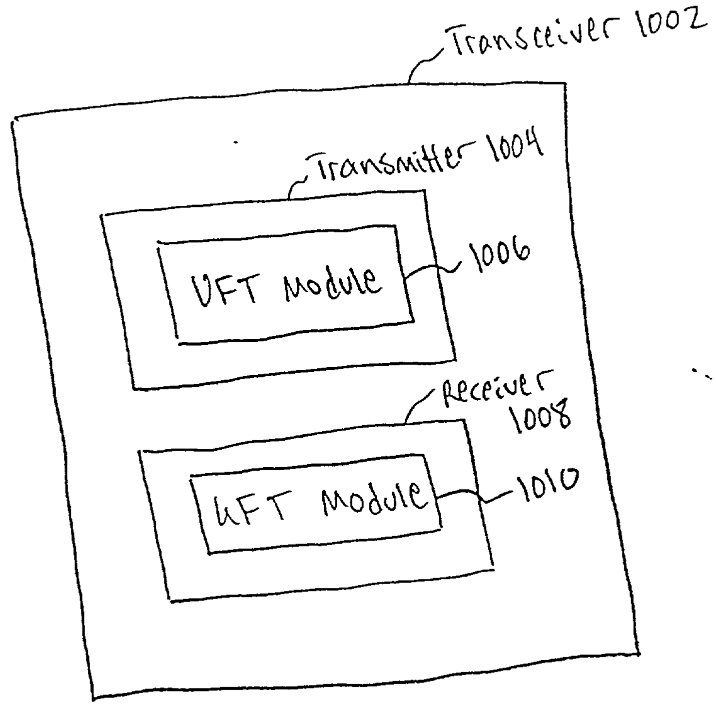


FIG. 9



Transceiver 1002
Transmitter 1004
UFT Module
1006
Receiver
1008
UFT Module
1010

FIG. 10

M

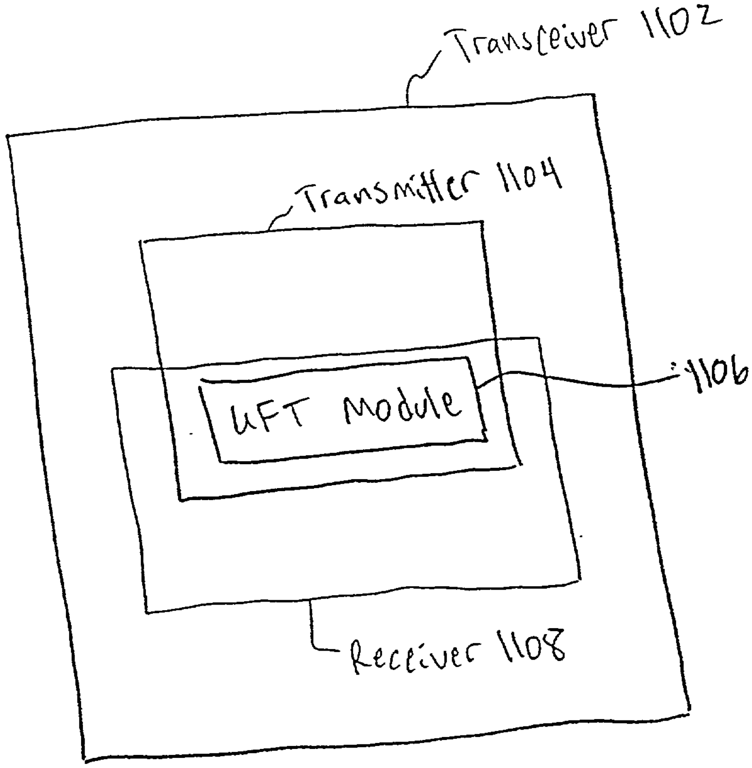

Transceiver 1102
Transmitter 1104
UFT Module
1106
Receiver 1108

FIG. 11

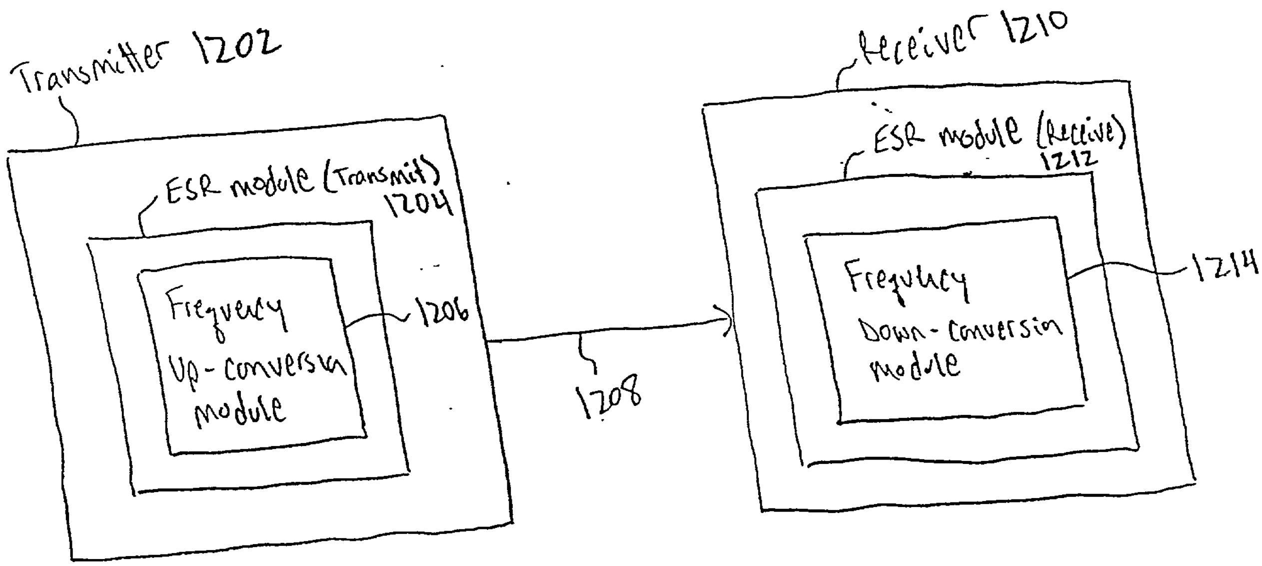
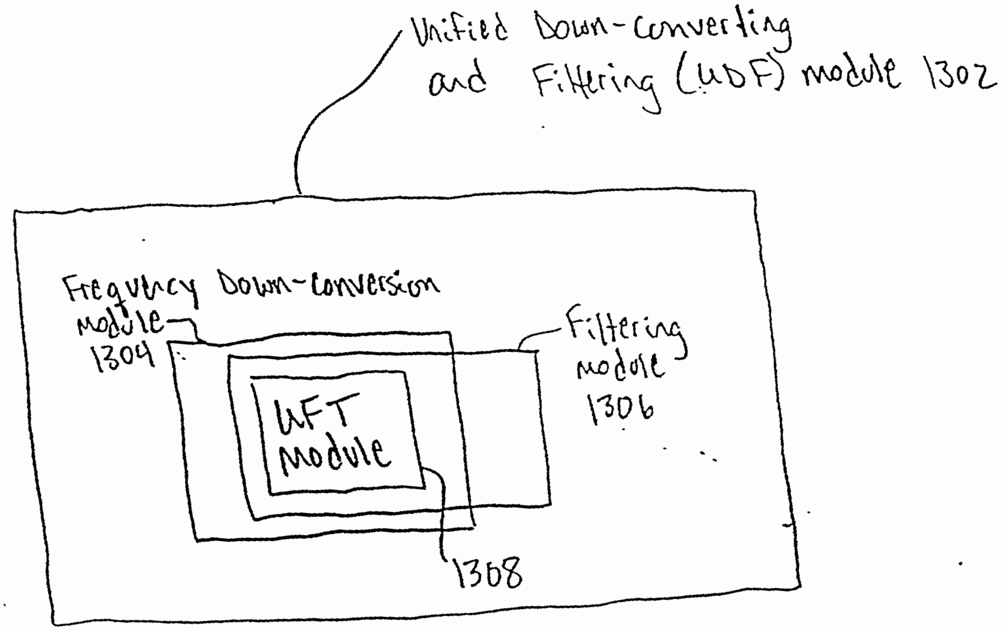

Transmitter 1202
ESR module (Transmit) 1204
Frequency Up-conversion module
1206
1208
Receiver 1210
ESR module (Receive) 1212
Frequency Down-conversion module
1214

FIG. 12



Unified Down-converting and Filtering (UDF) module 1302
Frequency Down-conversion module 1304
Filtering module 1306
UFT Module
1308

FIG. 13

M

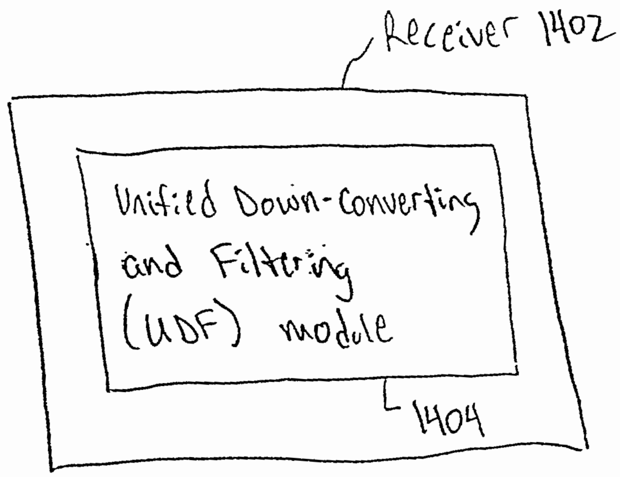

Receiver 1402
Unified Down-Converting and Filtering (UDF) module
1404

FIG. 14

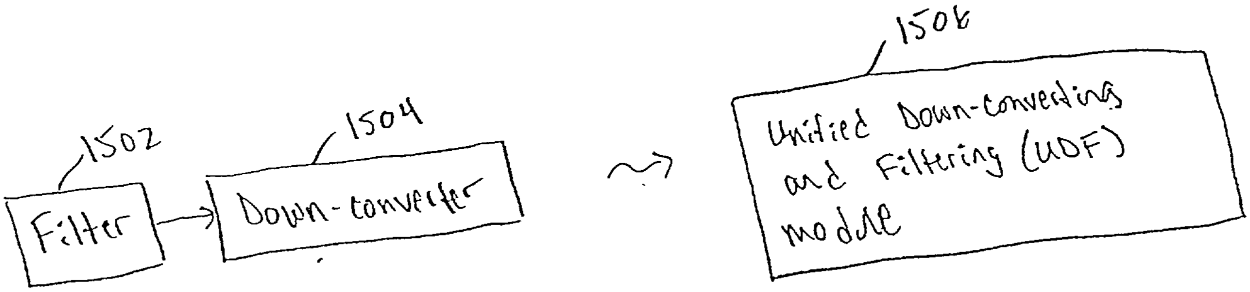


FIG. 15A

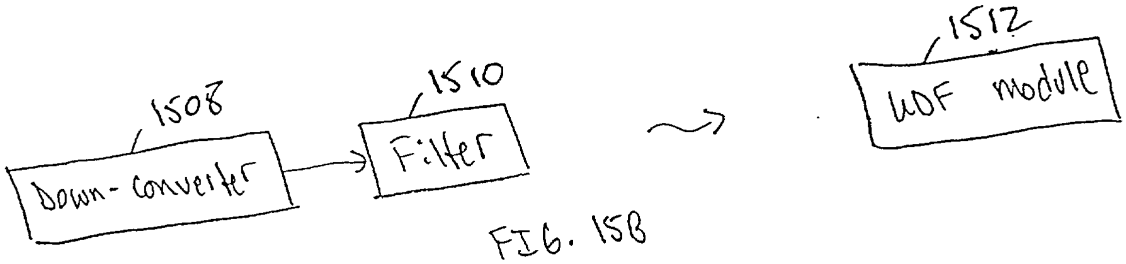


FIG. 15B

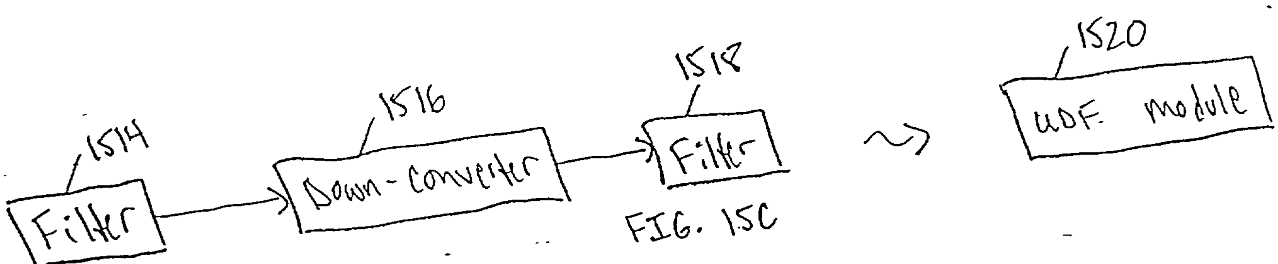


FIG. 15C

FIG. 15D

FIG. 15E

m

FIG. 15F

m

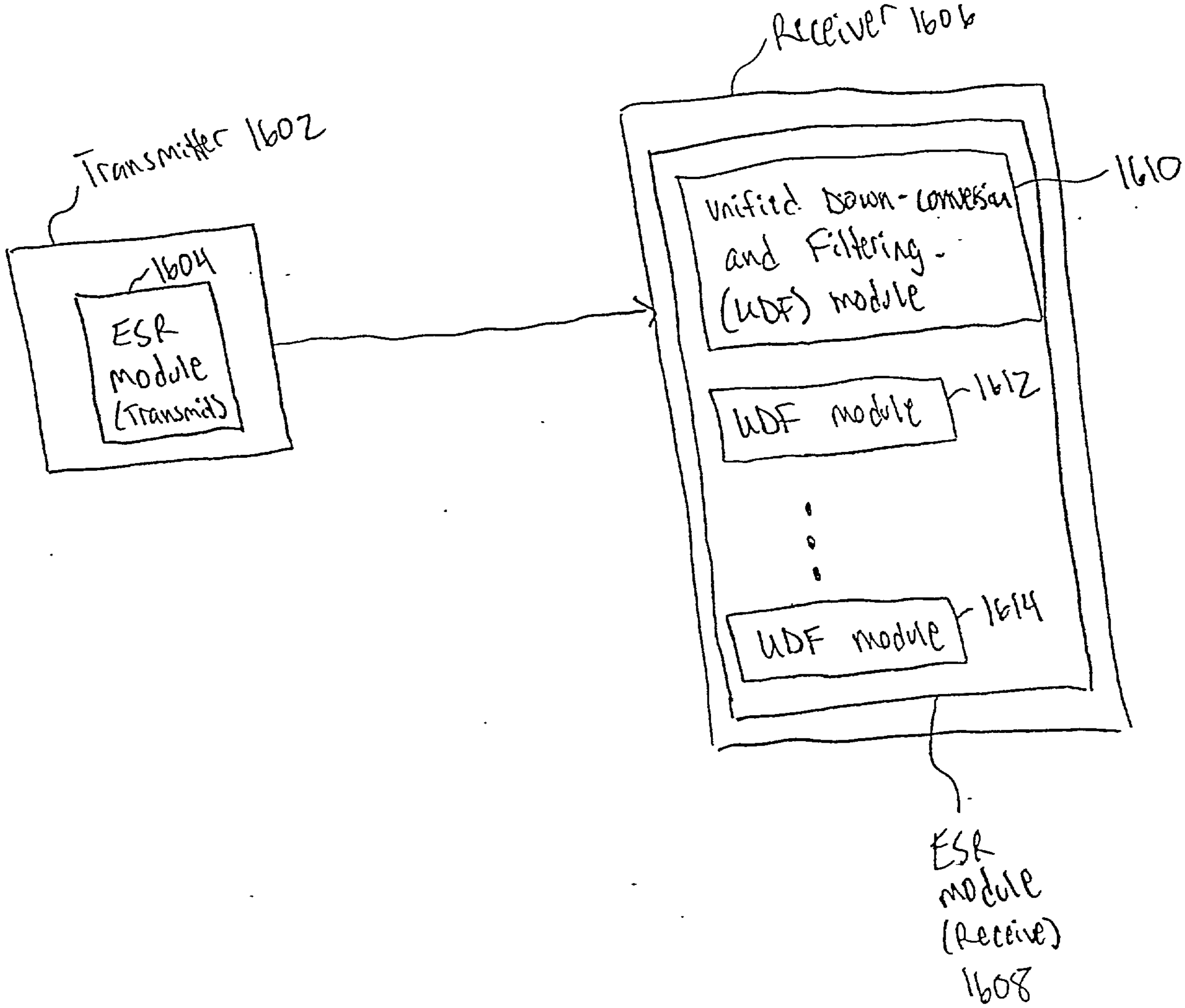

Transmitter 1602
1604
ESR module (Transmit)
Receiver 1606
Unified Down-conversion and Filtering (UDF) module
1610
UDF module
1612
UDF module
1614
ESR module (Receive) 1608

FIG. 16

M

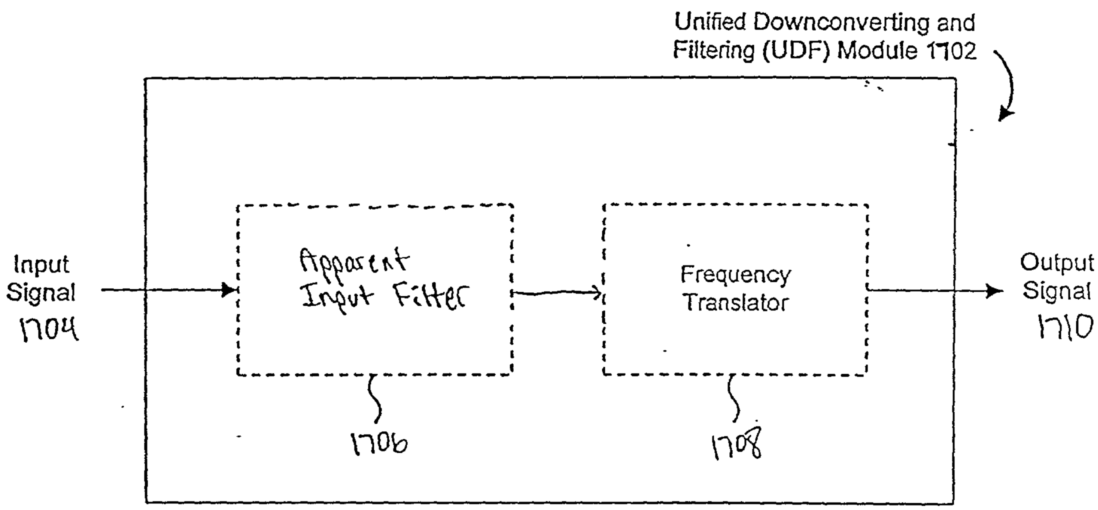


FIG. 17

9809-02.vsd/1

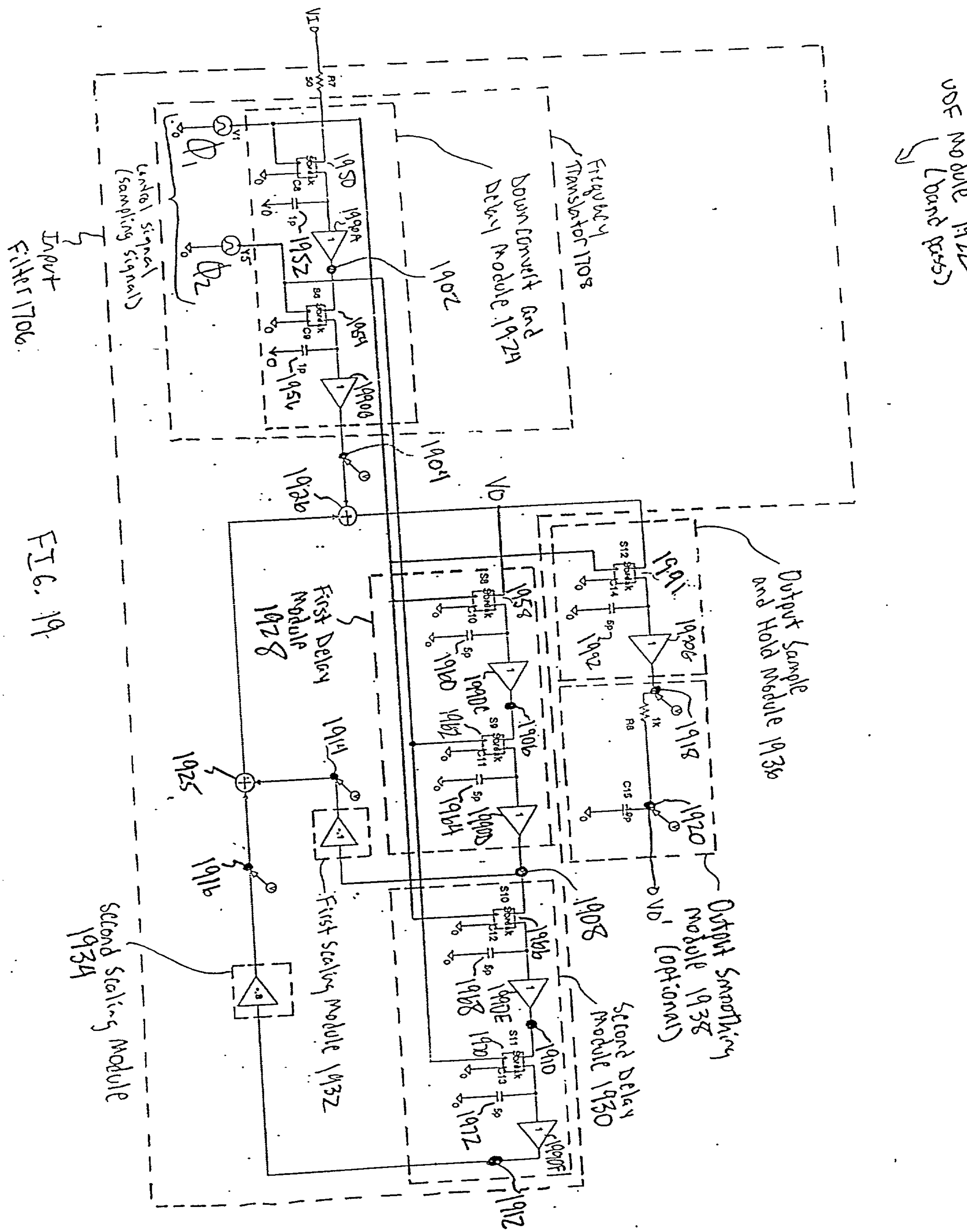
m

1802

Time / Node	t-1 (rising edge of ϕ_1)	t-1 (rising edge of ϕ_2)	t (rising edge of ϕ_1)	t (rising edge of ϕ_2)	t+1 (rising edge of ϕ_1)
1902	VI_{t-1} 1804	VI_{t-1} 1808	VI_t 1816	VI_t 1826	VI_{t+1} 1838
1904	—	VI_{t-1} 1810	VI_{t-1} 1818	VI_t 1828	VI_t 1840
1906	VO_{t-1} 1806	VO_{t-1} 1812	VO_t 1820	VO_t 1830	VO_{t+1} 1842
1908	—	VO_{t-1} 1814	VO_{t-1} 1822	VO_t 1832	VO_t 1844
1910	— 1807	—	VO_{t-1} 1824	VO_{t-1} 1834	VO_t 1846
1912	—	— 1815	—	VO_{t-1} 1836	VO_{t-1} 1848
1918	—	—	—	—	VI_t - 0.1 * VO_t - 0.8 * VO_{t-1} 1850

FIG. 18

9809-02.vsc



VDF Module 1922 (band pass)
Frequency Translator 1708
Down Convert and Delay Module 1924
Control signal (sampling signal)
Input Filter 1706
Output Sample and Hold Module 1936
Output Smoothing Module 1938
VO' (optional)
First Delay Module 1928
Second Delay Module 1930
First Scaling Module 1932
Second Scaling Module 1934

FIG. 19.

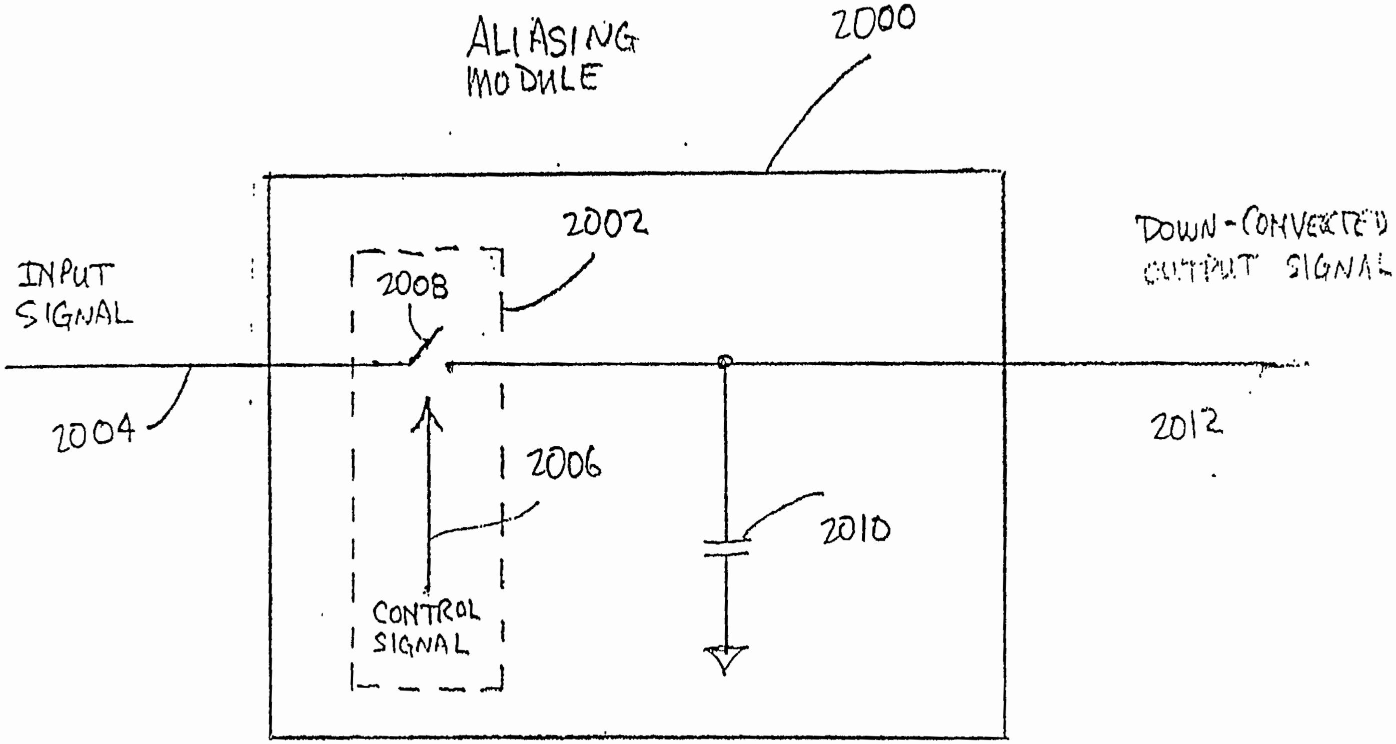

ALIASING MODULE
2000
2002
DOWN-CONVERTED OUTPUT SIGNAL
INPUT SIGNAL
2008
2004
2012
2006
2010
CONTROL SIGNAL

FIG. 20A

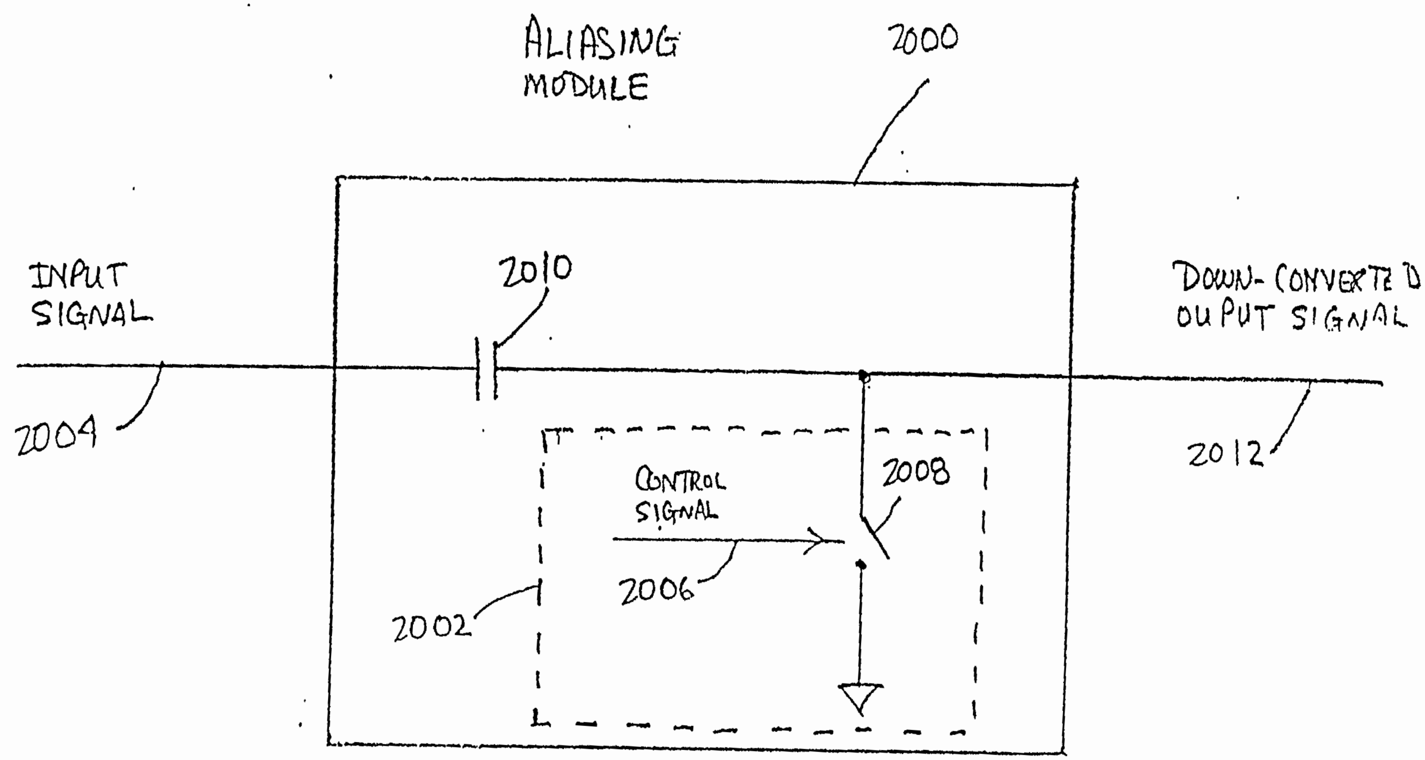

ALIASING
MODULE
2000
INPUT
SIGNAL
2010
DOWN-CONVERTED
OUPUT SIGNAL
2004
2012
2008
CONTROL
SIGNAL
2006
2002

FIG. 20A-1

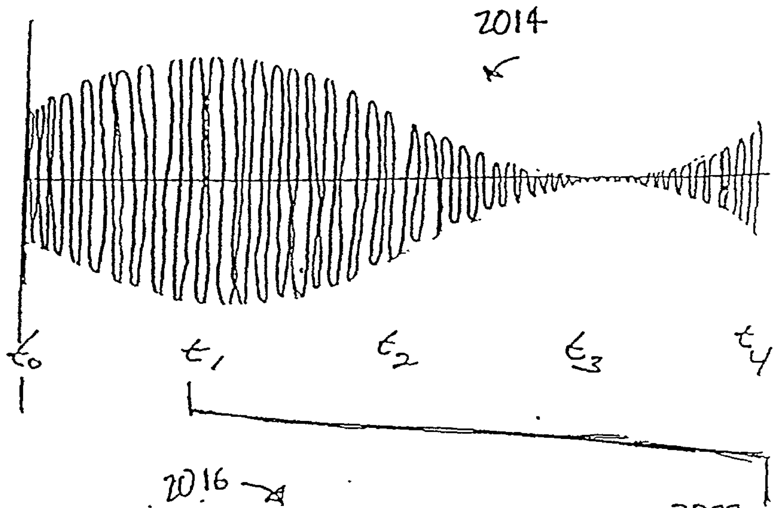


FIG. 20B

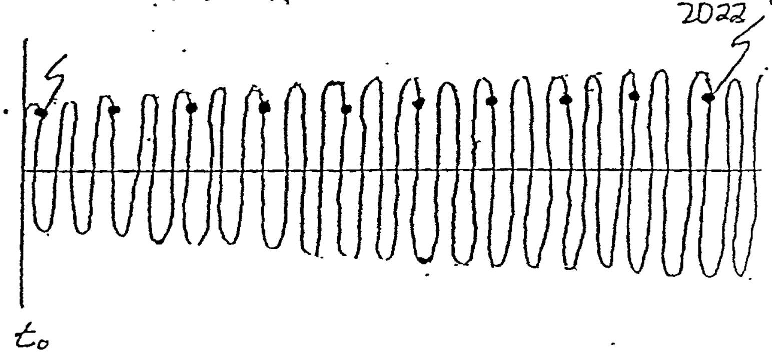


FIG. 20C

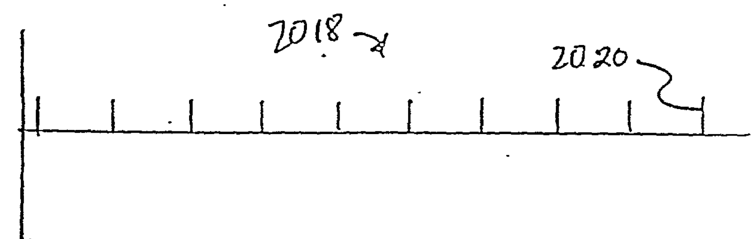


FIG. 20D

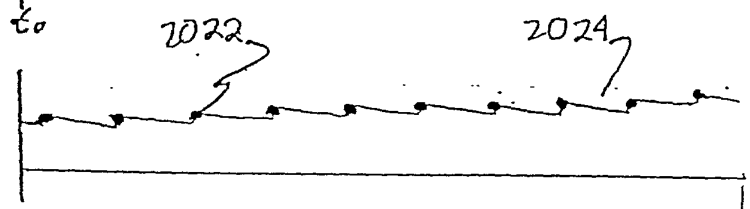


FIG. 20E

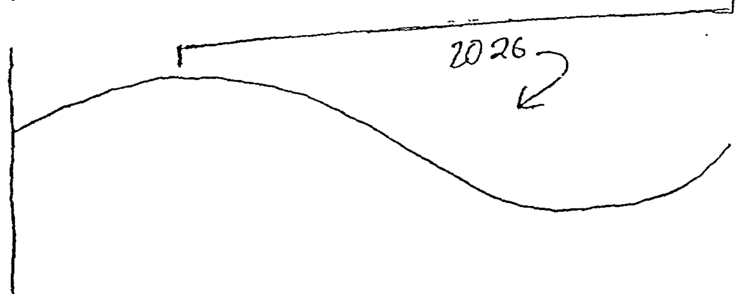


FIG. 20F

M

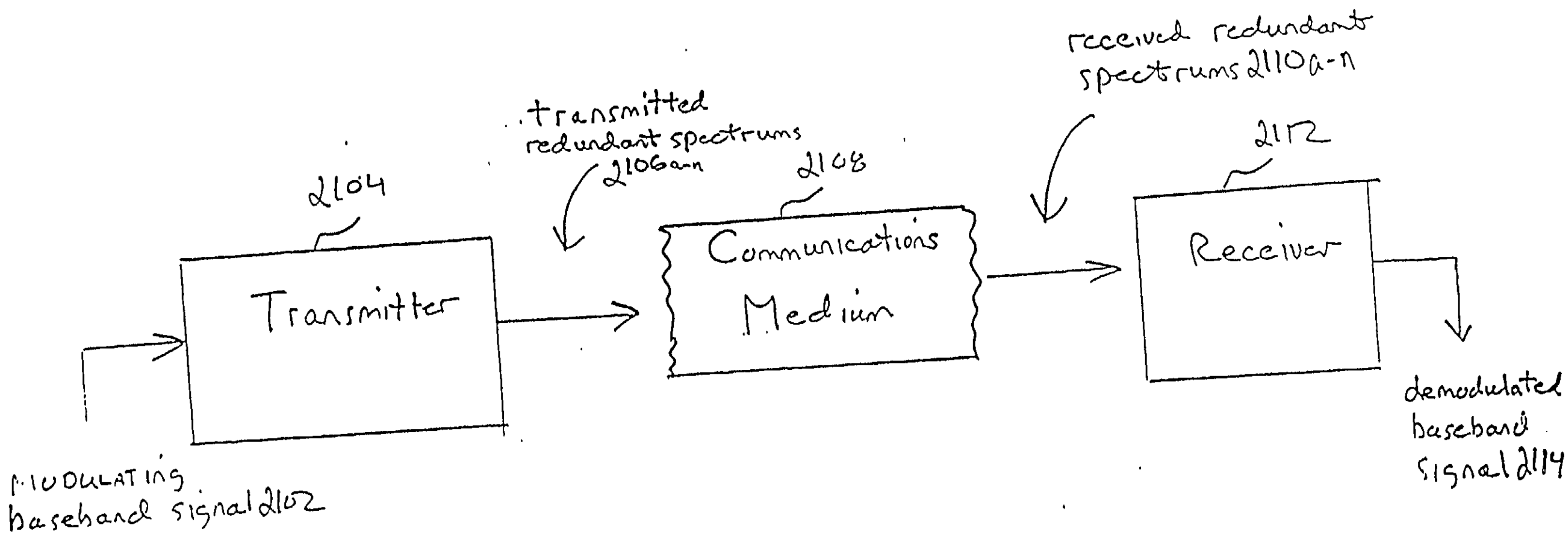

MODULATING baseband signal 2102
Transmitter
2104
transmitted redundant spectrums 2106a-n
Communications Medium
2108
received redundant spectrums 2110a-n
Receiver
2112
demodulated baseband signal 2114

FIG. 21

FIG. 22A

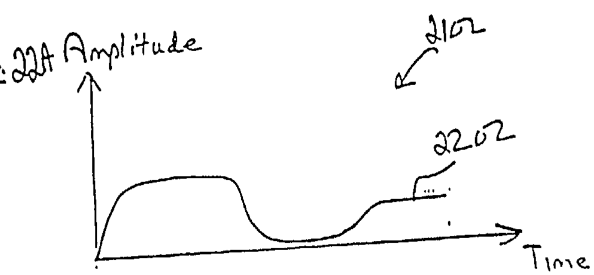


FIG. 22B

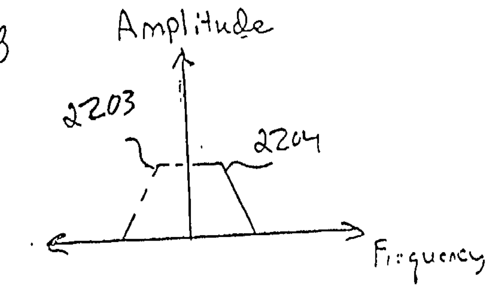


FIG. 22C

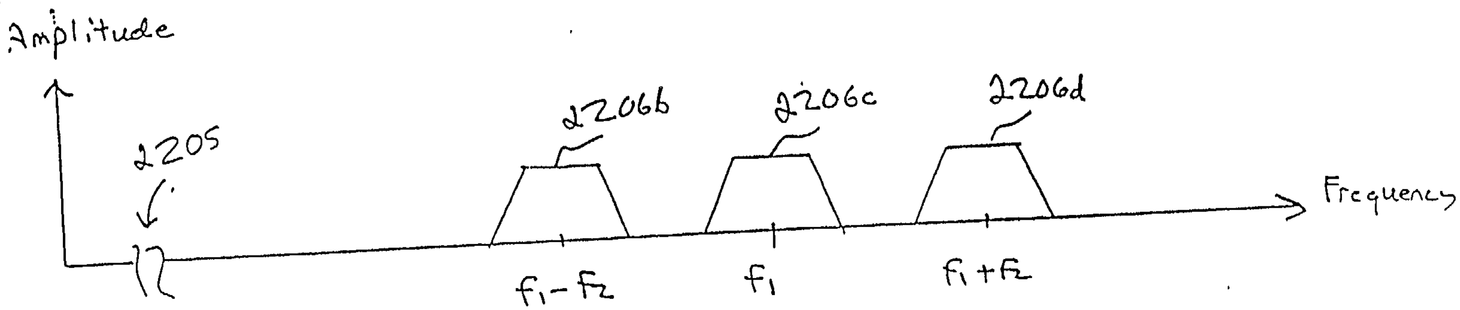
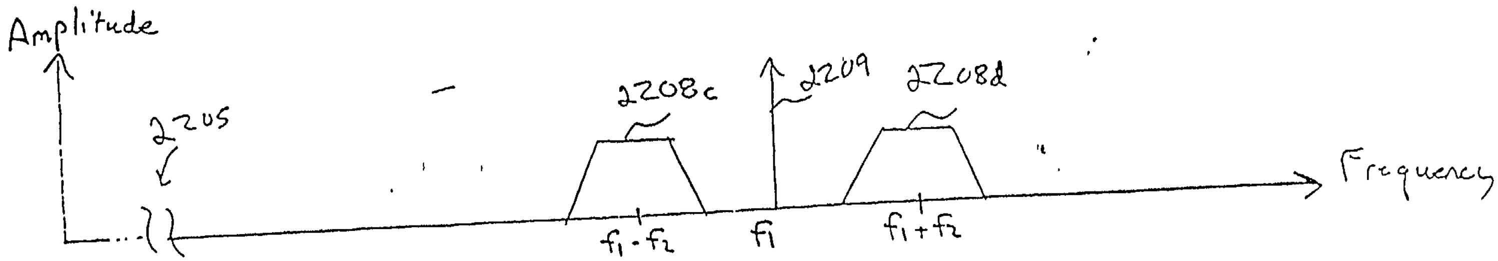


FIG. 22D



09632856 .080400

FIG. 22E

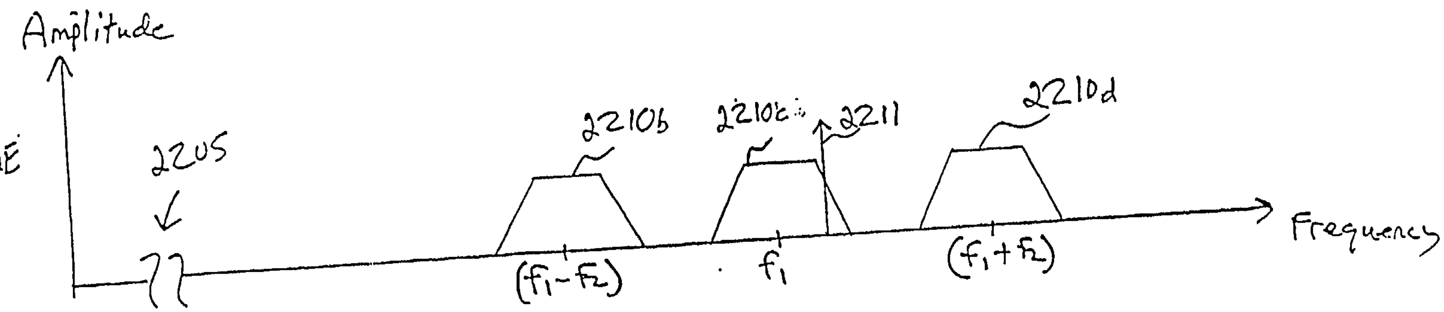


FIG. 22F

09632856.080400

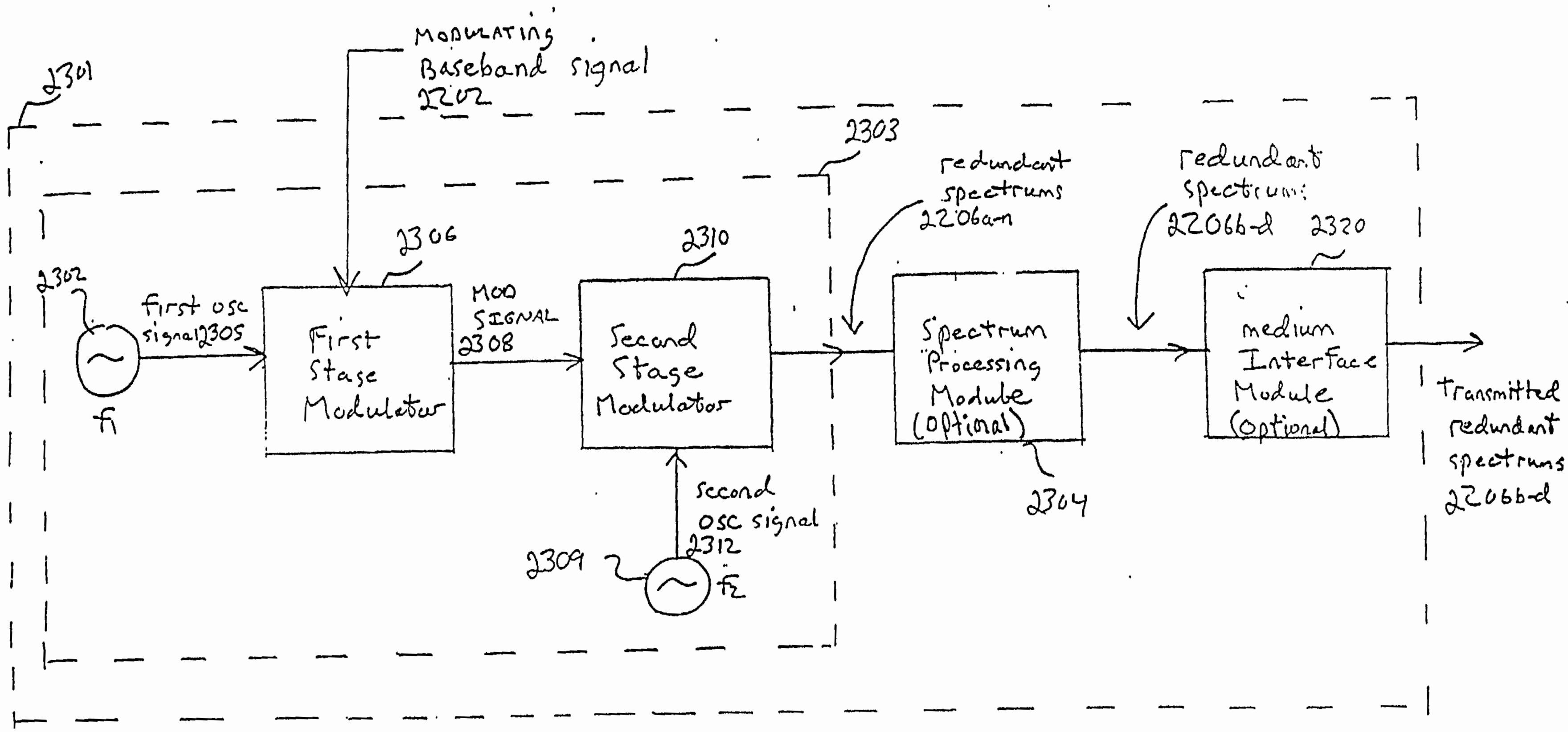

Modulating Baseband signal 2202
2301
2303
2302
first osc signal 2305
2306
First Stage Modulator
MOD SIGNAL 2308
2310
Second Stage Modulator
redundant spectrums 2206a-n
Spectrum Processing Module (optional)
2304
redundant spectrum 2206b-d
2320
medium Interface Module (optional)
Transmitted redundant spectrums 2206b-d
F1
second osc signal 2312
2309
F2

FIG. 23A

31

FIG. 23B

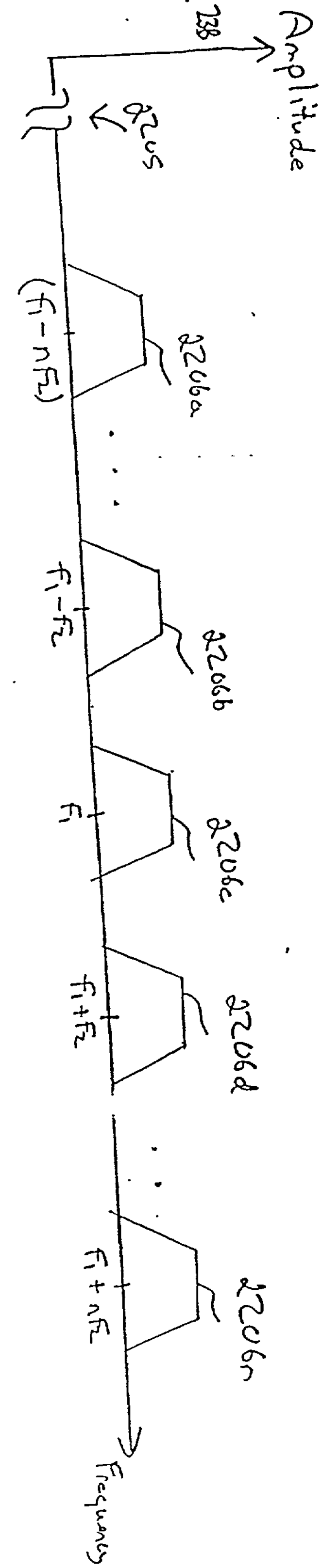
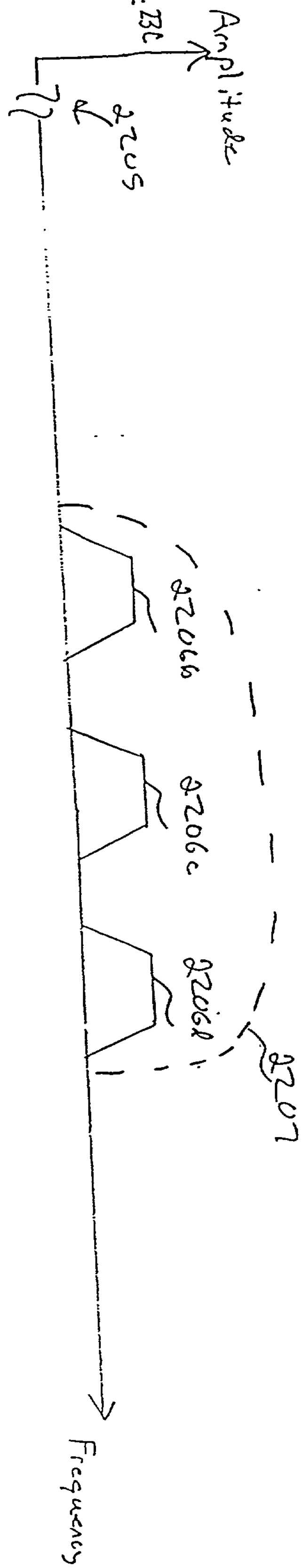


FIG. 23C



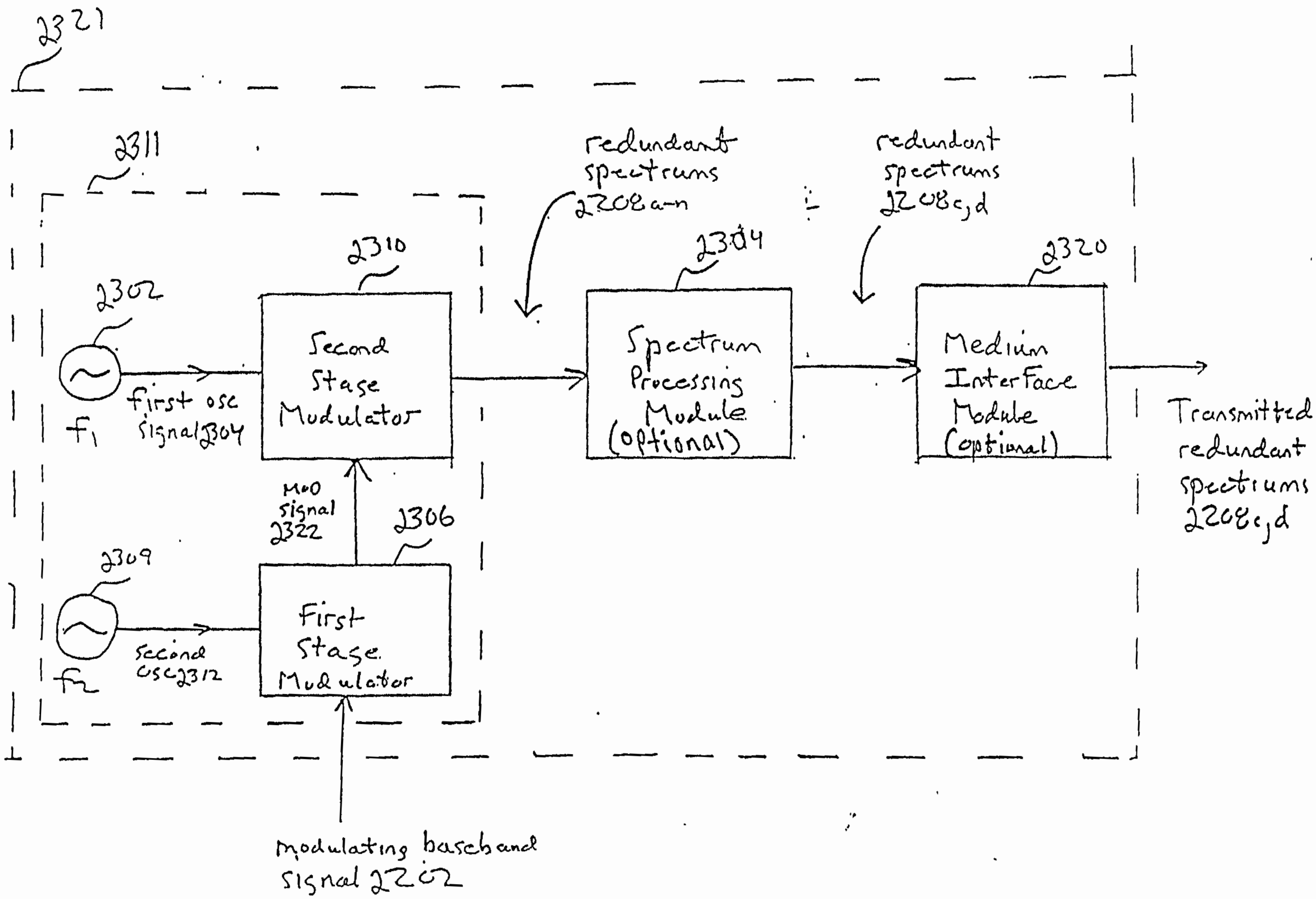

2321
2311
2310
2302
Second Stage Modulator
first osc signal 2304
f_1
MOD signal 2322
2306
2309
First Stage Modulator
second osc 2312
f_2
redundant spectrums 2208a-n
2304
Spectrum Processing Module (optional)
redundant spectrums 2208c,d
2320
Medium Interface Module (optional)
Transmitted redundant spectrums 2208c,d
modulating baseband signal 2202

FIG. 23D

FIG. 23E

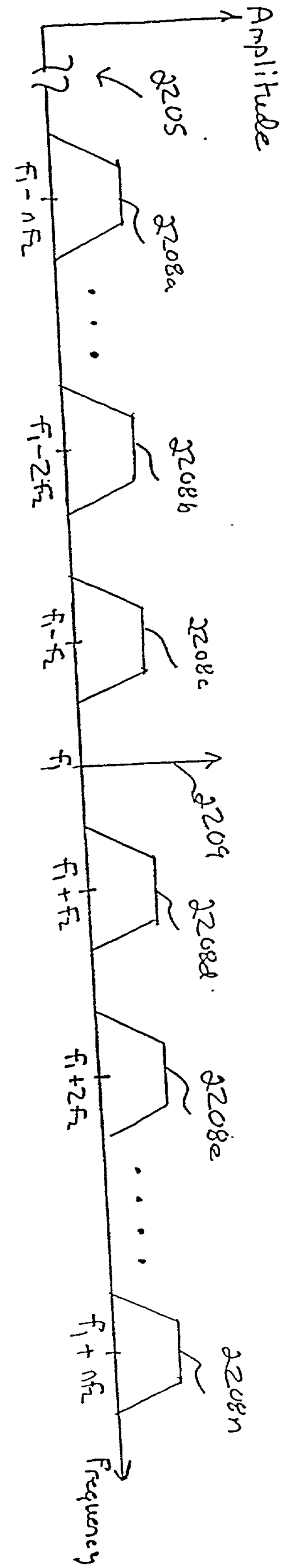
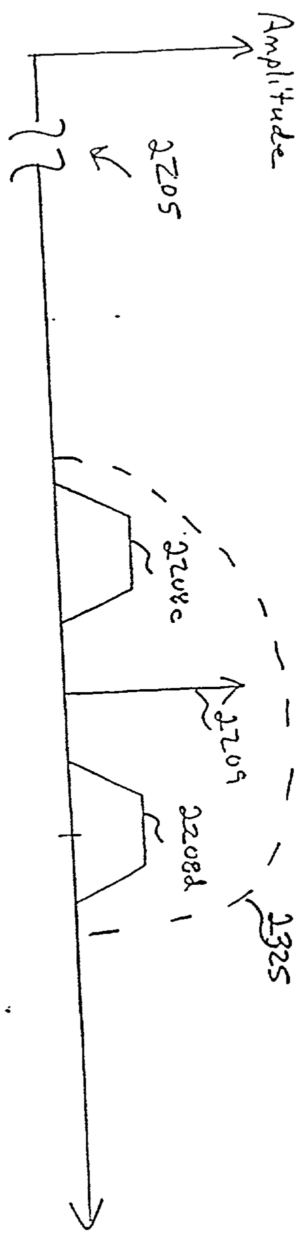


FIG. 23F



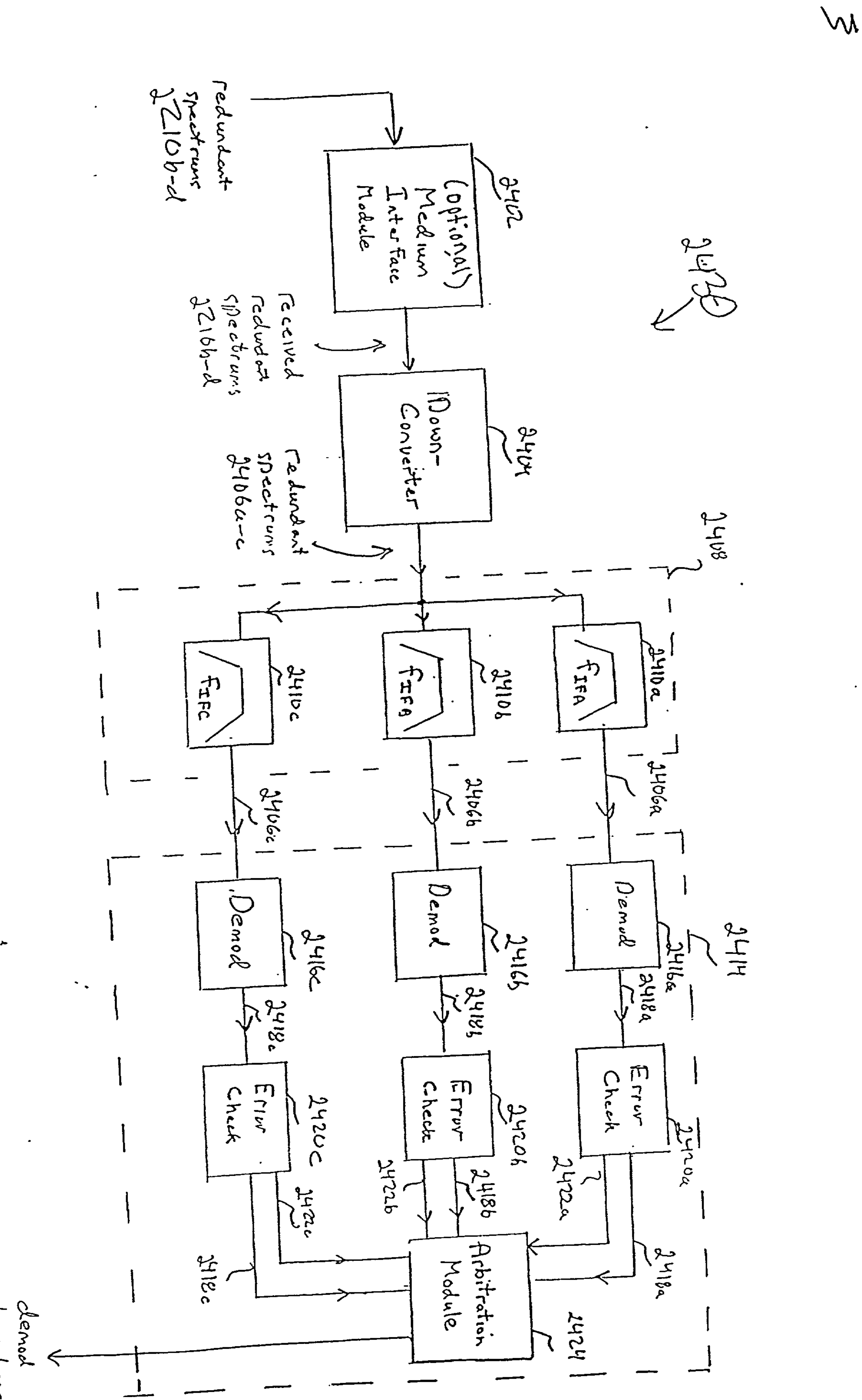

redundant spectrums 2210b-d
(Optional) Medium InterFace Module
2402
2400
received redundant spectrums 2216b-d
Down-Converter
2404
redundant spectrums 2406a-c
2408
f_{IFA}
2410a
f_{IFB}
2410b
f_{IFC}
2410c
2406a
2406b
2406c
Demod
2416a
Demod
2416b
Demod
2416c
2414
2418a
2418b
2418c
Error Check
2420a
Error Check
2420b
Error Check
2420c
2422a
2422b
2422c
2418a
2418b
2418c
Arbitration Module
2424
demod baseband signal 2212

FIG. 24A

FIG. 24B

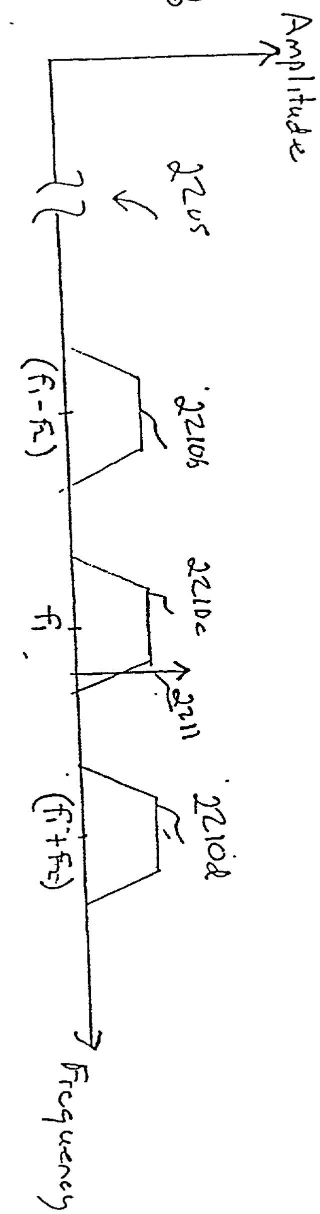
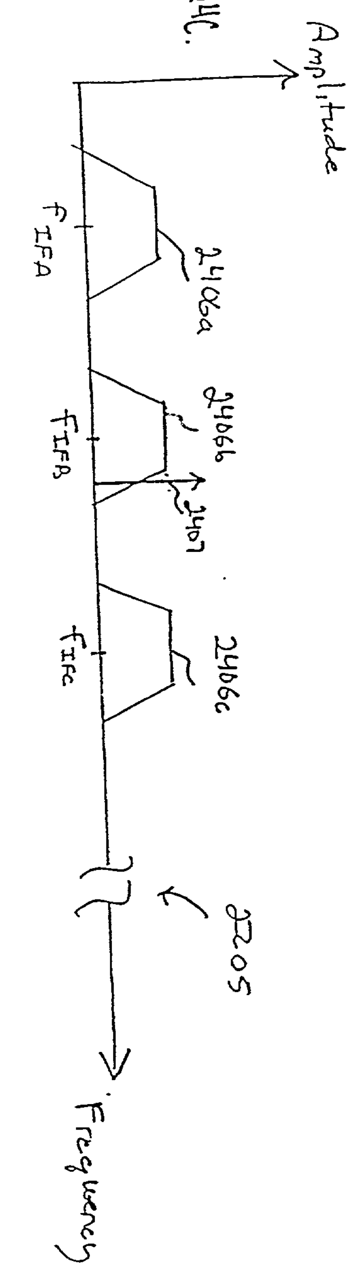


FIG. 24C.



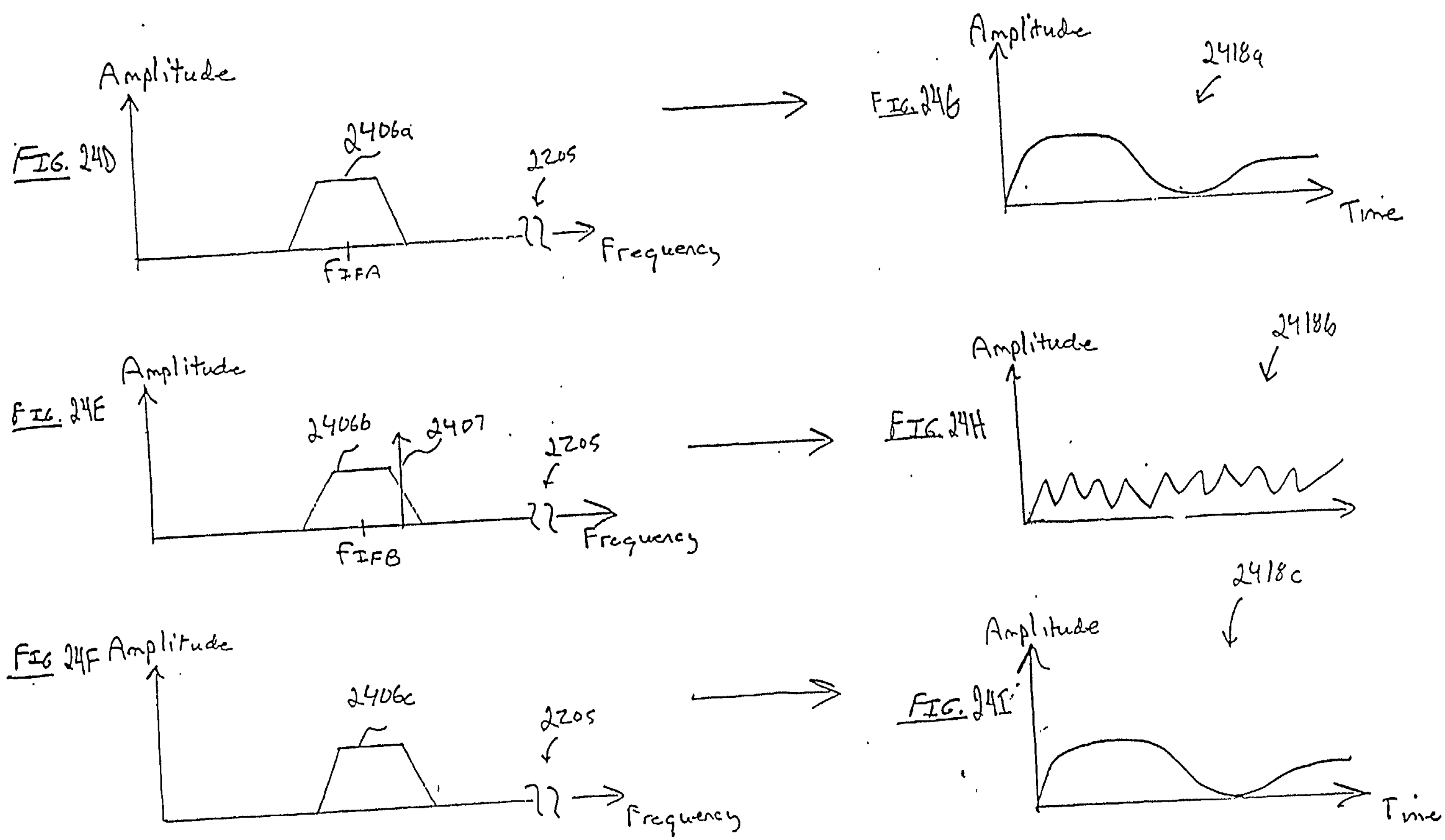


FIG. 24D
Amplitude
2406a
2205
FIFA
Frequency
FIG. 24G
Amplitude
2418a
Time
FIG. 24E
Amplitude
2406b
2407
2205
FIFB
Frequency
FIG. 24H
Amplitude
2418b
FIG 24F
Amplitude
2406c
2205
Frequency
FIG. 24I
Amplitude
2418c
Time

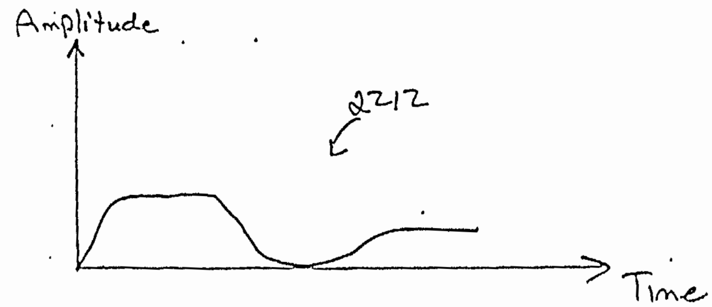
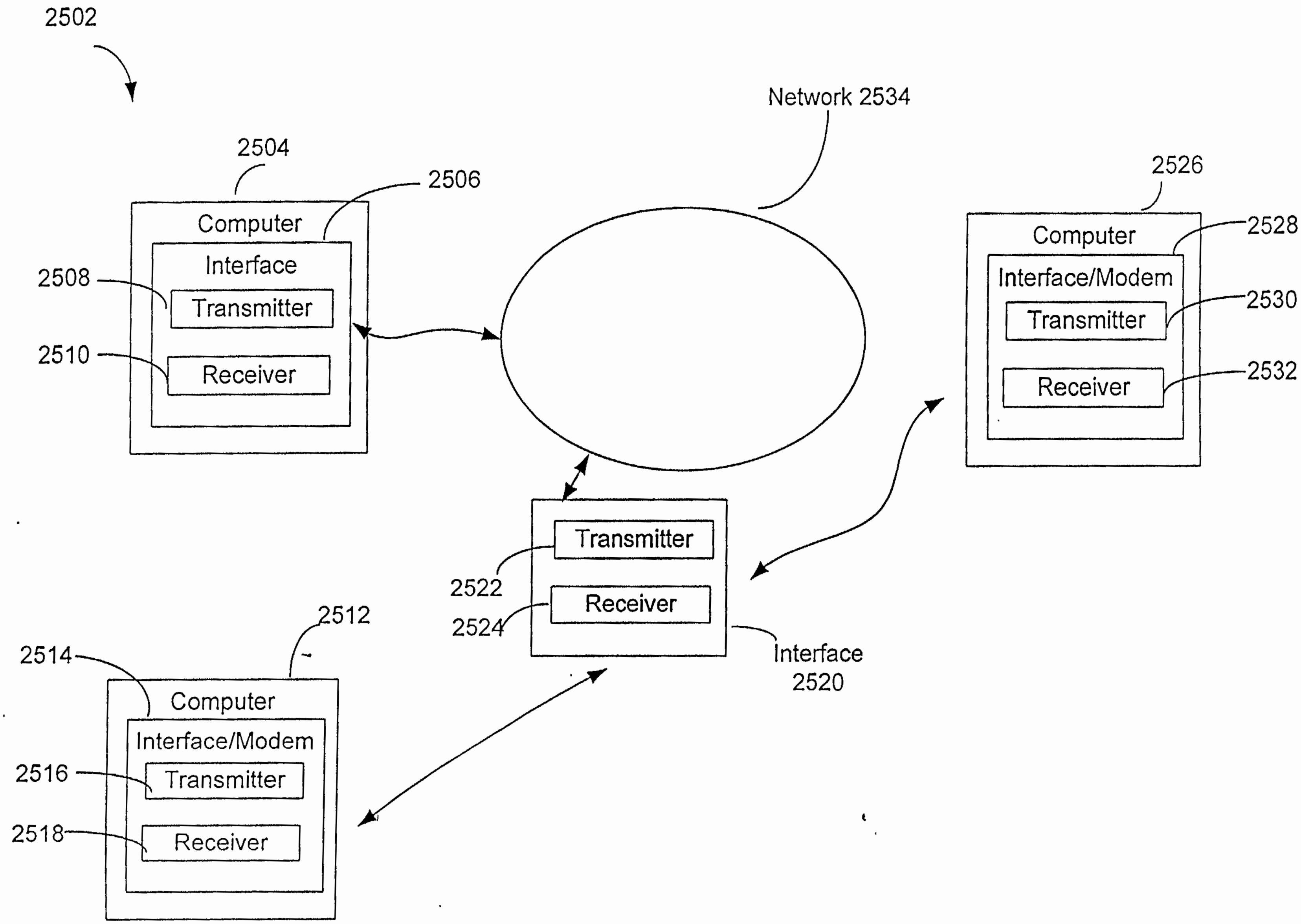


FIG. 24J



2502
2504
Computer
2506
Interface
2508
Transmitter
2510
Receiver
Network 2534
2526
Computer
2528
Interface/Modem
2530
Transmitter
2532
Receiver
Transmitter
2522
Receiver
2524
Interface
2520
2512
2514
Computer
Interface/Modem
2516
Transmitter
2518
Receiver

FIG. 25

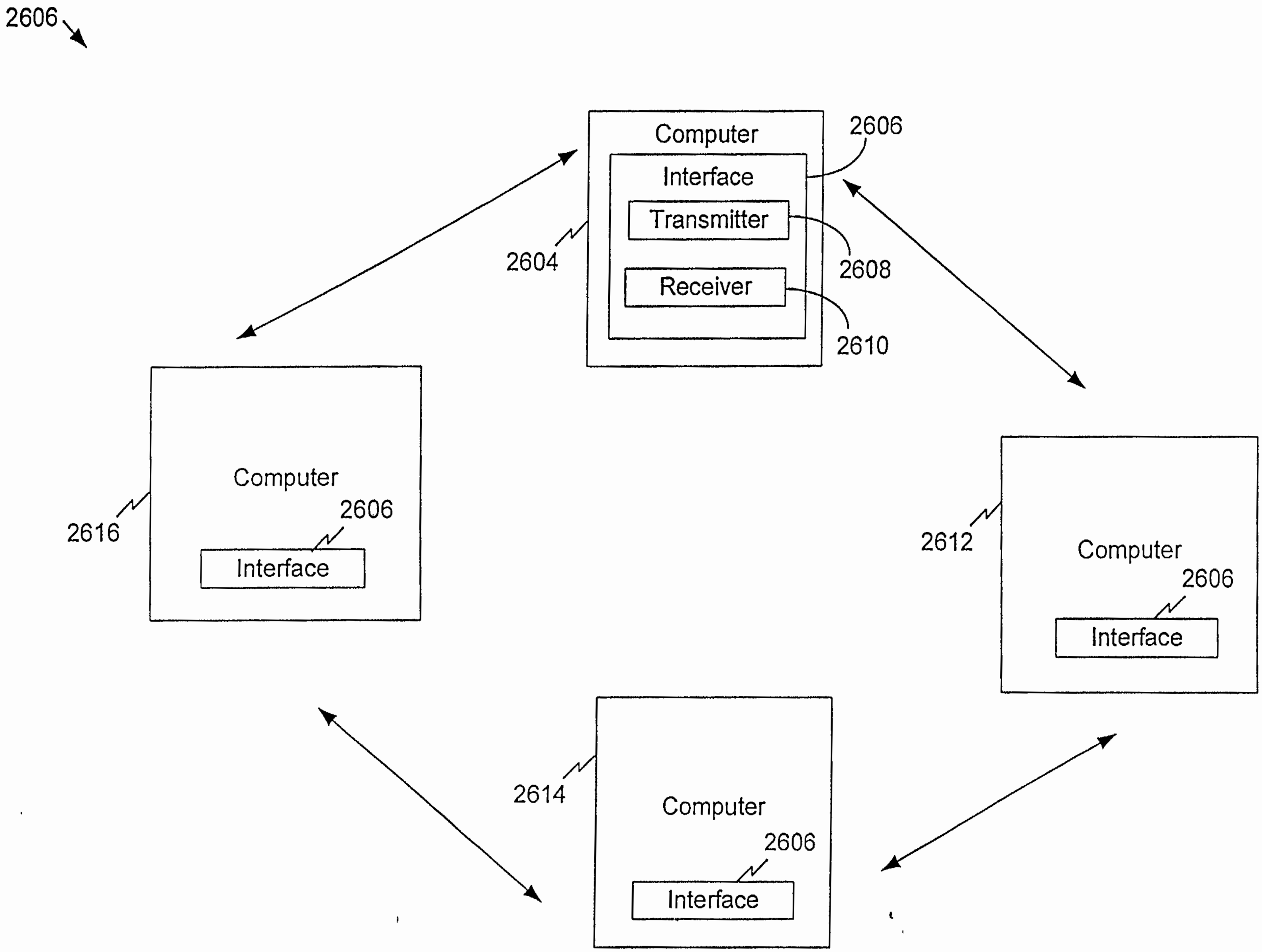


FIG. 26

9905-02

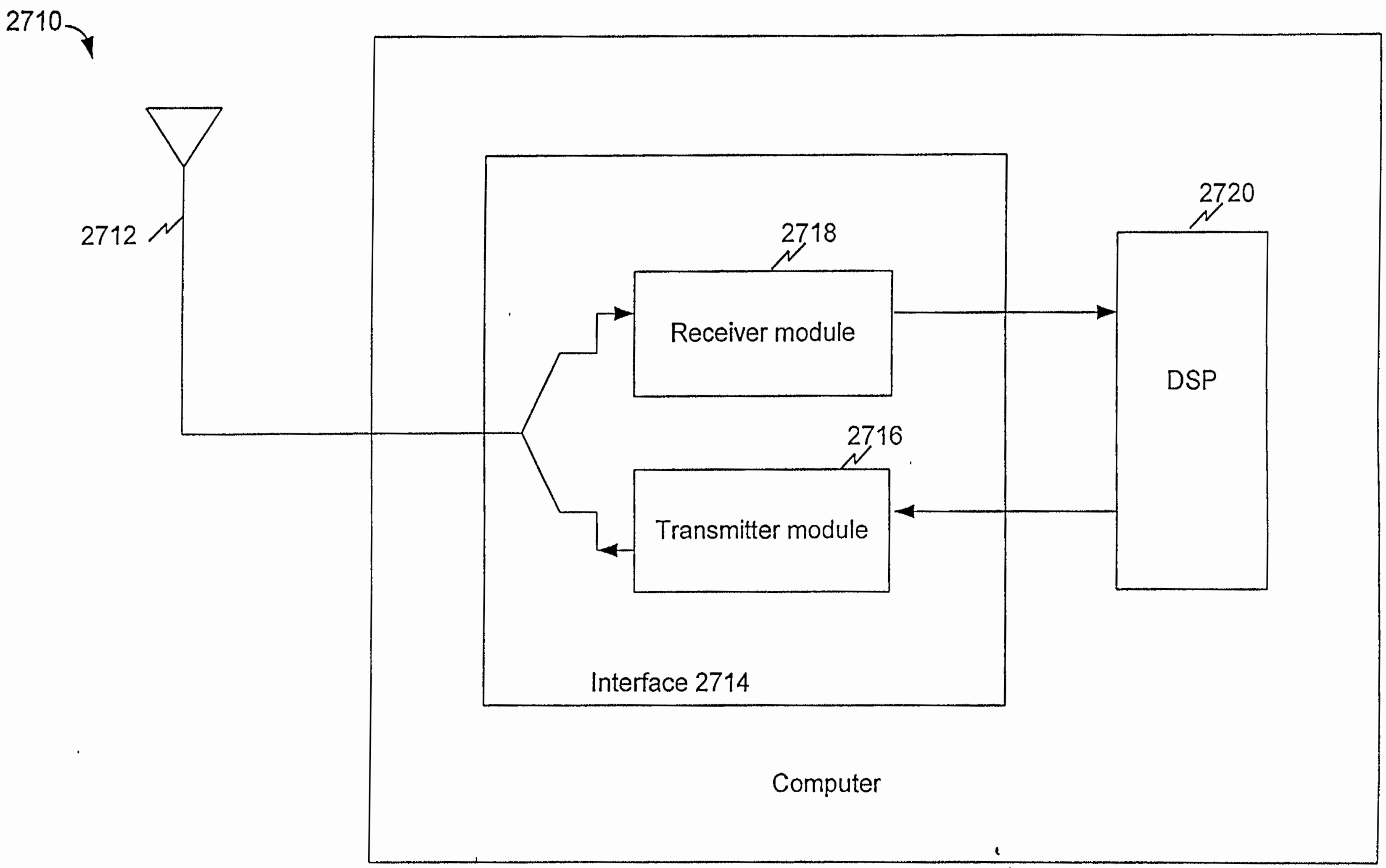
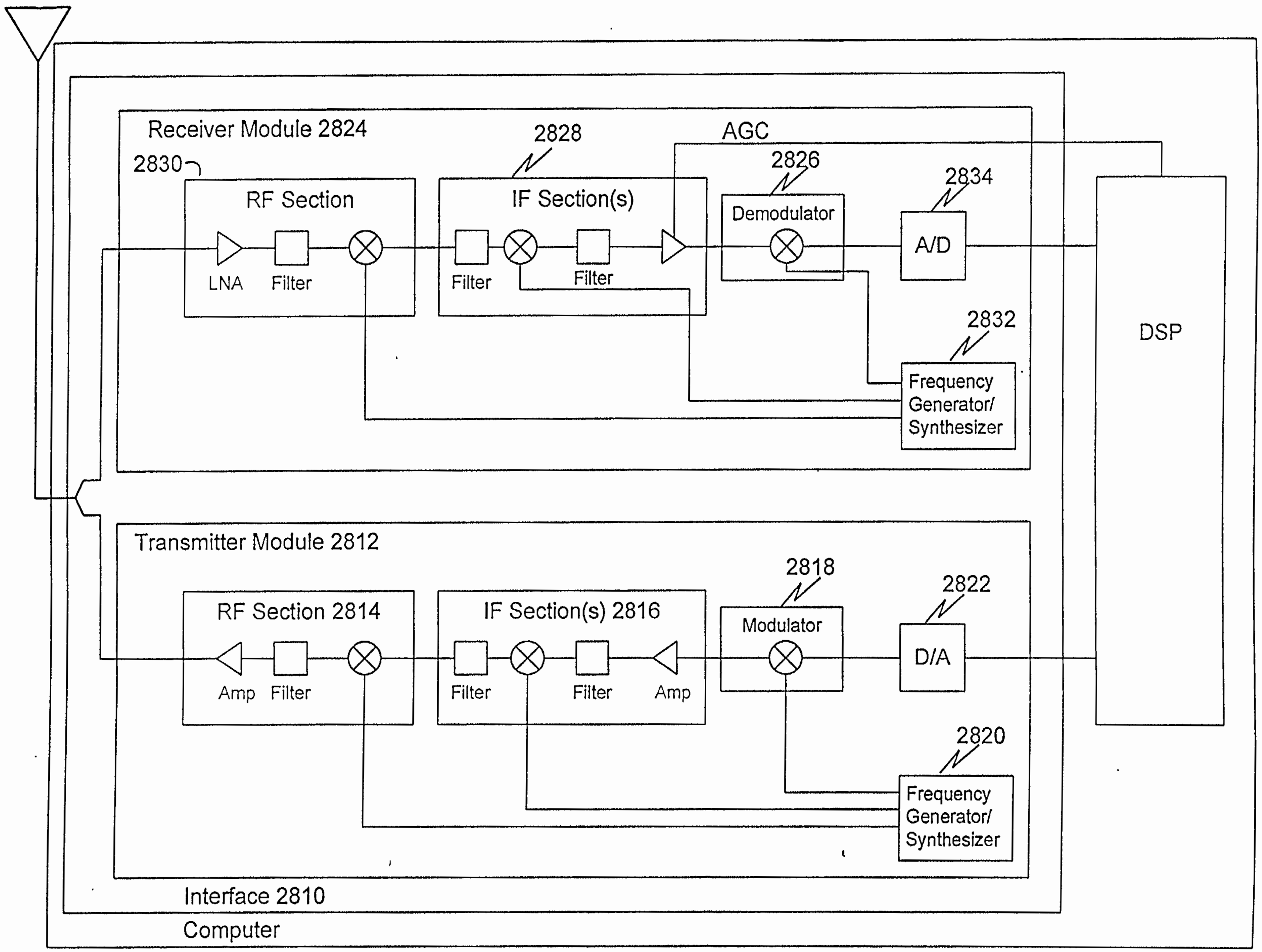

2710
2712
2718
2720
Receiver module
DSP
2716
Transmitter module
Interface 2714
Computer

FIG. 27



Heterodyne Implementation

FIG. 28

9905-02.vsd/2

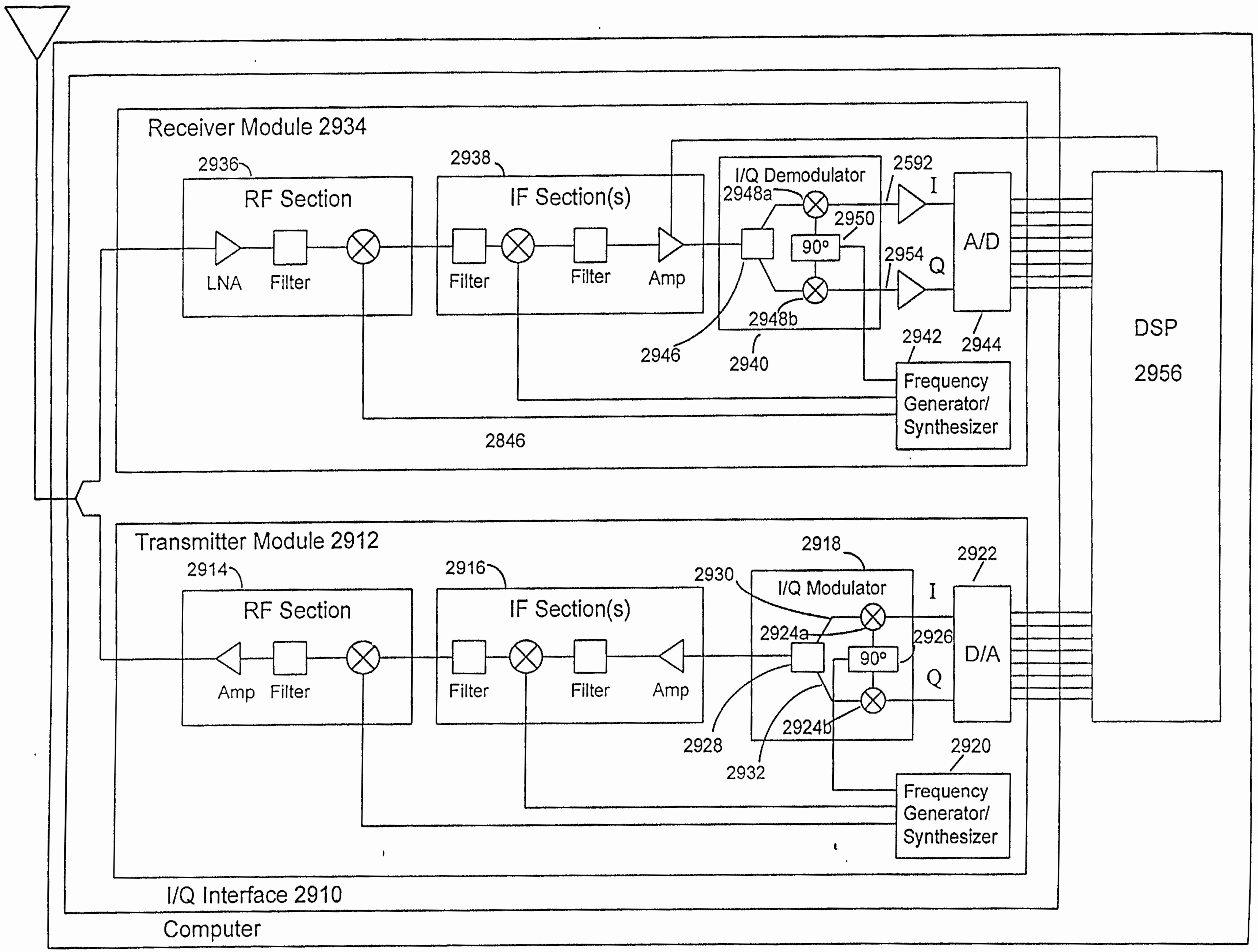


FIG. 29

9905-02.vsd/3

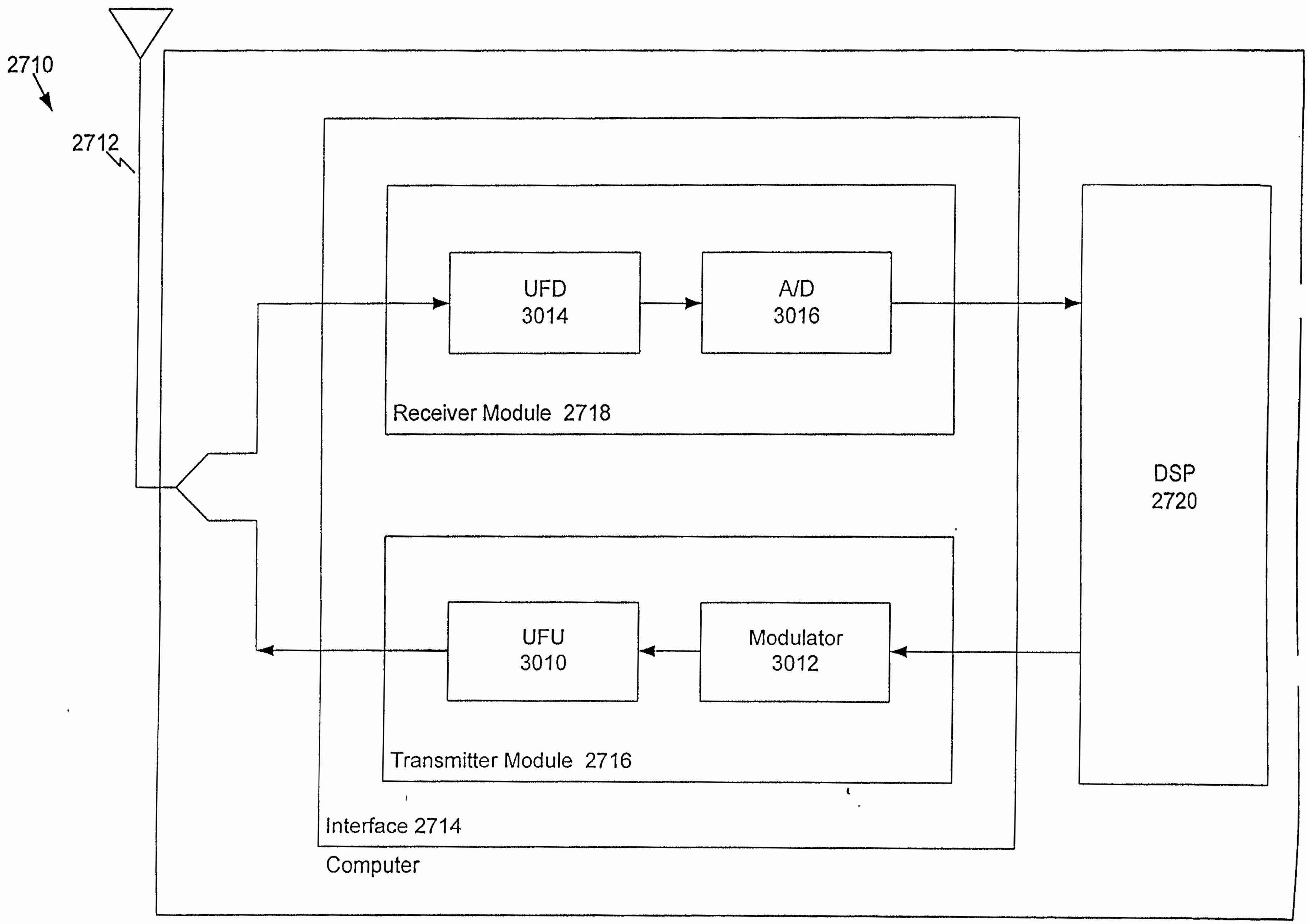

2710
2712
UFD
3014
A/D
3016
Receiver Module 2718
DSP
2720
UFU
3010
Modulator
3012
Transmitter Module 2716
Interface 2714
Computer

FIG. 30

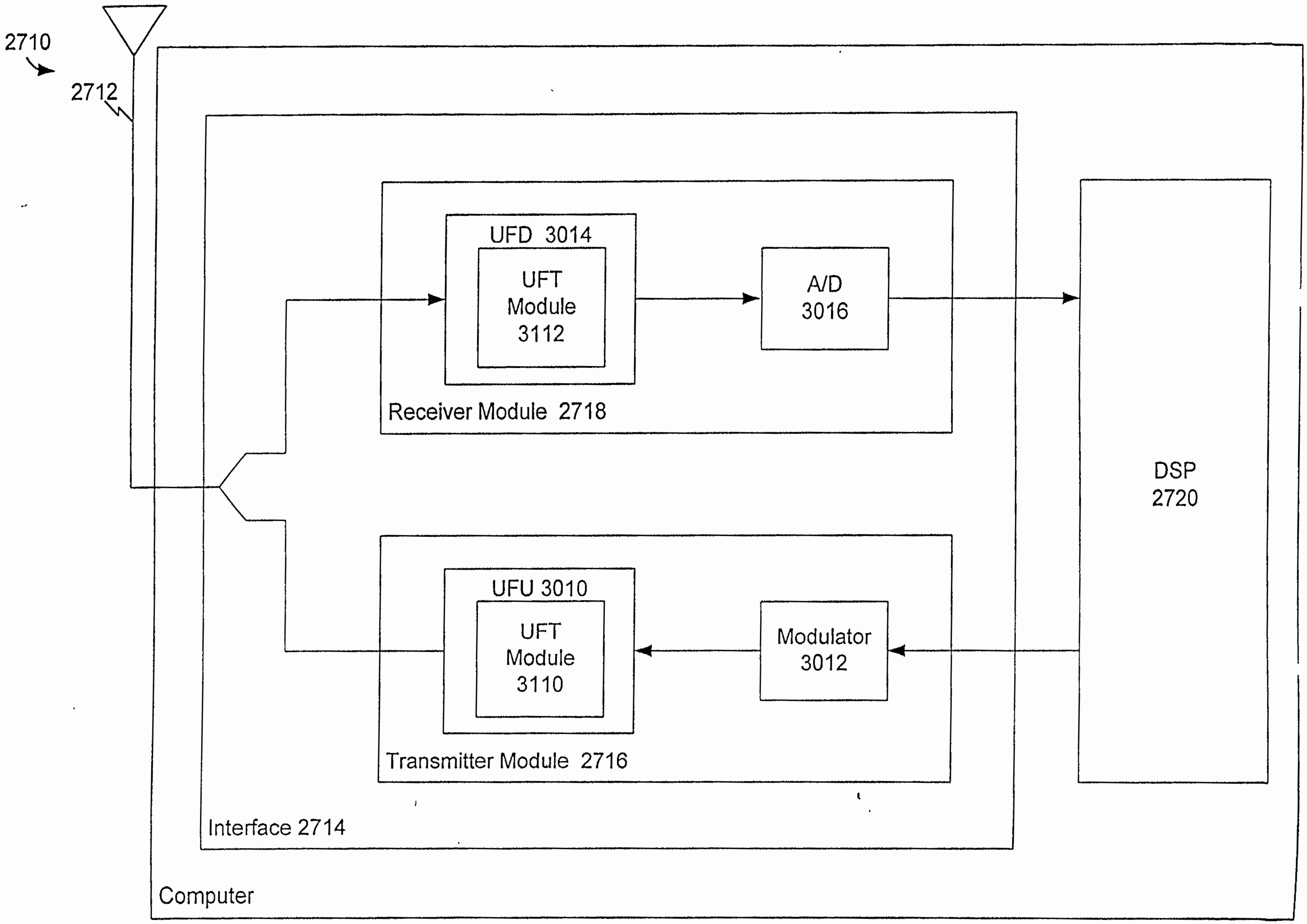

2710
2712
UFD 3014
UFT
Module
3112
A/D
3016
Receiver Module 2718
DSP
2720
UFU 3010
UFT
Module
3110
Modulator
3012
Transmitter Module 2716
Interface 2714
Computer

FIG. 31

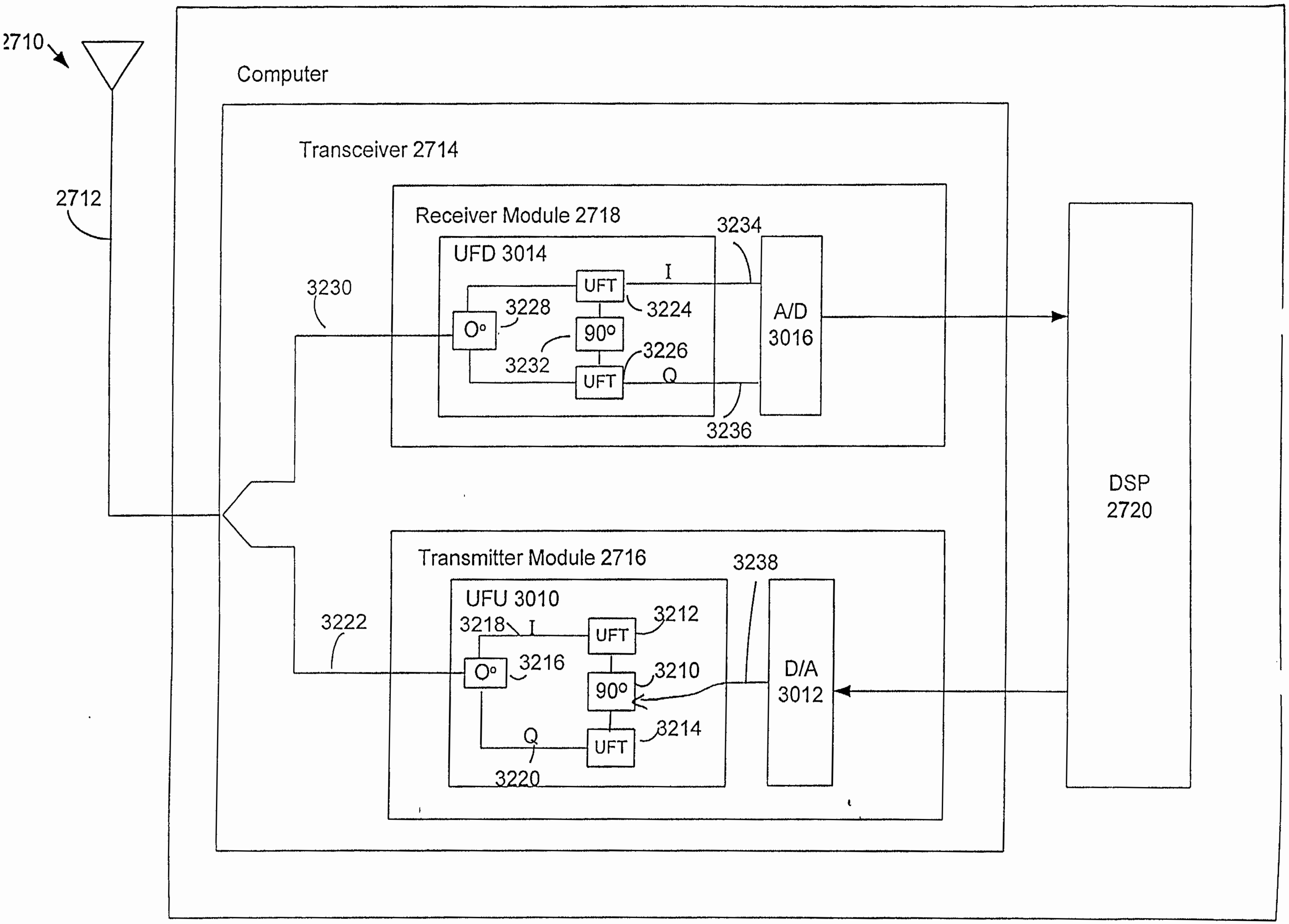


FIG. 32

09632856 .080400

9905-02.vsd/6

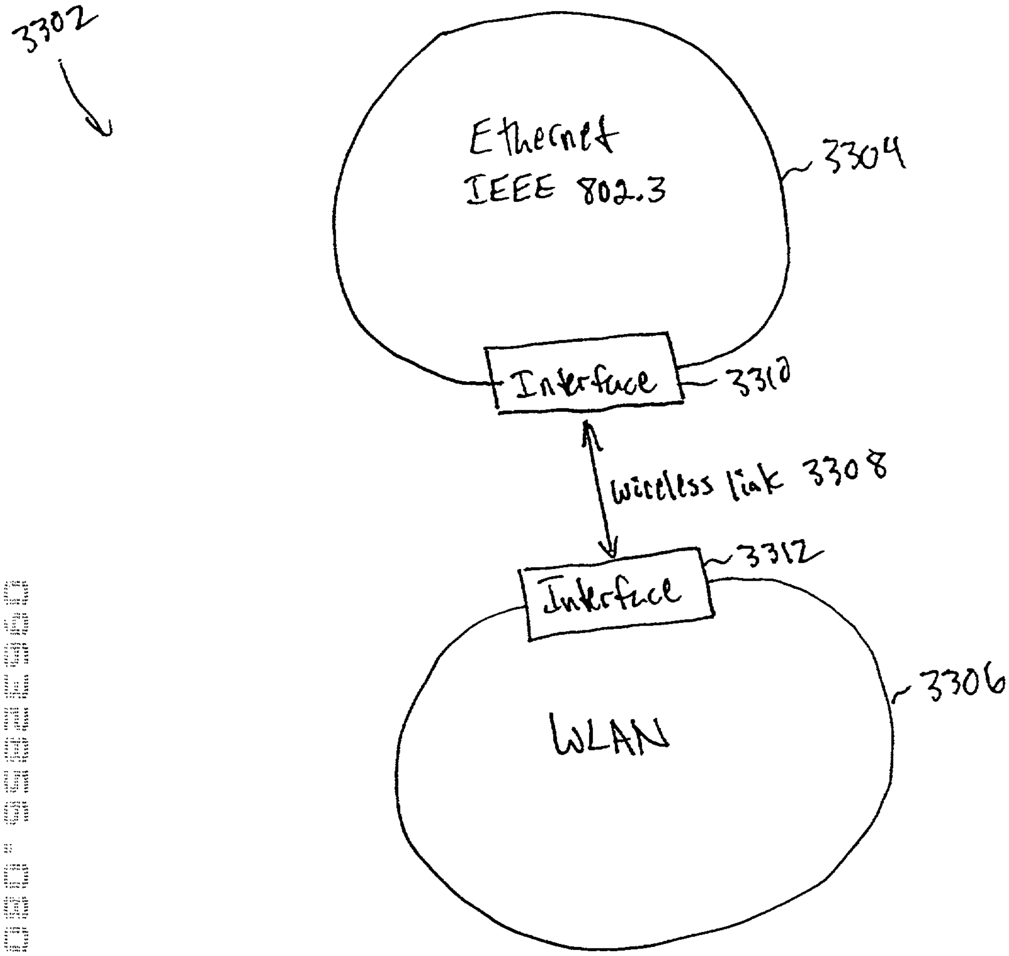

3302
Ethernet
IEEE 802.3
3304
Interface
3310
wireless link 3308
3312
Interface
3306
WLAN

FIG. 33

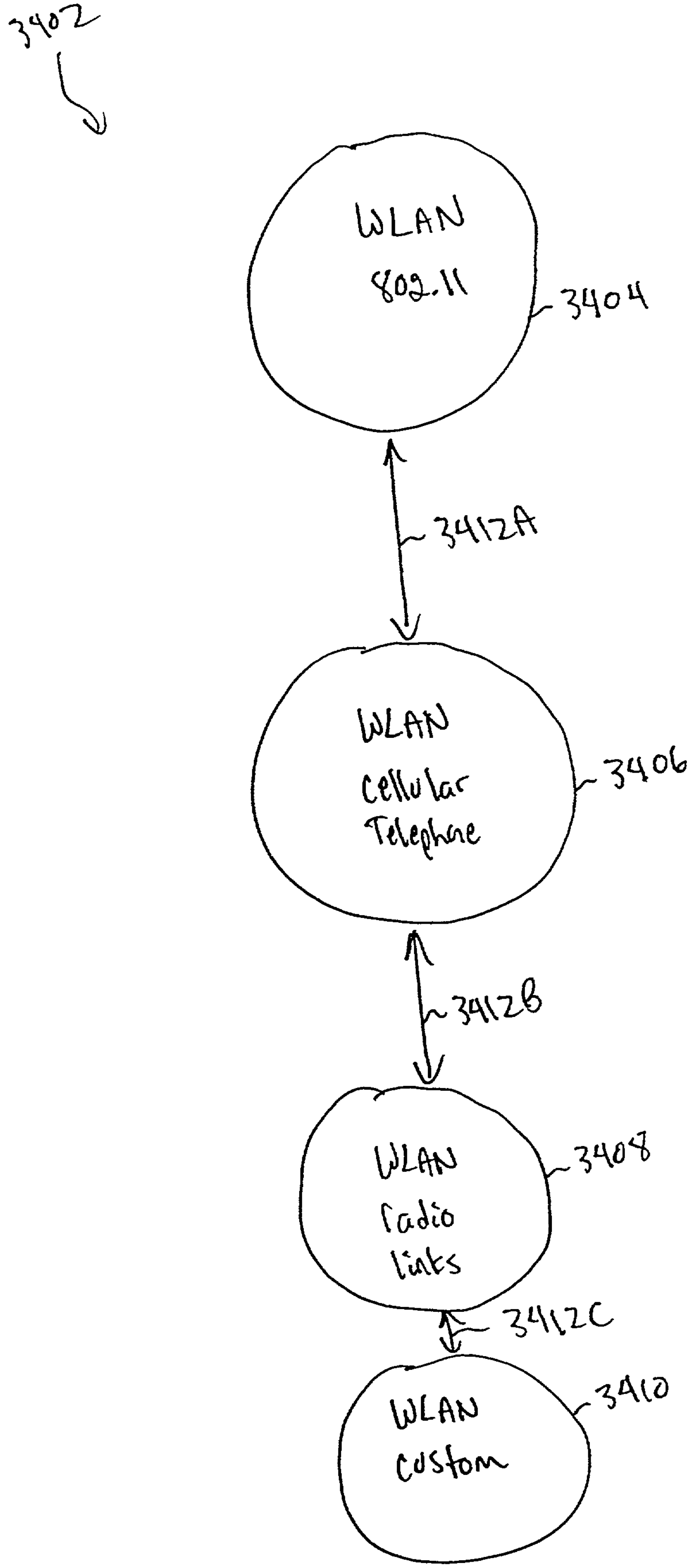

3402
WLAN
802.11
3404
3412A
WLAN
Cellular
Telephone
3406
3412B
WLAN
radio
links
3408
3412C
WLAN
custom
3410

FIG. 34

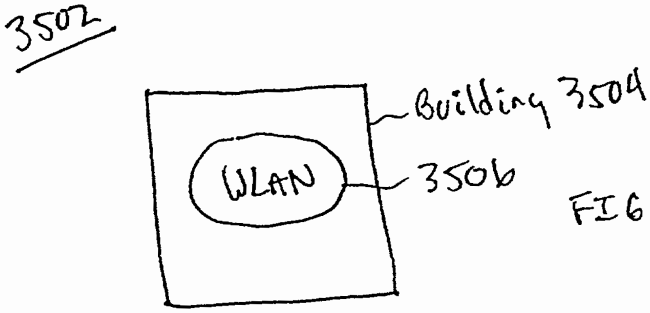

3502
Building 3504
WLAN
3506

FIG. 35

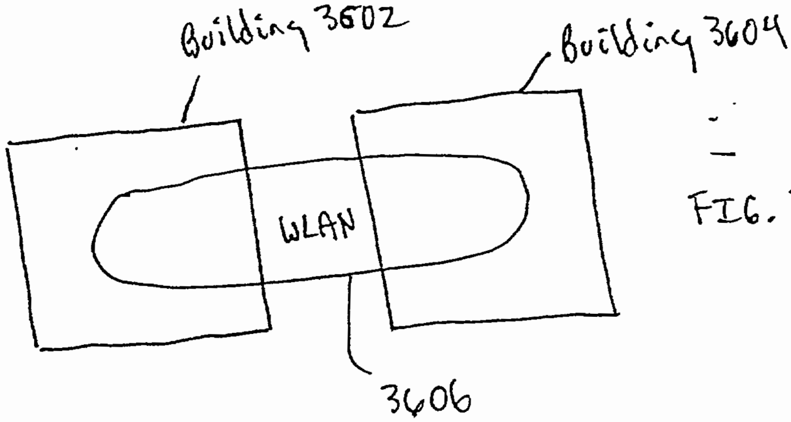

Building 3602
Building 3604
WLAN
3606

FIG. 36

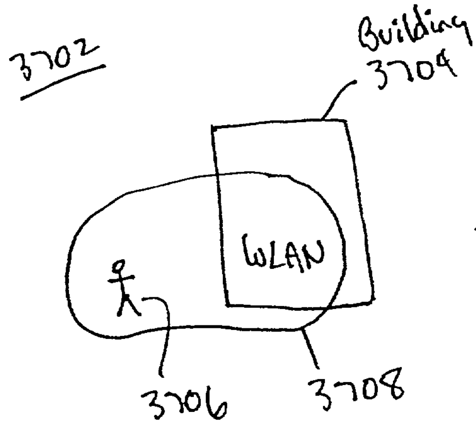

3702
Building
3704
WLAN
3706
3708

FIG. 37


3802
WLAN-specific
geographic area

FIG. 38

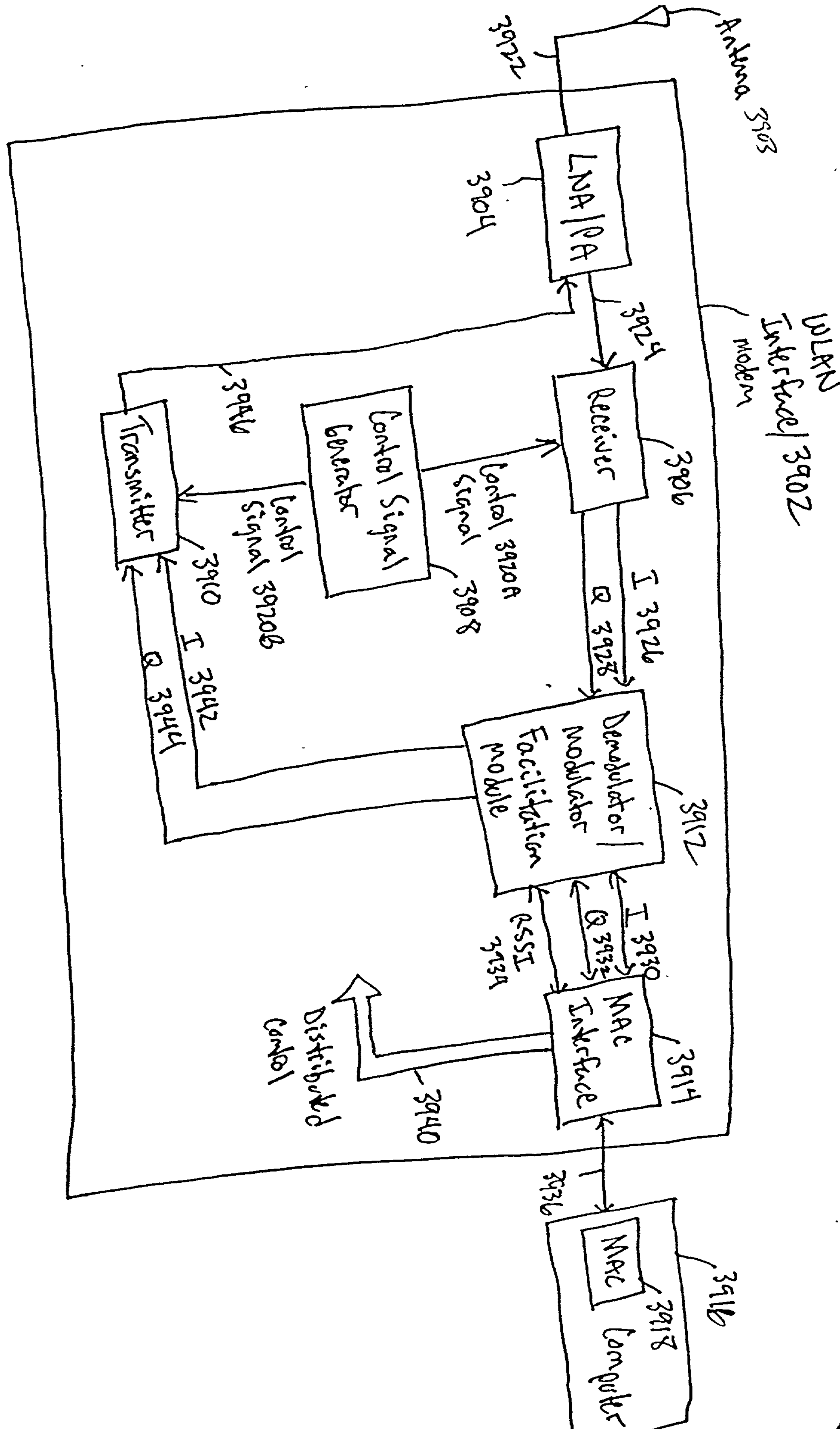

Antenna 3903
3922
WLAN Interface/modem 3902
LNA/PA
3904
3924
Receiver
3906
Control Signal Generator
3908
Control Signal 3920A
Control Signal 3920B
Transmitter
3910
3946
I 3926
Q 3928
Demodulator/Modulator Facilitation module
3912
I 3942
Q 3944
I 3930
Q 3932
RSSI 3934
MAC Interface
3914
Distributed Control
3940
3936
MAC
3918
Computer
3916

FIG. 39

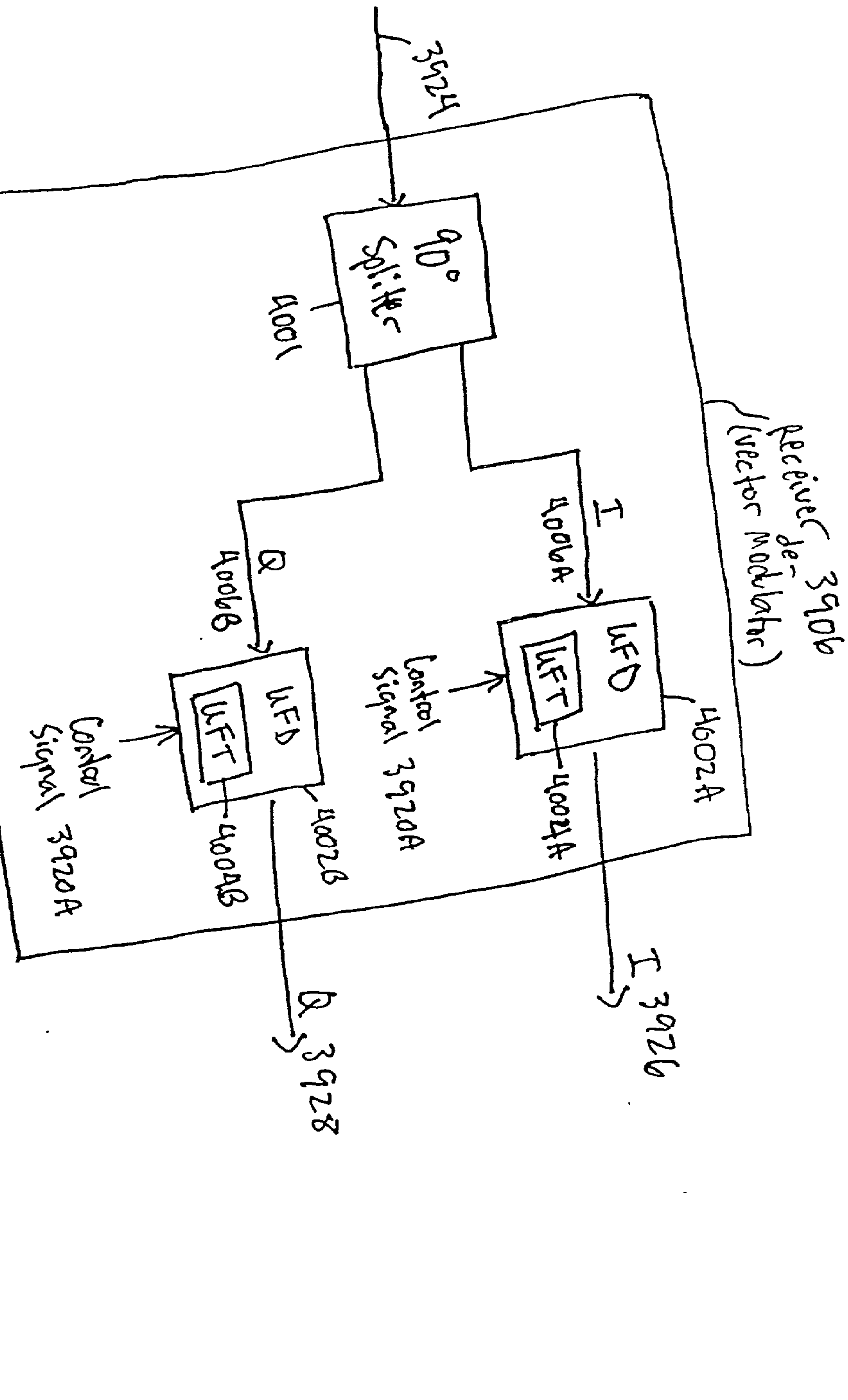

3924
90° Splitter
4001
Receiver 3906 (vector de-modulator)
I
4006A
Q
4006B
UFD
UFT
Control Signal 3920A
4002A
4004A
UFD
UFT
Control Signal 3920A
4002B
4004B
I 3926
Q 3928

FIG. 40

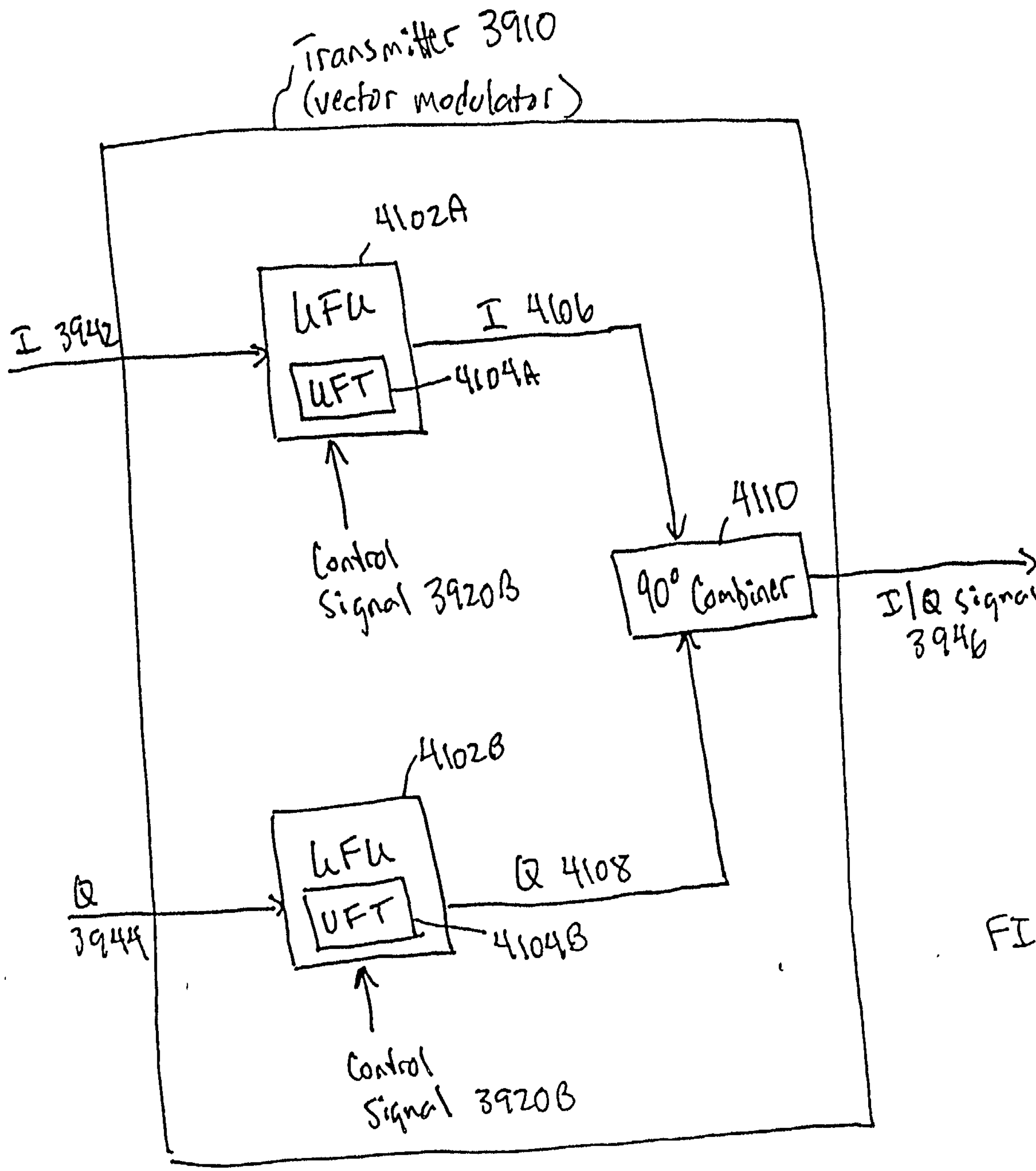
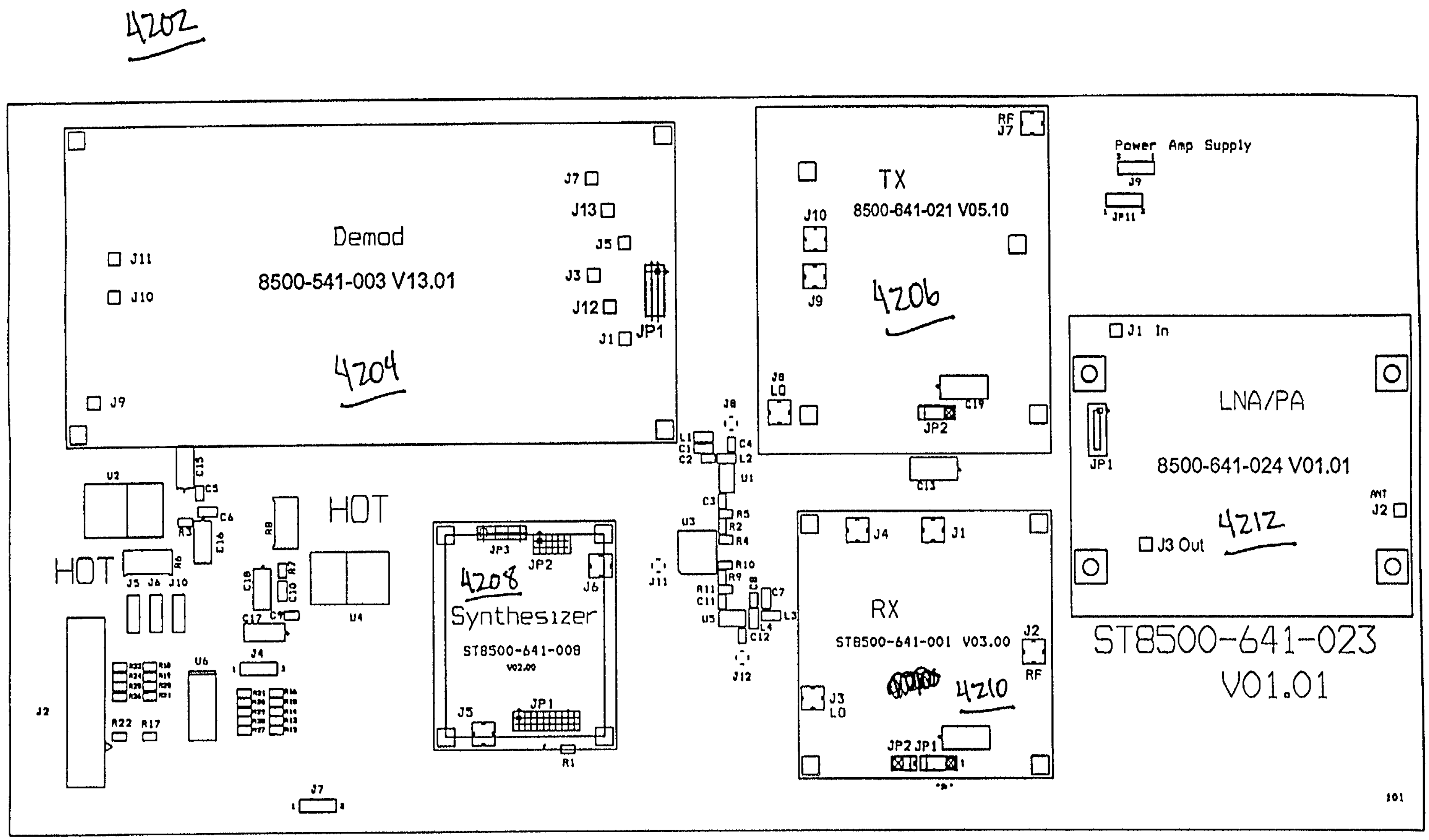

Transmitter 3910
(vector modulator)
4102A
UFU
UFT
4104A
I 3942
I 4106
Control
Signal 3920B
4110
90° Combiner
I/Q Signal
3946
4102B
UFU
UFT
4104B
Q
3944
Q 4108
Control
Signal 3920B

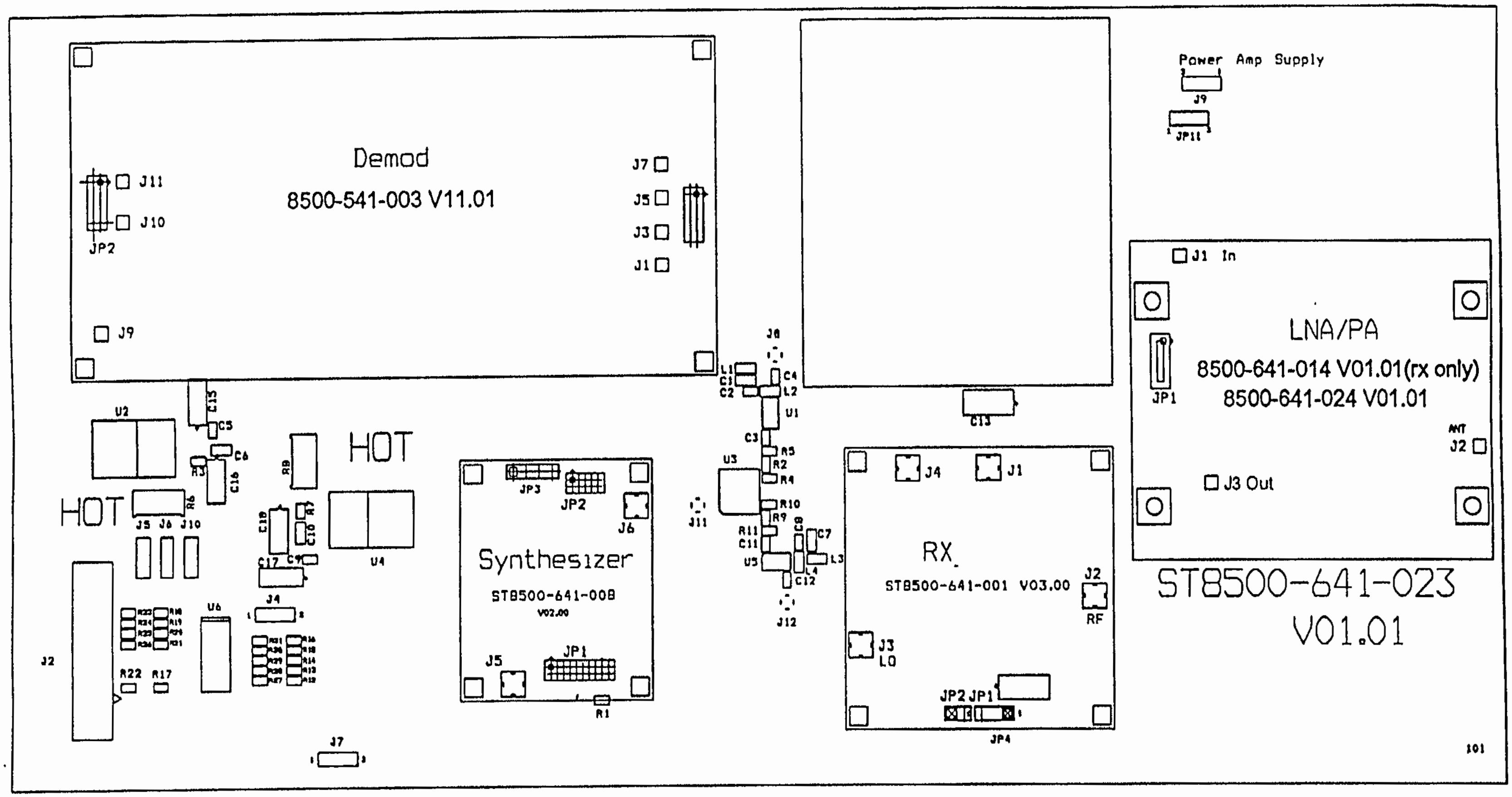
FIG. 41


4202
Demod
8500-541-003 V13.01
4204
TX
8500-641-021 V05.10
4206
Power Amp Supply
LNA/PA
8500-641-024 V01.01
4212
J1 In
J3 Out
HOT
HOT
Synthesizer
ST8500-641-008
4208
RX
ST8500-641-001 V03.00
4210
ST8500-641-023
V01.01

T/R

FIG. 42

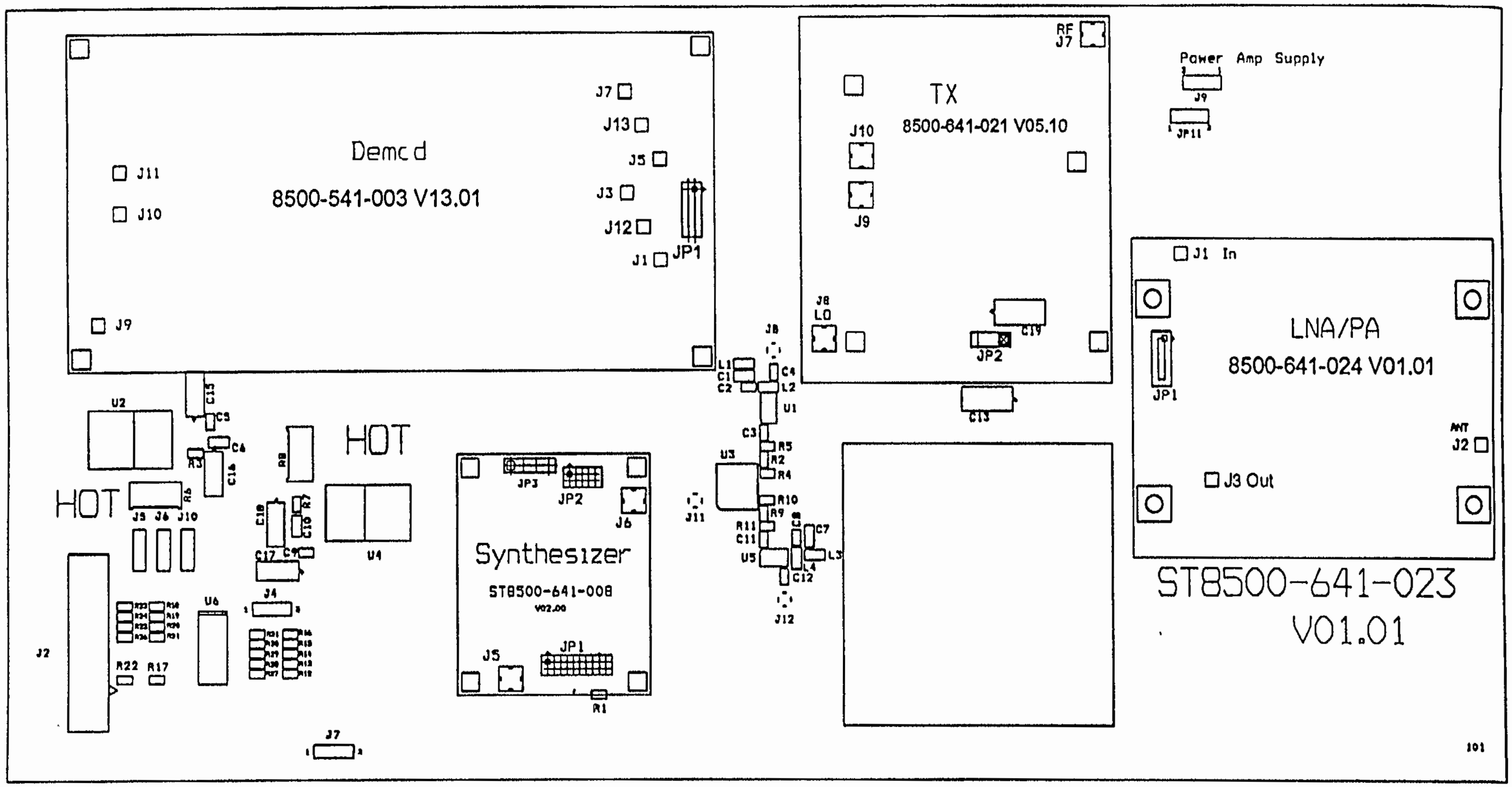
4302



Receive Only

FIG. 43

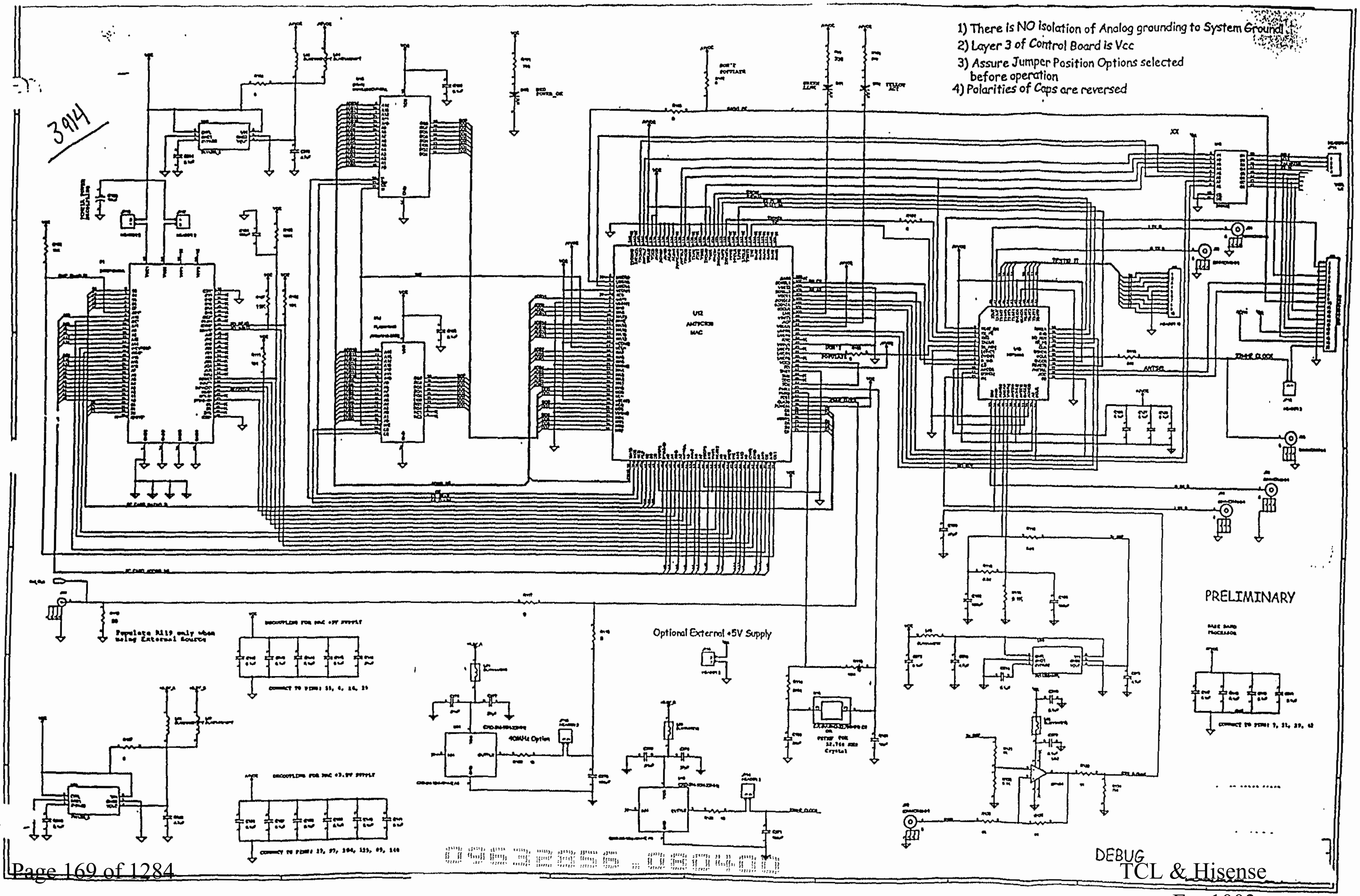
4402



Transmit Only

FIG. 44

FIG. 45


3914
1) There is NO Isolation of Analog grounding to System Ground
2) Layer 3 of Control Board is Vcc
3) Assure Jumper Position Options selected before operation
4) Polarities of Caps are reversed
Optional External +5V Supply
PRELIMINARY
DEBUG

PARK VISION PCMCIA CONTROLLER BOM

Item	Quantity	Reference	Part Description	Part Number	Manufacturer
1	1	C123	10uF CAP 6032, Tantalum,20%	TAJT106K010R	Kemet
2	3	C263, C273, C275, C282	4.7uF CAP 6032,Tantalum,20%	T491A475M006AS	Kemet
3	25	C120, C125, C126, C127, C128, C136, C137, C138, C139, C140, C141, C142, C143, C144, C145, C147, C148, C149, C264, C272, C274, C279, C280, C281, C283	0.1uF CAP 0603,X7R,10%	GRM39X7R104K050AD	Murata
4	3	C146, C269, C276	.01uF CAP 0603,X7R,10%	GRM39X7R103K050AD	Murata
5	5	C124, C132, C133, C271, C278	100pF CAP 0603,X7R,10%	GRM39COG101K050AD	Murata
6	1	C129	47pF CAP 0603,X7R,10%	GRM39COG470J100AD	Murata
7	2	C270, C277	27pF CAP 0603,X7R,10%	GRM39COG270K050AD	Murata
8	1	C130	22pF CAP 0603,X7R,10%	GRM39COG220K050AD	Murata
9	1	C131	10pF CAP 0603,X7R,10%	GRM39COG100D050AD	Murata
10	1	DS1	LED, Green	597-3311-420	Dialight
11	1	DS2	LED Yellow	597-3401-420	Dialight
12	1	DS3	LED Red	597-3111-420	Dialight
13	6	JP12, JP13, JP14, JP15, JP16, JP17	Connector HEADER 2Pin	2MS-19-33-01	Specialty Electronics
14	1	JP11	Connector HEADER 4Pin	100/VH/TM1SQ/W.100/4	BLKCON
15	7	J16, J20, J21, J22, J23, J24, J25	Connector 82MMCX	82MMCX-50-0-1	Huber/Shuner
16	1	J18	Connector Header10	TMS-110-01-G-S	samtec
17	1	J19	Connector with Ejector	EHT-1-10-01-S-D	samtec
18	1	P1	Connector 34X2PCMCIA	DICMJ-68S-SPC-M08	ITT Canon
19	7	L59, L60, L61, L63, L64, L65, L66	Ferrite Bead	BLM11A121S	Murata
20					
21	1	R112	10M, Resistor, 0603, 5%		
22	1	R114	390K, Resistor, 0603, 5%	ERJ-3GSYJ394V	Panasonic
23	1	R105	100K, Resistor, 0603, 5%	ERJ-3GSYJ104V	Panasonic
24	4	R106, R107, R108, R111	15K, Resistor, 0603, 5%	ERJ-3GSYJ153V	Panasonic
25	1	R116	9.1K, Resistor, 0603, 5%	ERJ-3GSYJ912V	Panasonic
26	1	R115	8.2K, Resistor, 0603, 5%	ERJ-3GSYJ822V	Panasonic
27	1	R113	3.9K, Resistor, 0603, 5%	ERJ-3GSYJ392V	Panasonic
28	1	R101	750, Resistor, 0603, 5%	ERJ-3GSYJ751V	Panasonic
29	1	R110	560, Resistor, 0603, 5%	ERJ-3GSYJ561V	Panasonic
30	2	R99, R100	330, Resistor, 0603, [illegible]	ERJ-3GSYJ331V	Panasonic

FIG. 46A

31	1	R119	50 , Resistor, 0603, F	ERJ-3GSYJ500V	Panasonic
32	2	R128, R129	10 , Resistor, 0603, 5	ERJ-3GSYJ100V	Panasonic
33	8	R102, R103, R104, R109, R117, R118, R120, R127	0, Resistor, 0603, 5%	RM732Z1J000ZT ERJ· 3GSYJ000V	KOA Panasonic
34	6	R121, R122, R123, R124, R125, R126	TBD, Resistor, 0603, 5%	R	Panasonic
35	1	U10	SRAM	KM62256DLTG-5L M5M5256CVP-55LL	Samsung Mitsubushi
36	1	U12	MAC	AM79C930	AMD
37	1	U13	Baseband Processor	HFA3842 A1	Harris
38	1	U14	FLASH RAM	AM29F010-55EC	AMD
39	1	U15	32 KHz Crystal	CX-6V-SM2-32.768KHz C/I	Statek
40	2	U45	Bus Buffer	DS3862	National
41	1	U48	Regulator 3.5 V	TK11235BMC	TOKO
42	1	U49	22MHz Oscillator	FOX F3346-22MHz	FOX
43	1	U50	2 Volt Refference	TK11220BMC	TOKO
44	1	U51	40MHz Oscillator	CXO-M-10N-40MHz A/I	Statek

FIG. 46B

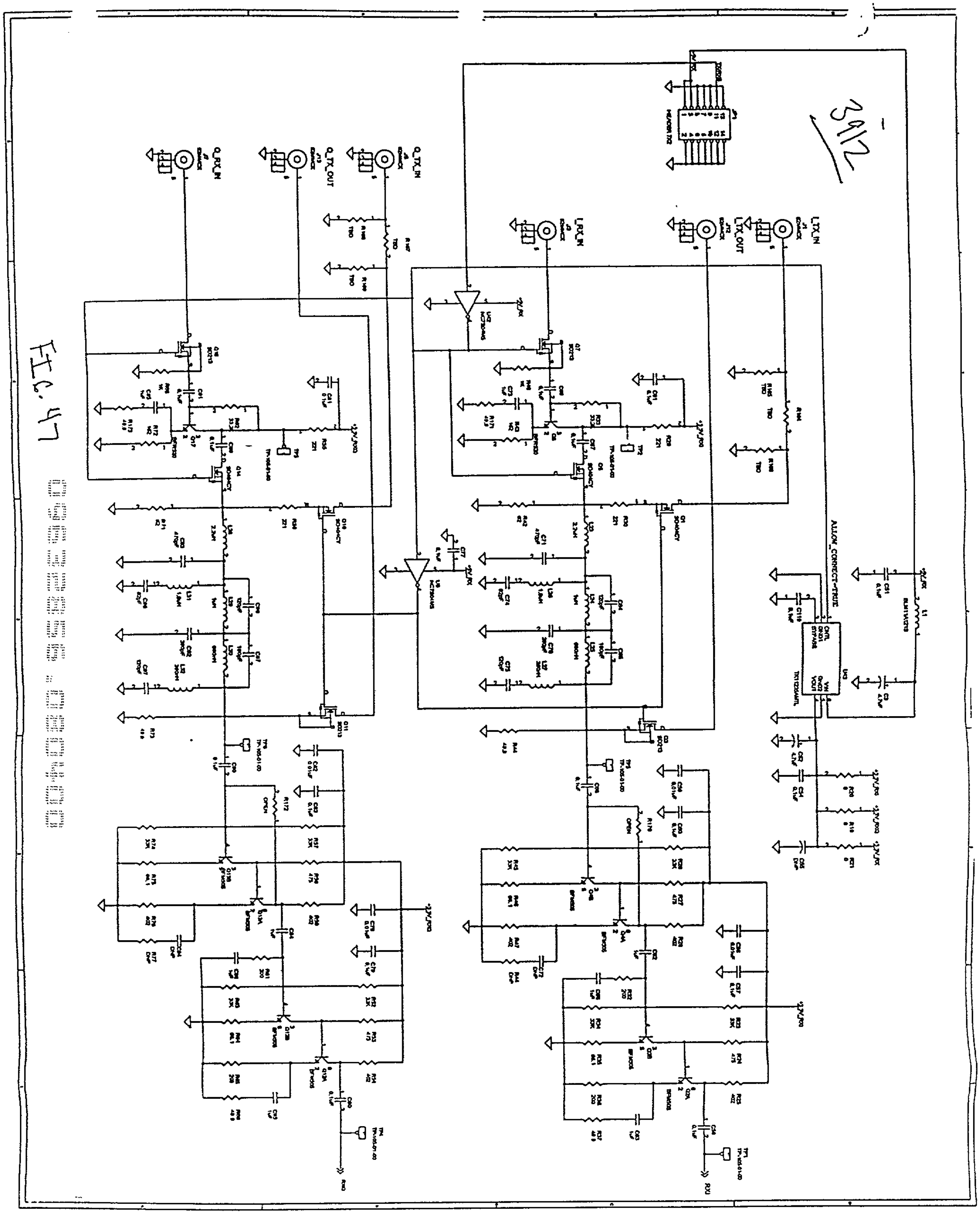


FIG. 47

3912

3912

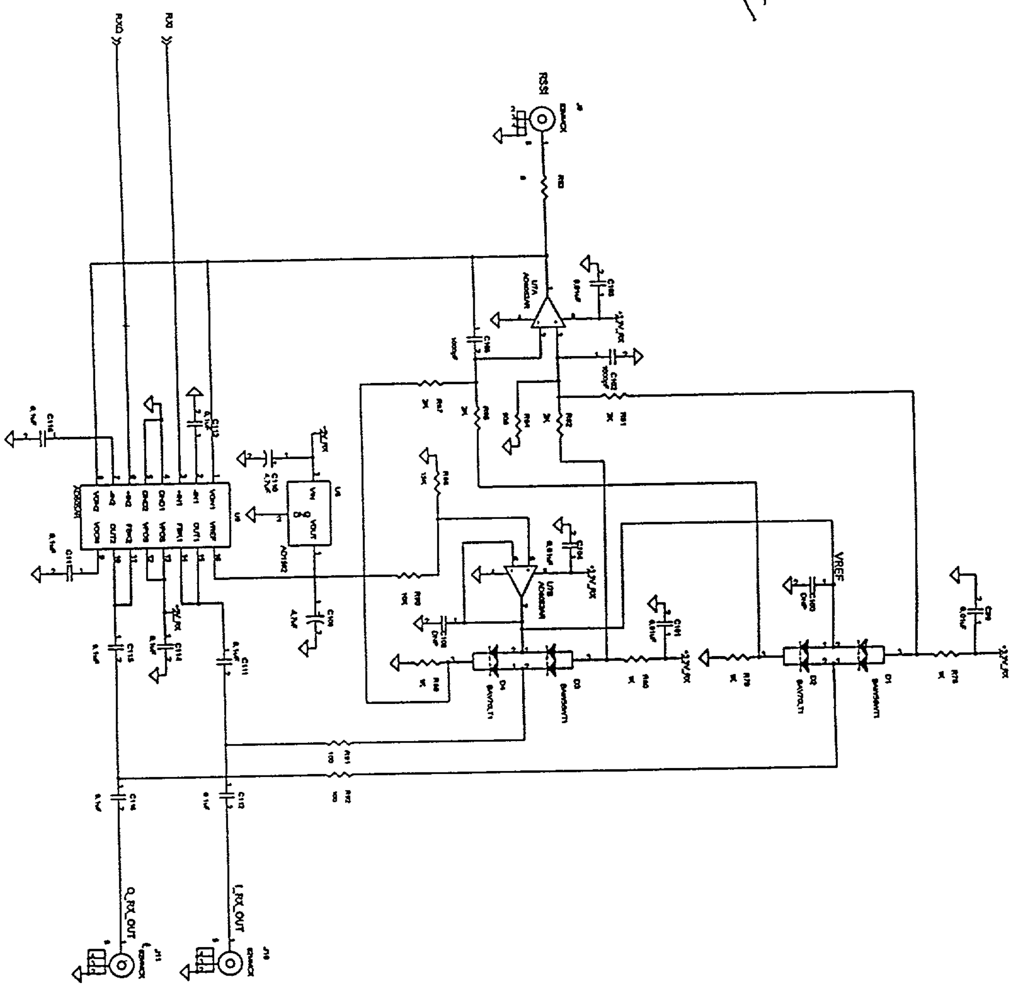


FIG. 48

Item	Quantity	Reference	Part	Part Number	Manufacturer
1	4	C3,C52,C108,C110	4.7uF	T491A475K006AS	KEMET
2	26	C51,C54,C57,C58,C60,C61,	0.1uF	GRM39Y5V104Z016	Murata
		C67,C68,C69,C77,C79,C80,			
		C81,C83,C89,C90,C91,C111,			
		C112,C113,C114,C115,C116,			
		C117,C118,C119			
3	1	C55	DNP	T491A475K006AS	KEMET
4	8	C56,C59,C78,C82,C99,C101,	0.01uF	GRM39X7R103K050	Murata
		C103,C104			
5	8	C62,C63,C66,C73,C84,C85,	1uF	GRM40Y5V105Z016	Murata
		C88,C95			
6	4	C64,C75,C86,C97	120pF	GRM39COG121J050	Murata
7	2	C65,C87	180pF	GRM39COG181J050	Murata
8	2	C70,C92	390pF	GRM39COG391J050	Murata
9	2	C71,C93	470pF	GRM39COG471J050	Murata
10	2	C72,C94	DNP	GRM40Y5V105Z016	Murata
11	2	C74,C96	82pF	GRM39COG820J050	Murata
12	2	C100,C106	DNP	DNP	Murata
13	2	C105,C102	1000pF	GRM39COG102K050	Murata
14	2	D3,D1	BAW56WT1	BAW56WT1	Motorola
15	2	D4,D2	BAV70LT1	BAV70LT1	Motorola
16	1	JP1	HEADER 7X2	FTSH-107-02-L-D	Samtec
17	9	J1,J3,J5,J7,J9,J10,J11,	82MMCX	82MMCX-50-0-1	Suhner
		J12,J13			
18	1	L1	BLM11A121S	BLM11A121S	Murata
19	2	L23,L28	2.2uH	LQG21N2R2K10	Murata
20	2	L29,L24	1uH	LQG21N1R0K10	Murata
21	2	L30,L25	680nH	LQG21NR68K10	Murata
22	2	L26,L31	1.8uH	LQG21N1R8K10	Murata
23	2	L32,L27	390nH	LQG21NR39K10	Murata
24	4	Q1,Q5,Q10,Q14	SD404CY	SD404CY	Calogic
25	4	Q2,Q4,Q12,Q13	BFM505	BFM505	Philips
26	4	Q3,Q7,Q11,Q16	SD213	SD213	Calogic
27	2	Q17,Q8	BFR520	BFR520	Philips
28	4	R19,R20,R21,R83	0	ERJ3GSY0R00	Panasonic
29	8	R23,R26,R34,R45,R52,R57,	33K	ERJ3GSYJ333	Panasonic
		R63,R74			
30	4	R24,R27,R53,R58	475	ERJ3EKF4750	Panasonic
31	6	R25,R28,R47,R54,R59,R76	402	ERJ3EKF4020	Panasonic
32	4	R29,R30,R55,R56	221	ERJ3EKF2210	Panasonic
33	2	R32,R61	200	ERJ3GSYJ201	Panasonic
34	2	R33,R62	33.2K	ERJ3GSYJ333	Panasonic
	4	R35,R46,R64,R75	68.1	ERJ3EKF68R1	Panasonic

FIG. 49A

36	2	R36,R65	200	ERJ3EKF2000	Panasonic
7	6	R37,R44,R66,R73,R171,	49.9	ERJ3EKF49R9	Panasonic
		R173			
38	6	R40,R68,R78,R79,R80,R89	1K	ERJ3EKF1001	Panasonic
39	2	R42,R71	62	ERJ3GSYJ620	Panasonic
40	2	R43,R72	162	ERJ3EKF1620	Panasonic
41	2	R77,R48	DNP	ERJ3GSYJ330	Panasonic
42	4	R81,R82,R85,R87	2K	ERJ3EKF2001	Panasonic
43	1	R84	909	ERJ3EKF9090	Panasonic
44	1	R88	15K	ERJ3EKF1502	Panasonic
45	1	R90	10K	ERJ3EKF1002	Panasonic
46	2	R91,R92	100	ERJ3EKF1000	Panasonic
47	6	R164,R165,R166,R167,R168,	TBD		Panasonic
		R169			
48	2	R170,R172	OPEN		Panasonic
49	6	TP1,TP2,TP3,TP4,TP5,TP6	TP-105-01-00		
50	2	U42,U6	NC7S04M5	NC7S04M5	National Semiconductor
51	1	U7	AD8052AR	AD8052AR	Analog Devices
52	1	U8	AD1582	AD1582	Analog Devices
53	1	U9	AD605AR	AD605AR	Analog Devices
54	1	U43	TK11235AMTL	TK11235BM	Toko
55	1		Board	8500.541.003 V13.01	

FIG. 49B

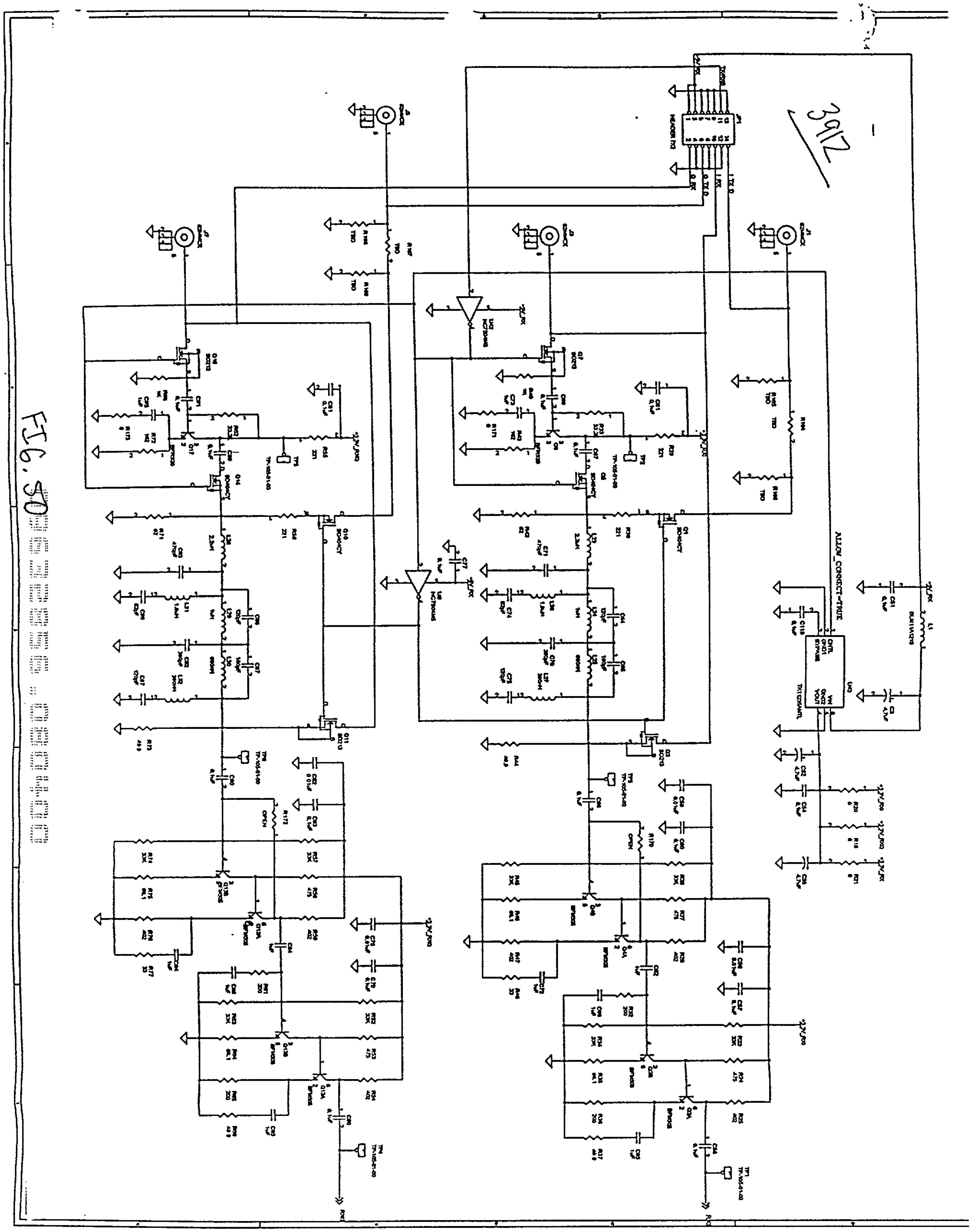


FIG. 50

3912

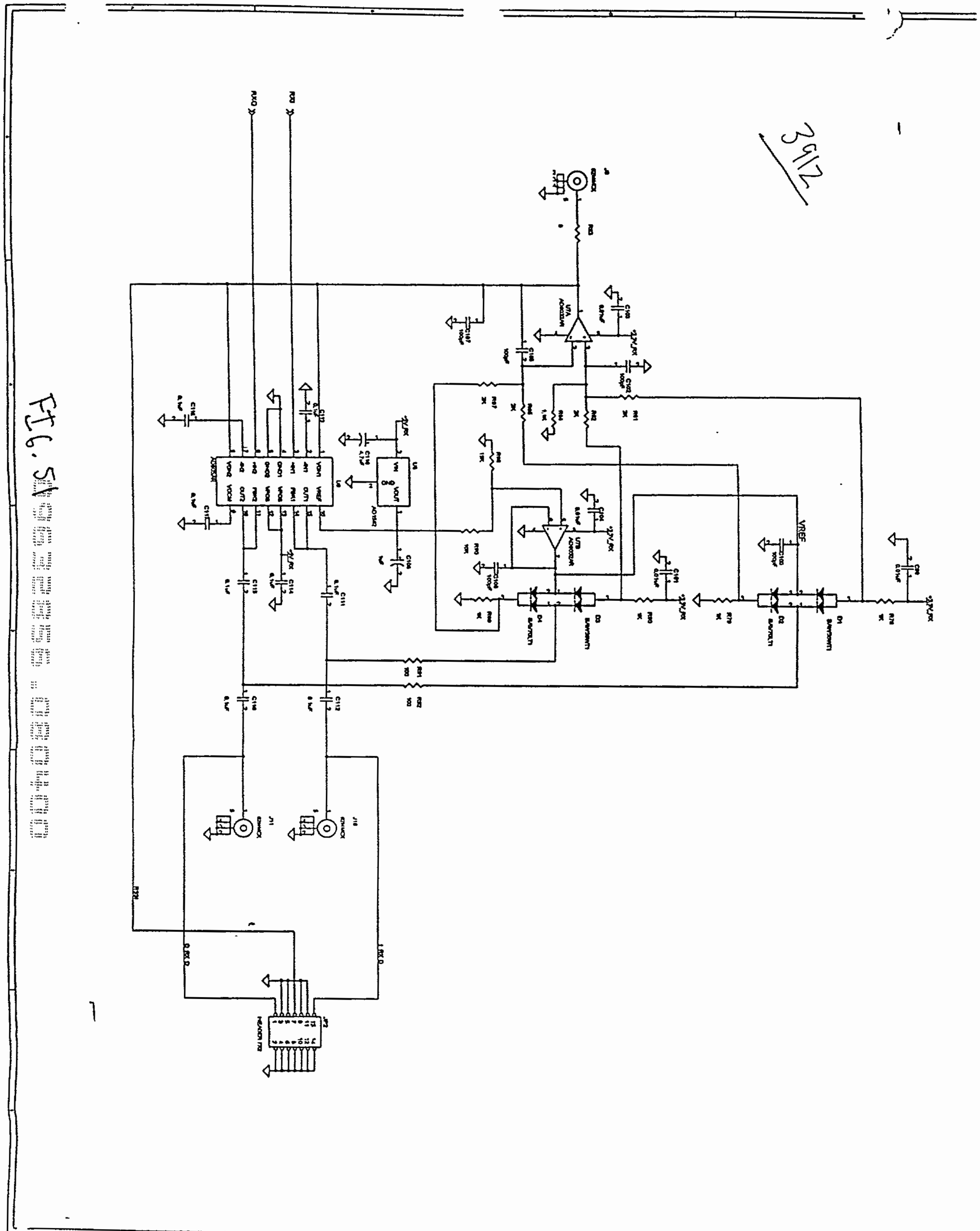


FIG. 5V

3912

Bill Of Materials

Item	Quantity	Reference	Part	Part Number	Manufacturer
1	3	C3,C52,C55	4.7uF	T491A475K006AS	KEMET
2	26	C51,C54,C57,C58,C60,C61,	0.1uF	GRM39Y5V104Z016	Murata
		C67,C68,C69,C77,C79,C80,			
		C81,C83,C89,C90,C91,C111,			
		C112,C113,C114,C115,C116,			
		C117,C118,C119			
3	8	C56,C59,C78,C82,C99,C101,	0.01uF	GRM39X7R103K050	Murata
		C103,C104			
4	10	C62,C63,C66,C72,C73,C84,	1uF	GRM40Y5V105Z016	Murata
		C85,C88,C94,C95			
5	4	C64,C75,C86,C97	120pF	GRM39COG121J050	Murata
6	2	C87,C65	180pF	GRM39COG181J050	Murata
7	2	C70,C92	390pF	GRM39COG391J050	Murata
8	2	C71,C93	470pF	GRM39COG471J050	Murata
9	2	C96,C74	82pF	GRM39COG820J050	Murata
10	5	C100,C102,C105,C106,C107	100pF	GRM39COG101K050	Murata
11	1	C108	1uF		
	1	C110	4.7uF		
13	2	D3,D1	BAW56WT1	BAW56WT1	Motorola
14	2	D4,D2	BAV70LT1	BAV70LT1	Motorola
15	2	JP2,JP1	HEADER 7X2		
16	6	J1,J3,J5,J7,J10,J11	82MMCX	142-0701-231	Johnson
17	1	J9	82MMCX	82MMCX-50-0-1	Suhner
18	1	L1	BLM11A121S	BLM11A121S	Murata
19	2	L28,L23	2.2uH	LQG21N2R2K10	Murata
20	2	L24,L29	1uH	LQG21N1R0K10	Murata
21	2	L30,L25	680nH	LQG21NR68K10	Murata
22	2	L26,L31	1.8uH	LQG21N1R8K10	Murata
23	2	L27,L32	390nH	LQG21NR39K10	Murata
24	4	Q1,Q5,Q10,Q14	SD404CY	SD404CY	Calogic
25	4	Q2,Q4,Q12,Q13	BFM505	BFM505	Philips
26	4	Q3,Q7,Q11,Q16	SD213	SD213	Calogic
27	2	Q17,Q8	BFR520	BFR505	Philips
28	5	R19,R20,R21,R171,R173	0		
29	8	R23,R26,R34,R45,R52,R57,	33K	ERJ3GSYJ333	Panasonic
		R63,R74			
30	4	R24,R27,R53,R58	475	ERJ3EKF4750	Panasonic
31	6	R25,R28,R47,R54,R59,R76	402	ERJ3EKF4020	Panasonic
32	4	R29,R30,R55,R56	221	ERJ3EKF2210	Panasonic
33	2	R32,R61	200	ERJ3GSYJ201	Panasonic
34	2	R33,R62	33.2K	ERJ3GSYJ333	Panasonic
	4	R35,R46,R64,R75	68.1	ERJ3EKF68R1	Panasonic
	2	R36,R65	200	ERJ3EKF2000	Panasonic

FIG. 52A

37	2	R66,R37	49.9	ERJ3EKF49R9	Panasonic
8	6	R40,R68,R78,R79,R80,R89	1K	ERJ3EKF1001	Panasonic
39	2	R42,R71	62	ERJ3GSYJ620	Panasonic
40	2	R43,R72	162	ERJ3EKF6810	Panasonic
41	2	R44,R73	49.9	ERJ3EKF1001	Panasonic
42	2	R77,R48	33	ERJ3GSYJ330	Panasonic
43	4	R81,R82,R85,R87	2K	ERJ3EKF2001	Panasonic
44	1	R83	0	ERJGSY0R00	Panasonic
45	1	R84	1.1K	ERJ3EKF2001	Panasonic
46	1	R88	15K	ERJ3EKF1502	Panasonic
47	1	R90	10K	ERJ3EKF1002	Panasonic
48	2	R91,R92	100	ERJ3EKF1000	Panasonic
49	6	R164,R165,R166,R167,R168,	TBD		
		R169			
50	2	R170,R172	OPEN		
51	6	TP1,TP2,TP3,TP4,TP5,TP6	TP-105-01-00		
52	2	U42,U6	NC7S04M5		National Semiconductor
53	1	U7	AD8032AR	AD8032AR	Analog Devices
54	1	U8	AD1582	AD1582	Analog Devices
55	1	U9	AD605AR	AD605AR	Analog Devices
56	1	U43	TK11235AMTL	TK11235AMTL	Toko

FIG. 52B

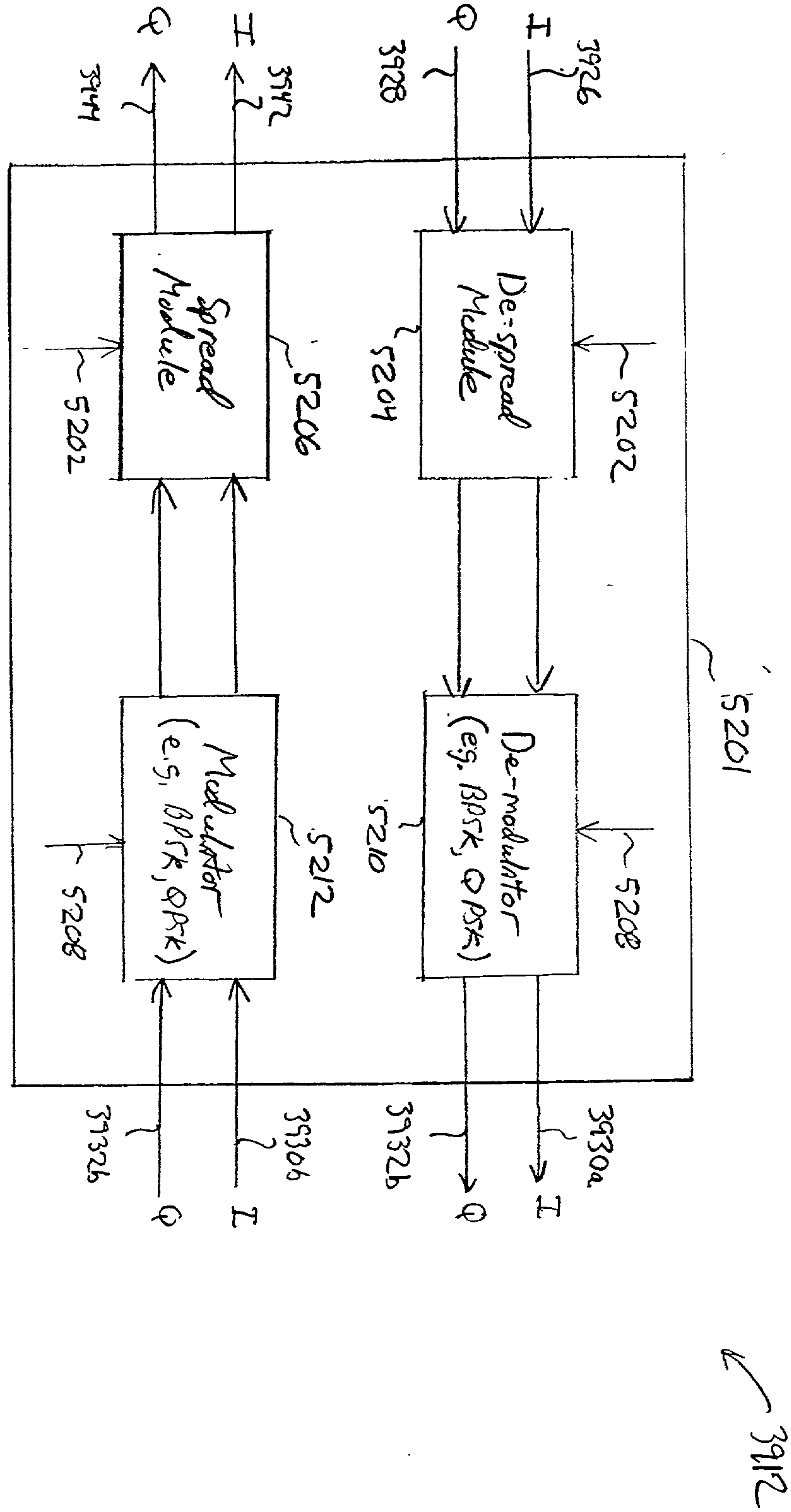
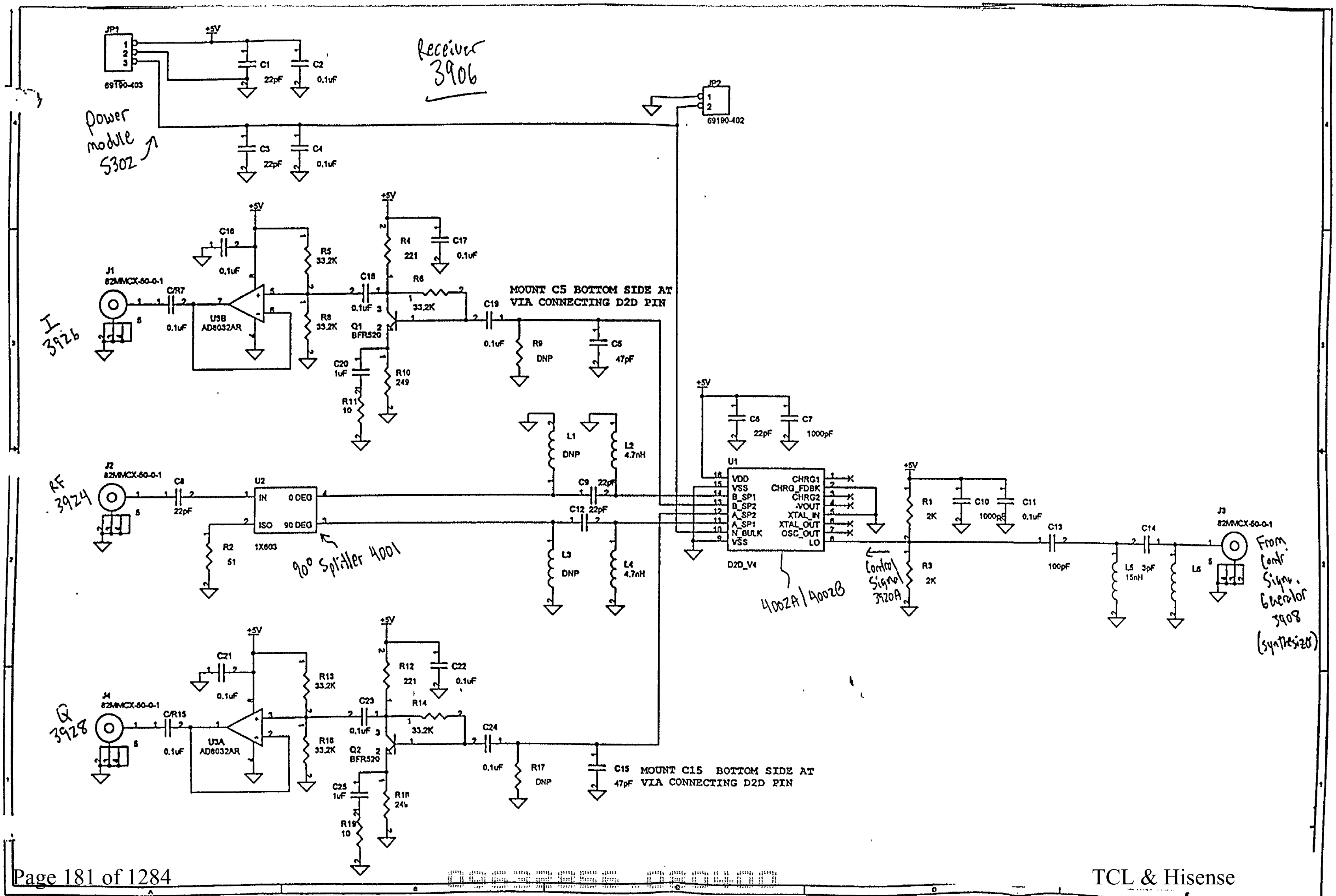

I
Q
3926
3928
De-spread Module
5204
5202
De-modulator (e.g. BPSK, QPSK)
5210
5208
3930a
3932b
I
Q
5201
I
Q
3942
3944
Spread Module
5206
5202
Modulator (e.g. BPSK, QPSK)
5212
5208
3930b
3932b
I
Q
3912

FIG. 52C

FIG. 53


Receiver 3906
Power module 5302
JP1
69190-403
JP2
69190-402
+5V
C1 22pF
C2 0.1uF
C3 22pF
C4 0.1uF
I 3926
J1 82MMCX-50-0-1
C/R7 0.1uF
U3B AD8032AR
C16 0.1uF
R5 33.2K
R8 33.2K
C18 0.1uF
R4 221
C17 0.1uF
R6 33.2K
Q1 BFR520
C20 1uF
R11 10
R10 249
C19 0.1uF
R9 DNP
C5 47pF
MOUNT C5 BOTTOM SIDE AT VIA CONNECTING D2D PIN
RF 3924
J2 82MMCX-50-0-1
C8 22pF
U2
IN
ISO
0 DEG
90 DEG
1X603
R2 51
90° Splitter 4001
L1 DNP
L2 4.7nH
L3 DNP
L4 4.7nH
C9 22pF
C12 22pF
C6 22pF
C7 1000pF
U1
VDD
VSS
B_SP1
B_SP2
A_SP2
A_SP1
N_BULK
VSS
CHRG1
CHRG_FDBK
CHRG2
-VOUT
XTAL_IN
XTAL_OUT
OSC_OUT
LO
D2D_V4
4002A/4002B
Control Signal 3920A
R1 2K
R3 2K
C10 1000pF
C11 0.1uF
C13 100pF
C14 3pF
L5 15nH
L6
J3 82MMCX-50-0-1
From Contr. Signal Generator 3908 (synthesizer)
Q 3928
J4 82MMCX-50-0-1
C/R15 0.1uF
U3A AD8032AR
C21 0.1uF
R13 33.2K
R16 33.2K
C23 0.1uF
R12 221
C22 0.1uF
R14 33.2K
Q2 BFR520
C25 1uF
R19 10
R18 249
C24 0.1uF
R17 DNP
C15 47pF
MOUNT C15 BOTTOM SIDE AT VIA CONNECTING D2D PIN

Page1

Item	Quantity	Reference	Part	Part Number	Manufacturer
1	10	C/R7,C/R15,C16,C17,C18,	0.1uF	GRM39Y5V104Z016	Murata
		C19,C21,C22,C23,C24			
2	6	C1,C3,C6,C8,C9,C12	22pF	GRM39COG220J050	Murata
3	3	C2,C4,C11	0.1uF	GRM39X7R104K016	Murata
4	2	C5,C15	47pF	GRM39COG470J050	Murata
5	2	C10,C7	1000pF	GRM39X7R102K050	Murata
6	1	C13	100pF	GRM39X7R101J050	Murata
7	1	C14	3pF	GRM40COG030B50V	Murata
8	2	C20,C25	1uF	GRM40Y5V105Z016	Murata
9	1	JP1	69190-403	69190-403	BERG
10	1	JP2	69190-402	69190-402	BERG
11	4	J1,J2,J3,J4	82MMCX-50-0-1	82MMCX-50-0-1	Suhner
12	2	L3,L1	DNP	L	TOKO
13	2	L4,L2	4.7nH	LL1608-F4N7K	TOKO
14	1	L5	15nH	LL2012FH15NJ	TOKO
15	1	L6	DNP	DNP	TOKO
16	2	Q1,Q2	BFR520	BFR520	Philips
17	2	R1,R3	2K	ERJ3GSYJ202	Panasonic
18	1	R2	51	ERJ3GSYJ510	Panasonic
19	2	R4,R12	221	ERJ3EKF2210	Panasonic
20	6	R5,R6,R8,R13,R14,R16	33.2K	ERJ3EKF3322	Panasonic
21	2	R9,R17	DNP	ERJ3EKF1001	Panasonic
22	2	R10,R18	249	ERJ3EKF2490	Panasonic
23	2	R11,R19	10	ERJ3GSYJ100	Panasonic
24	1	U1	D2D_V4	D2D_V4	Parker Vision
25	1	U2	1X603	1X603	Anaren
26	1	U3	AD8032AR	AD8032AR	Analog Devices
27	1		BOARD	ST8500.LA1.001	V03.00

FIG. 54

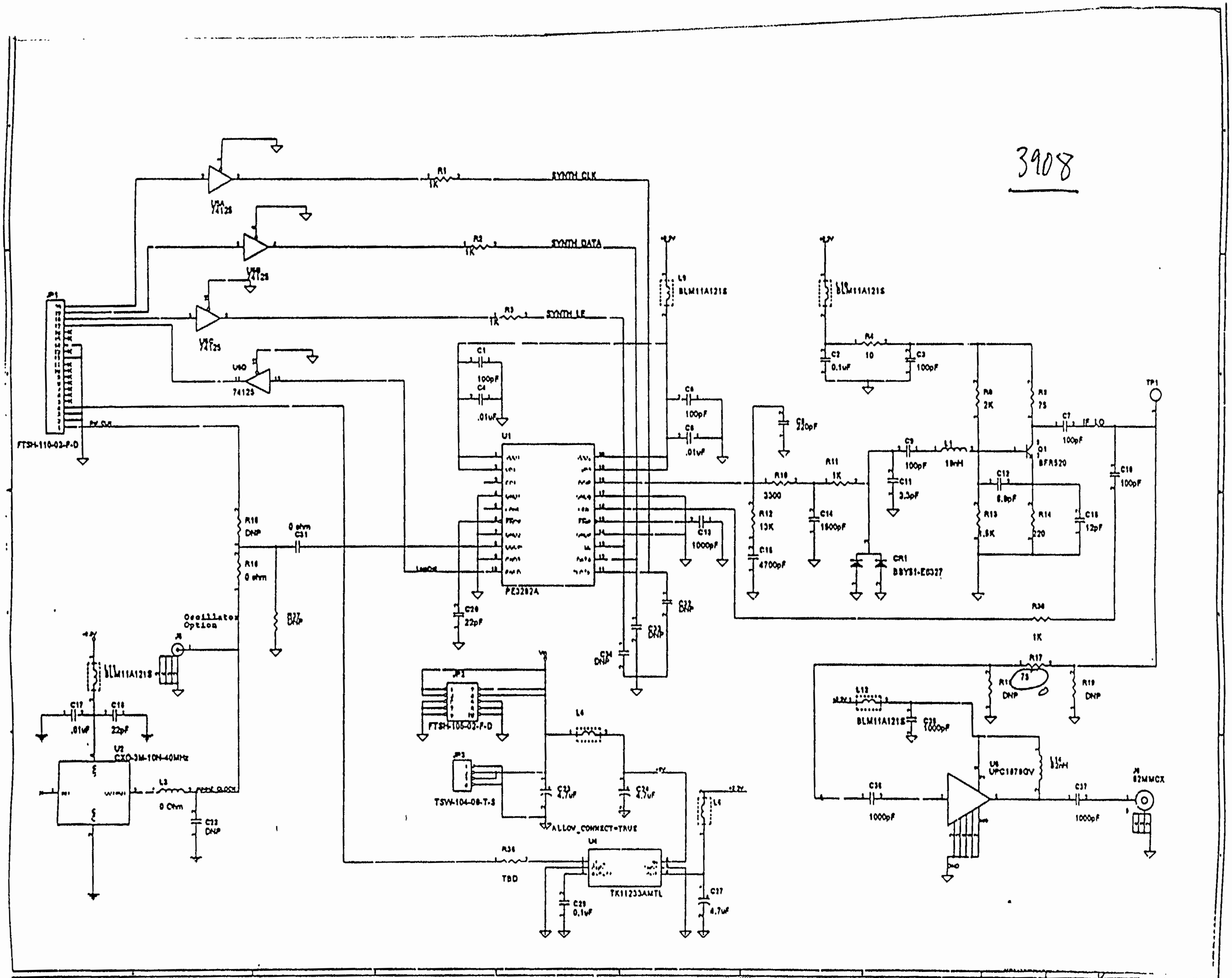

3908
SYNTH CLK
SYNTH DATA
SYNTH LE
74125
FTSH-110-02-F-D
PE3282A
BLM11A121S
BFR520
BBY51-E6327
IF LO
Oscillator Option
CXO-3M-10N-40MHz
FTSH-105-02-F-D
TSW-104-08-T-S
ALLOW_CONNECT=TRUE
TK11233AMTL
UPC1678GV
82MMCX

FIG. 55

Item	Qty	Reference	Part	Description	Part Number	Manufacturer
1	1	CR1	BBY51-E6327	Diode, Varactor	BBY51-E6327	Siemens
2	6	C1,C3,C5,C7,C9,C10	100pF	Capacitor, ceramic, 100pF, 10%, COG, 0603	GRM39COG101K050	Murata
3	2	C29,C2	0.1uF	Capacitor, ceramic, .1uF, 10%, X7R, 0603	GRM39X7R104K016AD	Murata
4	3	C4,C8,C17	.01uF	Capacitor, ceramic, .01uF, 10%, X7R, 0603	GRM39X7R103K050	Murata
5	1	C6	220pF	Capacitor, ceramic, 220pF, 5%, COG, 0603	GRM39COG221J025	Murata
6	1	C11	3.3pF	Capacitor, ceramic, 3.3pF, 5% , COG, 0603	GRM39COG3R3B100V	Murata
7	1	C12	6.8pF	Capacitor, ceramic, 6.8pF, +/-.25pF, COG, 0603	GRM39COG6R8C100V	Murata
8	4	C13,C35,C36,C37	1000pF	Capacitor, ceramic, 1000pF, 10%, X7R, 0603	GRM39X7R102K016	Murata
9	1	C14	1500pF	Capacitor, ceramic, 1500pF, 10%, X7R, 0603	GRM39X7R152K016	Murata
10	1	C15	12pF	Capacitor, ceramic, 12pF, 5%, COG, 0603	GRM39COG150J050	Murata 12pF
11	1	C16	4700pF	Capacitor, ceramic, 4700pF, 10%, 0603	GRM39X7R472K016	Murata
12	2	C20,C18	22pF	Capacitor, ceramic, 22pF, 10%, COG, 0603	GRM36COG220K050	Murata
13	4	C22,C32,C33,C34	DNP	Capacitor, ceramic, , , , 0603		Murata
14	3	C23,C24,C27	4.7uF	Capacitor, tantalum, 4.7uF, 10%, 3216	T491A475K006AS	Kemet
15	~~2~~ 3	R16,C31, R17	0 ohm	Resistor, zero ohm, 0603	ERJ3GSY0R00	Panasonic
16	1	JP1	FTSH-110-02-F-D	Header, dual row 10x2, .050x.050	FTSH-110-02-F-D	Samtec
17	1	JP2	FTSH-105-02-F-D	Header, dual row 5x2, .050x.050	FTSH-105-02-F-D	Samtec
18	1	JP3	TSW-104-08-T-S	Header, single row 4 pin, .100"	TSW-104-08-T-S	Berg
19	2	J5,J6	82MMCX	RF Connector	82MMCX-50-0-1	Suhner
20	1	L1	18nH	Inductor, 18nH, 10%, 0805	0805CS-180XJBC	Coilcraft
21	1	L3	0 Ohm	Zero Ohm Jumper	RM73ZIJT	KOA
22	6	L4,L6,L9,L10,L11,L12	BLM11A121S	Ferrite Bead, 0603	BLM11A121S	Murata
23	1	L14	82nH	Inductor, 82nH, 10%, 0805	LL2012-F82NK	Toko
24	1	Q1	BFR520	Transistor, NPN	BFR520	Philips
25	5	R1,R2,R3,R11,R30	1K	Resistor, 1K, 5%, 0603	ERJ3GSYJ102	Panasonic
26	1	R4	10	Resistor, 10 ohm, 5%, 0603	ERJ3GSYJ1R0	Panasonic
27	1	R8	2K	Resistor, 2K, 5%, 0603	ERJ3GSYJ202	Panasonic
28	~~2~~ 1	R9,~~R17~~	75	Resistor, 75 ohm, 5%, 0603	ERJ3GSYJ750	Panasonic
29	1	R10	3300	Resistor, 3.3K, 5%, 0603	ERJ3GSYJ332	Panasonic
30	1	R12	13K	Resistor, 13K, 5%, 0603	ERJ3GSYJ133	Panasonic
31	1	R13	1.5K	Resistor, 1.5K, 5%, 0603	ERJ3GSYJ152	Panasonic

FIG. 56A

32	1	R14	220	Resistor, 220 ohm, 5%, 0603	ERJ3GSYJ221	Panasonic
33	1	R15	DNP	Resistor, zero ohm, 0603	ERJ3GSY0R00	Panasonic
34	2	R18,R19	DNP	Resistor, 91 ohm, 5%, 0603	ERJ3GSYJ910	Panasonic
35	1	R36	TBD	Resistor, zero ohm, 0603	ERJ3GSY0R00	Panasonic
36	1	R37	DNP	Resistor, , , 0603		Panasonic
37	1	TP1	Test Point			
38	1	U1	PE3282A	IC, Synthesizer	PE3282A	Peregrine
39	1	U2	CXO-3M-10N-40MHz	Xtal Osc, 40MHz	CXO-3M-10N-40MHZ A/I	Statek
40	1	U4	TK11233AMTL	Voltage Regulator, 3.5V	TK11235BM	Toko
41	1	U5	74125	IC, BUFFER	MC74LCX125DT	Motorola
42	1	U6	UPC1678GV	IC, RF Amplifier	UPC1678GV	NEC
43	1		STB500.641.00B V02.00	BOARD		

FIG. 56B

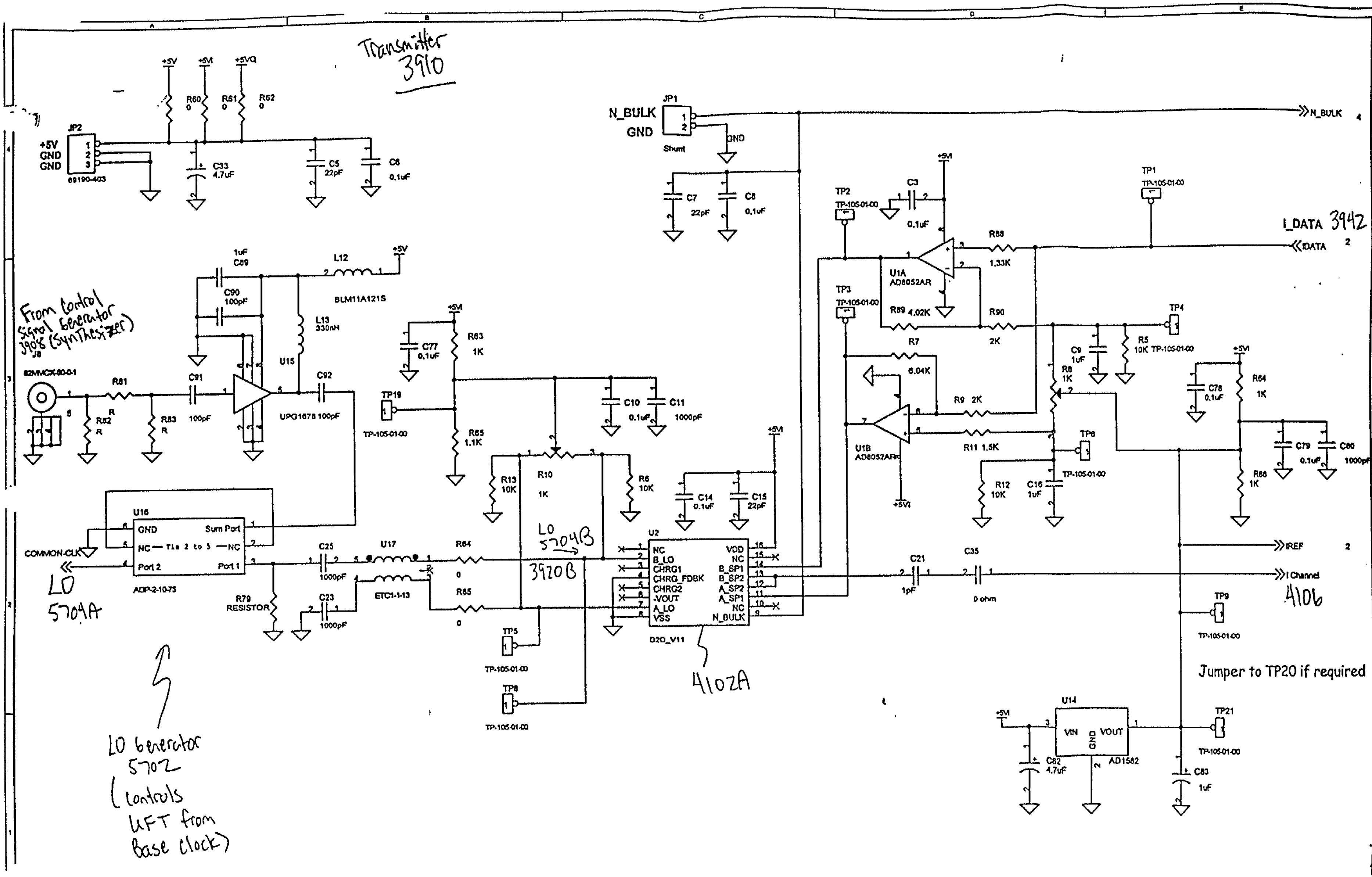

Transmitter
3910
From Control Signal Generator 3908 (Synthesizer)
LO
5704A
LO Generator
5702
(Controls LFT from Base clock)
LO
5704B
3920B
4102A
I_DATA 3942
4106
Jumper to TP20 if required
JP2
+5V
GND
GND
69190-403
+5V
+5VI
+5VQ
R60
R61
R62
C33
4.7uF
C5
22pF
C6
0.1uF
N_BULK
GND
JP1
Shunt
C7
22pF
C8
0.1uF
N_BULK
IDATA
IREF
I Channel
J8
R81
R82
R83
C91
100pF
U15
UPG1678
C92
100pF
C89
1uF
C90
100pF
L12
BLM11A121S
L13
330nH
C77
0.1uF
R63
1K
R65
1.1K
TP19
TP-105-01-00
C10
0.1uF
C11
1000pF
R13
10K
R10
1K
R6
10K
U16
GND
Sum Port
NC
NC
Port 2
Port 1
ADP-2-10-75
COMMON-CLK
C25
1000pF
C23
1000pF
U17
ETC1-1-13
R64
R85
R79
RESISTOR
TP5
TP8
U2
NC
B_LO
CHRG1
CHRG_FDBK
CHRG2
-VOUT
A_LO
VSS
VDD
B_SP1
B_SP2
A_SP2
A_SP1
N_BULK
D2D_V11
C14
0.1uF
C15
22pF
C21
1pF
C35
0 ohm
TP2
TP3
C3
0.1uF
U1A
AD8052AR
R88
1.33K
R89
4.02K
R90
2K
TP1
TP4
R7
6.04K
U1B
AD8052AR
R9 2K
R11 1.5K
R8
1K
C9
1uF
R5
10K
TP6
R12
10K
C16
1uF
C78
0.1uF
R84
1K
R86
1K
C79
0.1uF
C80
1000pF
TP9
TP21
U14
VIN
GND
VOUT
AD1582
C82
4.7uF
C83
1uF

FIG. 57

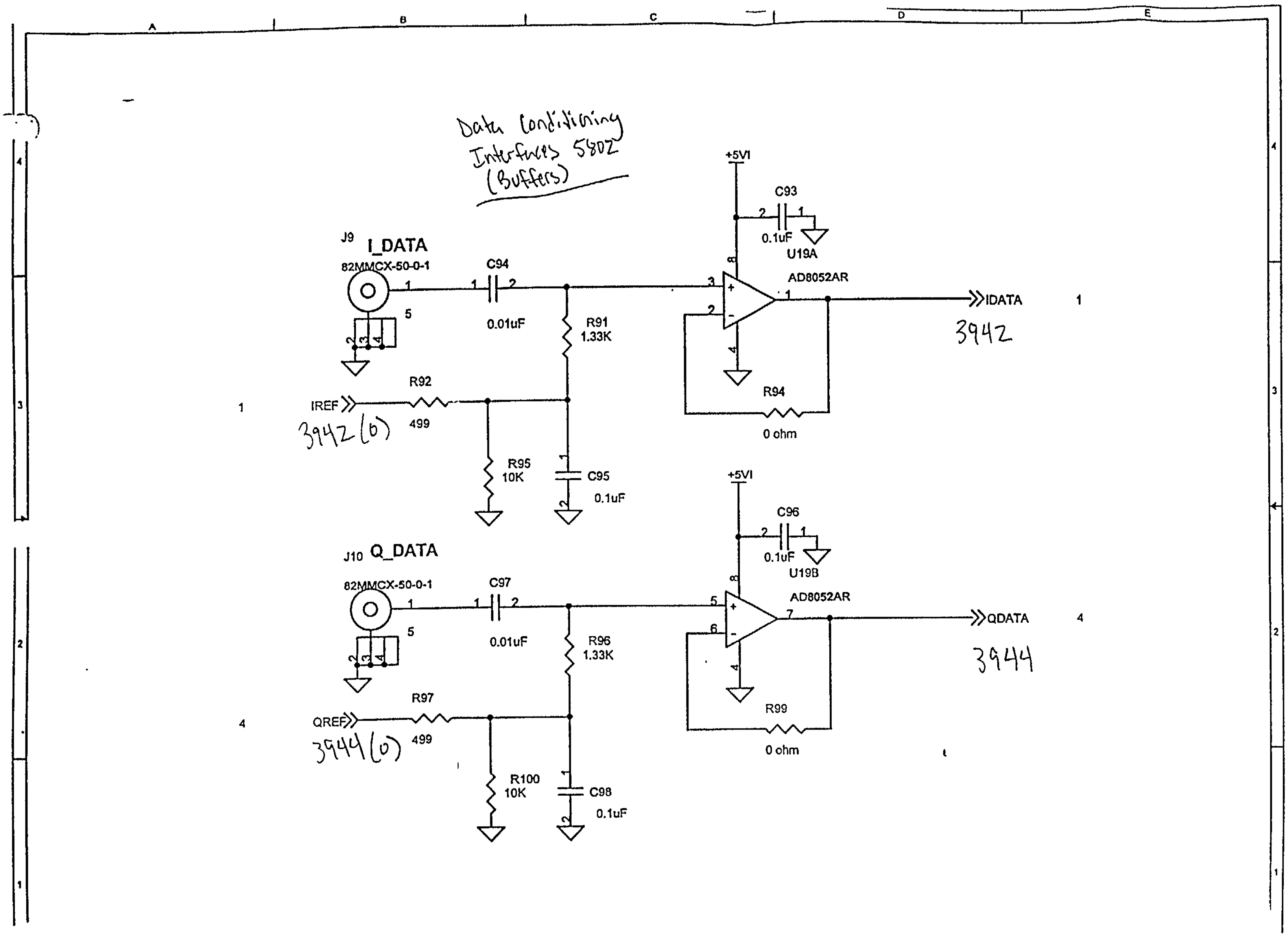

Data Conditioning Interfaces 5802 (Buffers)
J9 I_DATA
82MMCX-50-0-1
C94
0.01uF
R91
1.33K
IREF
3942(0)
R92
499
R95
10K
C95
0.1uF
+5VI
C93
0.1uF
U19A
AD8052AR
R94
0 ohm
IDATA
3942
J10 Q_DATA
82MMCX-50-0-1
C97
0.01uF
R96
1.33K
QREF
3944(0)
R97
499
R100
10K
C98
0.1uF
+5VI
C96
0.1uF
U19B
AD8052AR
R99
0 ohm
QDATA
3944

FIG. 58

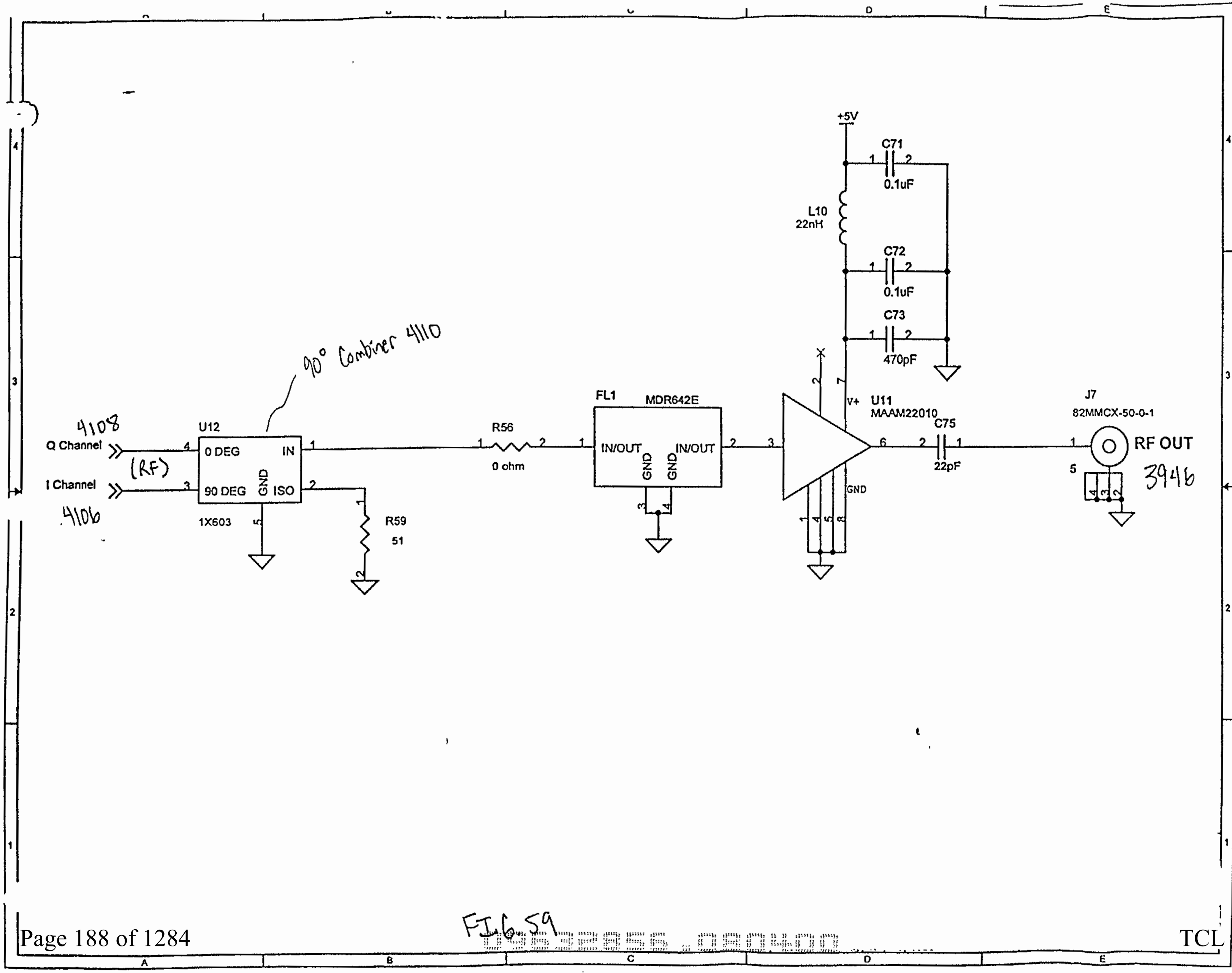

90° Combiner 4110
4108
Q Channel
(RF)
I Channel
4106
U12
0 DEG
IN
90 DEG
GND
ISO
1X603
R56
0 ohm
R59
51
FL1
MDR642E
IN/OUT
GND
GND
IN/OUT
+5V
C71
0.1uF
L10
22nH
C72
0.1uF
C73
470pF
V+
U11
MAAM22010
GND
C75
22pF
J7
82MMCX-50-0-1
RF OUT
3946

FIG.59

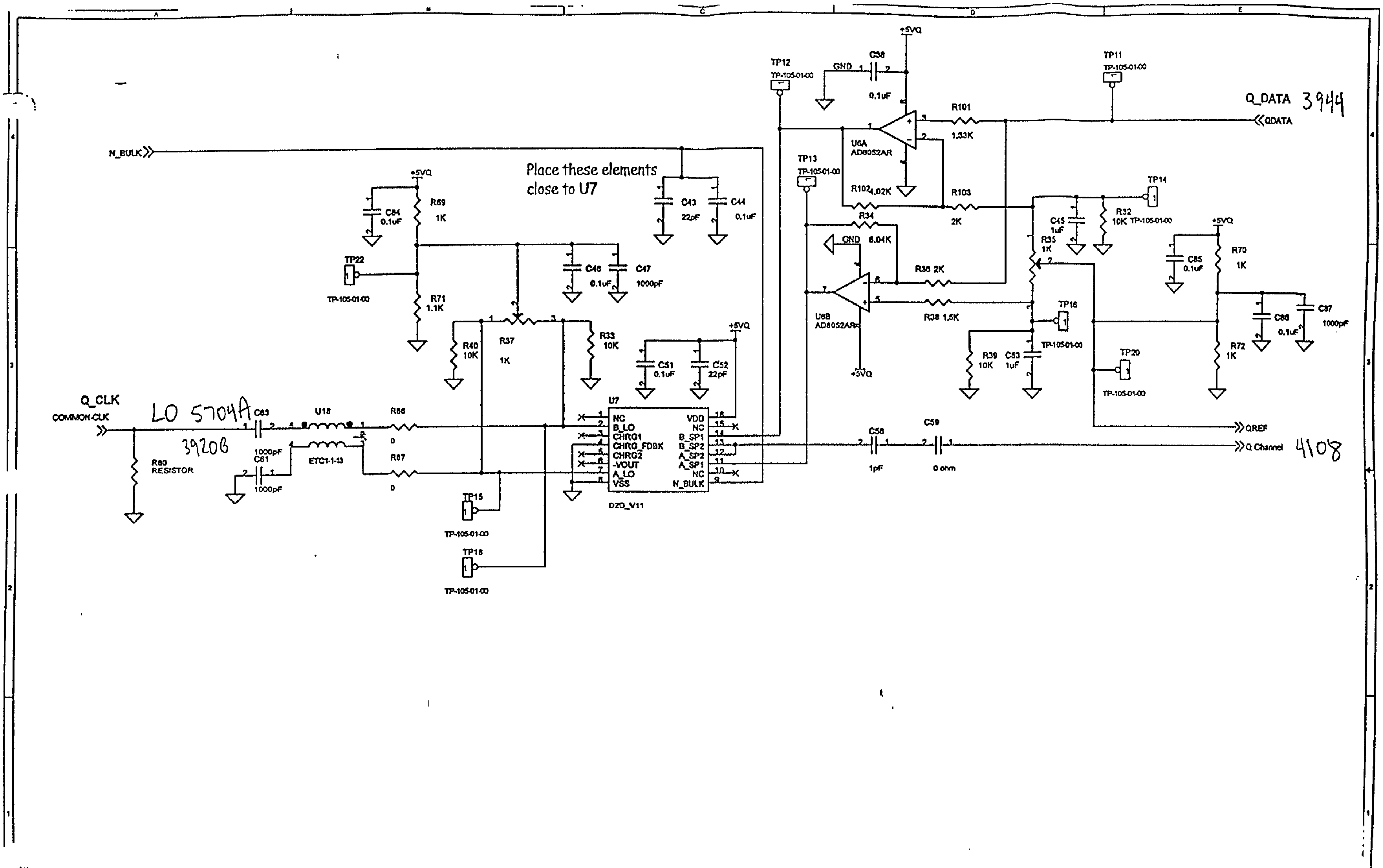

Q_DATA 3944
QDATA
N_BULK
Place these elements close to U7
Q_CLK
COMMON-CLK
LO 5704A
3920B
U7
DZD_V11
NC
B_LO
CHRG1
CHRG_FDBK
CHRG2
-VOUT
A_LO
VSS
VDD
B_SP1
B_SP2
A_SP2
A_SP1
N_BULK
U6A
AD8052AR
U6B
AD8052AR
U18
ETC1-1-13
R101 1.33K
R102 4.02K
R103 2K
R34 6.04K
R36 2K
R38 1.5K
R35 1K
R32 10K
R39 10K
R69 1K
R71 1.1K
R37 1K
R40 10K
R33 10K
R70 1K
R72 1K
R80 RESISTOR
R86 0
R87 0
C38 0.1uF
C43 22pF
C44 0.1uF
C84 0.1uF
C46 0.1uF
C47 1000pF
C51 0.1uF
C52 22pF
C45 1uF
C53 1uF
C85 0.1uF
C86 0.1uF
C87 1000pF
C83 1000pF
C61 1000pF
C58 1pF
C59 0 ohm
+5VQ
GND
TP11
TP12
TP13
TP14
TP15
TP16
TP18
TP20
TP22
TP-105-01-00
QREF
Q Channel 4108

FIG. 60

Page1

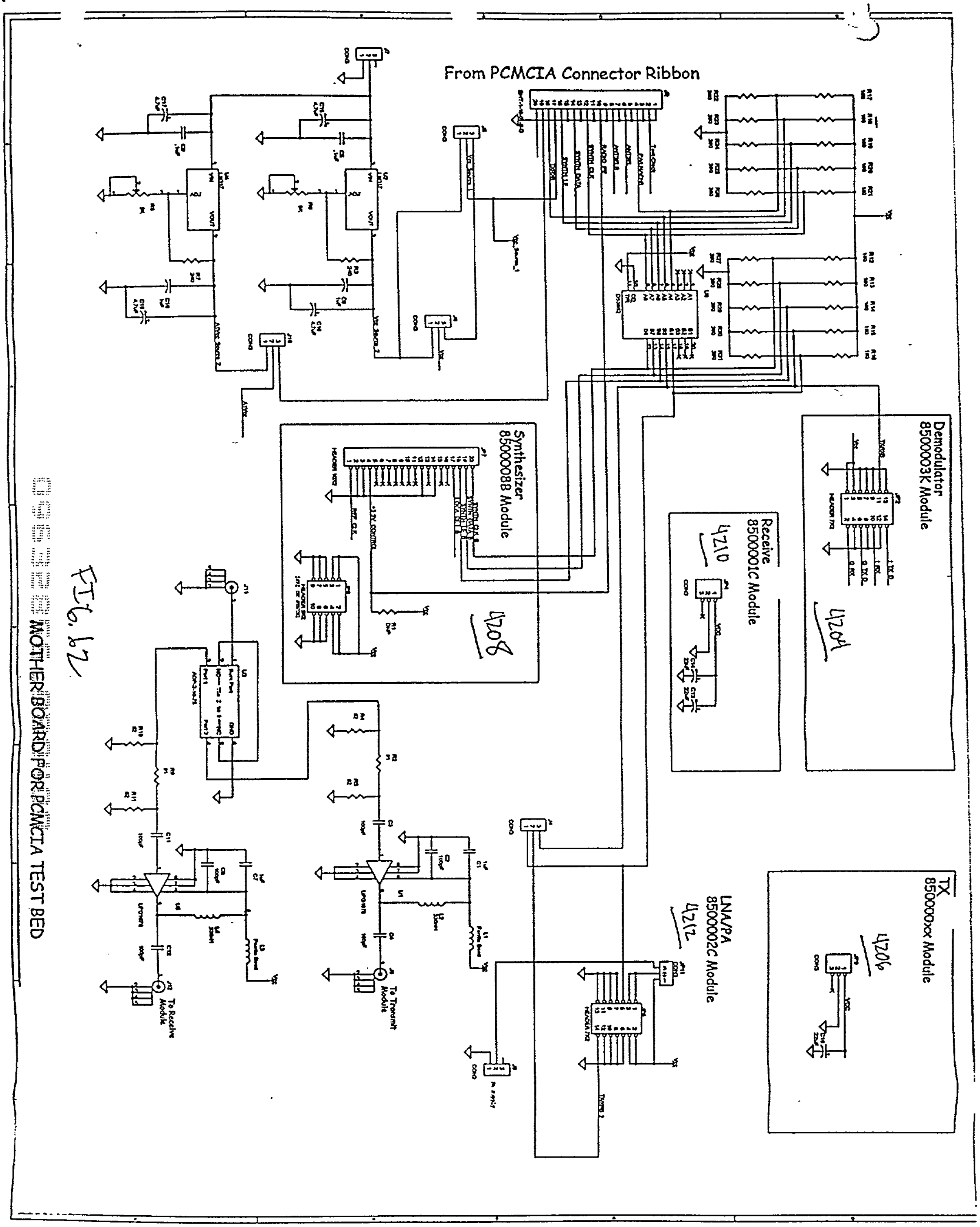
Bill Of Materials

Item	Quantity	Reference	Part	Part Number	Manufacturer
1	21	C3,C6,C8,C10,C14,C38,C44,	0.1uF	GRM39X7R104K016	Murata
		C46,C51,C71,C72,C77,C78,			
		C79,C84,C85,C86,C93,C95,			
		C96,C98			
2	6	C5,C7,C15,C43,C52,C75	22pF	GRM39COG220J050	Murata
3	5	C9,C16,C45,C53,C89	1uF	GRM40Y5V105Z016	Murata
4	8	C11,C23,C25,C47,C61,C63,	1000pF	GRM39X7R102K050	Murata
		C80,C87			
5	2	C58,C21	1pF	GRM39COG010B50V	Murata
6	2	C82,C33	4.7uF	T491A475K006AS	KEMET
7	2	C59,C35	0 ohm	GRM39COGxxxx50V	Murata
8	1	C73	470pF	GRM39COG471J050	Murata
9	1	C83	1uF	T491A105M016AS	Kemet
10	3	C90,C91,C92	100pF	ECU-V1H101JCV	
11	2	C94,C97	0.01uF	GRM39X7R103K016	Murata
12	1	FL1	MDR642E	MDR642E	Soshin
13	1	JP1	Shunt	69190-402	BERG
14	1	JP2	69190-403	69190-403	BERG
15	4	J7,J8,J9,J10	82MMCX-50-0-1	82MMCX-50-0-1	Suhner
16	1	L10	22nH	LL1608-F22NK	Coilcraft
17	1	L12	BLM11A121S	BLM11A121S	Murata
18	1	L13	330nH	LL2012-FR33K	
19	10	R5,R6,R12,R13,R32,R33,	10K	ERJ3EKF1002	Panasonic
		R39,R40,R95,R100			
20	2	R34,R7	6.04K	ERJ3EKF6041	Panasonic
21	4	R8,R10,R35,R37	1K	3224W-1-102	Bourns
22	4	R9,R36,R90,R103	2K	ERJ3EKF2001	Panasonic
23	2	R38,R11	1.5K	ERJ3EKF1501	Panasonic
24	3	R56,R94,R99	0 ohm	ERJ3GSY0R00	Panasonic
25	1	R59	51	ERJ3GSYJ510	Panasonic
26	7	R60,R61,R62,R84,R85,R86,	0	ERJ3GSY0R00	Panasonic
		R87			
27	6	R63,R64,R66,R69,R70,R72	1K	ERJ3EKF1001	Panasonic
28	2	R71,R65	1.1K	ERJ3EKF1101	Panasonic
29	2	R80,R79	RESISTOR		
30	3	R81,R82,R83	R		
31	4	R88,R91,R96,R101	1.33K	ERJ3EKF1331	Panasonic
32	2	R102,R89	4.02K	ERJ3EKF4021	Panasonic
33	2	R92,R97	499	ERJ3EKF4990	Panasonic
34	19	TP1,TP2,TP3,TP4,TP5,TP6,	TP-105-01-00		

FIG. 61A

		TP8,TP9,TP11,TP12,TP13,			
		TP14,TP15,TP16,TP18,TP19,			
		TP20,TP21,TP22			
35	3	U1,U6,U19	AD8052AR	AD8052AR	Analog Devices
36	2	U7,U2	D2D_V11	D2D_V11	Parker Vision
37	1	U11	MAAM22010	MAAM22010	MACOM
38	1	U12	1X603	1X603	Anaren
39	1	U14	AD1582	AD1582	Analog Devices
40	1	U15	UPG1678	UPG1678GV	NEC
41	1	U16	ADP-2-10-75	ADP-2-10-75	Mini-Circuits
42	1		BOARD	8500.641.021	V05.10

FIG. 61B

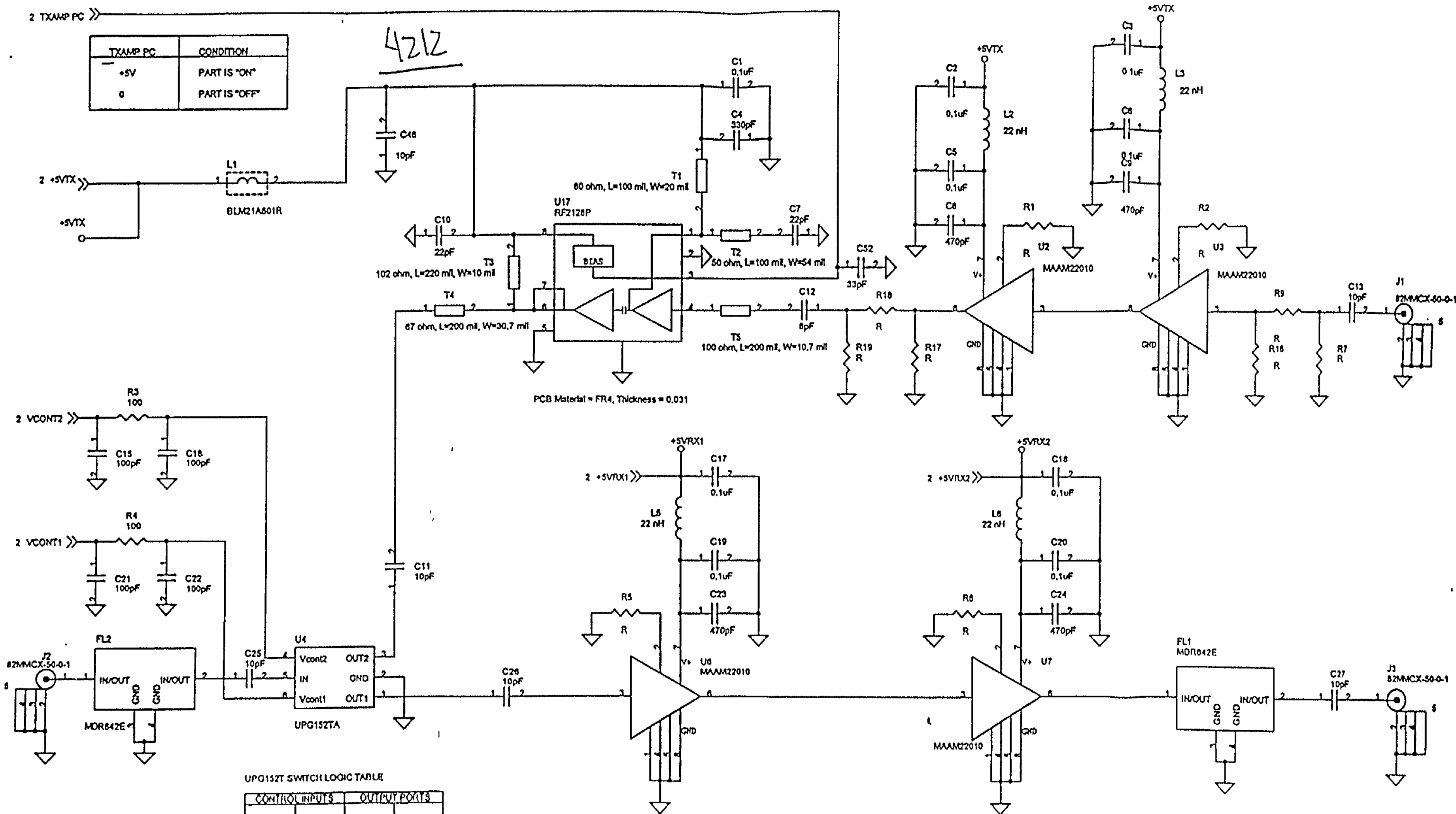

From PCMCIA Connector Ribbon
Synthesizer
8500008B Module
4208
Demodulator
8500003K Module
4204
Receive
8500001C Module
4210
LNA/PA
8500002C Module
4212
TX
85000xx Module
4206
To Receive Module
To Transmit Module
FIG. 62
MOTHER BOARD FOR PCMCIA TEST BED

Bill Of Materials

Item	Qty	Reference	Part	Description	Part Number	Vendor
1	4	C1,C6,C7,C10	1uF	Cap, 1uF, +80-20%, 0805	GRM40Y5V105Z016AD	Murata
2	6	C2,C3,C4,C8,C11,C12	100pF	Cap, 100pF, 5%, COG, 0603	ECU-V1H101JCV	Panasonic
3	2	C5,C9	.1uF	Cap, .1uF, +80-20%, Y5V, 0603		Murata
4	3	C13,C14,C19	22uF	Cap, Tant, 22uF, 20%, 20V	T491D226M020AS	Kemet
5	4	C15,C16,C17,C18	4.7uF	Cap, Tant, 4.7uF, 20%, 20V	T491C475M020AS	Kemet
6	2	JP2,JP6	HEADER 7X2	Receptacle, 7x2pin, .050	SFMC-107-L1-S-D	Samtek
7	9	JP4, J4, J5, J6, J7, JP9, J9, J10, JP11	CON3	Header, 3pin, .100"	69190-403	Berg
8	1	JP7	HEADER 10X2	Receptacle, 10x2pin, .050	SFMC-110-L1-S-D	Samtek
9	1	JP8	HEADER 5X2	Receptacle, 5x2pin, .050	SFMC-105-L1-S-D	Samtek
10	1	J2	EHT-1-10-01-S-D	Header, ribbon, 10x2pin, 2mm	EHT-1-10-01-S-D	Samtek
11	3	J8,J11,J12	82MMCX-50-0-1	Connector, RF	82MMCX-50-0-1	Suhner
12	2	L3,L1	Ferrite Bead	Ferrite Bead, 0805	BLM21A121S	Murata
13	2	L4,L2	330nH	Ind, 330nH, 10%, 0805	LL2012-FR33K	Toko
14	1	R1	DNP	Res, 0603		Panasonic
15	2	R9,R2	91	Res, 91 Ohm, 5%, 0603	ERJ-3GSYJ910	Panasonic
16	2	R7,R3	240	Res, 240 Ohm, 5%, 0603	ERJ-3GSYJ241	Panasonic
17	4	R4,R5,R10,R11	82	Res, 82 Ohm, 5%, 0603	ERJ-3GSYJ820	Panasonic
18	2	R8,R6	5K	Var Res, 5K, 10%	3296W001502	Bourns
19	10	R12, R13, R14, R15, R16, R17, R18, R19, R20, R21	180	Res, 180 Ohm, 5%, 0603	ERJ-3GSYJ181	Panasonic
20	10	R22, R23, R24, R25, R26, R27, R28, R29, R30, R31	390	Res, 390 Ohm, 5%, 0603	ERJ-3GSYJ391	Panasonic
21	2	U5,U1	UPG1678	IC, RF Buffer	UPG1678GV	NEC
22	2	U4,U2	LM317	IC, Voltage Regulator	LM317T	National
23	1	U3	ADP-2-10-75	RF Splitter	ADP-2-10-75	MiniCircuits
24	1	U6	DS3862	IC, Buffer	DS3862WM	National
25	1			BOARD	STBS00.641.023 VOL01	

FIG. 63

FIG 64

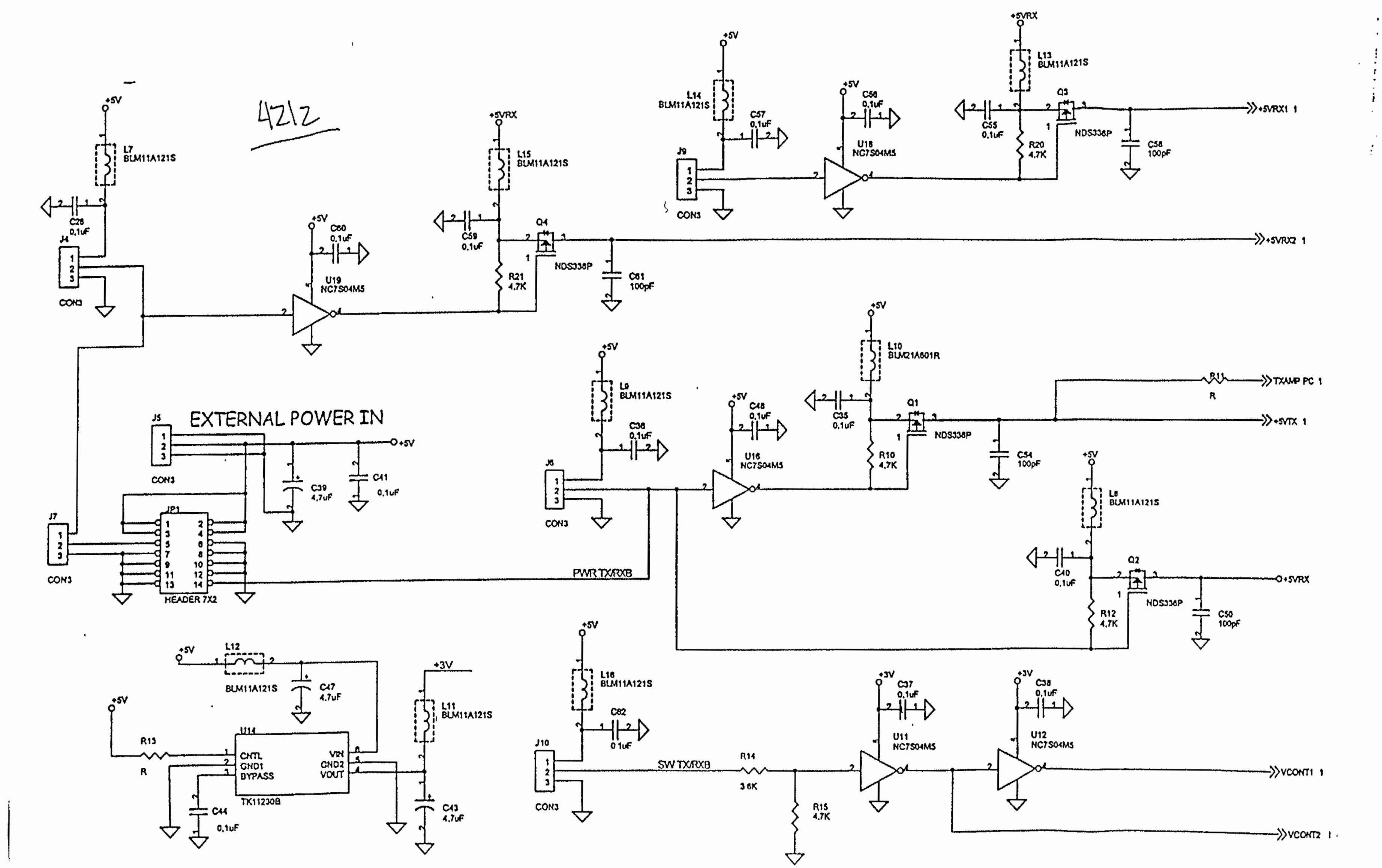


TXAMP PC	CONDITION
+5V	PART IS "ON"
0	PART IS "OFF"

UPG152T SWITCH LOGIC TABLE

CONTROL INPUTS		OUTPUT PORTS	
VCONT1	VCONT2	OUT1	OUT2
0	0	OFF	OFF
0	+3	ON	OFF
+3	0	OFF	ON
+3	+3	OFF	OFF

FIG. 65


4212
EXTERNAL POWER IN
+5V
+5VRX
+3V
L7 BLM11A121S
L15 BLM11A121S
L14 BLM11A121S
L13 BLM11A121S
L9 BLM11A121S
L10 BLM21A601R
L8 BLM11A121S
L12 BLM11A121S
L11 BLM11A121S
L16 BLM11A121S
U19 NC7S04M5
U18 NC7S04M5
U16 NC7S04M5
U11 NC7S04M5
U12 NC7S04M5
Q4 NDS336P
Q3 NDS336P
Q1 NDS336P
Q2 NDS336P
U14 TK11230B
CNTL
GND1
BYPASS
VIN
GND2
VOUT
JP1 HEADER 7X2
J4 CON3
J9 CON3
J5 CON3
J6 CON3
J7 CON3
J10 CON3
PWR TX/RXB
SW TX/RXB
+5VRX1
+5VRX2
TXAMP PC
+5VTX
VCONT1
VCONT2
R11 R
R13 R
R14 3.6K
R15 4.7K
R21 4.7K
R20 4.7K
R10 4.7K
R12 4.7K
C28 0.1uF
C59 0.1uF
C60 0.1uF
C61 100pF
C57 0.1uF
C56 0.1uF
C55 0.1uF
C58 100pF
C36 0.1uF
C48 0.1uF
C35 0.1uF
C54 100pF
C39 4.7uF
C41 0.1uF
C40 0.1uF
C50 100pF
C47 4.7uF
C44 0.1uF
C43 4.7uF
C62 0.1uF
C37 0.1uF
C38 0.1uF

S

Bill Of Materials

Item	Qty	Reference	Part	Manufacturer	Part Description	Part Number
1	24	C1,C2,C3,C5,C6,C17,C18,	0.1uF	Murata	.1uF,0603,X7R,20%,16V	GRM39X7R104MO16
		C19,C20,C28,C35,C36,C37,				
		C38,C40,C41,C44,C48,C55,				
		C56,C57,C59,C60,C62				
2	1	C4	330pF	Murata	330pF,0603,COG,10%,50	GRM39COG331K050
3	2	C10,C7	22pF	Murata	22pF,0603,COG,10%,50	GRM39COG220K050
4	4	C8,C9,C23,C24	470pF	Murata	470pF,0603,COG,10%,50	GRM39COG471K050
5	6	C11,C13,C25,C26,C27,C46	10pF	Murata	10pF,0603,COG,10%,50	GRM39COG100K050
6	1	C12	8pF	Murata	8pF,0603,COG,10%,50	GRM39COG080K050
7	8	C15,C16,C21,C22,C50,C54,	100pF	Murata	100pF,0603,COG,10%,50	GRM39COG101K050
		C58,C61				
8	3	C39,C43,C47	4.7uF	Panasonic	4.7 uF tantalum, 16V	ECS-T1CY475R
9	1	C52	33pF	Murata	330pF,0603,COG,10%,50	GRM39COG330K050
10	2	FL1,FL2	MDR642E	Soshin	2.4-2.5GHz BPF	MDR642E
11	1	JP1	HEADER 7X2	Samtec	Dual Row, 7 pins per row	FTSH-107-01-F-D
12	3	J1,J2,J3	82MMCX-50-0-1	Suhner	RF Connector	82MMCX-50-0-1
13	6	J4,J5,J6,J7,J9,J10	CON3	Berg	3 pin header w retentive leg	69190-403H
14	2	L10,L1	BLM21A601R	Murata	600 ohms@100MHz, 500 mA Ferrite Bead	BLM21A601R
15	4	L2,L3,L5,L6	22 nH	Coilcraft	22nH, 0805CS (2012), 5%	0805CS-220X-BC
16	9	L7,L8,L9,L11,L12,L13,L14,	BLM11A121S	Murata	RF Bead	BLM11A121S
		L15,L16				
17	4	Q1,Q2,Q3,Q4	NDS336P	National	P-Channel FET	NDS336P
18	12	R1,R2,R5,R6,R7,R9,R11,	R	Panasonic		
		R13,R16,R17,R18,R19				
19	2	R3,R4	100	Panasonic	0603, 100, 5%, 1/16 W	ERJ-3GSY-J-101
20	5	R10,R12,R15,R20,R21	4.7K	Panasonic	0603, 4.7K, 5%, 1/16 W	ERJ-3GSY-J-472
21	1	R14	3.6K	Panasonic	0603, 3.6K, 5%, 1/16 W	ERJ-3GSY-J-362
22	1	T1	80 ohm, L=100 mil, W=20 mil		80 ohm, L=100 mil, W=20 mil	
23	1	T2	50 ohm, L=100 mil, W=54 mil		50 ohm, L=100 mil, W=54 mil	
24	1	T3	102 ohm, L=220 mil, W=10 mil		102 ohm, L=220 mil, W=10 mil	
25	1	T4	67 ohm, L=200 mil, W=30.7 mil		67 ohm, L=200 mil, W=30.7 mil	
26	1	T5	100 ohm, L=200 mil, W=10.7 mil		100 ohm, L=200 mil, W=10.7 mil	
27	4	U2,U3,U6,U7	MAAM22010	MACOM	2.4-2.5 GHz LNA	MAAM22010
28	1	U4	UPG152TA	NEC	RF Switch	UPG152TA
29	5	U11,U12,U16,U18,U19	NC7S04M5	National	Inverter	NC7S04M5
30	1	U14	TK11230B	TOKO	Voltage Regulator	TK11230B
31	1	U17	RF2128P	RFMD	Medium Power Linear Amplifier	RF2128P

FIG. 66

Page 1 of 1

B500.641.024 V01

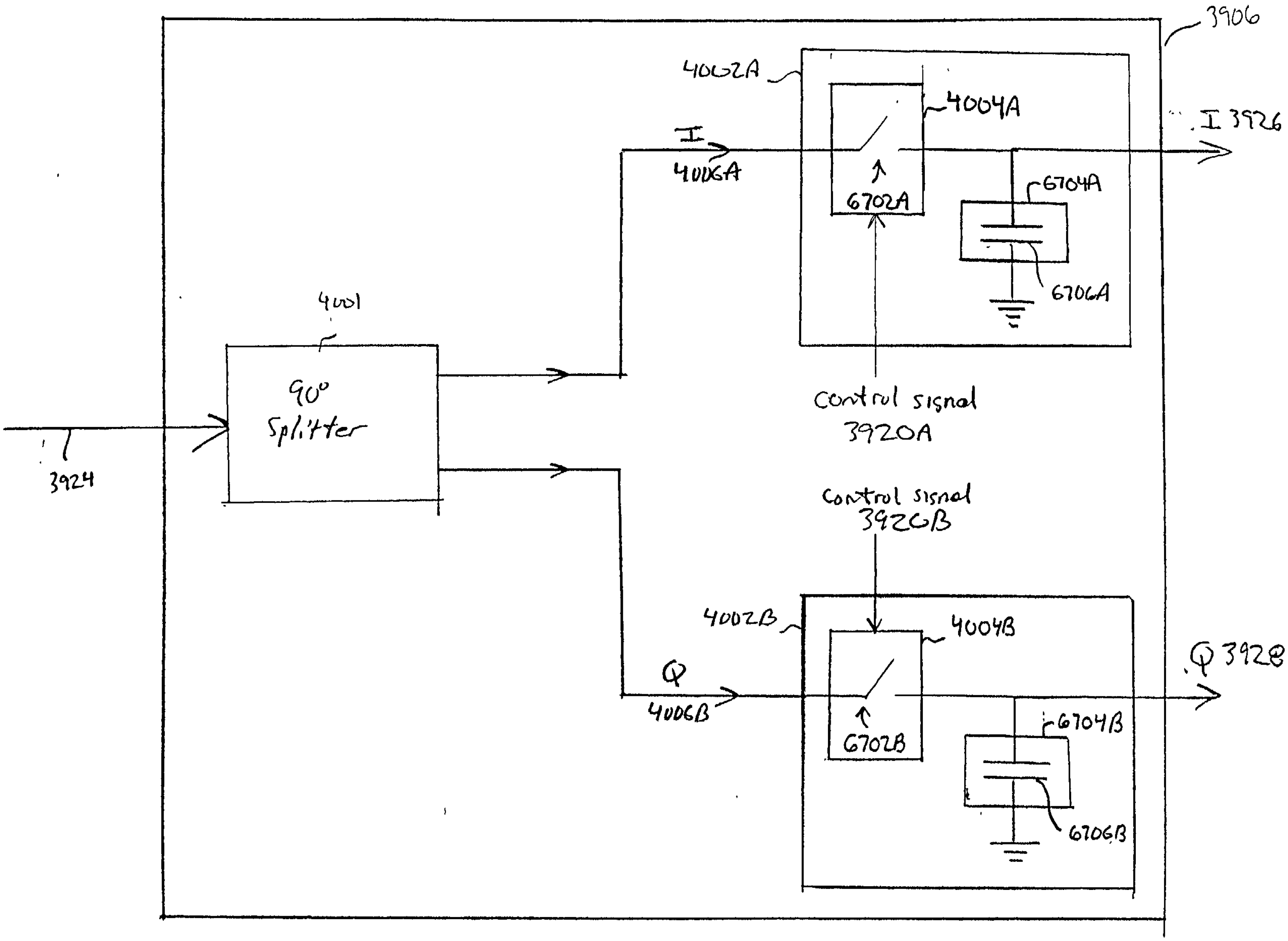

3906
4002A
4004A
I
4006A
I 3926
6704A
6702A
6706A
4001
90° Splitter
Control signal 3920A
3924
Control signal 3920B
4002B
4004B
Q
4006B
Q 3928
6702B
6704B
6706B

FIG. 67A

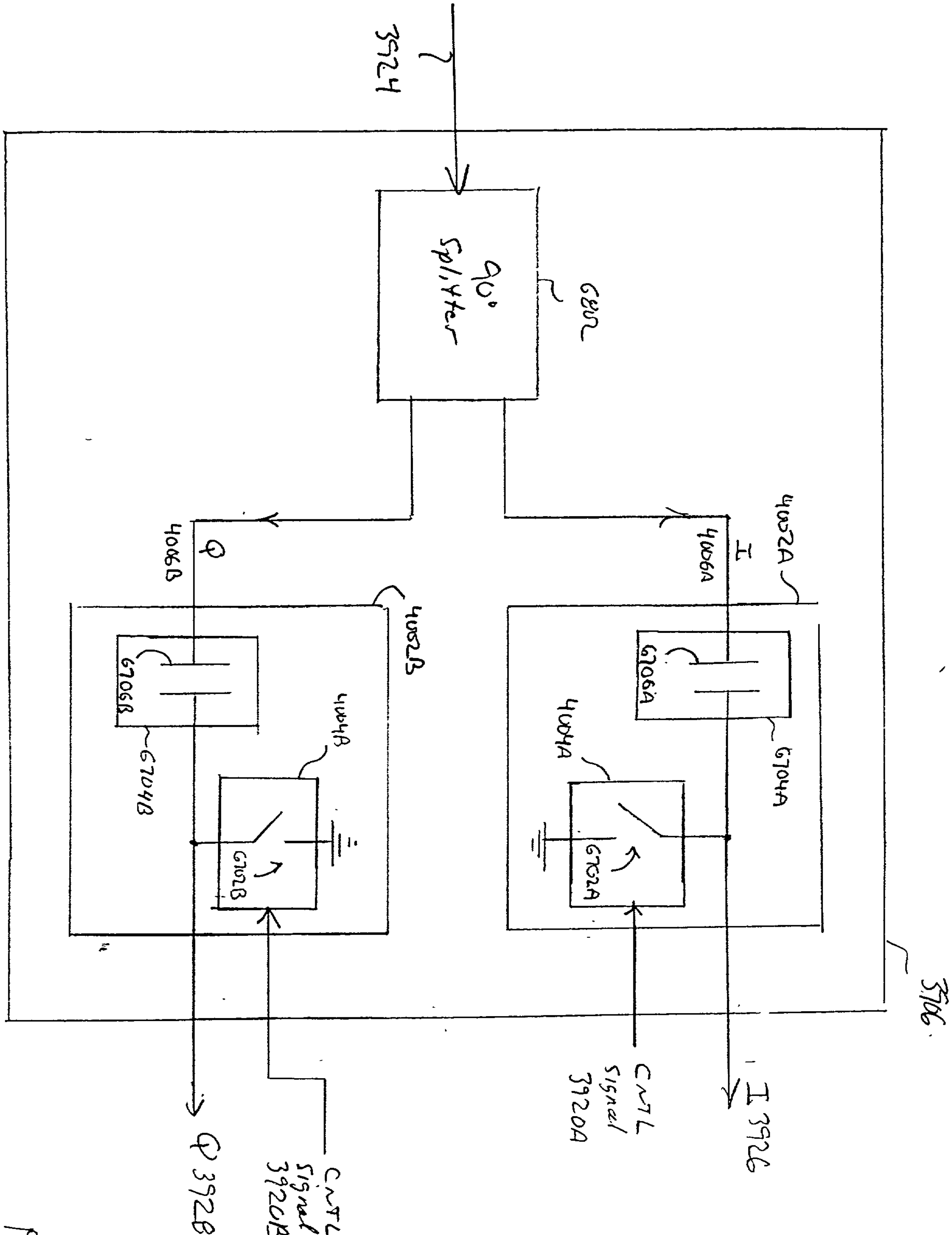

3924
90° Splitter
6802
4002A
4006A
I
4006B
Q
4002B
6706A
6704A
4004A
6702A
6706B
6704B
4004B
6702B
3706
CNTL Signal 3920A
I 3926
CNTL Signal 3920B
Q 3928

FIG.67B

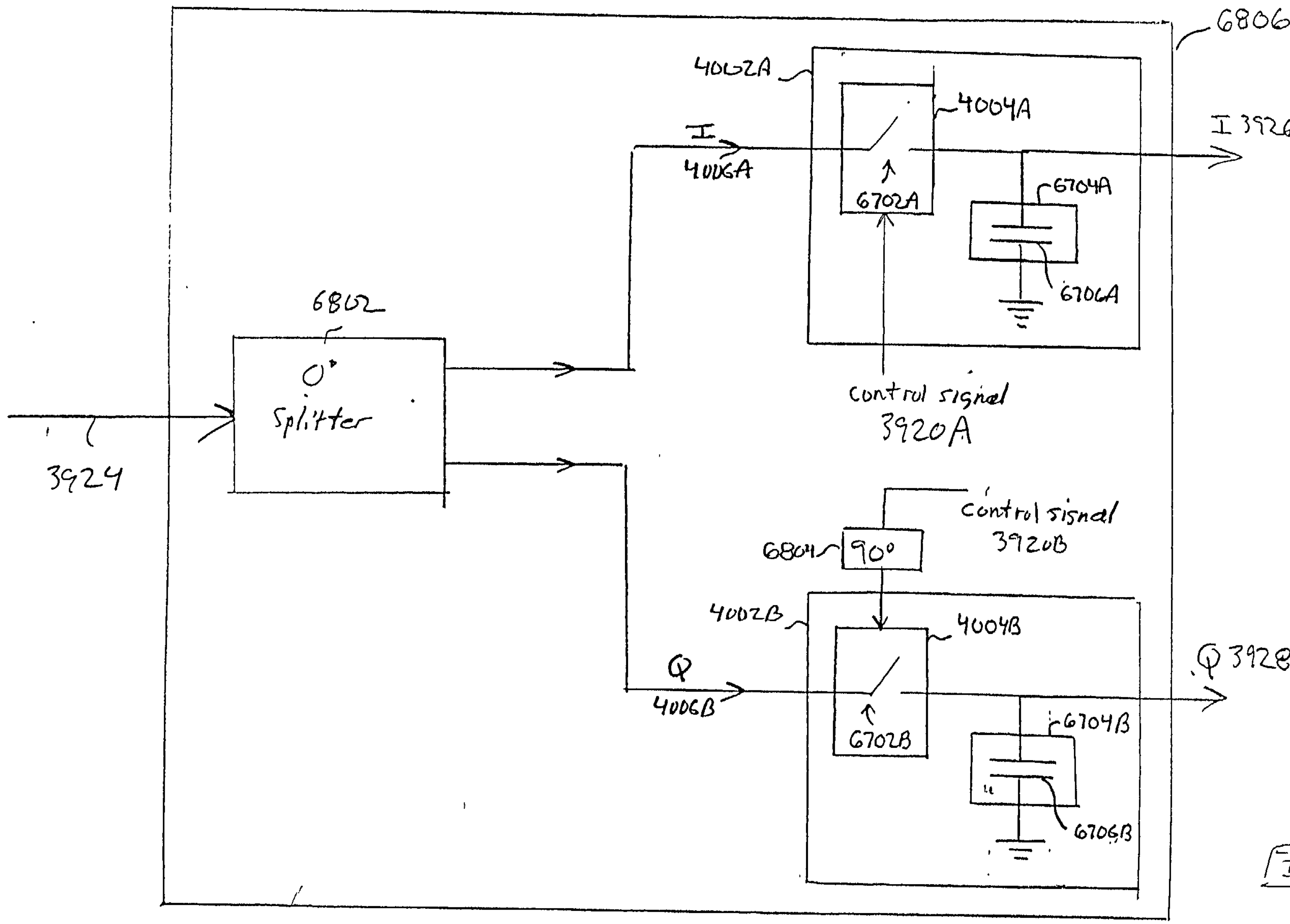


FIG. 68A

09632856 .080400

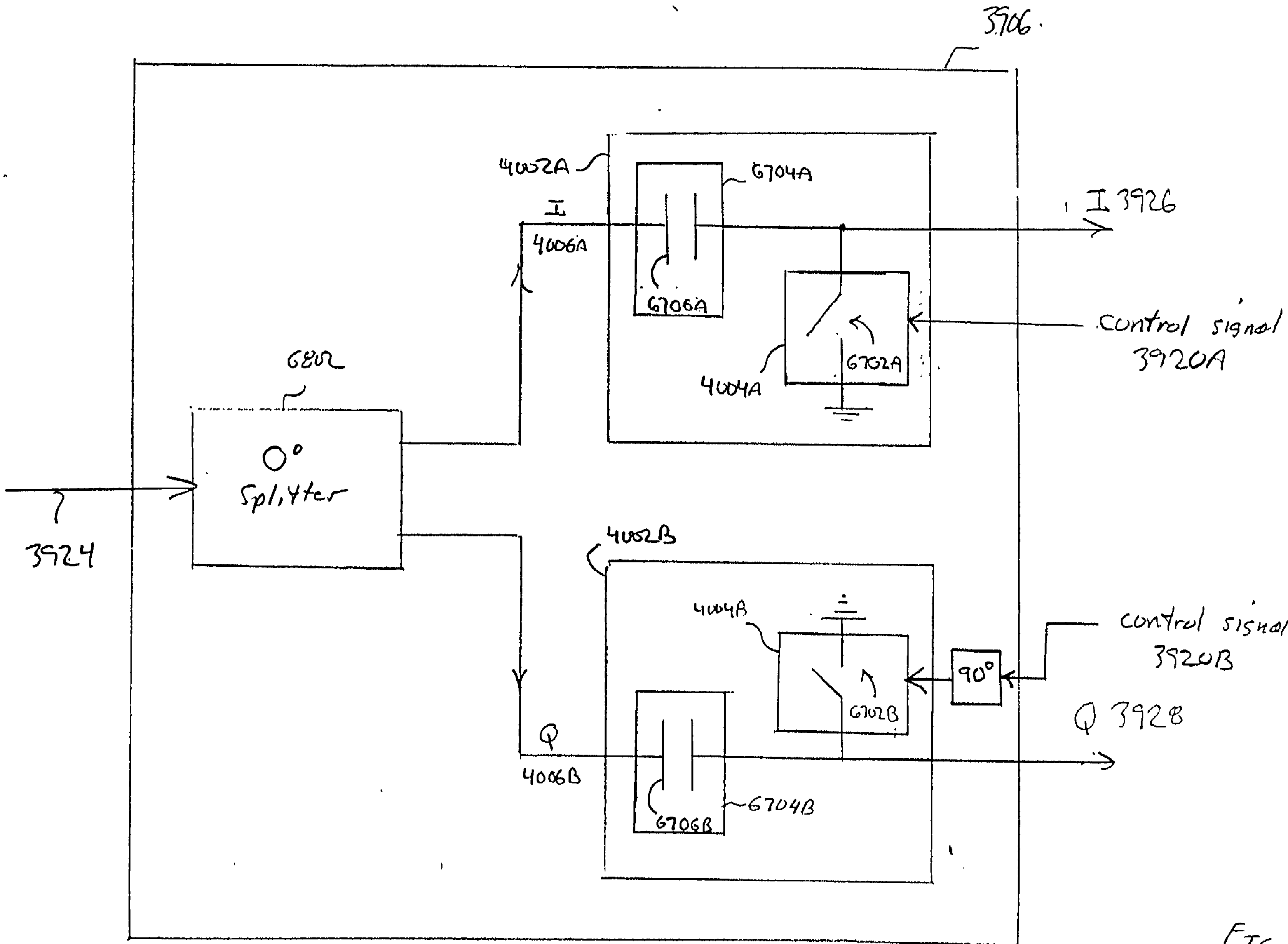

3906
4002A
6704A
I
4006A
I 3926
6706A
control signal
3920A
6702A
4004A
6802
0°
Splitter
3924
4002B
4004B
control signal
3920B
90°
6702B
Q 3928
Q
4006B
6704B
6706B

FIG. 68B

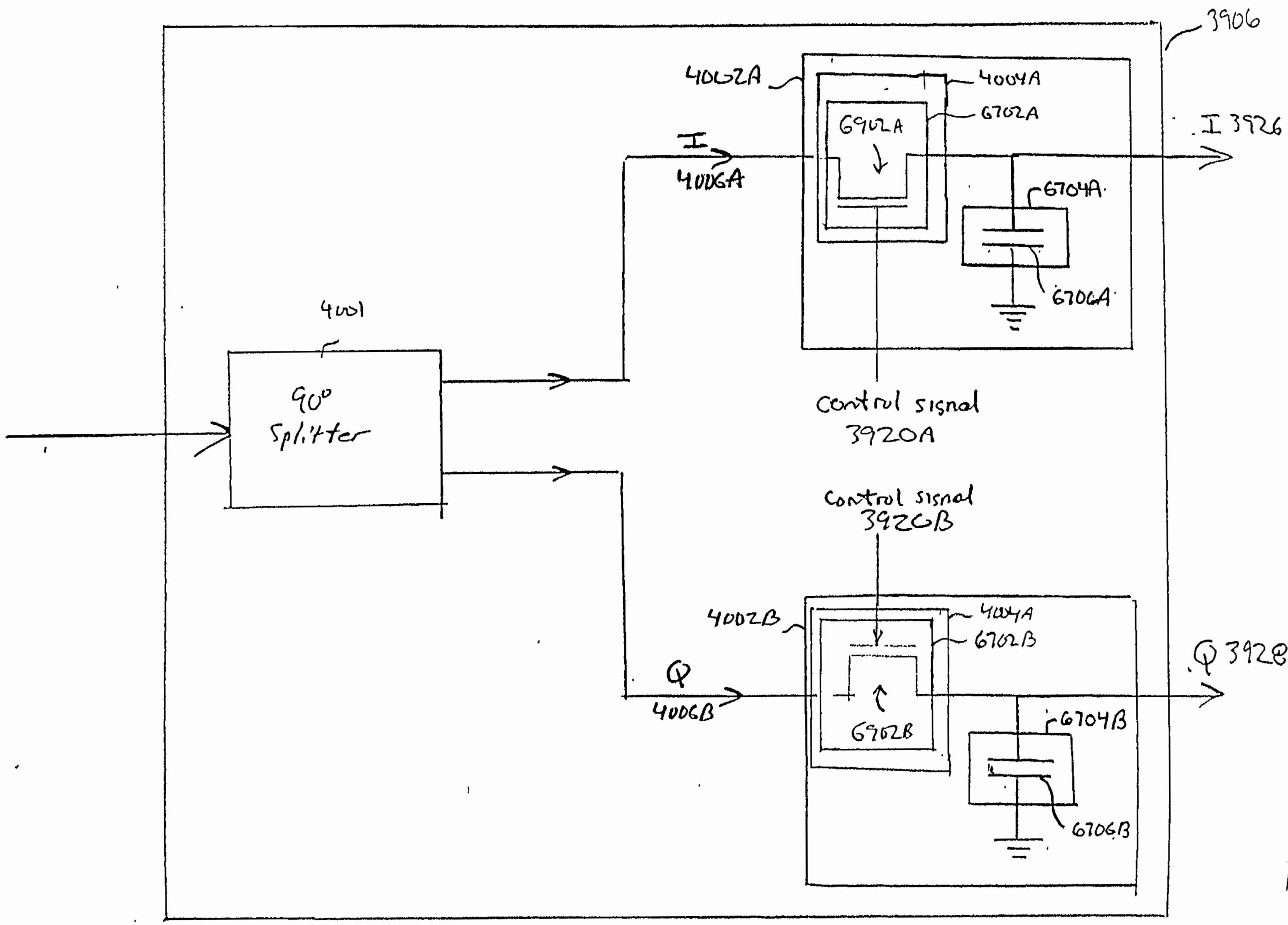

3906
4002A
4004A
6702A
6902A
I 3926
I
4006A
6704A
6706A
4001
90° Splitter
control signal 3920A
control signal 3920B
4002B
4004A
6702B
Q 3928
Q
4006B
6902B
6704B
6706B

FIG. 69A

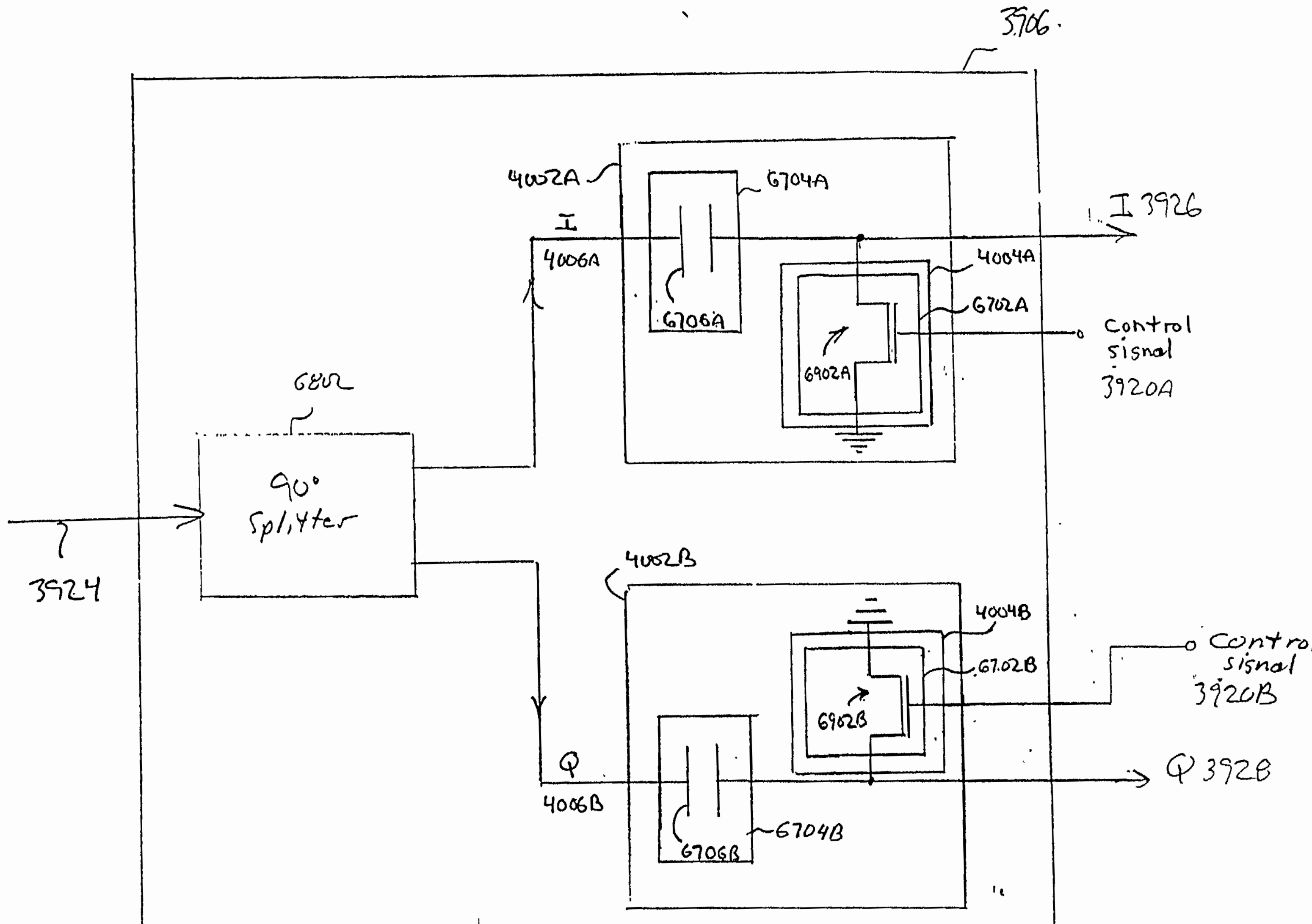


FIG. 69B

09632856 .080400

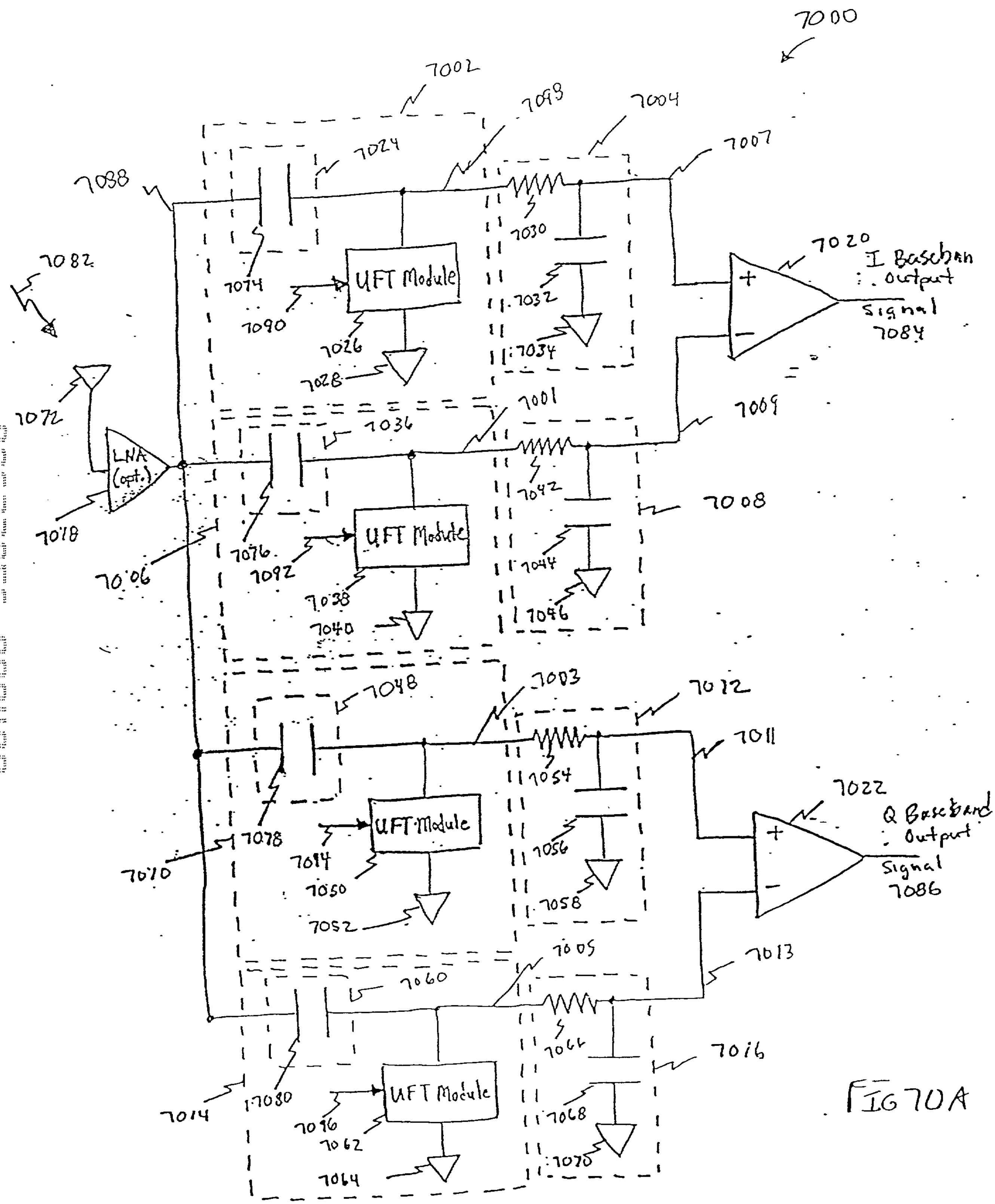

7000
7002
7098
7004
7007
7024
7088
7030
7020
I Baseban Output Signal 7084
7082
7074
UFT Module
7090
7032
7026
7034
7028
7072
7001
7009
7036
LNA (opt.)
7042
7008
7018
7076
UFT Module
7092
7044
7006
7038
7046
7040
7048
7003
7012
7011
7054
7022
Q Baseband Output Signal 7086
UFT Module
7078
7094
7056
7010
7050
7058
7052
7005
7013
7060
7066
7016
UFT Module
7014
7080
7096
7068
7062
7070
7064

FIG 70A

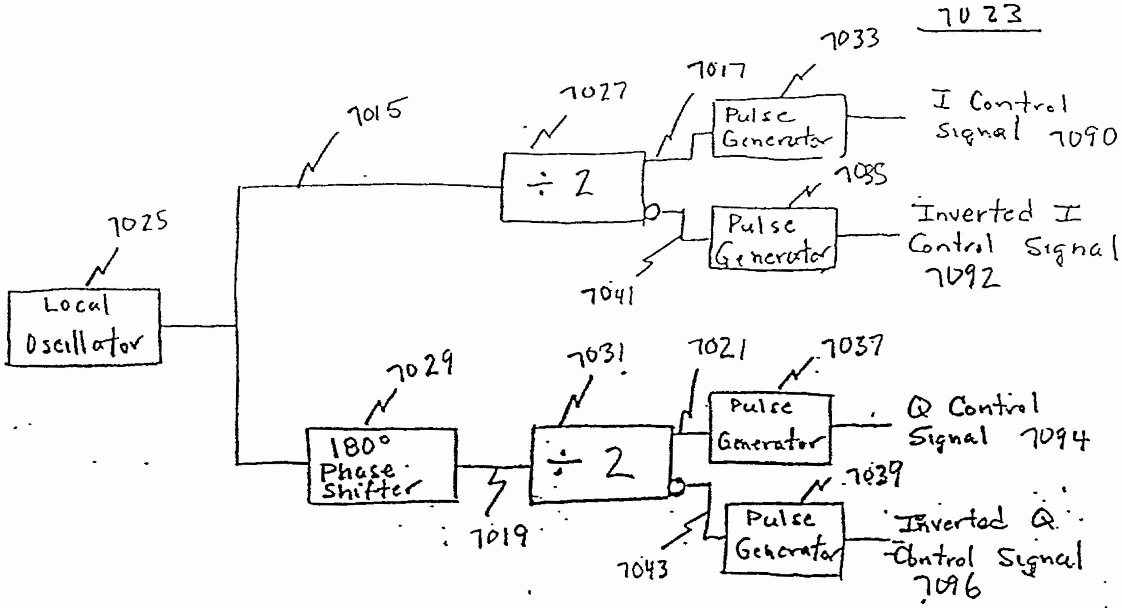


FIG. 70B

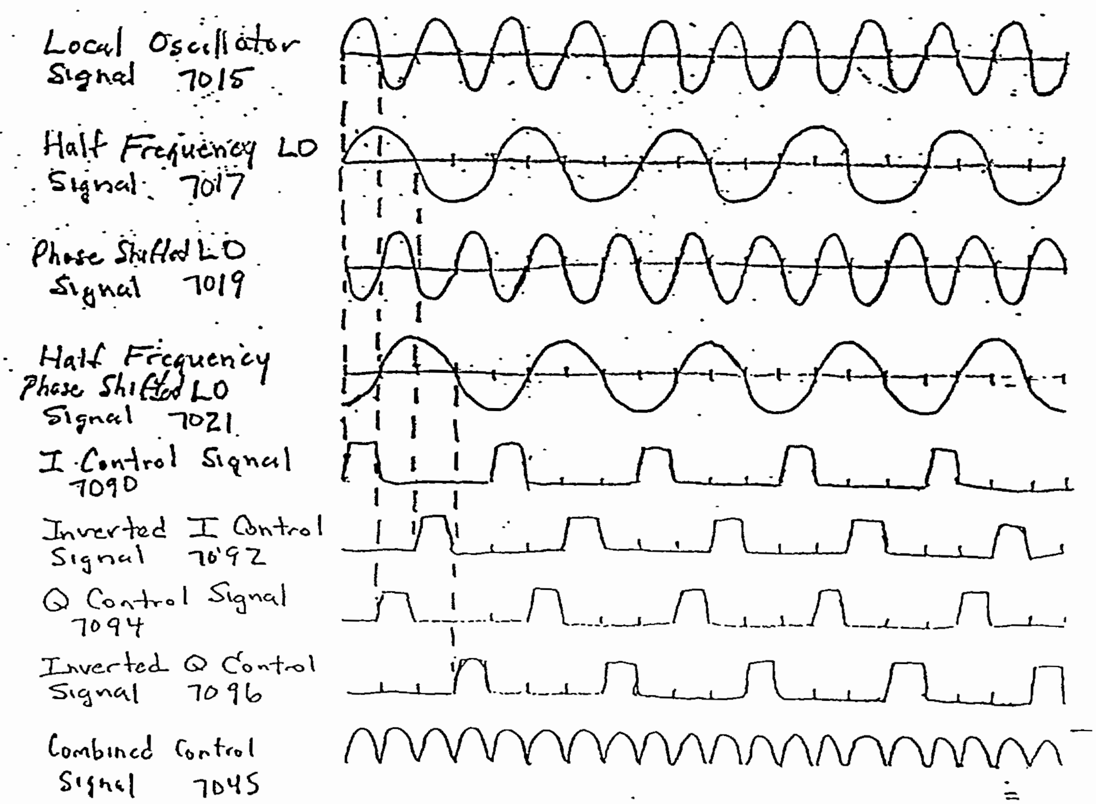


FIG. 70C

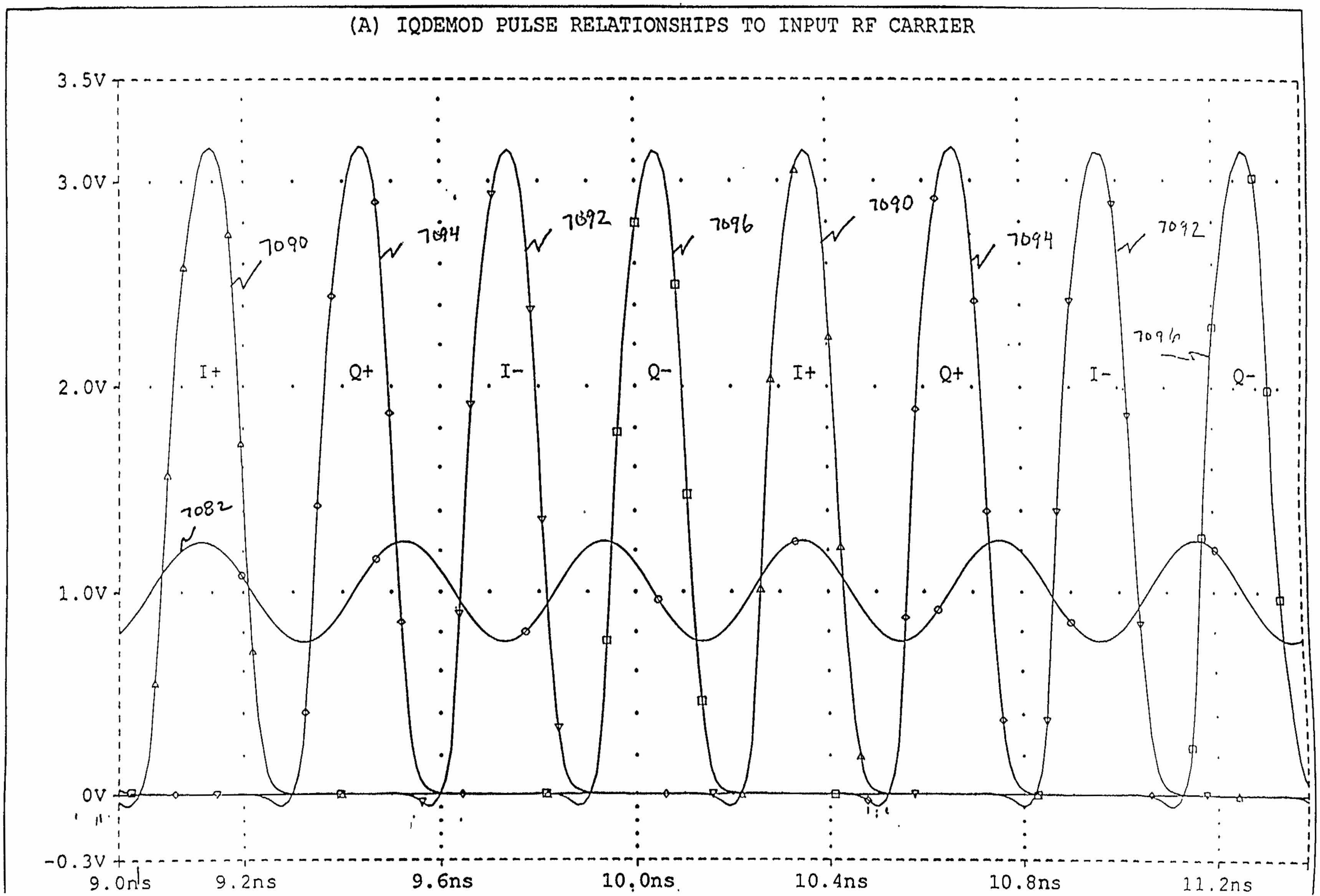

(A) IQDEMOD PULSE RELATIONSHIPS TO INPUT RF CARRIER
3.5V
3.0V
2.0V
1.0V
0V
-0.3V
9.0ns
9.2ns
9.6ns
10.0ns
10.4ns
10.8ns
11.2ns
I+
Q+
I-
Q-
I+
Q+
I-
Q-
7090
7094
7092
7096
7090
7094
7092
7096
7082

FIG. 70D

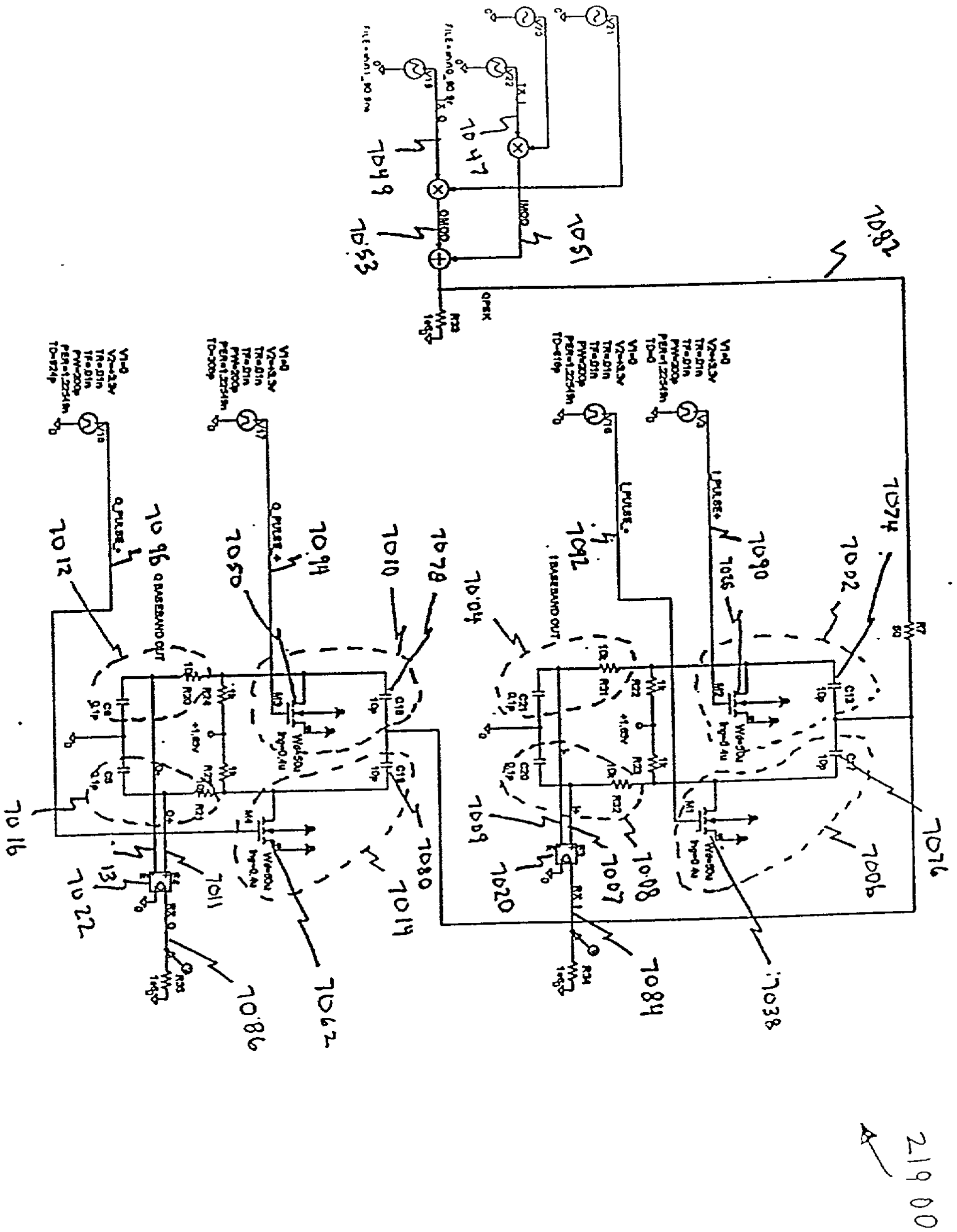
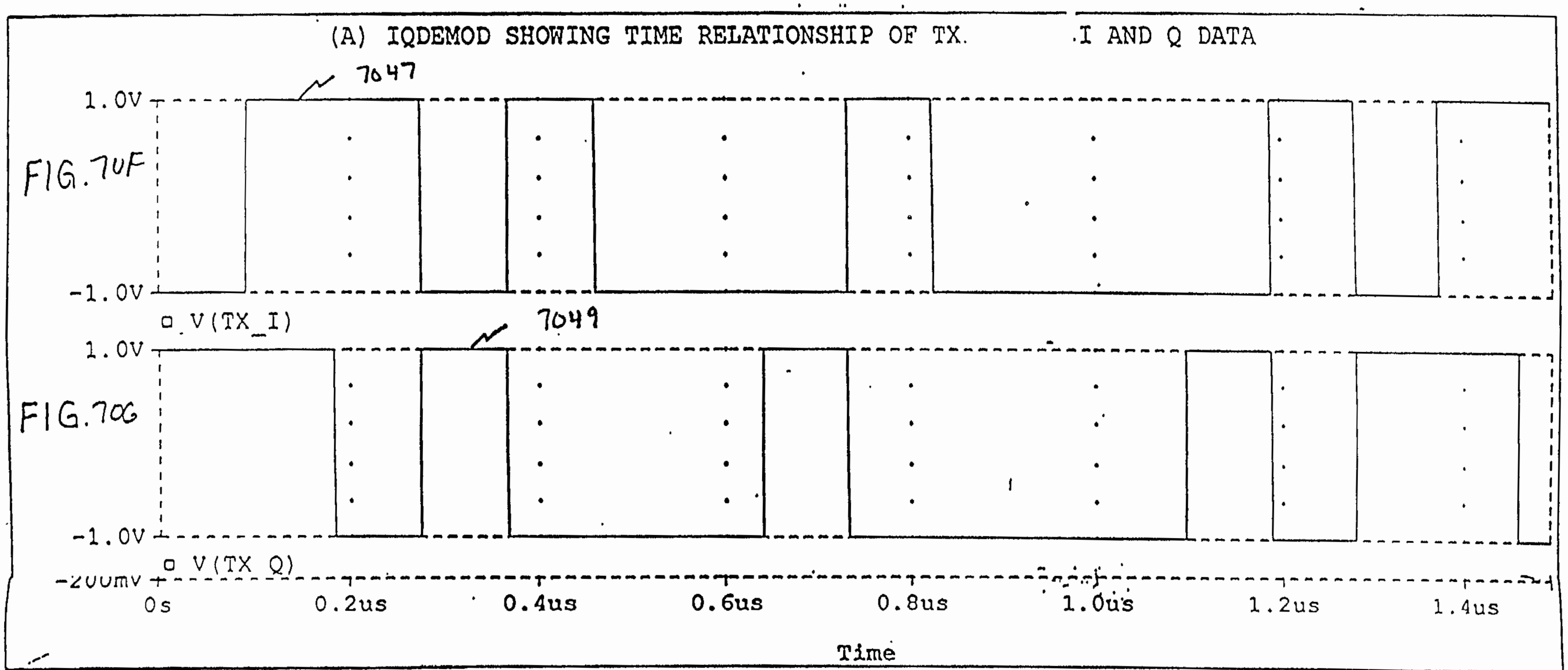
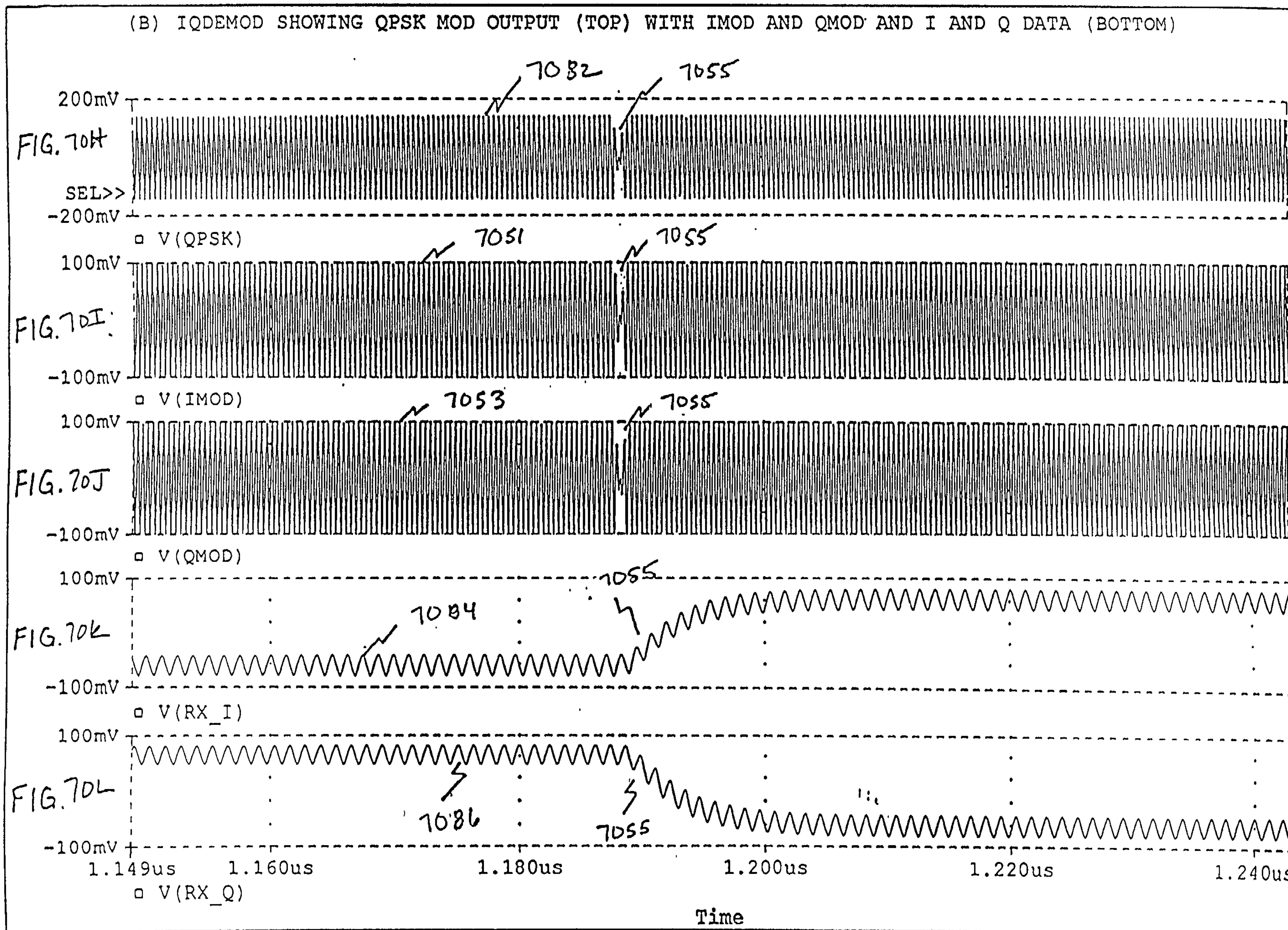


FIG. 70E

Page 1

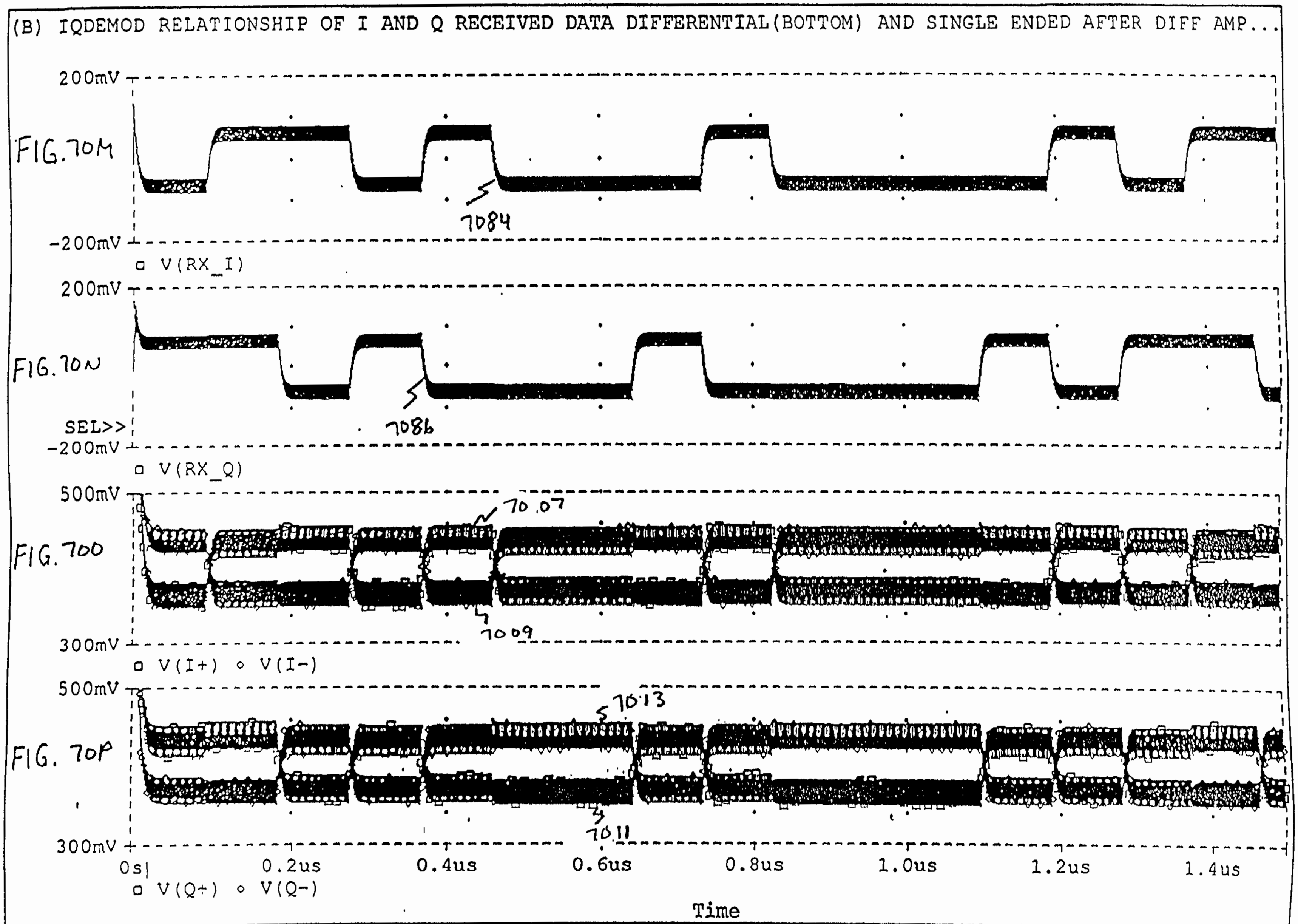


(A) IQDEMOD SHOWING TIME RELATIONSHIP OF TX. .I AND Q DATA
7047
1.0V
FIG.70F
-1.0V
V(TX_I)
7049
1.0V
FIG.70G
-1.0V
V(TX_Q)
-200mV
0s
0.2us
0.4us
0.6us
0.8us
1.0us
1.2us
1.4us
Time



Page 1

09632856 .080400


(B) IQDEMOD RELATIONSHIP OF I AND Q RECEIVED DATA DIFFERENTIAL(BOTTOM) AND SINGLE ENDED AFTER DIFF AMP...
FIG. 70M
200mV
-200mV
7084
V(RX_I)
FIG. 70N
200mV
SEL>>
-200mV
7086
V(RX_Q)
FIG. 70O
500mV
300mV
7007
7009
V(I+) V(I-)
FIG. 70P
500mV
300mV
7013
7011
0s
0.2us
0.4us
0.6us
0.8us
1.0us
1.2us
1.4us
V(Q+) V(Q-)
Time

Page 1

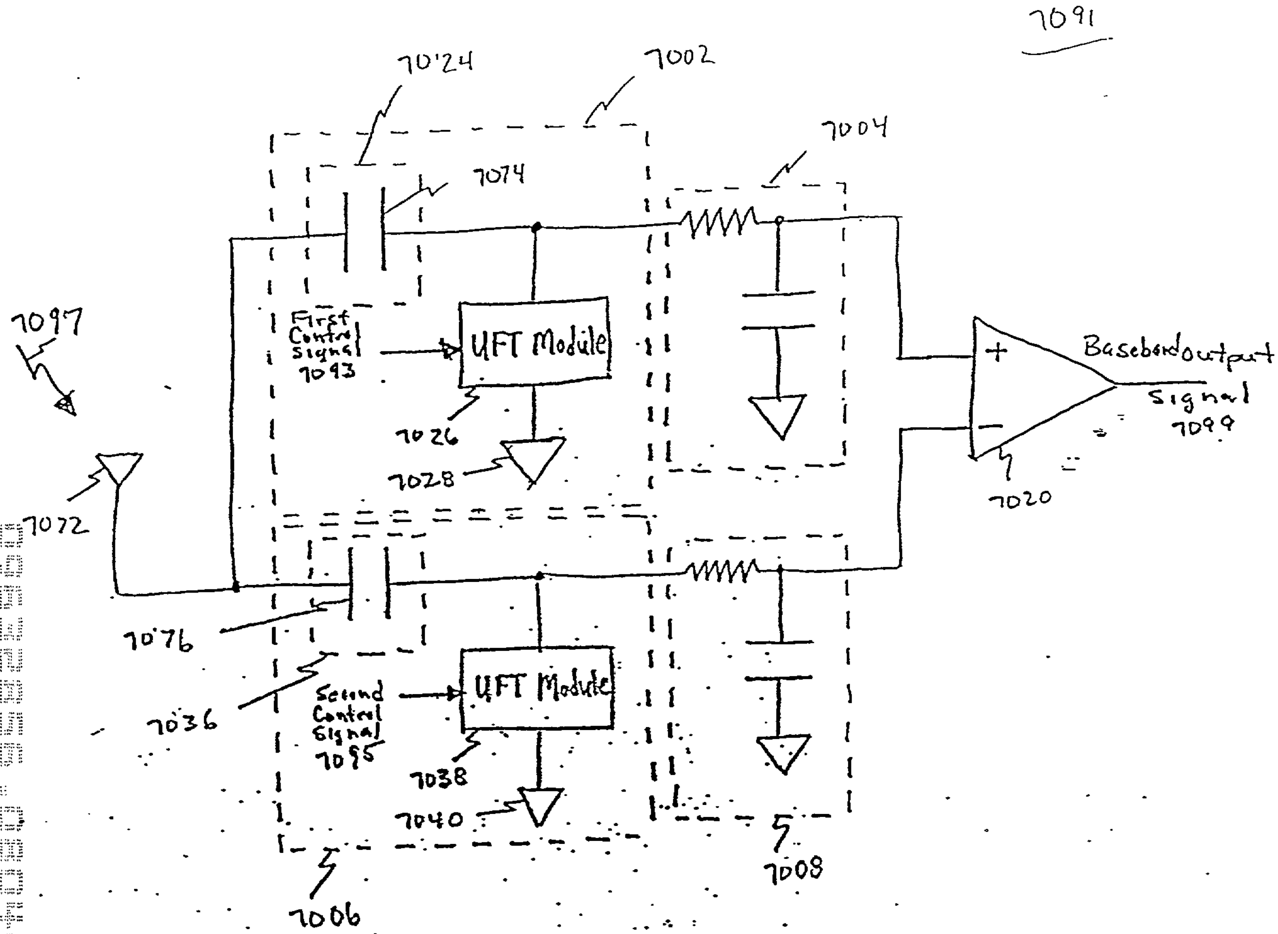

7091
7024
7002
7004
7074
7097
First Control Signal 7093
UFT Module
Baseband output signal 7099
7026
7028
7020
7072
7076
7036
Second Control Signal 7095
UFT Module
7038
7040
7008
7006

FIG. 70Q

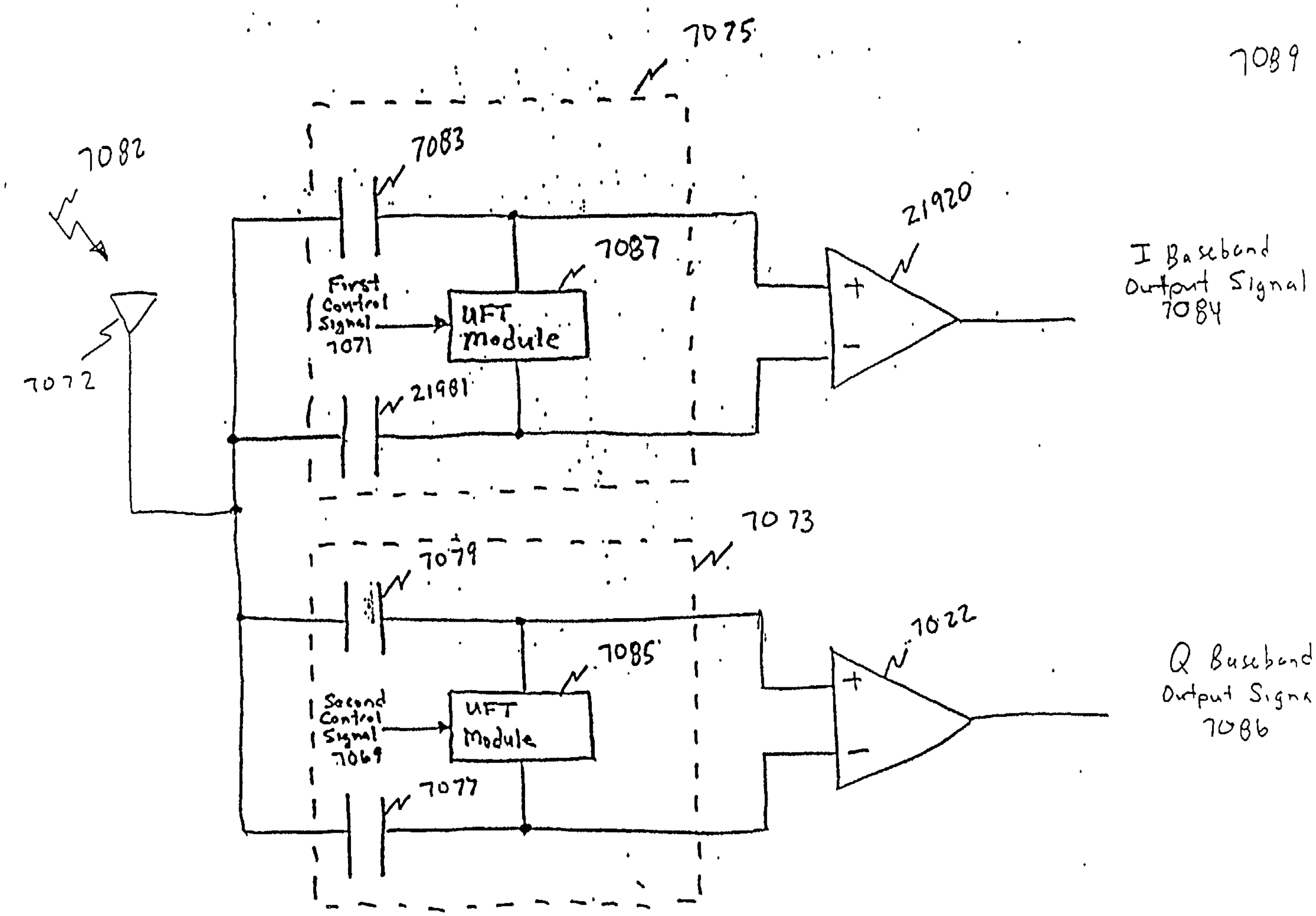


FIG. 70 R

09632856.080400

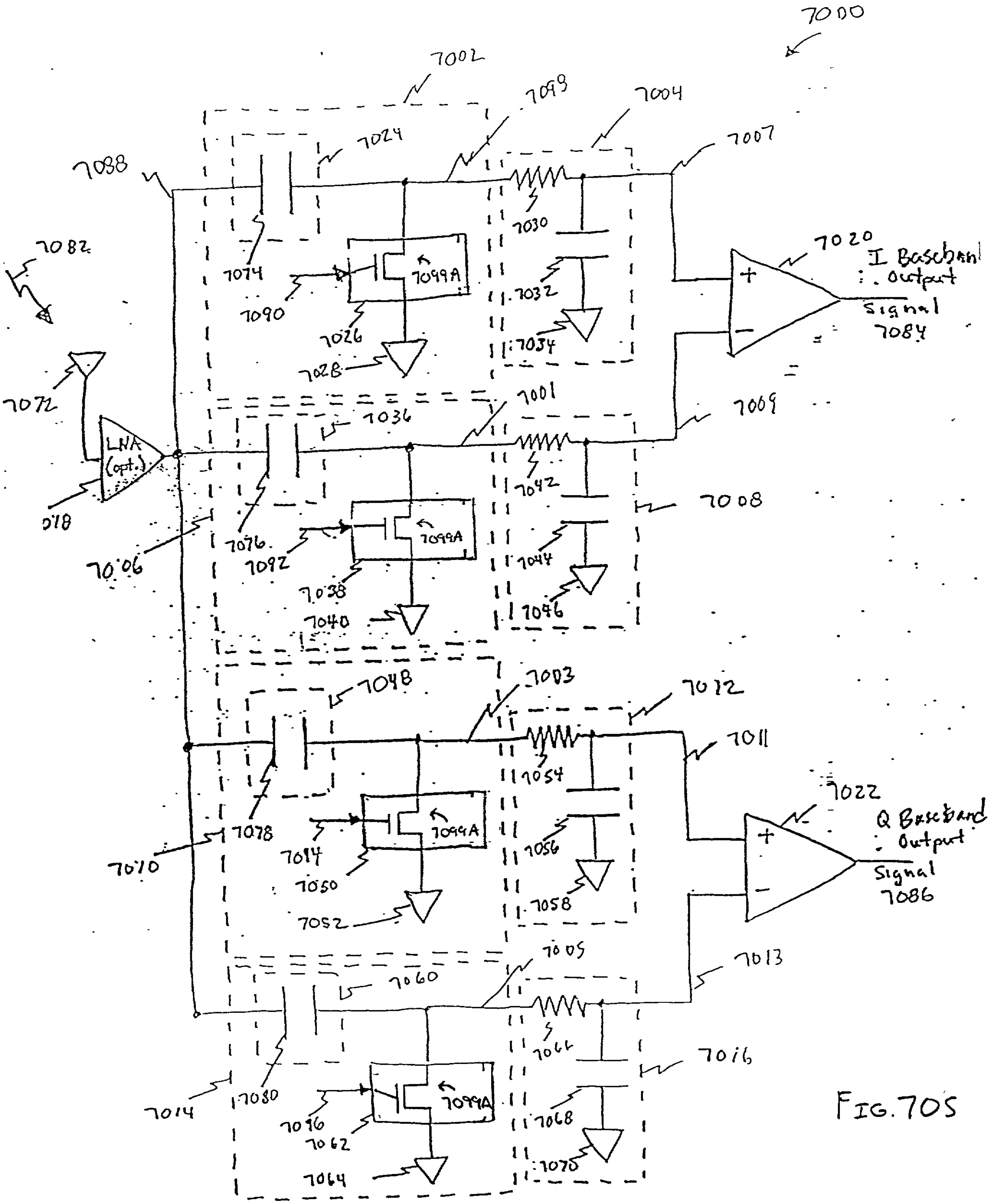

7000
7002
7098
7004
7024
7007
7088
7030
7020
I Baseband Output Signal 7084
7082
7074
7099A
7090
7032
7026
7034
7028
7072
7001
7036
7009
LNA (opt.)
7042
7008
7018
7076
7092
7044
7006
7038
7046
7040
7048
7003
7012
7011
7054
7022
Q Baseband Output Signal 7086
7010
7078
7094
7056
7050
7058
7052
7005
7013
7060
7066
7016
7014
7080
7096
7068
7062
7070
7064

FIG. 70S

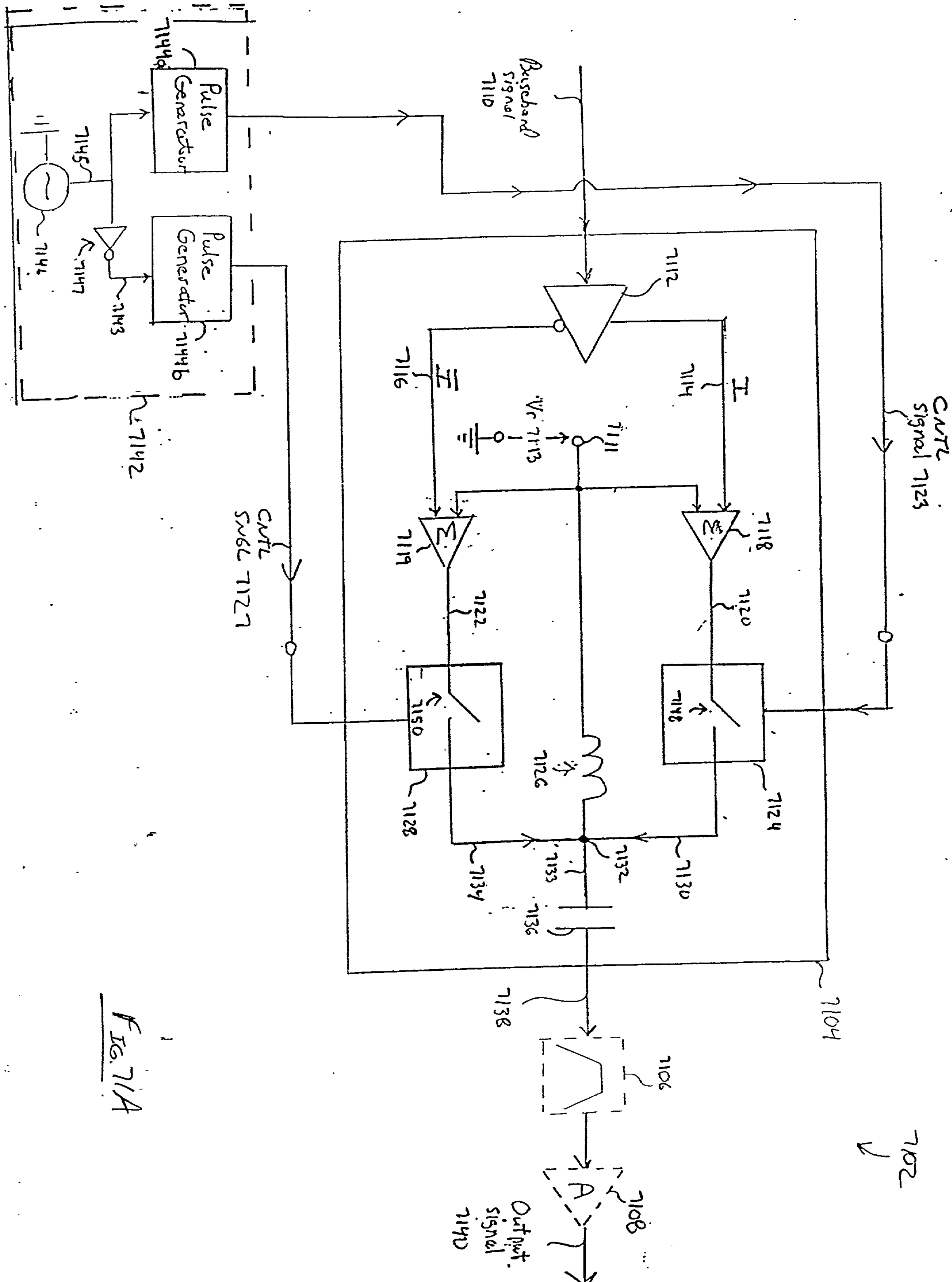

Pulse Generator
Pulse Generator
7144a
7144b
7145
7146
7147
7143
7142
Baseband signal 7110
CNTL signal 7123
CNTL SGNL 7127
7112
7116
7114
Vr 7113
7111
7119
7118
7122
7120
7150
7148
7126
7128
7124
7134
7133
7132
7130
7136
7138
7104
7106
7108
Output signal 7140
7102

FIG. 71A

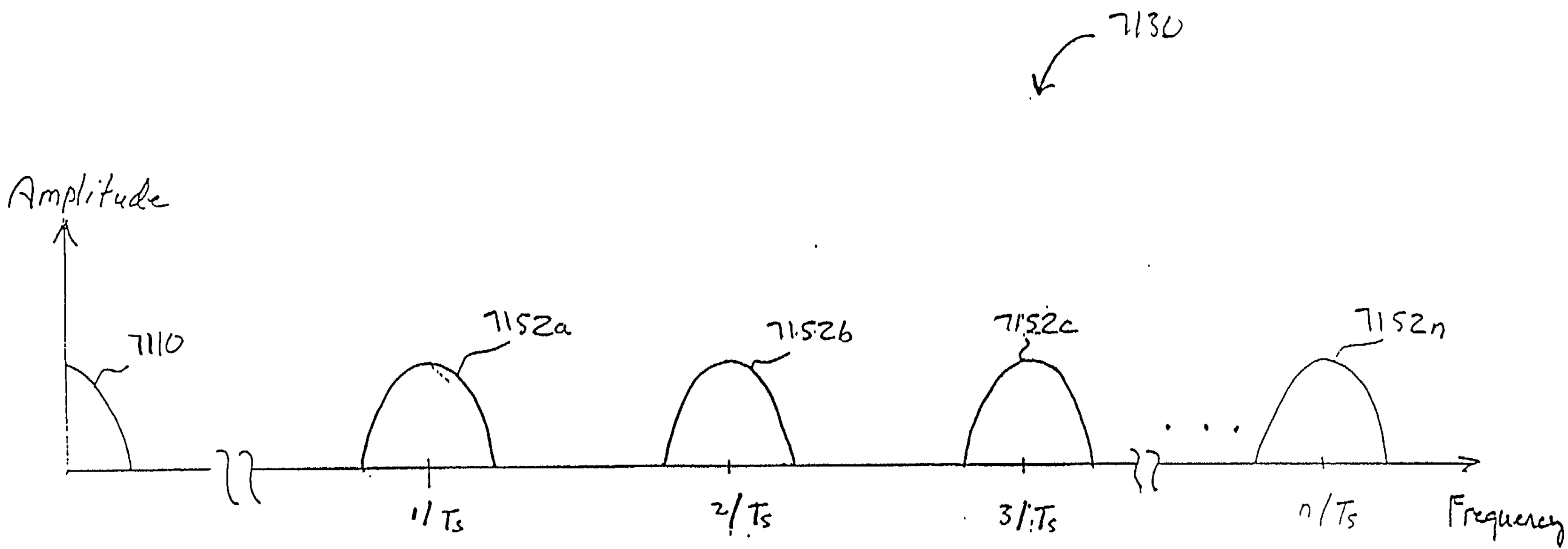

7130
Amplitude
7110
7152a
7152b
7152c
7152n
1/Ts
2/Ts
3/Ts
n/Ts
Frequency

FIG. 71B

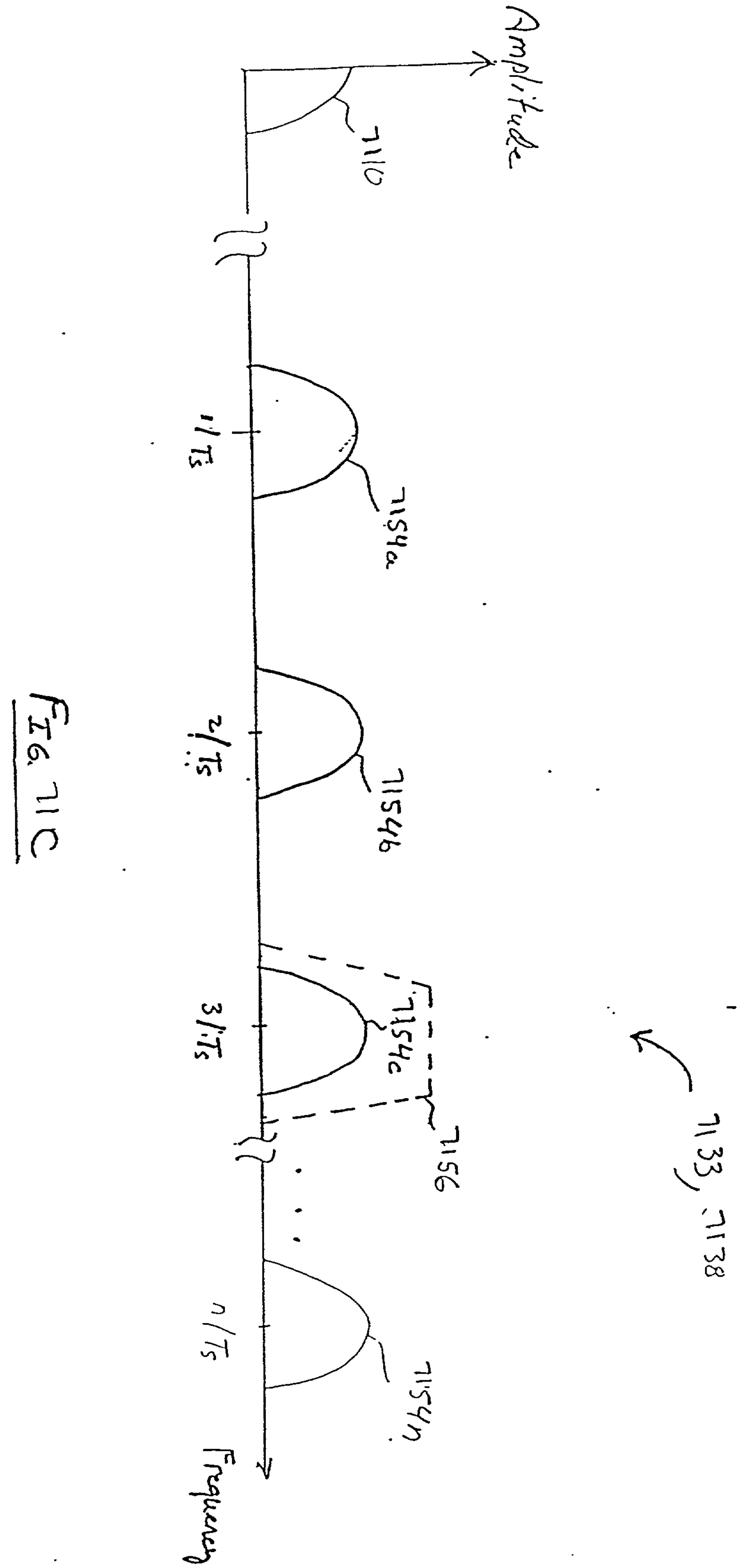

Amplitude
7110
1/Ts
7154a
2/Ts
7154b
3/Ts
7154c
7156
7133, 7138
n/Ts
7154n
Frequency

FIG. 71C

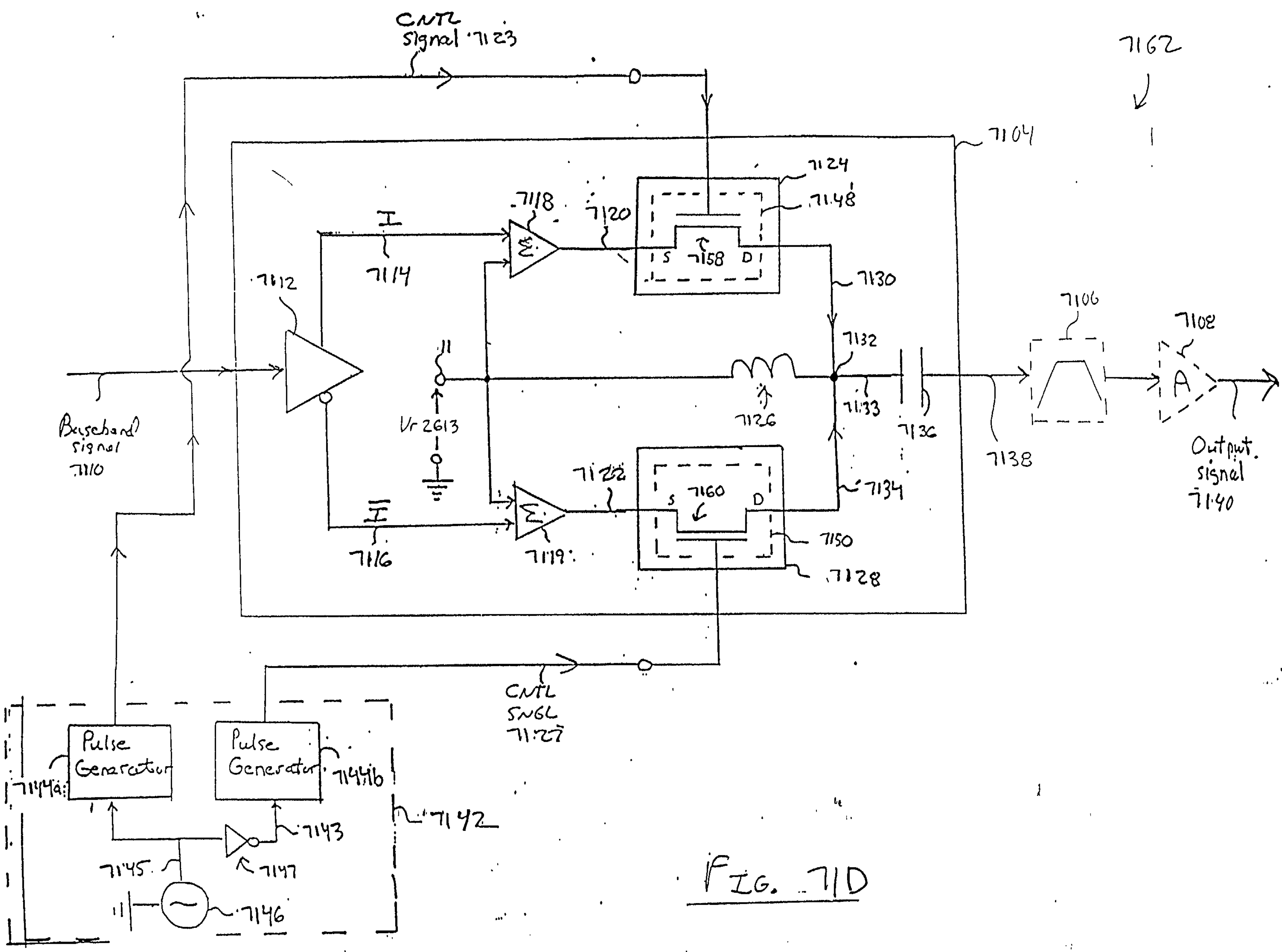

CNTL
Signal 7123
7162
7104
7124
7148
7118
7120
S
7158
D
7112
7114
7130
7106
7102
7132
A
Baseband signal 7110
Vr 2613
7126
7133
7136
7138
Output signal 7140
7122
S
7160
D
7134
7116
7119
7150
7128
CNTL SNGL 7127
Pulse Generator
Pulse Generator
7144a
7144b
7142
7145
7143
7147
7146

FIG. 71D

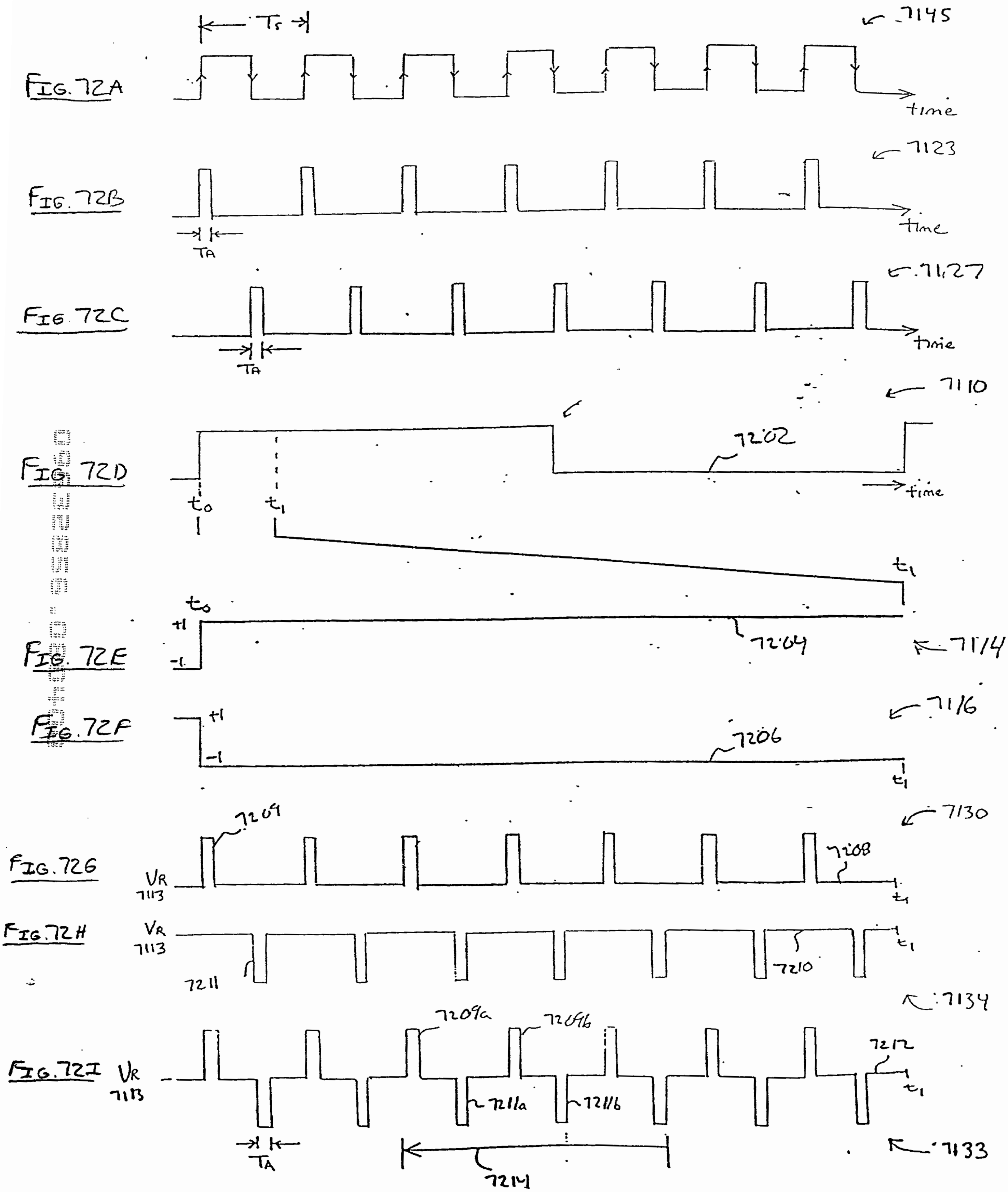


FIG. 72A
7145
T_s
time
FIG. 72B
7123
TA
time
FIG. 72C
7127
TA
time
FIG. 72D
7110
7202
t_0
t_1
time
FIG. 72E
t_0
+1
-1
7204
7114
FIG. 72F
7116
+1
-1
7206
t_1
FIG. 72G
7130
7204
7208
VR
7113
t_1
FIG. 72H
VR
7113
7211
7210
t_1
7134
FIG. 72I
VR
7113
7209a
7209b
7211a
7211b
7212
t_1
TA
7214
7133

Aperture = 500ps
Fundamental Clock = 200Mhz (5th Subharmonic)

Square Wave Frequency = 200Mhz

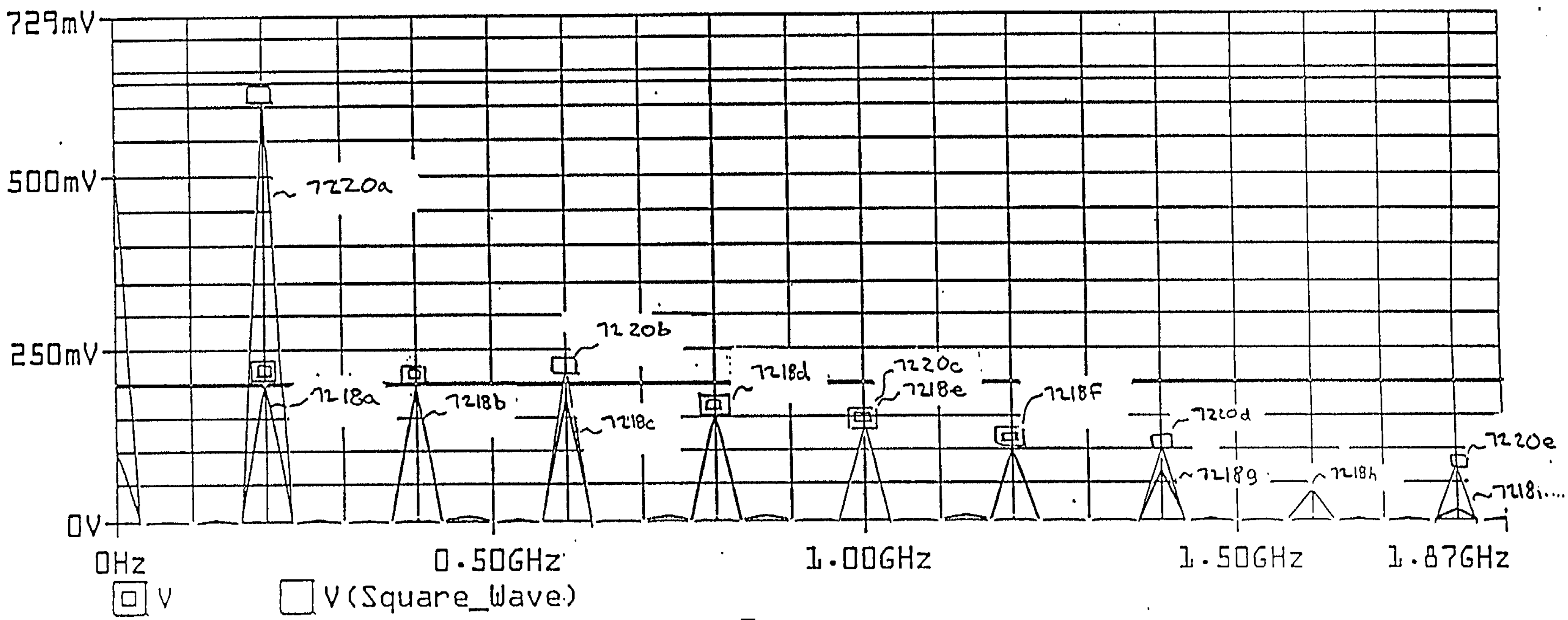


FIG. 72J

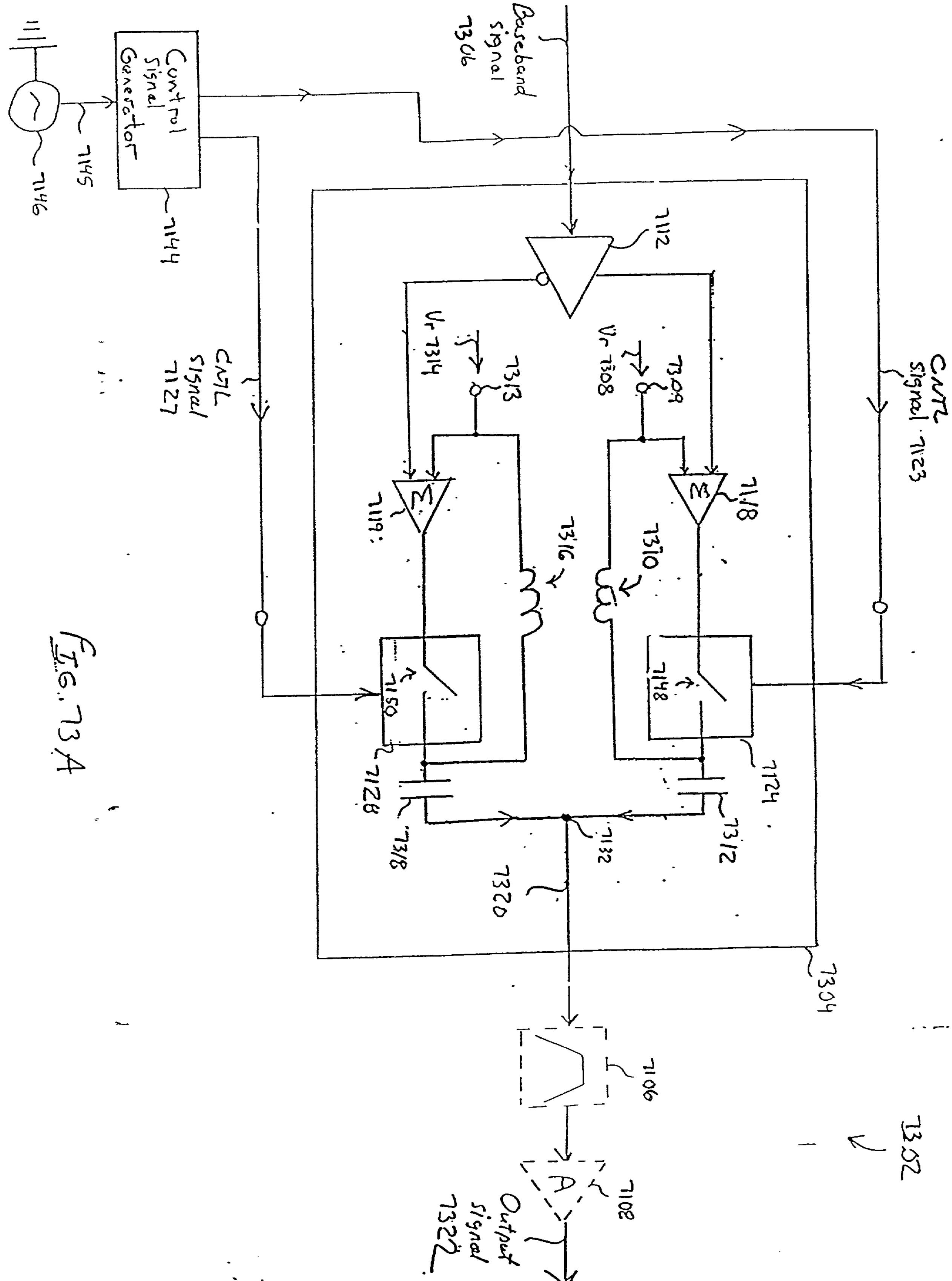
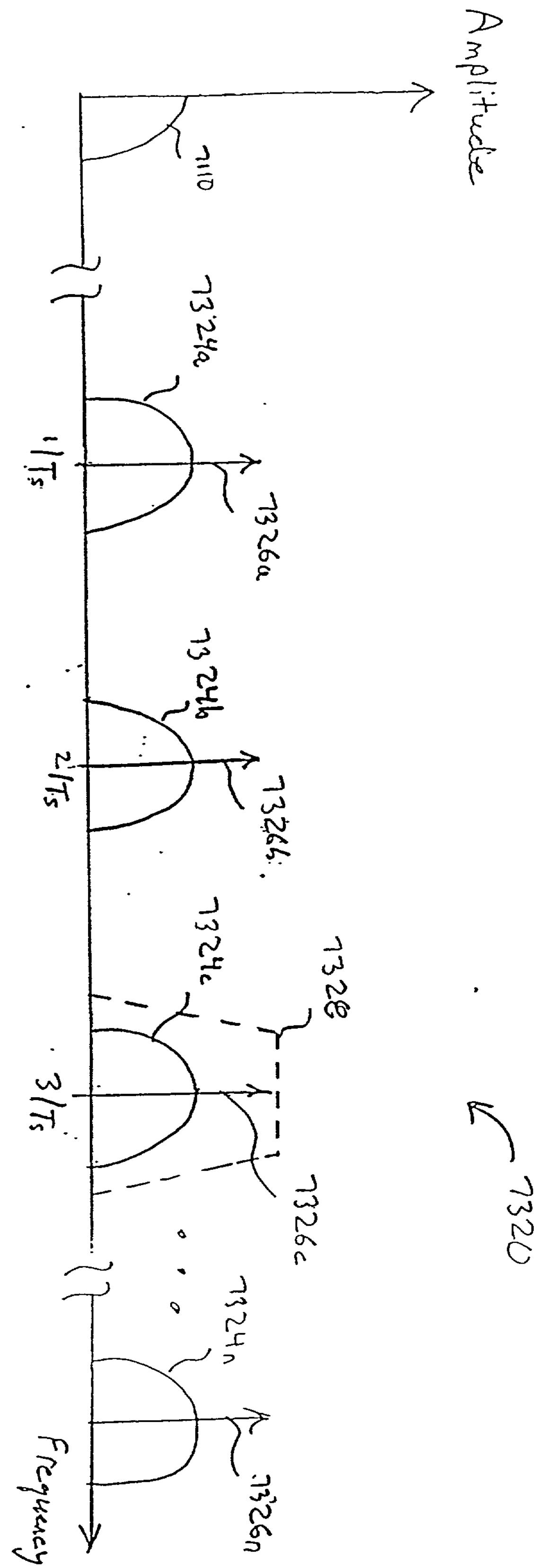

Control Signal Generator
Baseband signal 7306
CNTL signal 7123
CNTL signal 7127
Vr 7308
Vr 7314
Output signal 7322
7144
7145
7146
7112
7118
7119
7309
7310
7312
7313
7316
7318
7320
7124
7128
7132
7148
7150
7304
7106
7108
7302

FIG. 73A



Amplitude
7110
7324a
1/Ts
7326a
7324b
2/Ts
7326b
7324c
7328
3/Ts
7326c
7320
7324n
7326n
Frequency

FIG. 73B

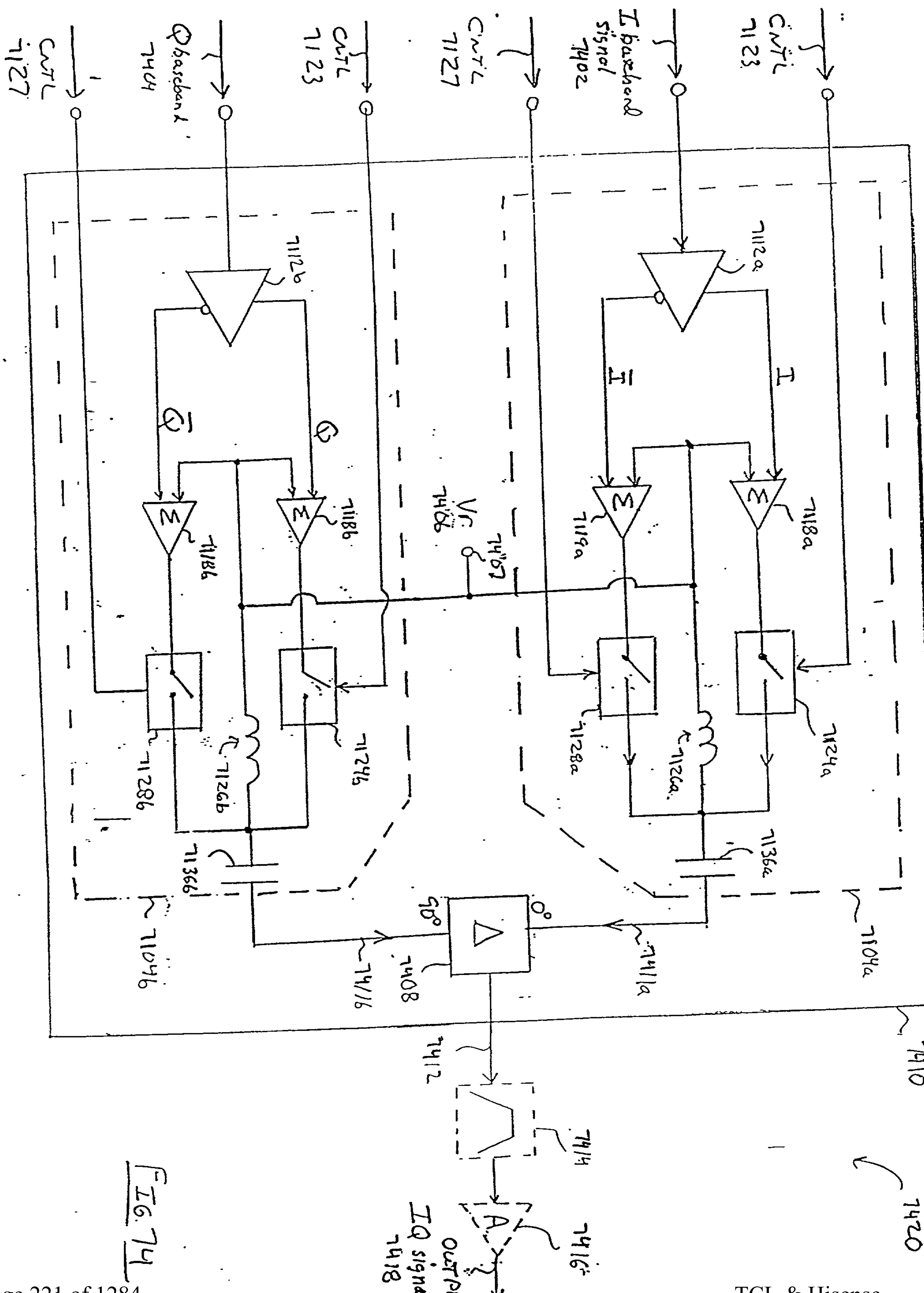

CNTL 7123
I baseband signal 7402
CNTL 7127
CNTL 7123
Q baseband 7404
CNTL 7127
7112a
7112b
7118a
7119a
7118b
7119b
Vr 7406
7124a
7128a
7126a
7136a
7124b
7128b
7126b
7136b
7104a
7104b
7411a
7416
7408
7410
7412
7414
7416
7420
OUTPUT IQ signal 7418

FIG. 74

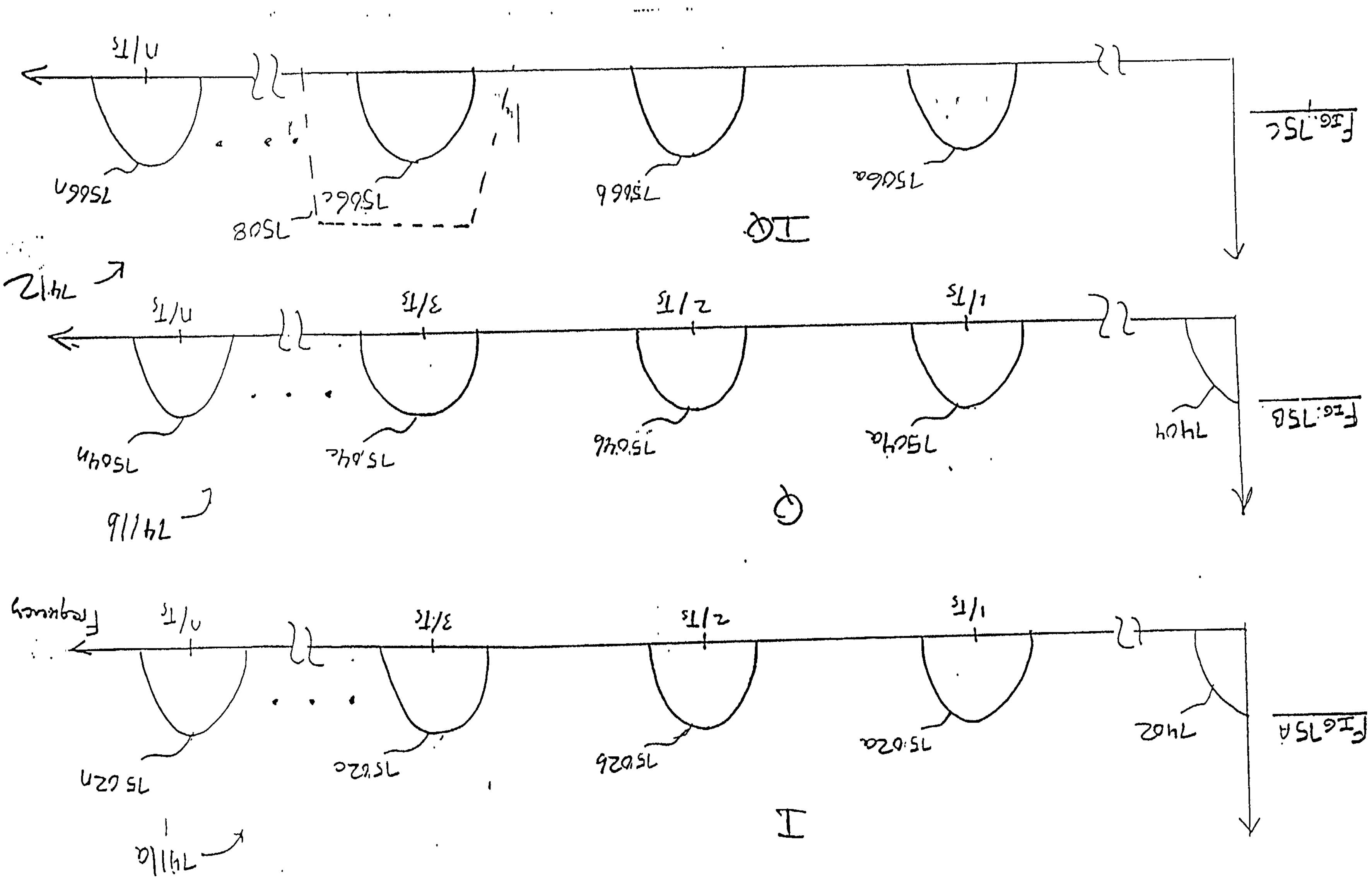


FIG 75A
I
7402
7502a
7502b
7502c
7502n
7411a
1/Ts
2/Ts
3/Ts
n/Ts
Frequency
FIG. 75B
Q
7404
7504a
7504b
7504c
7504n
7411b
1/Ts
2/Ts
3/Ts
n/Ts
7412
FIG. 75C
IQ
7506a
7506b
7506c
7506n
7508
n/Ts

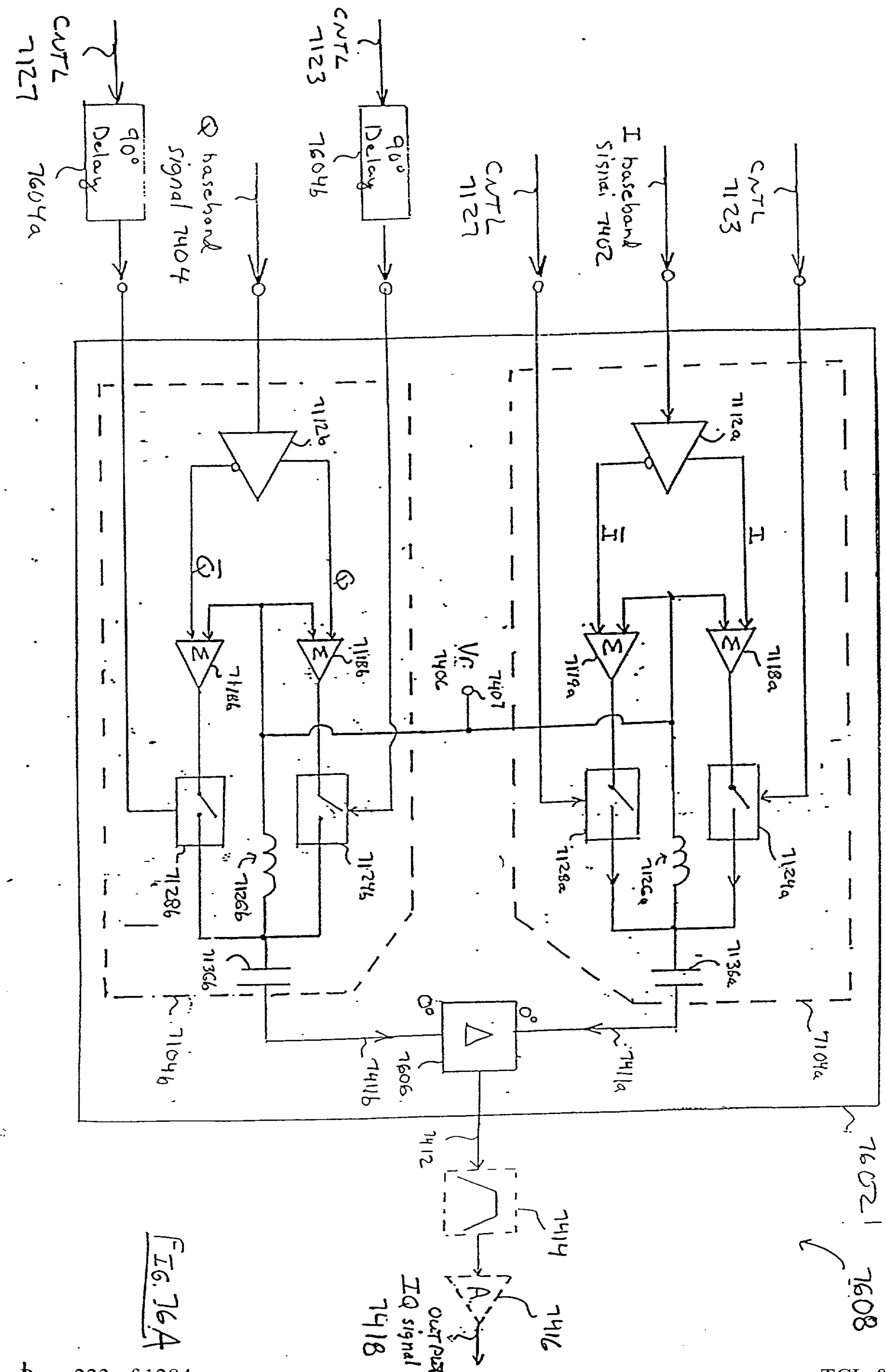
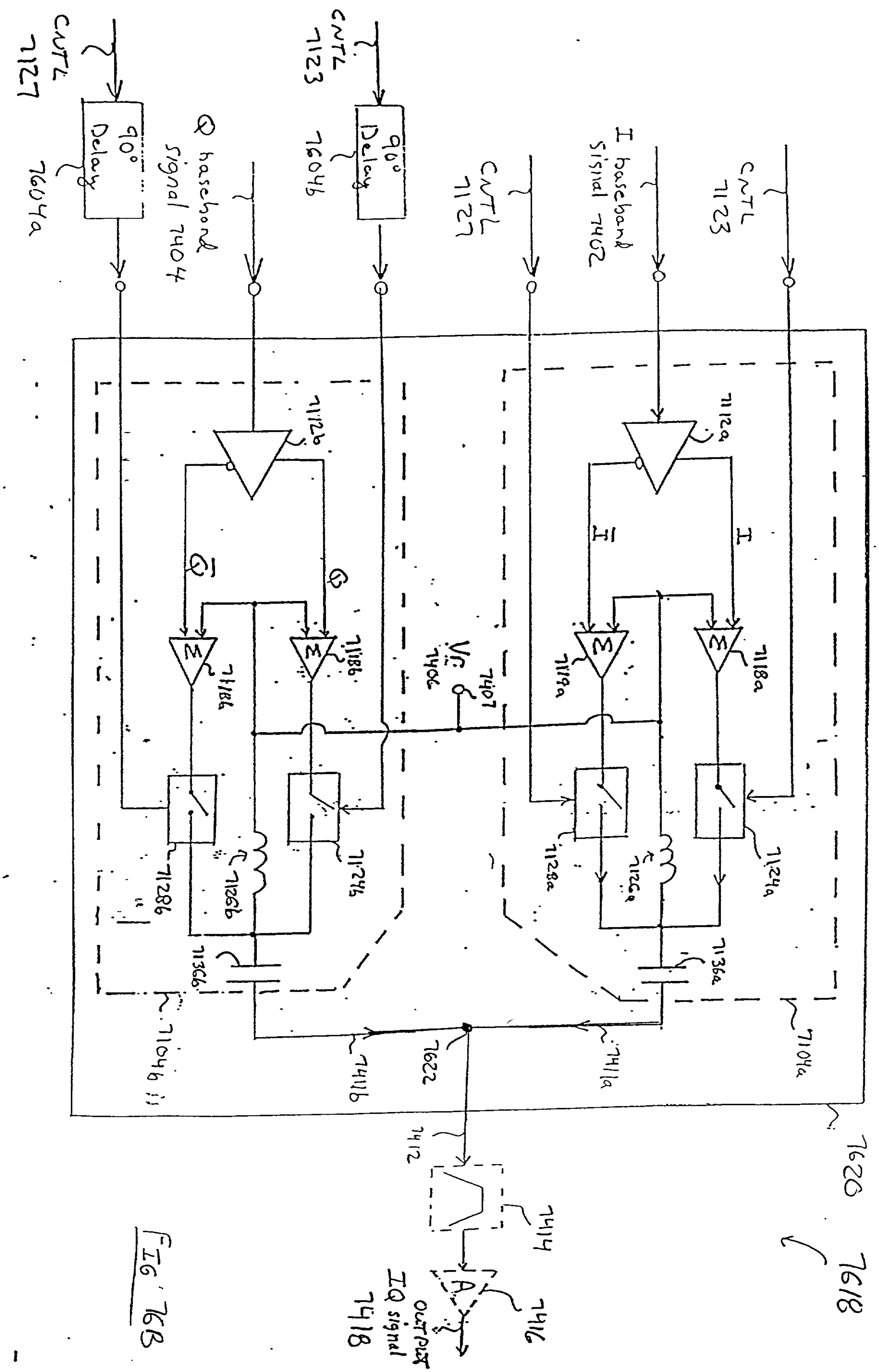

CNTL 7127
90° Delay
7604a
Q baseband signal 7404
CNTL 7123
90° Delay
7604b
CNTL 7127
I baseband signal 7402
CNTL 7123
7112a
7112b
I
I
Q
Q
7118a
7119a
7118b
7119b
Vr 7407
7406
7124a
7128a
7126a
7124b
7128b
7126b
7136a
7136b
7104a
7104b
0°
0°
7411a
7411b
7606
7602
7412
7414
7416
Output IQ signal
7418
7608

FIG. 76A



CNTL 7127
CNTL 7123
90° Delay 7604a
90° Delay 7604b
Q baseband signal 7404
I baseband signal 7402
CNTL 7127
CNTL 7123
7112a
7112b
I
Ī
Q
Q̄
M 7118a
M 7119a
M 7118b
M 7119b
Vr 7406
7407
7124a
7128a
7126a
7124b
7128b
7126b
7136a
7136b
7104a
7104b
7411a
7411b
7622
7620
7412
7414
A 7416
OUTPUT IQ signal 7418
7618

FIG 76B

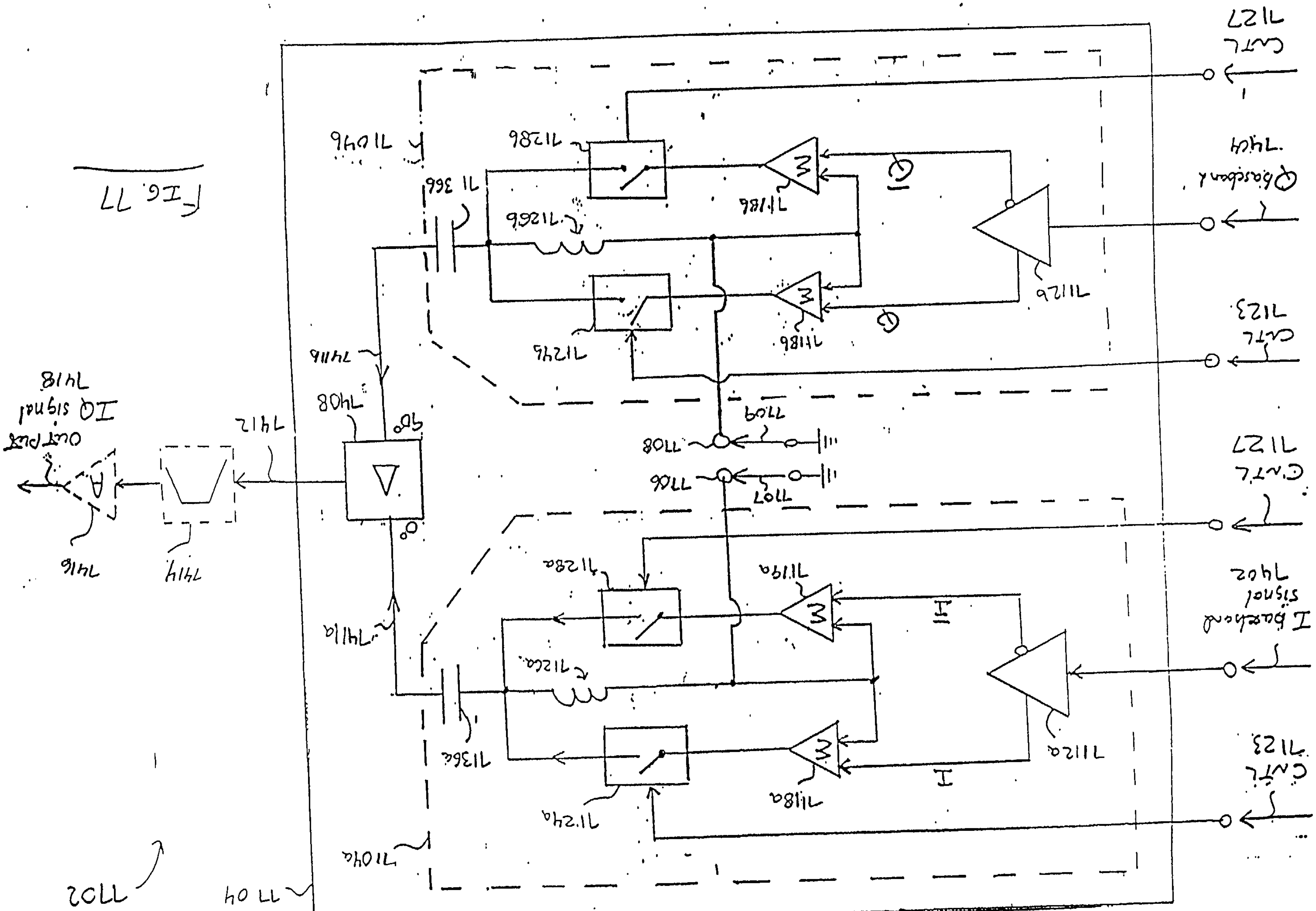

CNTL 7127
Q baseband 7404
CNTL 7123
I baseband signal 7402
IQ signal output 7418
7702
7704

FIG. 77

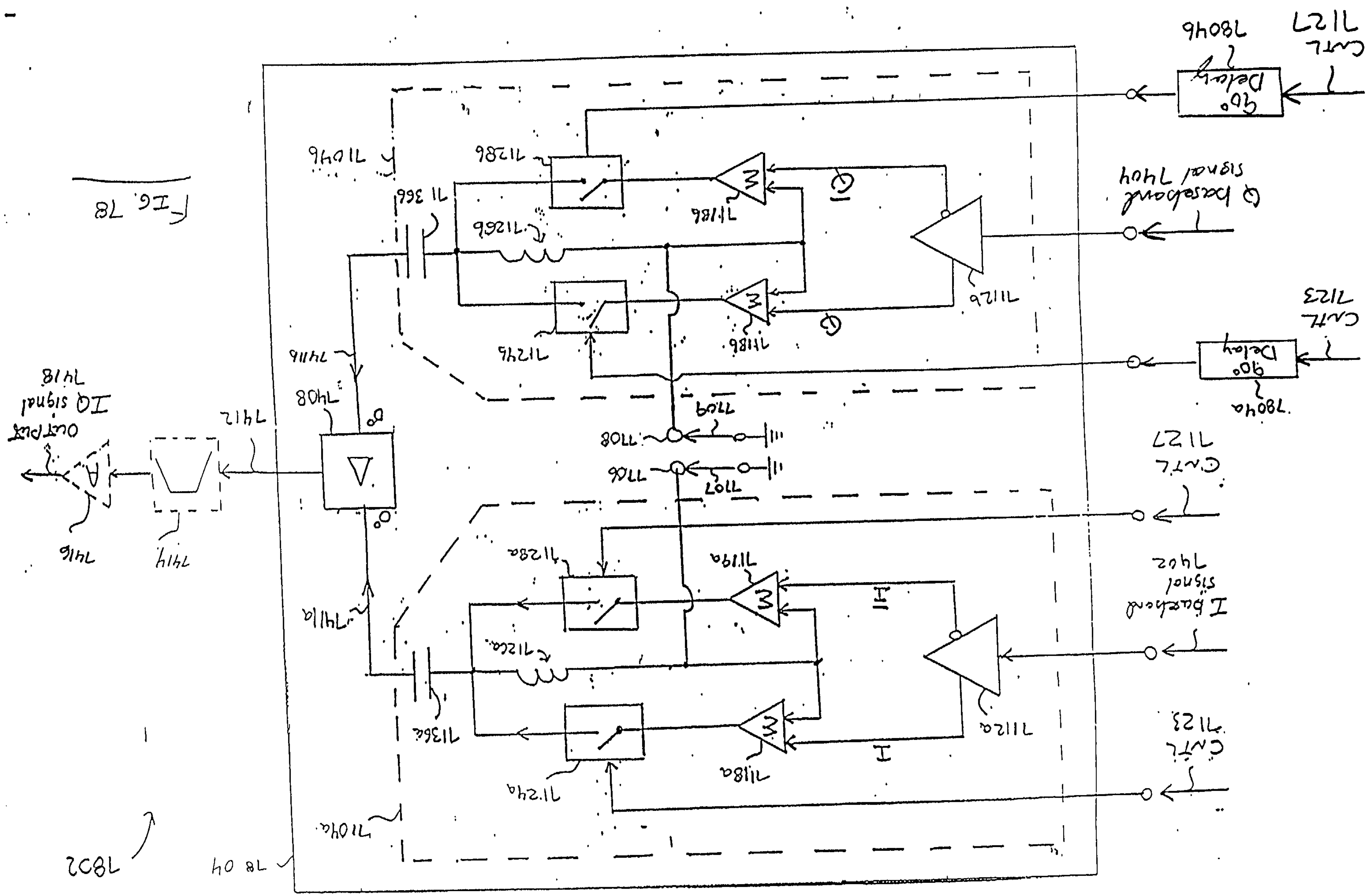

CNTL
7127
7804b
90° Delay
Q baseband signal 7404
CNTL
7123
7804a
I baseband signal 7402
OUTPUT
IQ signal
7418
7412
7408
7414
7416
7106
7108
7802
7804

FIG. 78

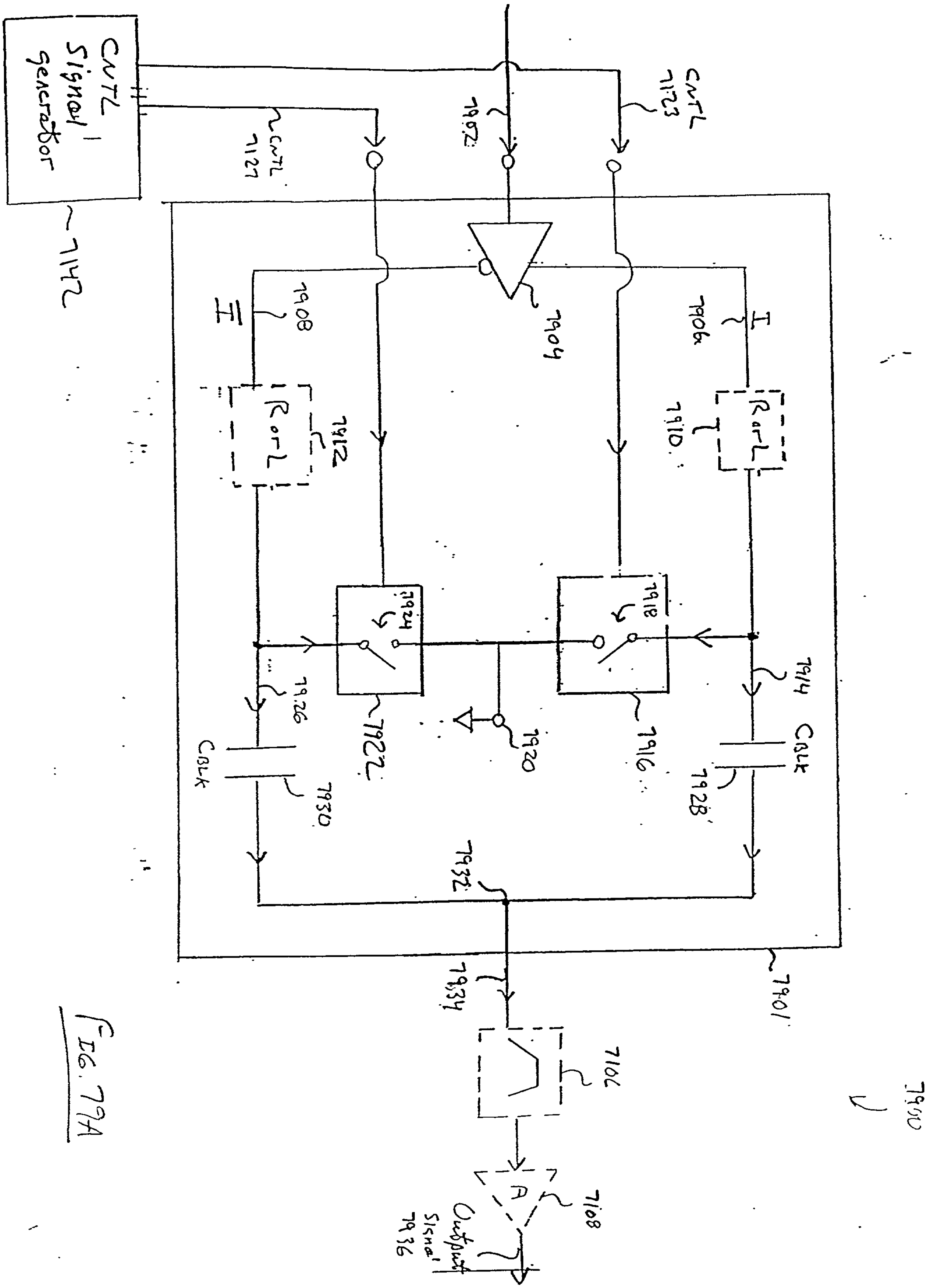

CNTL Signal Generator
7142
CNTL 7127
7902
CNTL 7123
7904
7908
7906
R or L
7912
R or L
7910
7924
7918
7914
7926
7922
7920
7916
CBLK
7930
CBLK
7928
7932
7901
7934
7106
A
7108
Output Signal 7936
7900

FIG. 79A

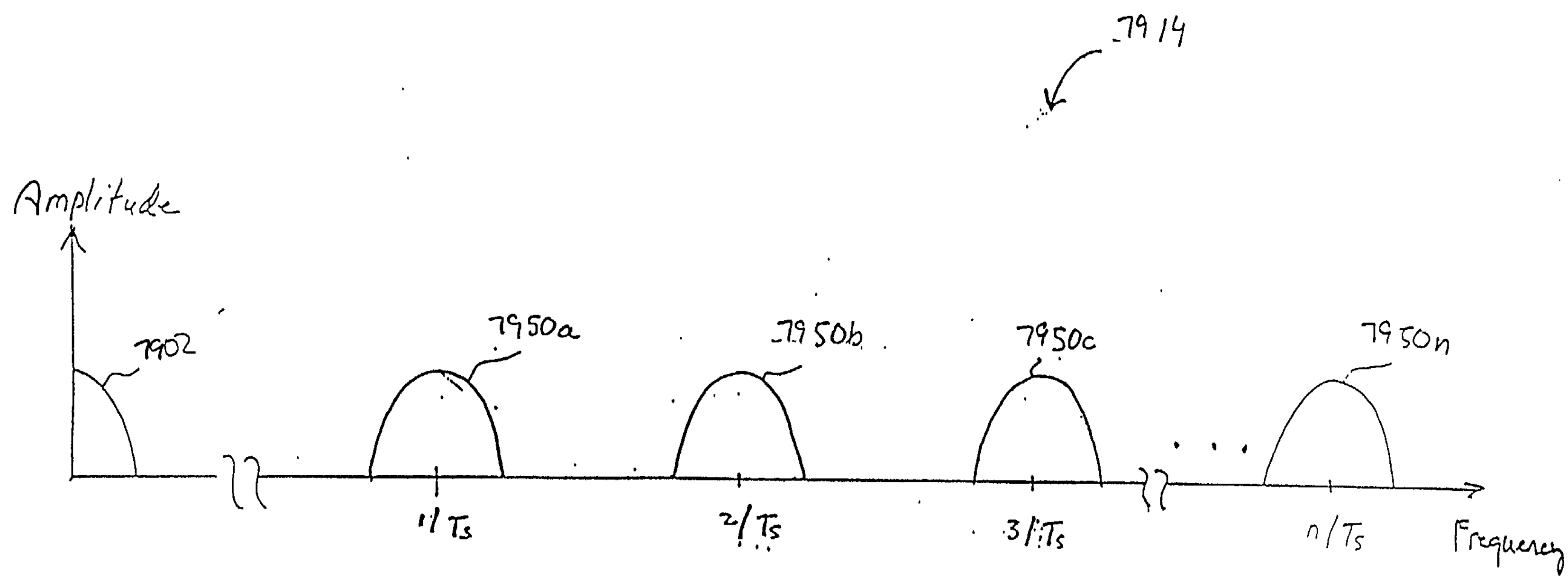


FIG. 79B

09632556 .080400

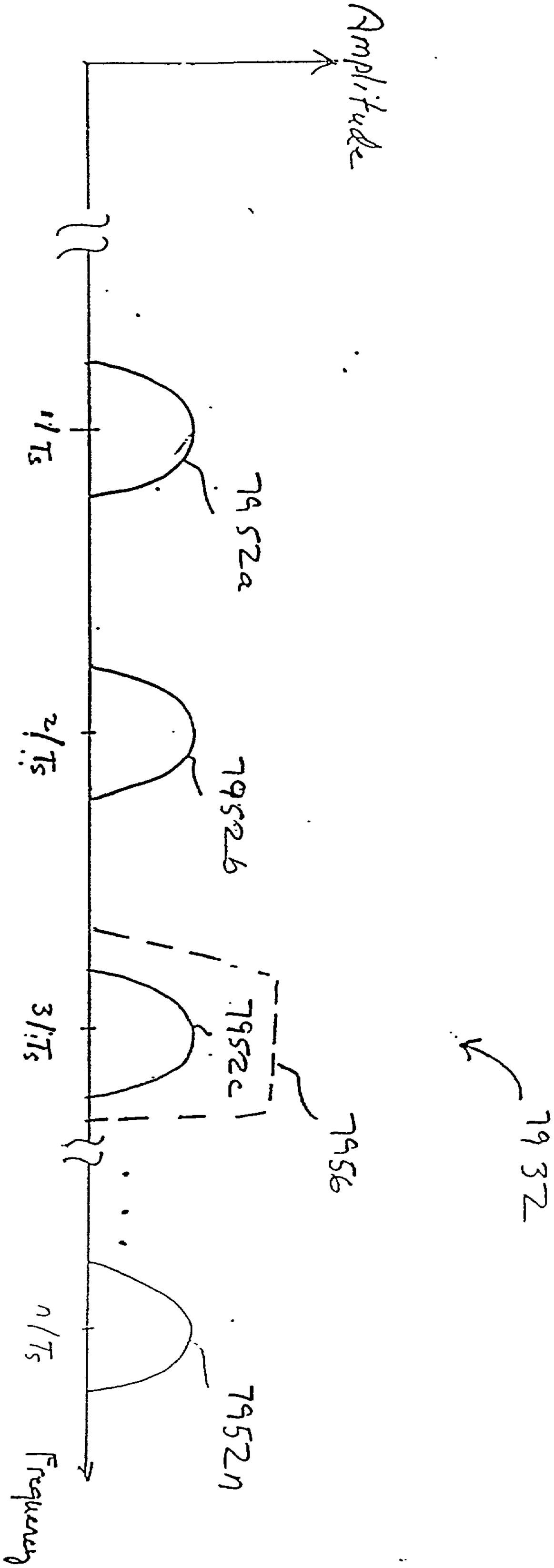

Amplitude
1/Ts
7952a
2/Ts
7952b
3/Ts
7952c
7956
7932
n/Ts
7952n
Frequency

FIG. 79c

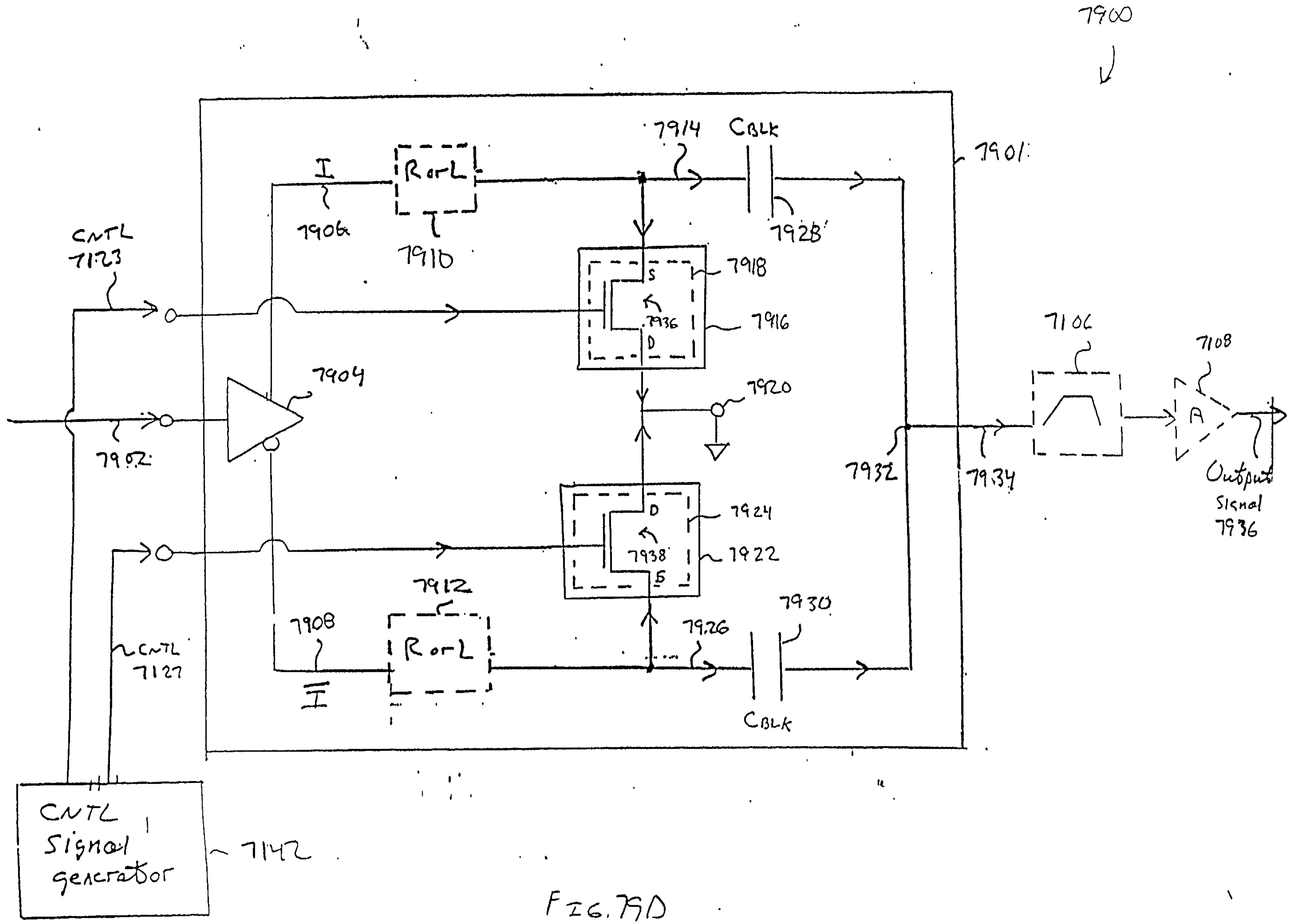

7900
7901
CBLK
7914
I
R or L
7906
7910
7928
CNTL
7123
7918
7936
7916
S
D
7106
7108
7904
7920
A
7902
7932
7934
Output Signal 7936
D
7924
7938
7922
S
7912
7930
7908
7926
CNTL 7127
R or L
I
CBLK
CNTL Signal generator
7142

FIG. 79D

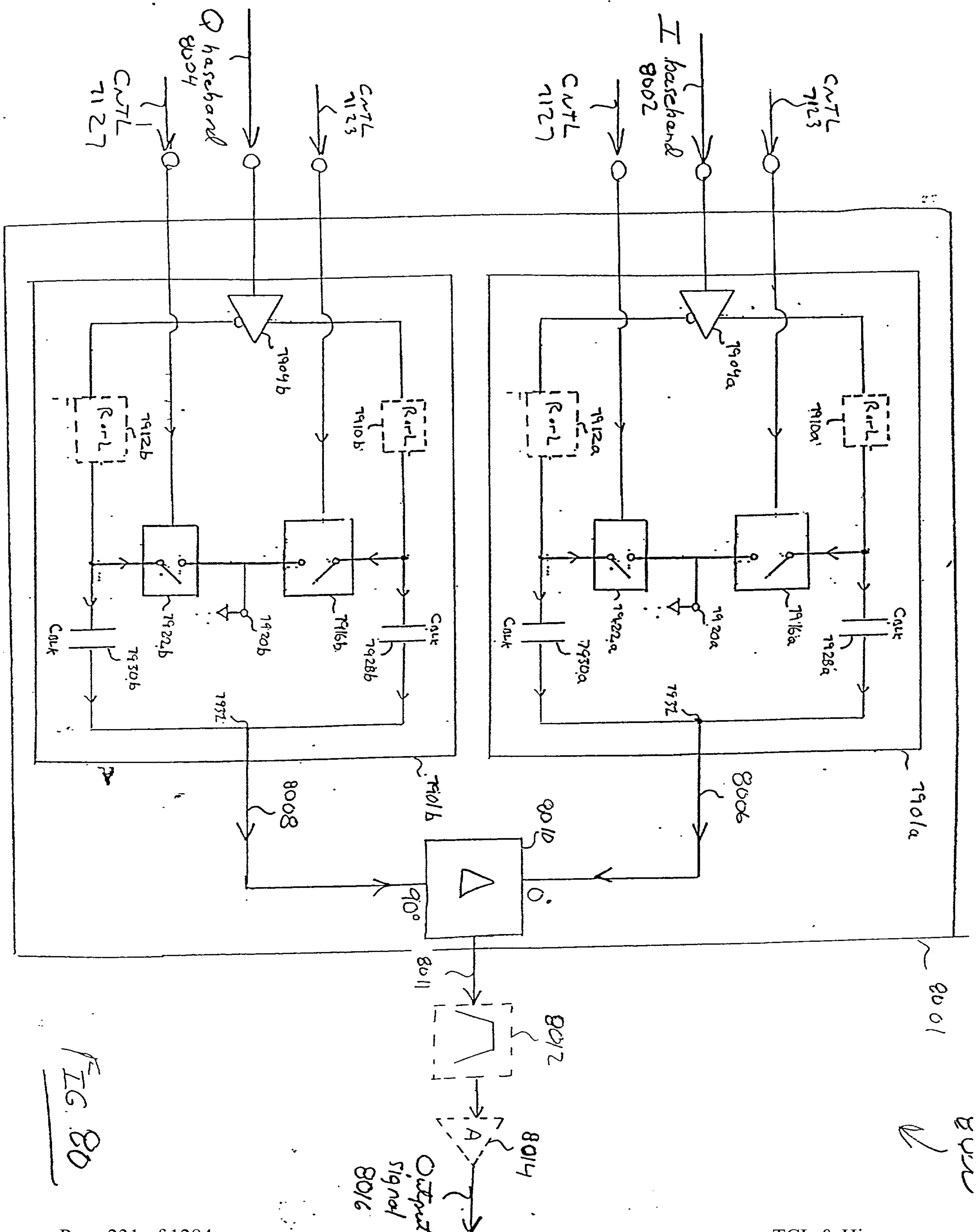

Q baseband 8004
CNTL 7127
CNTL 7123
I baseband 8002
CNTL 7127
CNTL 7123
7904a
7904b
R or L
7910a
7912a
7910b
7912b
7916a
7922a
7920a
7916b
7922b
7920b
CLLK
7928a
7930a
7928b
7930b
7932
7901a
7901b
8006
8008
8010
0°
90°
A
8011
8012
8014
8001
Output signal 8016

FIG. 80

FIG. 81A

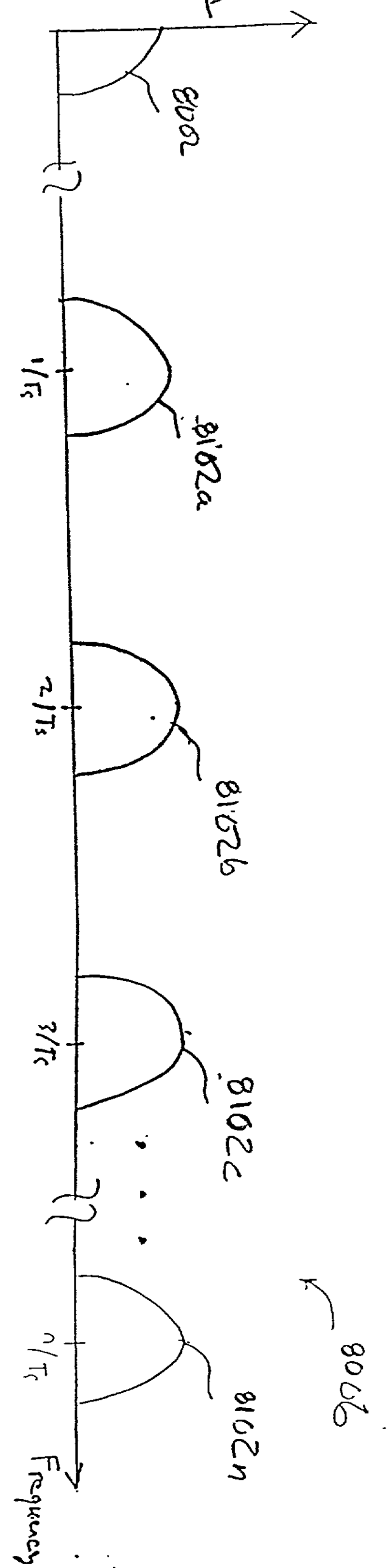


FIG. 81B

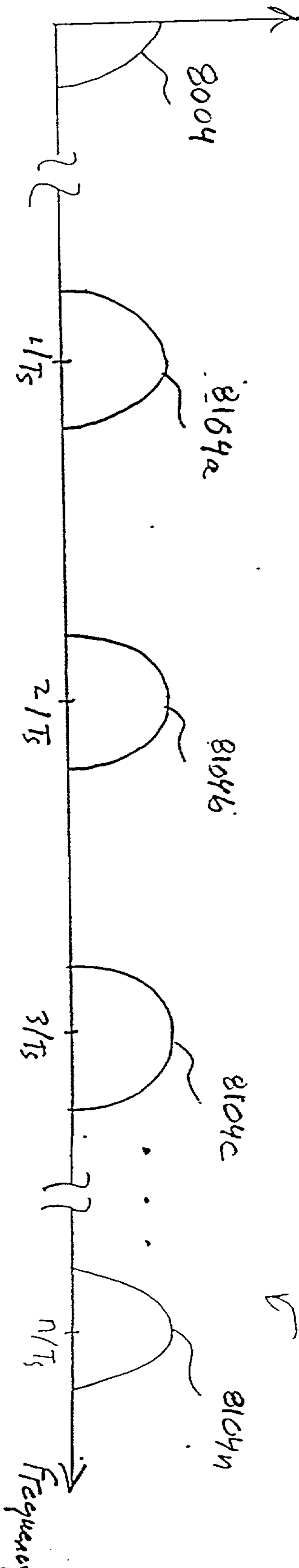
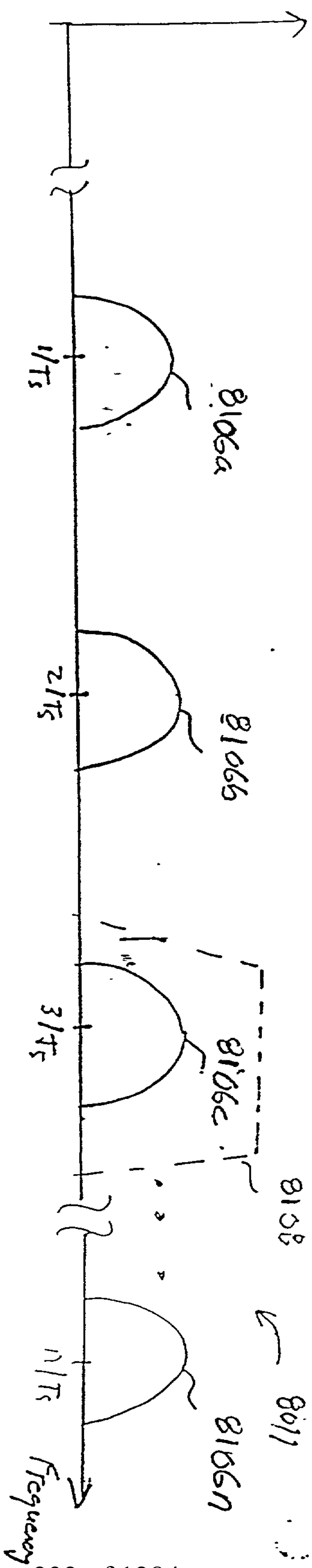


FIG. 81C



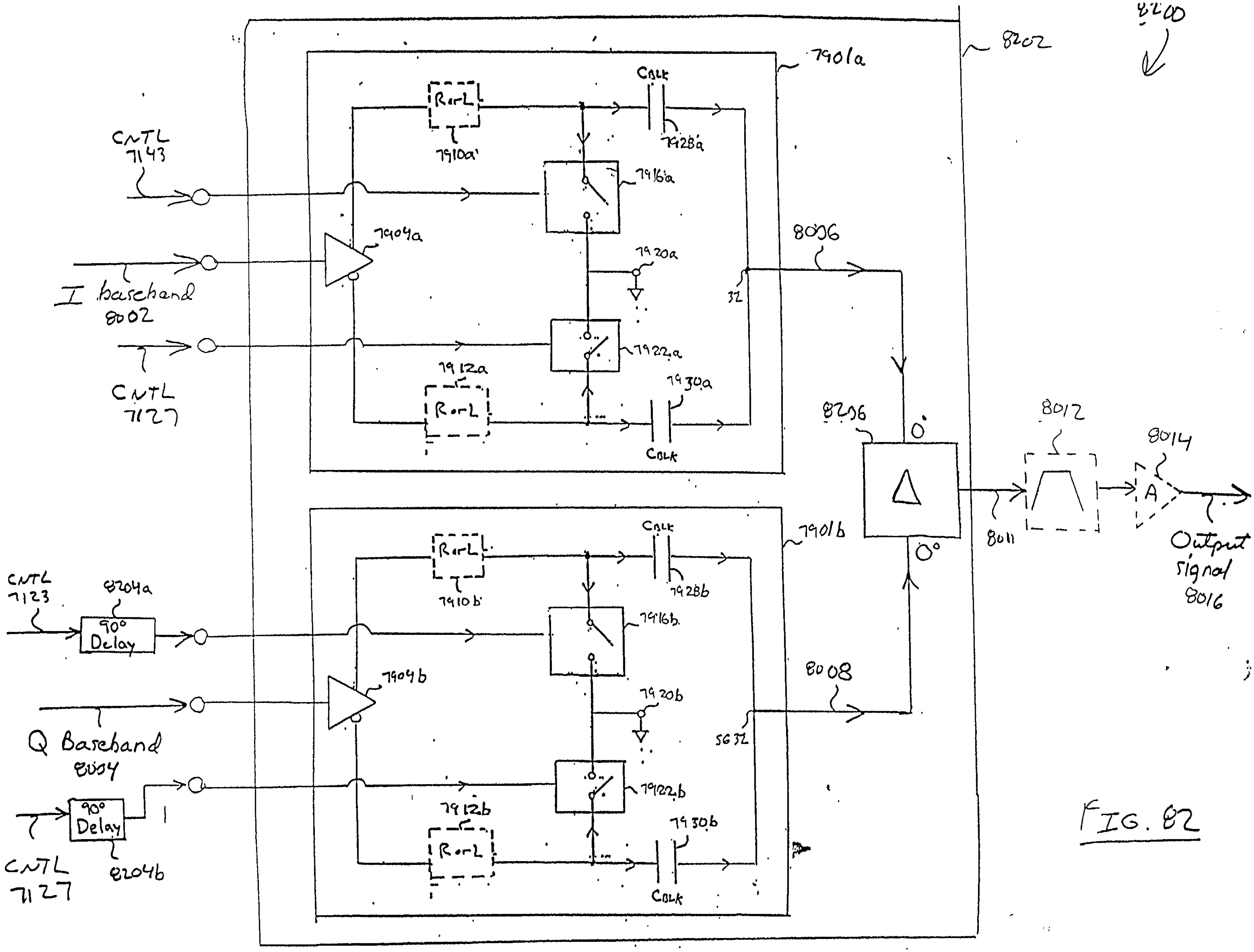
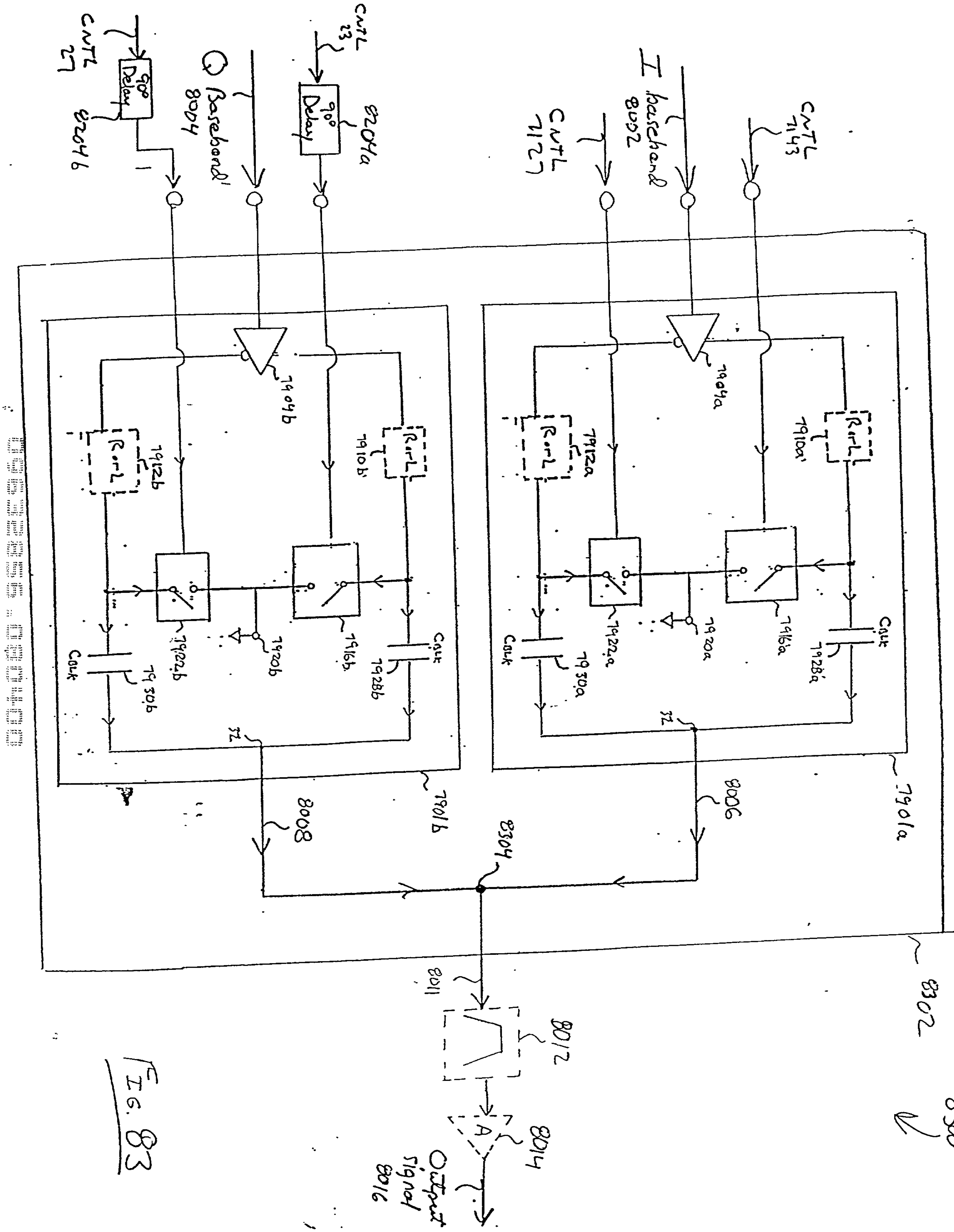

8200
8202
7901a
CNTL
7143
I baseband
8002
CNTL
7127
R or L
7910a'
CBLK
7928a
7916a
7904a
7920a
7922a
7912a
R or L
7930a
CBLK
32
8006
8206
0°
Δ
0°
8011
8012
8014
A
Output
signal
8016
7901b
CNTL
7123
8204a
90°
Delay
Q Baseband
8004
90°
Delay
CNTL
7127
8204b
R or L
7910b'
CBLK
7928b
7916b
7904b
7920b
7922b
7912b
R or L
7930b
CBLK
5632
8008

FIG. 82



CNTL 27
90° Delay
8204b
Q baseband 8004
CNTL 23
90° Delay
8204a
CNTL 7127
I baseband 8002
CNTL 7143
7904b
7904a
R or L
7912b
7910b
7912a
7910a
7922b
7920b
7916b
7922a
7920a
7916a
Cblk
7930b
7928b
7930a
7928a
7901b
7901a
8008
8006
8304
8302
8011
8012
8014
A
Output Signal 8016
8300

FIG. 83

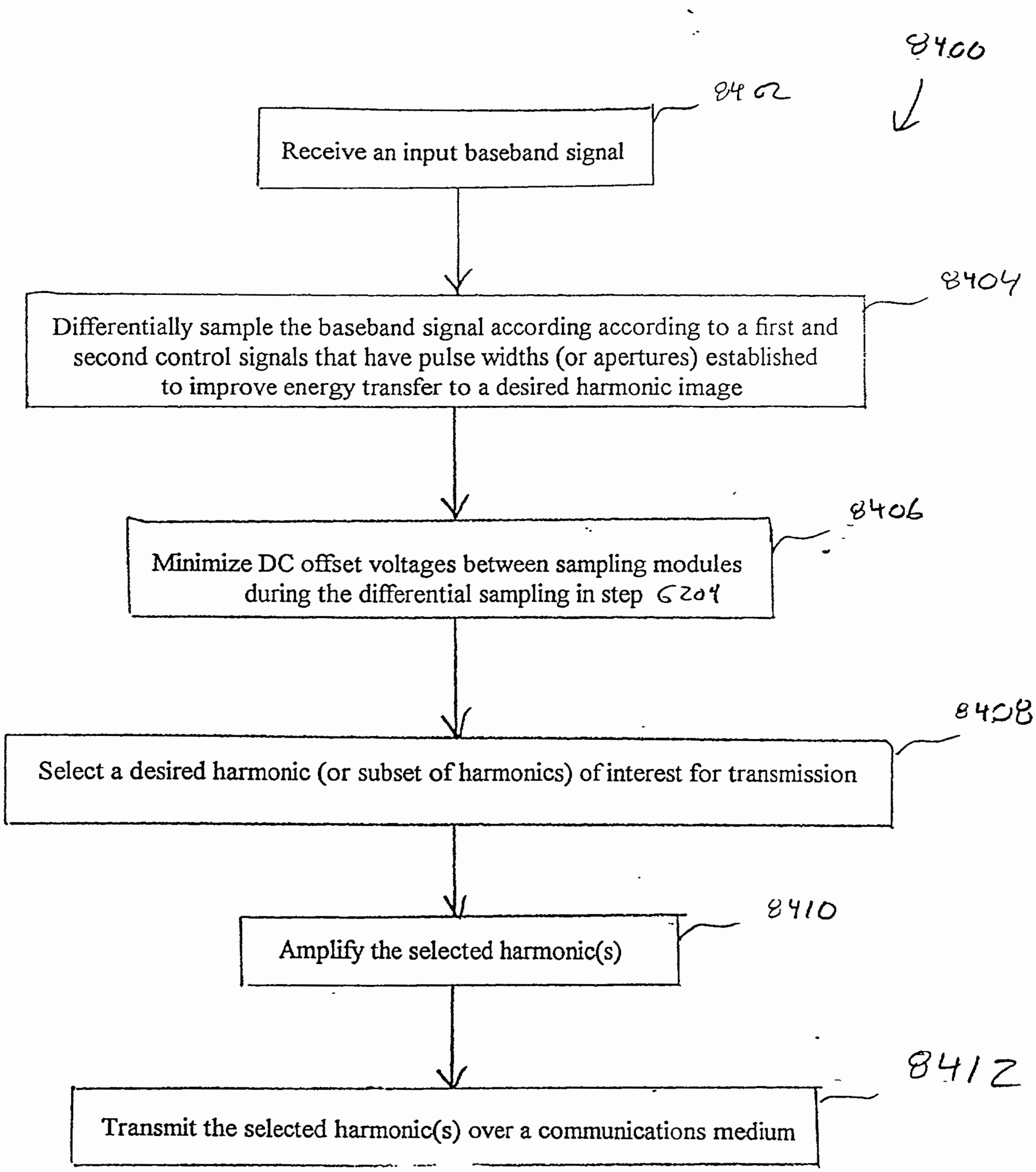

8400
8402
Receive an input baseband signal
8404
Differentially sample the baseband signal according according to a first and second control signals that have pulse widths (or apertures) established to improve energy transfer to a desired harmonic image
8406
Minimize DC offset voltages between sampling modules during the differential sampling in step 6204
8408
Select a desired harmonic (or subset of harmonics) of interest for transmission
8410
Amplify the selected harmonic(s)
8412
Transmit the selected harmonic(s) over a communications medium

FIG. 84

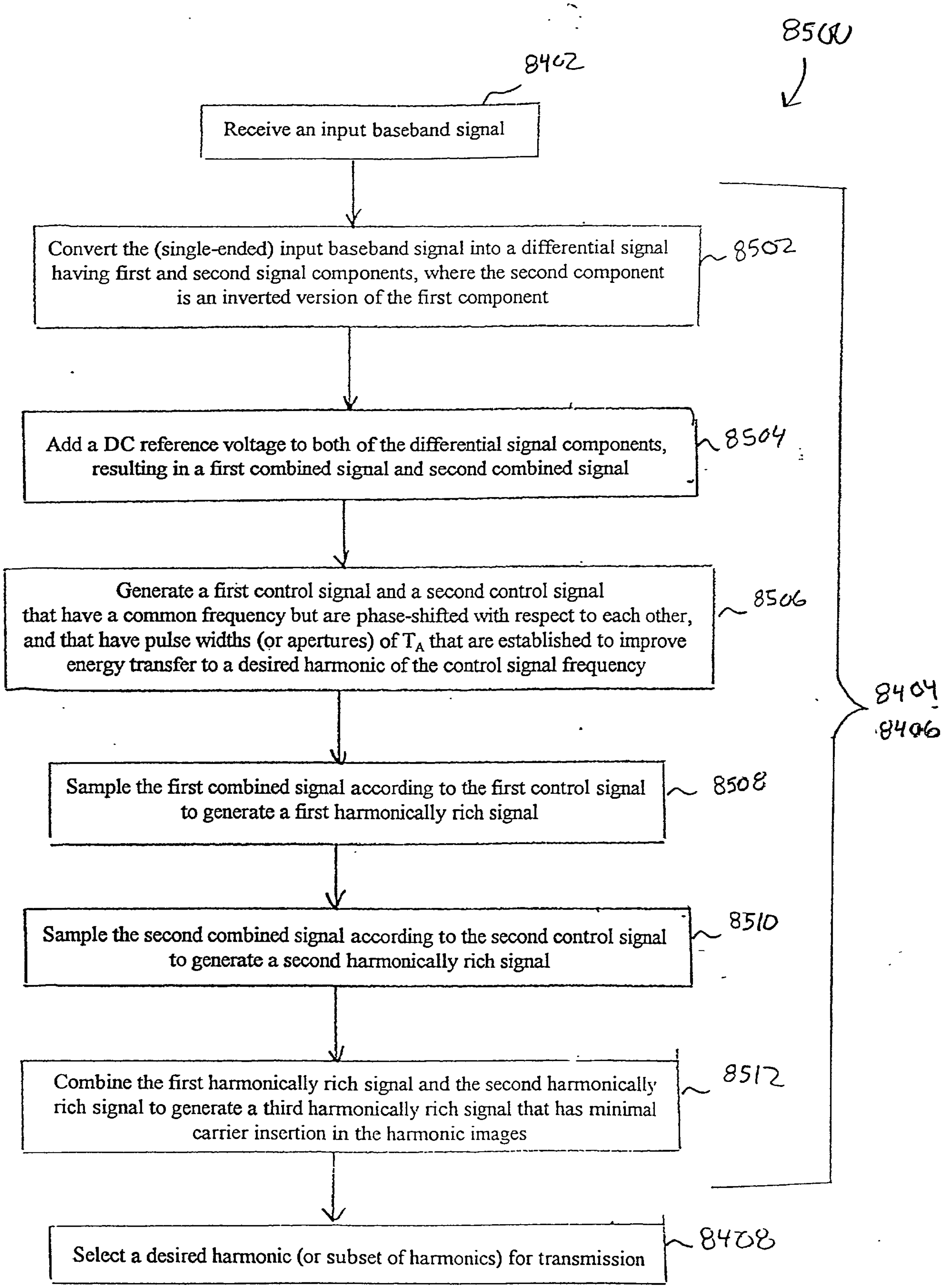

8500
8402
Receive an input baseband signal
Convert the (single-ended) input baseband signal into a differential signal having first and second signal components, where the second component is an inverted version of the first component
8502
Add a DC reference voltage to both of the differential signal components, resulting in a first combined signal and second combined signal
8504
Generate a first control signal and a second control signal that have a common frequency but are phase-shifted with respect to each other, and that have pulse widths (or apertures) of T_A that are established to improve energy transfer to a desired harmonic of the control signal frequency
8506
8404
8406
Sample the first combined signal according to the first control signal to generate a first harmonically rich signal
8508
Sample the second combined signal according to the second control signal to generate a second harmonically rich signal
8510
Combine the first harmonically rich signal and the second harmonically rich signal to generate a third harmonically rich signal that has minimal carrier insertion in the harmonic images
8512
Select a desired harmonic (or subset of harmonics) for transmission
8408

FIG. 85

8600

Receive an input baseband signal 8402

Convert the (single-ended) input baseband signal into a differential signal having first and second signal components, where the second component is an inverted version of the first component 8602

Generate a first control signal and a second control signal that have a common frequency but are phase-shifted with respect to each other, and that have pulse widths (or apertures) of T_A that are established to improve energy transfer to a desired harmonic of the control signal frequency 8604

Shunt the first differential signal component to ground according to the first control signal to generate a first harmonically rich signal 8606

Shunt the second differential signal component to ground according to the second control signal to generate a second harmonically rich signal 8608

Combine the first harmonically rich signal and the second harmonically rich signal to generate a third harmonically rich signal that has minimal carrier insertion in the harmonic images 8610

8404, 8406

Select a desired harmonic (or subset of harmonics) for transmission 8408

FIG. 86

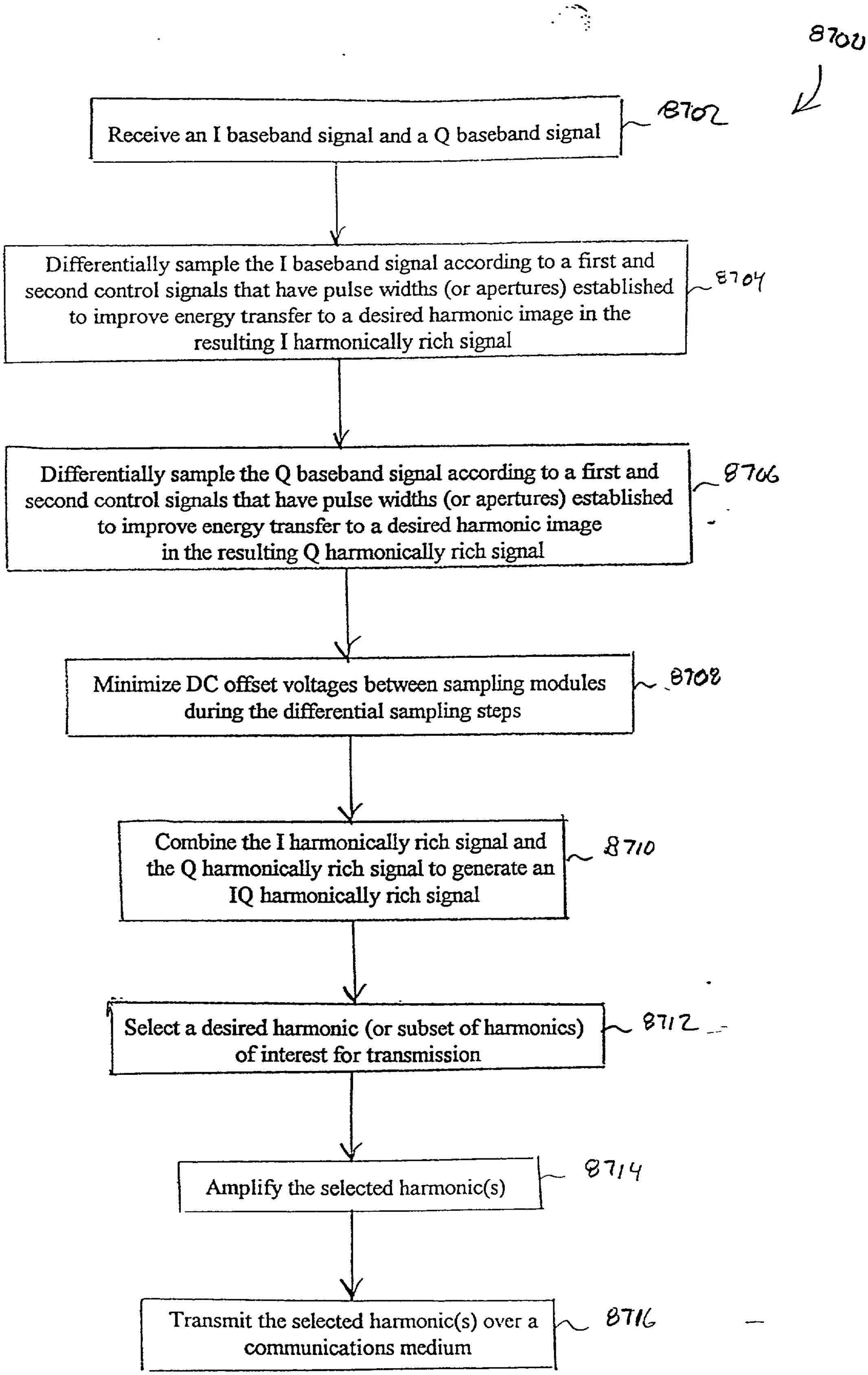

8700
Receive an I baseband signal and a Q baseband signal
8702
Differentially sample the I baseband signal according to a first and second control signals that have pulse widths (or apertures) established to improve energy transfer to a desired harmonic image in the resulting I harmonically rich signal
8704
Differentially sample the Q baseband signal according to a first and second control signals that have pulse widths (or apertures) established to improve energy transfer to a desired harmonic image in the resulting Q harmonically rich signal
8706
Minimize DC offset voltages between sampling modules during the differential sampling steps
8708
Combine the I harmonically rich signal and the Q harmonically rich signal to generate an IQ harmonically rich signal
8710
Select a desired harmonic (or subset of harmonics) of interest for transmission
8712
Amplify the selected harmonic(s)
8714
Transmit the selected harmonic(s) over a communications medium
8716

FIG. 87

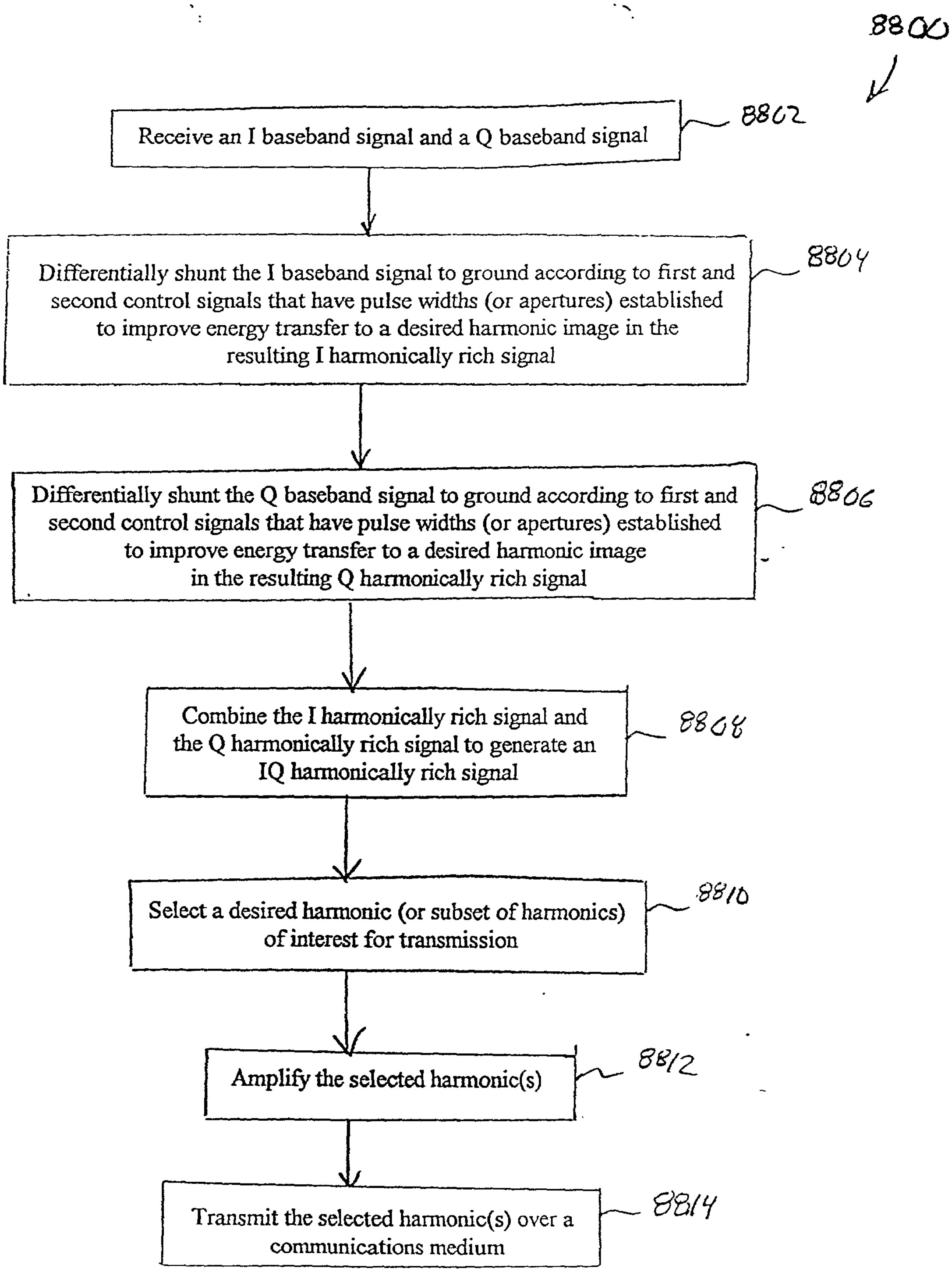

8800
Receive an I baseband signal and a Q baseband signal
8802
Differentially shunt the I baseband signal to ground according to first and second control signals that have pulse widths (or apertures) established to improve energy transfer to a desired harmonic image in the resulting I harmonically rich signal
8804
Differentially shunt the Q baseband signal to ground according to first and second control signals that have pulse widths (or apertures) established to improve energy transfer to a desired harmonic image in the resulting Q harmonically rich signal
8806
Combine the I harmonically rich signal and the Q harmonically rich signal to generate an IQ harmonically rich signal
8808
Select a desired harmonic (or subset of harmonics) of interest for transmission
8810
Amplify the selected harmonic(s)
8812
Transmit the selected harmonic(s) over a communications medium
8814

FIG. 88

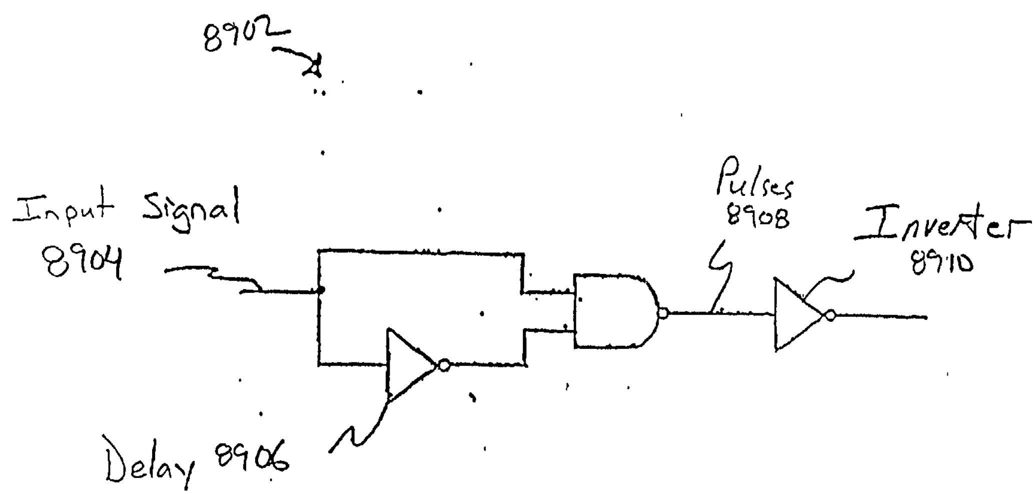
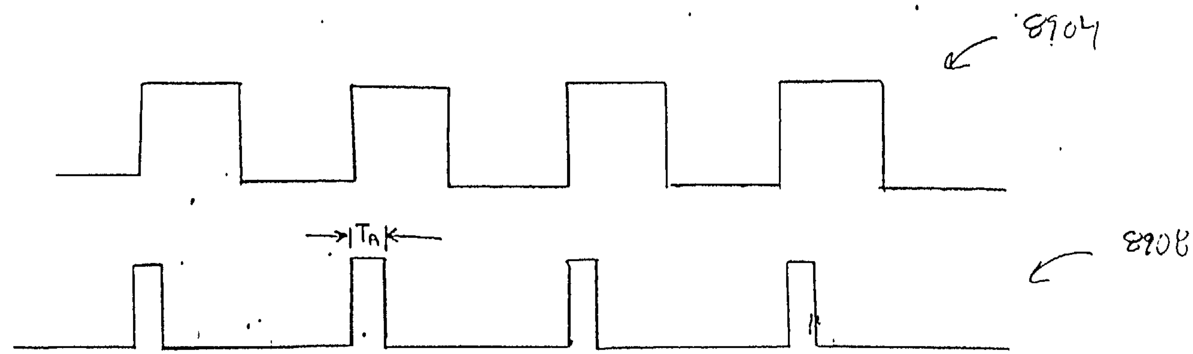


FIG. 89A

FIG. 89B

FIG. 89C



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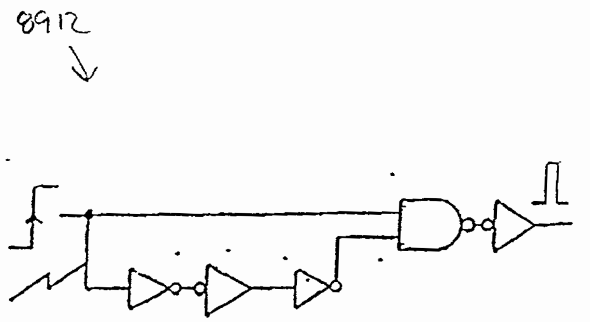
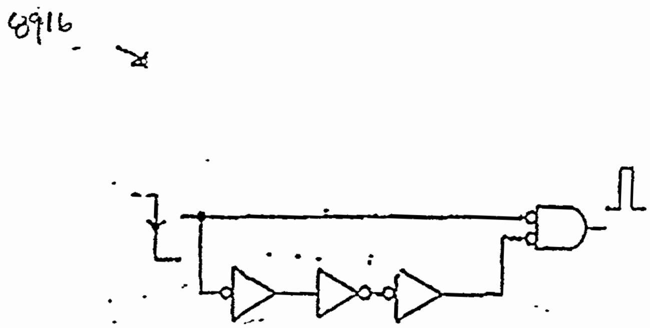


A. rising edge pulse generator

FIG. 89D



B. falling-edge pulse generator

FIG. 89E

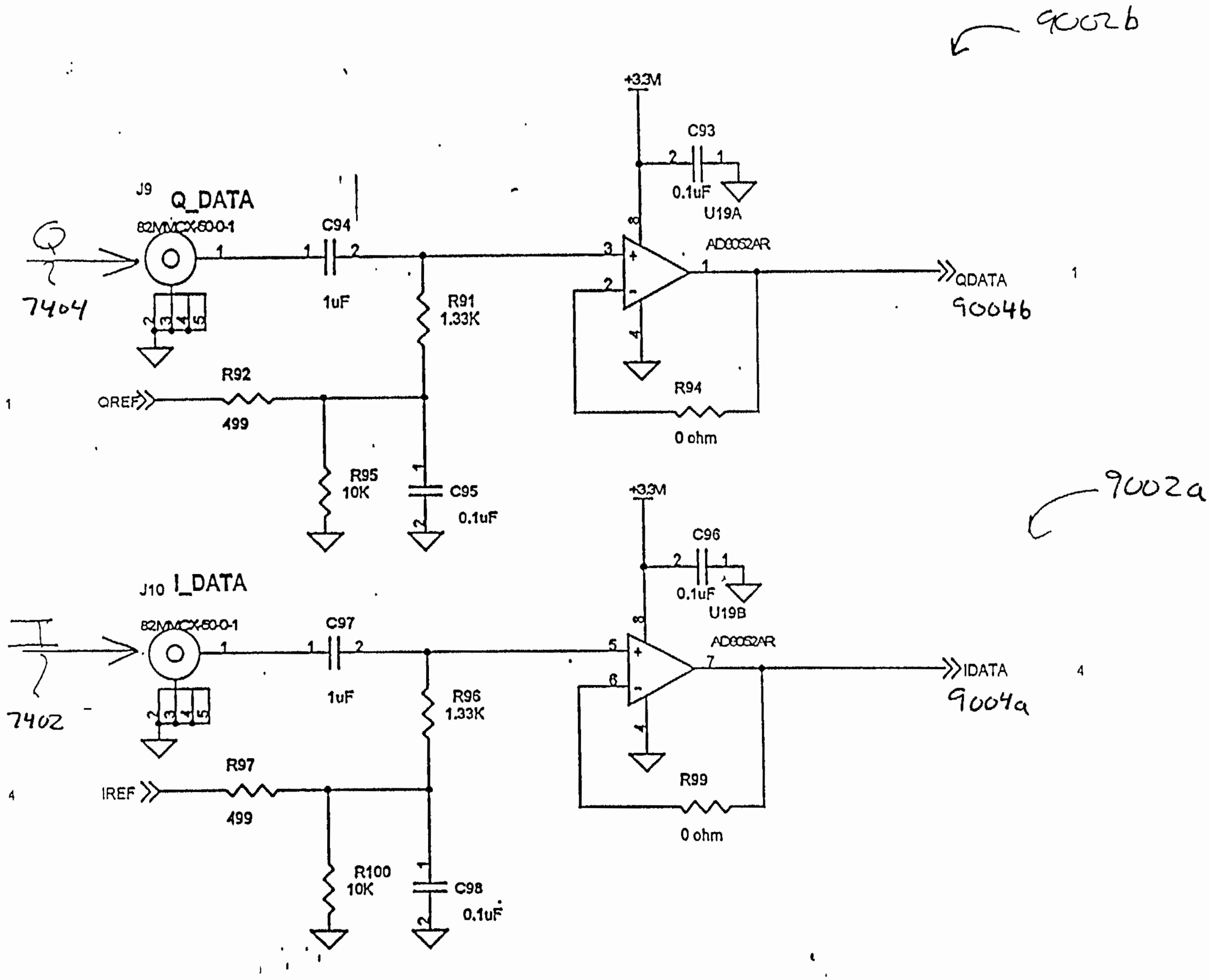

9002b
+3.3M
C93
0.1uF
U19A
AD8052AR
J9
Q_DATA
82MMCX-50-0-1
C94
1uF
Q
7404
R91
1.33K
QREF
R92
499
R94
0 ohm
R95
10K
C95
0.1uF
QDATA
9004b
9002a
+3.3M
C96
0.1uF
U19B
AD8052AR
J10
I_DATA
82MMCX-50-0-1
C97
1uF
I
7402
R96
1.33K
IREF
R97
499
R99
0 ohm
R100
10K
C98
0.1uF
IDATA
9004a

FIG. 90A

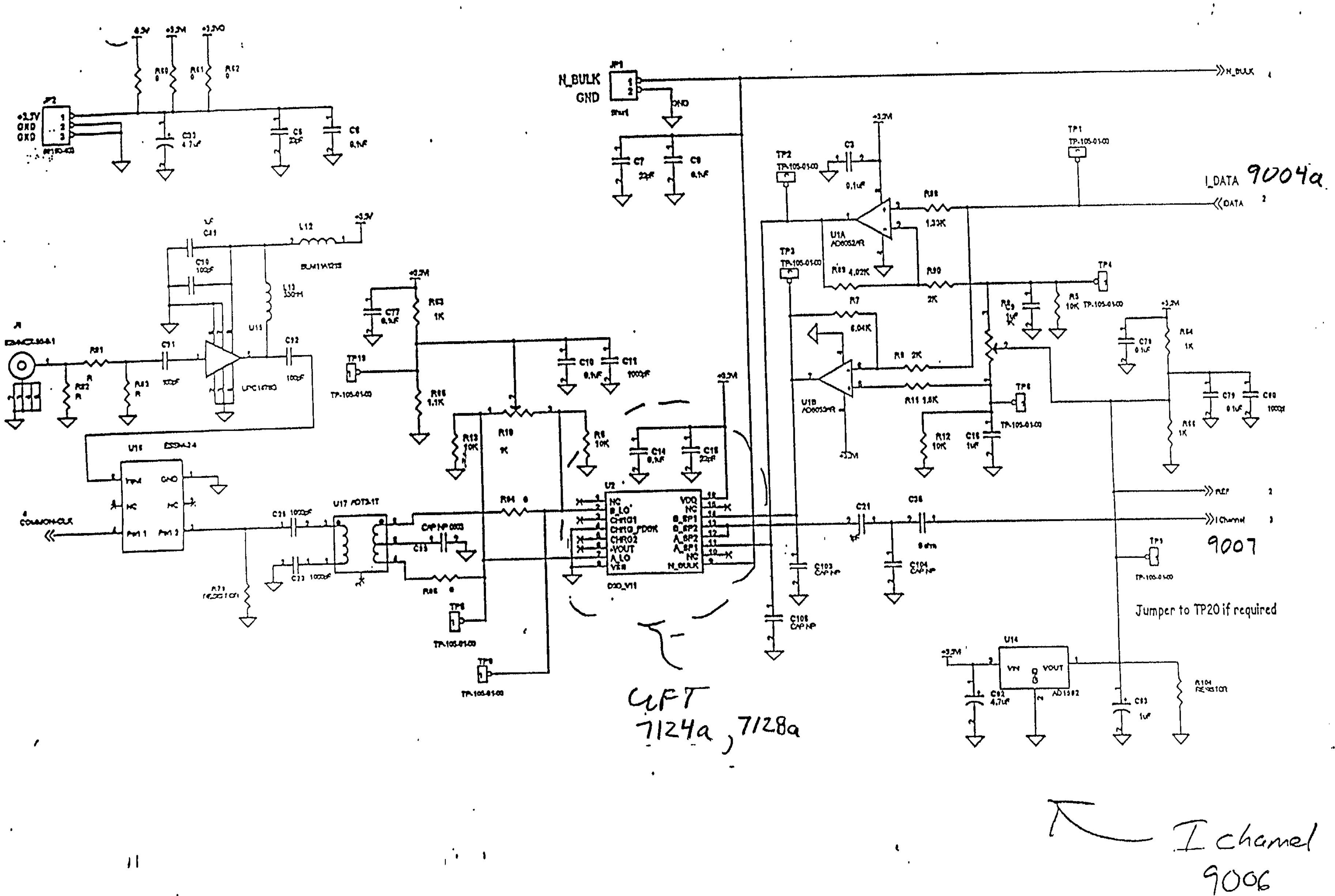

N_BULK
GND
I_DATA 9004a
U1A AD8052/R
U1B AD8052/R
U2
U14
U15
U16
U17
Jumper to TP20 if required
9007
LFT
7124a, 7128a
I channel
9006

FIG. 90B

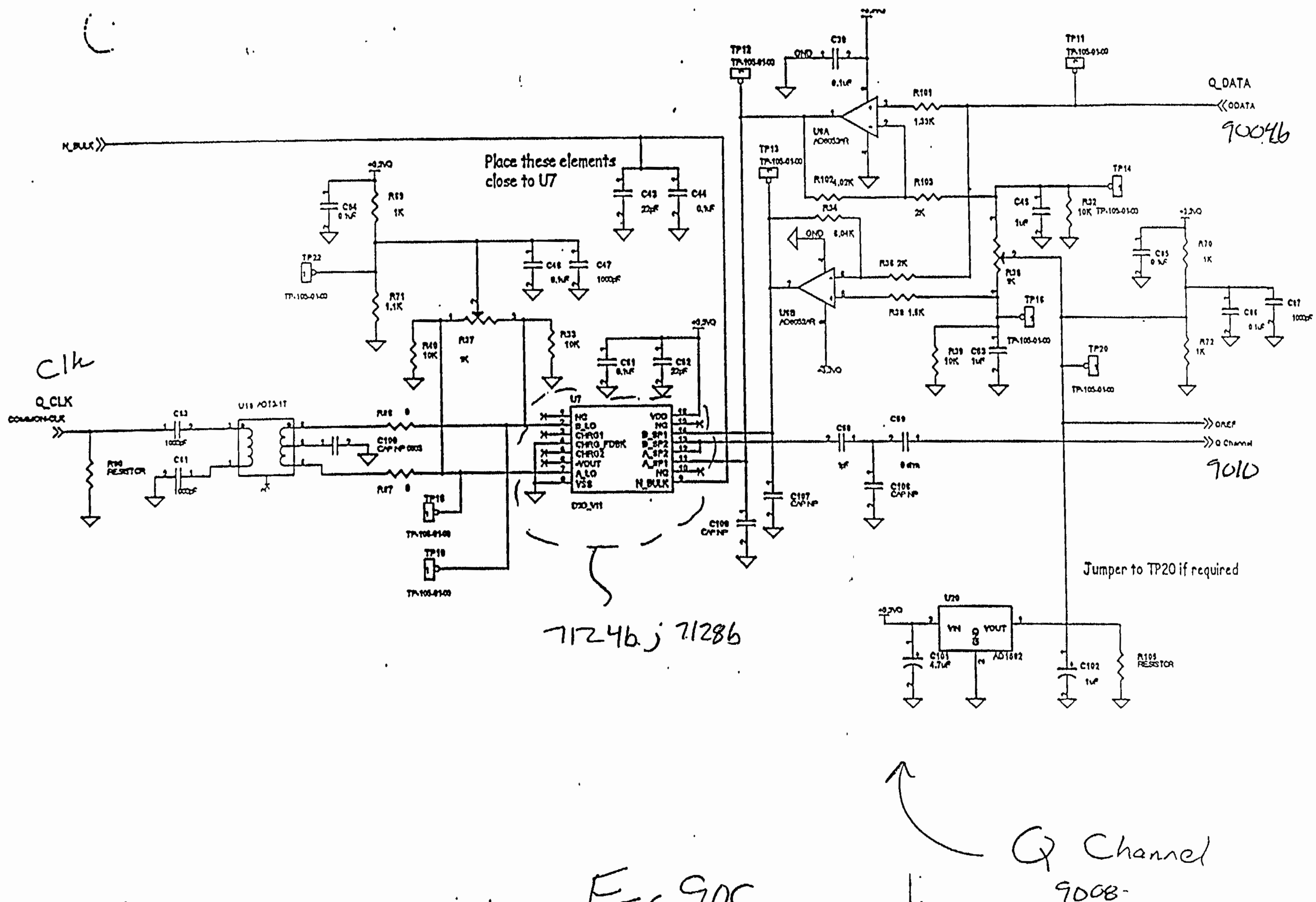

Place these elements close to U7
Q_DATA
9004b
Clk
Q_CLK
9010
Jumper to TP20 if required
7124b; 7128b
Q Channel
9008

FIG. 90C

09638256.080400

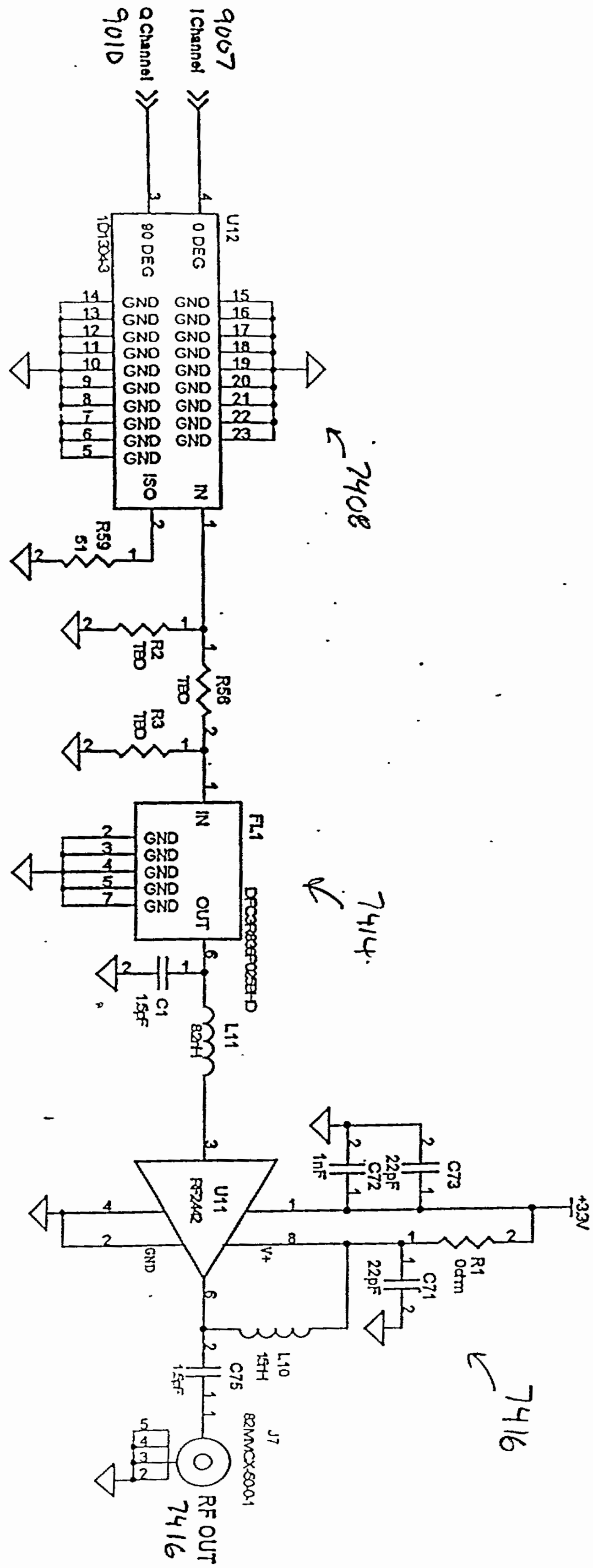


FIG. 9D

Combiner
9012

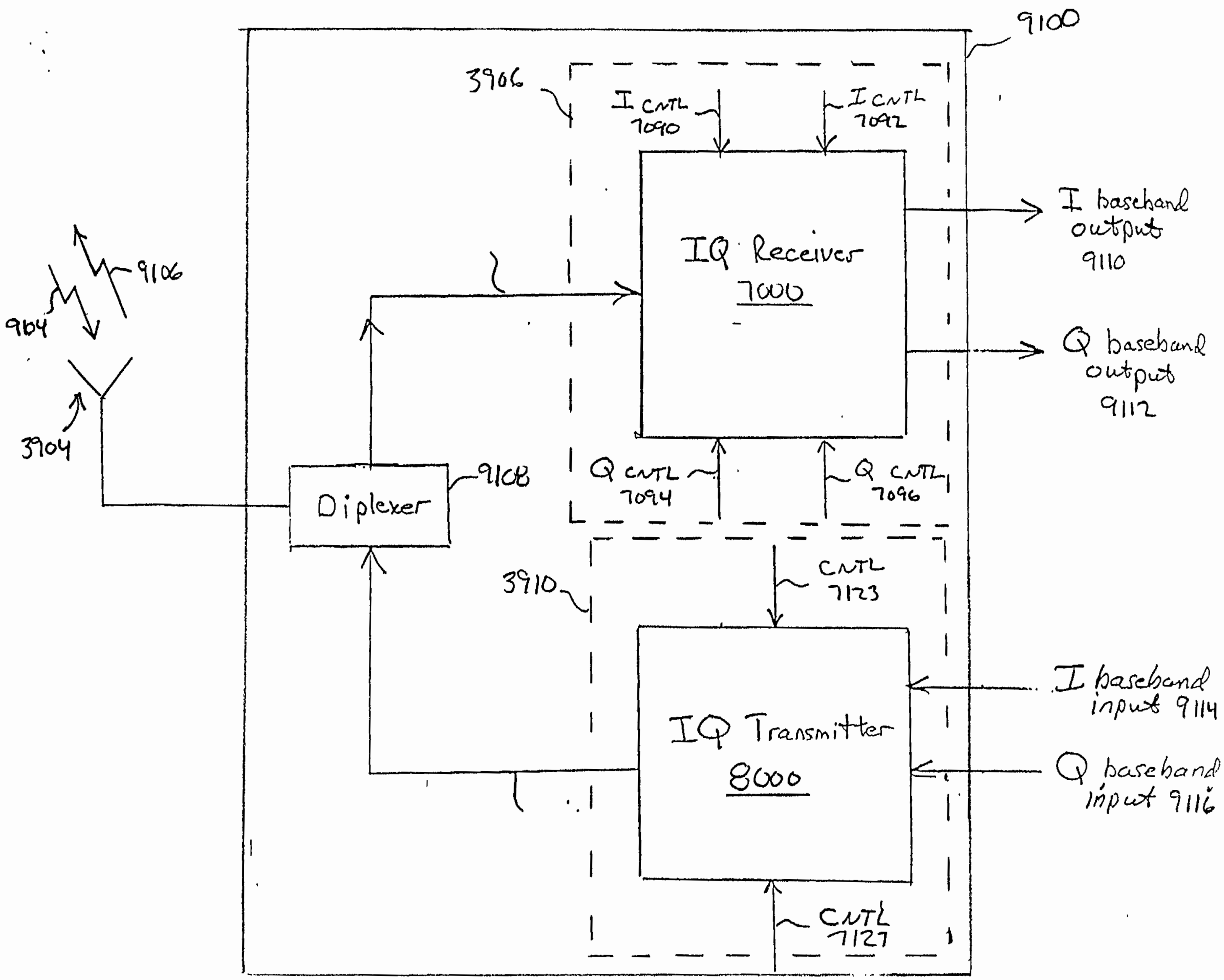
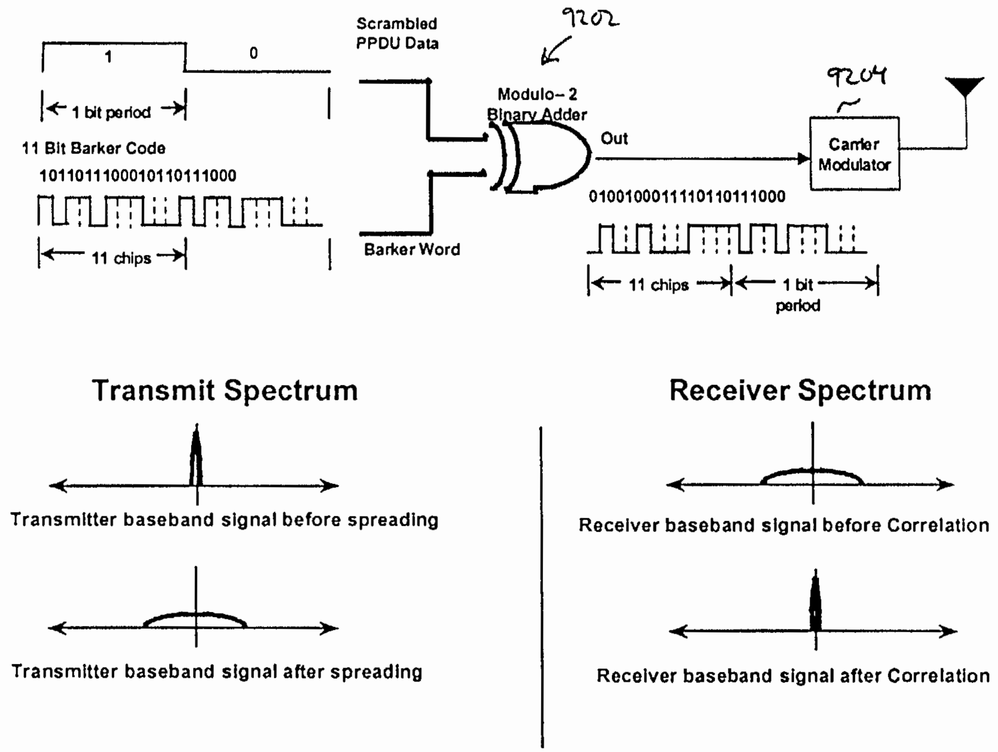

9100
3906
I CNTL 7090
I CNTL 7092
IQ Receiver 7000
I baseband output 9110
Q baseband output 9112
9106
904
3904
Diplexer
9108
Q CNTL 7094
Q CNTL 7096
3910
CNTL 7123
I baseband input 9114
IQ Transmitter 8000
Q baseband input 9116
CNTL 7127

FIG. 91



1
0
1 bit period
11 Bit Barker Code
10110111000101101110000
11 chips
Scrambled
PPDU Data
Barker Word
9202
Modulo- 2
Binary Adder
Out
01001000111101101110000
11 chips
1 bit
period
9204
Carrier
Modulator
Transmit Spectrum
Transmitter baseband signal before spreading
Transmitter baseband signal after spreading
Receiver Spectrum
Receiver baseband signal before Correlation
Receiver baseband signal after Correlation

FIG 92

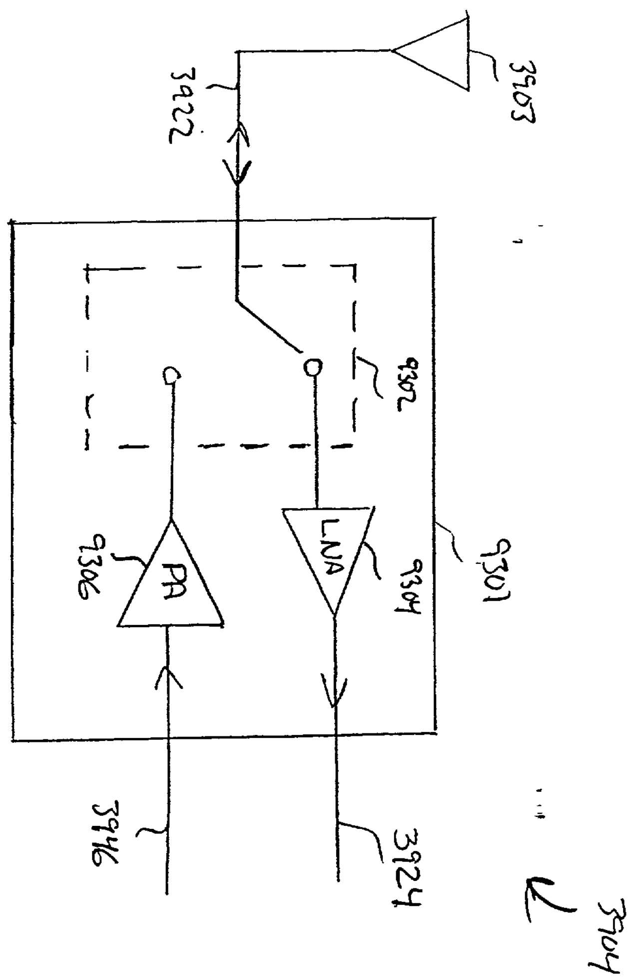


FIG. 93

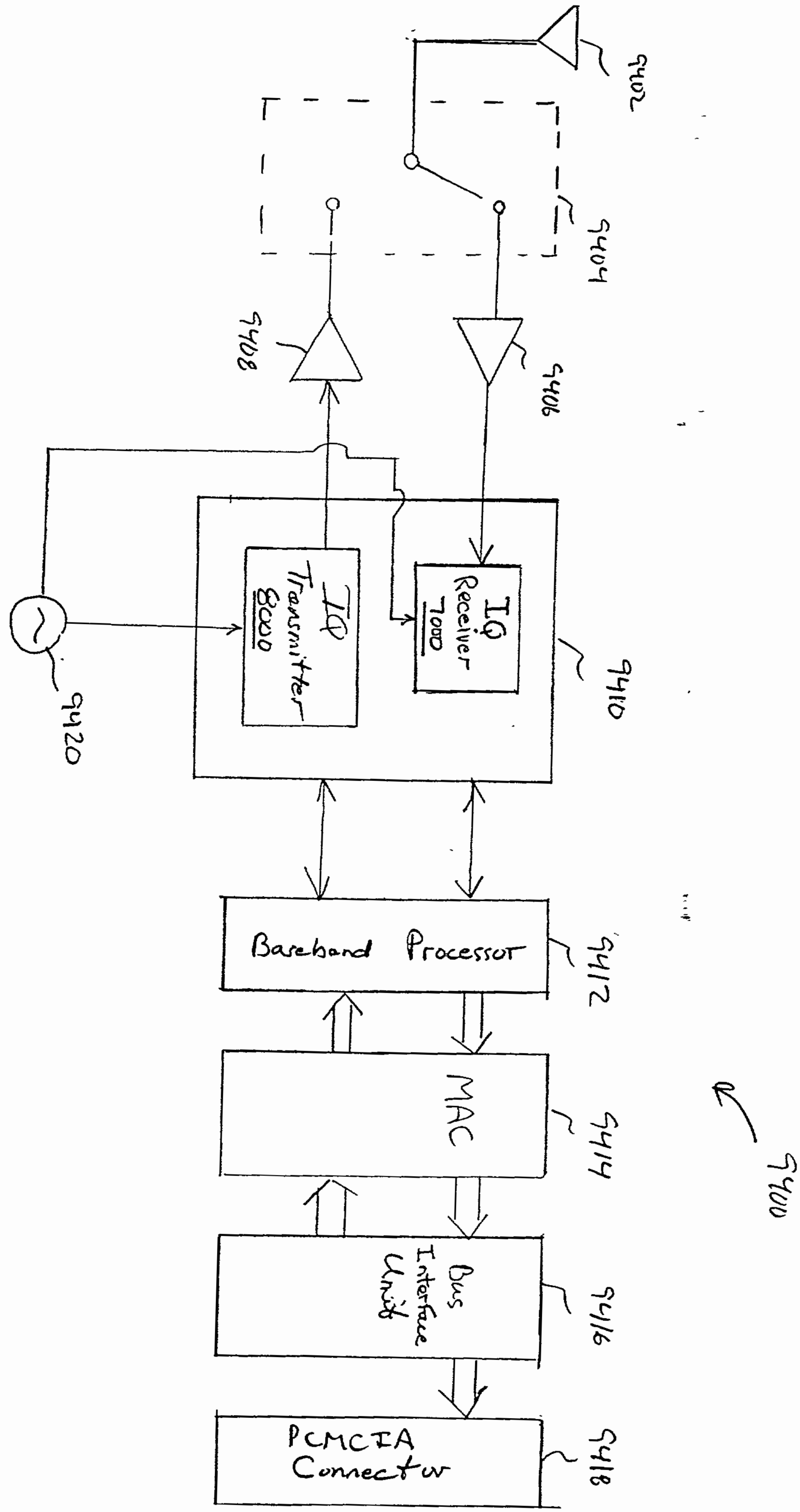
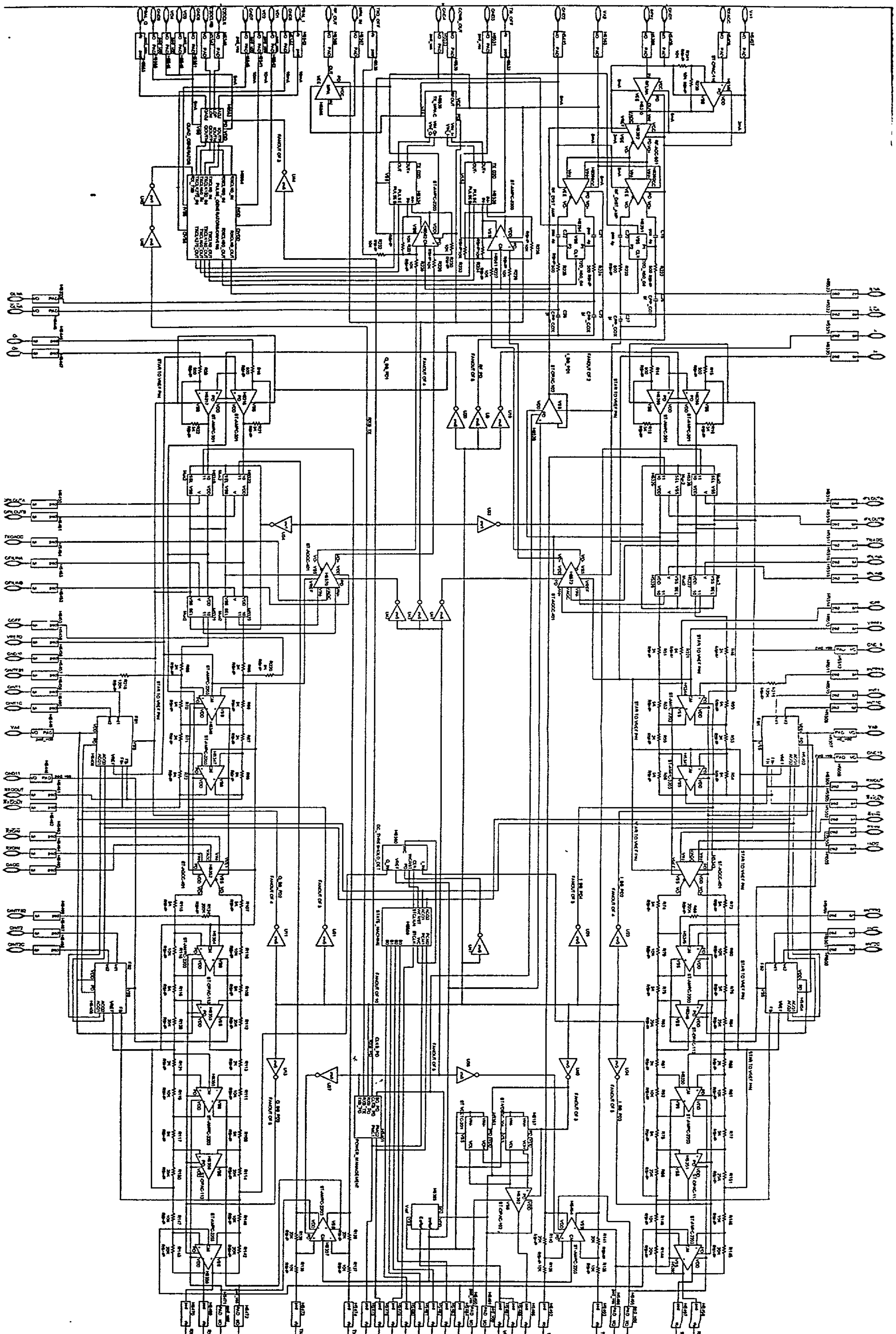

9402
9404
9406
9408
IQ Transmitter 8000
IQ Receiver 7000
9410
9420
Baseband Processor
9412
MAC
9414
Bus Interface Unit
9416
PCMCIA Connector
9418
9400

FIG. 94

FIG. 95A



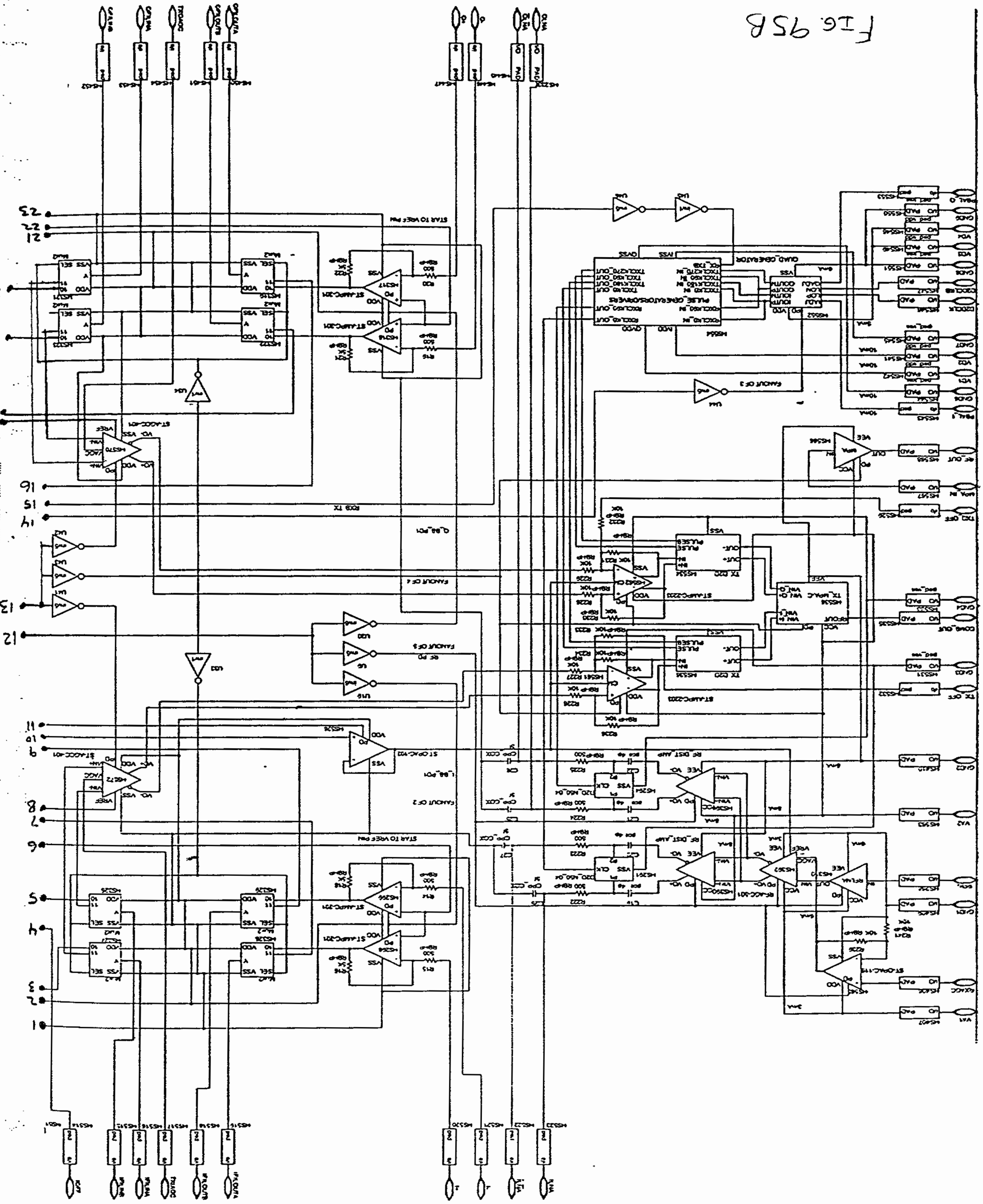


FIG. 95B

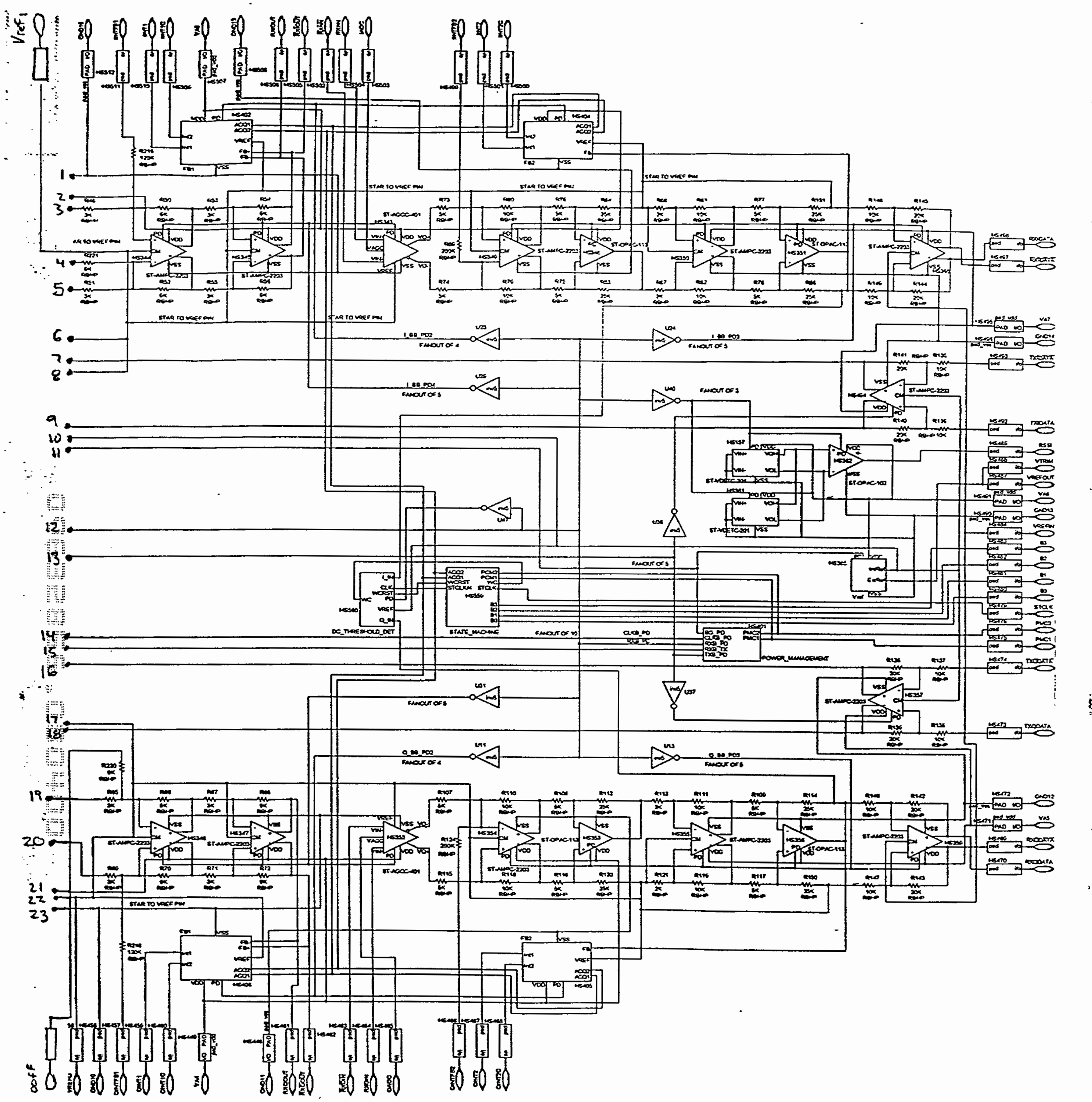
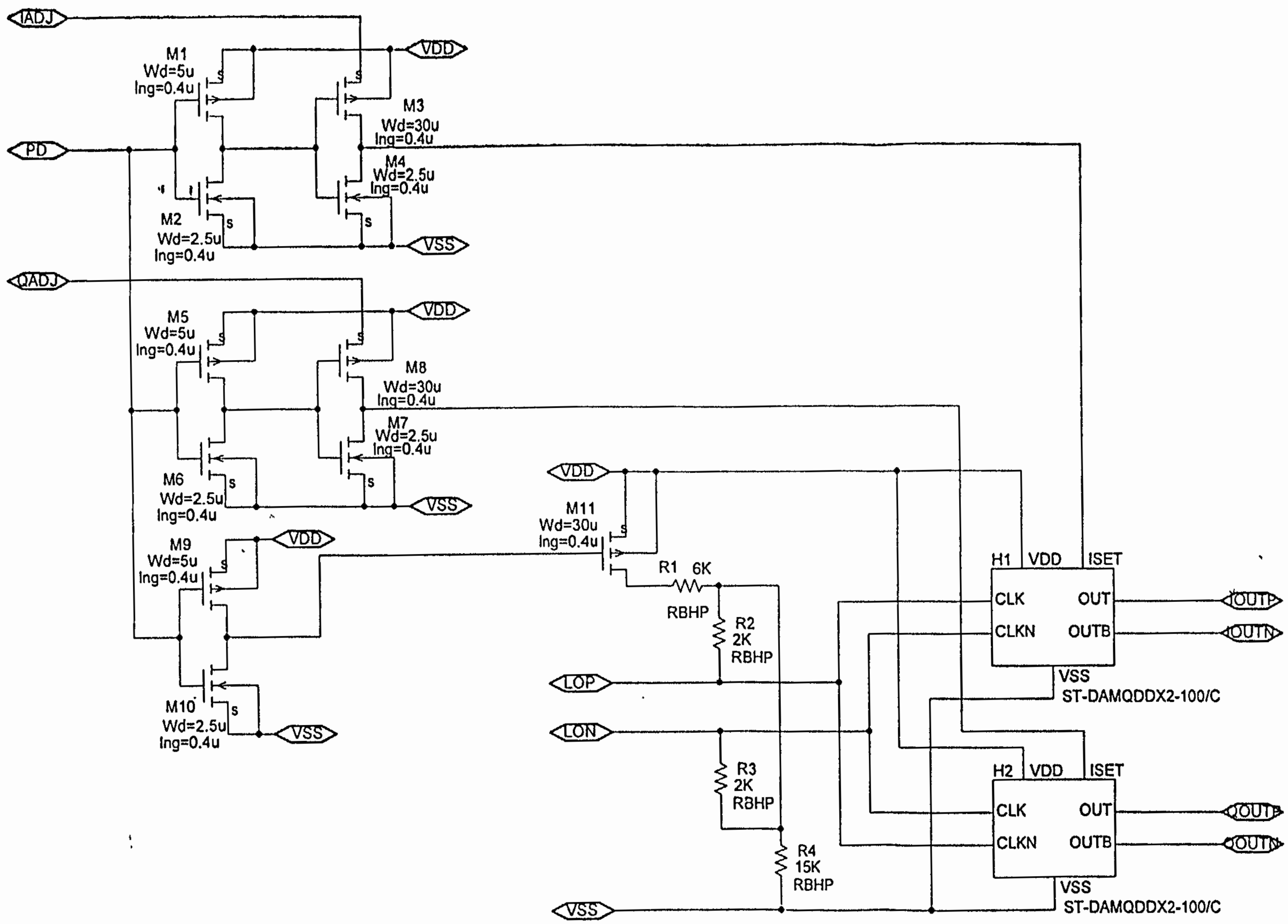


FIG. 95C



IADJ
VDD
M1
Wd=5u
lng=0.4u
M3
Wd=30u
lng=0.4u
PD
M4
Wd=2.5u
lng=0.4u
M2
Wd=2.5u
lng=0.4u
VSS
QADJ
VDD
M5
Wd=5u
lng=0.4u
M8
Wd=30u
lng=0.4u
M7
Wd=2.5u
lng=0.4u
M6
Wd=2.5u
lng=0.4u
VSS
M9
Wd=5u
lng=0.4u
VDD
M11
Wd=30u
lng=0.4u
R1 6K
RBHP
R2
2K
RBHP
M10
Wd=2.5u
lng=0.4u
VSS
LOP
LON
R3
2K
RBHP
R4
15K
RBHP
VSS
H1 VDD ISET
CLK OUT
CLKN OUTB
VSS
ST-DAMQDDX2-100/C
IOUTP
IOUTN
H2 VDD ISET
CLK OUT
CLKN OUTB
VSS
ST-DAMQDDX2-100/C
QOUTP
QOUTN

FIG. 96

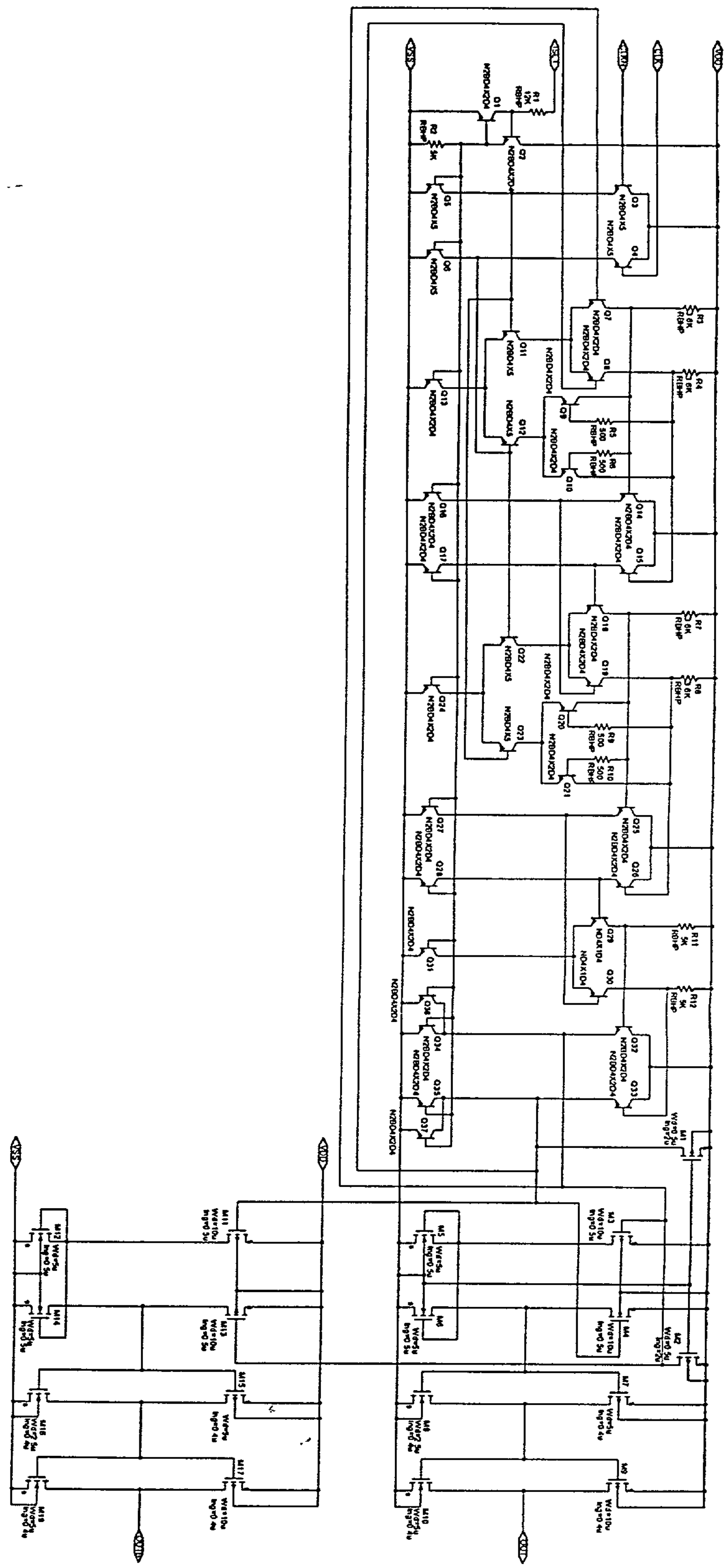
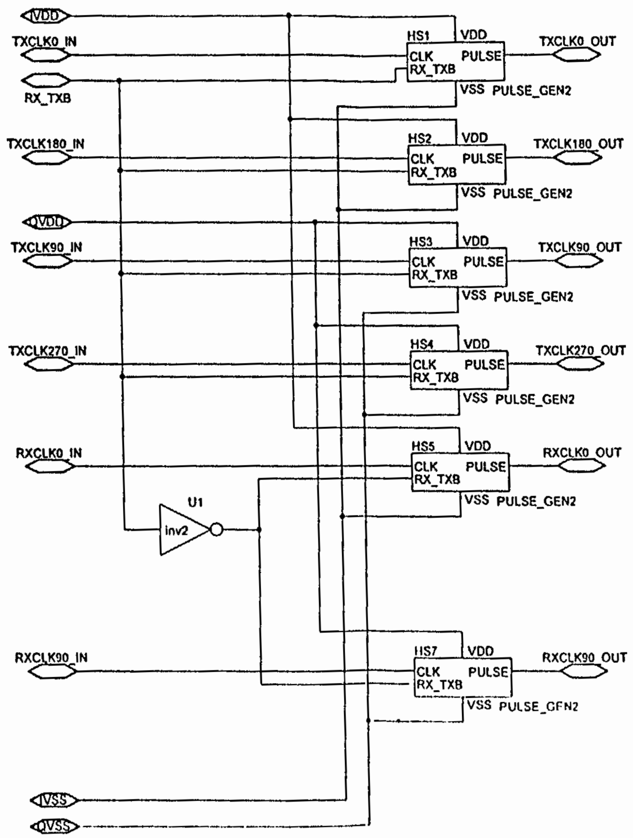


FIG. 17



VDD
TXCLK0_IN
RX_TXB
TXCLK180_IN
QVDD
TXCLK90_IN
TXCLK270_IN
RXCLK0_IN
RXCLK90_IN
IVSS
QVSS
U1
inv2
HS1
HS2
HS3
HS4
HS5
HS7
VDD
CLK
RX_TXB
PULSE
VSS
PULSE_GEN2
TXCLK0_OUT
TXCLK180_OUT
TXCLK90_OUT
TXCLK270_OUT
RXCLK0_OUT
RXCLK90_OUT

FIG. 98

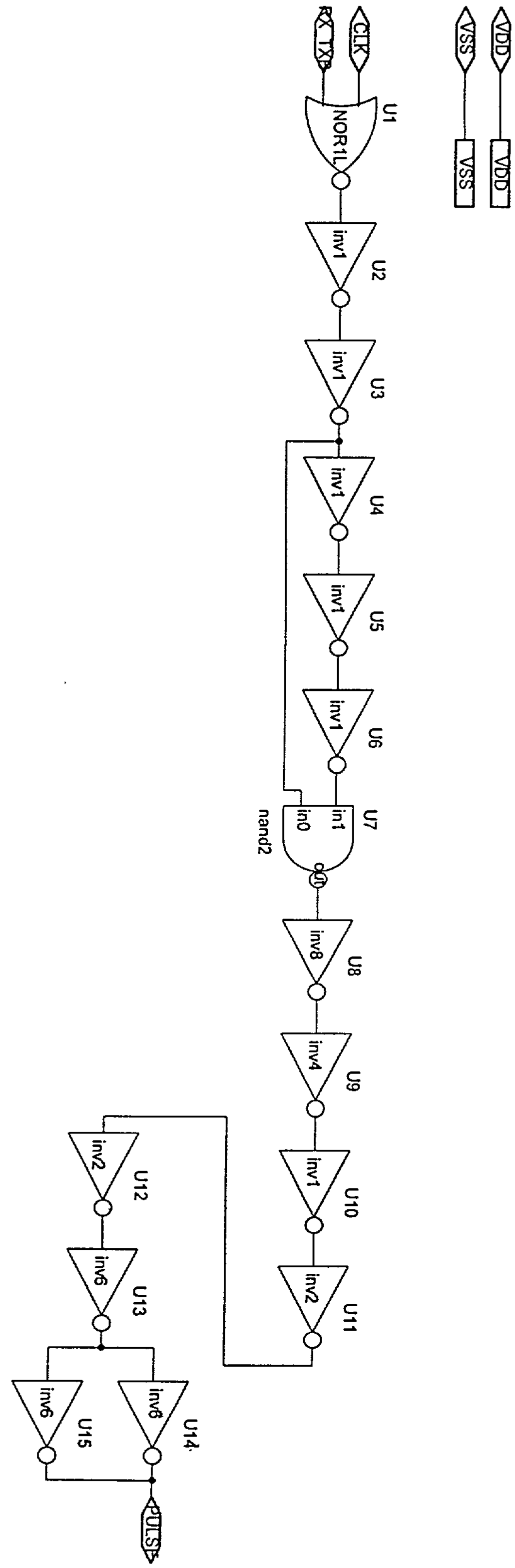

RX_TX
CLK
VSS
VDD
VSS
VDD
U1
NOR1L
inv1
U2
inv1
U3
inv1
U4
inv1
U5
inv1
U6
U7
in1
in0
nand2
out
inv8
U8
inv4
U9
inv1
U10
inv2
U11
inv2
U12
inv6
U13
inv6
U14
inv6
U15
PULS

FIG. 79

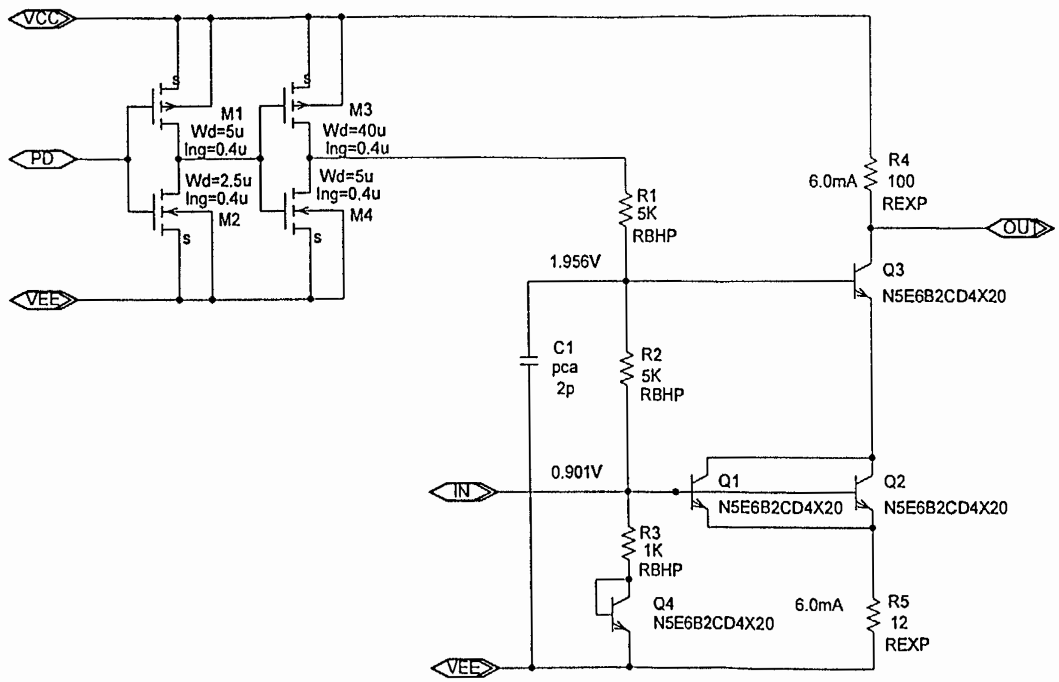

VCC
PD
VEE
M1
Wd=5u
lng=0.4u
Wd=2.5u
lng=0.4u
M2
M3
Wd=40u
lng=0.4u
Wd=5u
lng=0.4u
M4
R1
5K
RBHP
R4
100
REXP
6.0mA
OUT
1.956V
Q3
N5E6B2CD4X20
C1
pca
2p
R2
5K
RBHP
IN
0.901V
Q1
N5E6B2CD4X20
Q2
N5E6B2CD4X20
R3
1K
RBHP
Q4
N5E6B2CD4X20
6.0mA
R5
12
REXP
VEE

FIG. 16

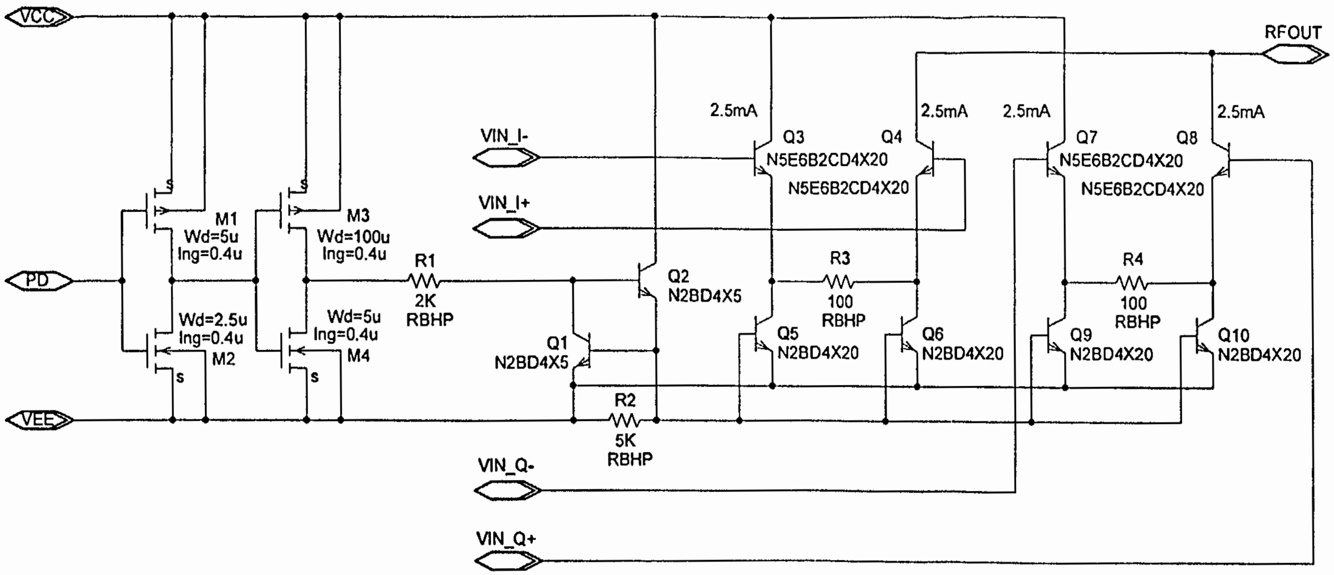

VCC
PD
VEE
M1
Wd=5u
lng=0.4u
Wd=2.5u
lng=0.4u
M2
M3
Wd=100u
lng=0.4u
Wd=5u
lng=0.4u
M4
R1
2K
RBHP
Q2
N2BD4X5
Q1
N2BD4X5
R2
5K
RBHP
VIN_I-
VIN_I+
VIN_Q-
VIN_Q+
2.5mA
Q3
N5E6B2CD4X20
Q4
N5E6B2CD4X20
R3
100
RBHP
Q5
N2BD4X20
Q6
N2BD4X20
Q7
N5E6B2CD4X20
Q8
N5E6B2CD4X20
R4
100
RBHP
Q9
N2BD4X20
Q10
N2BD4X20
RFOUT

FIG. 101

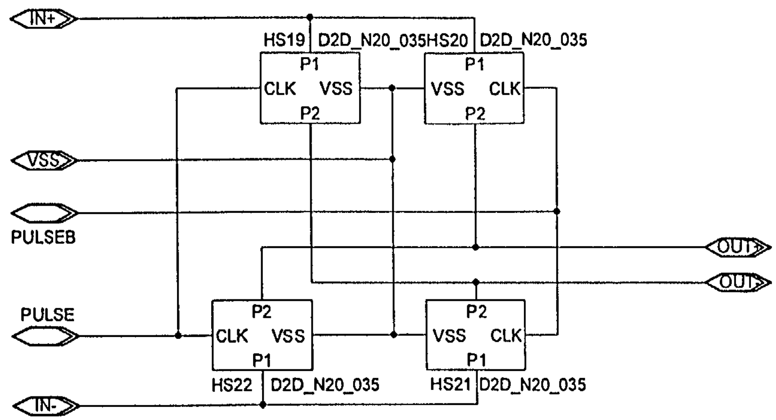

IN+
HS19
D2D_N20_035
HS20
D2D_N20_035
P1
CLK
VSS
P2
P1
VSS
CLK
P2
VSS
PULSEB
OUT+
OUT-
PULSE
P2
CLK
VSS
P1
P2
VSS
CLK
P1
HS22
D2D_N20_035
HS21
D2D_N20_035
IN-

FIG. 102

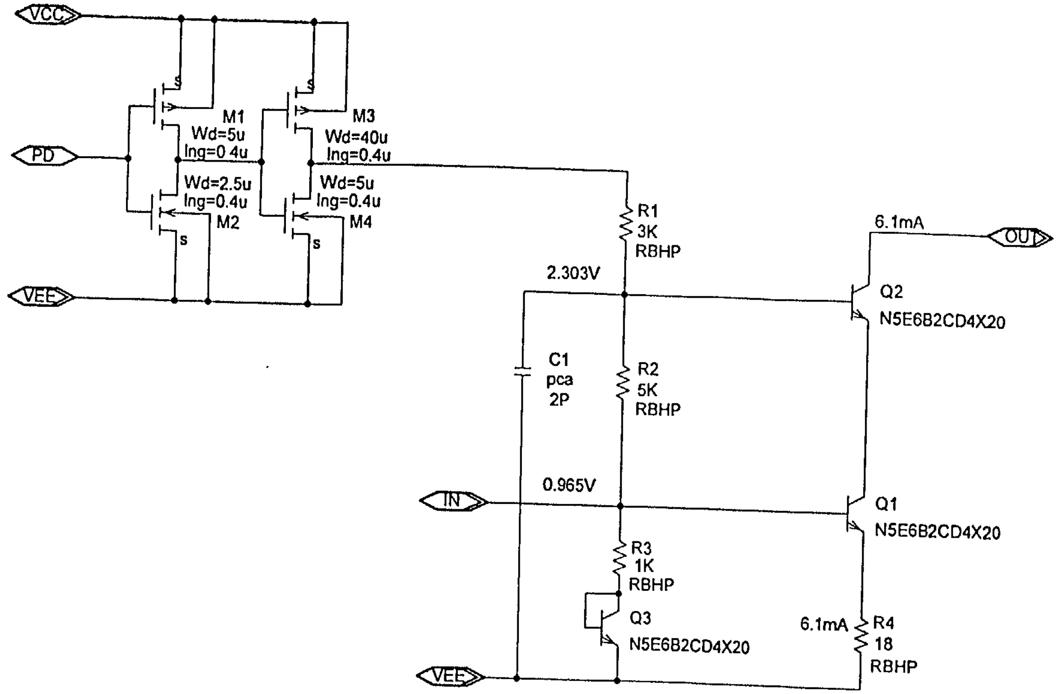

VCC
PD
VEE
M1
Wd=5u
lng=0.4u
Wd=2.5u
lng=0.4u
M2
M3
Wd=40u
lng=0.4u
Wd=5u
lng=0.4u
M4
R1
3K
RBHP
2.303V
C1
pca
2P
R2
5K
RBHP
IN
0.965V
R3
1K
RBHP
Q3
N5E6B2CD4X20
VEE
6.1mA
OUT
Q2
N5E6B2CD4X20
Q1
N5E6B2CD4X20
6.1mA
R4
18
RBHP

FIG. 103

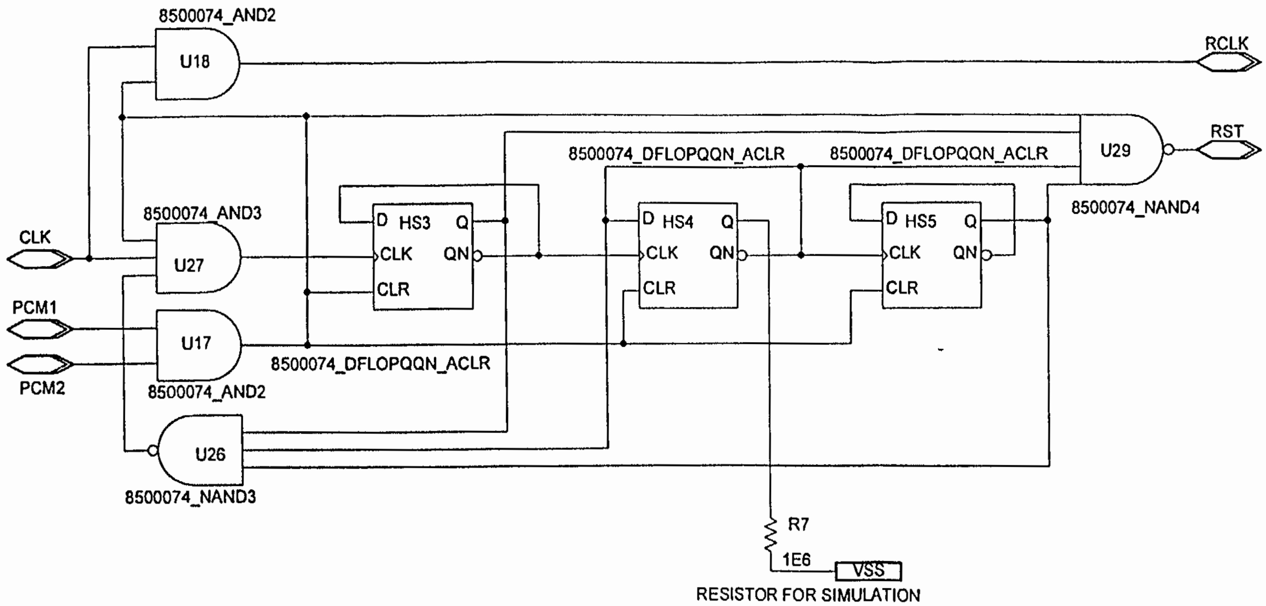
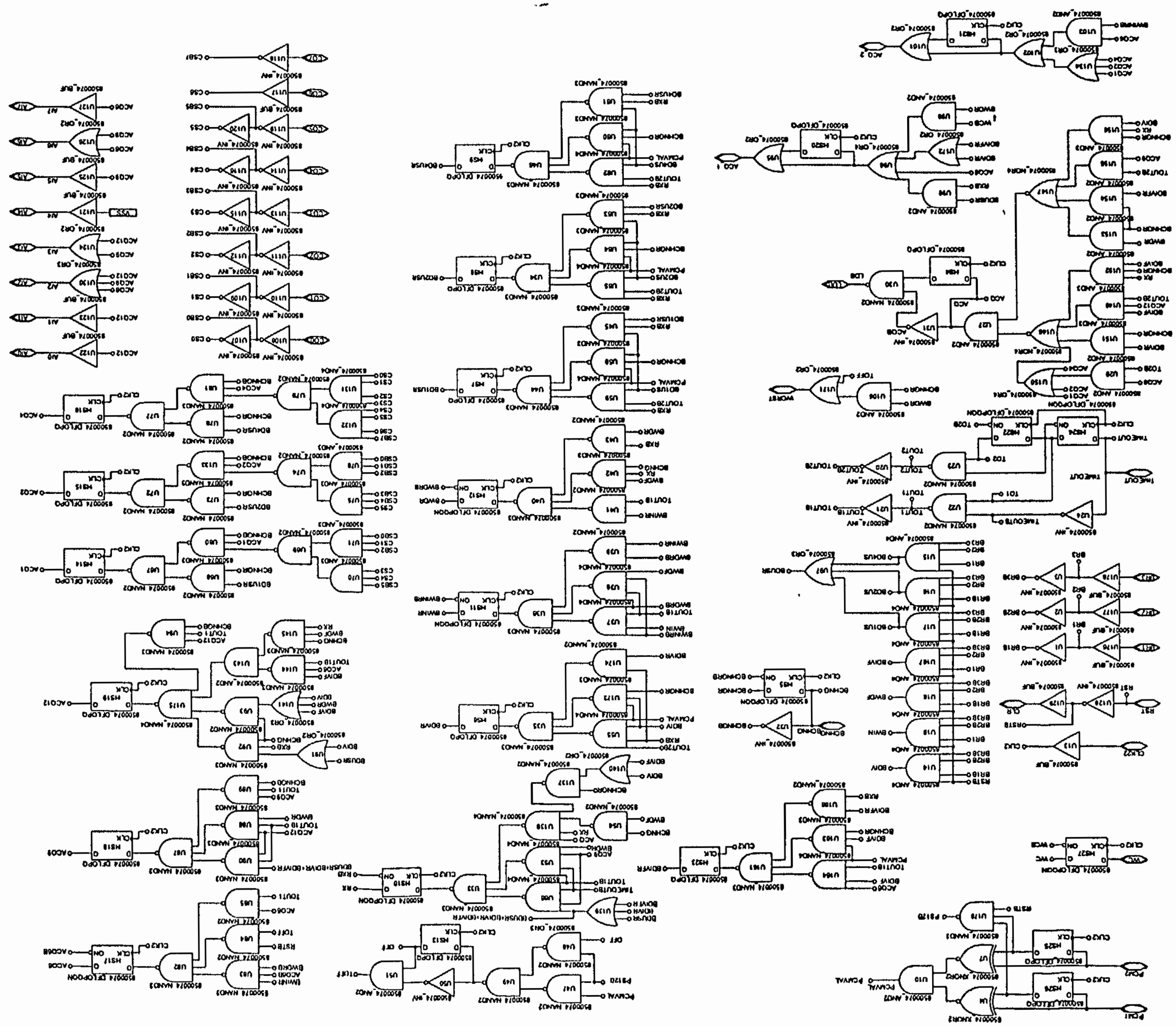

8500074_AND2
U18
RCLK
U29
RST
8500074_DFLOPQQN_ACLR
8500074_DFLOPQQN_ACLR
8500074_NAND4
8500074_AND3
CLK
U27
D HS3 Q
CLK QN
CLR
D HS4 Q
CLK QN
CLR
D HS5 Q
CLK QN
CLR
PCM1
U17
PCM2
8500074_DFLOPQQN_ACLR
8500074_AND2
U26
8500074_NAND3
R7
1E6
VSS
RESISTOR FOR SIMULATION

FIG 104

FIG. 105



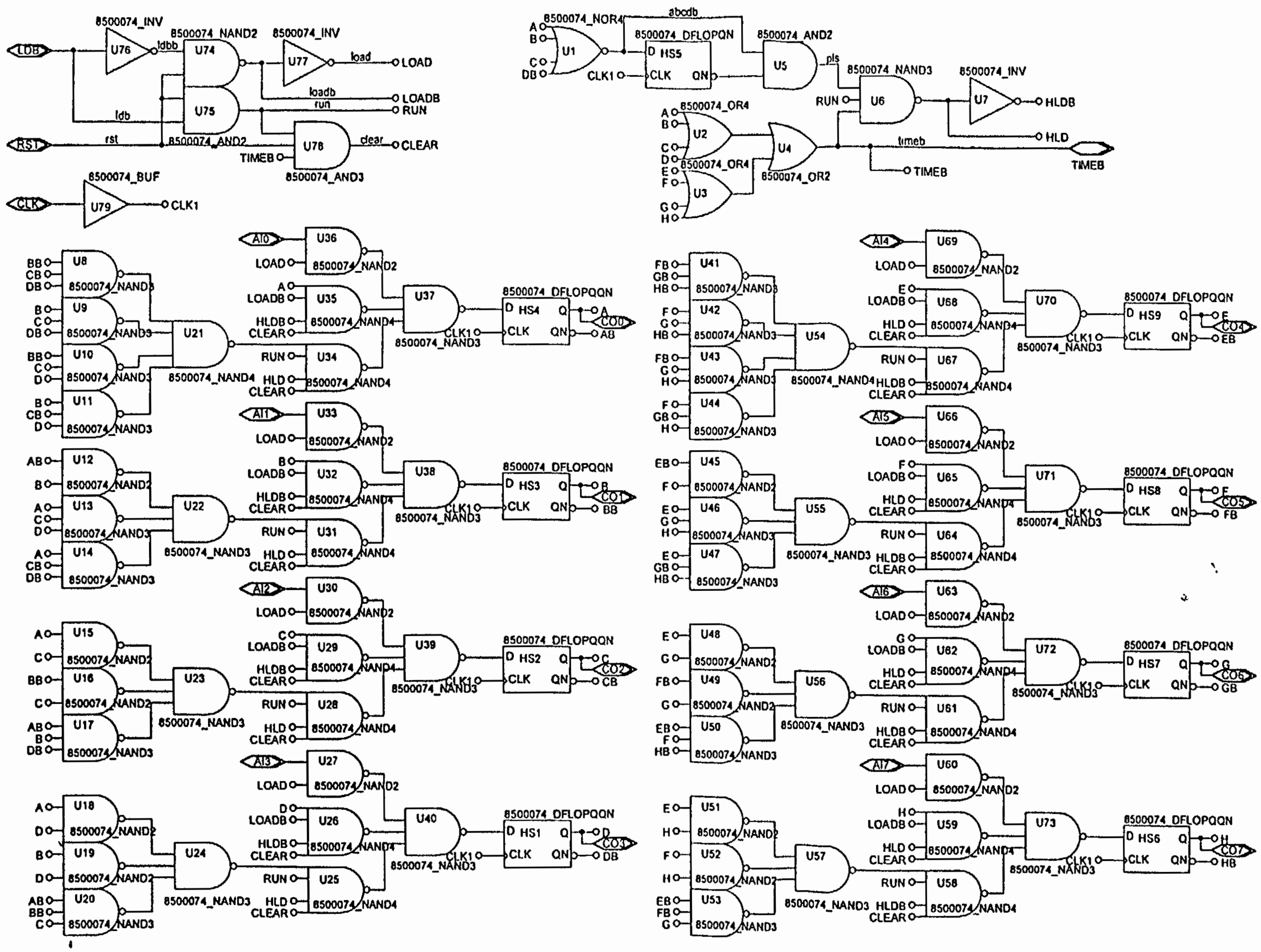


Fig. 106

09632856 .080400

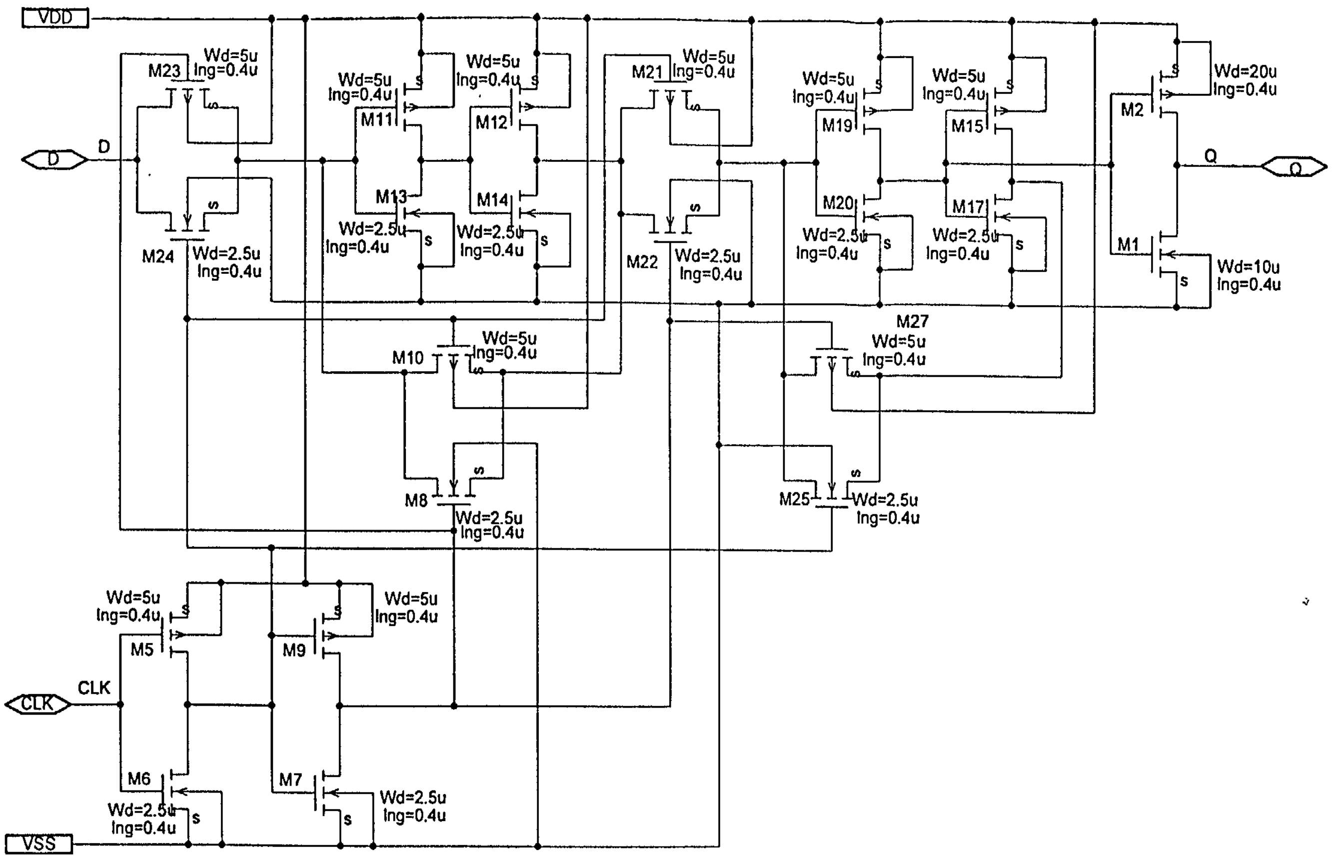

VDD
D
M23
Wd=5u
lng=0.4u
M24
Wd=2.5u
lng=0.4u
M11
M12
M13
M14
M21
M22
M19
M20
M15
M17
M2
Wd=20u
lng=0.4u
M1
Wd=10u
lng=0.4u
Q
M10
M8
M27
M25
M5
M9
M6
M7
CLK
VSS

FIG. 107

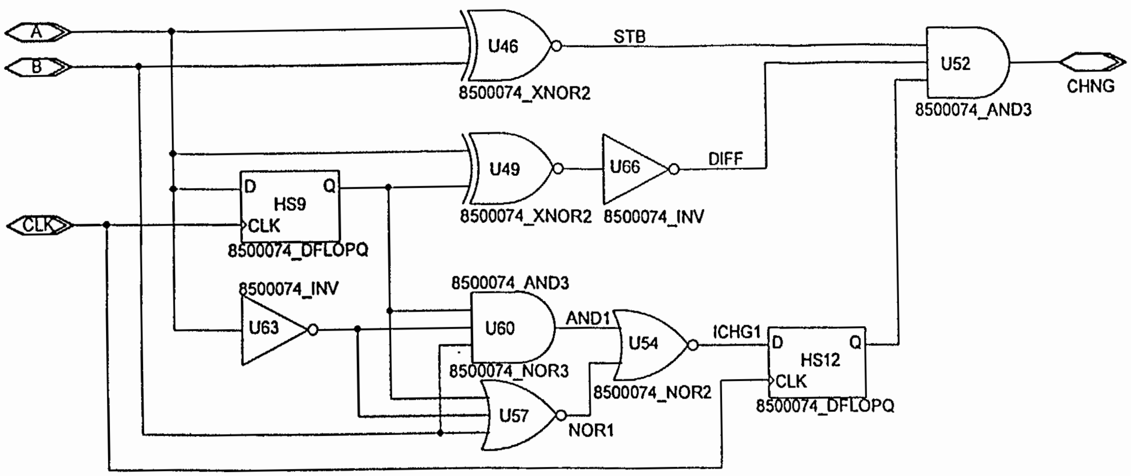

A
B
CLK
U46
8500074_XNOR2
STB
U52
8500074_AND3
CHNG
U49
8500074_XNOR2
U66
8500074_INV
DIFF
D
HS9
Q
CLK
8500074_DFLOPQ
8500074_INV
U63
8500074_AND3
U60
AND1
U54
ICHG1
D
HS12
Q
CLK
8500074_NOR3
8500074_NOR2
8500074_DFLOPQ
U57
NOR1

FIG. 108

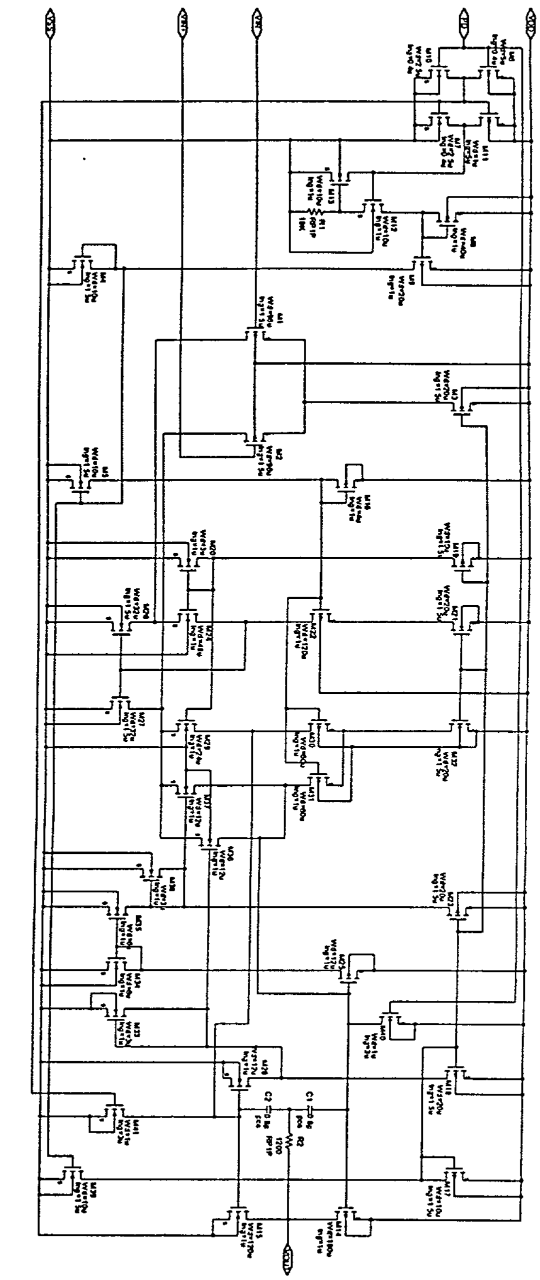


Fig. 107

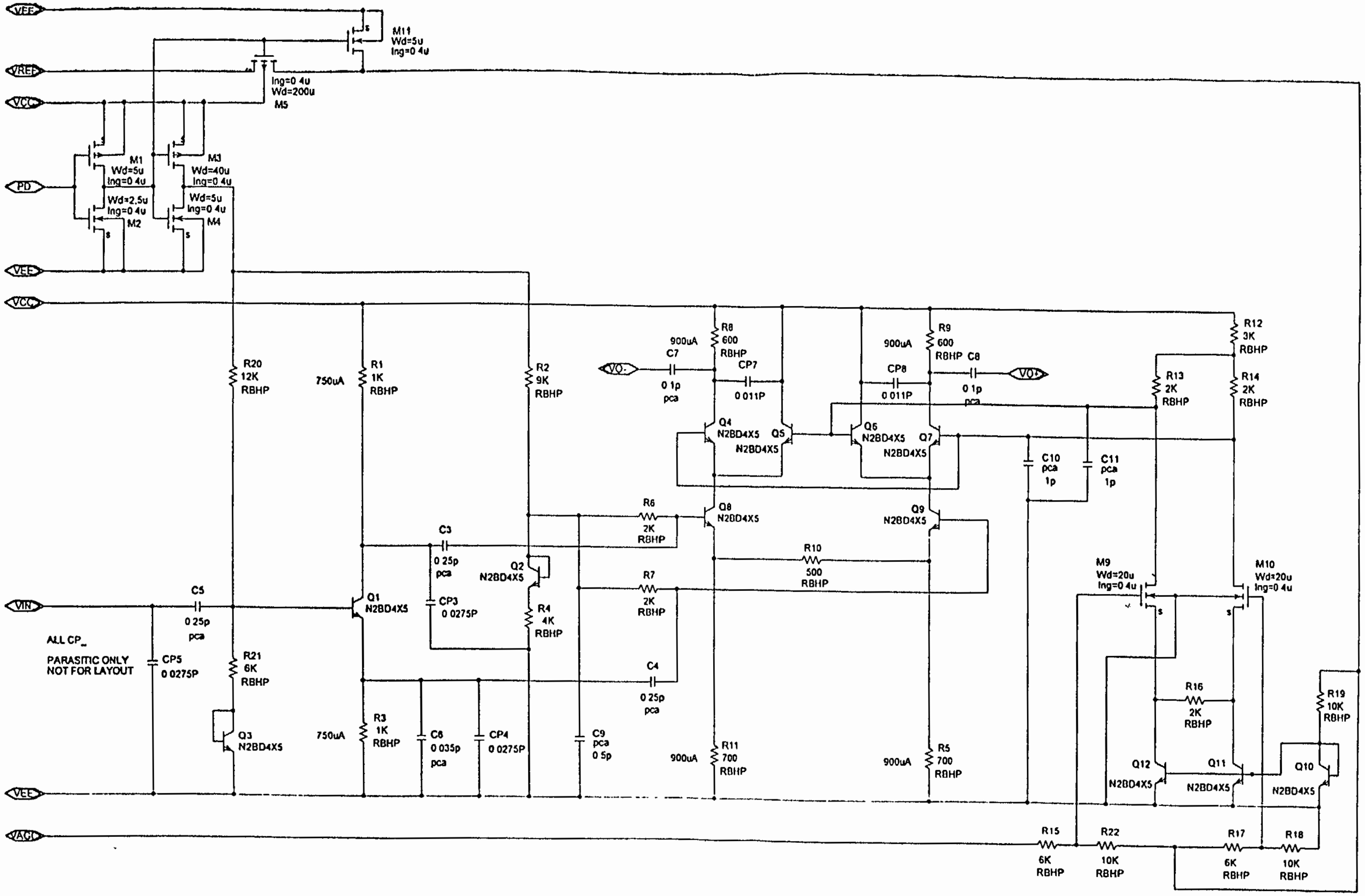


Fig. 110

09632556 .080400

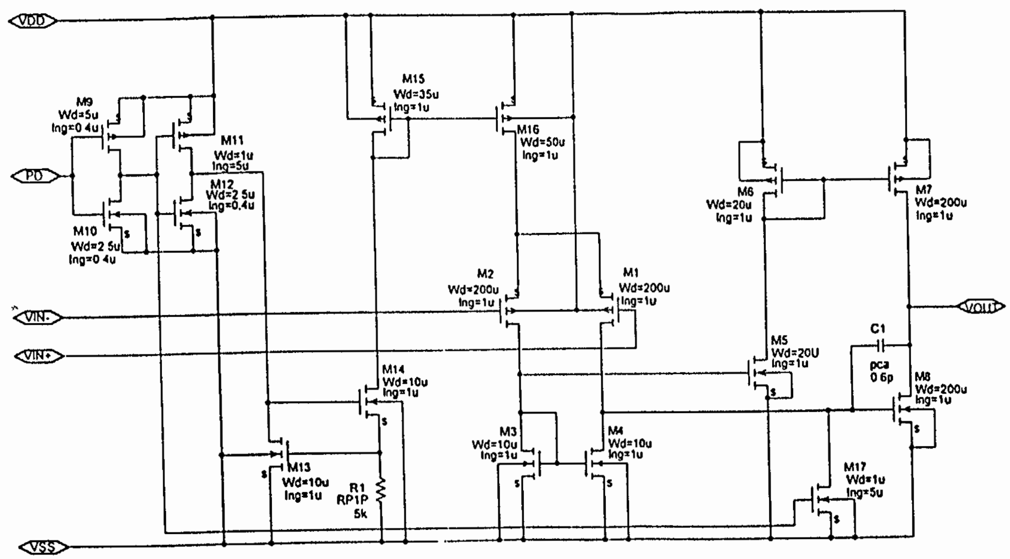

VDD
PD
VIN-
VIN+
VSS
VOUT
M9
Wd=5u
lng=0.4u
M10
Wd=2.5u
lng=0.4u
M11
Wd=1u
lng=5u
M12
Wd=2.5u
lng=0.4u
M15
Wd=35u
lng=1u
M16
Wd=50u
lng=1u
M2
Wd=200u
lng=1u
M1
Wd=200u
lng=1u
M14
Wd=10u
lng=1u
M13
Wd=10u
lng=1u
R1
RP1P
5k
M3
Wd=10u
lng=1u
M4
Wd=10u
lng=1u
M6
Wd=20u
lng=1u
M7
Wd=200u
lng=1u
M5
Wd=20U
lng=1u
C1
pca
0.6p
M8
Wd=200u
lng=1u
M17
Wd=1u
lng=5u

Fig. 111

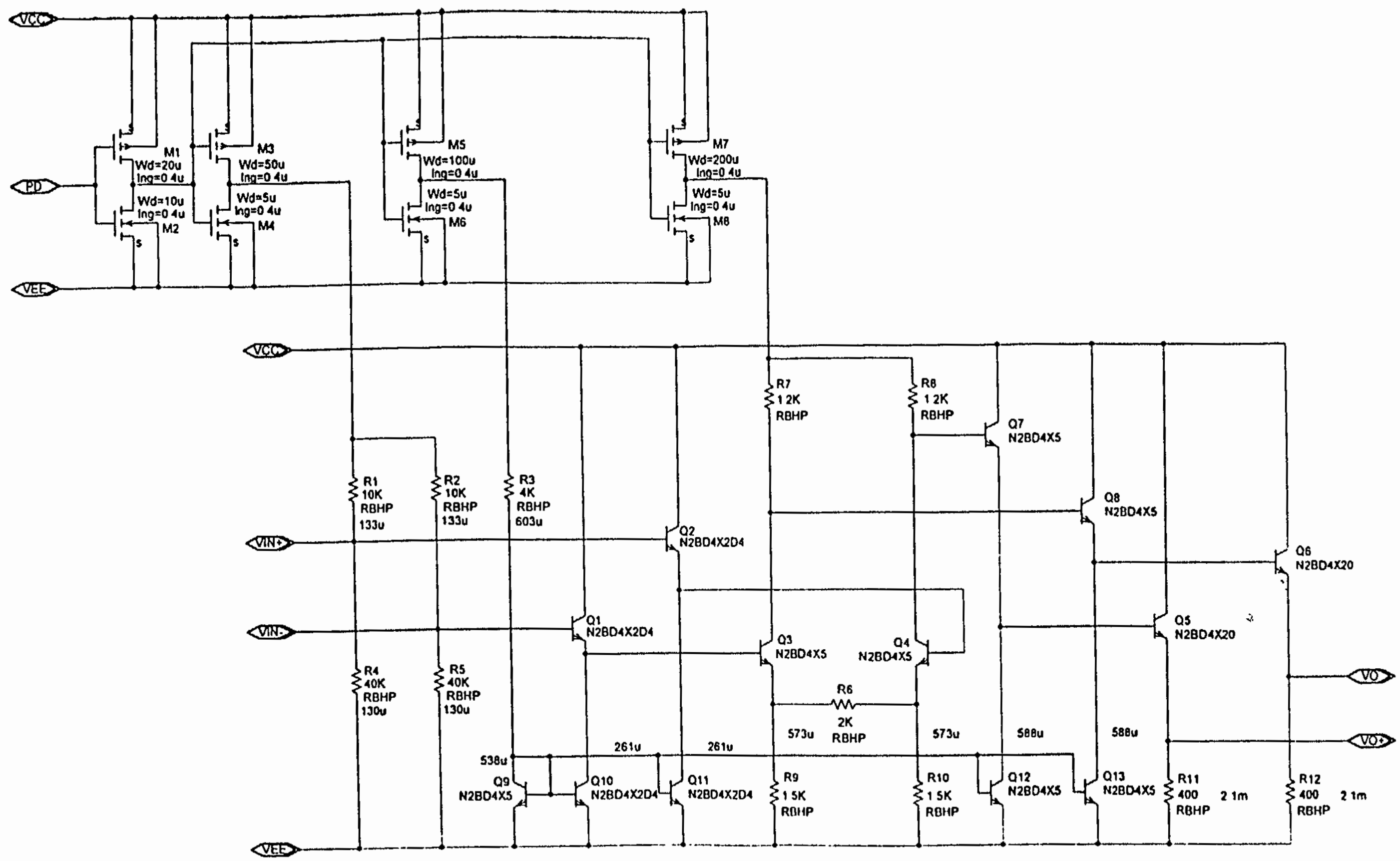
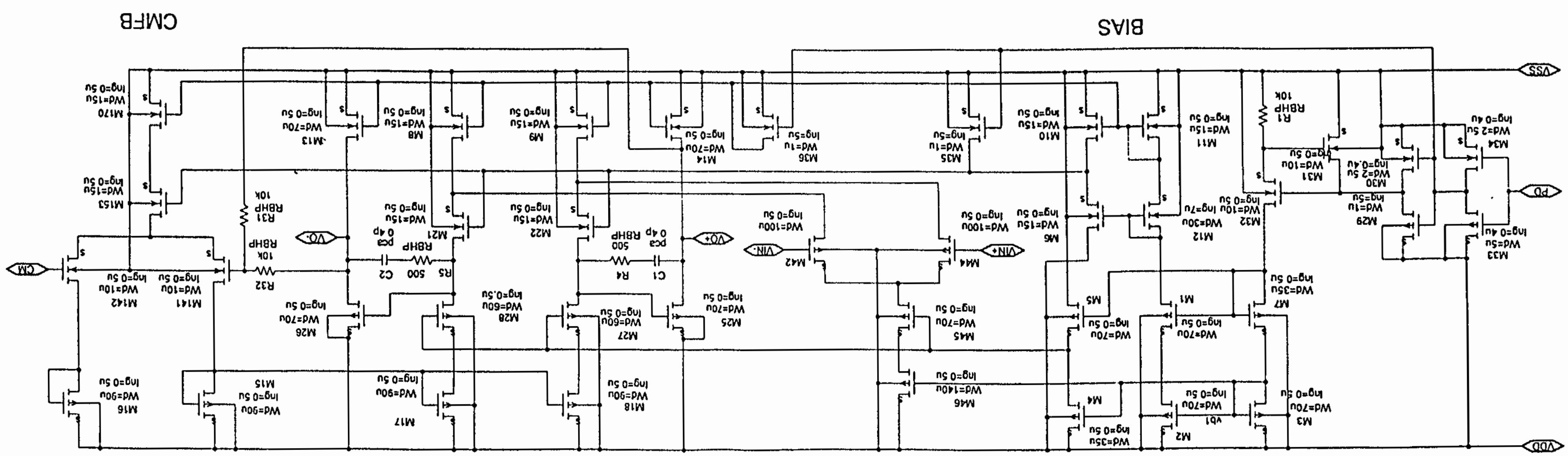

VCC
PD
VEE
M1
Wd=20u
lng=0.4u
Wd=10u
lng=0.4u
M2
M3
Wd=50u
lng=0.4u
Wd=5u
lng=0.4u
M4
M5
Wd=100u
lng=0.4u
Wd=5u
lng=0.4u
M6
M7
Wd=200u
lng=0.4u
Wd=5u
lng=0.4u
M8
VCC
R1
10K
RBHP
133u
R2
10K
RBHP
133u
R3
4K
RBHP
603u
R7
1.2K
RBHP
R8
1.2K
RBHP
Q7
N2BD4X5
Q8
N2BD4X5
Q6
N2BD4X20
VIN+
Q2
N2BD4X2D4
VIN-
Q1
N2BD4X2D4
Q3
N2BD4X5
Q4
N2BD4X5
Q5
N2BD4X20
VO-
VO+
R4
40K
RBHP
130u
R5
40K
RBHP
130u
R6
2K
RBHP
573u
573u
588u
588u
538u
261u
261u
Q9
N2BD4X5
Q10
N2BD4X2D4
Q11
N2BD4X2D4
R9
1.5K
RBHP
R10
1.5K
RBHP
Q12
N2BD4X5
Q13
N2BD4X5
R11
400
RBHP
2.1m
R12
400
RBHP
2.1m
VEE

FIG. 112

Fig. 113



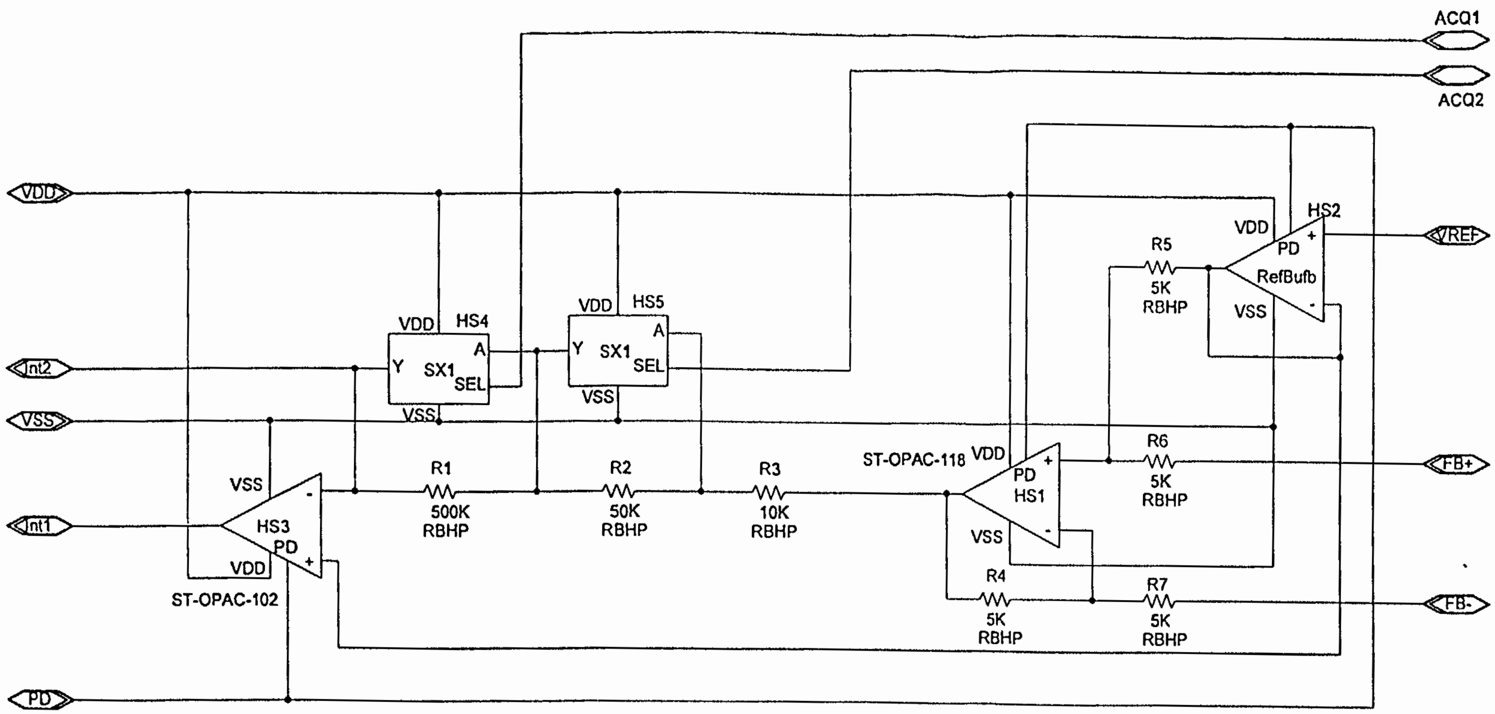

ACQ1
ACQ2
VDD
Int2
VSS
Int1
PD
VREF
FB+
FB-
VDD
HS4
Y
SX1
A
SEL
VSS
VDD
HS5
Y
SX1
A
SEL
VSS
R1
500K
RBHP
R2
50K
RBHP
R3
10K
RBHP
VSS
HS3
PD
VDD
ST-OPAC-102
ST-OPAC-118
VDD
PD
HS1
VSS
R4
5K
RBHP
R5
5K
RBHP
R6
5K
RBHP
R7
5K
RBHP
VDD
HS2
PD
RefBufb
VSS

FIG. 114

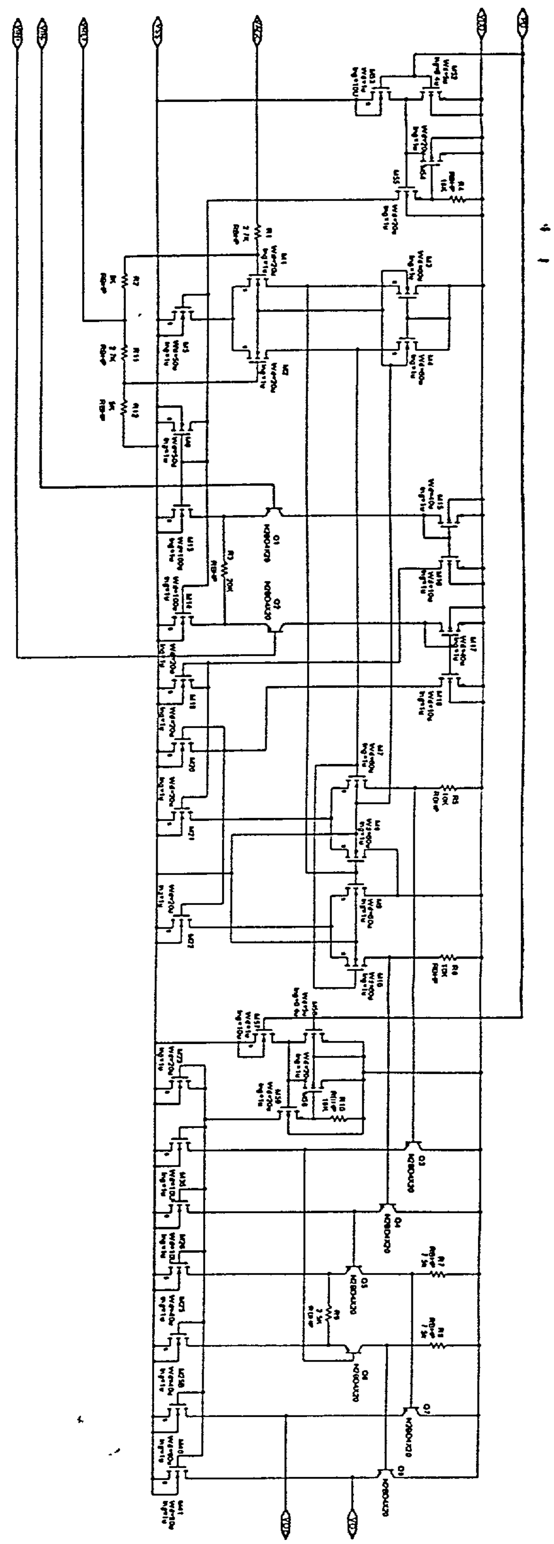


FIG. 115

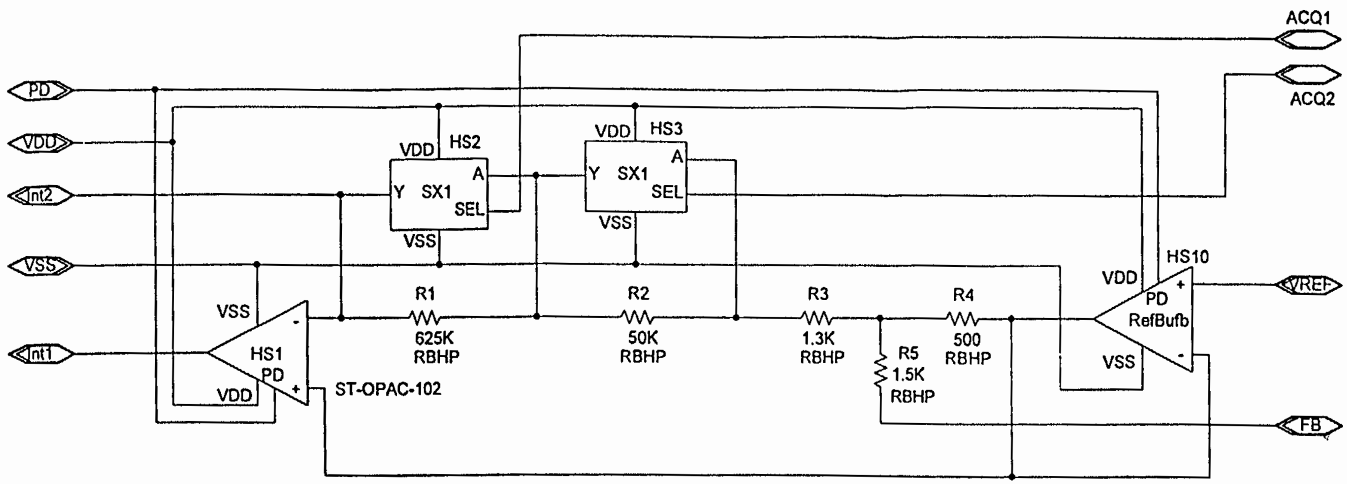

ACQ1
ACQ2
PD
VDD
Int2
VSS
Int1
VDD
HS2
Y
SX1
A
SEL
VSS
VDD
HS3
Y
SX1
A
SEL
VSS
VSS
HS1
PD
VDD
ST-OPAC-102
R1
625K
RBHP
R2
50K
RBHP
R3
1.3K
RBHP
R4
500
RBHP
R5
1.5K
RBHP
VDD
HS10
PD
RefBufb
VSS
VREF
FB

FIG. 116

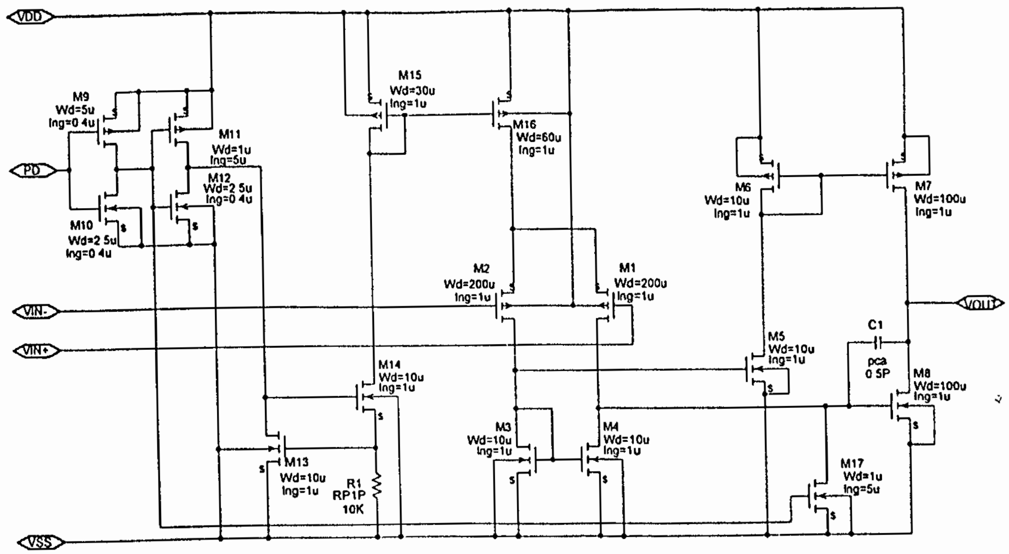


FIG 117

09632856 .080400

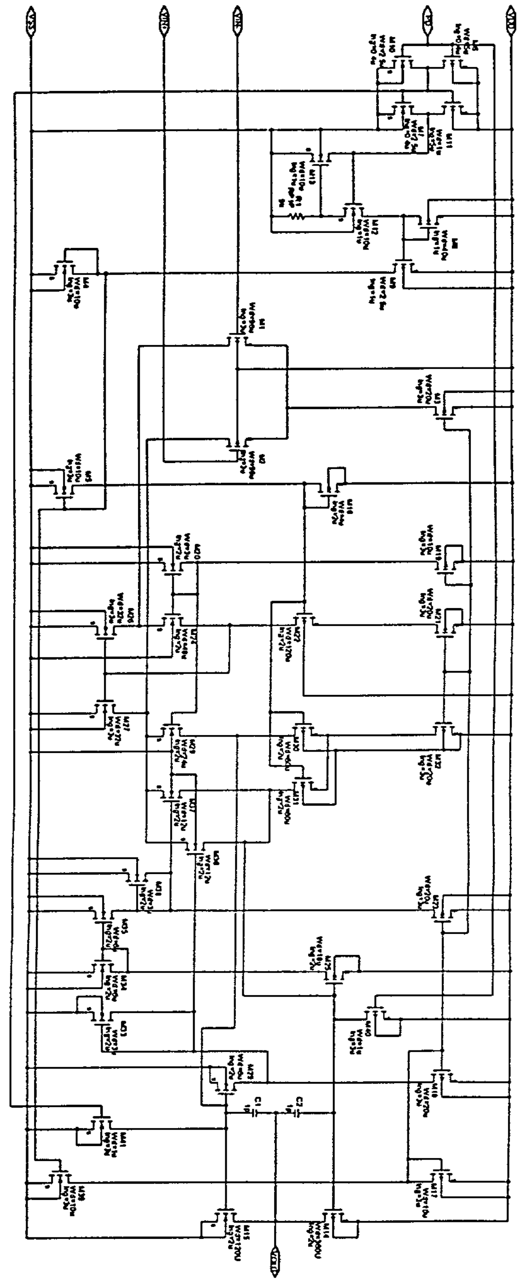


Fig 118

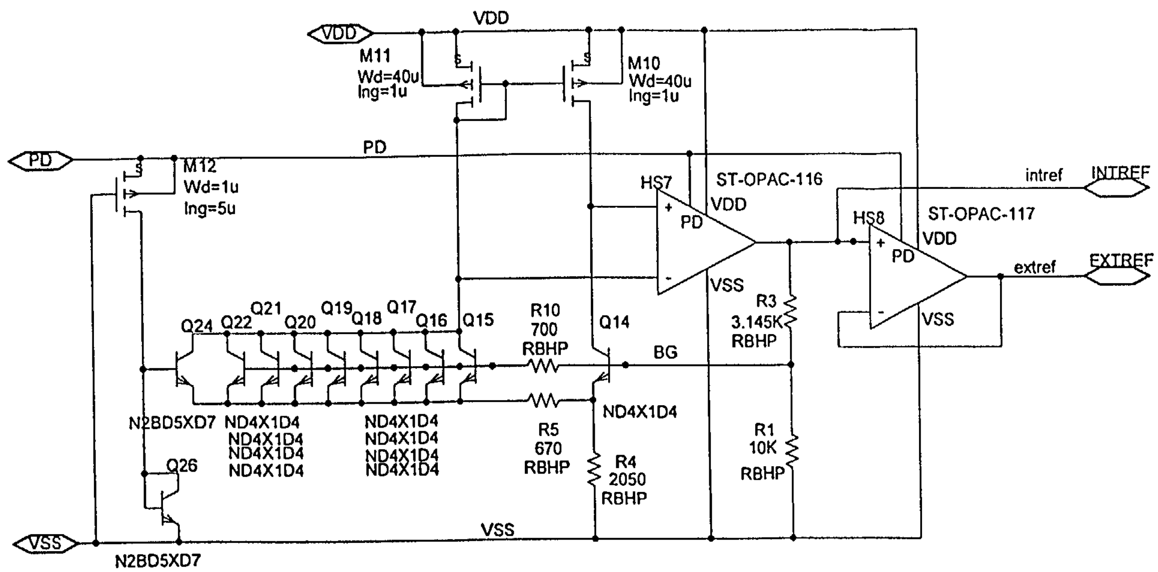

VDD
VDD
M11
Wd=40u
lng=1u
M10
Wd=40u
lng=1u
PD
PD
M12
Wd=1u
lng=5u
HS7
ST-OPAC-116
PD
VDD
VSS
HS8
ST-OPAC-117
PD
VDD
VSS
intref
INTREF
extref
EXTREF
Q24
Q22
Q21
Q20
Q19
Q18
Q17
Q16
Q15
R10
700
RBHP
Q14
BG
R3
3.145K
RBHP
N2BD5XD7
ND4X1D4
ND4X1D4
ND4X1D4
ND4X1D4
ND4X1D4
ND4X1D4
ND4X1D4
ND4X1D4
R5
670
RBHP
ND4X1D4
R4
2050
RBHP
R1
10K
RBHP
Q26
VSS
VSS
N2BD5XD7

Fig. 119

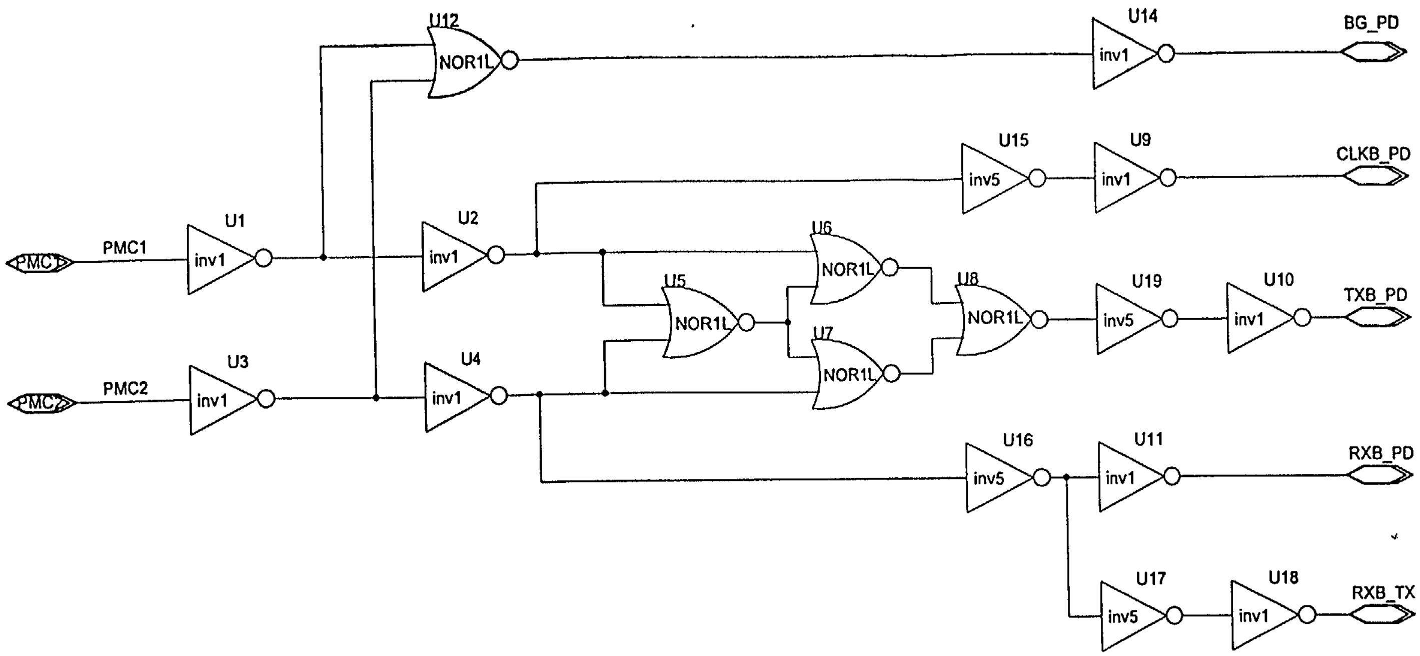
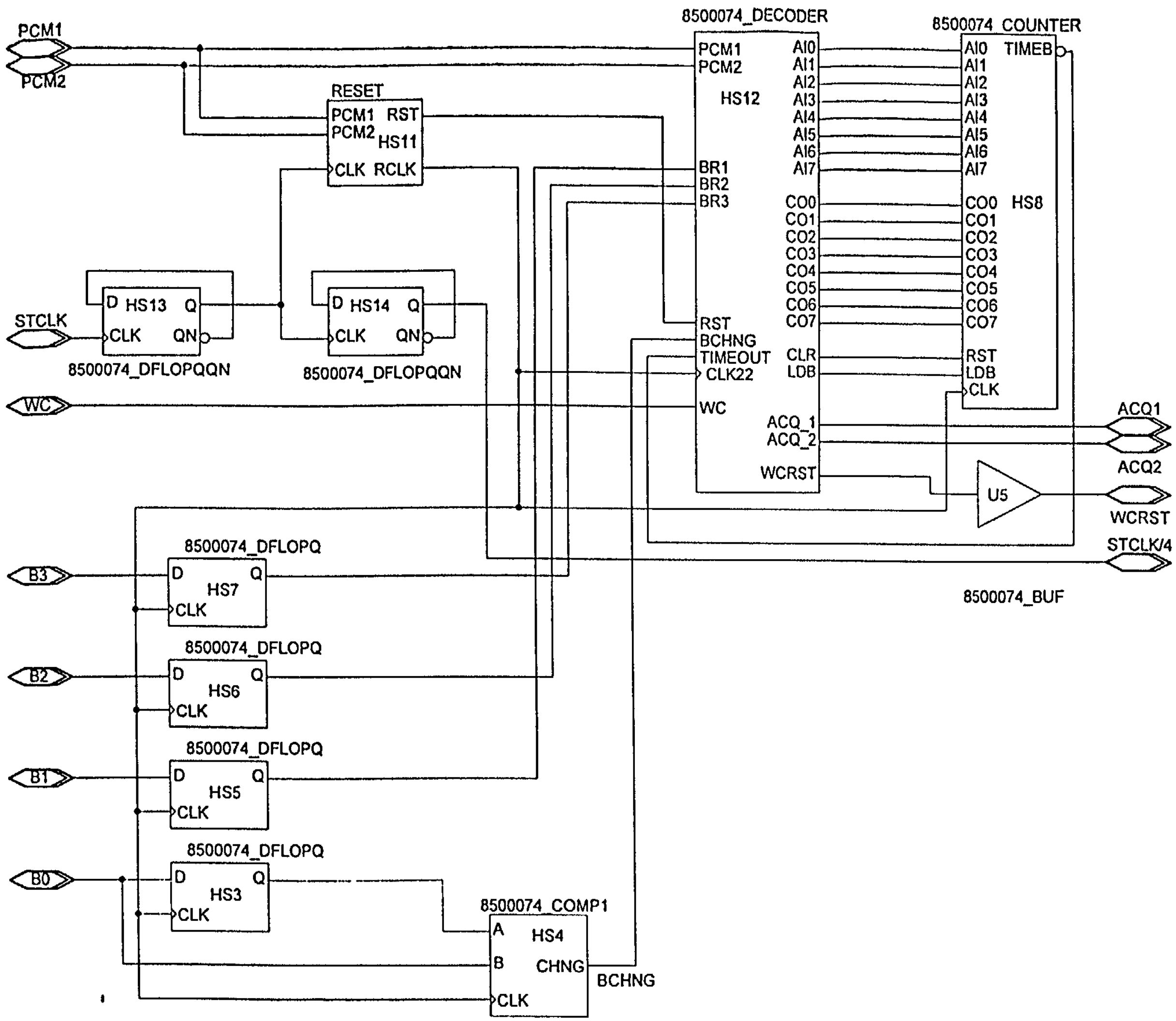

U12
NOR1L
U14
inv1
BG_PD
U15
inv5
U9
inv1
CLKB_PD
PMC1
PMC1
U1
inv1
U2
inv1
U6
NOR1L
U5
NOR1L
U8
NOR1L
U19
inv5
U10
inv1
TXB_PD
U7
NOR1L
PMC2
PMC2
U3
inv1
U4
inv1
U16
inv5
U11
inv1
RXB_PD
U17
inv5
U18
inv1
RXB_TX

FIG. 120



PCM1
PCM2
8500074_DECODER
HS12
PCM1
PCM2
BR1
BR2
BR3
RST
BCHNG
TIMEOUT
CLK22
WC
AI0
AI1
AI2
AI3
AI4
AI5
AI6
AI7
CO0
CO1
CO2
CO3
CO4
CO5
CO6
CO7
CLR
LDB
ACQ_1
ACQ_2
WCRST
8500074_COUNTER
HS8
TIMEB
RST
LDB
CLK
RESET
HS11
PCM1
PCM2
RST
CLK
RCLK
STCLK
HS13
HS14
D
Q
CLK
QN
8500074_DFLOPQQN
8500074_DFLOPQQN
WC
ACQ1
ACQ2
U5
WCRST
STCLK/4
8500074_BUF
B3
B2
B1
B0
8500074_DFLOPQ
HS7
HS6
HS5
HS3
8500074_COMP1
HS4
A
B
CLK
CHNG
BCHNG

FIG. 121

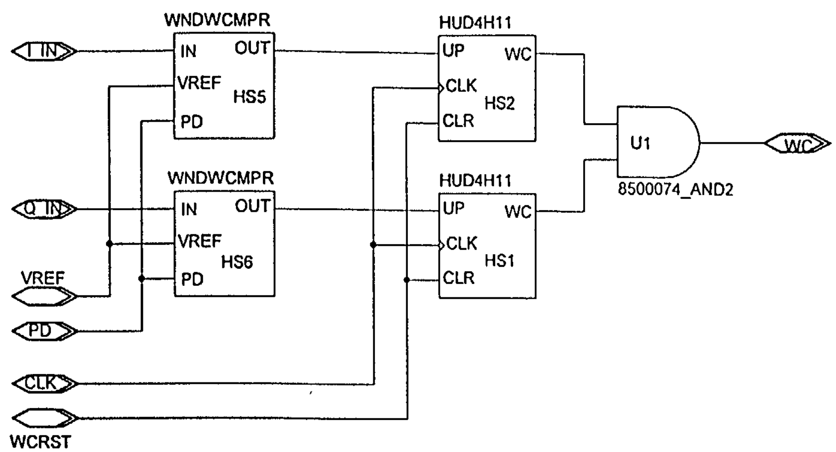

WNDWCMPR
IN
OUT
VREF
HS5
PD
WNDWCMPR
IN
OUT
VREF
HS6
PD
HUD4H11
UP
WC
CLK
HS2
CLR
HUD4H11
UP
WC
CLK
HS1
CLR
U1
8500074_AND2
I IN
Q IN
VREF
PD
CLK
WCRST
WC

FIG 122

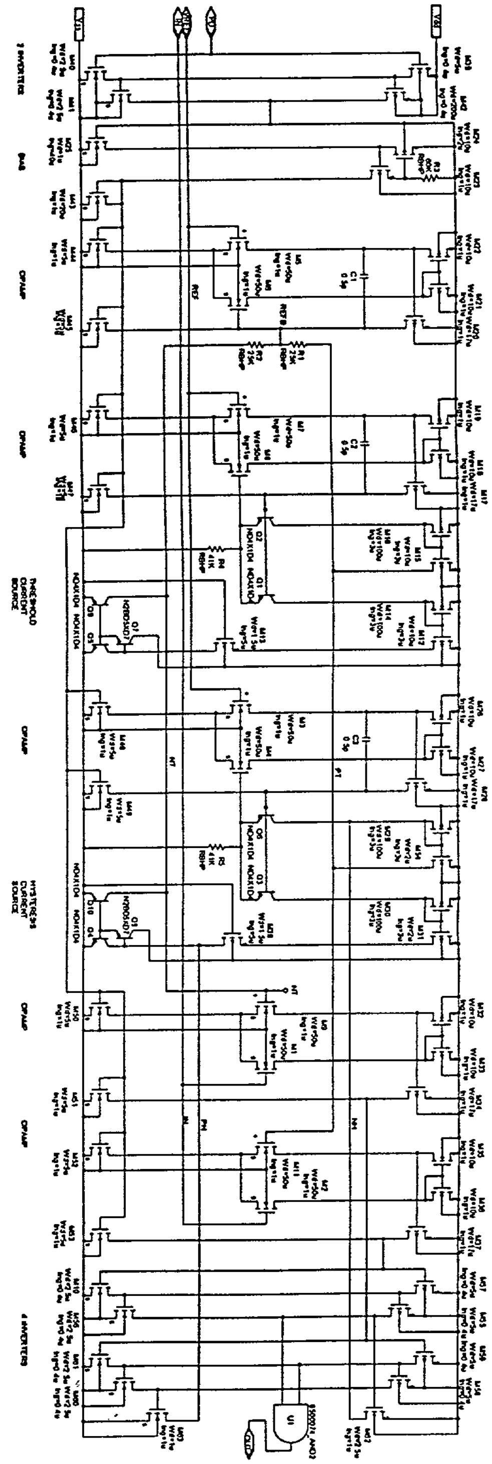


FIG. 123

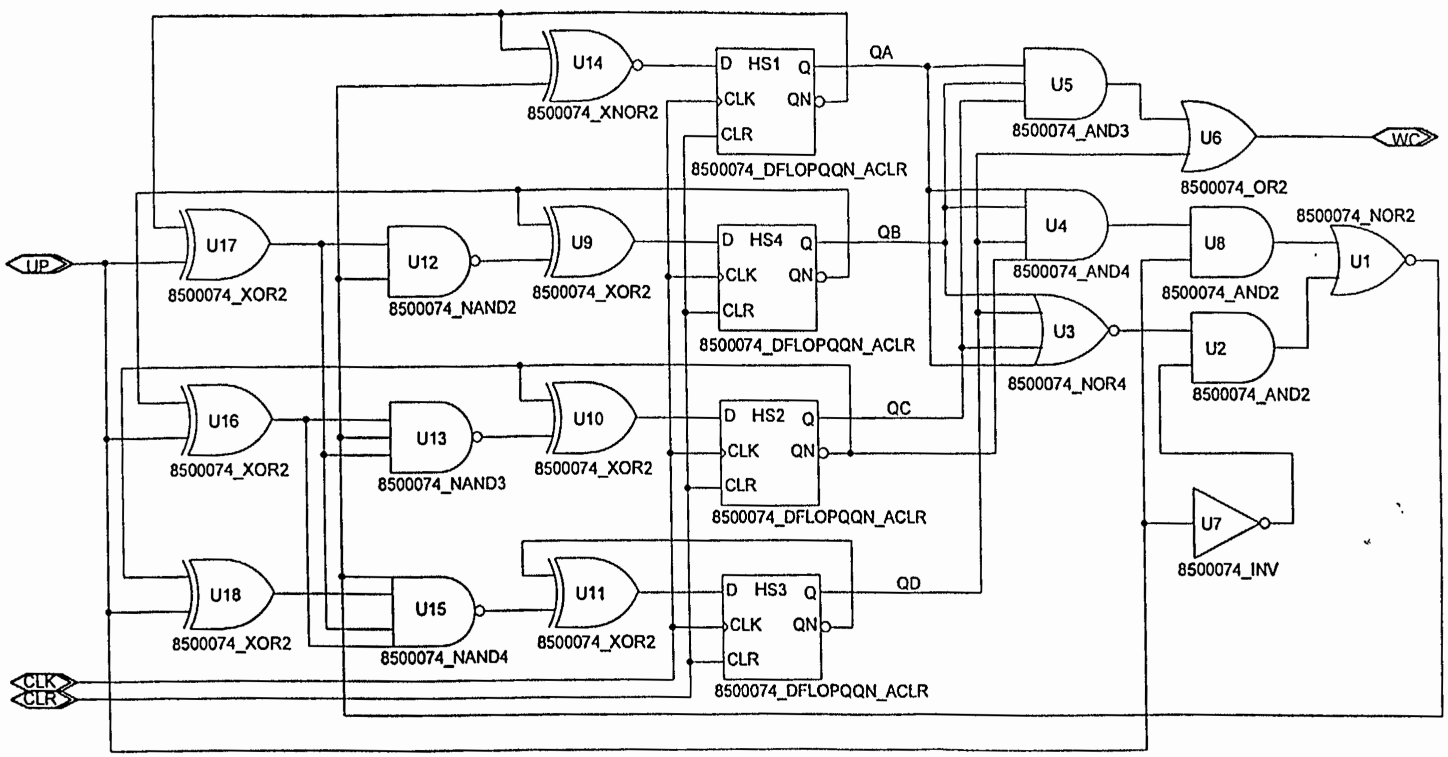
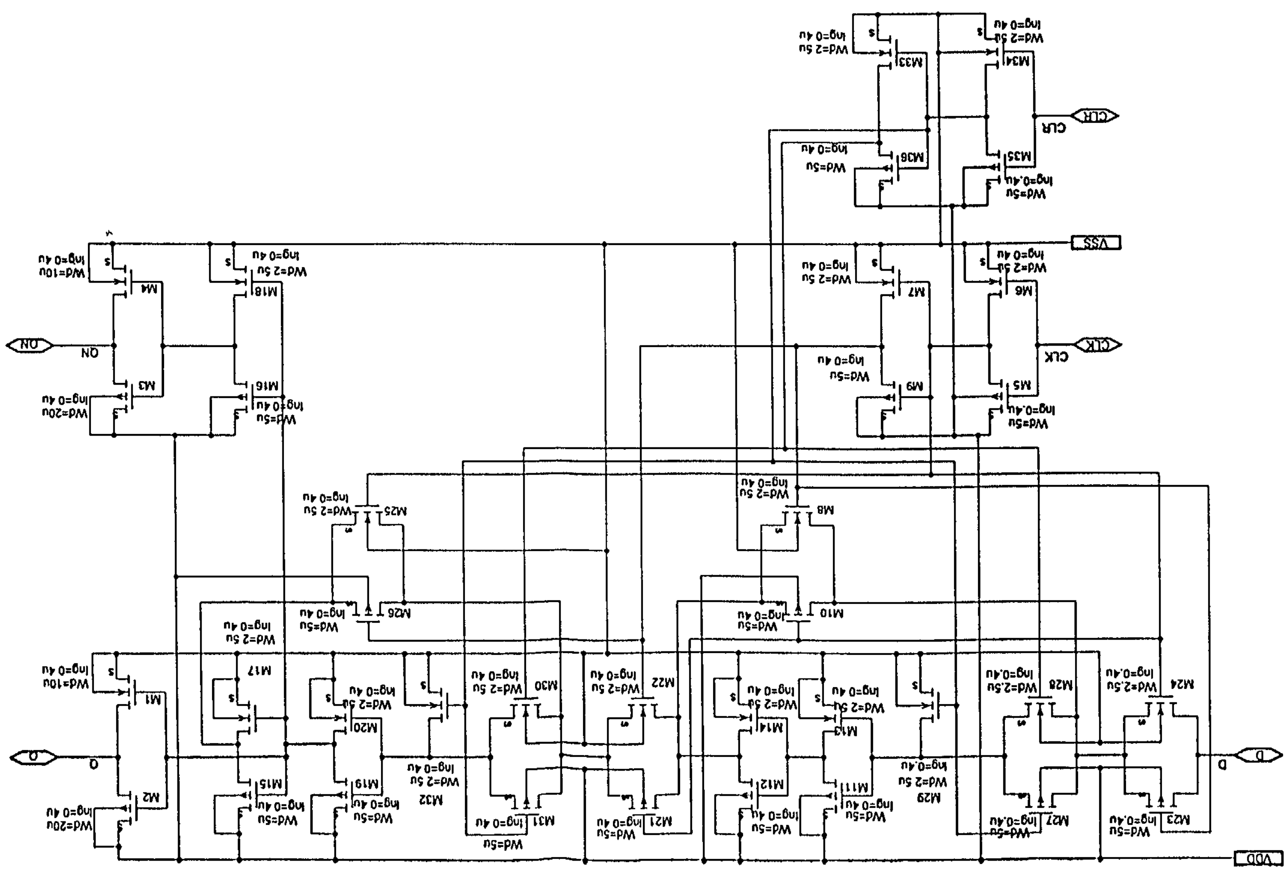

UP
CLK
CLR
U14
8500074_XNOR2
HS1
D
Q
CLK
QN
CLR
8500074_DFLOPQQN_ACLR
QA
U5
8500074_AND3
U6
8500074_OR2
WC
U17
8500074_XOR2
U12
8500074_NAND2
U9
8500074_XOR2
HS4
8500074_DFLOPQQN_ACLR
QB
U4
8500074_AND4
U8
8500074_AND2
8500074_NOR2
U1
U3
8500074_NOR4
U2
8500074_AND2
U16
8500074_XOR2
U13
8500074_NAND3
U10
8500074_XOR2
HS2
8500074_DFLOPQQN_ACLR
QC
U7
8500074_INV
U18
8500074_XOR2
U15
8500074_NAND4
U11
8500074_XOR2
HS3
8500074_DFLOPQQN_ACLR
QD

FIG 124

Fig. 125



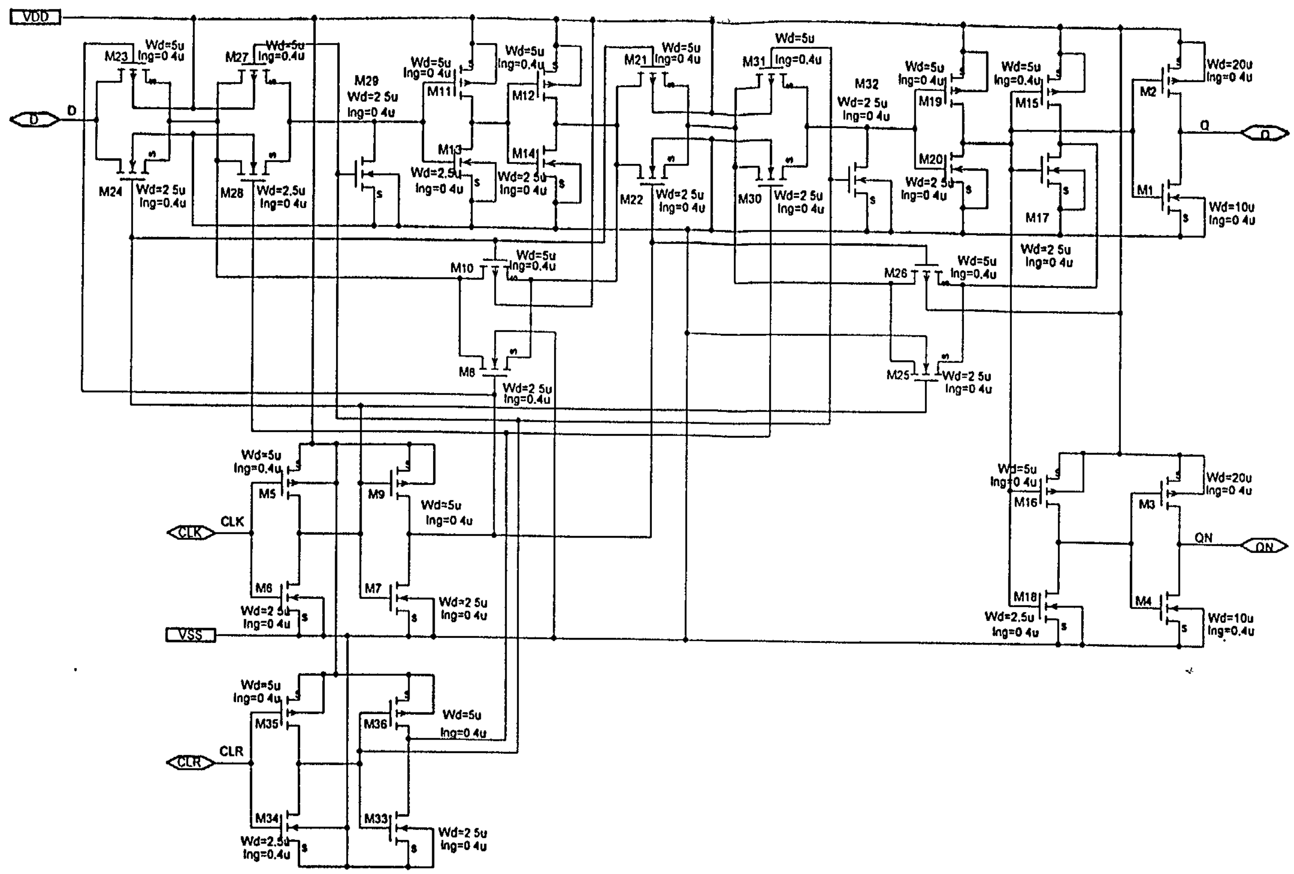

VDD
VSS
D
Q
QN
CLK
CLR
M1
M2
M3
M4
M5
M6
M7
M8
M9
M10
M11
M12
M13
M14
M15
M16
M17
M18
M19
M20
M21
M22
M23
M24
M25
M26
M27
M28
M29
M30
M31
M32
M33
M34
M35
M36
Wd=5u
lng=0.4u
Wd=2.5u
Wd=20u
Wd=10u

FIG 126

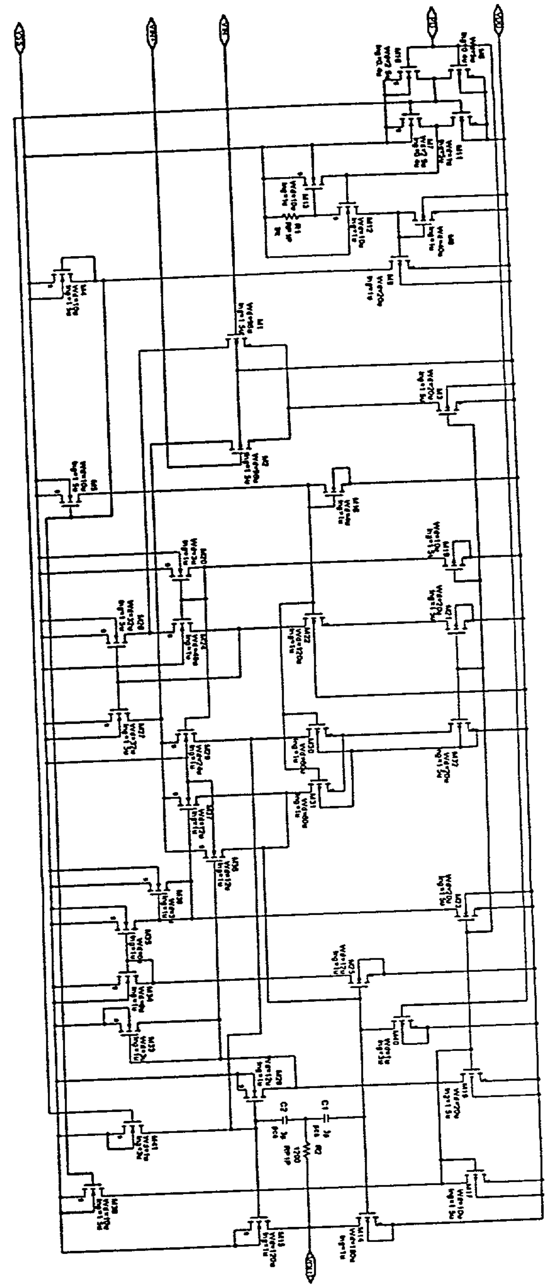
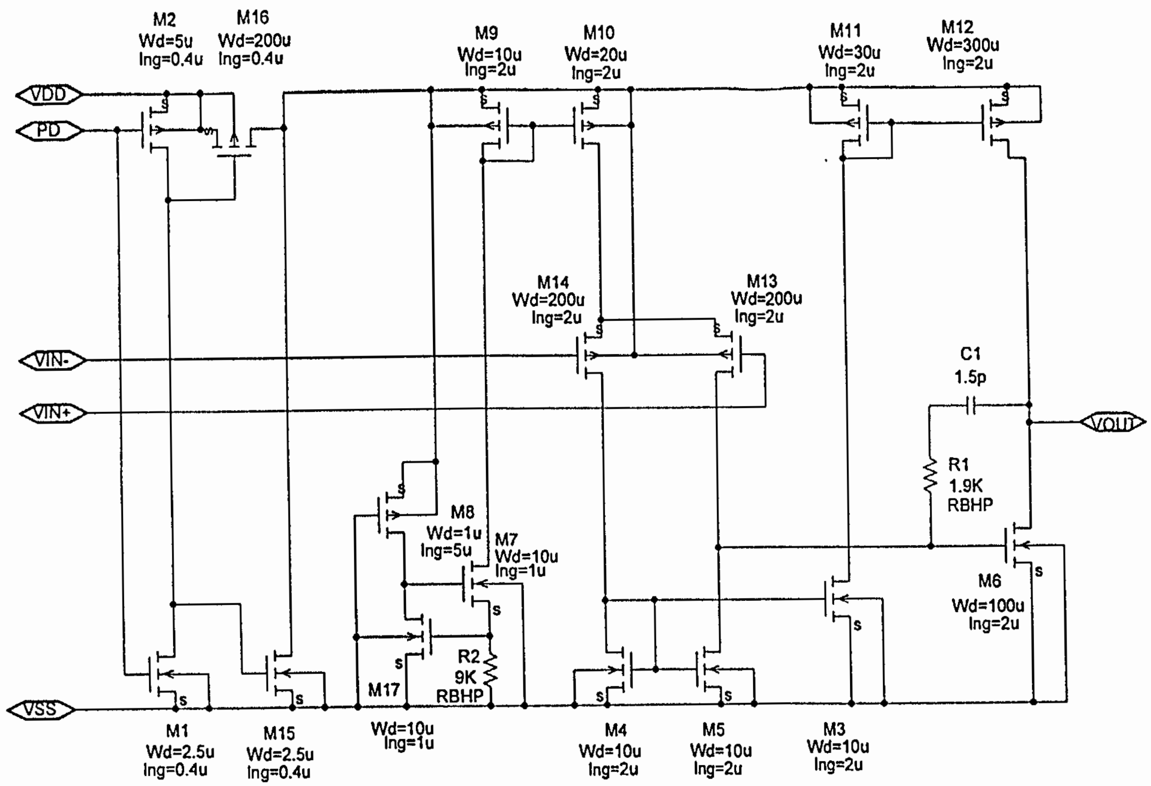


FIG. 12T



M2
Wd=5u
lng=0.4u
M16
Wd=200u
lng=0.4u
M9
Wd=10u
lng=2u
M10
Wd=20u
lng=2u
M11
Wd=30u
lng=2u
M12
Wd=300u
lng=2u
VDD
PD
M14
Wd=200u
lng=2u
M13
Wd=200u
lng=2u
VIN-
VIN+
C1
1.5p
VOUT
R1
1.9K
RBHP
M8
Wd=1u
lng=5u
M7
Wd=10u
lng=1u
M6
Wd=100u
lng=2u
R2
9K
RBHP
M17
VSS
M1
Wd=2.5u
lng=0.4u
M15
Wd=2.5u
lng=0.4u
Wd=10u
lng=1u
M4
Wd=10u
lng=2u
M5
Wd=10u
lng=2u
M3
Wd=10u
lng=2u

FIG. 128

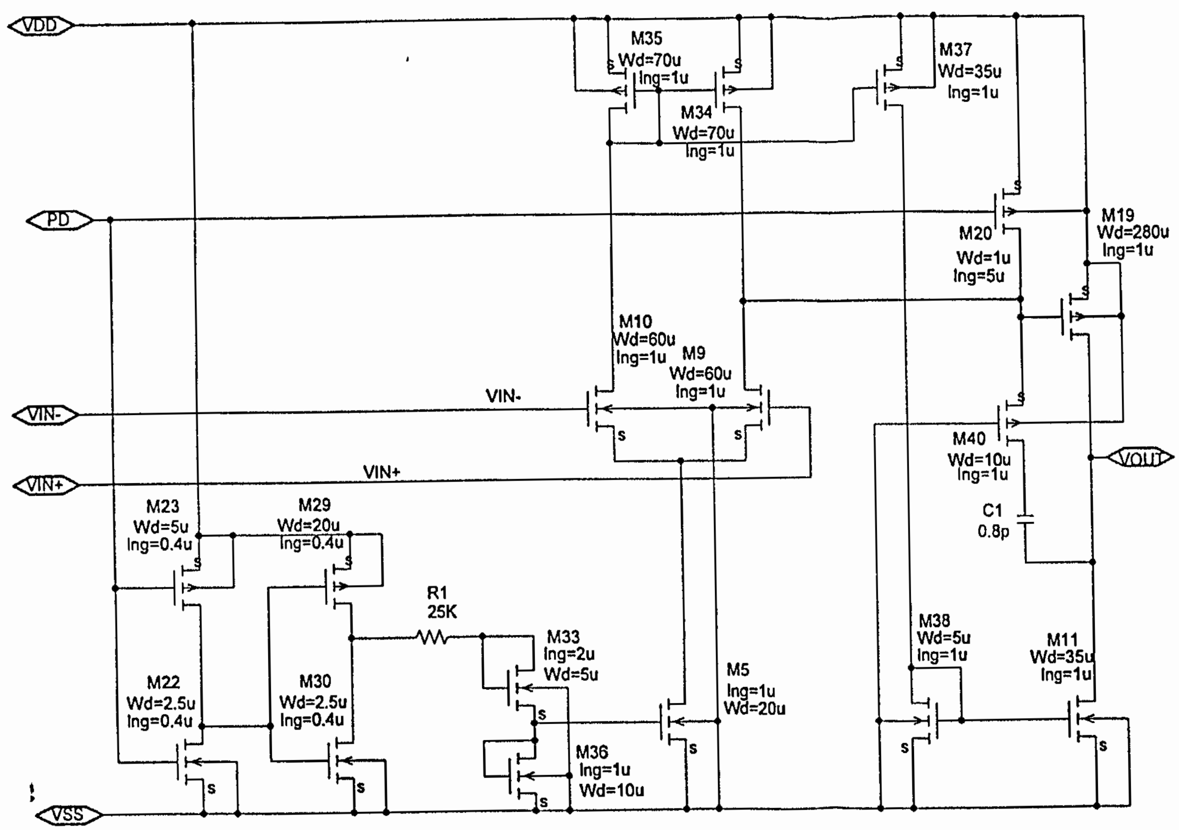

VDD
M35
Wd=70u
lng=1u
M34
Wd=70u
lng=1u
M37
Wd=35u
lng=1u
PD
M20
Wd=1u
lng=5u
M19
Wd=280u
lng=1u
M10
Wd=60u
lng=1u
M9
Wd=60u
lng=1u
VIN-
VIN+
M40
Wd=10u
lng=1u
VOUT
C1
0.8p
M23
Wd=5u
lng=0.4u
M29
Wd=20u
lng=0.4u
R1
25K
M33
lng=2u
Wd=5u
M22
Wd=2.5u
lng=0.4u
M30
Wd=2.5u
lng=0.4u
M36
lng=1u
Wd=10u
M5
lng=1u
Wd=20u
M38
Wd=5u
lng=1u
M11
Wd=35u
lng=1u
VSS

FIG. 129

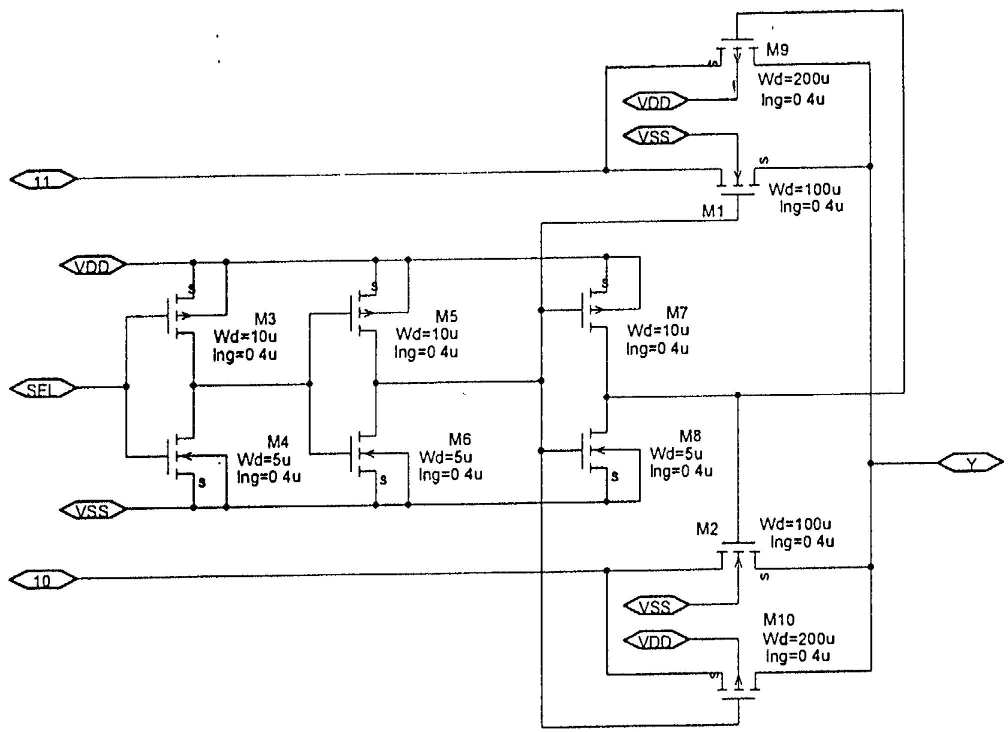


FIG 130

09632256 .060400

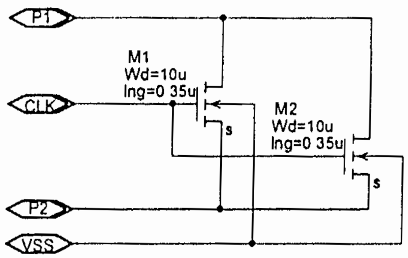


FIG. 131

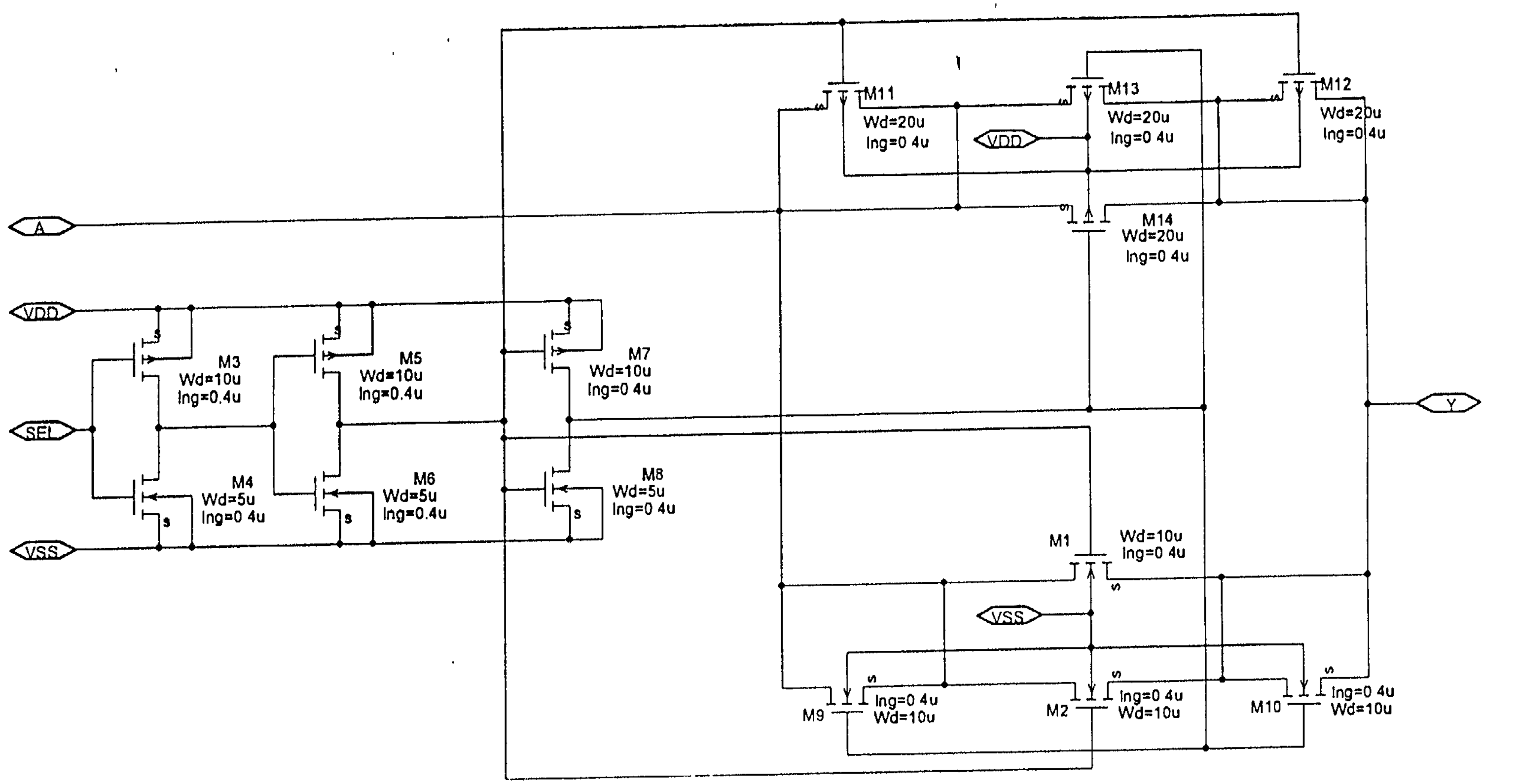
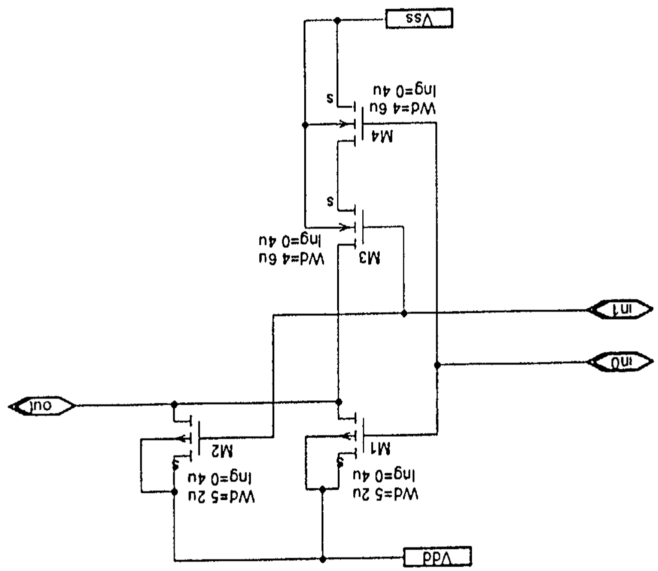

A
VDD
SEL
VSS
Y
M3
Wd=10u
lng=0.4u
M4
Wd=5u
lng=0 4u
M5
Wd=10u
lng=0.4u
M6
Wd=5u
lng=0.4u
M7
Wd=10u
lng=0 4u
M8
Wd=5u
lng=0 4u
M11
Wd=20u
lng=0 4u
M13
Wd=20u
lng=0 4u
M12
Wd=20u
lng=0 4u
M14
Wd=20u
lng=0 4u
M1
Wd=10u
lng=0 4u
M9
lng=0 4u
Wd=10u
M2
lng=0 4u
Wd=10u
M10
lng=0 4u
Wd=10u

FIG. 132

09525960 . 080400

Fig. 133



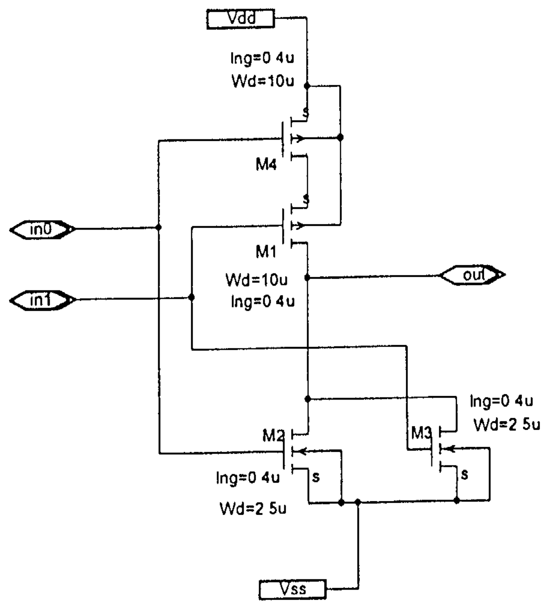

Vdd
lng=0 4u
Wd=10u
M4
in0
M1
Wd=10u
lng=0 4u
out
in1
lng=0 4u
Wd=2 5u
M2
M3
lng=0 4u
Wd=2 5u
Vss

FIG. 134

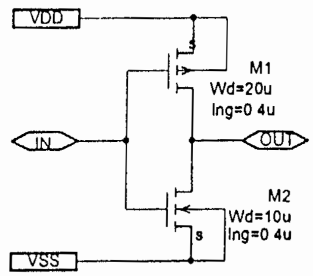


FIG. 135

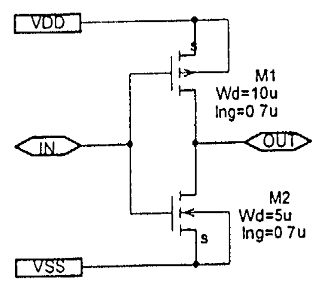


FIG. 13G

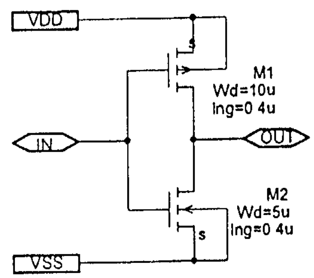


FIG 137

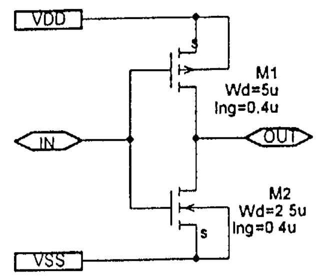


Fig. 138

09632856 .080400

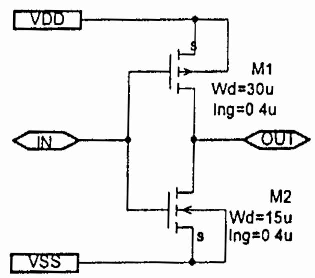


Fig 139

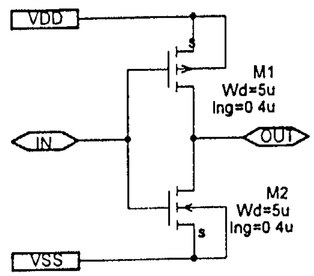


FIG. 140

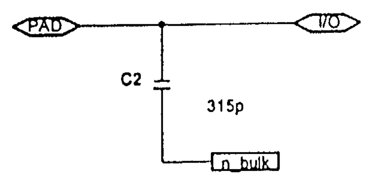


Fig. 141

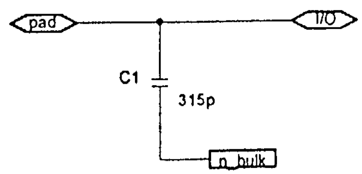
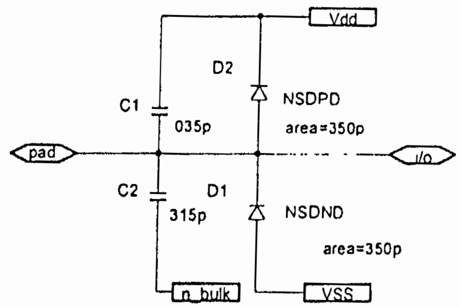


FIG 142



Vdd
D2
C1
NSDPD
035p
area=350p
pad
i/o
C2
D1
315p
NSDND
area=350p
n_bulk
VSS

FIG 143

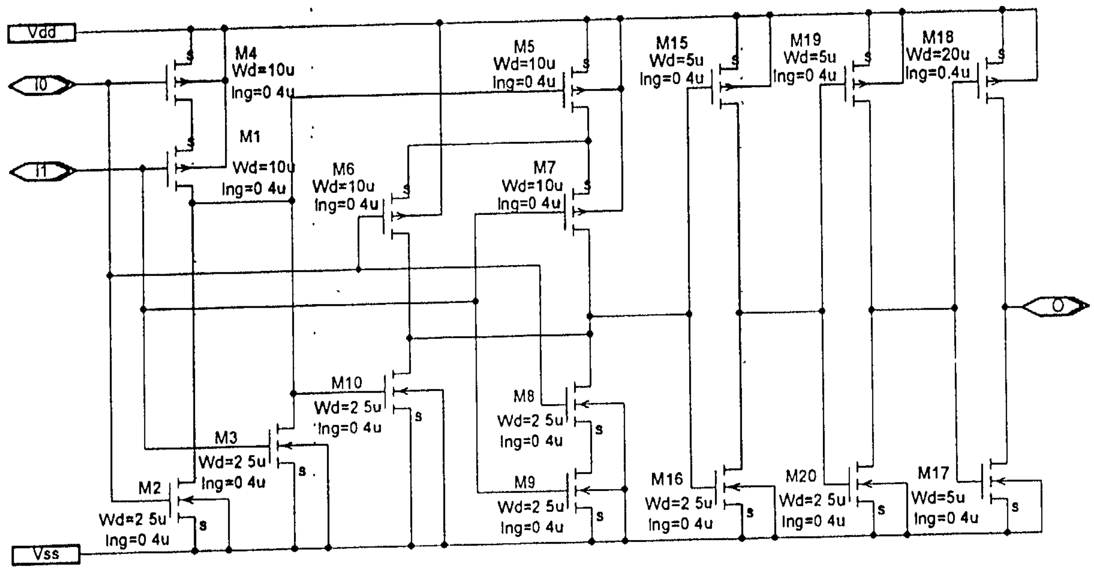


FIG 144

09632056 .080400

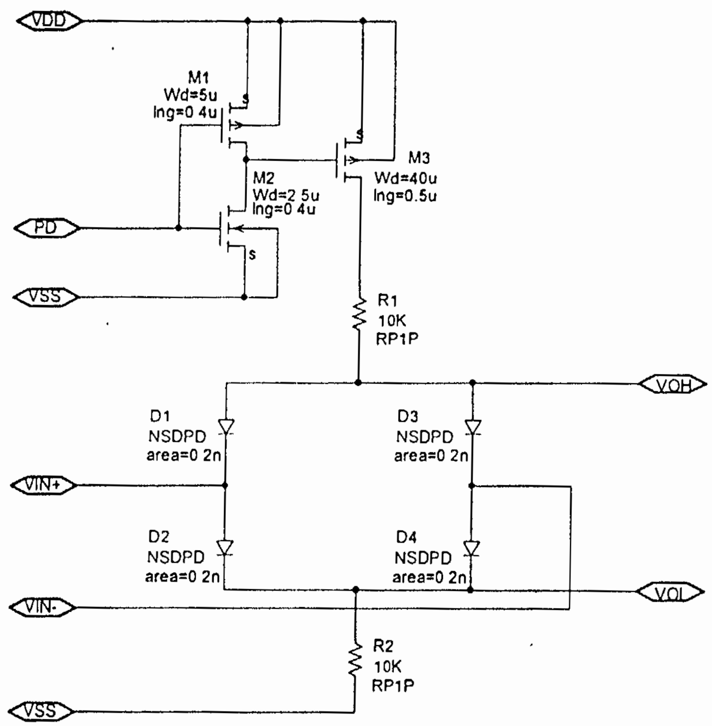

VDD
M1
Wd=5u
lng=0 4u
s
M3
Wd=40u
lng=0.5u
M2
Wd=2 5u
lng=0 4u
PD
s
VSS
R1
10K
RP1P
VOH
D1
NSDPD
area=0 2n
D3
NSDPD
area=0 2n
VIN+
D2
NSDPD
area=0 2n
D4
NSDPD
area=0 2n
VIN-
VOL
R2
10K
RP1P
VSS

FIG. 145

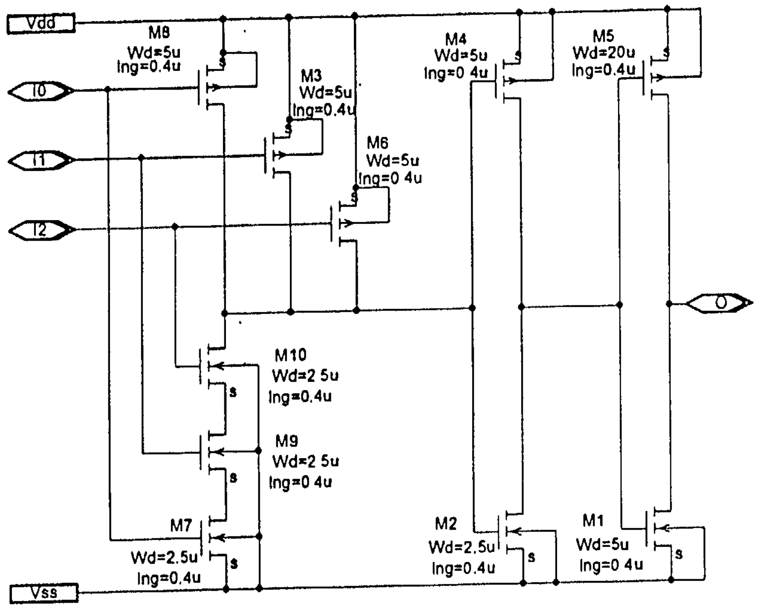

Vdd
M8
Wd=5u
lng=0.4u
M3
Wd=5u
lng=0.4u
M6
Wd=5u
lng=0 4u
M4
Wd=5u
lng=0 4u
M5
Wd=20u
lng=0.4u
I0
I1
I2
O
M10
Wd=2 5u
lng=0.4u
M9
Wd=2 5u
lng=0 4u
M7
Wd=2.5u
lng=0.4u
M2
Wd=2.5u
lng=0.4u
M1
Wd=5u
lng=0 4u
Vss
s

FIG. 146

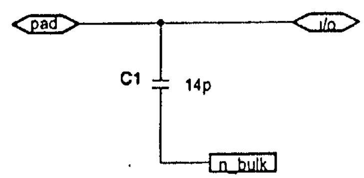


FIG. 147

09632856 . 080400

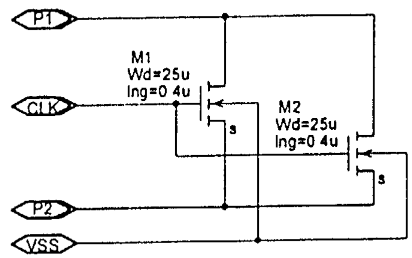


FIG. 148

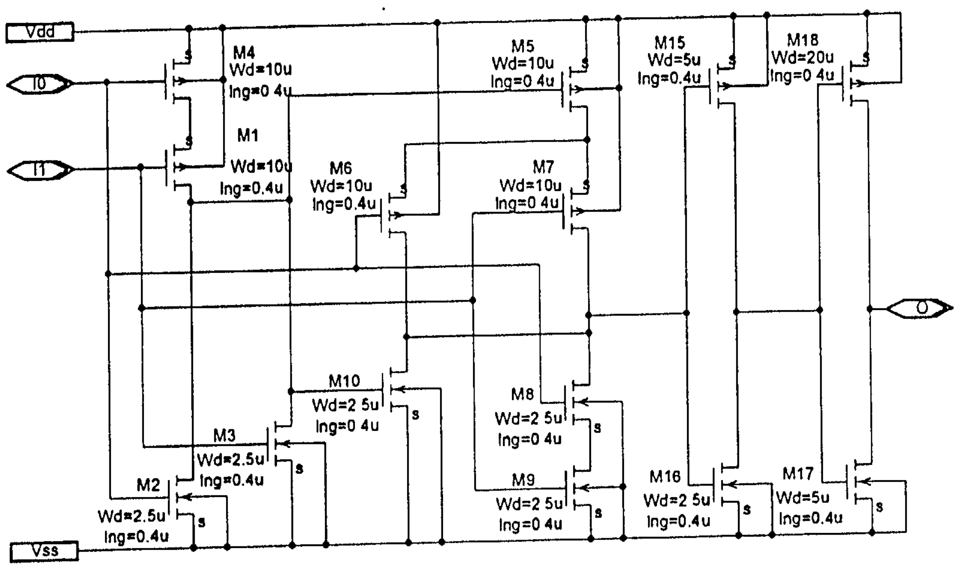


Fig. 149

09632856 .080400

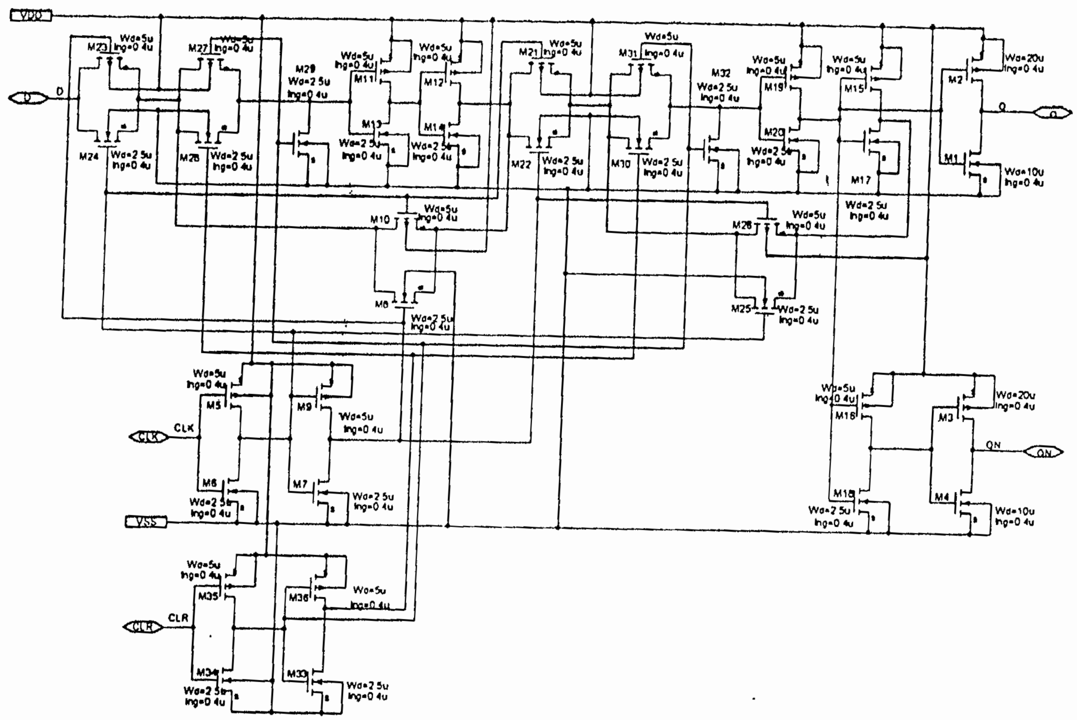

VDD
D
Q
QN
CLK
VSS
CLR
M1
M2
M3
M4
M5
M6
M7
M8
M9
M10
M11
M12
M13
M14
M15
M16
M17
M18
M19
M20
M21
M22
M23
M24
M25
M26
M27
M28
M29
M31
M32
M33
M34
M35
M36

Fig. 150

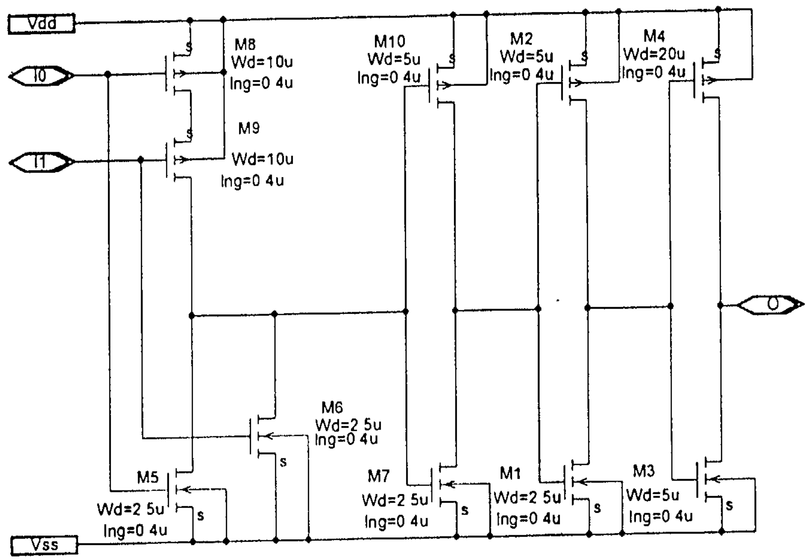

Vdd
I0
I1
M8
Wd=10u
lng=0 4u
M9
Wd=10u
lng=0 4u
M10
Wd=5u
lng=0 4u
M2
Wd=5u
lng=0 4u
M4
Wd=20u
lng=0 4u
O
M6
Wd=2 5u
lng=0 4u
M5
Wd=2 5u
lng=0 4u
M7
Wd=2 5u
lng=0 4u
M1
Wd=2 5u
lng=0 4u
M3
Wd=5u
lng=0 4u
Vss

FIG. 151

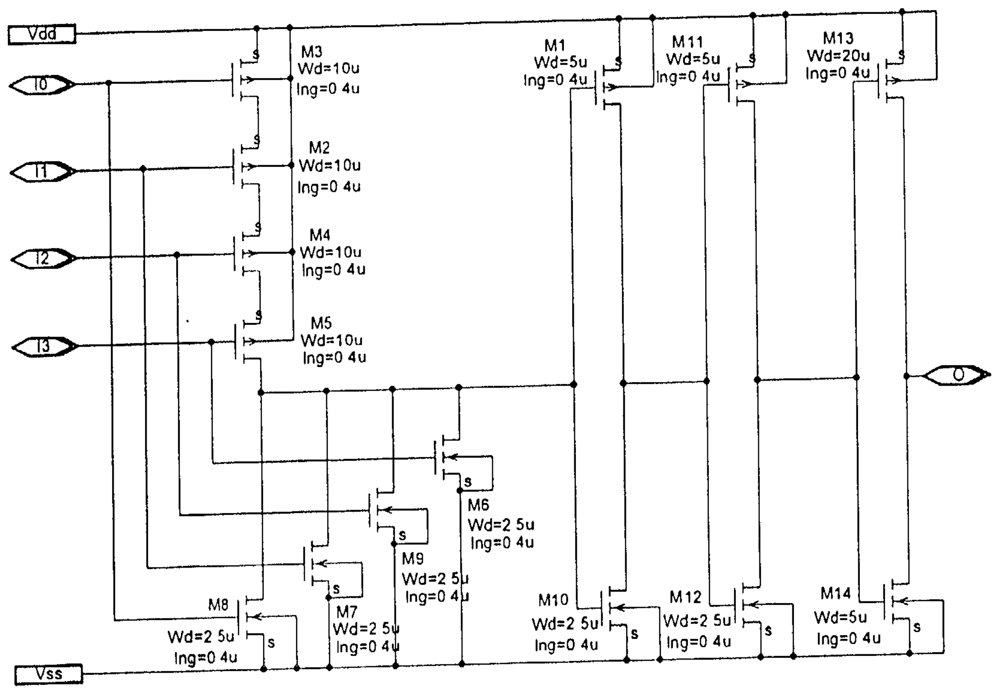

Vdd
I0
I1
I2
I3
M3
Wd=10u
lng=0 4u
M2
Wd=10u
lng=0 4u
M4
Wd=10u
lng=0 4u
M5
Wd=10u
lng=0 4u
M1
Wd=5u
lng=0 4u
M11
Wd=5u
lng=0 4u
M13
Wd=20u
lng=0 4u
O
M6
Wd=2 5u
lng=0 4u
M9
Wd=2 5u
lng=0 4u
M7
Wd=2 5u
lng=0 4u
M8
Wd=2 5u
lng=0 4u
M10
Wd=2 5u
lng=0 4u
M12
Wd=2 5u
lng=0 4u
M14
Wd=5u
lng=0 4u
Vss

FIG. 152

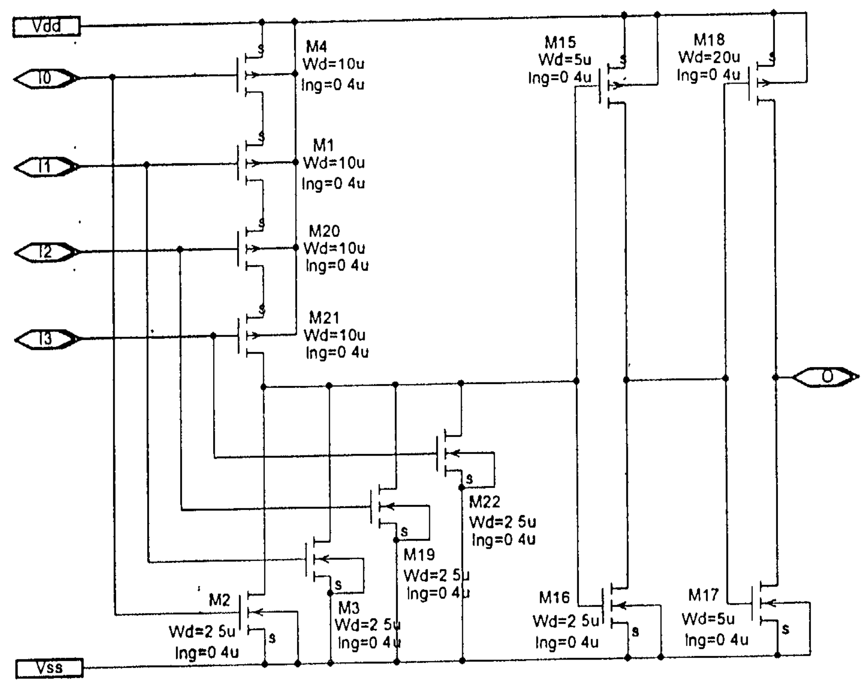
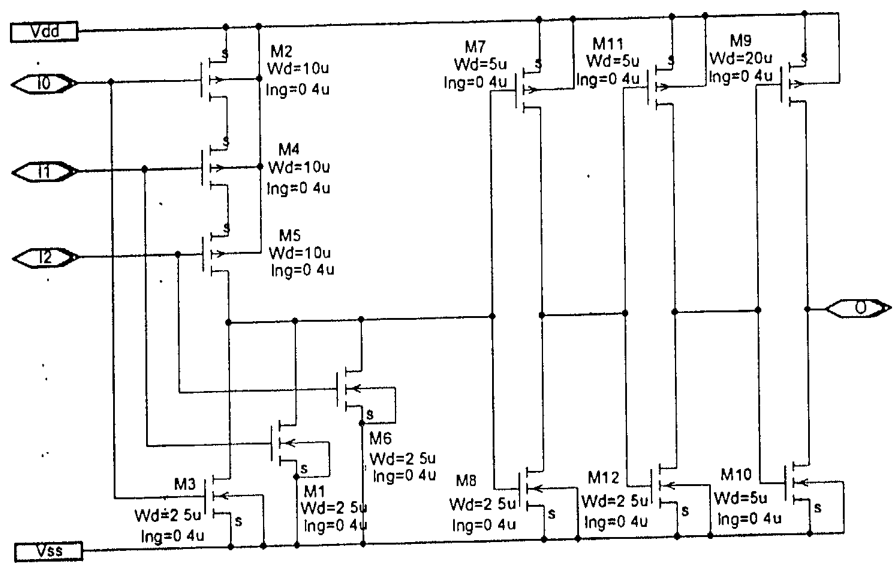

Vdd
I0
I1
I2
I3
M4
Wd=10u
lng=0 4u
M1
Wd=10u
lng=0 4u
M20
Wd=10u
lng=0 4u
M21
Wd=10u
lng=0 4u
M15
Wd=5u
lng=0 4u
M18
Wd=20u
lng=0 4u
O
M22
Wd=2 5u
lng=0 4u
M19
Wd=2 5u
lng=0 4u
M3
Wd=2 5u
lng=0 4u
M2
Wd=2 5u
lng=0 4u
M16
Wd=2 5u
lng=0 4u
M17
Wd=5u
lng=0 4u
Vss

FIG. 153



Vdd
I0
I1
I2
M2
Wd=10u
lng=0 4u
M4
Wd=10u
lng=0 4u
M5
Wd=10u
lng=0 4u
M7
Wd=5u
lng=0 4u
M11
Wd=5u
lng=0 4u
M9
Wd=20u
lng=0 4u
O
M6
Wd=2 5u
lng=0 4u
M3
Wd=2 5u
lng=0 4u
M1
Wd=2 5u
lng=0 4u
M8
Wd=2 5u
lng=0 4u
M12
Wd=2 5u
lng=0 4u
M10
Wd=5u
lng=0 4u
Vss

FIG. 154

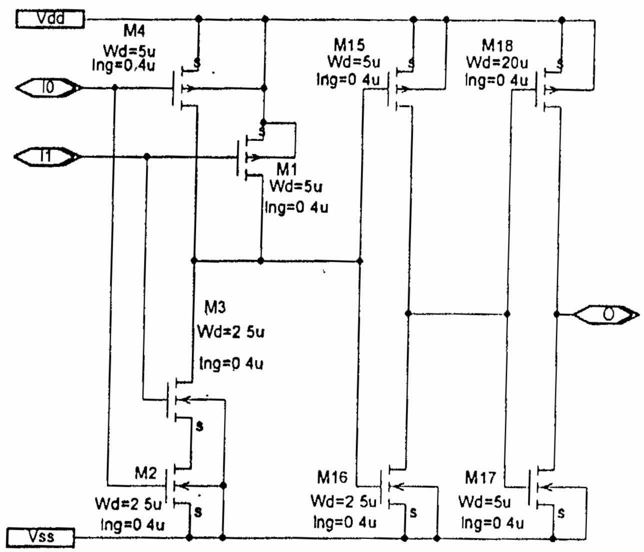

Vdd
M4
Wd=5u
lng=0.4u
s
I0
I1
s
M1
Wd=5u
lng=0 4u
M15
Wd=5u
lng=0 4u
s
M18
Wd=20u
lng=0 4u
s
O
M3
Wd=2 5u
lng=0 4u
s
M2
Wd=2 5u
lng=0 4u
s
Vss
M16
Wd=2 5u
lng=0 4u
s
M17
Wd=5u
lng=0 4u
s

FIG. 155

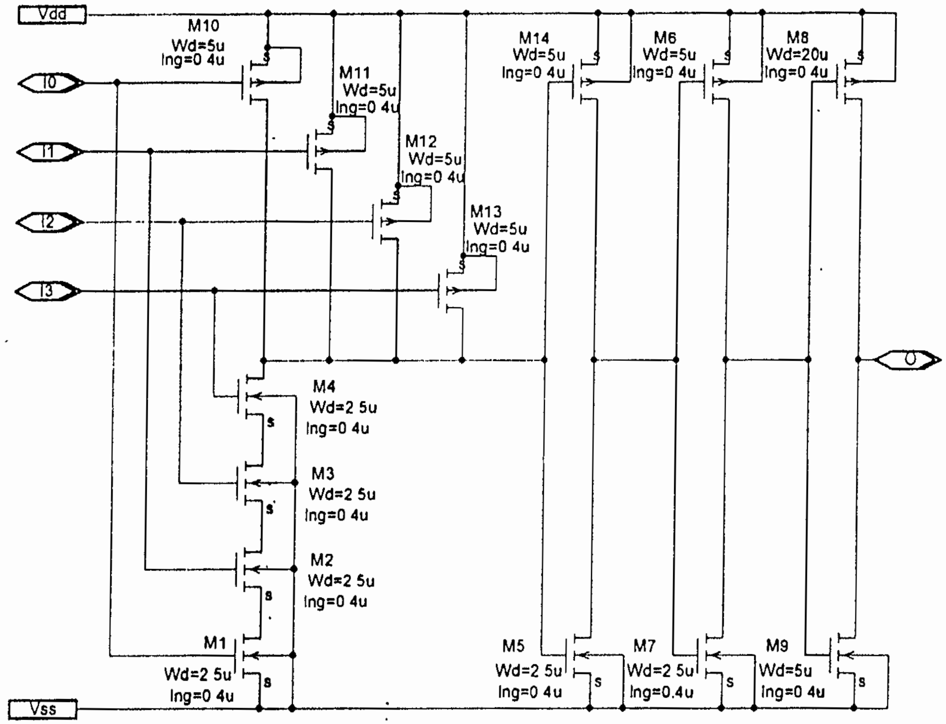

Vdd
M10
Wd=5u
lng=0 4u
I0
M11
Wd=5u
lng=0 4u
I1
M12
Wd=5u
lng=0 4u
I2
M13
Wd=5u
lng=0 4u
I3
M14
Wd=5u
lng=0 4u
M6
Wd=5u
lng=0 4u
M8
Wd=20u
lng=0 4u
O
M4
Wd=2 5u
lng=0 4u
M3
Wd=2 5u
lng=0 4u
M2
Wd=2 5u
lng=0 4u
M1
Wd=2 5u
lng=0 4u
M5
Wd=2 5u
lng=0 4u
M7
Wd=2 5u
lng=0.4u
M9
Wd=5u
lng=0 4u
Vss

FIG. 156

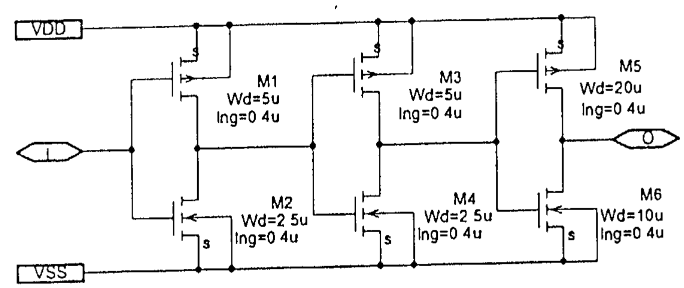
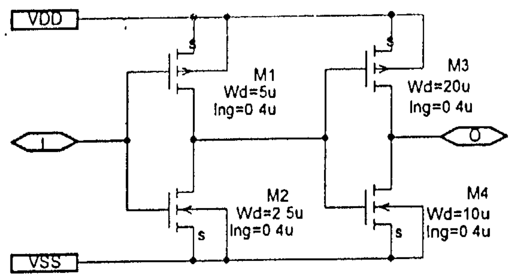


FIG. 157

09632856 .080400



VDD
M1
Wd=5u
lng=0 4u
M3
Wd=20u
lng=0 4u
I
O
M2
Wd=2 5u
lng=0 4u
M4
Wd=10u
lng=0 4u
VSS
s

FIG. 158

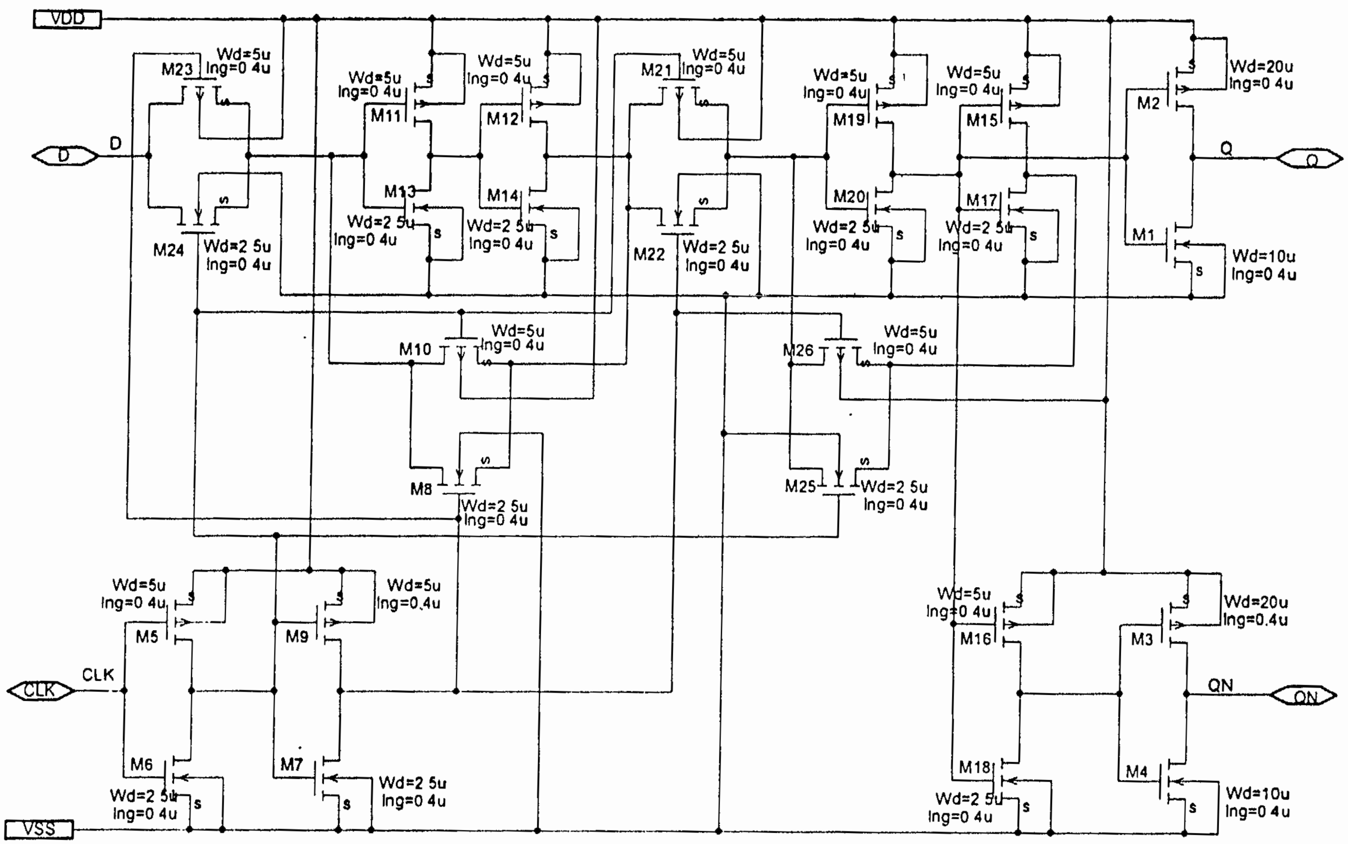
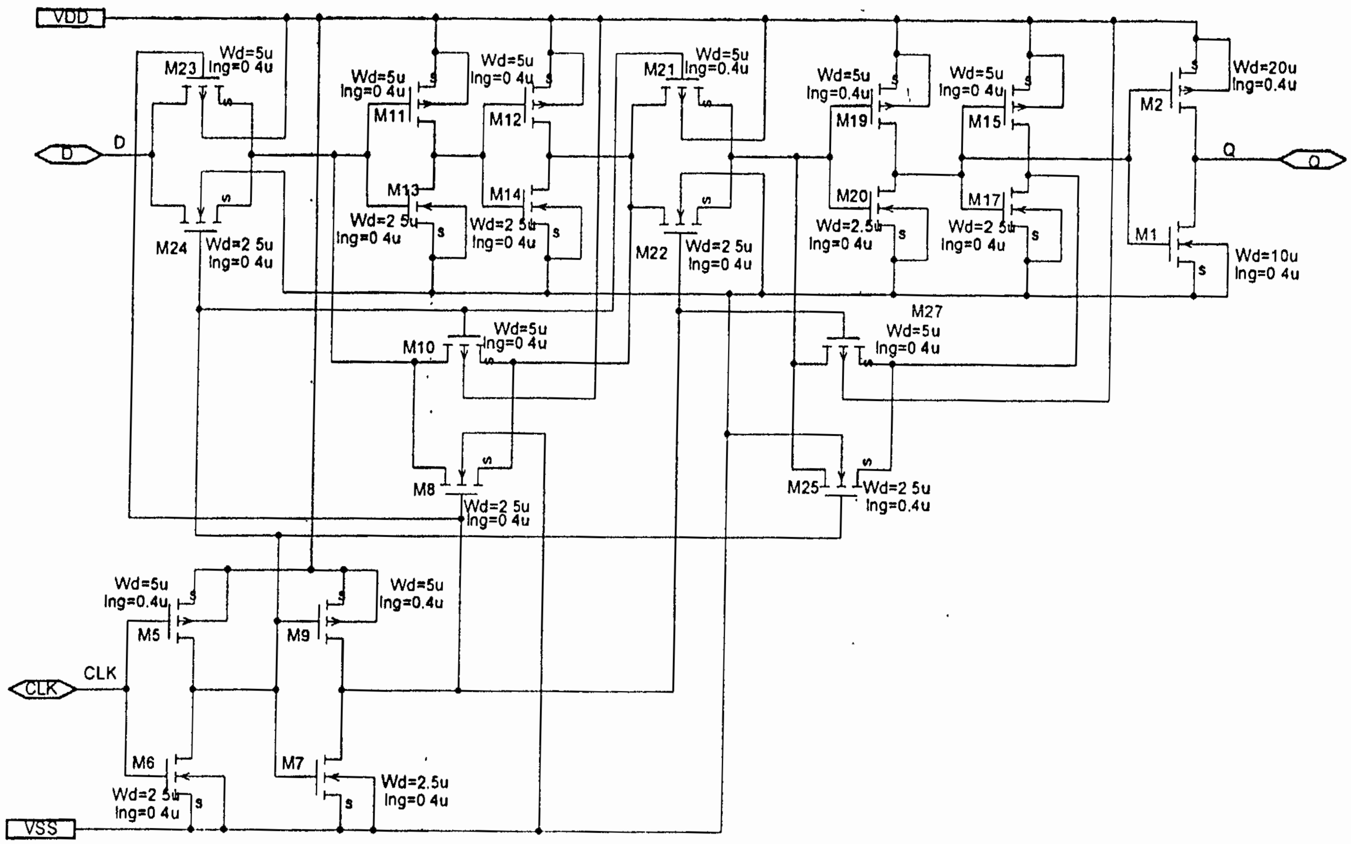
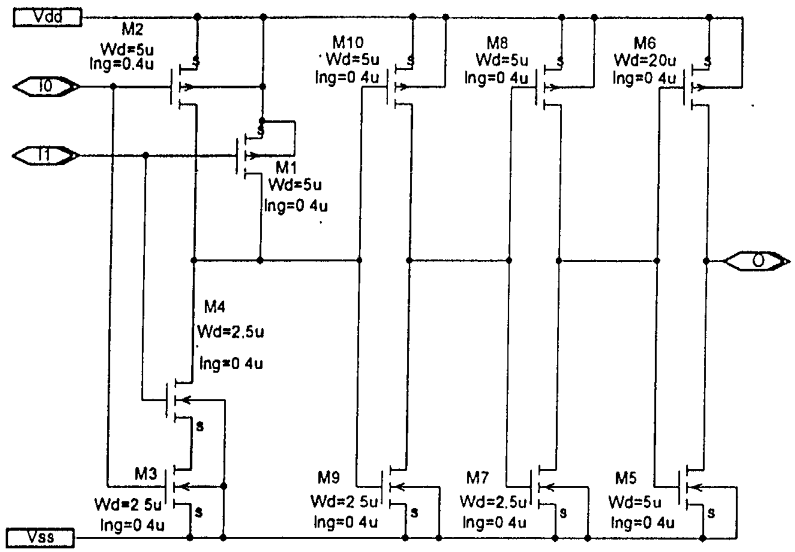


FIG 159



VDD
D
D
Q
Q
CLK
CLK
VSS
M23
Wd=5u
lng=0 4u
M24
Wd=2 5u
lng=0 4u
M11
Wd=5u
lng=0 4u
M12
Wd=5u
lng=0 4u
M13
Wd=2 5u
lng=0 4u
M14
Wd=2 5u
lng=0 4u
M21
Wd=5u
lng=0.4u
M22
Wd=2 5u
lng=0 4u
M19
Wd=5u
lng=0.4u
M15
Wd=5u
lng=0 4u
M20
Wd=2.5u
lng=0 4u
M17
Wd=2 5u
lng=0 4u
M2
Wd=20u
lng=0.4u
M1
Wd=10u
lng=0 4u
M10
Wd=5u
lng=0 4u
M27
Wd=5u
lng=0 4u
M8
Wd=2 5u
lng=0 4u
M25
Wd=2 5u
lng=0.4u
M5
Wd=5u
lng=0.4u
M9
Wd=5u
lng=0.4u
M6
Wd=2 5u
lng=0 4u
M7
Wd=2.5u
lng=0 4u

FIG. 160



Vdd
M2
Wd=5u
lng=0.4u
I0
I1
M10
Wd=5u
lng=0 4u
M8
Wd=5u
lng=0 4u
M6
Wd=20u
lng=0 4u
M1
Wd=5u
lng=0 4u
O
M4
Wd=2.5u
lng=0 4u
M3
Wd=2 5u
lng=0 4u
M9
Wd=2 5u
lng=0 4u
M7
Wd=2.5u
lng=0 4u
M5
Wd=5u
lng=0 4u
Vss

FIG 161

JC882 U.S. PTO
09/632856
08/04/00

Class	Subclass

ISSUE CLASSIFICATION

PATENT NUMBER

...ITY Patent Application

O.I.P.E.
SCANNED KW BK(3) Q.A.

PATENT DATE

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/632856	D	455		2682 2634	

APPLICANTS
David Sorrells
Michael Bultman
Robert Cook
Richard Looke

TITLE
Wireless local area network (WLAN) using universal frequency translation technology including multi-phase embodiments and circuit implementations

PTO-2040
12/99

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)						
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					
INTERNATIONAL CLASSIFICATION								
				☐ Continued on Issue Slip Inside File Jacket				

☐ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
☐ The term of this patent subsequent to ____________ (date) has been disclaimed.	(Assistant Examiner) (Date)			NOTICE OF ALLOWANCE MAILED	
☐ The term of this patent shall not extend beyond the expiration date of U.S Patent. No. ____________	(Primary Examiner) (Date)			ISSUE FEE	
				Amount Due	Date Paid
☐ The terminal ____months of this patent have been disclaimed.	(Legal Instruments Examiner) (Date)			ISSUE BATCH NUMBER	

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Class	Sub.	Date	Exmr.
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	349	3/11/04	[illegible]
455	131		
	150.1		
	189.1		
	190.1		
	313		
	323		
	326		

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	Date	Exmr.
"EAST"	3/11/04	[illegible]

INTERFERENCE SEARCHED			
Class	Sub.	Date	Exmr.

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ISSUE SLIP STAPLE AREA (for additional cross references)

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FEE DETERMINATION		65614	
O.I.P.E. CLASSIFIER		32	8/17
FORMALITY REVIEW	EVB	64293	09/26/00
RESPONSE FORMALITY REVIEW			

INDEX OF CLAIMS

✔	Rejected		N	Non-elected
=	Allowed		I	Interference
— (Through numeral)	Canceled		A	Appeal
÷	Restricted		O	Objected

Claim Final	Claim Original	Date	Date
	1		
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	4		
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	48		
	49		
	50	÷	

Claim Final	Claim Original	Date	Date
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Claim Final	Claim Original	Date
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If more than 150 claims or 10 actions staple additional sheet here

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APPLICATION
09/632

APPLICANTS David Michae Robert Richar

TITLE Wirele transl implem

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TERMI DISCL

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STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
ATTORNEYS AT LAW
1100 NEW YORK AVENUE, N.W., SUITE 600
WASHINGTON, D.C. 20005-3934

www.skgf.com
PHONE: (202) 371-2600 FACSIMILE: (202) 371-2540

August 4, 2000

WRITER'S DIRECT NUMBER:
(202) 371-2677
INTERNET ADDRESS:
RSOKOHL@SKGF.COM

Commissioner for Patents
Washington, D.C. 20231

Box Patent Application

Re: U.S. Non-Provisional Utility Patent Application under 37 C.F.R. § 1.53(b)
Appl. No. To be assigned; Filed: August 4, 2000
For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations**
Inventors: David F. Sorrells, Michael J. Bultman, Robert W. Cook, Richard C. Looke, Charley D. Moses, Jr., Gregory S. Rawlins, and Michael W. Rawlins
Our Ref: 1744.0630003

Sir:

The following documents are forwarded herewith for appropriate action by the U.S. Patent and Trademark Office:

1. USPTO Utility Patent Application Transmittal Form PTO/SB/05;

2. U.S. Utility Patent Application entitled:

   Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations

   and naming as inventors:

   David F. Sorrells, Michael J. Bultman, Robert W. Cook, Richard C. Looke, Charley D. Moses, Jr., Gregory S. Rawlins, and Michael W. Rawlins

the application comprising:

a. specification containing:

i. 98 pages of description prior to the claims;

ii. 7 pages of claims (40 claims);

iii. a one (1) page abstract;

b. Two-hundred and eight (208) sheets of drawings: (Figures 1A-D, 2A, 2B, 3-14, 15A-F, 16-19, 20A, 20A-1, 20B-F, 21, 22A-F, 23A, 24A-J, 25-45, 46A, 46B, 47, 48, 49A, 49B,50, 51, 52A-C, 53-55, 56A, 56B, 57-60, 61A, 61B, 62-66, 67A, 67B, 68A, 68B, 69A, 69B, 70A-S, 71A-D, 72A-J, 73A, 73B, 74, 75A-C, 76A, 76B, 77, 78, 79A-D, 80, 81A-C, 82-88, 89A-E, 90A-D, 91-94, 95A-C, 96-161);

3. 37 C.F.R. § 1.136(a)(3) Authorization to Treat a Reply As Incorporating An Extension of Time (in duplicate); and

4. Two (2) return postcards.

It is respectfully requested that, of the two attached postcards, one be stamped with the filing date of these documents and returned to our courier, and the other, prepaid postcard, be stamped with the filing date and unofficial application number and returned as soon as possible.

This patent application is being submitted under 37 C.F.R. § 1.53(b) without Declaration and without filing fee.

Commissioner for Patents
August 4, 2000
Page 3

This application claims priority to U.S. Provisional Application No. 60/147,129, filed August 4, 1999; U.S. Application No. 09/525,615, filed on March 14, 2000; and U.S. Application No. 09/526,041, filed on March 14, 2000.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Robert Sokohl
Attorney for Applicants
Registration No. 36,013

0630003.pto

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

JC882 U.S. PTO
09/632856
08/04/00

In re application of:	
Sorrells *et al.*	Art Unit: To be assigned
Appl. No. To be assigned	Examiner: To be assigned
Filed: August 4, 2000	Atty. Docket: 1744.0630003
For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations**	

Authorization To Treat A Reply As Incorporating An Extension Of Time Under 37 C.F.R. § 1.136(a)(3)

Commissioner for Patents
Washington, D.C. 20231

Sir:

The U.S. Patent and Trademark Office is hereby authorized to treat any concurrent or future reply that requires a petition for an extension of time under this paragraph for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. The U.S. Patent and Trademark Office is hereby authorized to charge all required extension of time fees to our Deposit Account No. 19-0036, if such fees are not otherwise provided for in such reply. A duplicate copy of this authorization is enclosed.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Robert Sokohl
Attorney for Applicants
Registration No. 36,013

Date: 8/4/00

1100 New York Avenue, N.W.
Suite 600
Washington, D.C. 20005-3934
(202) 371-2600
0630003.aut

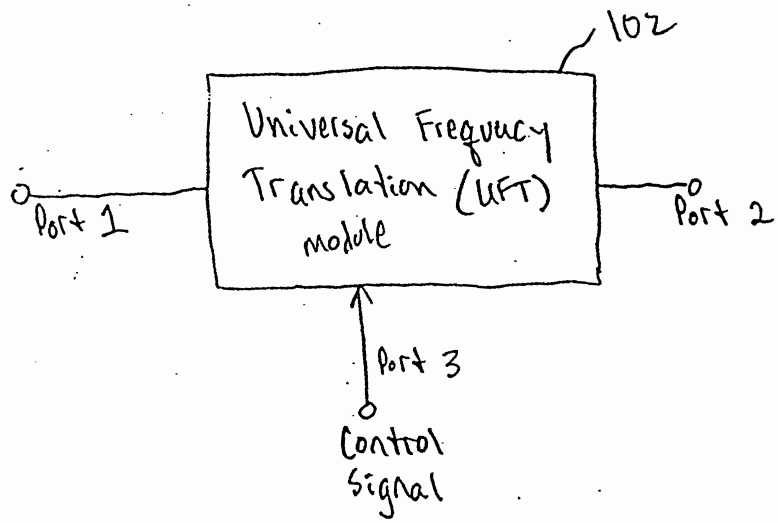
102
Universal Frequucy Translation (UFT) module
Port 1
Port 2
Port 3
Control Signal

FIG. 1A

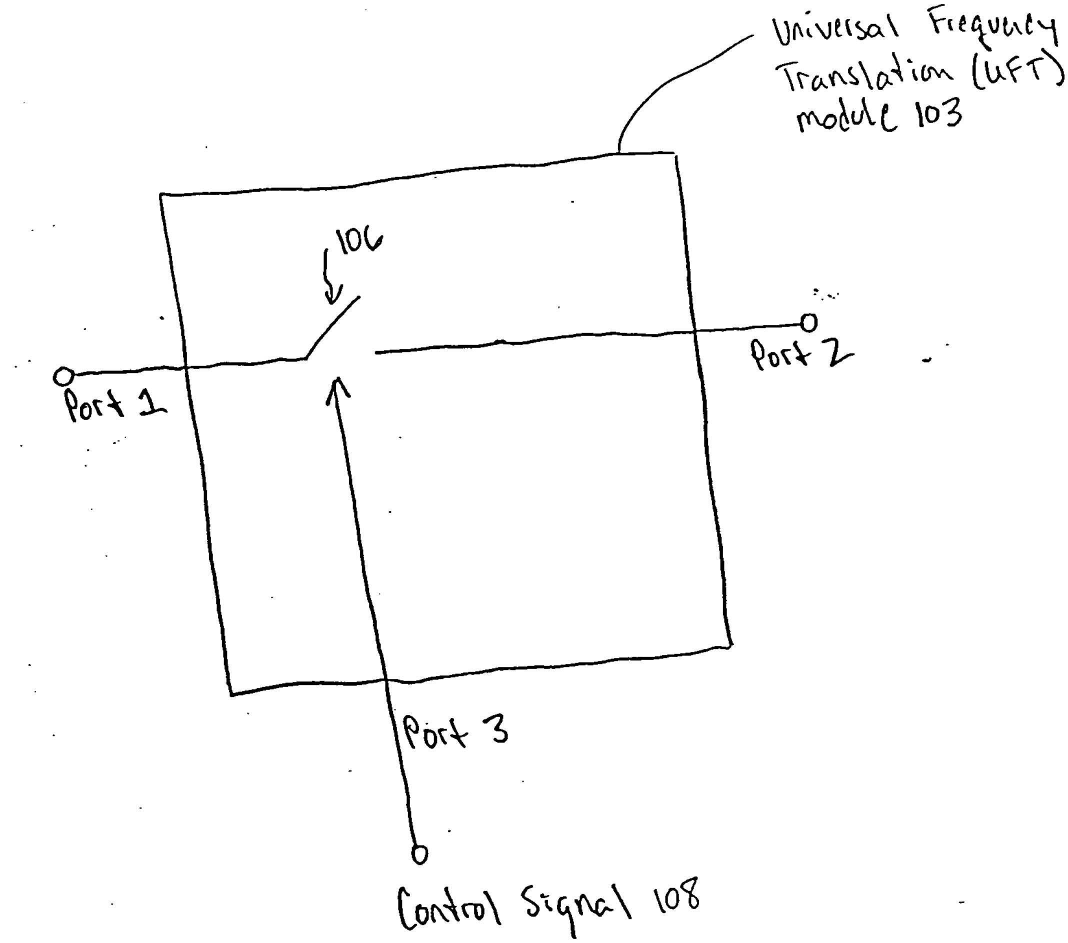

FIG. 1B

09632856.080400

M

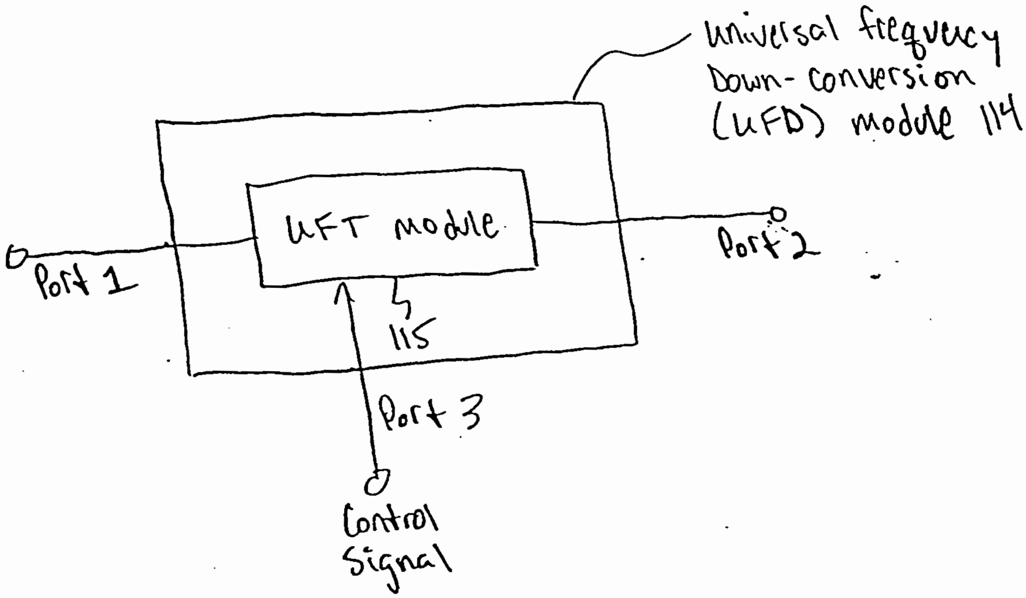
universal frequency
Down-conversion
(UFD) module 114
UFT module
Port 1
Port 2
115
Port 3
Control
Signal

FIG. 1C

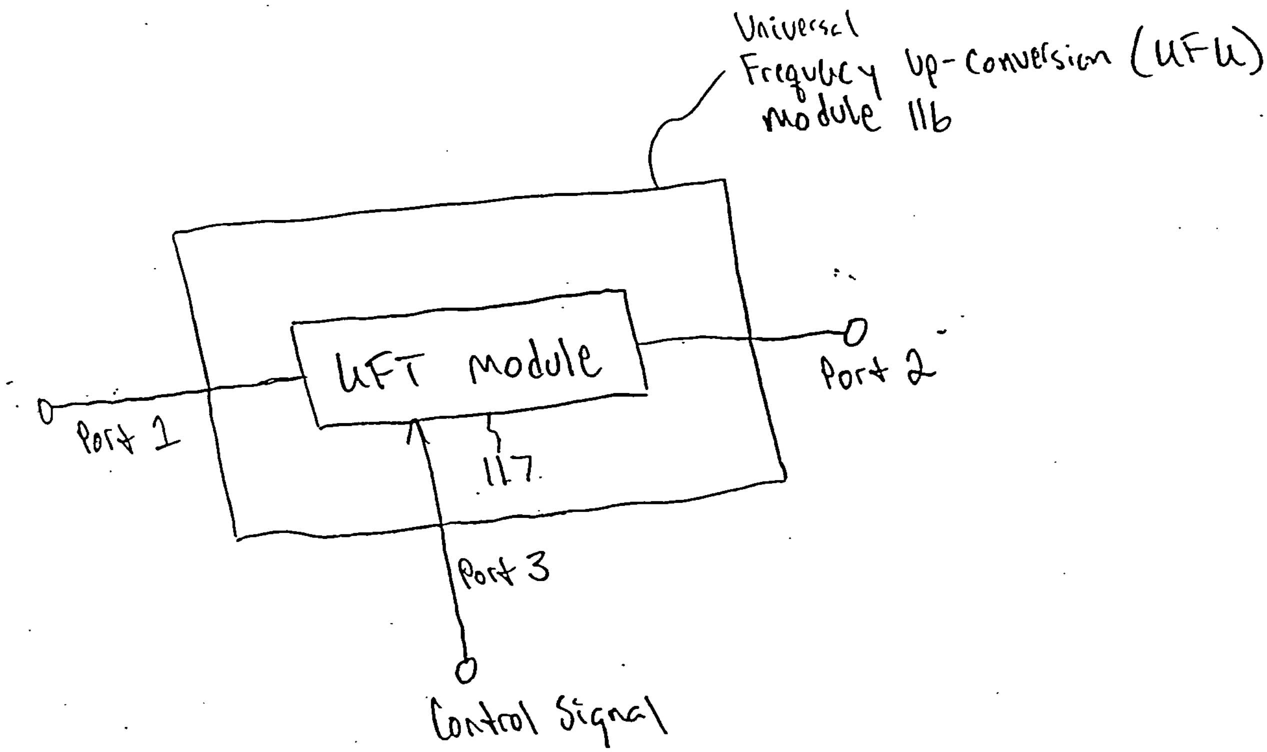
Universal
Frequency Up-Conversion (UFU)
module 116
UFT module
Port 1
Port 2
117
Port 3
Control Signal

FIG. 1D

nn

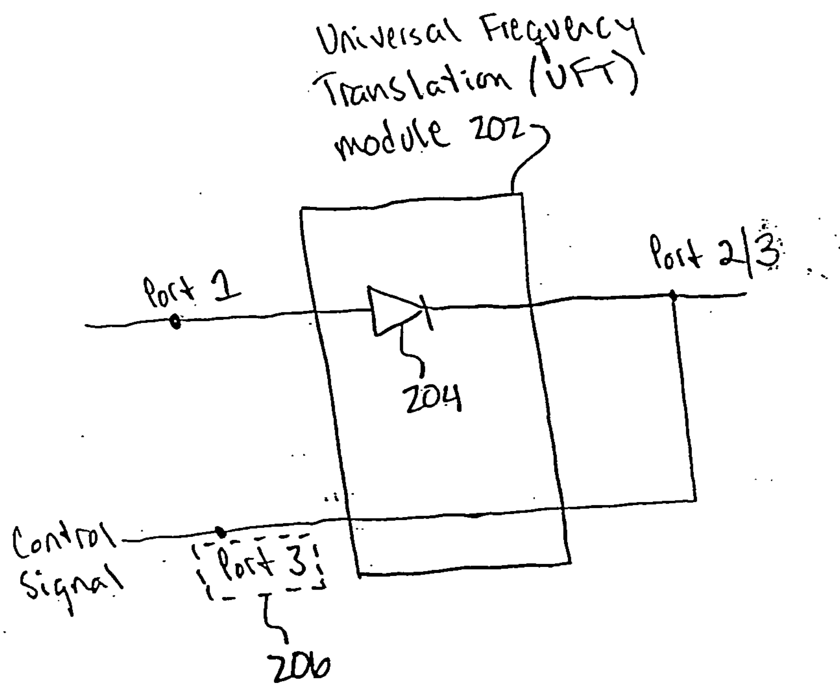
Universal Frequency Translation (UFT) module 202
Port 1
204
Port 2/3
Control Signal
Port 3
206

FIG. 2A

09532856.080400

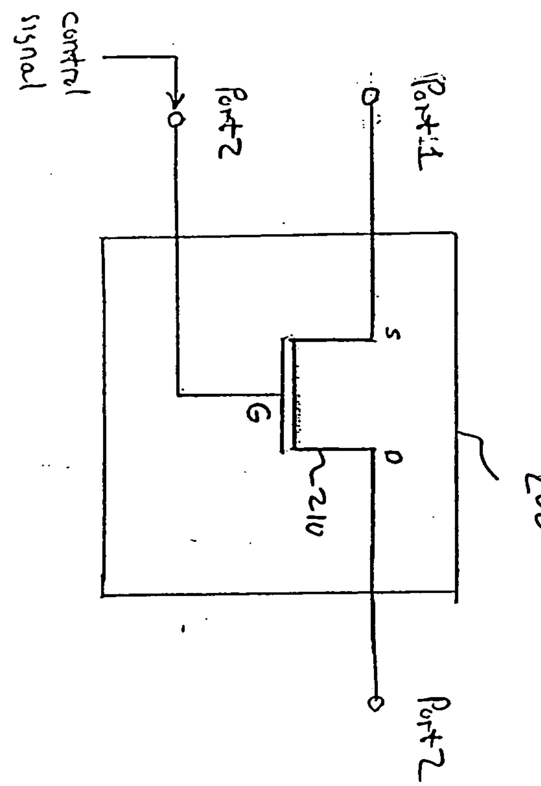

FIG. 2B

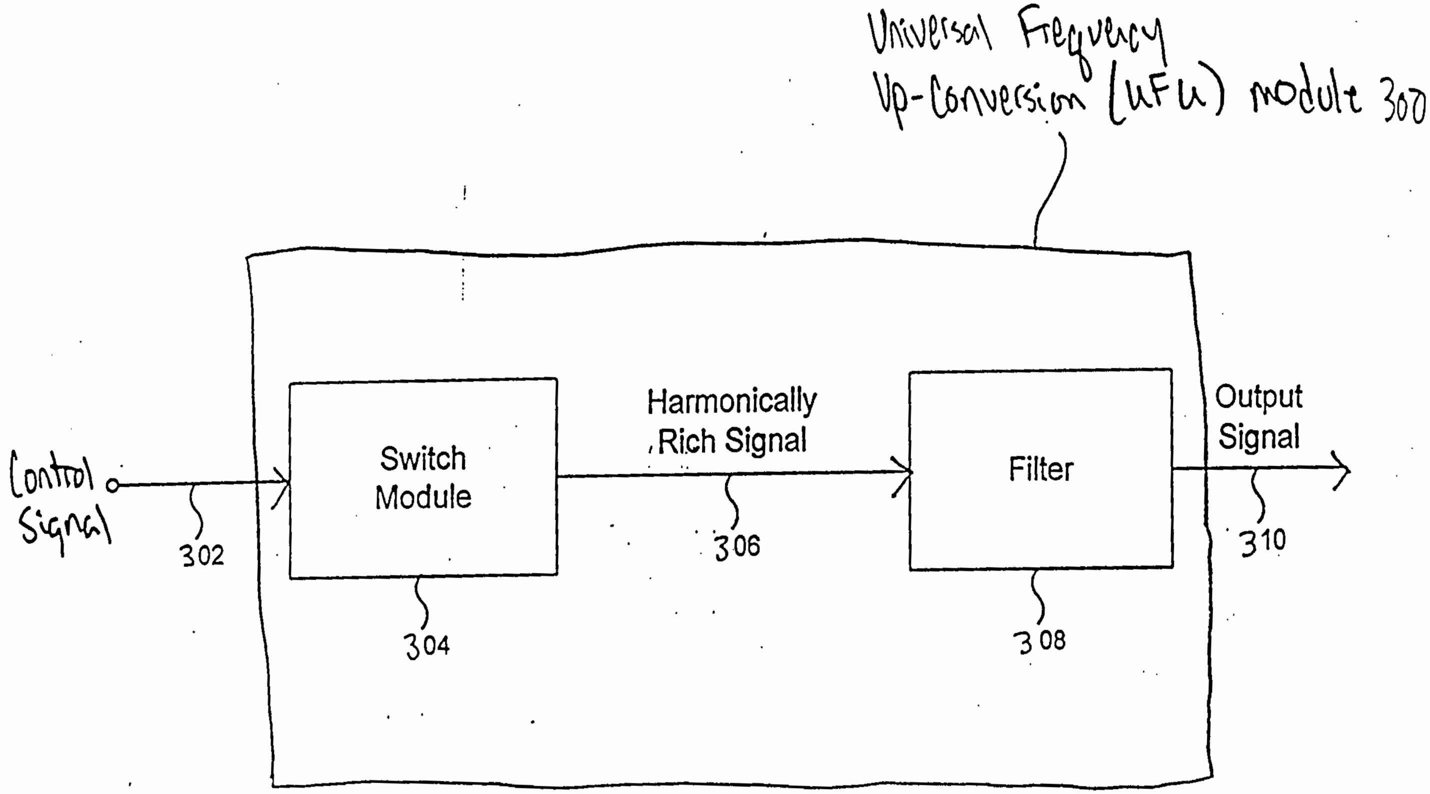
Universal Frequency
Up-Conversion (UFU) module 300
Control
Signal
302
Switch
Module
304
Harmonically
Rich Signal
306
Filter
308
Output
Signal
310

FIG. 3

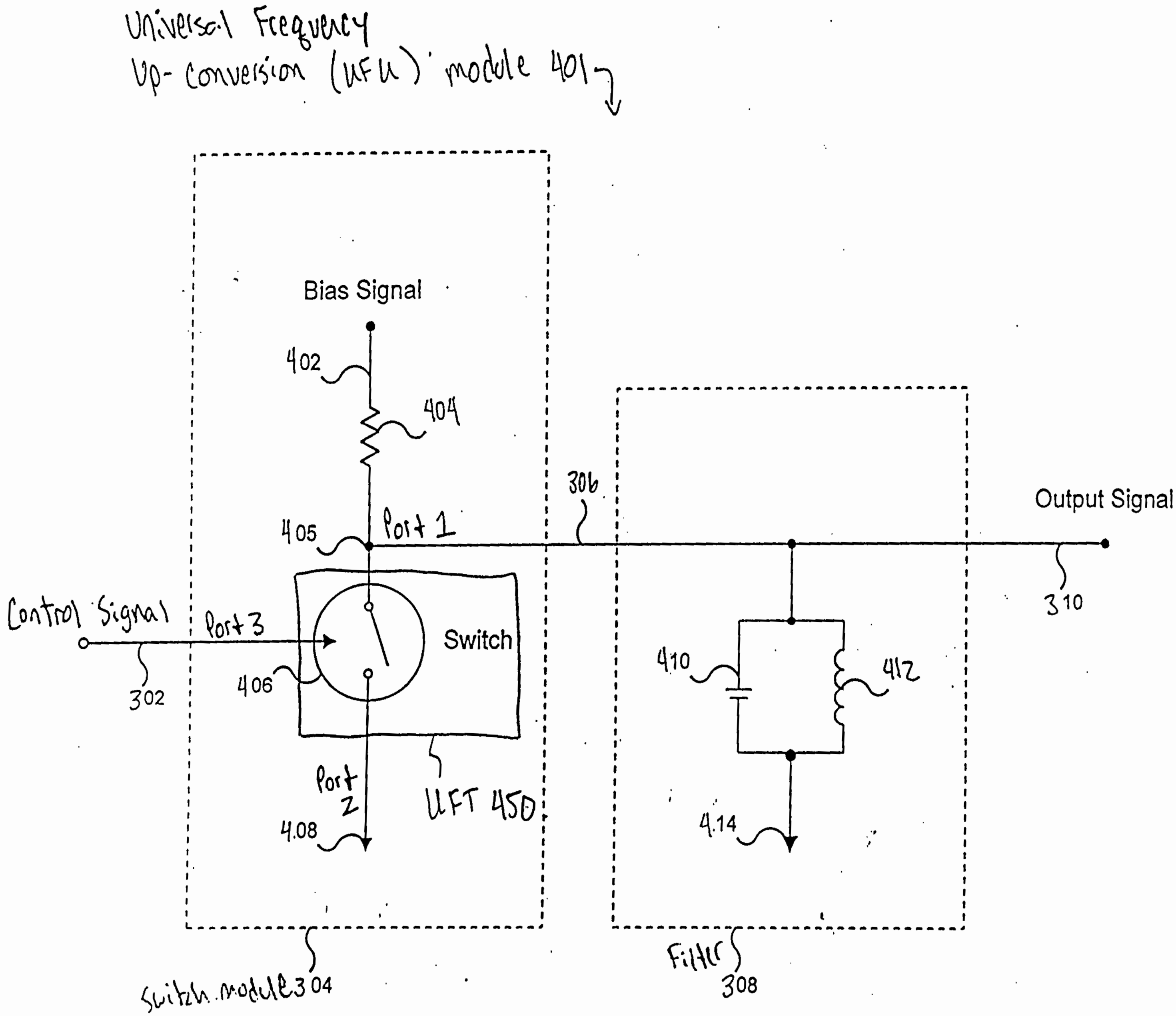
Universal Frequency Up-Conversion (UFU) module 401
Bias Signal
402
404
405
Port 1
306
Output Signal
310
Control Signal
Port 3
302
406
Switch
UFT 450
Port 2
408
410
412
414
Switch module 304
Filter 308

FIG. 4

3

Universal Frequency Up-conversion (UFU) module 590

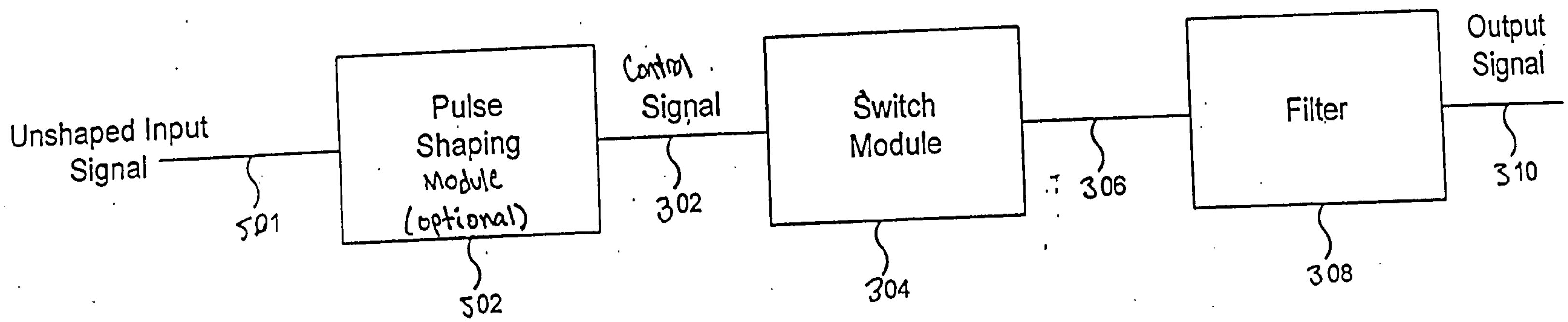

FIG. 5

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9808-02.vsd/48

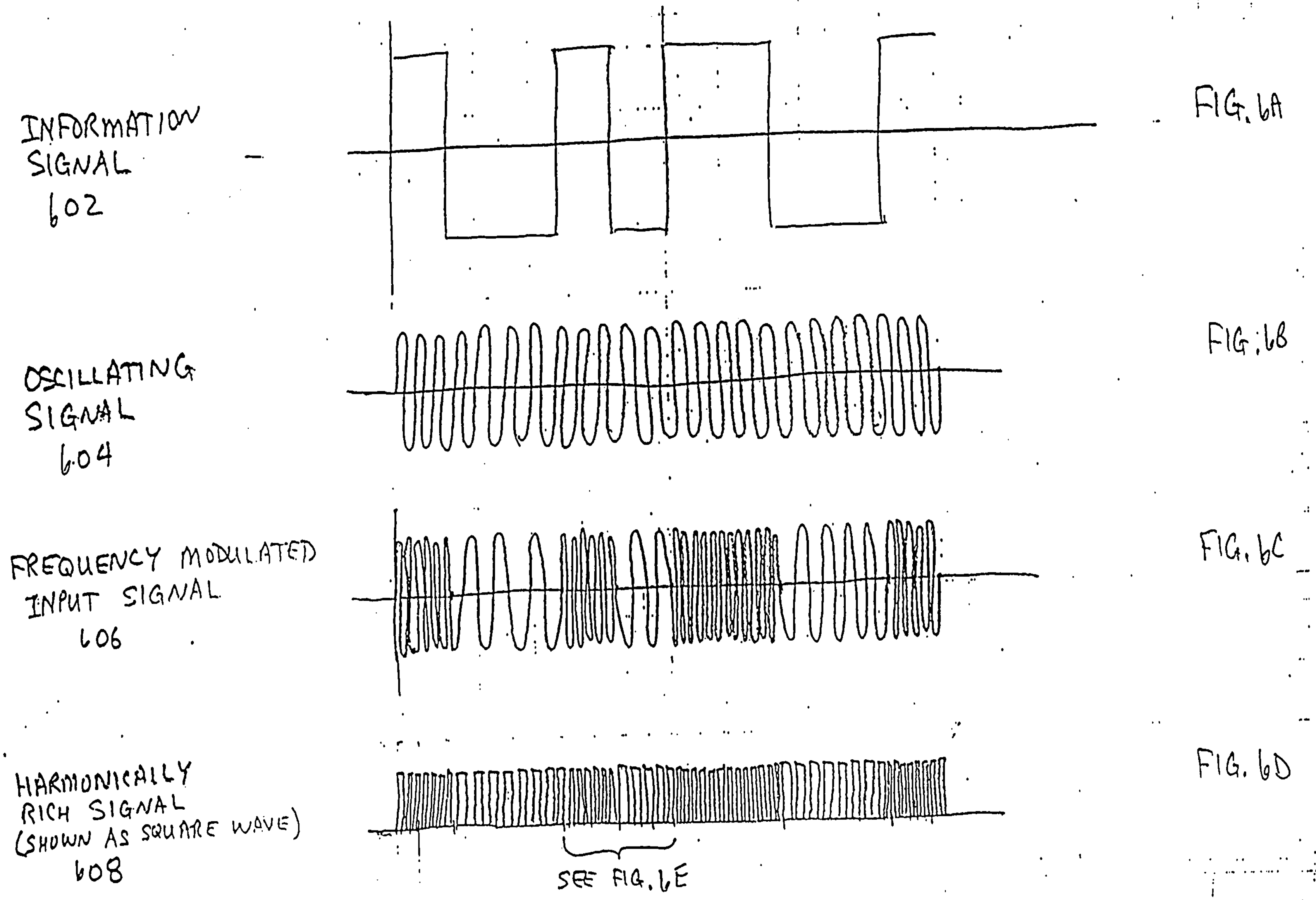
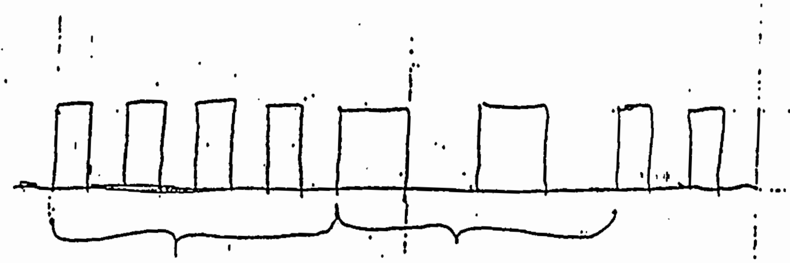

INFORMATION SIGNAL 602
OSCILLATING SIGNAL 604
FREQUENCY MODULATED INPUT SIGNAL 606
HARMONICALLY RICH SIGNAL (SHOWN AS SQUARE WAVE) 608
SEE FIG. 6E
FIG. 6A
FIG. 6B
FIG. 6C
FIG. 6D

FIG. 6

3

EXPANDED VIEW OF HARMONICALLY RICH SIGNAL 608

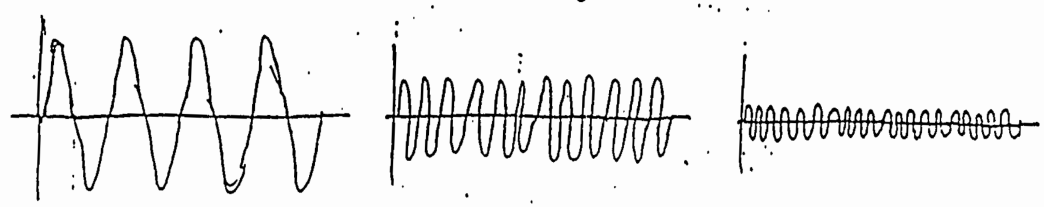


610 SEE FIG. 6F

612 SEE FIG. 6G

FIG 6E

HARMONICS OF SIGNAL 610 (SHOWN SEPARATELY)



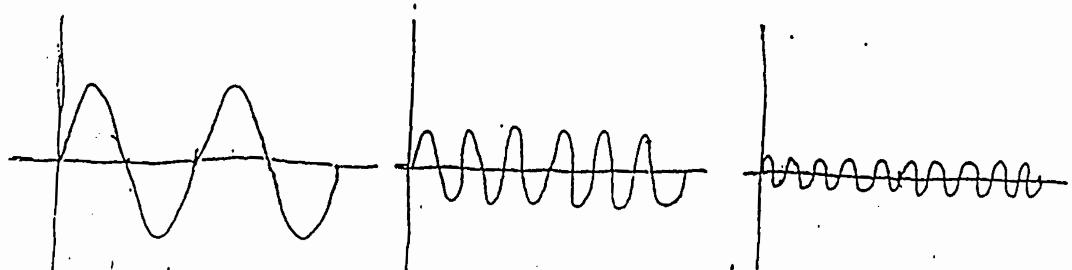
FUNDAMENTAL FREQUENCY 610A

THIRD HARMONIC 610B

FIFTH HARMONIC 610C

FIG. 6F

HARMONICS OF SIGNAL 612 (SHOWN SEPARATELY)



FUNDAMENTAL FREQUENCY 612A

THIRD HARMONIC 612B

FIFTH HARMONIC 612C

FIG. 6G

FIG. 6 (cont.)

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3

HARMONICS OF SIGNALS 610 AND 612. (SHOWN SIMULTANEOUSLY BUT NOT SUMMED)

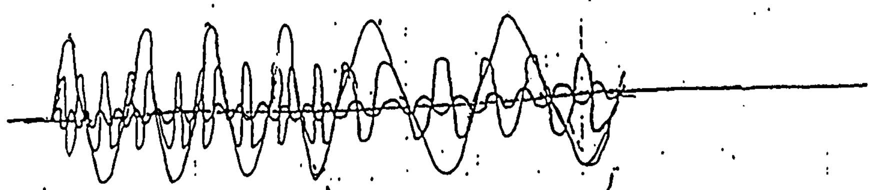

FIG 6H

FILTERED OUTPUT SIGNAL 614

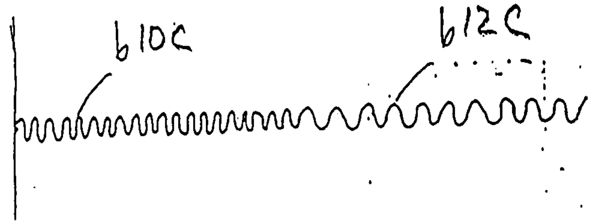

FIG. 6I

FIG 6 (cont)

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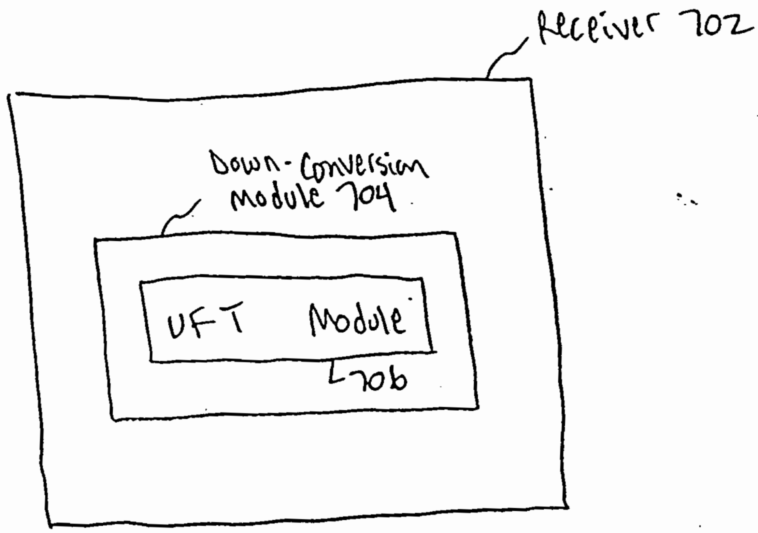

FIG. 7

m

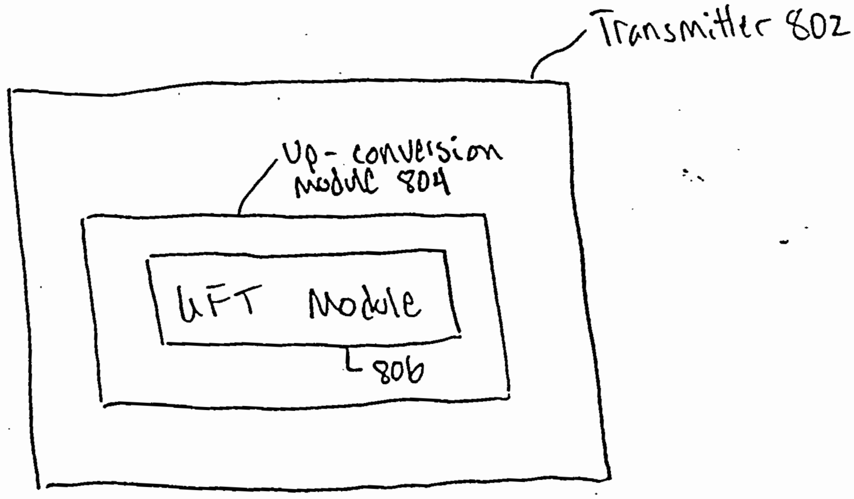

FIG. 8

M

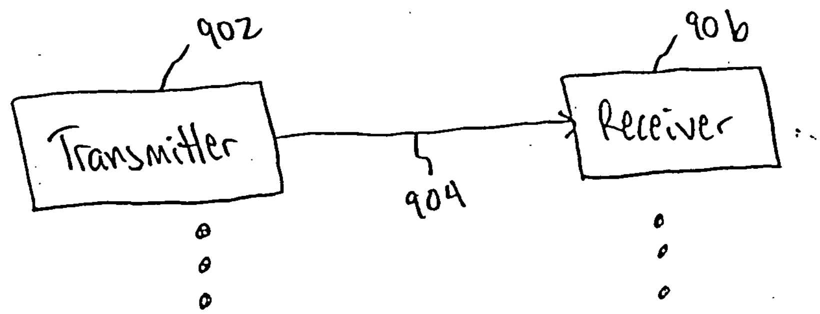

FIG. 9

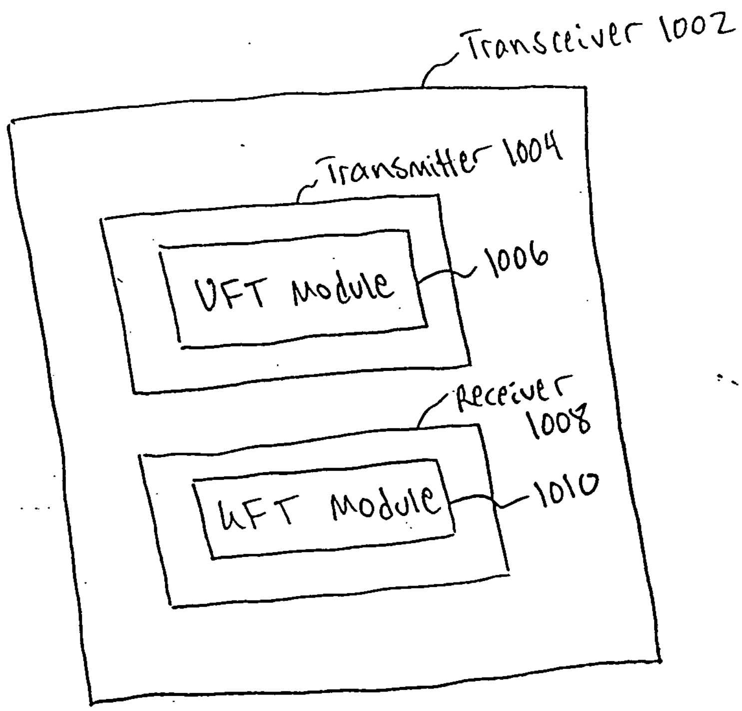

FIG. 10

09325561.080400

M

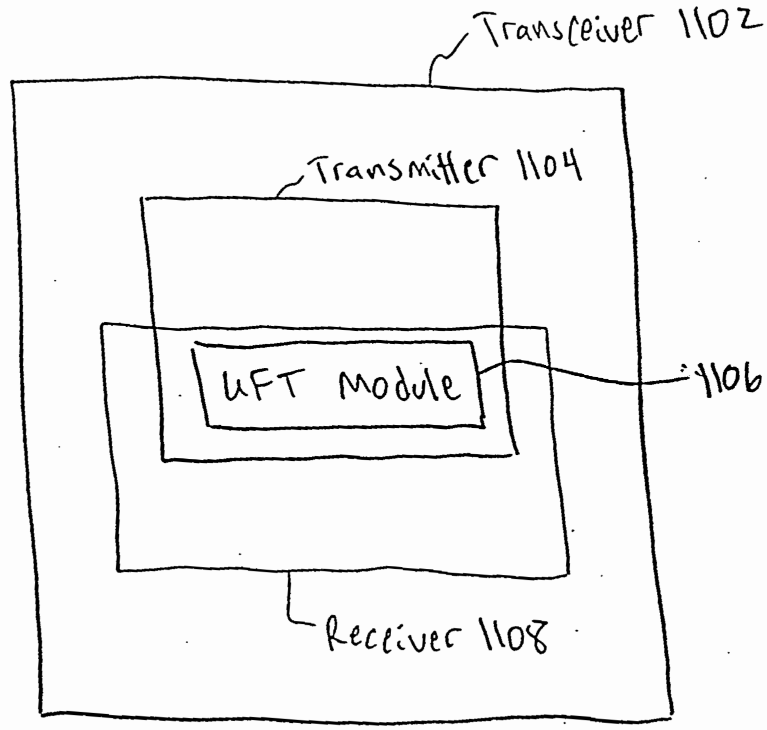
Transceiver 1102
Transmitter 1104
UFT Module
1106
Receiver 1108

FIG. 11

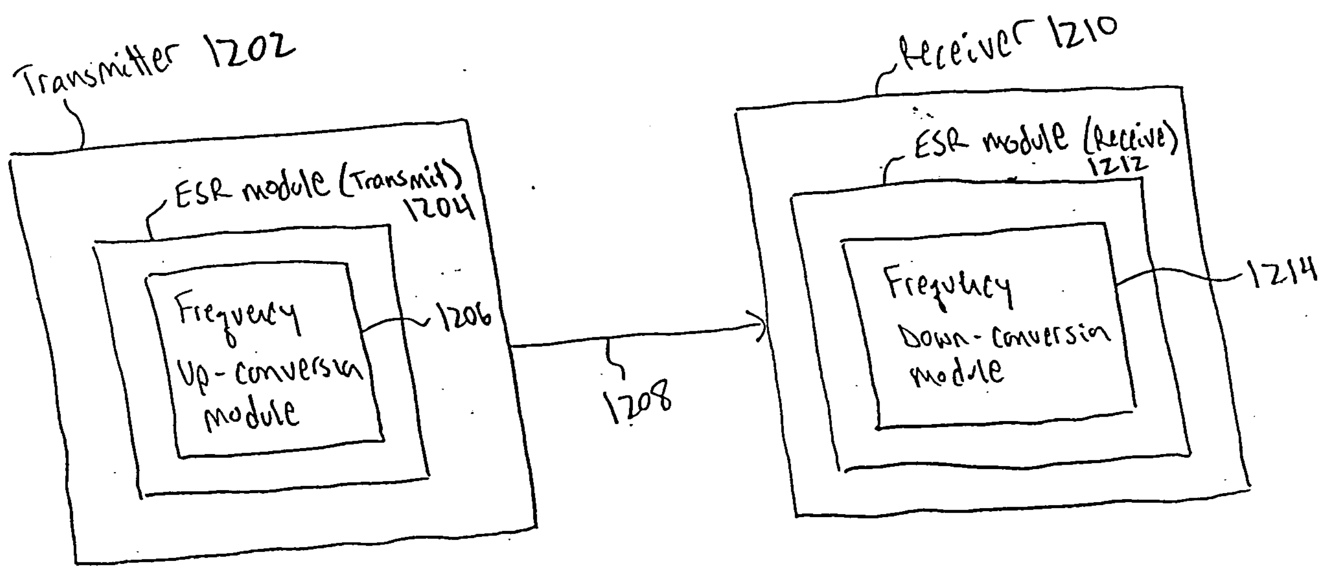
Transmitter 1202
ESR module (Transmit) 1204
Frequency Up-conversion module
1206
1208
Receiver 1210
ESR module (Receive) 1212
Frequency Down-conversion module
1214

FIG. 12

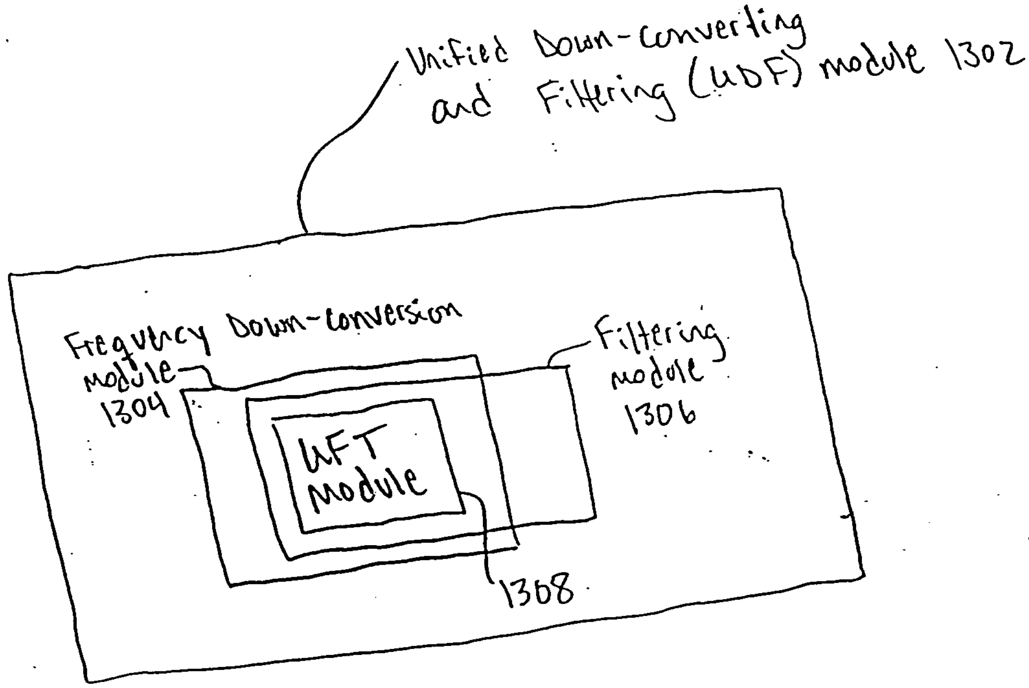
Unified Down-converting and Filtering (UDF) module 1302
Frequency Down-conversion module 1304
Filtering module 1306
UFT Module
1308

FIG. 13

m

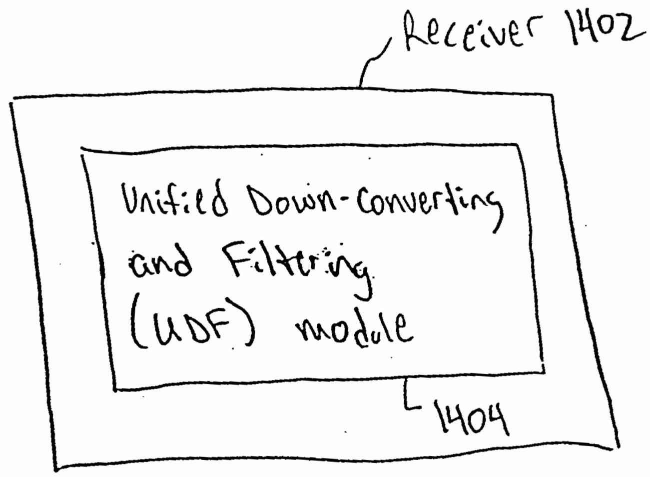
Receiver 1402
Unified Down-Converting and Filtering (UDF) module
1404

FIG. 14

M

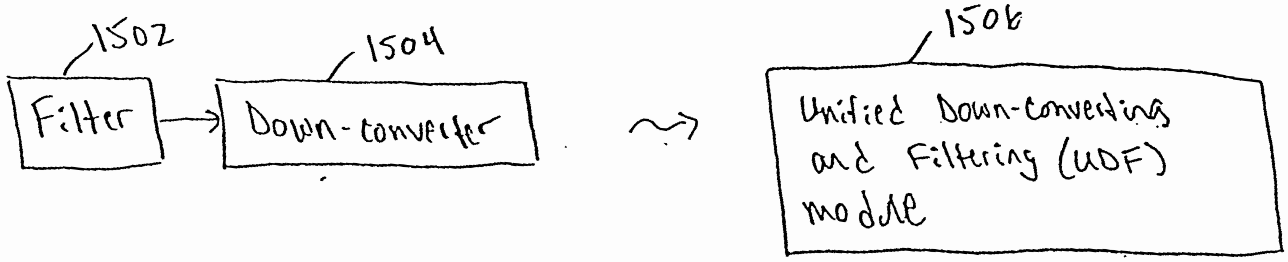

FIG. 15A

FIG. 15B

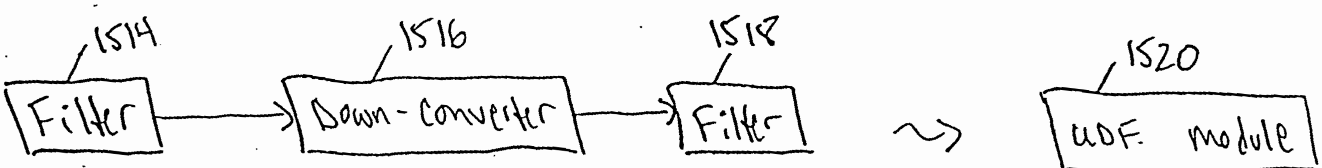

FIG. 15C

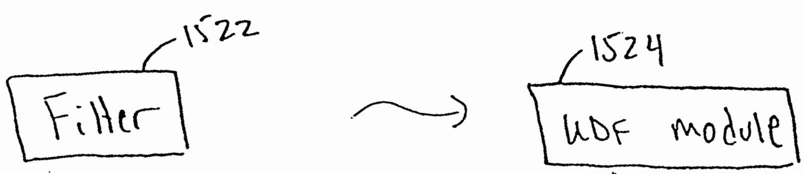

FIG. 15D

FIG. 15E

FIG. 15F

m

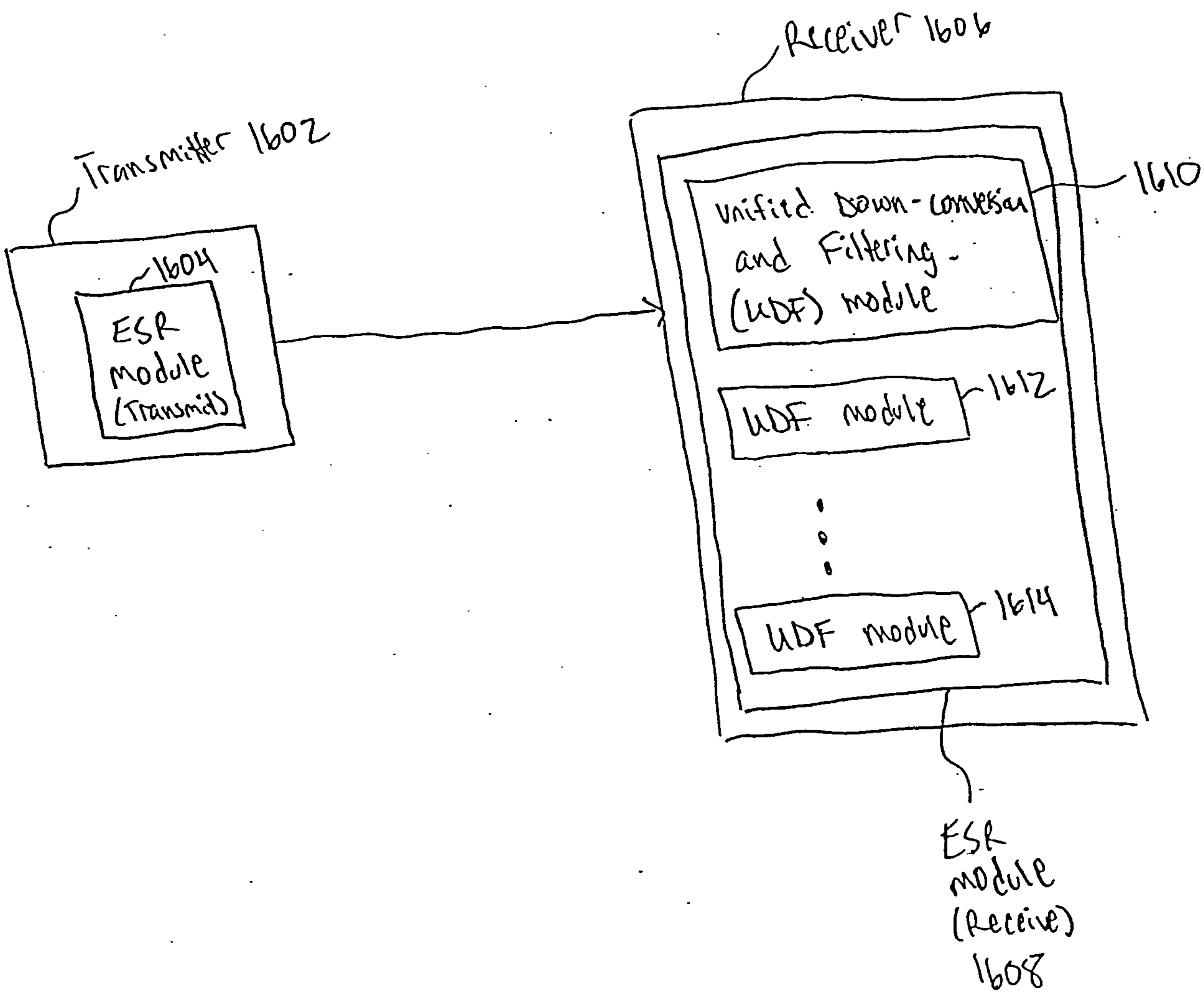
Transmitter 1602
1604
ESR module (Transmit)
Receiver 1606
Unified Down-conversion and Filtering (UDF) module
1610
UDF module
1612
UDF module
1614
ESR module (Receive) 1608

FIG. 16

M

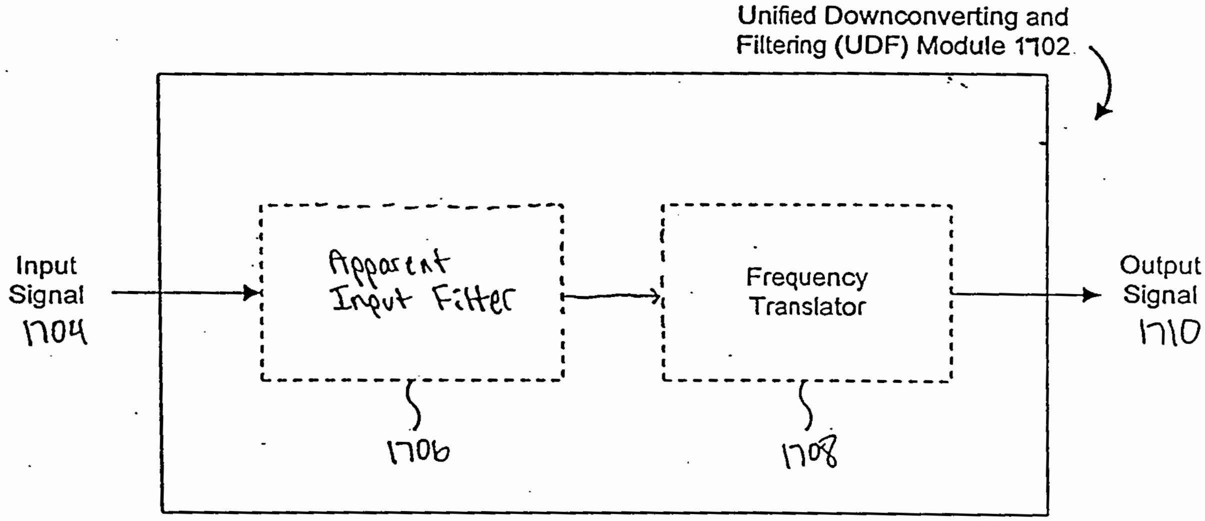

FIG. 17

9809-02.vsd/1

m

1802

Node \ Time	t-1 (rising edge of ϕ_1)	t-1 (rising edge of ϕ_2)	t (rising edge of ϕ_1)	t (rising edge of ϕ_2)	t+1 (rising edge of ϕ_1)
1902	VI_{t-1} 1804	VI_{t-1} 1808	VI_t 1816	VI_t 1826	VI_{t+1} 1838
1904	—	VI_{t-1} 1810	VI_{t-1} 1818	VI_t 1828	VI_t 1840
1906	VO_{t-1} 1806	VO_{t-1} 1812	VO_t 1820	VO_t 1830	VO_{t+1} 1842
1908	—	VO_{t-1} 1814	VO_{t-1} 1822	VO_t 1832	VO_t 1844
1910	— 1807	—	VO_{t-1} 1824	VO_{t-1} 1834	VO_t 1846
1912	—	— 1815	—	VO_{t-1} 1836	VO_{t-1} 1848
1918	—	—	—	—	VI_t - $0.1 * VO_t$ - $0.8 * VO_{t-1}$ 1850

FIG. 18

9809-02.vsc

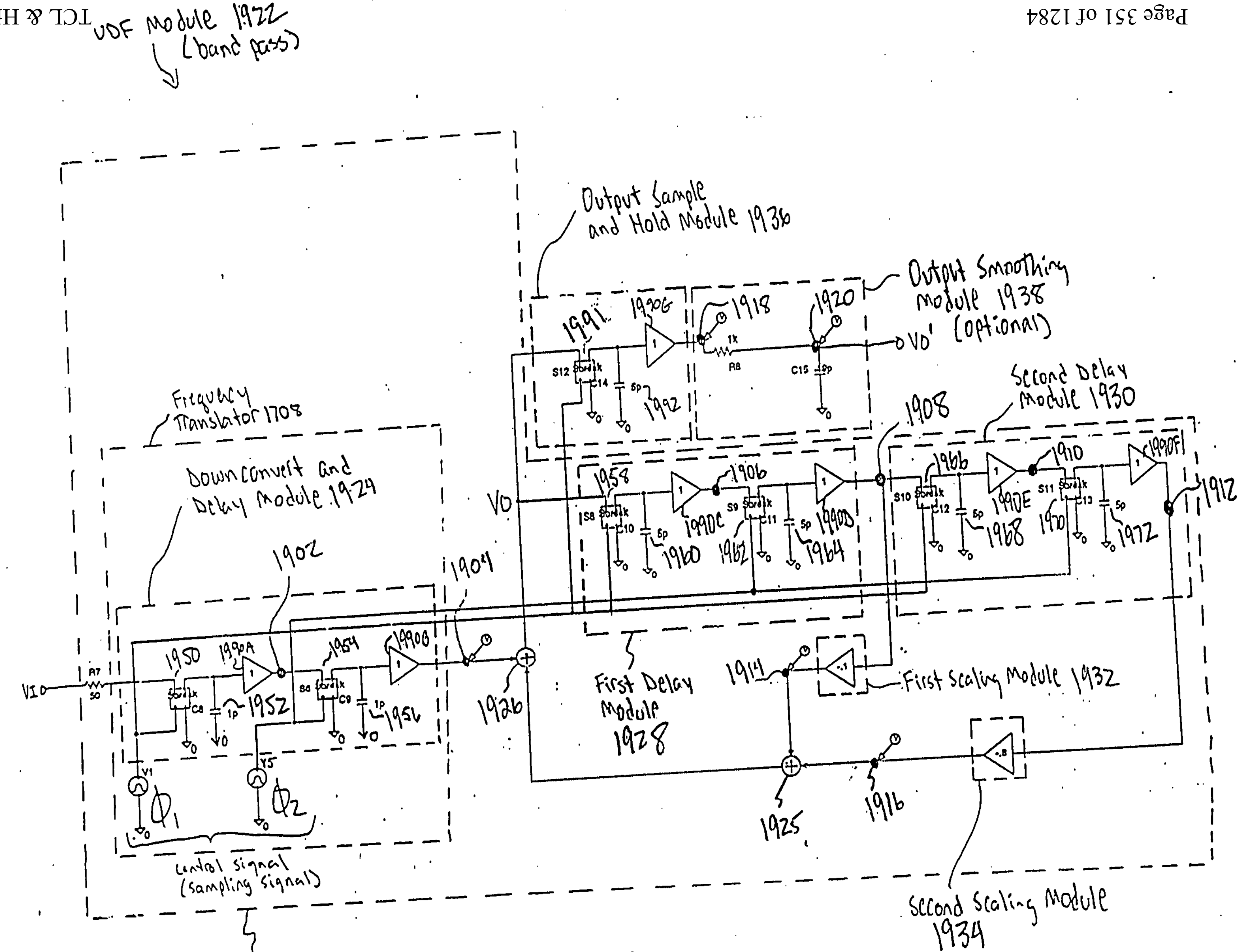

FIG. 19

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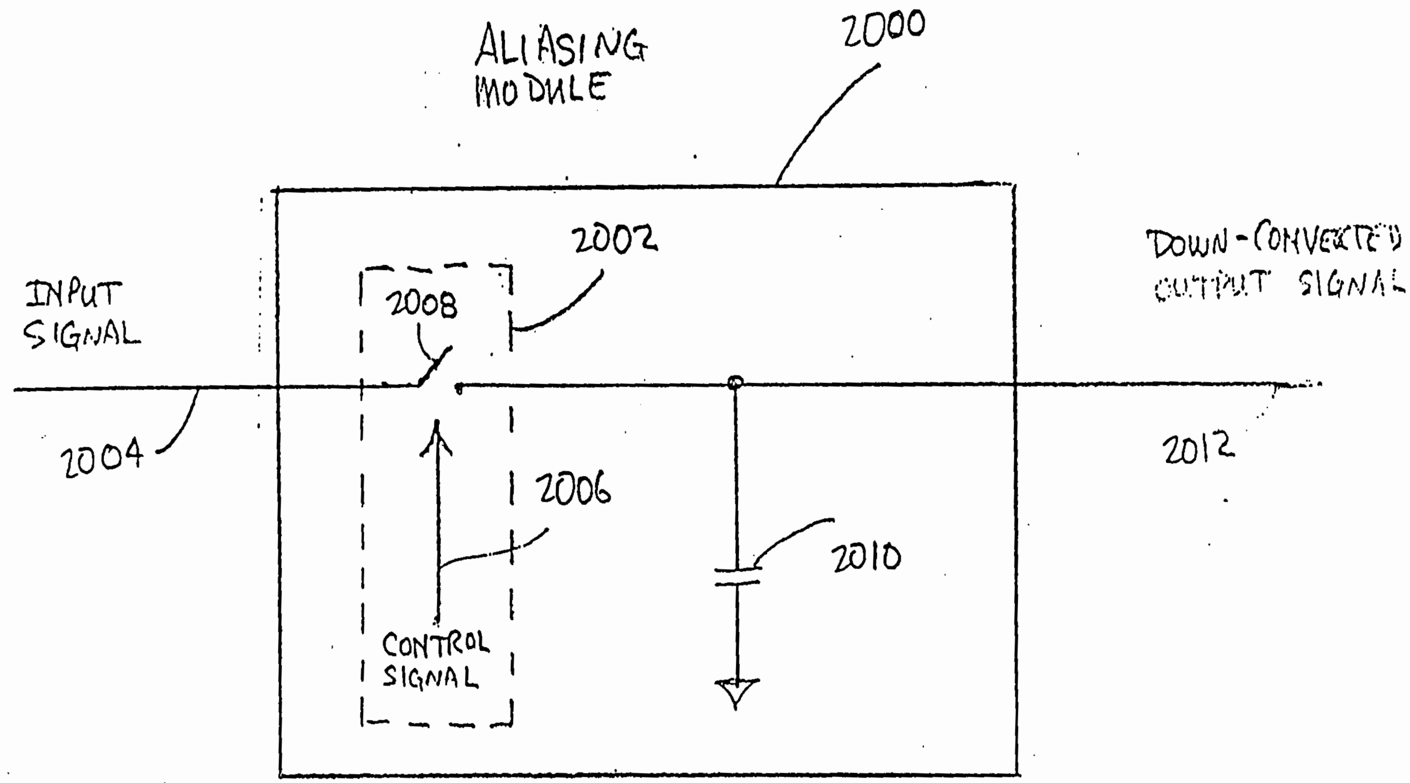


FIG. 20A

09632856 .080400

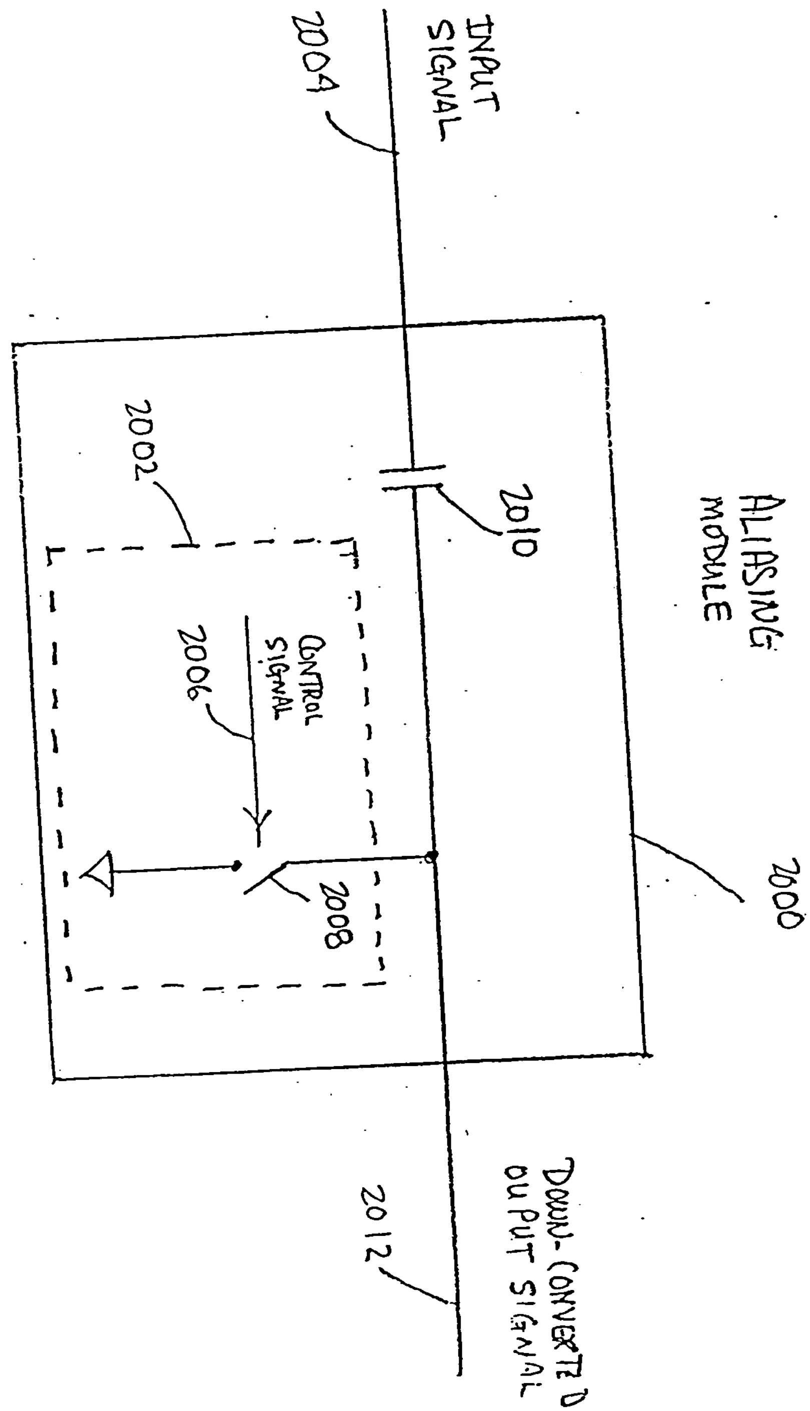

INPUT SIGNAL
2004
ALIASING MODULE
2010
2002
CONTROL SIGNAL
2006
2008
2000
2012
DOWN-CONVERTED OUPUT SIGNAL

FIG. 20A-1

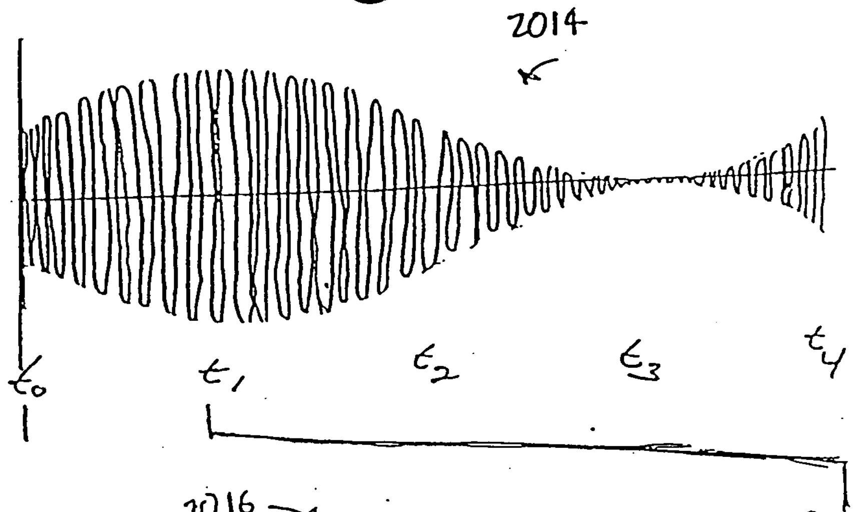


FIG. 20B

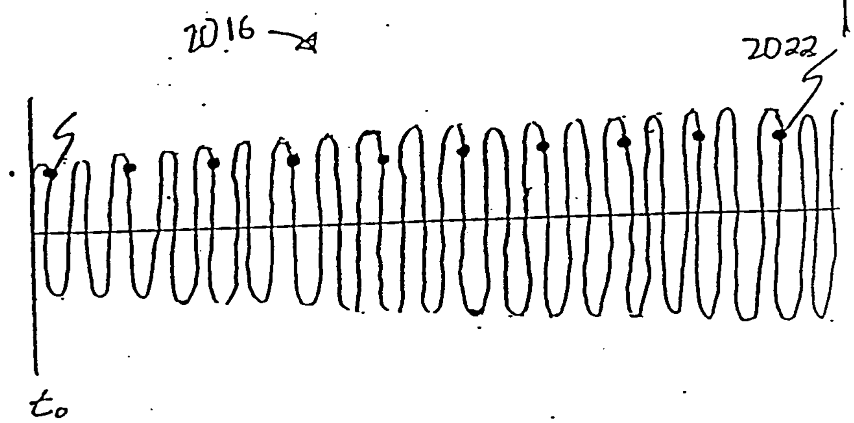


FIG. 20C

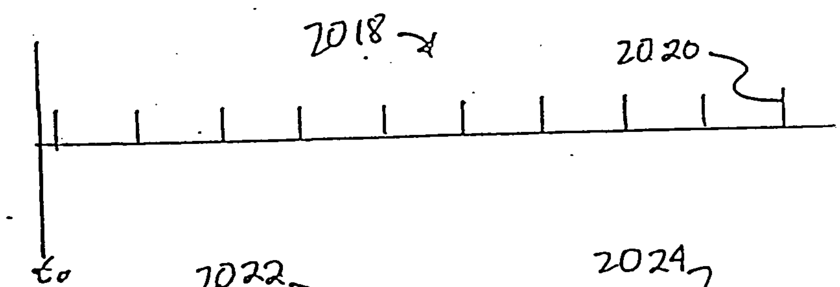


FIG. 20D

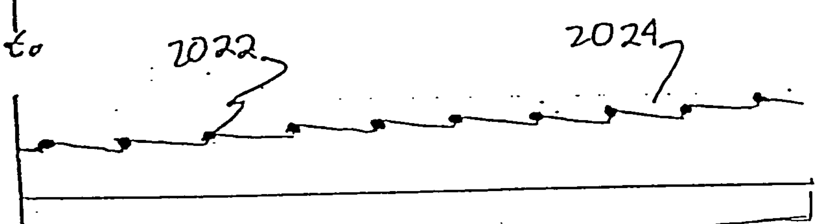


FIG. 20E

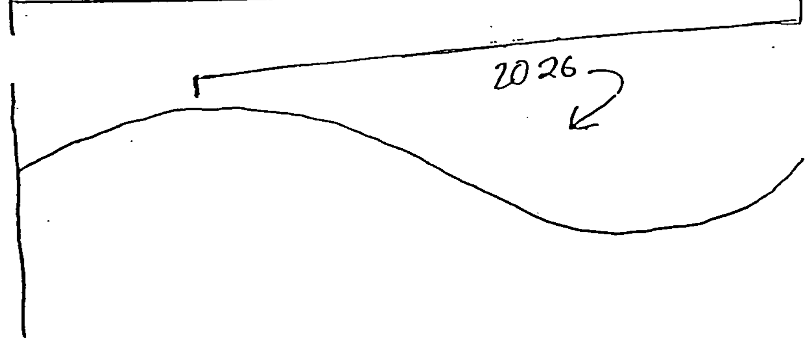


FIG. 20F

M

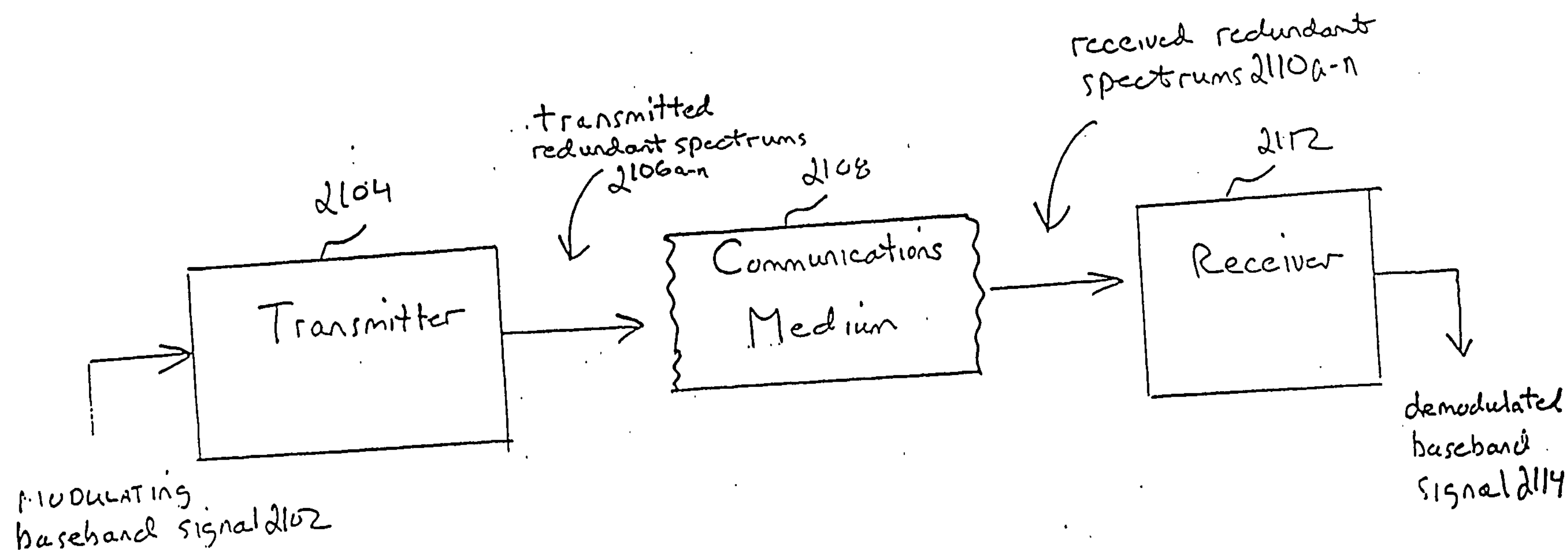


FIG. 21

09632856 .080400

FIG. 22A

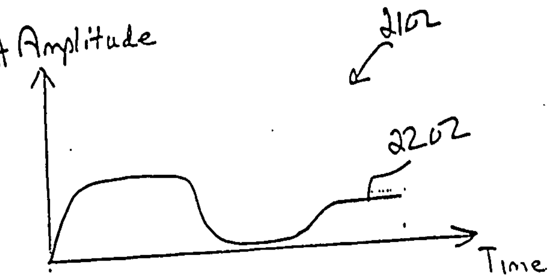


FIG. 22B

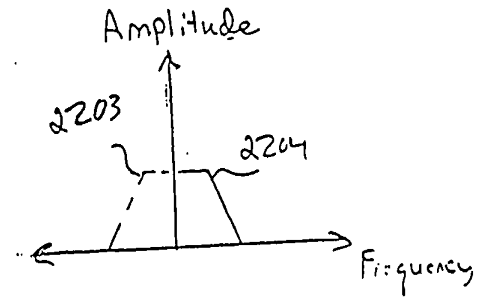


FIG. 22C

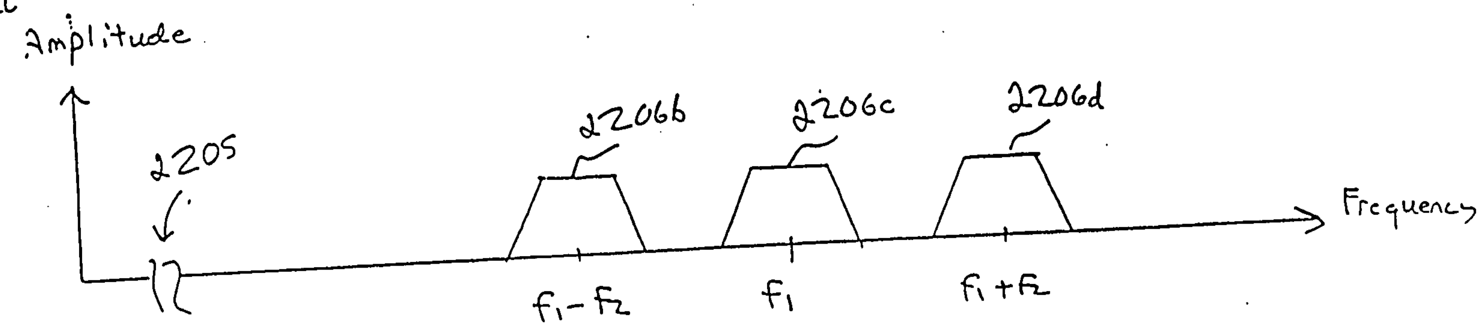
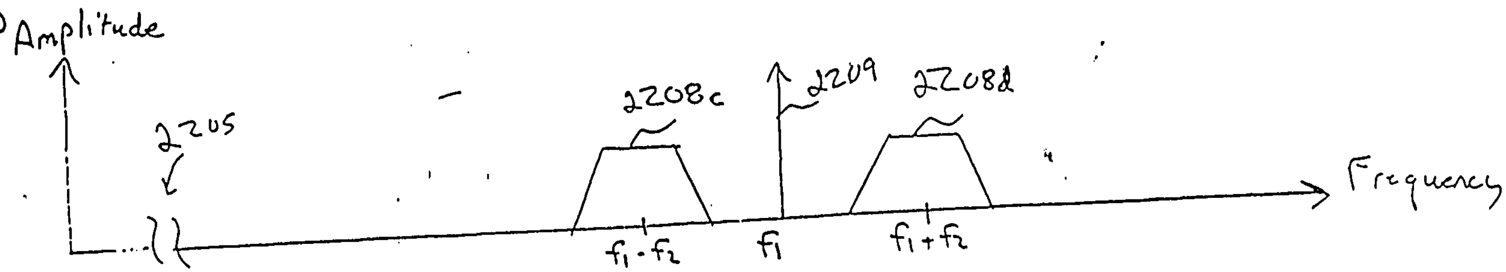


FIG. 22D



09632856 .080400

Fig. 22E

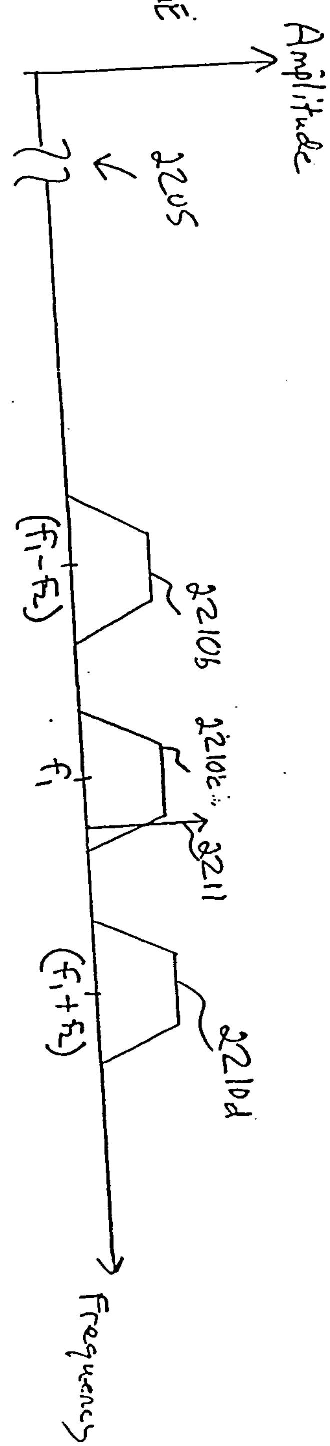


Fig. 22F

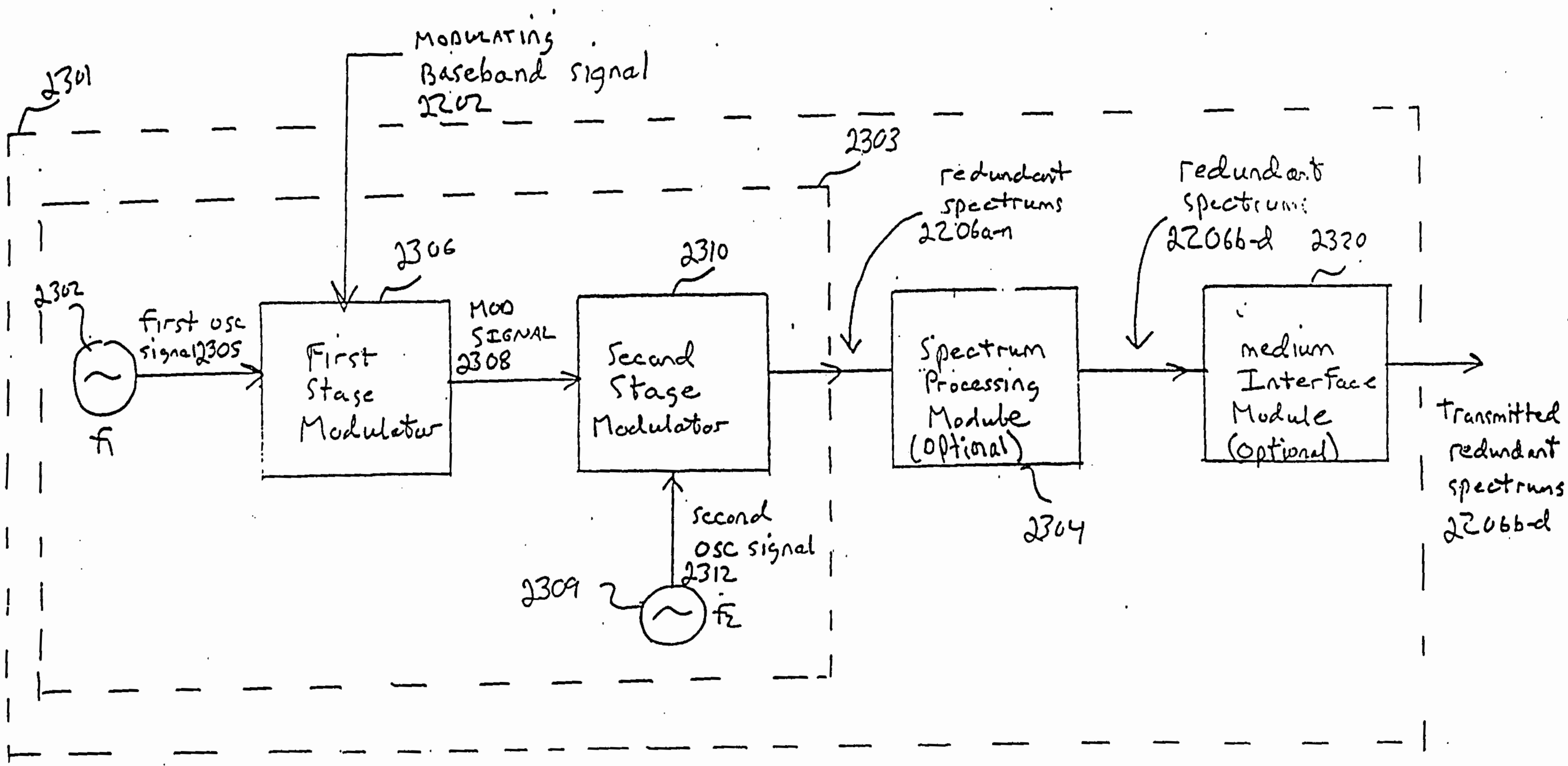


FIG. 23A

09632856 .080400

FIG. 23B

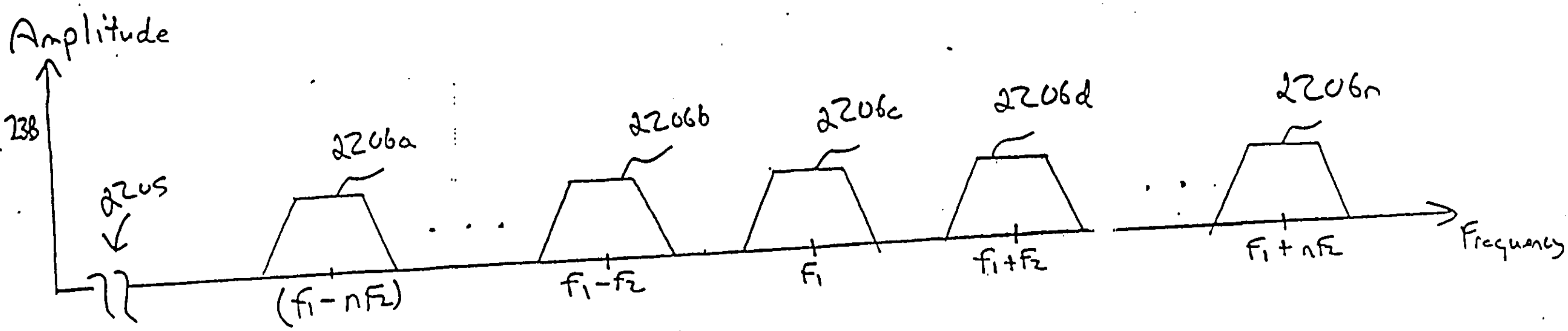
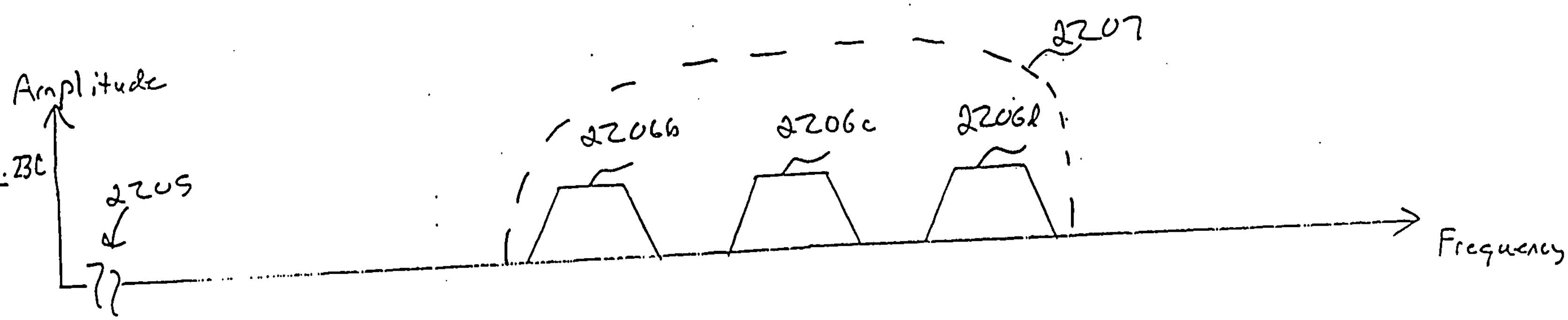


FIG. 23C



09632856 .080400

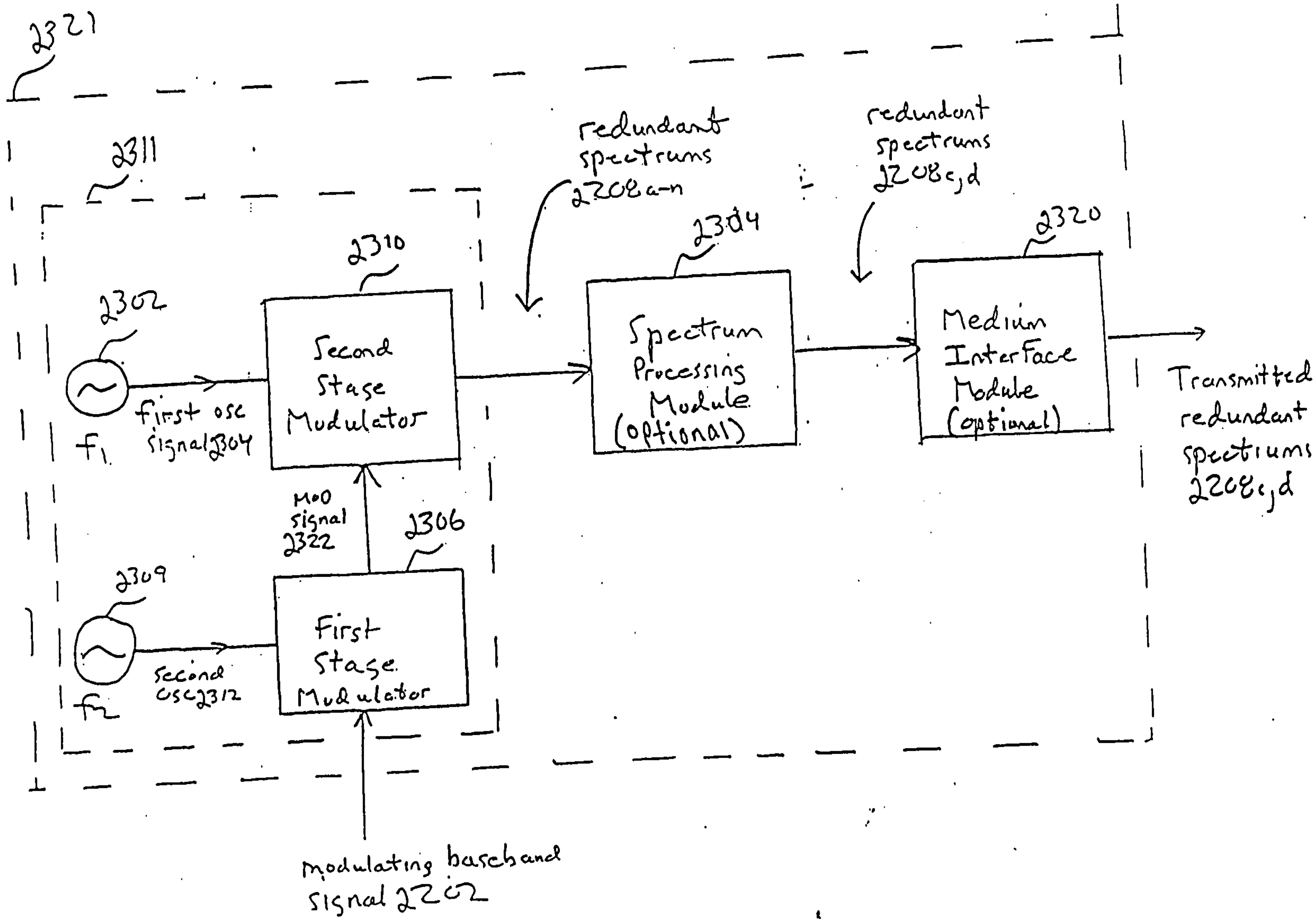


FIG. 23D

09632856 .080400

FIG. 23E

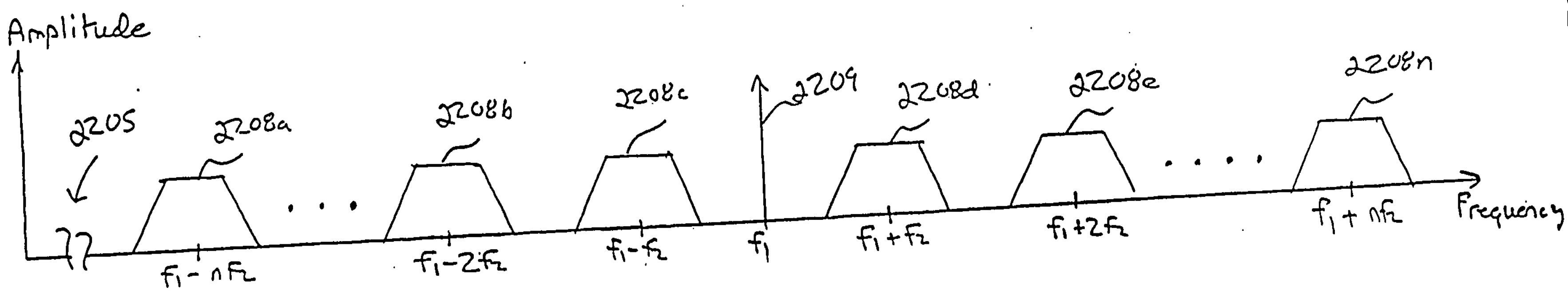
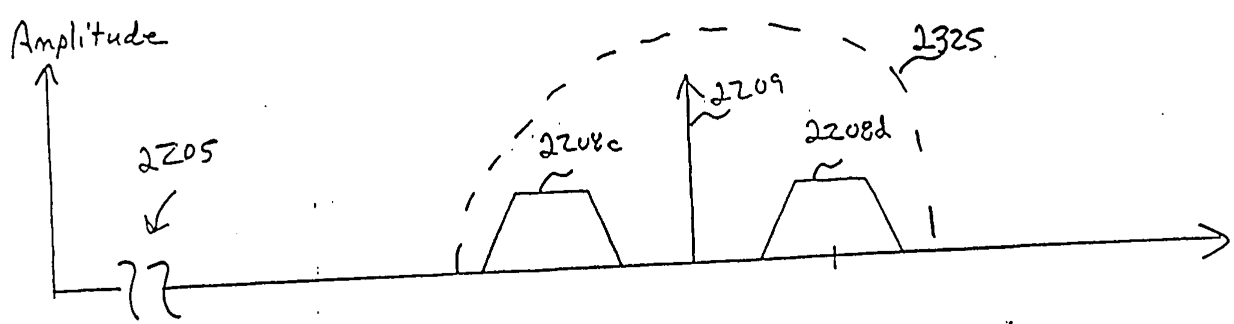


FIG. 23F



09632856 .080400

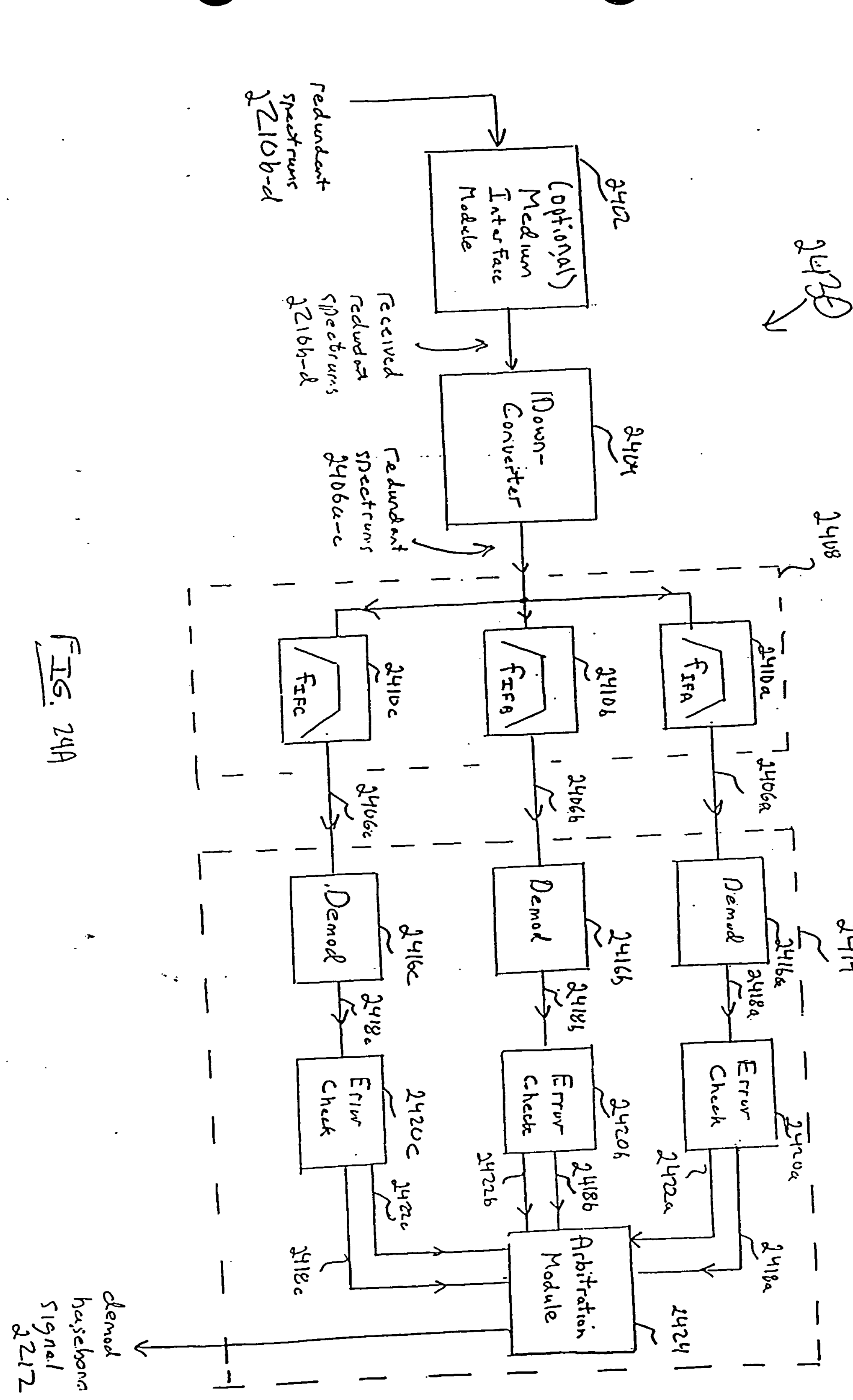

2400
redundant spectrums 2210b-d
(Optional) Medium Interface Module
2402
received redundant spectrums 2216b-d
Down-Converter
2404
redundant spectrums 2406a-c
2408
f_{IFA}
2410a
f_{IFB}
2410b
f_{IFC}
2410c
2406a
2406b
2406c
2414
Demod
2416a
Demod
2416b
Demod
2416c
2418a
2418b
2418c
Error Check
2420a
Error Check
2420b
Error Check
2420c
2422a
2422b
2422c
2418a
2418b
2418c
Arbitration Module
2424
demod baseband signal 2212

FIG. 24A

3

FIG. 24B

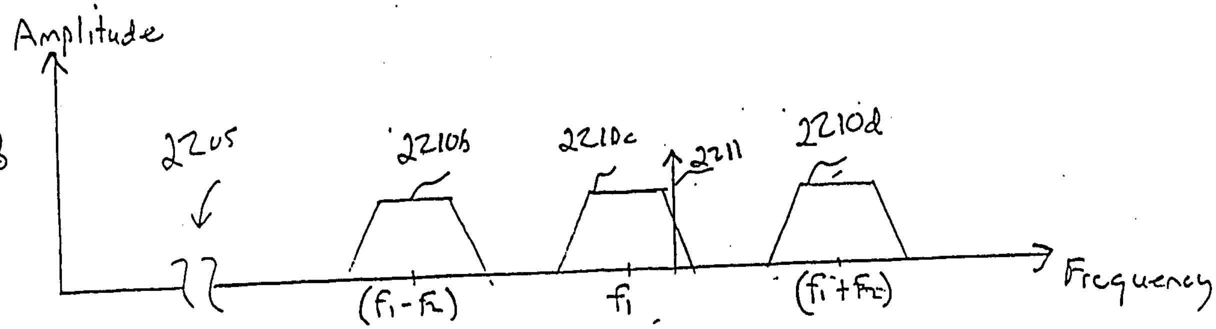
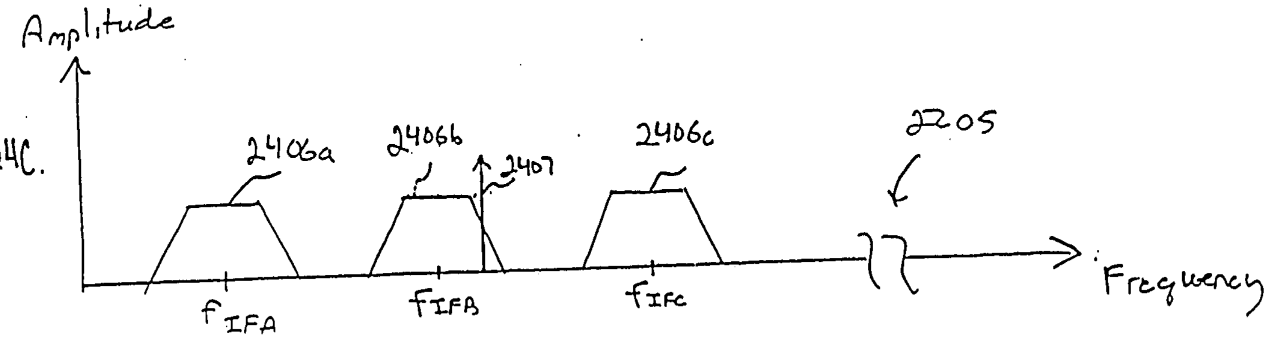


FIG. 24C.



09632856 .080400

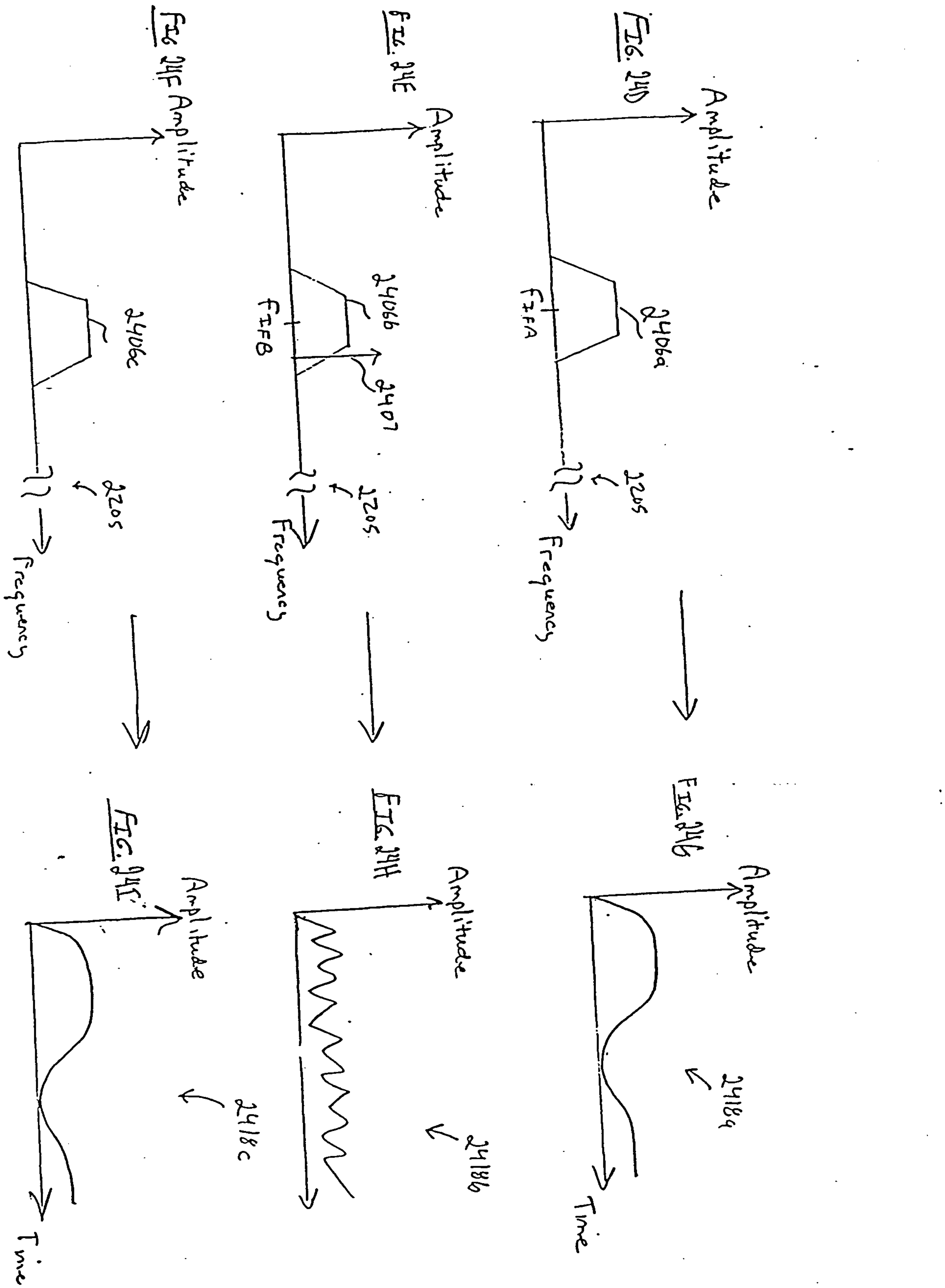


FIG. 24D
Amplitude
fIFA
2406a
2205
Frequency
FIG. 24E
Amplitude
2406b
fIFB
2407
2205
Frequency
FIG. 24F
Amplitude
2406c
2205
Frequency
FIG. 24G
Amplitude
2418a
Time
FIG. 24H
Amplitude
2418b
FIG. 24I
Amplitude
2418c
Time

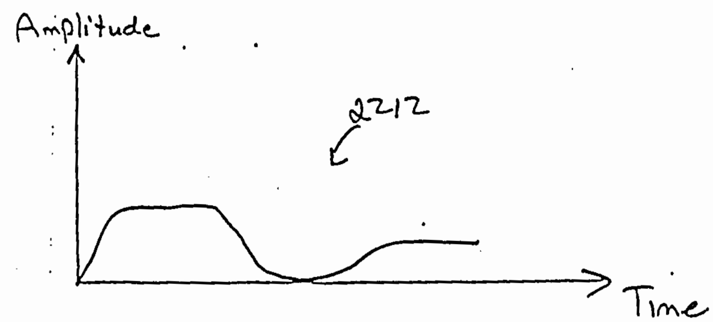


FIG. 24J

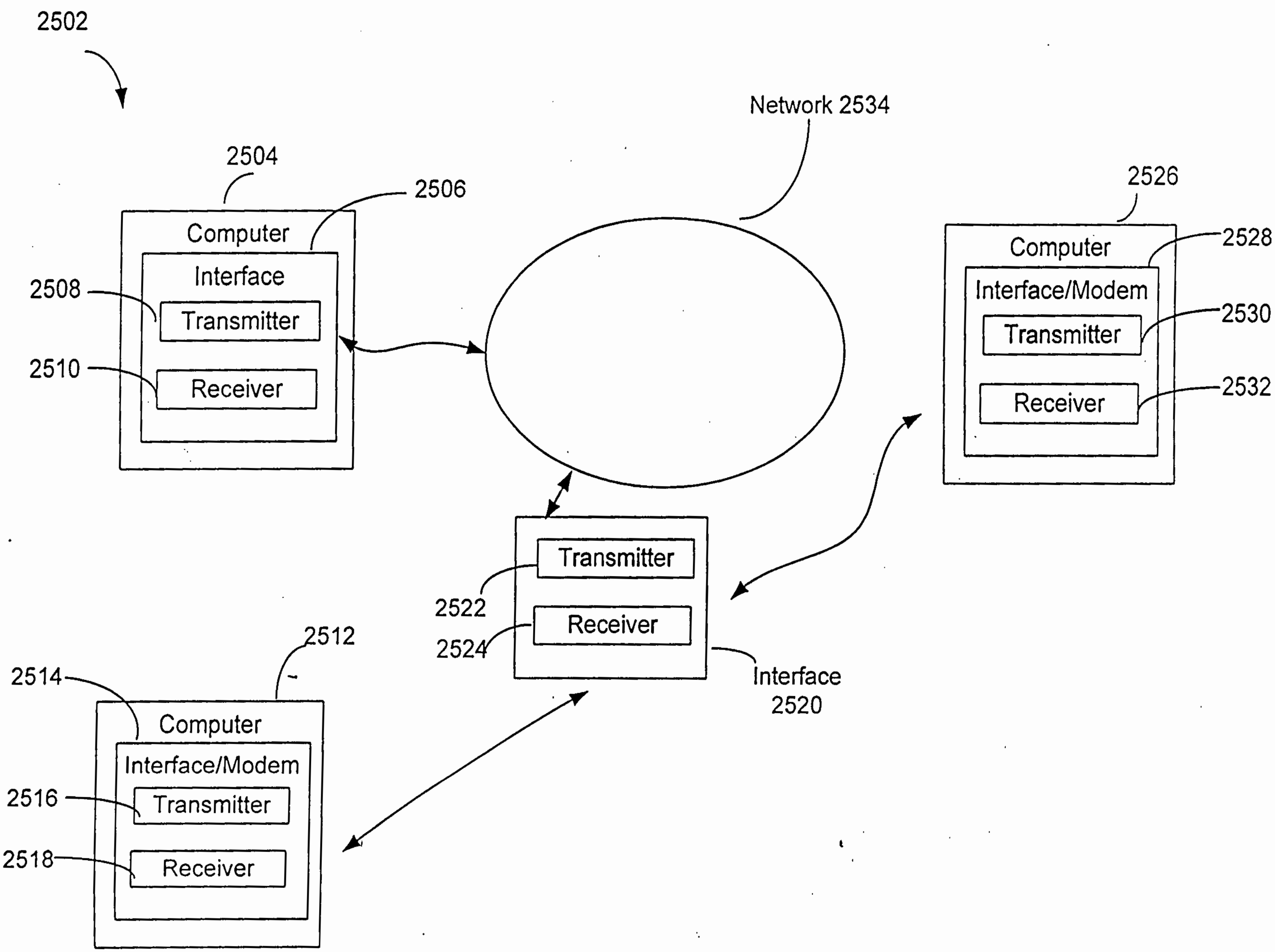

2502
2504
2506
Computer
Interface
Transmitter
Receiver
2508
2510
Network 2534
2526
2528
Computer
Interface/Modem
Transmitter
Receiver
2530
2532
Transmitter
Receiver
2522
2524
Interface
2520
2512
2514
Computer
Interface/Modem
Transmitter
Receiver
2516
2518

FIG. 25

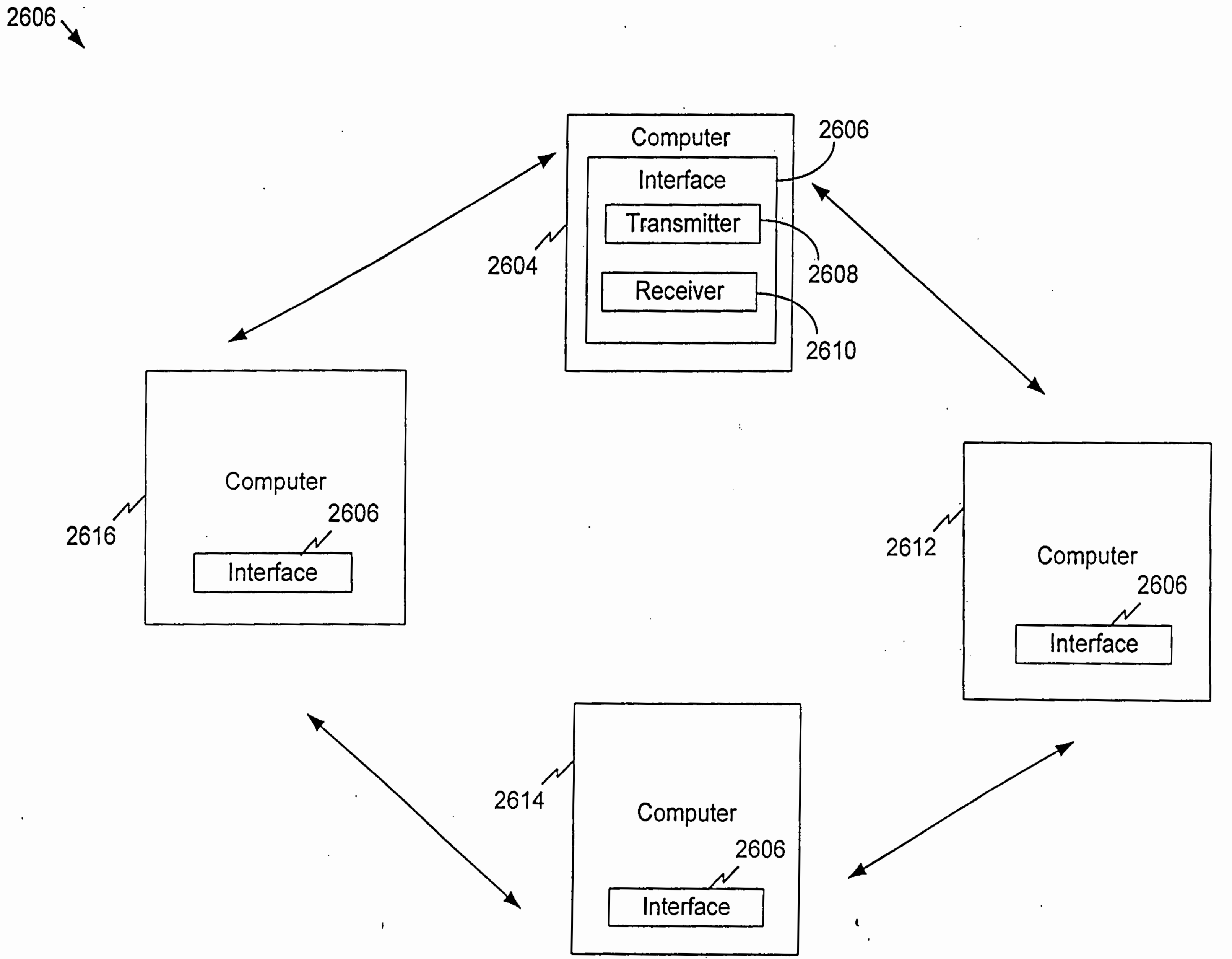

2606
Computer
Interface
Transmitter
Receiver
2606
2604
2608
2610
2616
Computer
2606
Interface
2612
Computer
2606
Interface
2614
Computer
2606
Interface

FIG. 26

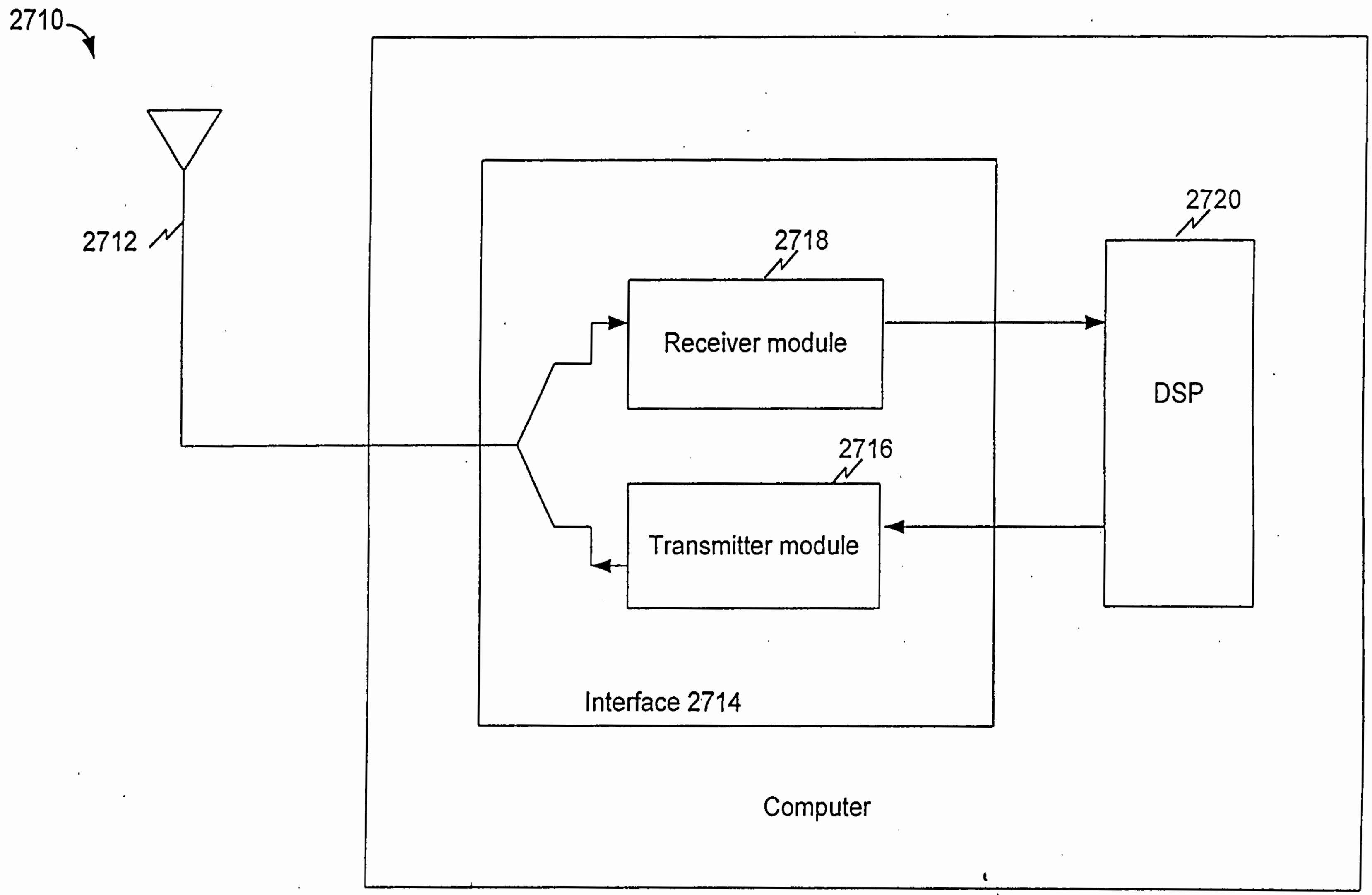
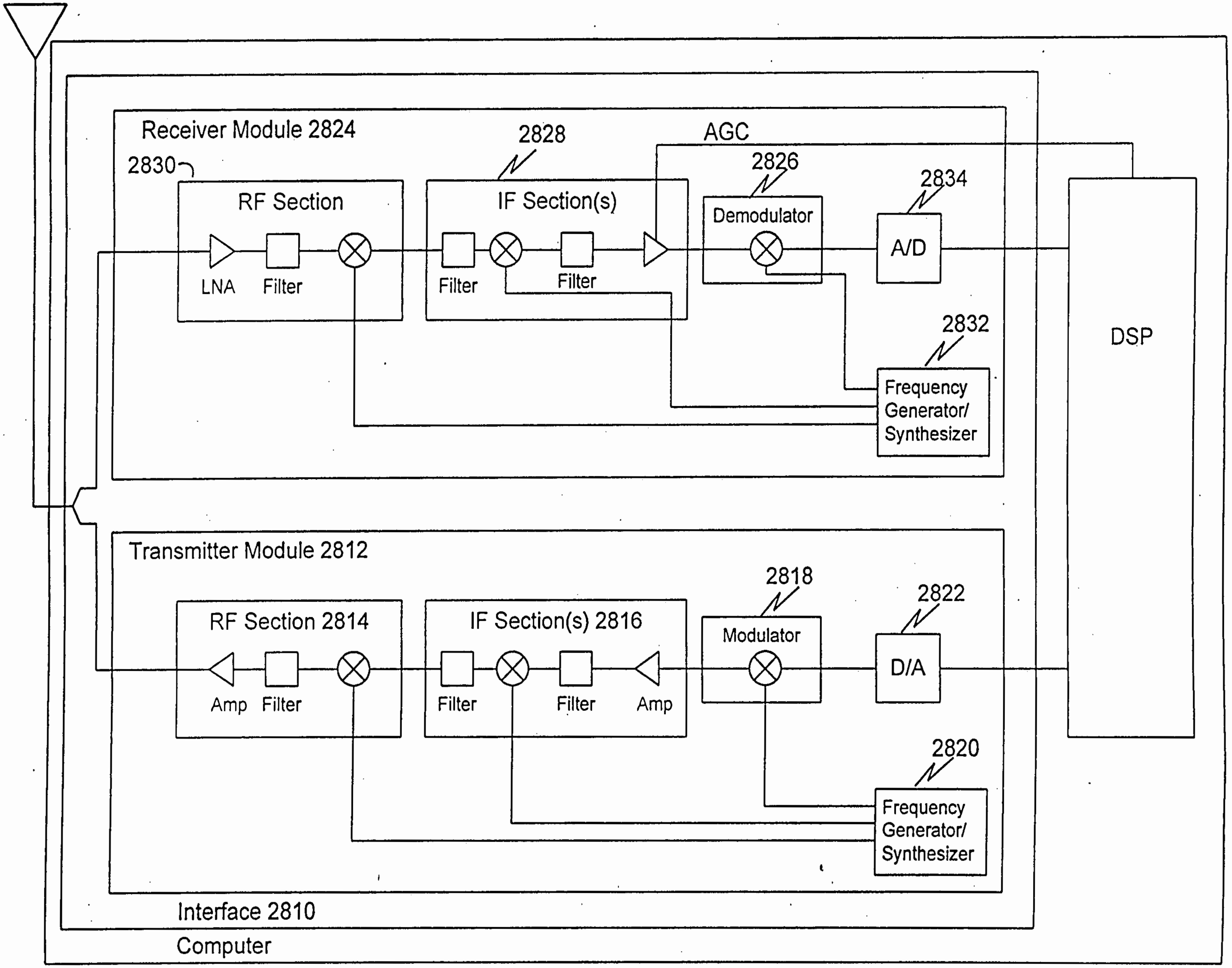


FIG. 27

9905-02.vsd/1

09632856 .080400



Heterodyne Implementation

FIG. 28

9905-02.vsd/2

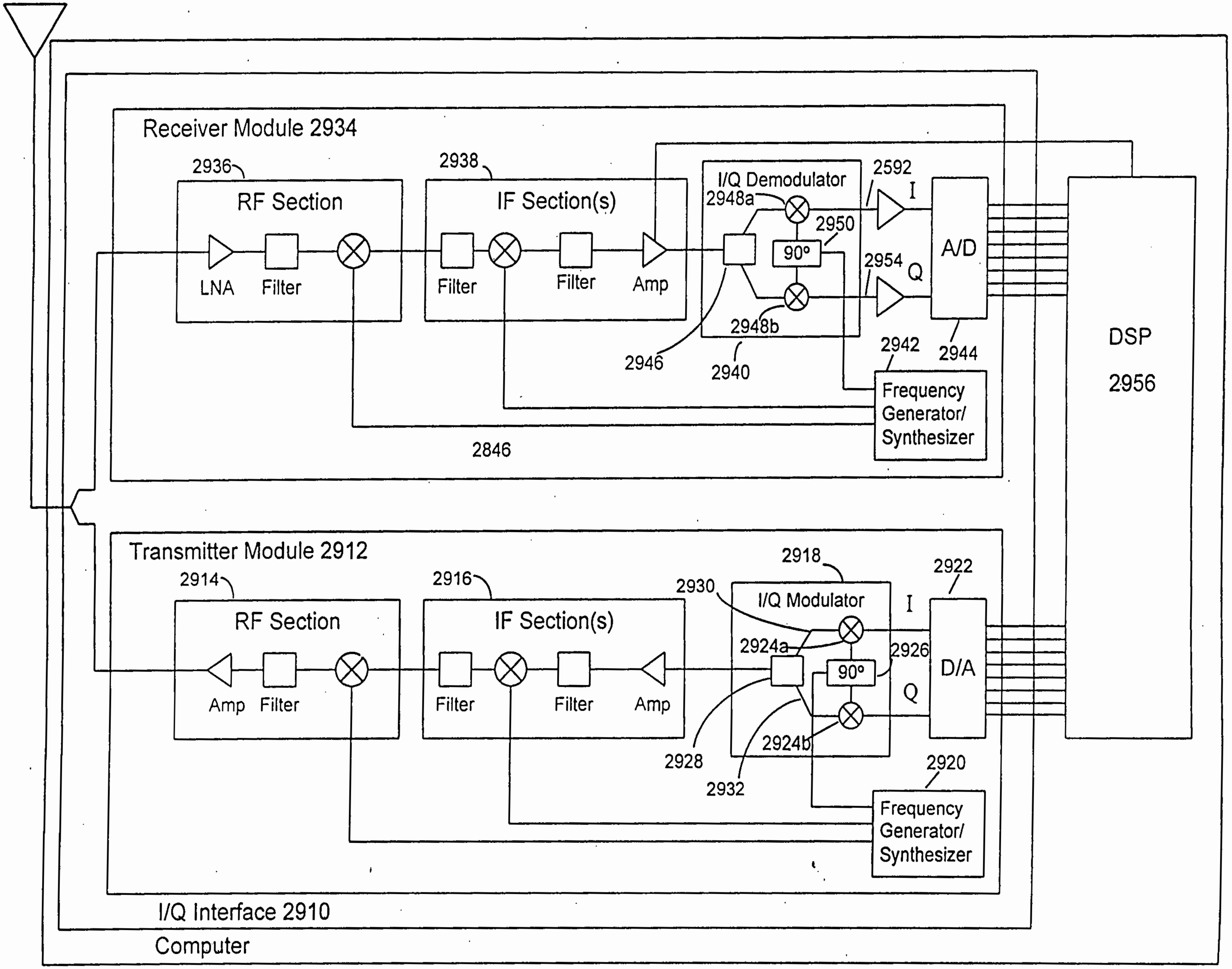


FIG. 29

0963285 .060400

9905-02.vsd/3

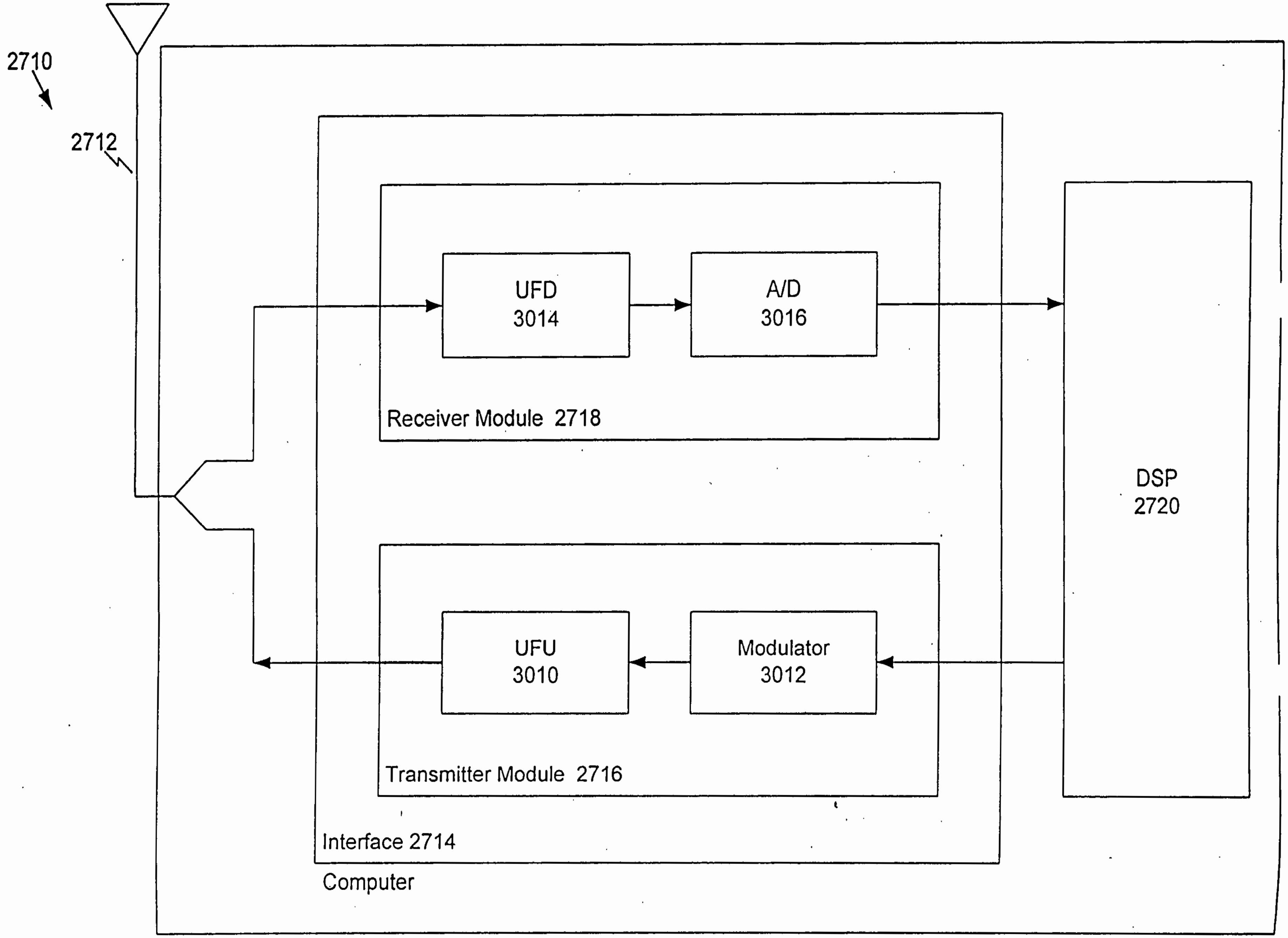


FIG. 30

09632856 .080400

9905-02.vsd/4

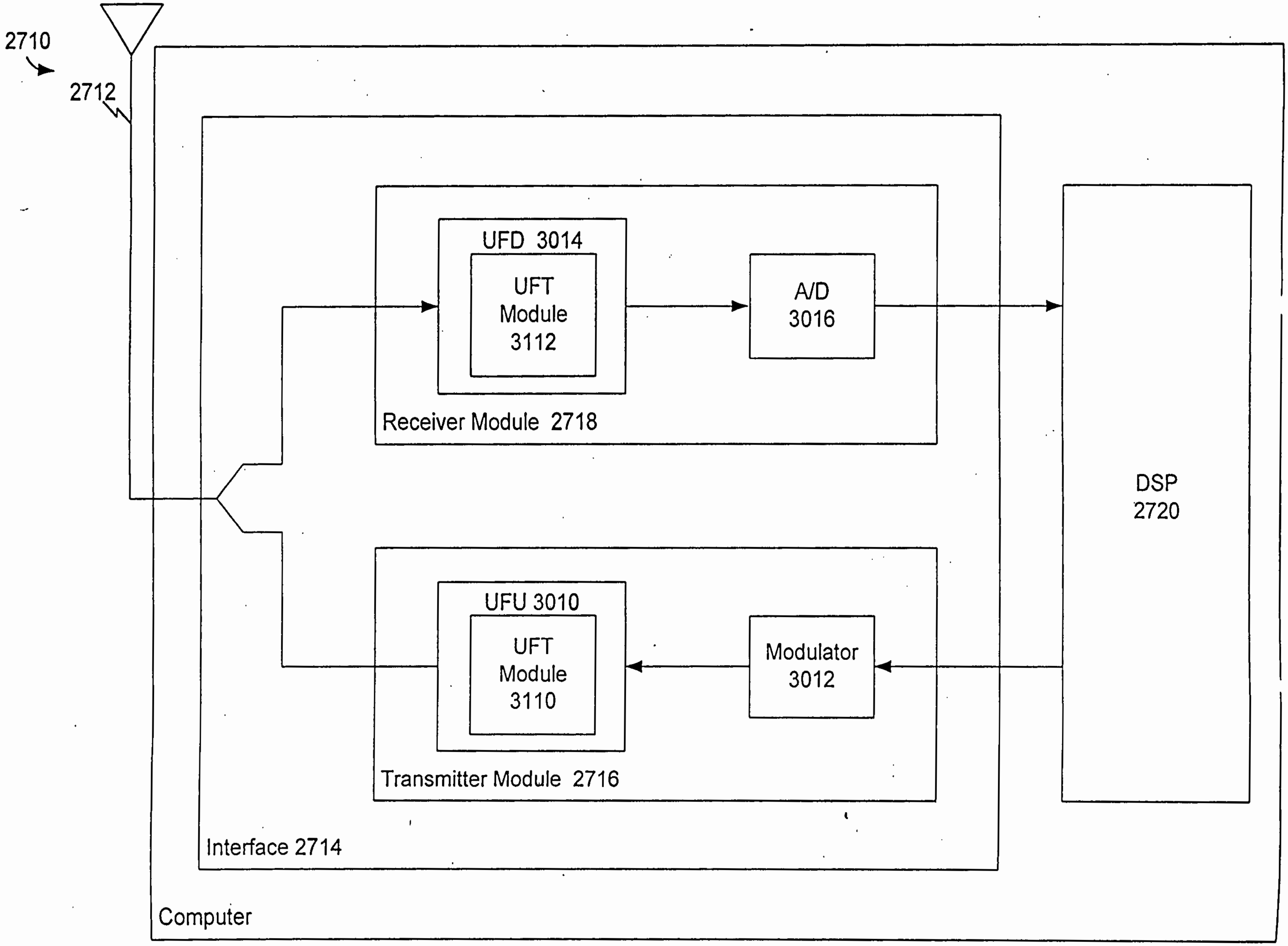

2710
2712
UFD 3014
UFT
Module
3112
A/D
3016
Receiver Module 2718
DSP
2720
UFU 3010
UFT
Module
3110
Modulator
3012
Transmitter Module 2716
Interface 2714
Computer

FIG. 31

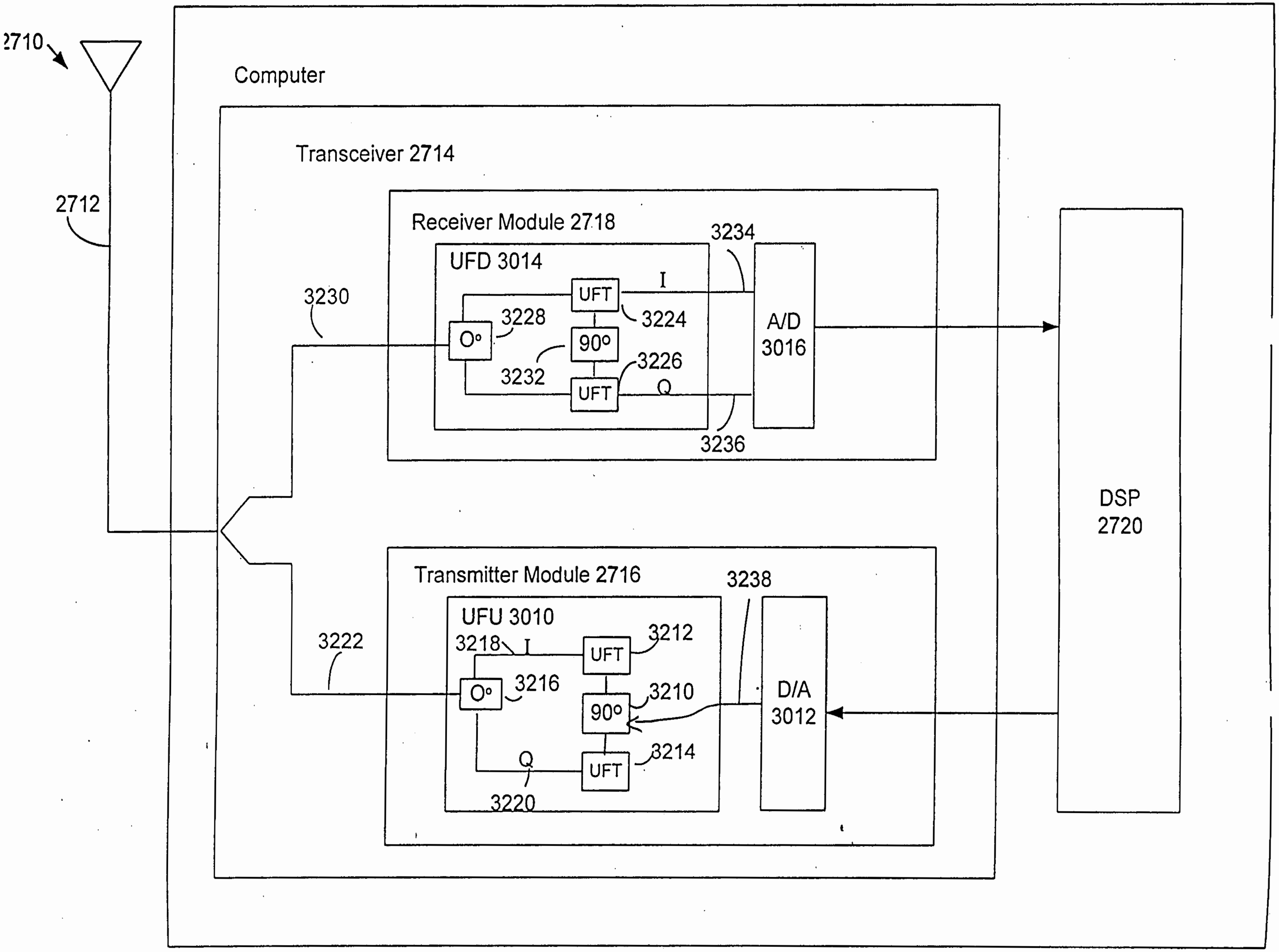
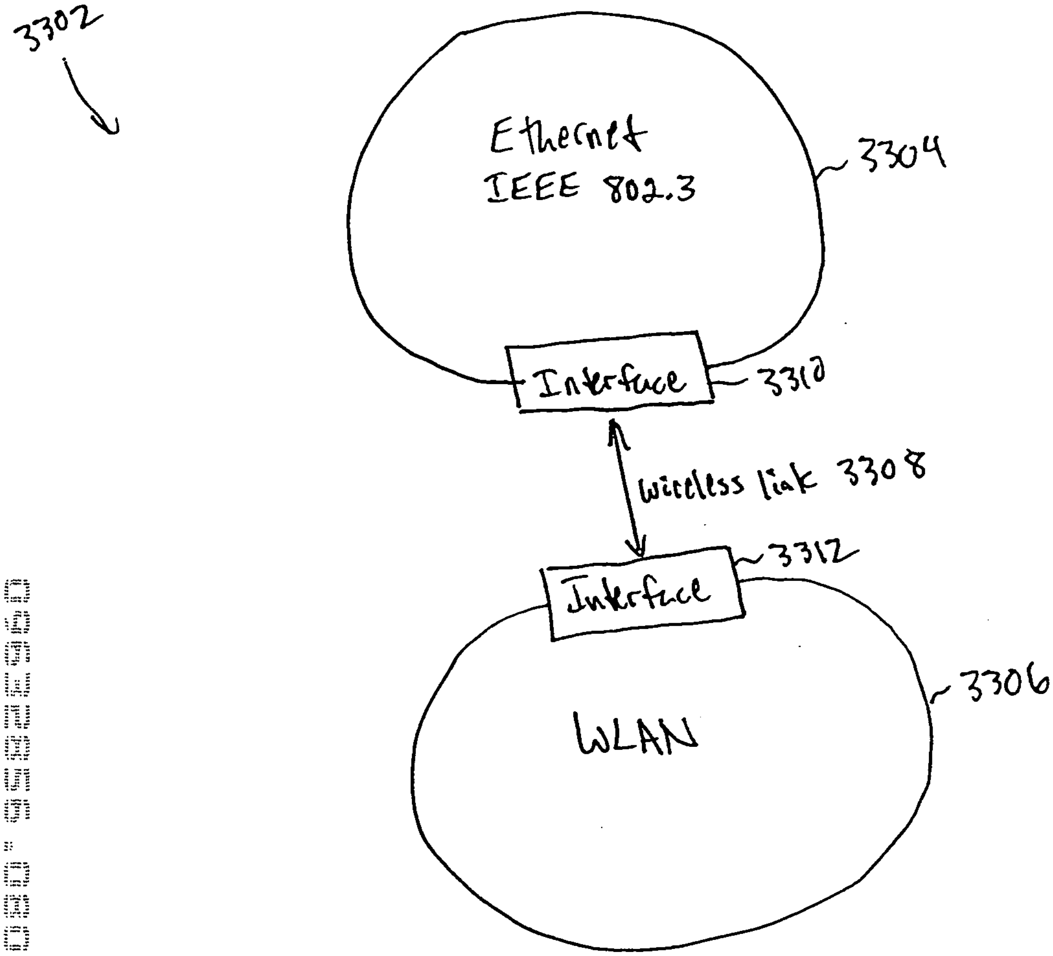

2710
2712
Computer
Transceiver 2714
Receiver Module 2718
UFD 3014
3230
UFT
I
3224
3228
O°
90°
3232
3226
UFT
Q
3234
A/D
3016
3236
DSP
2720
Transmitter Module 2716
UFU 3010
3222
3218
I
UFT
3212
O°
3216
90°
3210
Q
UFT
3214
3220
3238
D/A
3012

FIG. 32



3302
Ethernet
IEEE 802.3
3304
Interface
3310
wireless link 3308
3312
Interface
3306
WLAN

FIG. 33

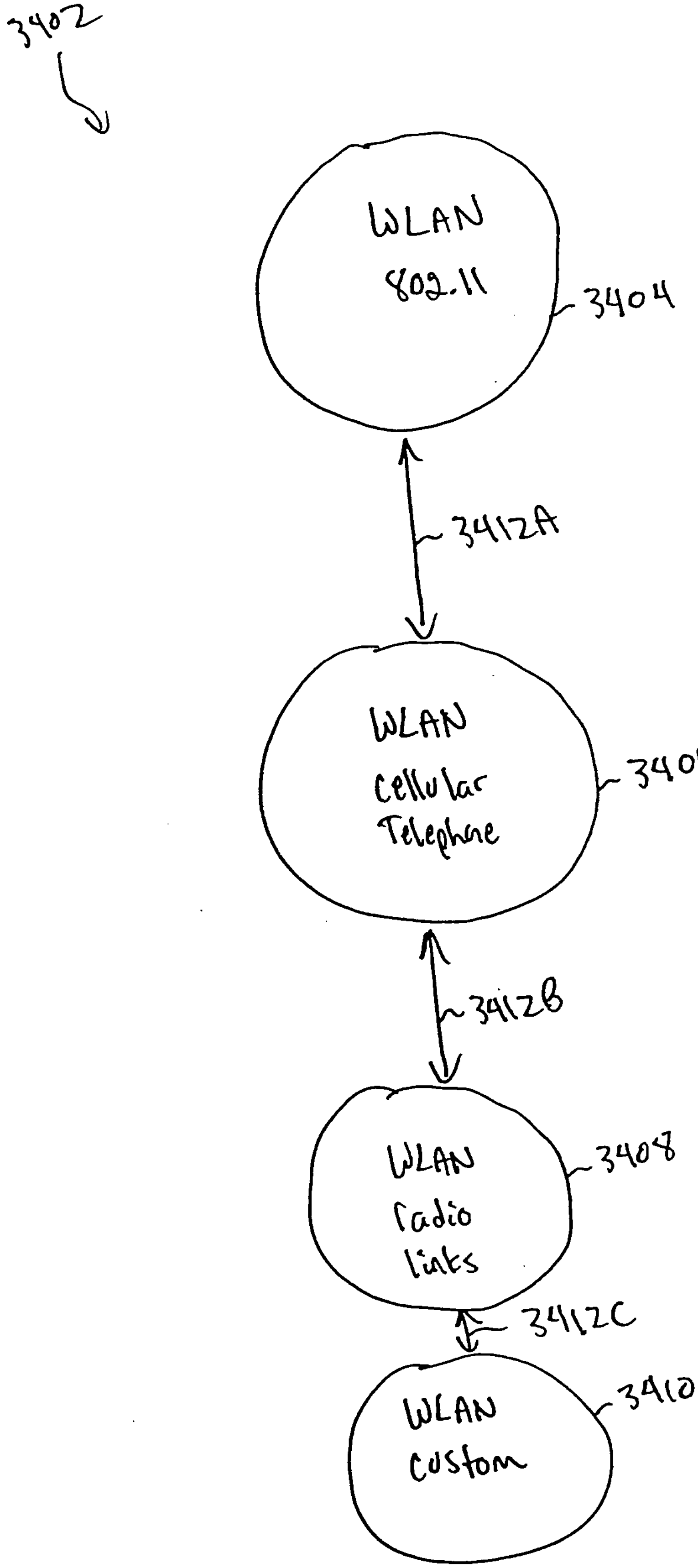

3402
WLAN 802.11
3404
3412A
WLAN Cellular Telephone
3406
3412B
WLAN radio links
3408
3412C
WLAN custom
3410

FIG. 34

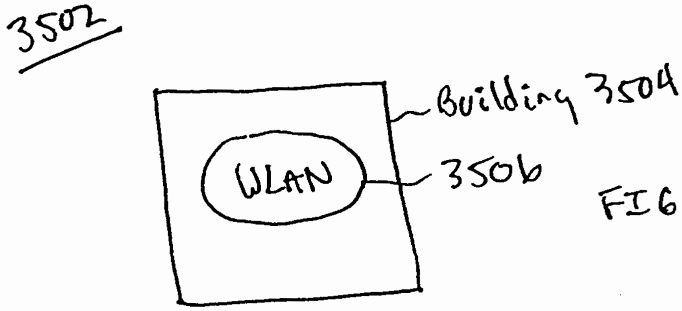

3502
Building 3504
WLAN
3506

FIG. 35

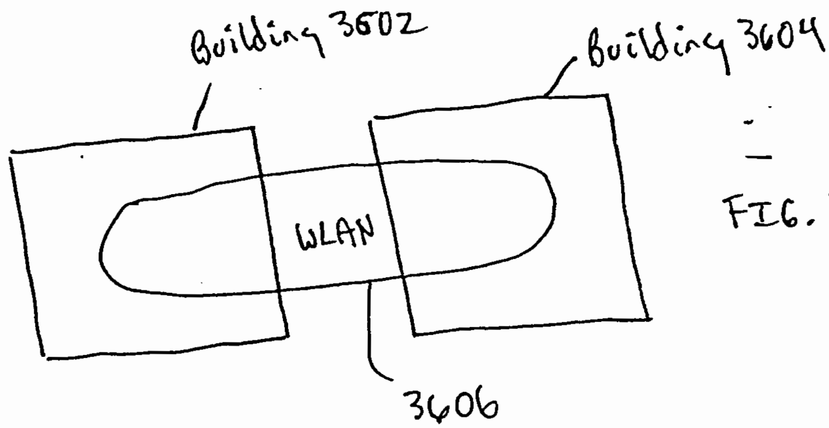

Building 3602
Building 3604
WLAN
3606

FIG. 36

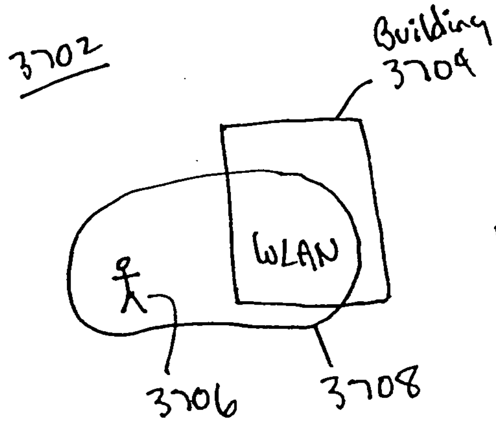

3702
Building
3704
WLAN
3706
3708

FIG. 37

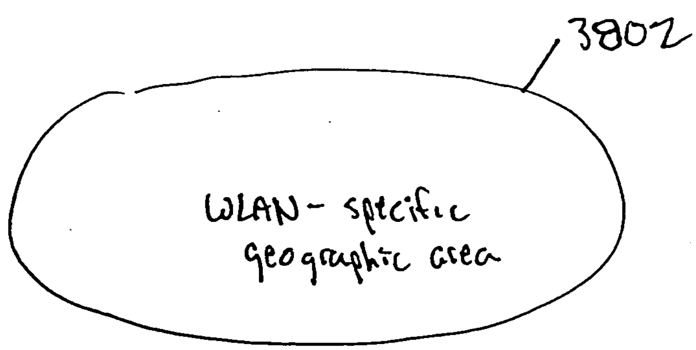
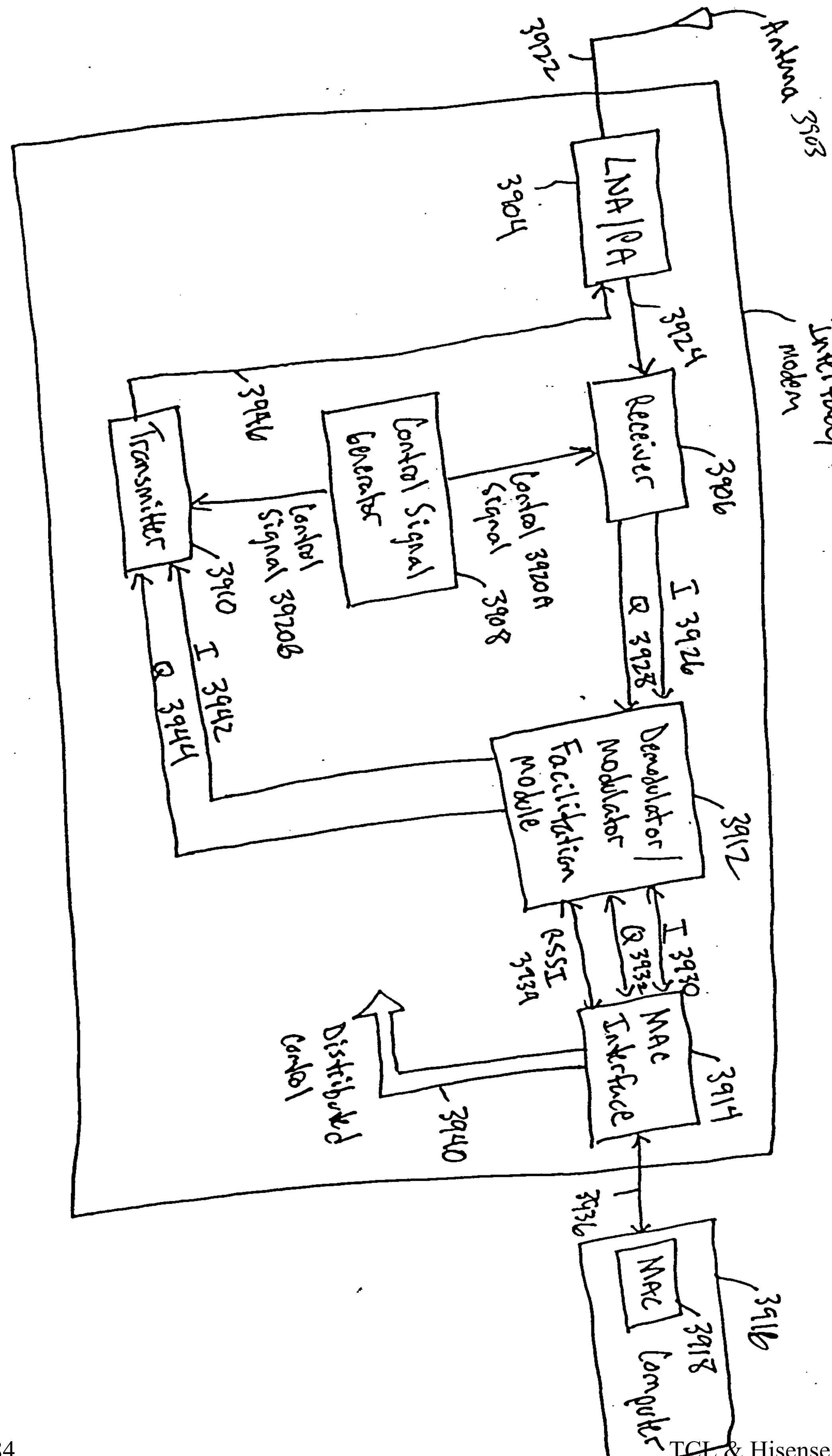

3802
WLAN-specific
geographic area

FIG. 38



Antenna 3903
3922
LNA/PA
3904
3924
WLAN Interface/modem 3902
Receiver
3906
Control Signal Generator
3908
Control Signal 3920A
Control Signal 3920B
Transmitter
3910
3946
I 3926
Q 3928
Demodulator/Modulator Facilitation Module
3912
I 3942
Q 3944
I 3930
Q 3932
RSSI 3939
MAC Interface
3914
Distributed Control
3940
3936
MAC
3918
Computer
3916

FIG. 39

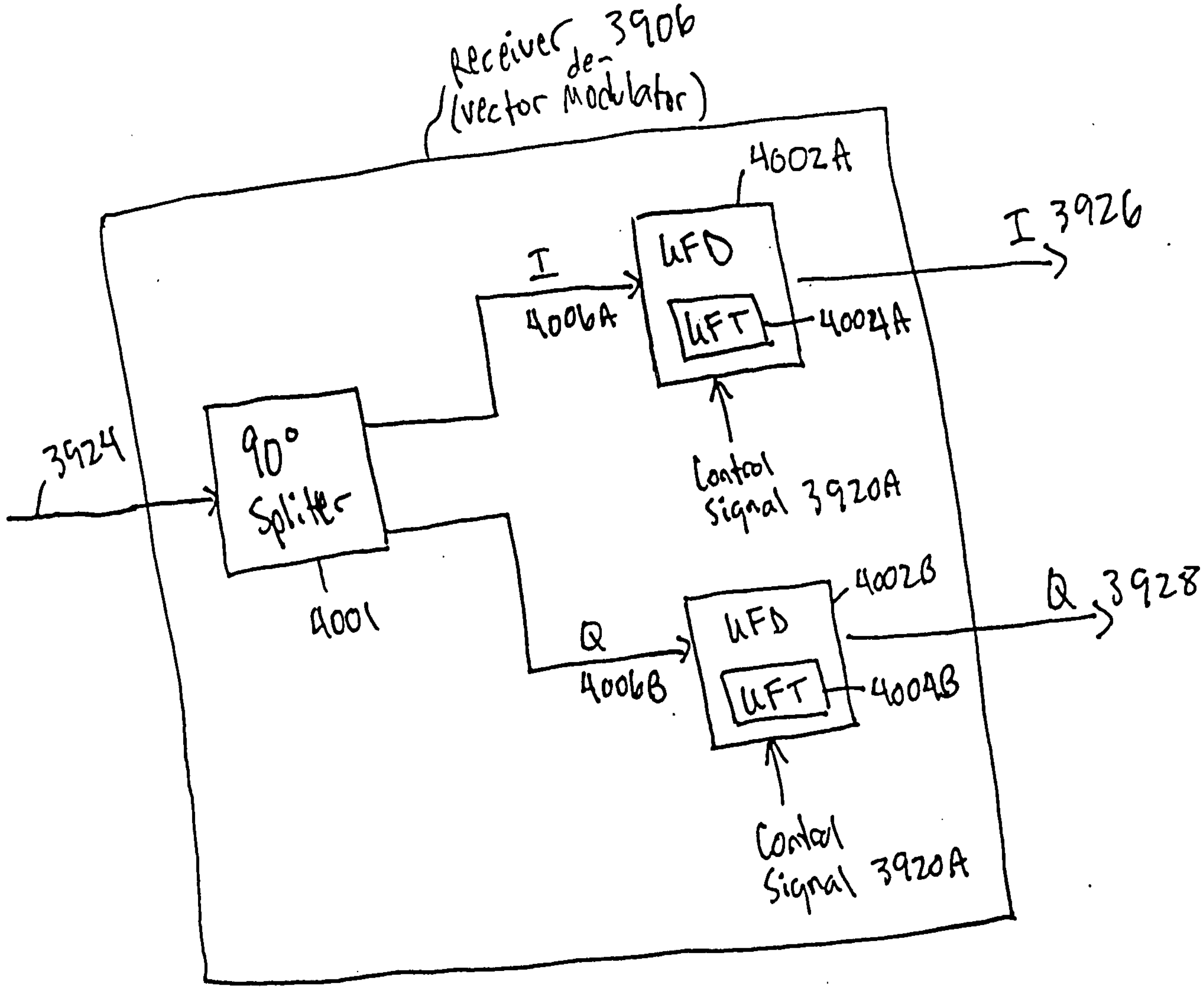


FIG. 40

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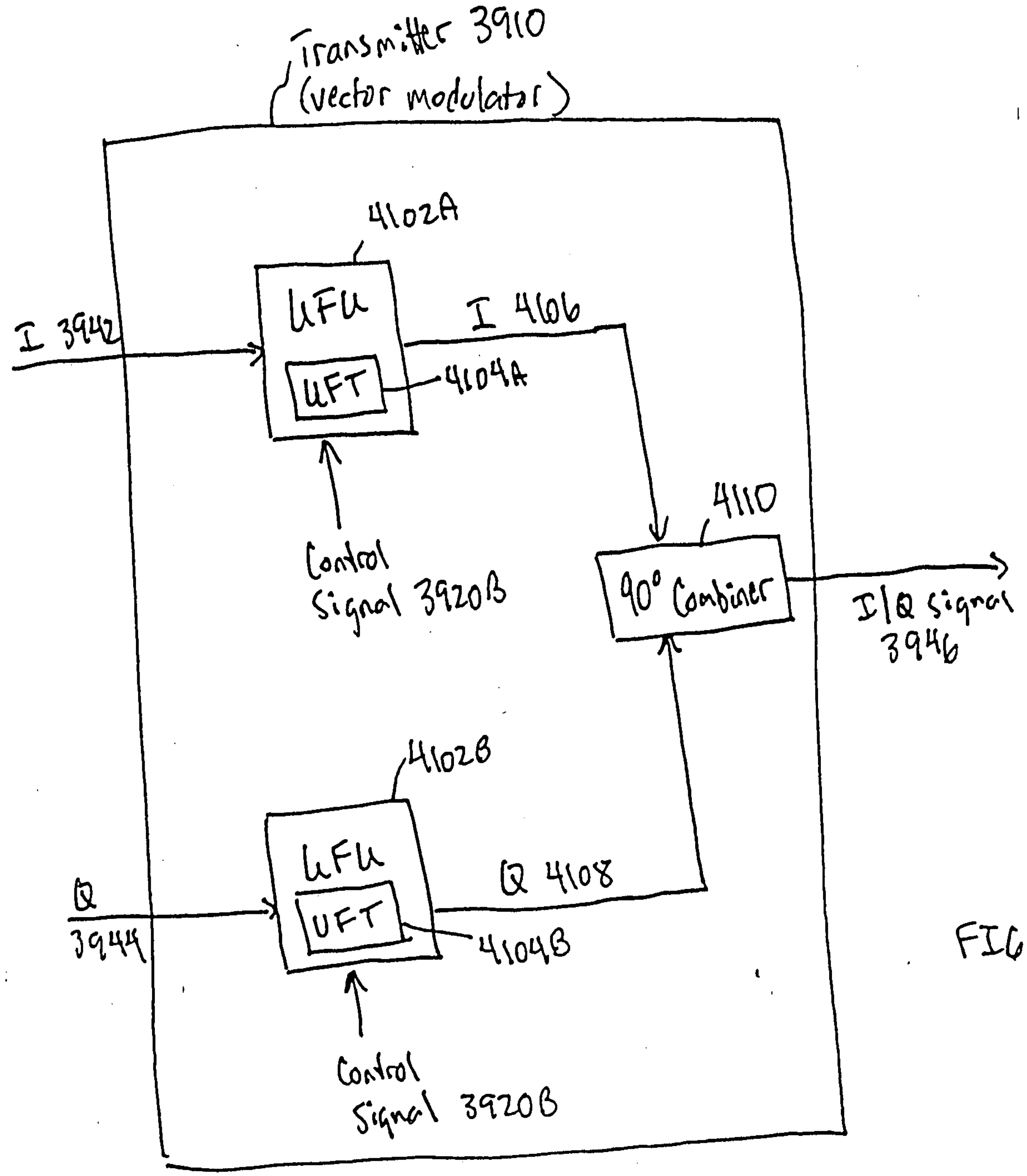
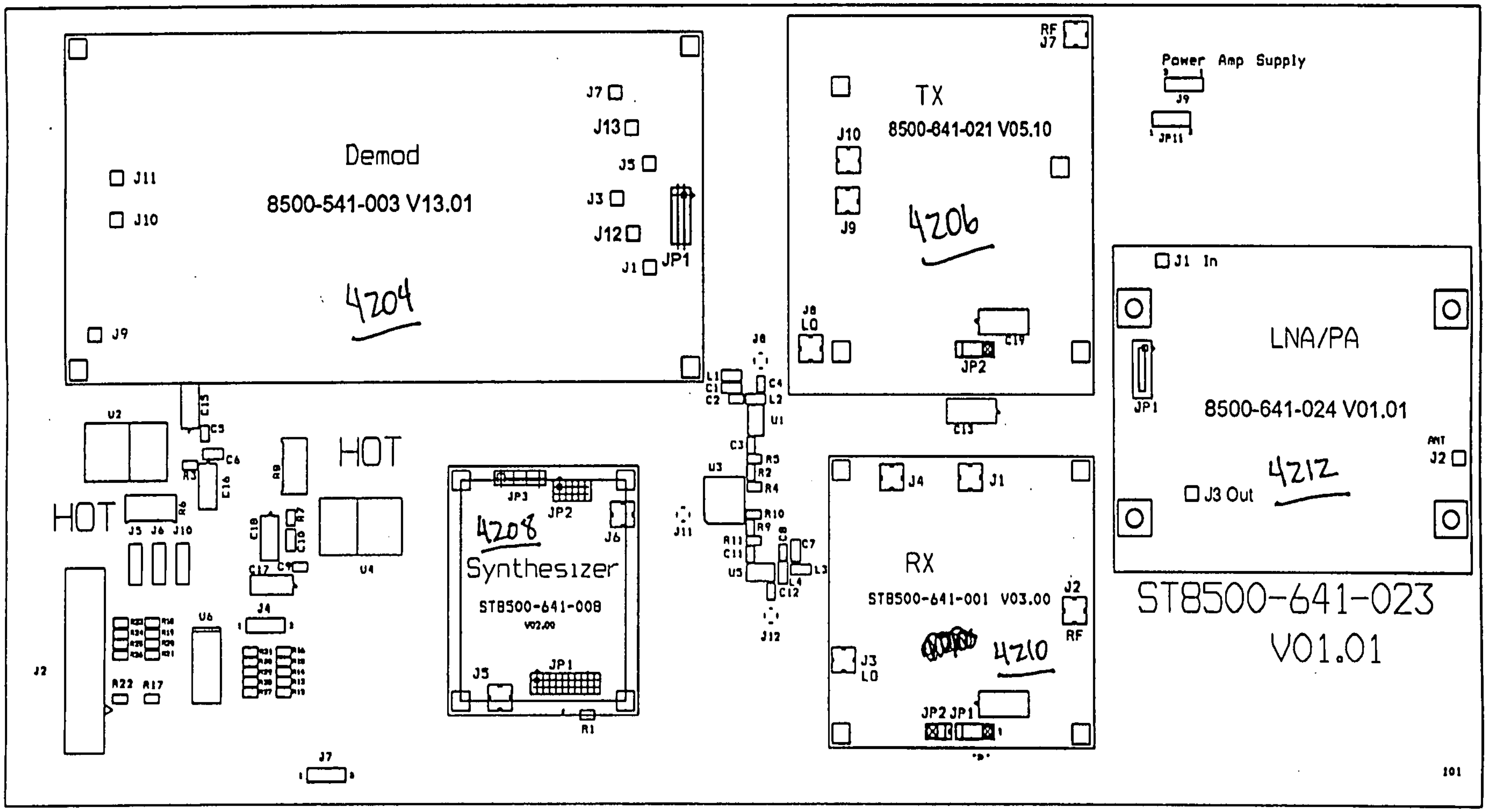


FIG. 41

09632856 .080400

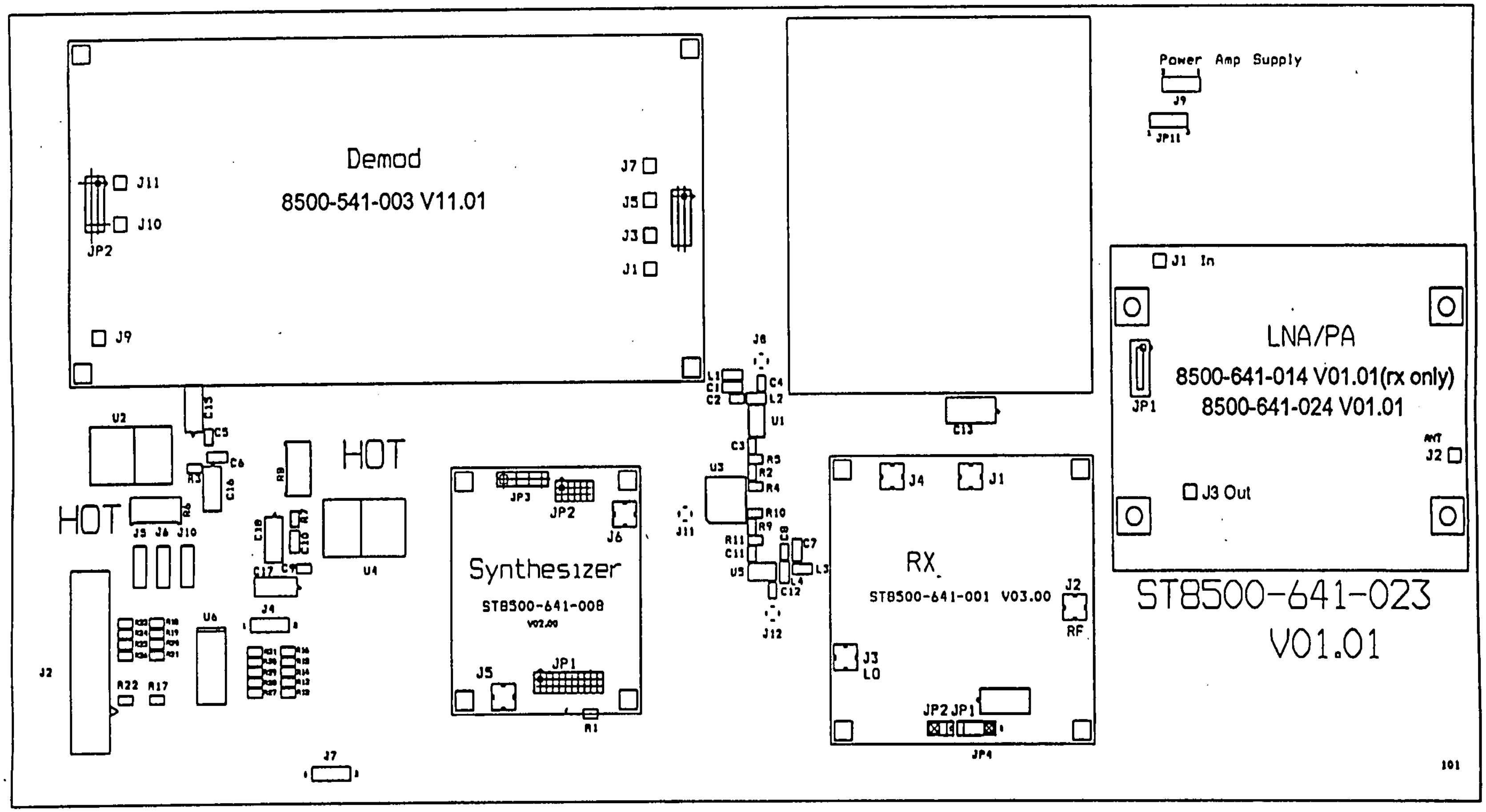
4202



T/R

FIG. 42

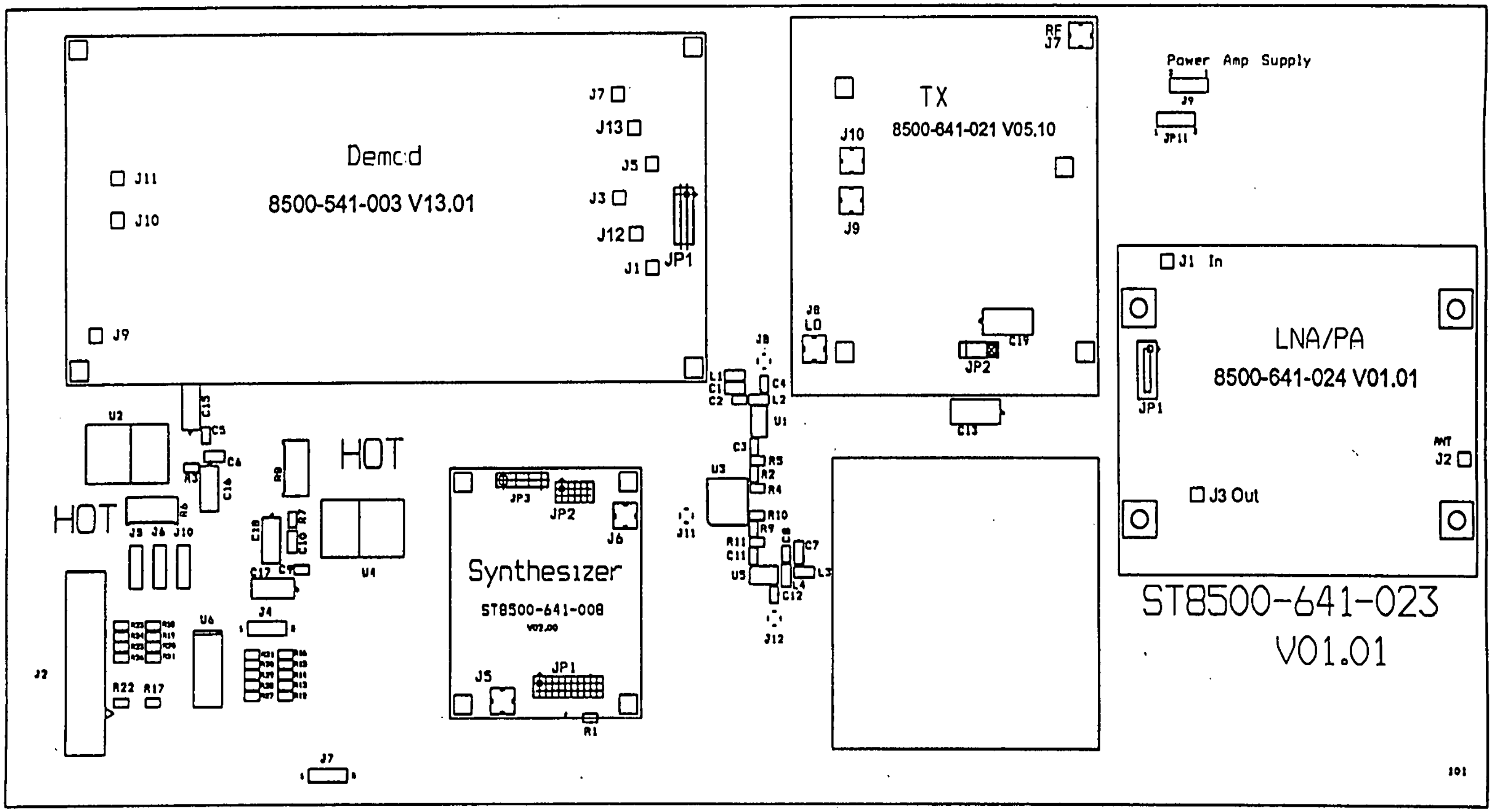
4302



Receive Only

FIG. 43

4402

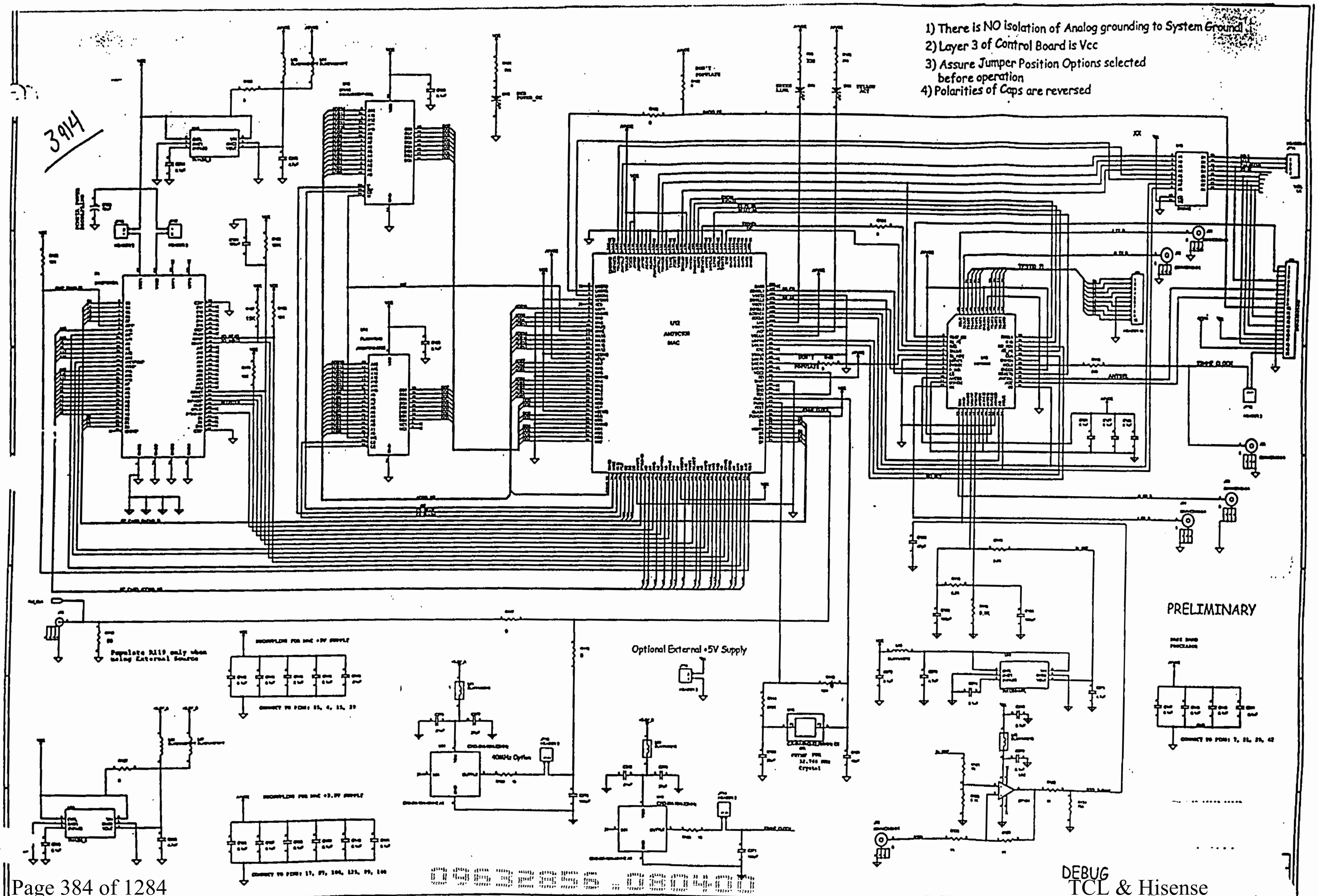


Transmit Only

FIG. 44

FIG. 45

3914



1) There is NO isolation of Analog grounding to System Ground!
2) Layer 3 of Control Board is Vcc
3) Assure Jumper Position Options selected before operation
4) Polarities of Caps are reversed
PRELIMINARY
Optional External +5V Supply
DEBUG

PARK VISION PCMCIA CONTROLLER BOM

Item	Quantity	Reference	Part Description	Part Number	Manufacturer
1	1	C123	10uF CAP 6032, Tantalum,20%	TAJT106K010R	Kemet
2	3	C263, C273, C275, C282	4.7uF CAP 6032,Tantalum,20%	T491A475M006AS	Kemet
3	25	C120, C125, C126, C127, C128, C136, C137, C138, C139, C140, C141, C142, C143, C144, C145, C147, C148, C149, C264, C272, C274, C279, C280, C281, C283	0.1uF CAP 0603,X7R,10%	GRM39X7R104K050AD	Murata
4	3	C146, C269, C276	.01uF CAP 0603,X7R,10%	GRM39X7R103K050AD	Murata
5	5	C124, C132, C133, C271, C278	100pF CAP 0603,X7R,10%	GRM39COG101K050AD	Murata
6	1	C129	47pF CAP 0603,X7R,10%	GRM39COG470J100AD	Murata
7	2	C270, C277	27pF CAP 0603,X7R,10%	GRM39COG270K050AD	Murata
8	1	C130	22pF CAP 0603,X7R,10%	GRM39COG220K050AD	Murata
9	1	C131	10pF CAP 0603,X7R,10%	GRM39COG100D050AD	Murata
10	1	DS1	LED, Green	597-3311-420	Dialight
11	1	DS2	LED Yellow	597-3401-420	Dialight
12	1	DS3	LED Red	597-3111-420	Dialight
13	6	JP12, JP13, JP14, JP15, JP16, JP17	Connector HEADER 2Pin	2MS-19-33-01	Specialty Electronics
14	1	JP11	Connector HEADER 4Pin	100/VH/TM1SQ/W.100/4	BLKCON
15	7	J16, J20, J21, J22, J23, J24, J25	Connector 82MMCX	82MMCX-50-0-1	Huber/Shuner
16	1	J18	Connector Header10	TMS-110-01-G-S	samtec
17	1	J19	Connector with Ejector	EHT-1-10-01-S-D	samtec
18	1	P1	Connector 34X2PCMCIA	DICMJ-68S-SPC-M08	ITT Canon
19	7	L59, L60, L61, L63, L64, L65, L66	Ferrite Bead	BLM11A121S	Murata
20					
21	1	R112	10M, Resistor, 0603, 5%		
22	1	R114	390K, Resistor, 0603, 5%	ERJ-3GSYJ394V	Panasonic
23	1	R105	100K, Resistor, 0603, 5%	ERJ-3GSYJ104V	Panasonic
24	4	R106, R107, R108, R111	15K, Resistor, 0603, 5%	ERJ-3GSYJ153V	Panasonic
25	1	R116	9.1K, Resistor, 0603, 5%	ERJ-3GSYJ912V	Panasonic
26	1	R115	8.2K, Resistor, 0603, 5%	ERJ-3GSYJ822V	Panasonic
27	1	R113	3.9K, Resistor, 0603, 5%	ERJ-3GSYJ392V	Panasonic
28	1	R101	750, Resistor, 0603, 5%	ERJ-3GSYJ751V	Panasonic
29	1	R110	560, Resistor, 0603, 5%	ERJ-3GSYJ561V	Panasonic
30	2	R99, R100	330, Resistor, 0603, 5%	ERJ-3GSYJ331V	Panasonic

FIG. 46A

31	1	R119	50 , Resistor, 0603, 5	ERJ-3GSYJ500V	Panasonic
32	2	R128, R129	10 , Resistor, 0603, 5	ERJ-3GSYJ100V	Panasonic
33	8	R102, R103, R104, R109, R117, R118, R120, R127	0, Resistor, 0603, 5%	RM732Z1J000ZT ERJ-3GSYJ000V	KOA Panasonic
34	6	R121, R122, R123, R124, R125, R126	TBD, Resistor, 0603, 5%	R	Panasonic
35	1	U10	SRAM	KM62256DLTG-5L M5M5256CVP-55LL	Samsung Mitsubushi
36	1	U12	MAC	AM79C930	AMD
37	1	U13	Baseband Processor	HFA3842 A1	Harris
38	1	U14	FLASH RAM	AM29F010-55EC	AMD
39	1	U15	32 KHz Crystal	CX-6V-SM2-32.768KHz C/I	Statek
40	2	U45	Bus Buffer	DS3862	National
41	1	U48	Regulator 3.5 V	TK11235BMC	TOKO
42	1	U49	22MHz Oscillator	FOX F3346-22MHz	FOX
43	1	U50	2 Volt Refference	TK11220BMC	TOKO
44	1	U51	40MHz Oscillator	CXO-M-10N-40MHz A/I	Statek

FIG. 46B

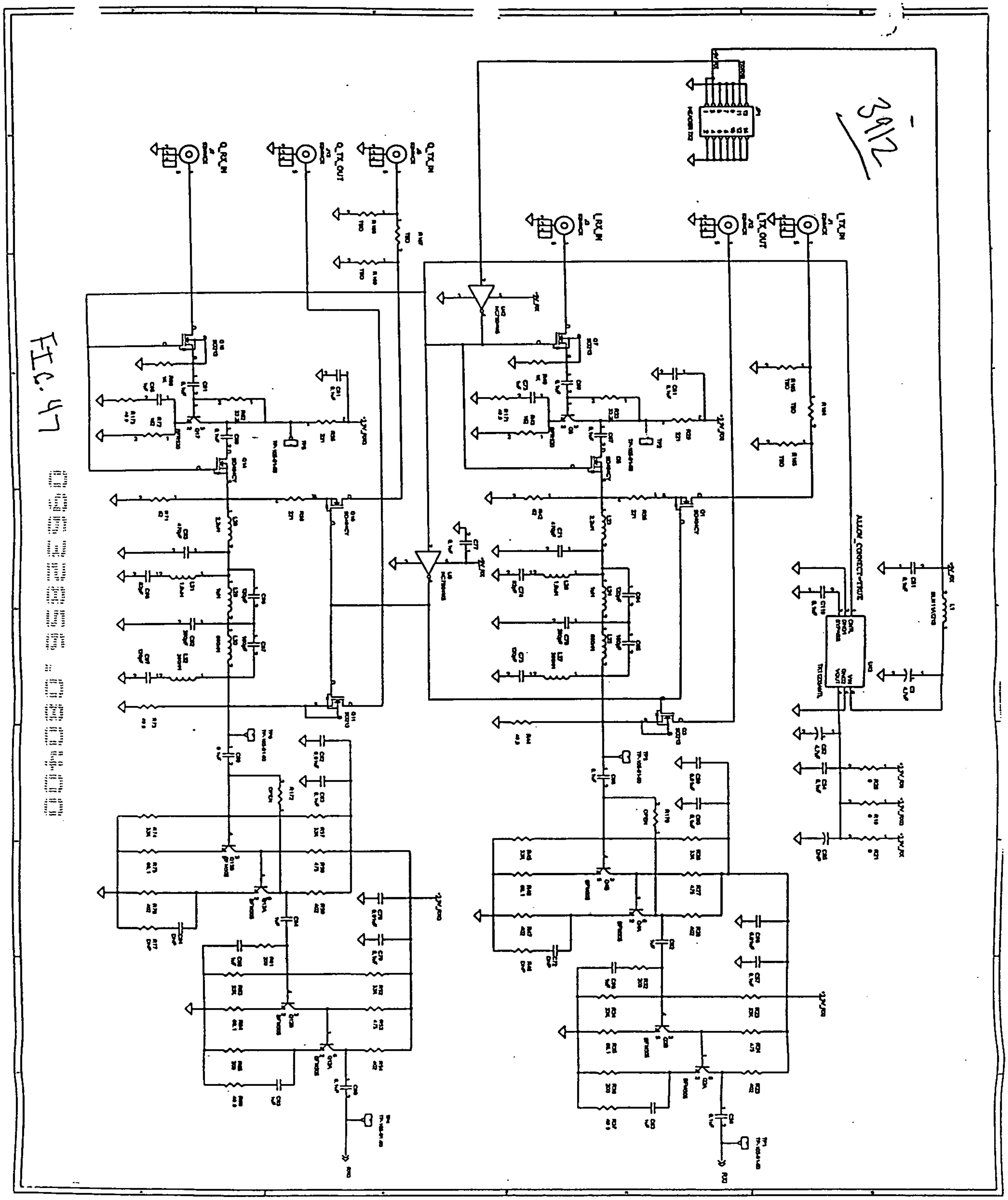
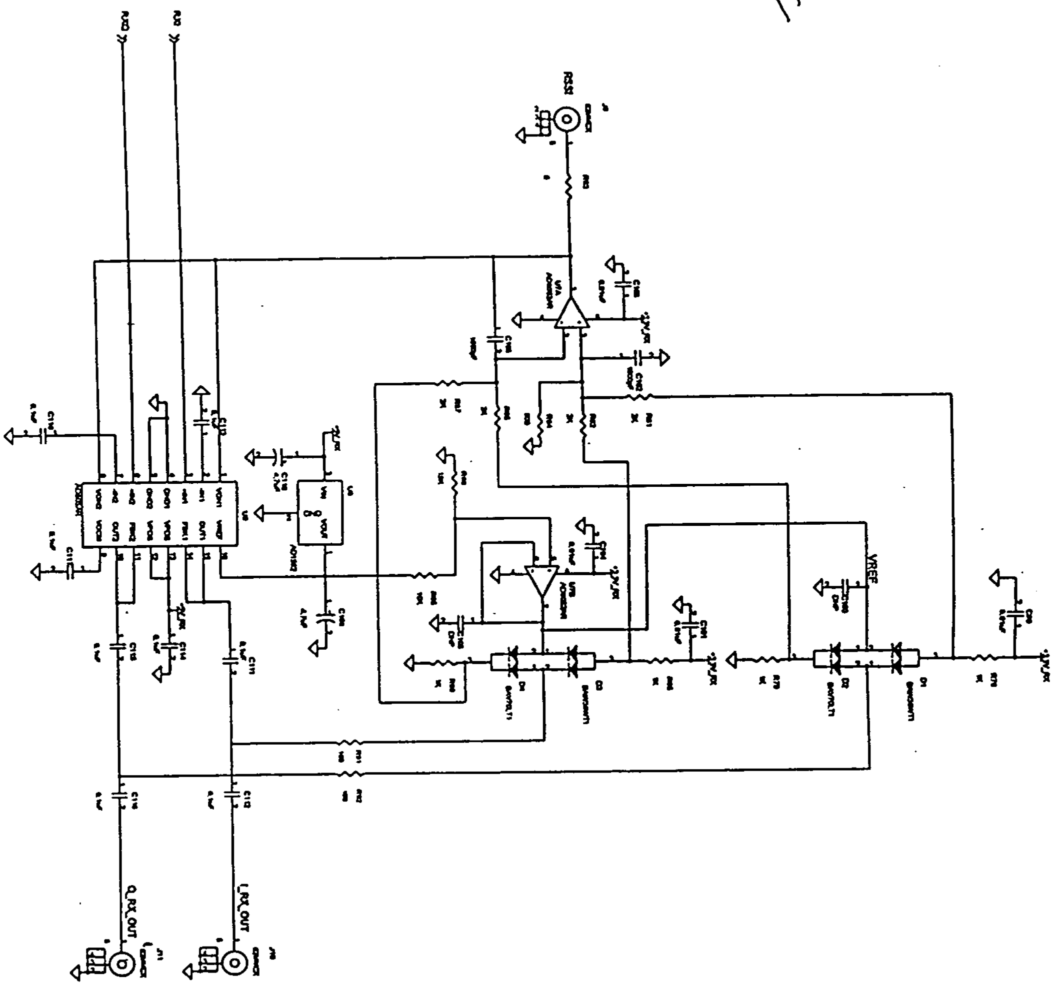


FIG. 47

3912

FIG. 48

09653856 .080400



Item	Quantity	Reference	Part	Part Number	Manufacturer
1	4	C3,C52,C108,C110	4.7uF	T491A475K006AS	KEMET
2	26	C51,C54,C57,C58,C60,C61,	0.1uF	GRM39Y5V104Z016	Murata
		C67,C68,C69,C77,C79,C80,			
		C81,C83,C89,C90,C91,C111,			
		C112,C113,C114,C115,C116,			
		C117,C118,C119			
3	1	C55	DNP	T491A475K006AS	KEMET
4	8	C56,C59,C78,C82,C99,C101,	0.01uF	GRM39X7R103K050	Murata
		C103,C104			
5	8	C62,C63,C66,C73,C84,C85,	1uF	GRM40Y5V105Z016	Murata
		C88,C95			
6	4	C64,C75,C86,C97	120pF	GRM39COG121J050	Murata
7	2	C65,C87	180pF	GRM39COG181J050	Murata
8	2	C70,C92	390pF	GRM39COG391J050	Murata
9	2	C71,C93	470pF	GRM39COG471J050	Murata
10	2	C72,C94	DNP	GRM40Y5V105Z016	Murata
11	2	C74,C96	82pF	GRM39COG820J050	Murata
[illegible]	2	C100,C106	DNP	DNP	Murata
13	2	C105,C102	1000pF	GRM39COG102K050	Murata
14	2	D3,D1	BAW56WT1	BAW56WT1	Motorola
15	2	D4,D2	BAV70LT1	BAV70LT1	Motorola
16	1	JP1	HEADER 7X2	FTSH-107-02-L-D	Samtec
17	9	J1,J3,J5,J7,J9,J10,J11,	82MMCX	82MMCX-50-0-1	Suhner
		J12,J13			
18	1	L1	BLM11A121S	BLM11A121S	Murata
19	2	L23,L28	2.2uH	LQG21N2R2K10	Murata
20	2	L29,L24	1uH	LQG21N1R0K10	Murata
21	2	L30,L25	680nH	LQG21NR68K10	Murata
22	2	L26,L31	1.8uH	LQG21N1R8K10	Murata
23	2	L32,L27	390nH	LQG21NR39K10	Murata
24	4	Q1,Q5,Q10,Q14	SD404CY	SD404CY	Calogic
25	4	Q2,Q4,Q12,Q13	BFM505	BFM505	Philips
26	4	Q3,Q7,Q11,Q16	SD213	SD213	Calogic
27	2	Q17,Q8	BFR520	BFR520	Philips
28	4	R19,R20,R21,R83	0	ERJ3GSY0R00	Panasonic
29	8	R23,R26,R34,R45,R52,R57,	33K	ERJ3GSYJ333	Panasonic
		R63,R74			
30	4	R24,R27,R53,R58	475	ERJ3EKF4750	Panasonic
31	6	R25,R28,R47,R54,R59,R76	402	ERJ3EKF4020	Panasonic
32	4	R29,R30,R55,R56	221	ERJ3EKF2210	Panasonic
33	2	R32,R61	200	ERJ3GSYJ201	Panasonic
[illegible]	2	R33,R62	33.2K	ERJ3GSYJ333	Panasonic
	4	R35,R46,R64,R75	68.1	ERJ3EKF68R1	Panasonic

FIG. 49A

36	2	R36,R65	200	ERJ3EKF2000	Panasonic
7	6	R37,R44,R66,R73,R171,	49.9	ERJ3EKF49R9	Panasonic
		R173			
38	6	R40,R68,R78,R79,R80,R89	1K	ERJ3EKF1001	Panasonic
39	2	R42,R71	62	ERJ3GSYJ620	Panasonic
40	2	R43,R72	162	ERJ3EKF1620	Panasonic
41	2	R77,R48	DNP	ERJ3GSYJ330	Panasonic
42	4	R81,R82,R85,R87	2K	ERJ3EKF2001	Panasonic
43	1	R84	909	ERJ3EKF9090	Panasonic
44	1	R88	15K	ERJ3EKF1502	Panasonic
45	1	R90	10K	ERJ3EKF1002	Panasonic
46	2	R91,R92	100	ERJ3EKF1000	Panasonic
47	6	R164,R165,R166,R167,R168,	TBD		Panasonic
		R169			
48	2	R170,R172	OPEN		Panasonic
49	6	TP1,TP2,TP3,TP4,TP5,TP6	TP-105-01-00		
50	2	U42,U6	NC7S04M5	NC7S04M5	National Semiconductor
51	1	U7	AD8052AR	AD8052AR	Analog Devices
52	1	U8	AD1582	AD1582	Analog Devices
53	1	U9	AD605AR	AD605AR	Analog Devices
54	1	U43	TK11235AMTL	TK11235BM	Toko
55	1		Board	8500.541.003 V13.01	

FIG. 49B

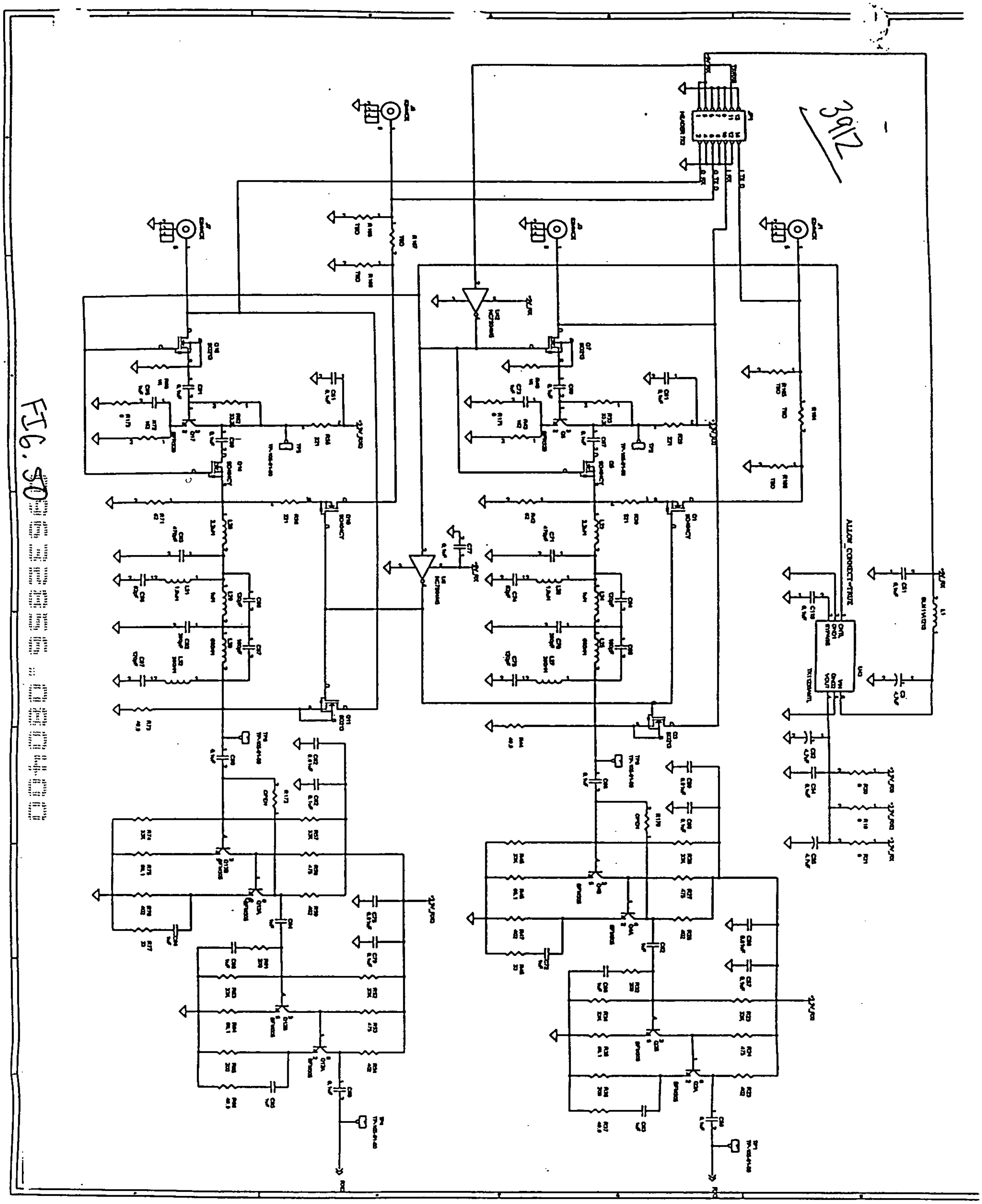


FIG. 5D

3912

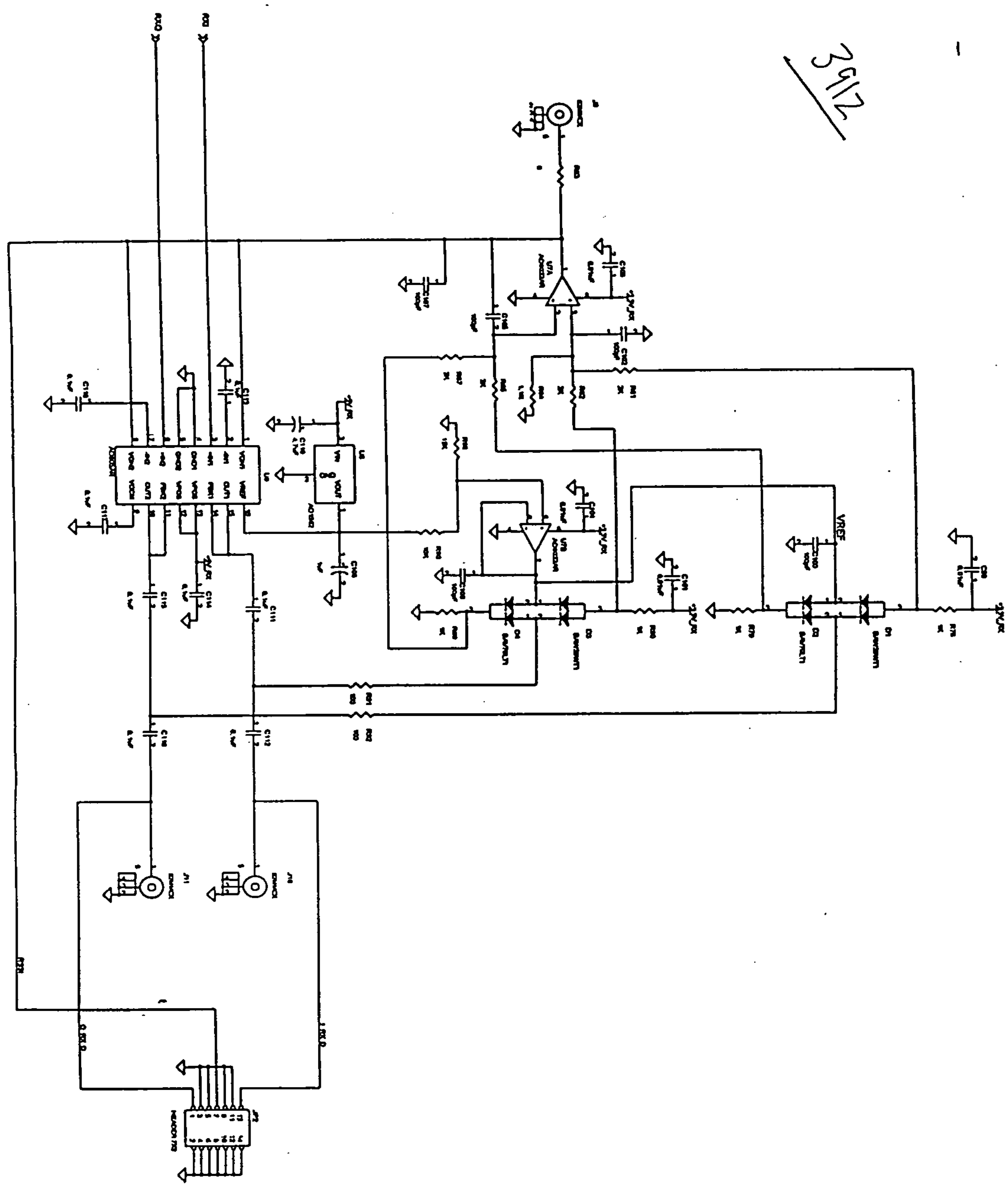


FIG. 5A

Bill Of Materials

Item	Quantity	Reference	Part	Part Number	Manufacturer
1	3	C3,C52,C55	4.7uF	T491A475K006AS	KEMET
2	26	C51,C54,C57,C58,C60,C61,	0.1uF	GRM39Y5V104Z016	Murata
		C67,C68,C69,C77,C79,C80,			
		C81,C83,C89,C90,C91,C111,			
		C112,C113,C114,C115,C116,			
		C117,C118,C119			
3	8	C56,C59,C78,C82,C99,C101,	0.01uF	GRM39X7R103K050	Murata
		C103,C104			
4	10	C62,C63,C66,C72,C73,C84,	1uF	GRM40Y5V105Z016	Murata
		C85,C88,C94,C95			
5	4	C64,C75,C86,C97	120pF	GRM39COG121J050	Murata
6	2	C87,C65	180pF	GRM39COG181J050	Murata
7	2	C70,C92	390pF	GRM39COG391J050	Murata
8	2	C71,C93	470pF	GRM39COG471J050	Murata
9	2	C96,C74	82pF	GRM39COG820J050	Murata
10	5	C100,C102,C105,C106,C107	100pF	GRM39COG101K050	Murata
11	1	C108	1uF		
	1	C110	4.7uF		
13	2	D3,D1	BAW56WT1	BAW56WT1	Motorola
14	2	D4,D2	BAV70LT1	BAV70LT1	Motorola
15	2	JP2,JP1	HEADER 7X2		
16	6	J1,J3,J5,J7,J10,J11	82MMCX	142-0701-231	Johnson
17	1	J9	82MMCX	82MMCX-50-0-1	Suhner
18	1	L1	BLM11A121S	BLM11A121S	Murata
19	2	L28,L23	2.2uH	LQG21N2R2K10	Murata
20	2	L24,L29	1uH	LQG21N1R0K10	Murata
21	2	L30,L25	680nH	LQG21NR68K10	Murata
22	2	L26,L31	1.8uH	LQG21N1R8K10	Murata
23	2	L27,L32	390nH	LQG21NR39K10	Murata
24	4	Q1,Q5,Q10,Q14	SD404CY	SD404CY	Calogic
25	4	Q2,Q4,Q12,Q13	BFM505	BFM505	Philips
26	4	Q3,Q7,Q11,Q16	SD213	SD213	Calogic
27	2	Q17,Q8	BFR520	BFR505	Philips
28	5	R19,R20,R21,R171,R173	0		
29	8	R23,R26,R34,R45,R52,R57,	33K	ERJ3GSYJ333	Panasonic
		R63,R74			
30	4	R24,R27,R53,R58	475	ERJ3EKF4750	Panasonic
31	6	R25,R28,R47,R54,R59,R76	402	ERJ3EKF4020	Panasonic
32	4	R29,R30,R55,R56	221	ERJ3EKF2210	Panasonic
33	2	R32,R61	200	ERJ3GSYJ201	Panasonic
34	2	R33,R62	33.2K	ERJ3GSYJ333	Panasonic
	4	R35,R46,R64,R75	68.1	ERJ3EKF68R1	Panasonic
	2	R36,R65	200	ERJ3EKF2000	Panasonic

FIG. 52A

37	2	R66,R37	49.9	ERJ3EKF49R9	Panasonic
8	6	R40,R68,R78,R79,R80,R89	1K	ERJ3EKF1001	Panasonic
39	2	R42,R71	62	ERJ3GSYJ620	Panasonic
40	2	R43,R72	162	ERJ3EKF6810	Panasonic
41	2	R44,R73	49.9	ERJ3EKF1001	Panasonic
42	2	R77,R48	33	ERJ3GSYJ330	Panasonic
43	4	R81,R82,R85,R87	2K	ERJ3EKF2001	Panasonic
44	1	R83	0	ERJGSY0R00	Panasonic
45	1	R84	1.1K	ERJ3EKF2001	Panasonic
46	1	R88	15K	ERJ3EKF1502	Panasonic
47	1	R90	10K	ERJ3EKF1002	Panasonic
48	2	R91,R92	100	ERJ3EKF1000	Panasonic
49	6	R164,R165,R166,R167,R168,	TBD		
		R169			
50	2	R170,R172	OPEN		
51	6	TP1,TP2,TP3,TP4,TP5,TP6	TP-105-01-00		
52	2	U42,U6	NC7S04M5		National Semiconductor
53	1	U7	AD8032AR	AD8032AR	Analog Devices
54	1	U8	AD1582	AD1582	Analog Devices
55	1	U9	AD605AR	AD605AR	Analog Devices
56	1	U43	TK11235AMTL	TK11235AMTL	Toko

FIG. 52B

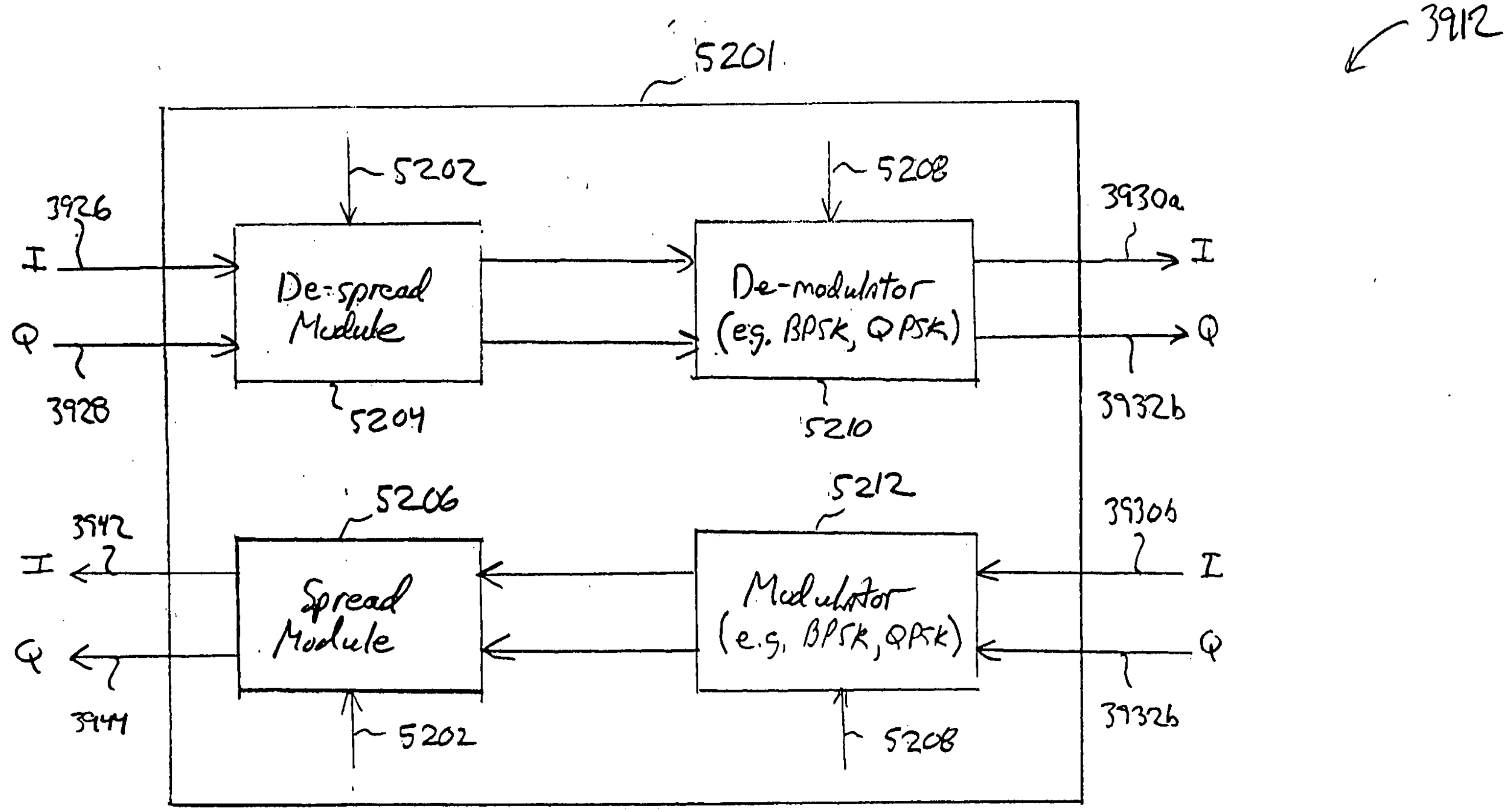
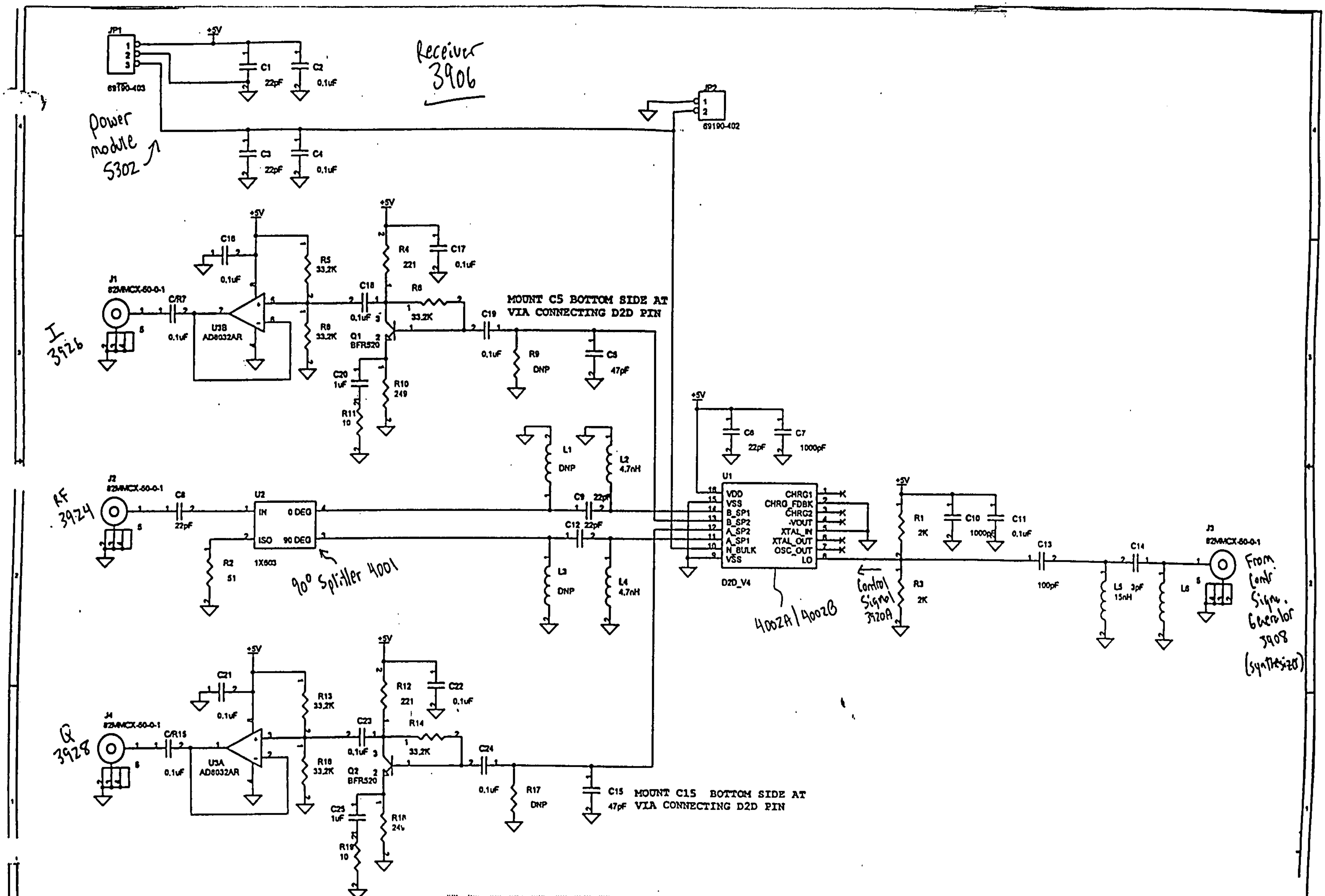


FIG. 52C

09632856 .080400

FIG. 53


Receiver 3906
Power module 5302
JP1
69190-403
+5V
C1
22pF
C2
0.1uF
C3
22pF
C4
0.1uF
JP2
69190-402
I 3926
J1
82MMCX-50-0-1
C/R7
0.1uF
C16
0.1uF
U3B
AD8032AR
R5
33.2K
R8
33.2K
R4
221
C17
0.1uF
C18
0.1uF
R6
33.2K
Q1
BFR520
C20
1uF
R11
10
R10
249
C19
0.1uF
R9
DNP
C5
47pF
MOUNT C5 BOTTOM SIDE AT
VIA CONNECTING D2D PIN
RF 3924
J2
82MMCX-50-0-1
C8
22pF
U2
IN
0 DEG
ISO
90 DEG
1X603
R2
51
90° Splitter 4001
L1
DNP
L2
4.7nH
C9
22pF
C12
22pF
L3
DNP
L4
4.7nH
C6
22pF
C7
1000pF
U1
VDD
VSS
B_SP1
B_SP2
A_SP2
A_SP1
N_BULK
VSS
CHRG1
CHRG_FDBK
CHRG2
-VOUT
XTAL_IN
XTAL_OUT
OSC_OUT
LO
D2D_V4
4002A/4002B
R1
2K
C10
1000pF
C11
0.1uF
R3
2K
Control Signal 3920A
C13
100pF
L5
15nH
C14
3pF
L6
J3
82MMCX-50-0-1
From Contr. Signal Generator 3908 (synthesizer)
Q 3928
J4
82MMCX-50-0-1
C/R15
0.1uF
C21
0.1uF
U3A
AD8032AR
R13
33.2K
R16
33.2K
R12
221
C22
0.1uF
C23
0.1uF
R14
33.2K
Q2
BFR520
C25
1uF
R19
10
C24
0.1uF
R17
DNP
C15
47pF
MOUNT C15 BOTTOM SIDE AT
VIA CONNECTING D2D PIN

Page1

Item	Quantity	Reference	Part	Part Number	Manufacturer
1	10	C/R7,C/R15,C16,C17,C18,	0.1uF	GRM39Y5V104Z016	Murata
		C19,C21,C22,C23,C24			
2	6	C1,C3,C6,C8,C9,C12	22pF	GRM39COG220J050	Murata
3	3	C2,C4,C11	0.1uF	GRM39X7R104K016	Murata
4	2	C5,C15	47pF	GRM39COG470J050	Murata
5	2	C10,C7	1000pF	GRM39X7R102K050	Murata
6	1	C13	100pF	GRM39X7R101J050	Murata
7	1	C14	3pF	GRM40COG030B50V	Murata
8	2	C20,C25	1uF	GRM40Y5V105Z016	Murata
9	1	JP1	69190-403	69190-403	BERG
10	1	JP2	69190-402	69190-402	BERG
11	4	J1,J2,J3,J4	82MMCX-50-0-1	82MMCX-50-0-1	Suhner
12	2	L3,L1	DNP	L	TOKO
13	2	L4,L2	4.7nH	LL1608-F4N7K	TOKO
14	1	L5	15nH	LL2012FH15NJ	TOKO
15	1	L6	DNP	DNP	TOKO
16	2	Q1,Q2	BFR520	BFR520	Philips
17	2	R1,R3	2K	ERJ3GSYJ202	Panasonic
18	1	R2	51	ERJ3GSYJ510	Panasonic
19	2	R4,R12	221	ERJ3EKF2210	Panasonic
20	6	R5,R6,R8,R13,R14,R16	33.2K	ERJ3EKF3322	Panasonic
21	2	R9,R17	DNP	ERJ3EKF1001	Panasonic
22	2	R10,R18	249	ERJ3EKF2490	Panasonic
23	2	R11,R19	10	ERJ3GSYJ100	Panasonic
24	1	U1	D2D_V4	D2D_V4	Parker Vision
25	1	U2	1X603	1X603	Anaren
26	1	U3	AD8032AR	AD8032AR	Analog Devices
27	1		BOARD	ST B500. LA1.001	V03.00

FIG. 54

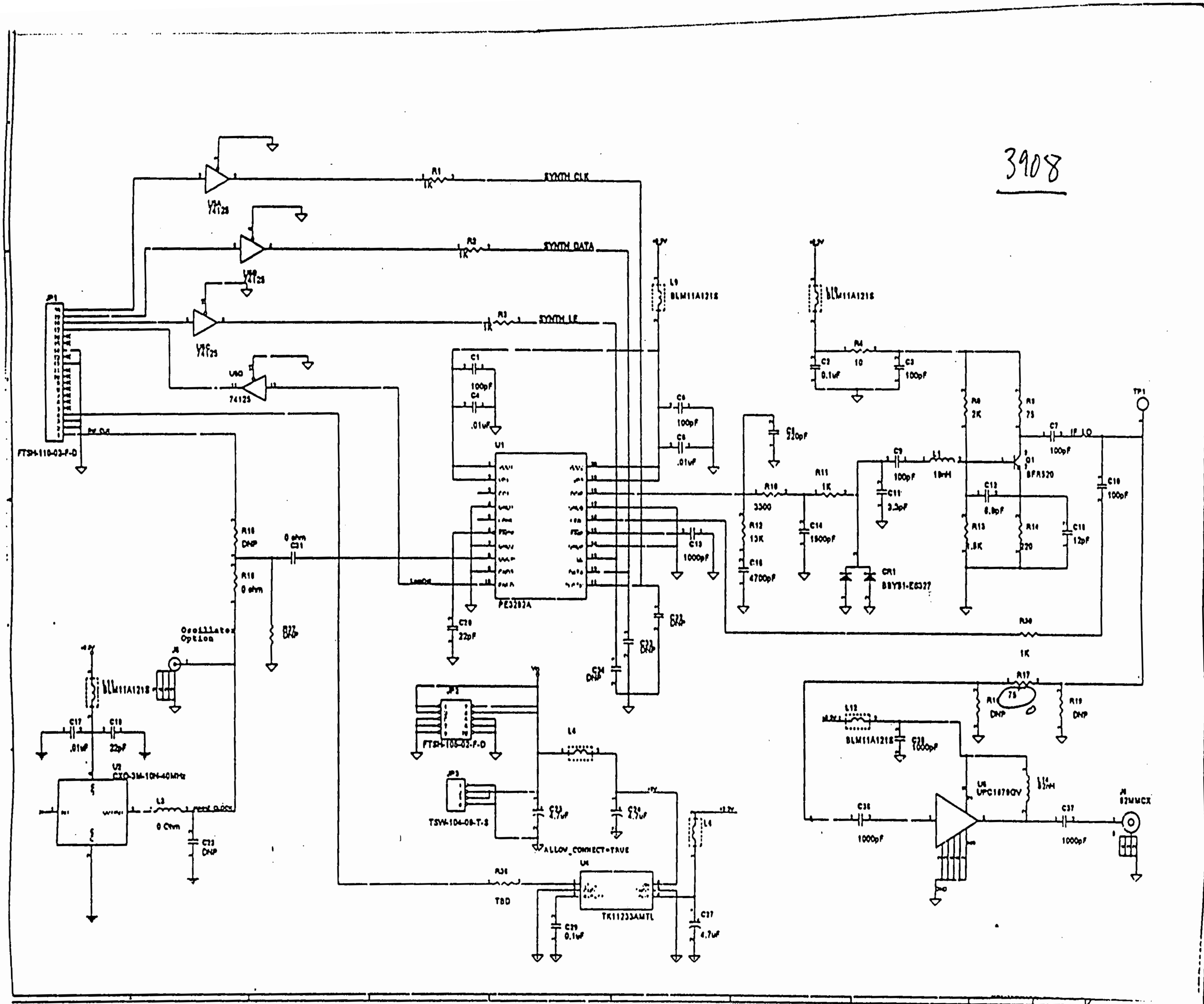

3908
SYNTH CLK
SYNTH DATA
SYNTH LE
74125
JP1
FTSH-110-03-F-D
U1
PE3282A
BLM11A121S
BFR520
BBY51-E6327
IF LO
TP1
Oscillator Option
U2
CXO-3M-10H-40MHz
FTSH-105-02-F-D
TSW-104-08-T-S
ALLOW_CONNECT=TRUE
TK11233AMTL
UPC1678GV

FIG. 55

Item	Qty	Reference	Part	Description	Part Number	Manufacturer
1	1	CR1	BBY51-E6327	Diode, Varactor	BBY51-E6327	Siemens
2	6	C1,C3,C5,C7,C9,C10	100pF	Capacitor, ceramic, 100pF, 10%, COG, 0603	GRM39COG101K050	Murata
3	2	C29,C2	0.1uF	Capacitor, ceramic, .1uF, 10%, X7R, 0603	GRM39X7R104K016AD	Murata
4	3	C4,C8,C17	.01uF	Capacitor, ceramic, .01uF, 10%, X7R, 0603	GRM39X7R103K050	Murata
5	1	C6	220pF	Capacitor, ceramic, 220pF, 5%, COG, 0603	GRM39COG221J025	Murata
6	1	C11	3.3pF	Capacitor, ceramic, 3.3pF, 5% , COG, 0603	GRM39COG3R3B100V	Murata
7	1	C12	6.8pF	Capacitor, ceramic, 6.8pF, +/-.25pF, COG, 0603	GRM39COG6R8C100V	Murata
8	4	C13,C35,C36,C37	1000pF	Capacitor, ceramic, 1000pF, 10%, X7R, 0603	GRM39X7R102K016	Murata
9	1	C14	1500pF	Capacitor, ceramic, 1500pF, 10%, X7R, 0603	GRM39X7R152K016	Murata
10	1	C15	12pF	Capacitor, ceramic, 12pF, 5%, COG, 0603	GRM39COG150J050	Murata 12pF
11	1	C16	4700pF	Capacitor, ceramic, 4700pF, 10%, 0603	GRM39X7R472K016	Murata
12	2	C20,C18	22pF	Capacitor, ceramic, 22pF, 10%, COG, 0603	GRM36COG220K050	Murata
13	4	C22,C32,C33,C34	DNP	Capacitor, ceramic, , , , 0603		Murata
14	3	C23,C24,C27	4.7uF	Capacitor, tantalum, 4.7uF, 10%, 3216	T491A475K006AS	Kemet
15	~~2~~ 3	R16,C31, R17	0 ohm	Resistor, zero ohm, 0603	ERJ3GSY0R00	Panasonic
16	1	JP1	FTSH-110-02-F-D	Header, dual row 10x2, .050x.050	FTSH-110-02-F-D	Samtec
17	1	JP2	FTSH-105-02-F-D	Header, dual row 5x2, .050x.050	FTSH-105-02-F-D	Samtec
18	1	JP3	TSW-104-08-T-S	Header, single row 4 pin, .100"	TSW-104-08-T-S	Berg
19	2	J5,J6	82MMCX	RF Connector	82MMCX-50-0-1	Suhner
20	1	L1	18nH	Inductor, 18nH, 10%, 0805	0805CS-180XJBC	Coilcraft
21	1	L3	0 Ohm	Zero Ohm Jumper	RM73ZIJT	KOA
22	6	L4,L6,L9,L10,L11,L12	BLM11A121S	Ferrite Bead, 0603	BLM11A121S	Murata
23	1	L14	82nH	Inductor, 82nH, 10%, 0805	LL2012-F82NK	Toko
24	1	Q1	BFR520	Transistor, NPN	BFR520	Philips
25	5	R1,R2,R3,R11,R30	1K	Resistor, 1K, 5%, 0603	ERJ3GSYJ102	Panasonic
26	1	R4	10	Resistor, 10 ohm, 5%, 0603	ERJ3GSYJ1R0	Panasonic
27	1	R8	2K	Resistor, 2K, 5%, 0603	ERJ3GSYJ202	Panasonic
28	~~2~~ 1	R9,~~R17~~	75	Resistor, 75 ohm, 5%, 0603	ERJ3GSYJ750	Panasonic
29	1	R10	3300	Resistor, 3.3K, 5%, 0603	ERJ3GSYJ332	Panasonic
30	1	R12	13K	Resistor, 13K, 5%, 0603	ERJ3GSYJ133	Panasonic
31	1	R13	1.5K	Resistor, 1.5K, 5%, 0603	ERJ3GSYJ152	Panasonic

FIG. 56A

32	1	R14	220	Resistor, 220 ohm, 5%, 0603	ERJ3GSYJ221	Panasonic
33	1	R15	DNP	Resistor, zero ohm, 0603	ERJ3GSY0R00	Panasonic
34	2	R18,R19	DNP	Resistor, 91 ohm, 5%, 0603	ERJ3GSYJ910	Panasonic
35	1	R36	TBD	Resistor, zero ohm, 0603	ERJ3GSY0R00	Panasonic
36	1	R37	DNP	Resistor, , , 0603		Panasonic
37	1	TP1	Test Point			
38	1	U1	PE3282A	IC, Synthesizer	PE3282A	Peregrine
39	1	U2	CXO-3M-10N-40MHz	Xtal Osc, 40MHz	CXO-3M-10N-40MHZ A/I	Statek
40	1	U4	TK11233AMTL	Voltage Regulator, 3.5V	TK11235BM	Toko
41	1	U5	74125	IC, BUFFER	MC74LCX125DT	Motorola
42	1	U6	UPC1678GV	IC, RF Amplifier	UPC1678GV	NEC
43	1		STB500.641.00B V02.00	BOARD		

FIG. 56B

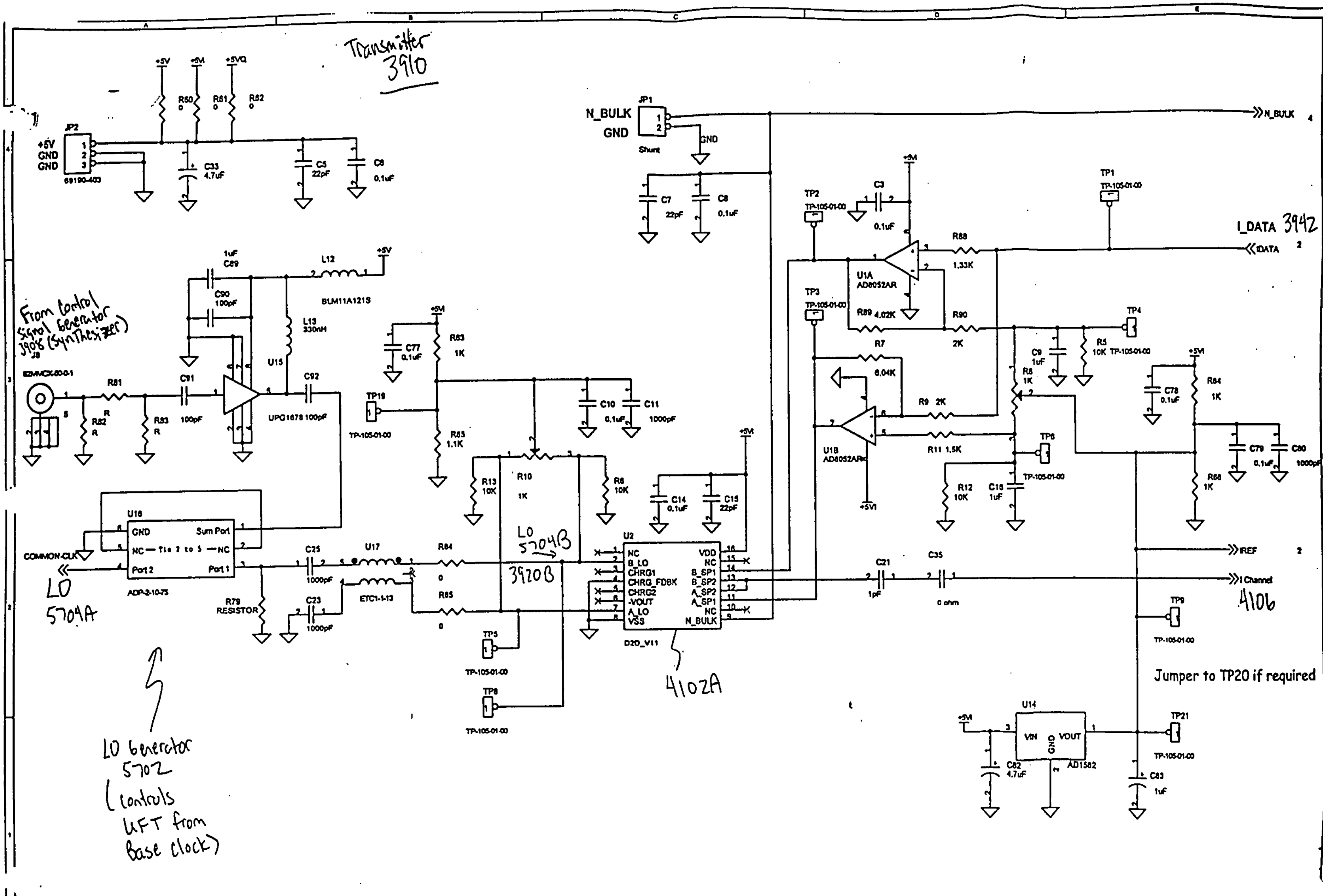


FIG. 57 72856_080400

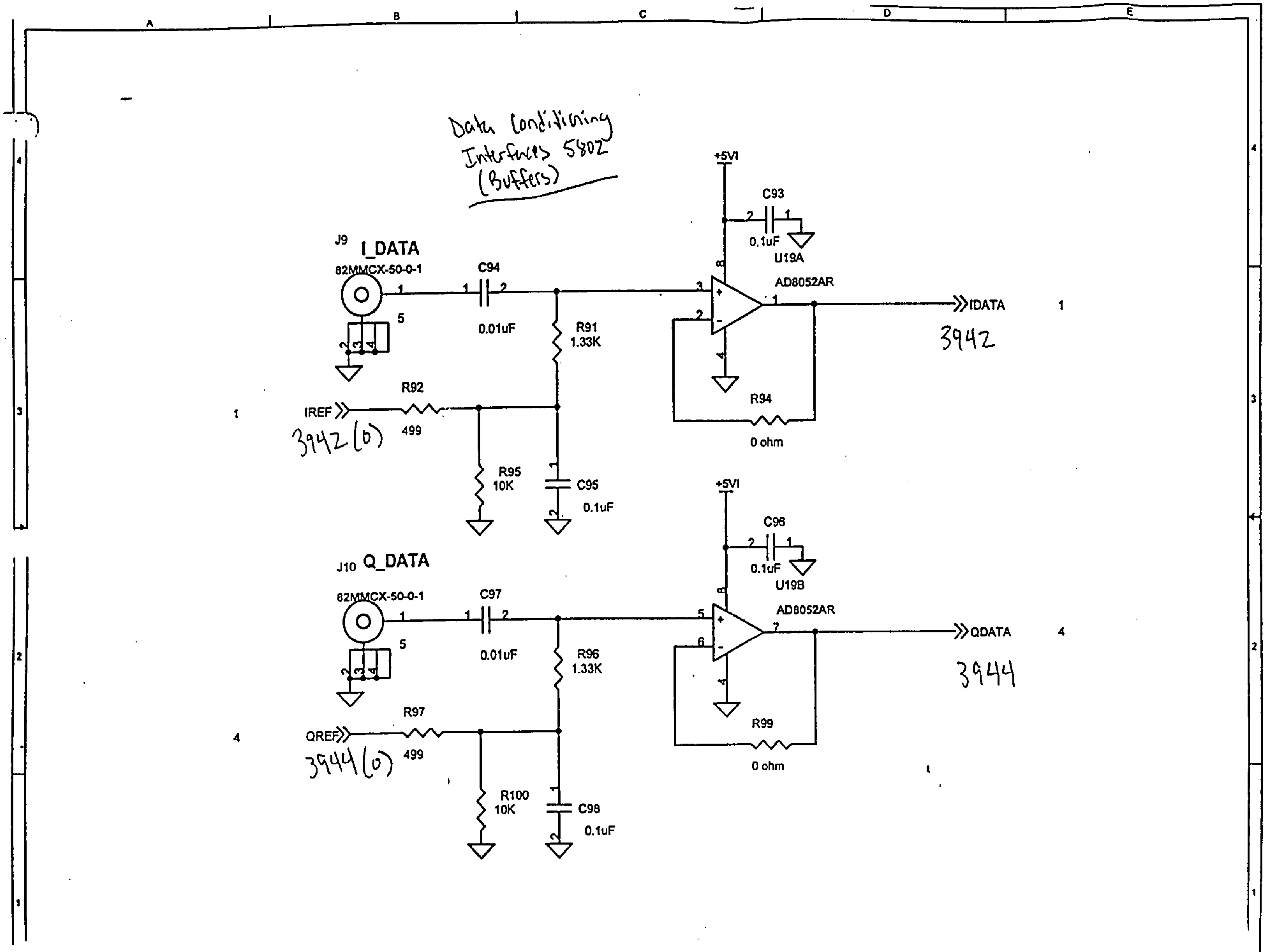

Data Conditioning Interfaces 5802 (Buffers)
J9
I_DATA
82MMCX-50-0-1
C94
0.01uF
R91
1.33K
+5VI
C93
0.1uF
U19A
AD8052AR
IDATA
3942
IREF
3942(0)
R92
499
R95
10K
C95
0.1uF
R94
0 ohm
J10
Q_DATA
82MMCX-50-0-1
C97
0.01uF
R96
1.33K
+5VI
C96
0.1uF
U19B
AD8052AR
QDATA
3944
QREF
3944(0)
R97
499
R100
10K
C98
0.1uF
R99
0 ohm

FIG. 58

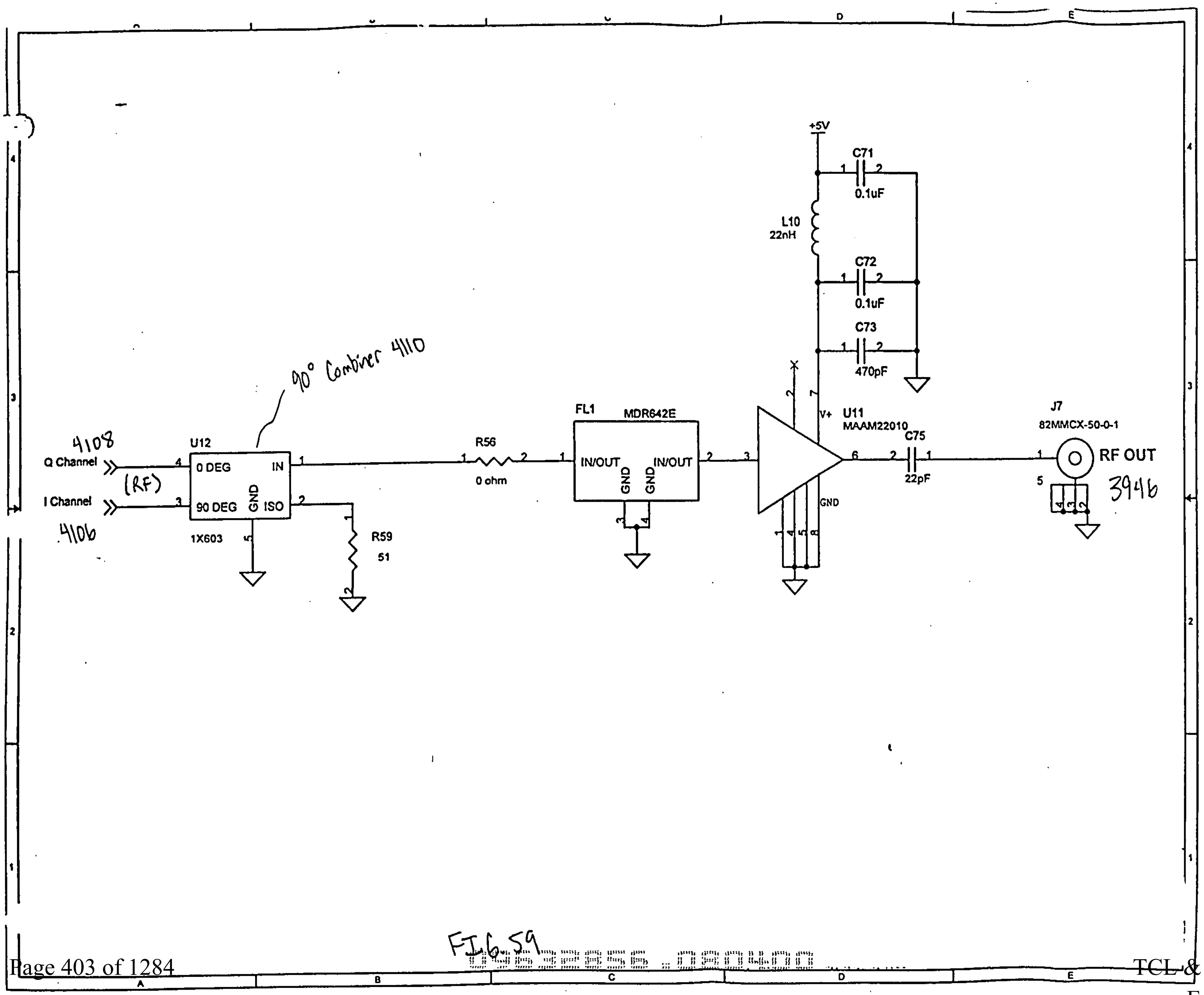

90° Combiner 4110
4108
Q Channel
(RF)
I Channel
4106
U12
0 DEG
IN
90 DEG
GND
ISO
1X603
R56
0 ohm
R59
51
FL1
MDR642E
IN/OUT
IN/OUT
GND
GND
+5V
C71
0.1uF
L10
22nH
C72
0.1uF
C73
470pF
V+
U11
MAAM22010
GND
C75
22pF
J7
82MMCX-50-0-1
RF OUT
3946

FIG. 59

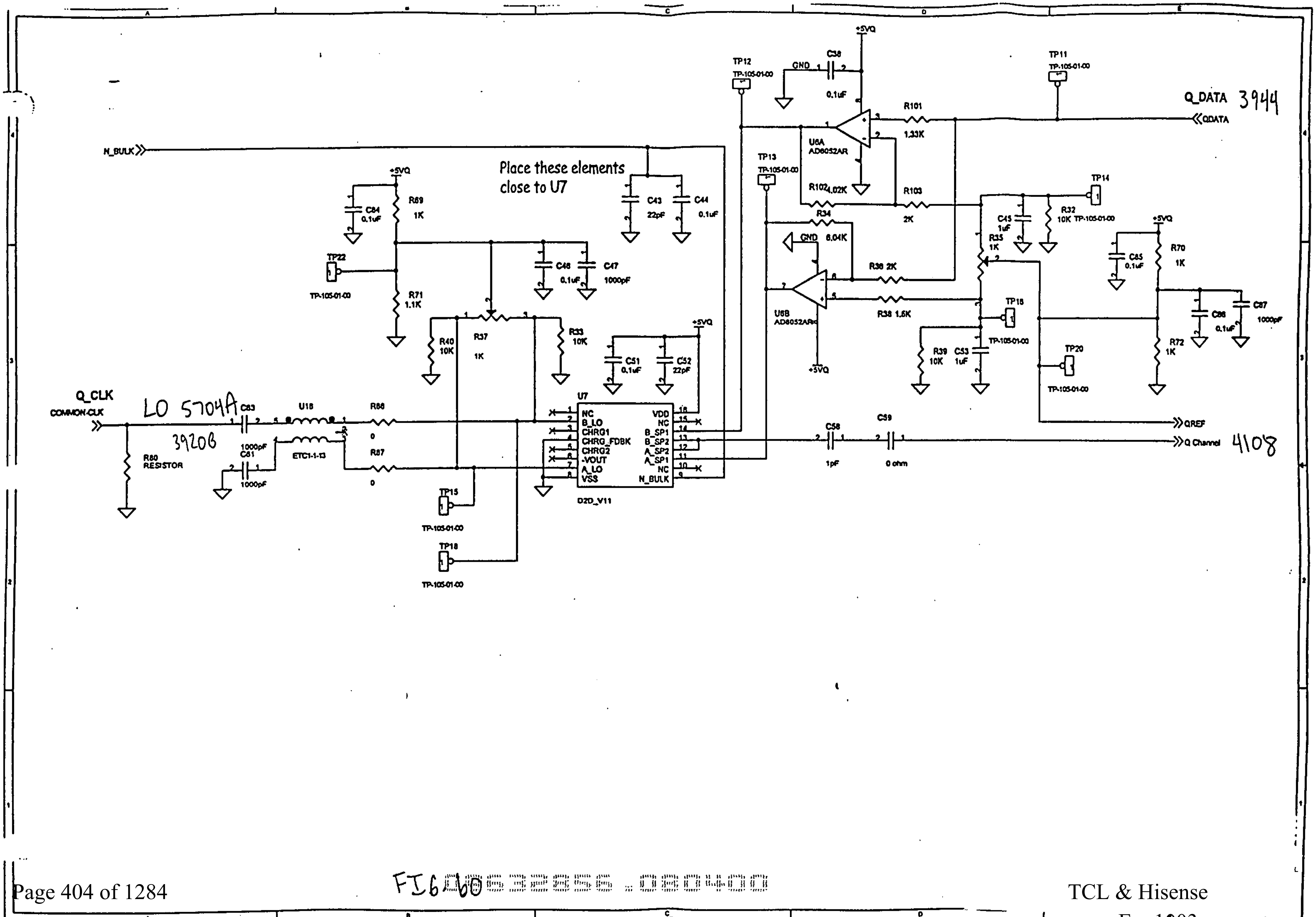


FIG 60 06 32856 .080400

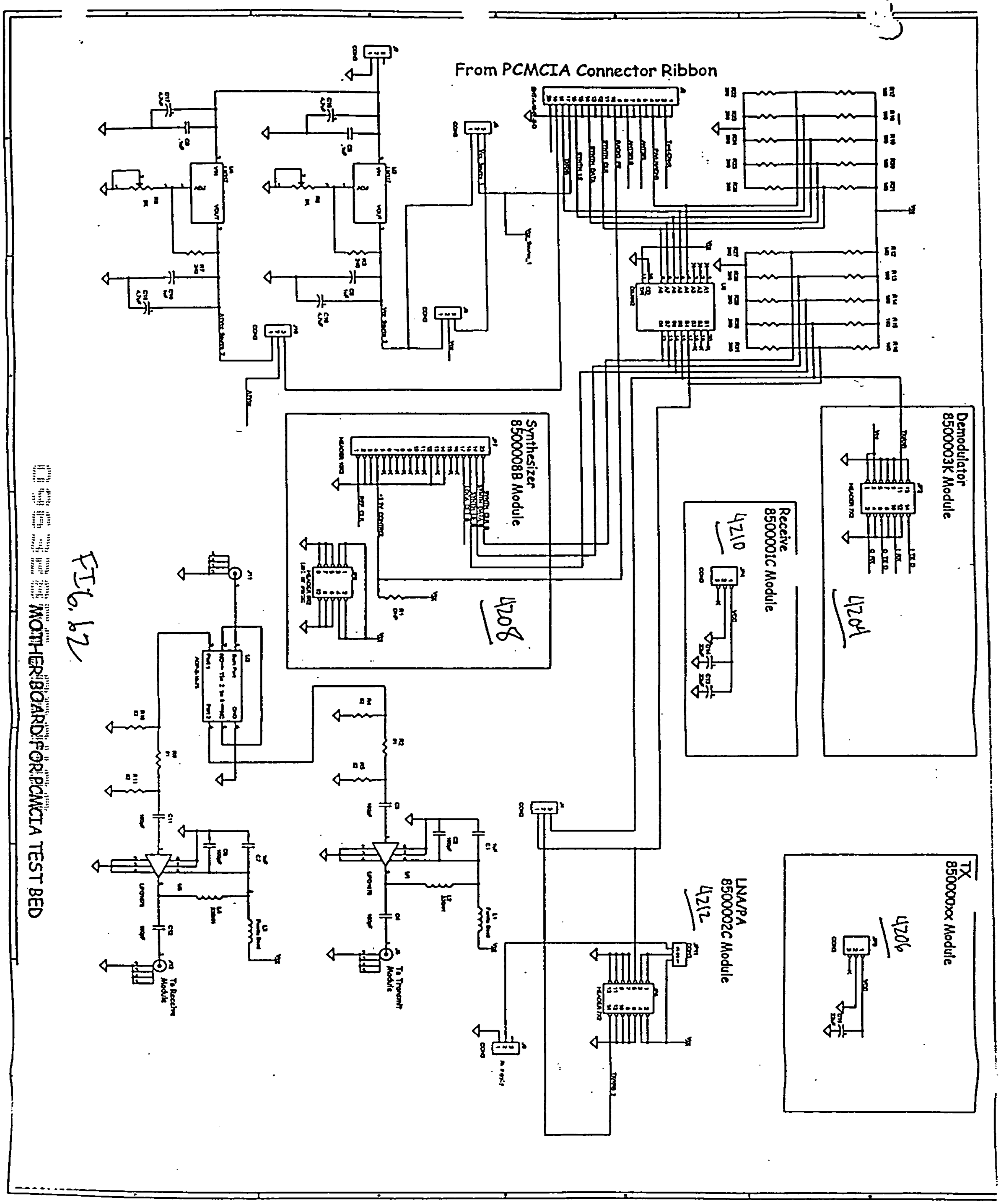
Bill Of Materials

Item	Quantity	Reference	Part	Part Number	Manufacturer
1	21	C3,C6,C8,C10,C14,C38,C44,	0.1uF	GRM39X7R104K016	Murata
		C46,C51,C71,C72,C77,C78,			
		C79,C84,C85,C86,C93,C95,			
		C96,C98			
2	6	C5,C7,C15,C43,C52,C75	22pF	GRM39COG220J050	Murata
3	5	C9,C16,C45,C53,C89	1uF	GRM40Y5V105Z016	Murata
4	8	C11,C23,C25,C47,C61,C63,	1000pF	GRM39X7R102K050	Murata
		C80,C87			
5	2	C58,C21	1pF	GRM39COG010B50V	Murata
6	2	C82,C33	4.7uF	T491A475K006AS	KEMET
7	2	C59,C35	0 ohm	GRM39COGxxxx50V	Murata
8	1	C73	470pF	GRM39COG471J050	Murata
9	1	C83	1uF	T491A105M016AS	Kemet
10	3	C90,C91,C92	100pF	ECU-V1H101JCV	
11	2	C94,C97	0.01uF	GRM39X7R103K016	Murata
12	1	FL1	MDR642E	MDR642E	Soshin
13	1	JP1	Shunt	69190-402	BERG
14	1	JP2	69190-403	69190-403	BERG
15	4	J7,J8,J9,J10	82MMCX-50-0-1	82MMCX-50-0-1	Suhner
16	1	L10	22nH	LL1608-F22NK	Coilcraft
17	1	L12	BLM11A121S	BLM11A121S	Murata
18	1	L13	330nH	LL2012-FR33K	
19	10	R5,R6,R12,R13,R32,R33,	10K	ERJ3EKF1002	Panasonic
		R39,R40,R95,R100			
20	2	R34,R7	6.04K	ERJ3EKF6041	Panasonic
21	4	R8,R10,R35,R37	1K	3224W-1-102	Bourns
22	4	R9,R36,R90,R103	2K	ERJ3EKF2001	Panasonic
23	2	R38,R11	1.5K	ERJ3EKF1501	Panasonic
24	3	R56,R94,R99	0 ohm	ERJ3GSY0R00	Panasonic
25	1	R59	51	ERJ3GSYJ510	Panasonic
26	7	R60,R61,R62,R84,R85,R86,	0	ERJ3GSY0R00	Panasonic
		R87			
27	6	R63,R64,R66,R69,R70,R72	1K	ERJ3EKF1001	Panasonic
28	2	R71,R65	1.1K	ERJ3EKF1101	Panasonic
29	2	R80,R79	RESISTOR		
30	3	R81,R82,R83	R		
31	4	R88,R91,R96,R101	1.33K	ERJ3EKF1331	Panasonic
32	2	R102,R89	4.02K	ERJ3EKF4021	Panasonic
33	2	R92,R97	499	ERJ3EKF4990	Panasonic
34	19	TP1,TP2,TP3,TP4,TP5,TP6,	TP-105-01-00		

FIG. 61A

		TP8,TP9,TP11,TP12,TP13,			
		TP14,TP15,TP16,TP18,TP19,			
		TP20,TP21,TP22			
35	3	U1,U6,U19	AD8052AR	AD8052AR	Analog Devices
36	2	U7,U2	D2D_V11	D2D_V11	Parker Vision
37	1	U11	MAAM22010	MAAM22010	MACOM
38	1	U12	1X603	1X603	Anaren
39	1	U14	AD1582	AD1582	Analog Devices
40	1	U15	UPG1678	UPG1678GV	NEC
41	1	U16	ADP-2-10-75	ADP-2-10-75	Mini-Circuits
42	1		BOARD	B500.641.021	V05.10

FIG. 61B



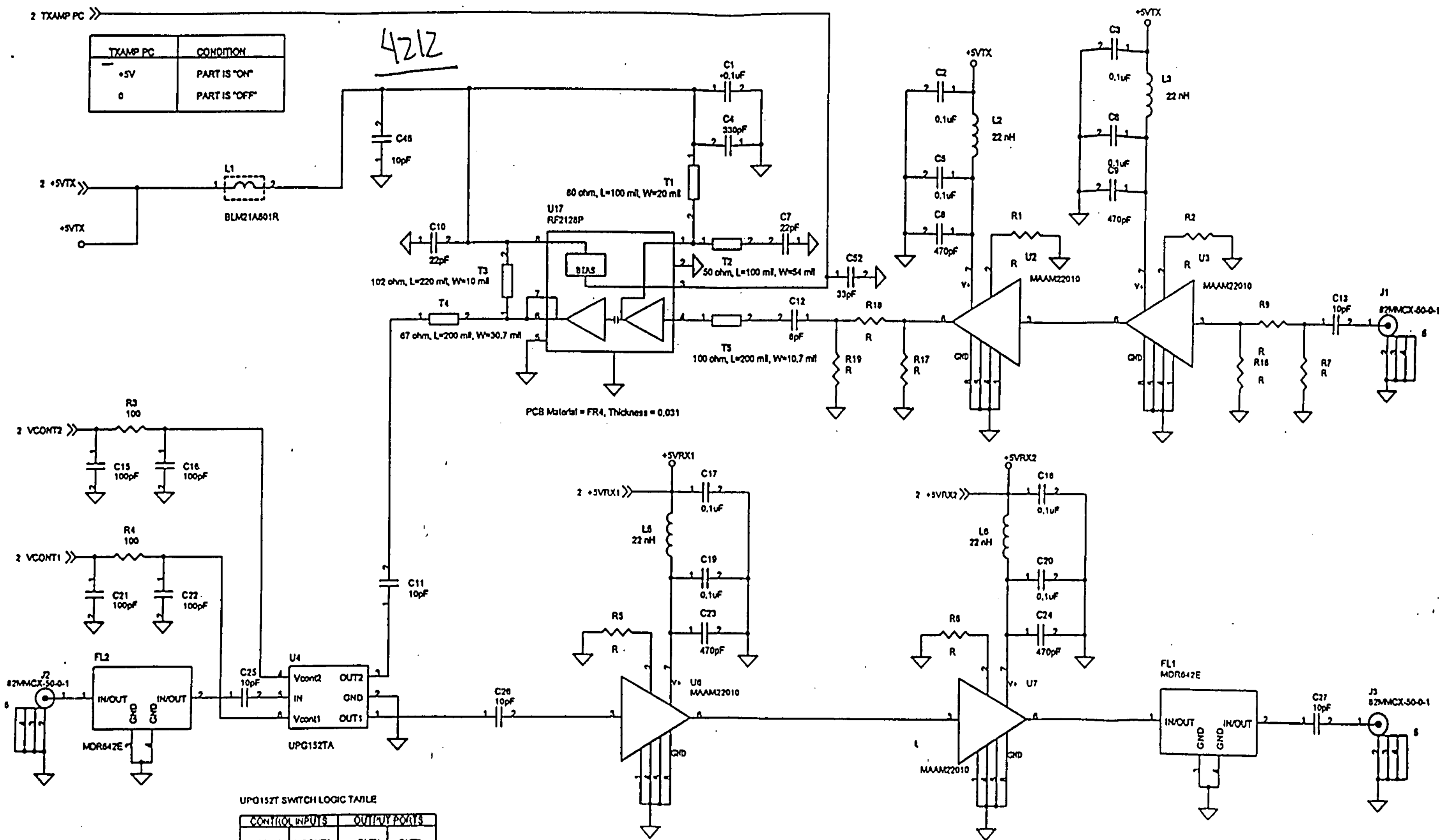
From PCMCIA Connector Ribbon
Synthesizer 8500008B Module
4208
Demodulator 8500003K Module
4204
Receive 8500001C Module
4210
LNA/PA 8500002C Module
4212
TX 85000xx Module
4206
To Receive Module
To Transmit Module
FIG. 62
MOTHER BOARD FOR PCMCIA TEST BED

Bill Of Materials

Item	Qty	Reference	Part	Description	Part Number	Vendor
1	4	C1,C6,C7,C10	1uF	Cap, 1uF, +80-20%, 0805	GRM40Y5V105Z016AD	Murata
2	6	C2,C3,C4,C8,C11,C12	100pF	Cap, 100pF, 5%, COG, 0603	ECU-V1H101JCV	Panasonic
3	2	C5,C9	.1uF	Cap, .1uF, +80-20%, Y5V, 0603		Murata
4	3	C13,C14,C19	22uF	Cap, Tant, 22uF, 20%, 20V	T491D226M020AS	Kemet
5	4	C15,C16,C17,C18	4.7uF	Cap, Tant, 4.7uF, 20%, 20V	T491C475M020AS	Kemet
6	2	JP2,JP6	HEADER 7X2	Receptacle, 7x2pin, .050	SFMC-107-L1-S-D	Samtek
7	9	JP4, J4, J5, J6, J7, JP9, J9, J10, JP11	CON3	Header, 3pin, .100"	69190-403	Berg
8	1	JP7	HEADER 10X2	Receptacle, 10x2pin, .050	SFMC-110-L1-S-D	Samtek
9	1	JP8	HEADER 5X2	Receptacle, 5x2pin, .050	SFMC-105-L1-S-D	Samtek
10	1	J2	EHT-1-10-01-S-D	Header, ribbon, 10x2pin, 2mm	EHT-1-10-01-S-D	Samtek
11	3	J8,J11,J12	82MMCX-50-0-1	Connector, RF	82MMCX-50-0-1	Suhner
12	2	L3,L1	Ferrite Bead	Ferrite Bead, 0805	BLM21A121S	Murata
13	2	L4,L2	330nH	Ind, 330nH, 10%, 0805	LL2012-FR33K	Toko
14	1	R1	DNP	Res, 0603		Panasonic
15	2	R9,R2	91	Res, 91 Ohm, 5%, 0603	ERJ-3GSYJ910	Panasonic
16	2	R7,R3	240	Res, 240 Ohm, 5%, 0603	ERJ-3GSYJ241	Panasonic
17	4	R4,R5,R10,R11	82	Res, 82 Ohm, 5%, 0603	ERJ-3GSYJ820	Panasonic
18	2	R8,R6	5K	Var Res, 5K, 10%	3296W001502	Bourns
19	10	R12, R13, R14, R15, R16, R17, R18, R19, R20, R21	180	Res, 180 Ohm, 5%, 0603	ERJ-3GSYJ181	Panasonic
20	10	R22, R23, R24, R25, R26, R27, R28, R29, R30, R31	390	Res, 390 Ohm, 5%, 0603	ERJ-3GSYJ391	Panasonic
21	2	U5,U1	UPG1678	IC, RF Buffer	UPG1678GV	NEC
22	2	U4,U2	LM317	IC, Voltage Regulator	LM317T	National
23	1	U3	ADP-2-10-75	RF Splitter	ADP-2-10-75	MiniCircuits
24	1	U6	DS3862	IC, Buffer	DS3862WM	National
25	1			BOARD	STB500.641.023	VOL 01

FIG. 63

FIG. 64

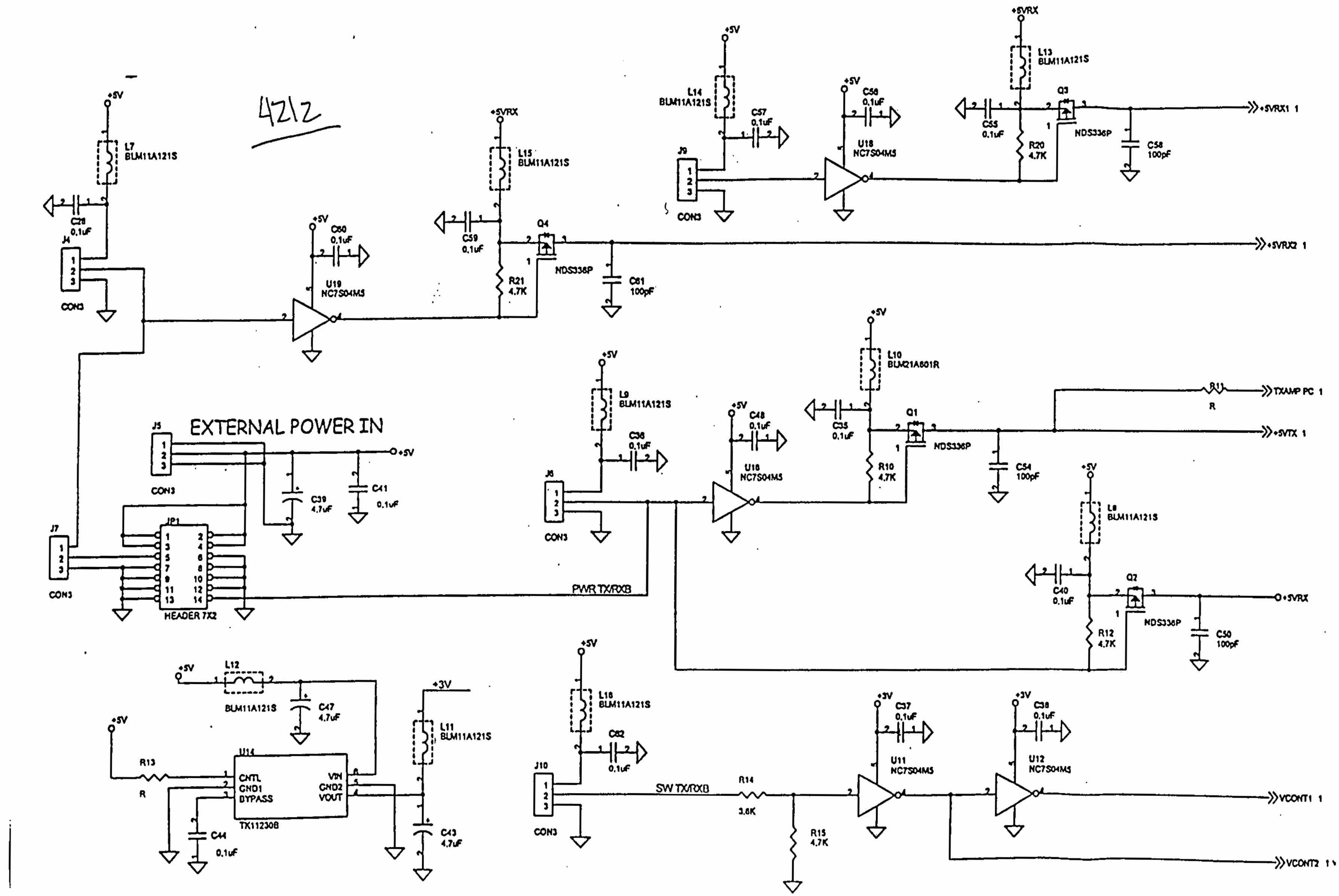


TXAMP PC	CONDITION
+5V	PART IS "ON"
0	PART IS "OFF"

UPG152T SWITCH LOGIC TABLE

CONTROL INPUTS		OUTPUT PORTS	
VCONT1	VCONT2	OUT1	OUT2
0	0	OFF	OFF
0	+3	ON	OFF
+3	0	OFF	ON
+3	+3	OFF	OFF

FIG. 65


4212
EXTERNAL POWER IN
+5V
+5VRX
+3V
L7
BLM11A121S
L15
BLM11A121S
L14
BLM11A121S
L13
BLM11A121S
L10
BLM21A601R
L9
BLM11A121S
L8
BLM11A121S
L12
BLM11A121S
L11
BLM11A121S
L16
BLM11A121S
C28
0.1uF
C60
0.1uF
C59
0.1uF
C61
100pF
C57
0.1uF
C56
0.1uF
C55
0.1uF
C58
100pF
C48
0.1uF
C35
0.1uF
C36
0.1uF
C54
100pF
C40
0.1uF
C50
100pF
C39
4.7uF
C41
0.1uF
C47
4.7uF
C44
0.1uF
C43
4.7uF
C62
0.1uF
C37
0.1uF
C38
0.1uF
U19
NC7S04M5
U18
NC7S04M5
U16
NC7S04M5
U11
NC7S04M5
U12
NC7S04M5
Q4
Q3
Q1
Q2
NDS336P
R21
4.7K
R20
4.7K
R10
4.7K
R12
4.7K
R11
R
R13
R
R14
3.6K
R15
4.7K
J4
J9
J5
J6
J7
J10
CON3
JP1
HEADER 7X2
PWR TX/RXB
SW TX/RXB
U14
CNTL
GND1
BYPASS
VIN
GND2
VOUT
TK11230B
+5VRX1 1
+5VRX2 1
TXAMP PC 1
+5VTX 1
+5VRX
VCONT1 1
VCONT2 1

S

Bill Of Materials

Item	Qty	Reference	Part	Manufacturer	Part Description	Part Number
1	24	C1,C2,C3,C5,C6,C17,C18,	0.1uF	Murata	.1uF,0603,X7R,20%,16V	GRM39X7R104MO16
		C19,C20,C28,C35,C36,C37,				
		C38,C40,C41,C44,C48,C55,				
		C56,C57,C59,C60,C62				
2	1	C4	330pF	Murata	330pF,0603,COG,10%,50	GRM39COG331K050
3	2	C10,C7	22pF	Murata	22pF,0603,COG,10%,50	GRM39COG220K050
4	4	C8,C9,C23,C24	470pF	Murata	470pF,0603,COG,10%,50	GRM39COG471K050
5	6	C11,C13,C25,C26,C27,C46	10pF	Murata	10pF,0603,COG,10%,50	GRM39COG100K050
6	1	C12	8pF	Murata	8pF,0603,COG,10%,50	GRM39COG080K050
7	8	C15,C16,C21,C22,C50,C54,	100pF	Murata	100pF,0603,COG,10%,50	GRM39COG101K050
		C58,C61				
8	3	C39,C43,C47	4.7uF	Panasonic	4.7 uF tantalum, 16V	ECS-T1CY475R
9	1	C52	33pF	Murata	330pF,0603,COG,10%,50	GRM39COG330K050
10	2	FL1,FL2	MDR642E	Soshin	2.4-2.5GHz BPF	MDR642E
11	1	JP1	HEADER 7X2	Samtec	Dual Row, 7 pins per row	FTSH-107-01-F-D
12	3	J1,J2,J3	82MMCX-50-0-1	Suhner	RF Connector	82MMCX-50-0-1
13	6	J4,J5,J6,J7,J9,J10	CON3	Berg	3 pin header w retentive leg	69190-403H
14	2	L10,L1	BLM21A601R	Murata	600 ohms@100MHz, 500 mA Ferrite Bead	BLM21A601R
15	4	L2,L3,L5,L6	22 nH	Coilcraft	22nH, 0805CS (2012), 5%	0805CS-220X-BC
16	9	L7,L8,L9,L11,L12,L13,L14,	BLM11A121S	Murata	RF Bead	BLM11A121S
		L15,L16				
17	4	Q1,Q2,Q3,Q4	NDS336P	National	P-Channel FET	NDS336P
18	12	R1,R2,R5,R6,R7,R9,R11,	R	Panasonic		
		R13,R16,R17,R18,R19				
19	2	R3,R4	100	Panasonic	0603, 100, 5%, 1/16 W	ERJ-3GSY-J-101
20	5	R10,R12,R15,R20,R21	4.7K	Panasonic	0603, 4.7K, 5%, 1/16 W	ERJ-3GSY-J-472
21	1	R14	3.6K	Panasonic	0603, 3.6K, 5%, 1/16 W	ERJ-3GSY-J-362
22	1	T1	80 ohm, L=100 mil, W=20 mil		80 ohm, L=100 mil, W=20 mil	
23	1	T2	50 ohm, L=100 mil, W=54 mil		50 ohm, L=100 mil, W=54 mil	
24	1	T3	102 ohm, L=220 mil, W=10 mil		102 ohm, L=220 mil, W=10 mil	
25	1	T4	67 ohm, L=200 mil, W=30.7 mil		67 ohm, L=200 mil, W=30.7 mil	
26	1	T5	100 ohm, L=200 mil, W=10.7 mil		100 ohm, L=200 mil, W=10.7 mil	
27	4	U2,U3,U6,U7	MAAM22010	MACOM	2.4-2.5 GHz LNA	MAAM22010
28	1	U4	UPG152TA	NEC	RF Switch	UPG152TA
29	5	U11,U12,U16,U18,U19	NC7S04M5	National	Inverter	NC7S04M5
30	1	U14	TK11230B	TOKO	Voltage Regulator	TK11230B
31	1	U17	RF2128P	RFMD	Medium Power Linear Amplifier	RF2128P

FIG. 66

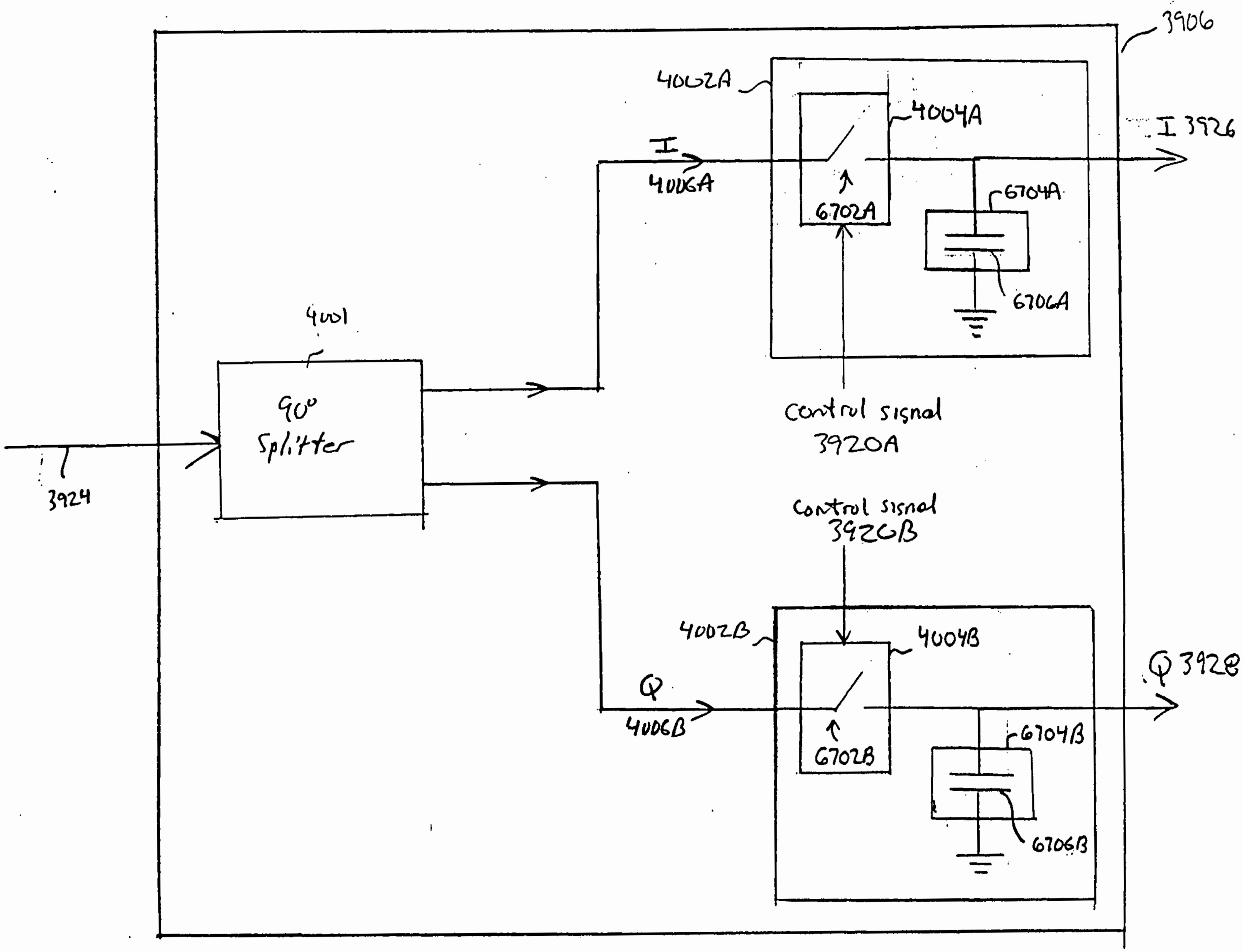

3906
4002A
4004A
I 3926
I
4006A
6702A
6704A
6706A
4001
90° Splitter
3924
Control signal
3920A
Control signal
3920B
4002B
4004B
Q 3928
Q
4006B
6702B
6704B
6706B

FIG. 67A

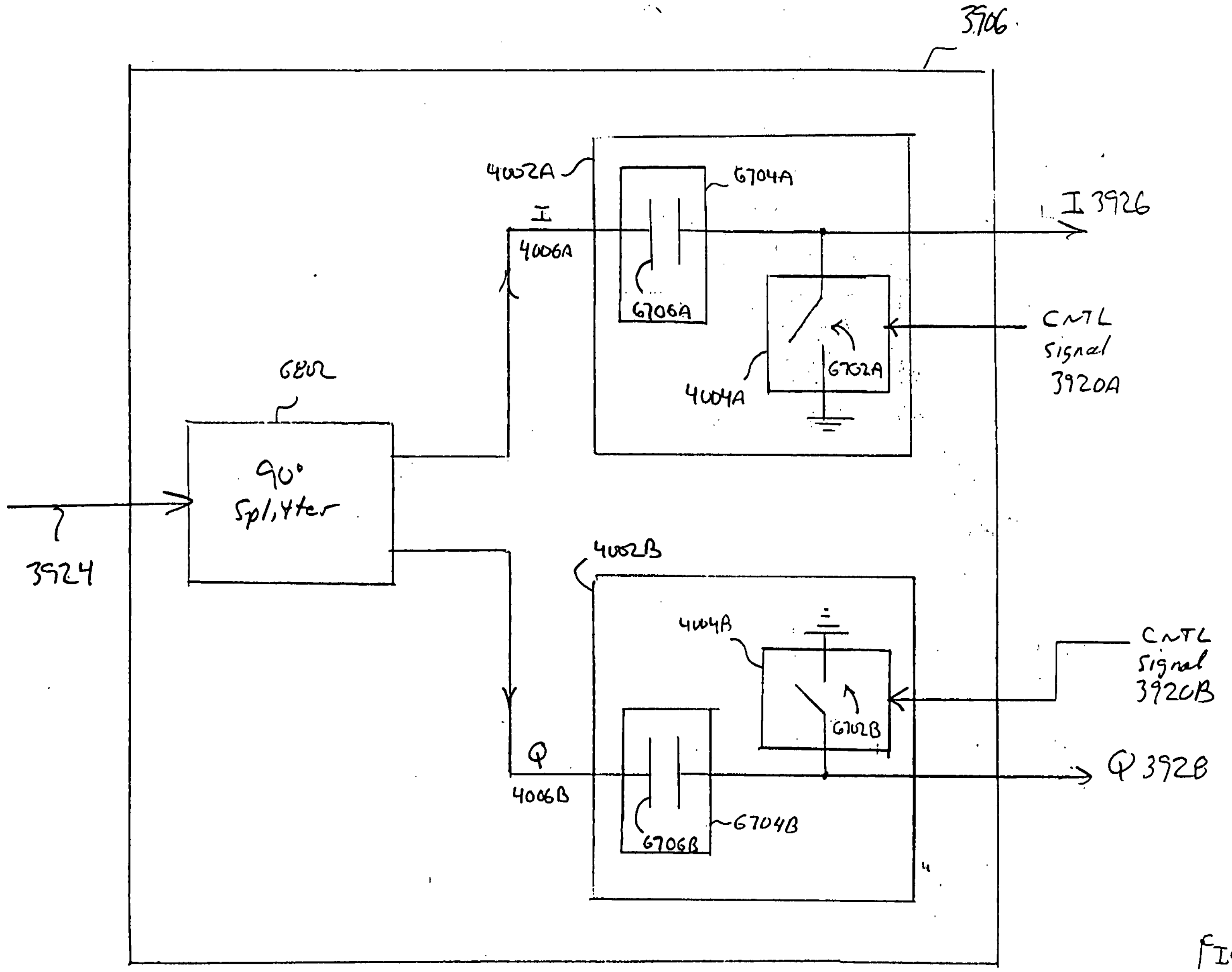

3906
4002A
6704A
I
4006A
6706A
I 3926
CNTL
Signal
3920A
6702A
4004A
6802
90°
Splitter
3924
4002B
4004B
CNTL
Signal
3920B
6702B
Q
Q 3928
4006B
6706B
6704B

FIG. 67B

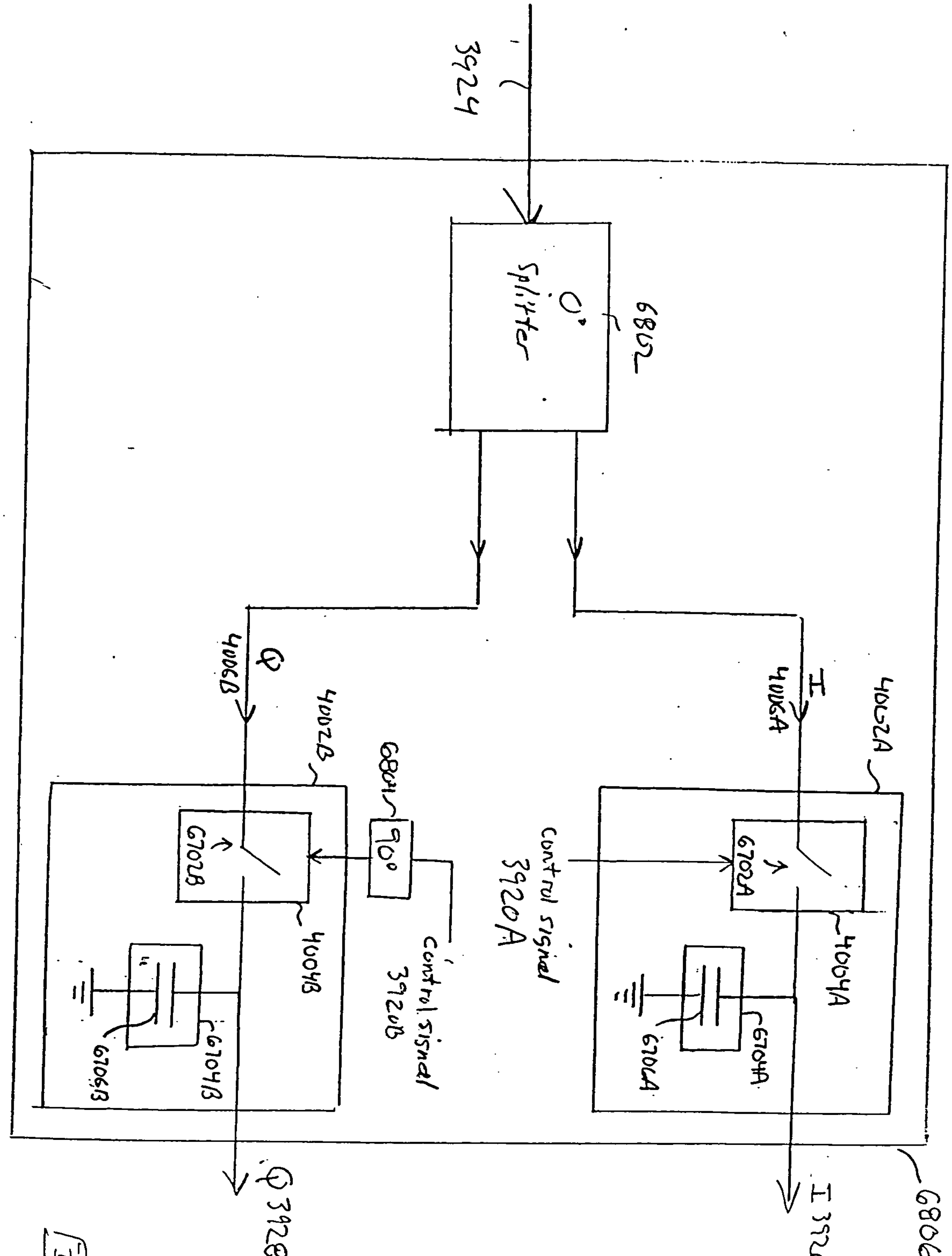

3924
0° Splitter
6802
Q
4006B
I
4006A
4002B
4002A
6804
90°
6702B
6702A
control signal 3920A
control signal 3920B
4004B
4004A
6704B
6706B
6704A
6706A
Q 3928
I 3926
6806

FIG. 68A

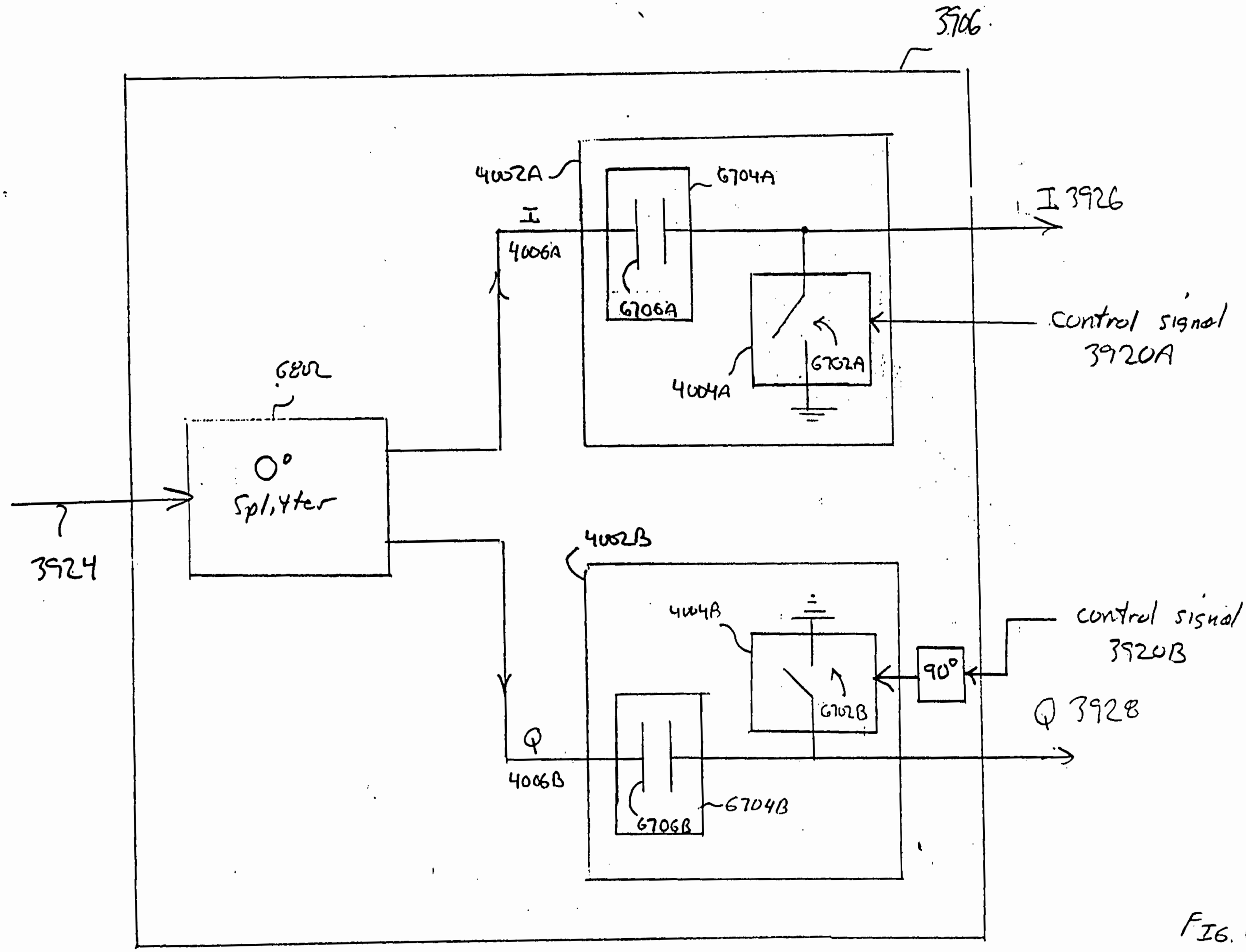

3906
4002A
6704A
I
I 3926
4006A
6706A
control signal
3920A
6702A
4004A
6802
0°
Splitter
3924
4002B
4004B
control signal
3920B
90°
6702B
Q 3928
Q
4006B
6706B
6704B

FIG. 68B

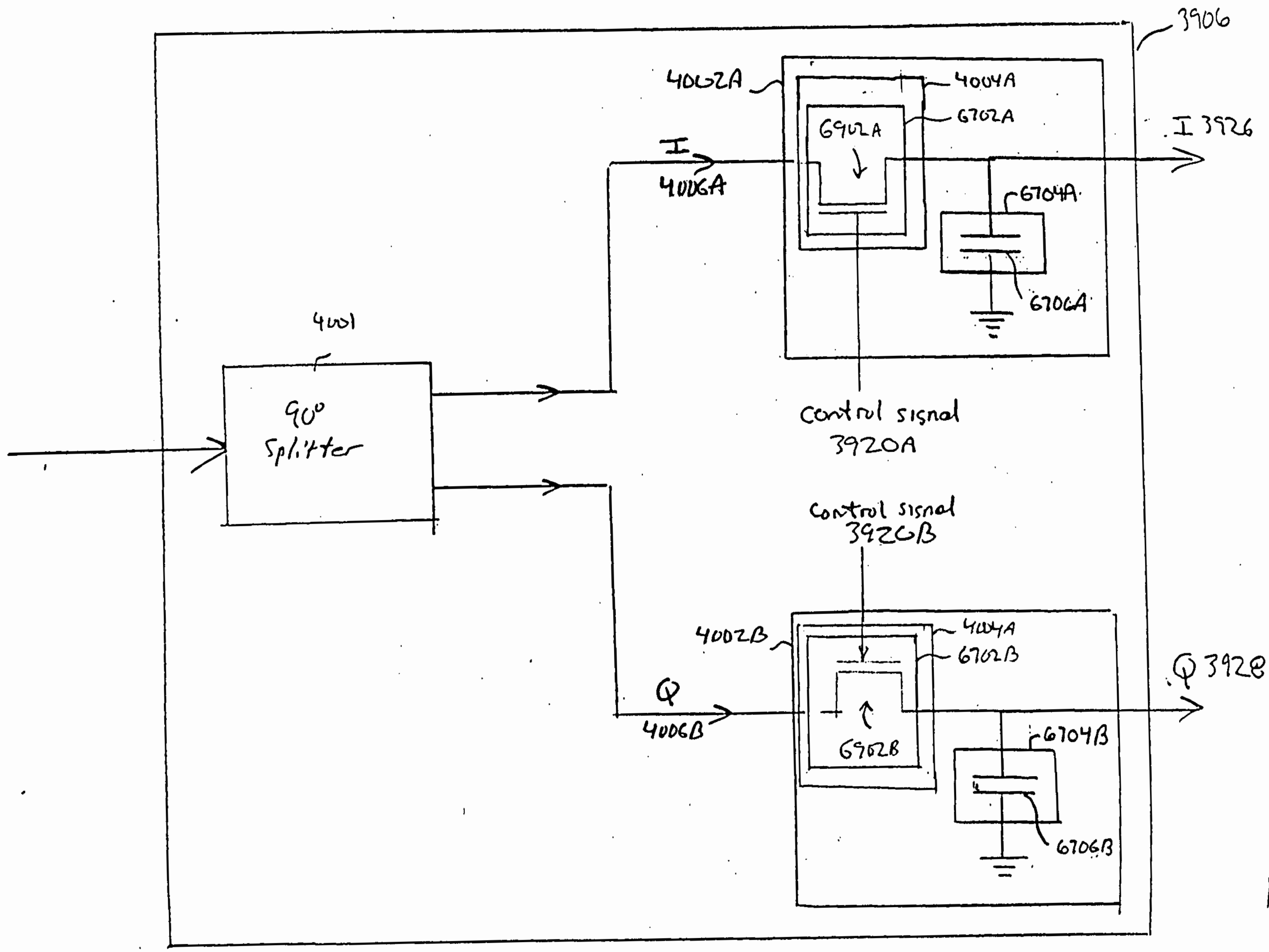


FIG. 69A

09632856 .080400

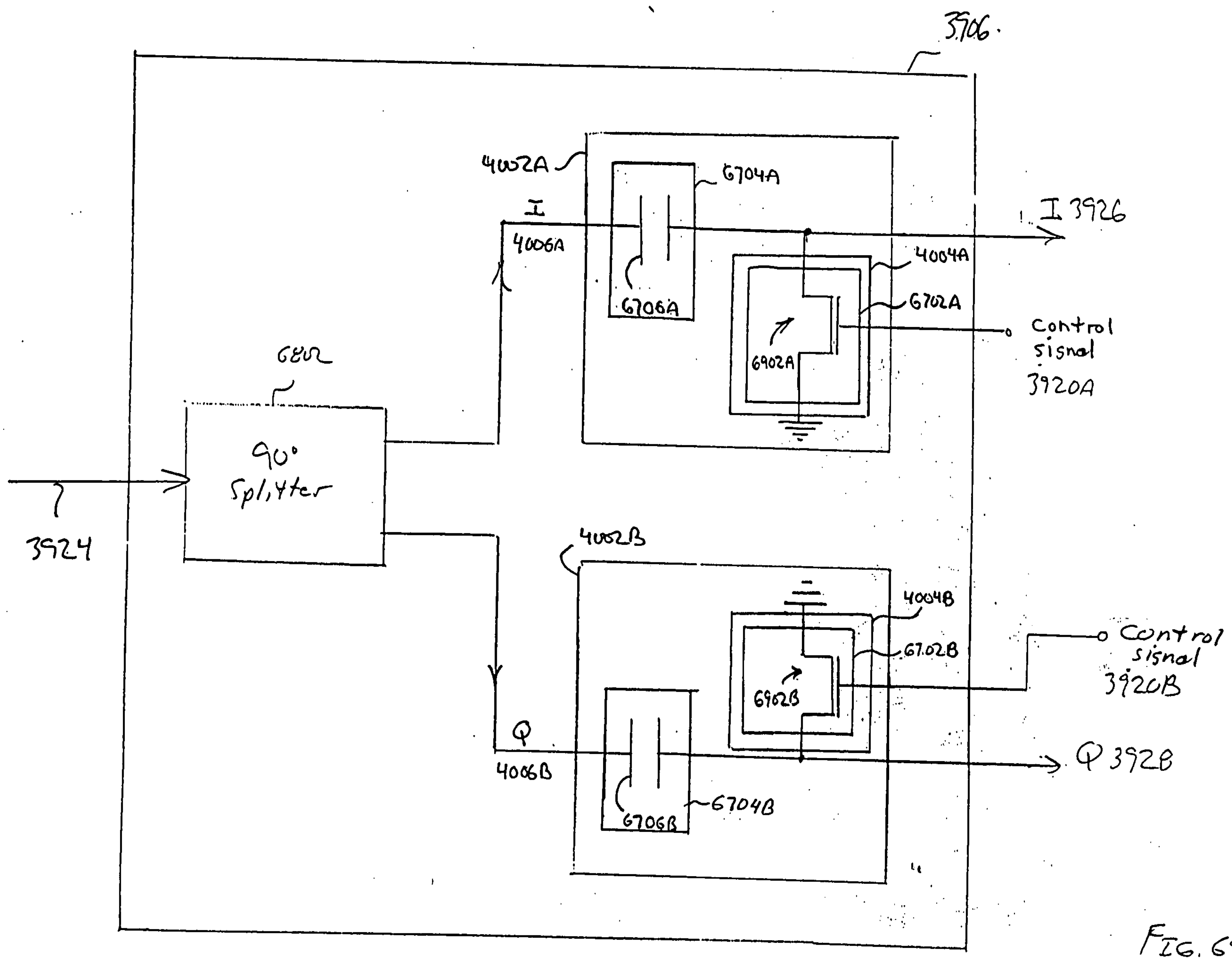


FIG. 69B

09632856 .080400

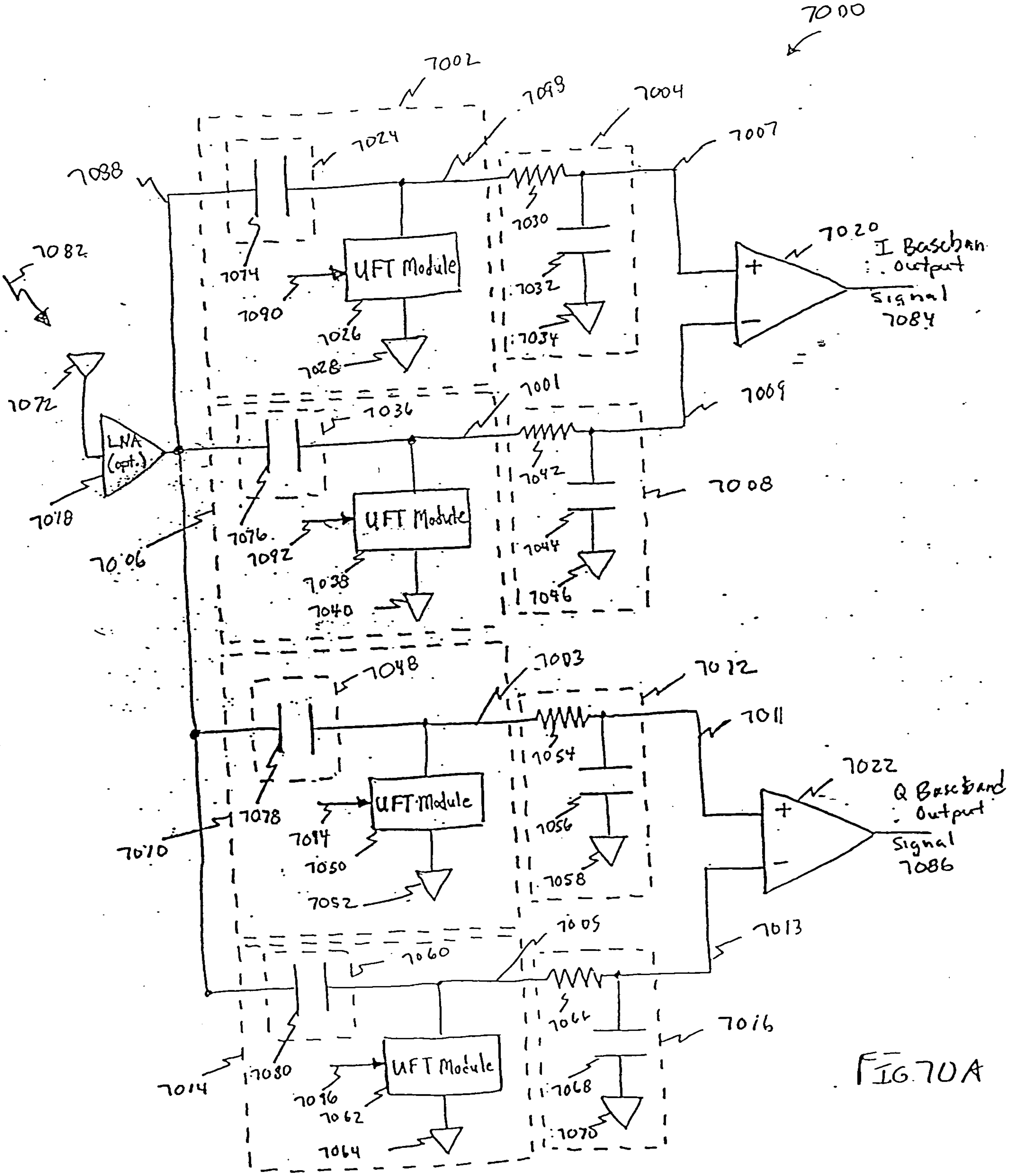

7000
7002
7098
7004
7024
7007
7088
7030
7020
I Baseband Output Signal 7084
7082
7074
UFT Module
7032
7090
7026
7034
7028
7072
7001
7009
7036
LNA (opt.)
7042
7008
7018
UFT Module
7044
7076
7092
7006
7038
7046
7040
7048
7003
7012
7011
7054
7078
UFT Module
7022
Q Baseband Output Signal 7086
7010
7094
7056
7050
7058
7052
7005
7013
7060
7066
7016
UFT Module
7014
7080
7096
7068
7062
7064
7070

FIG 70A

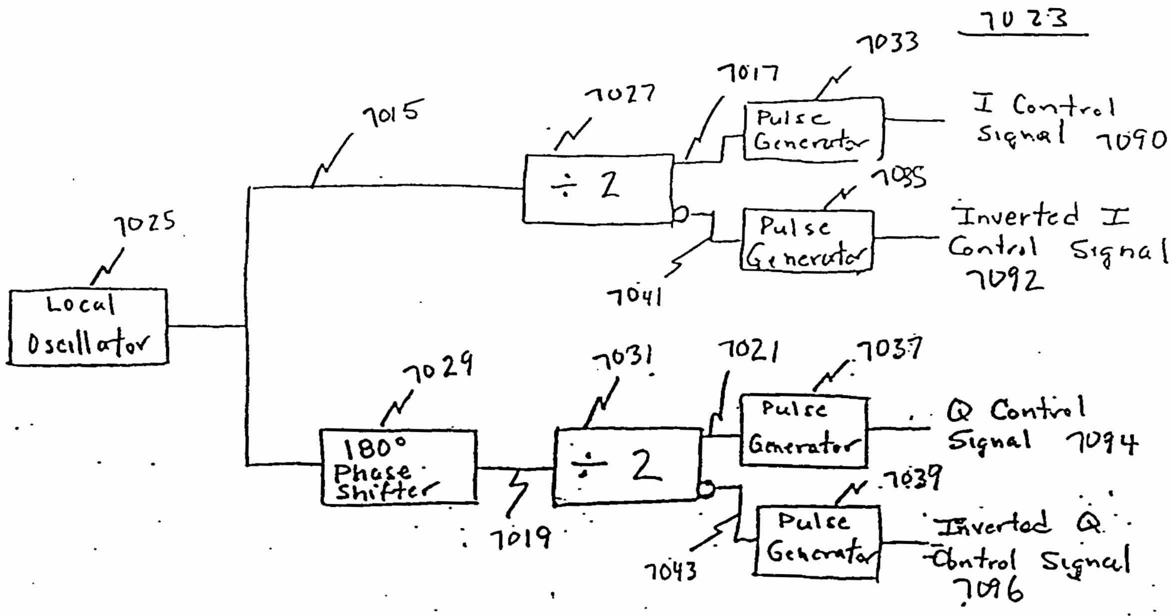


FIG. 70B

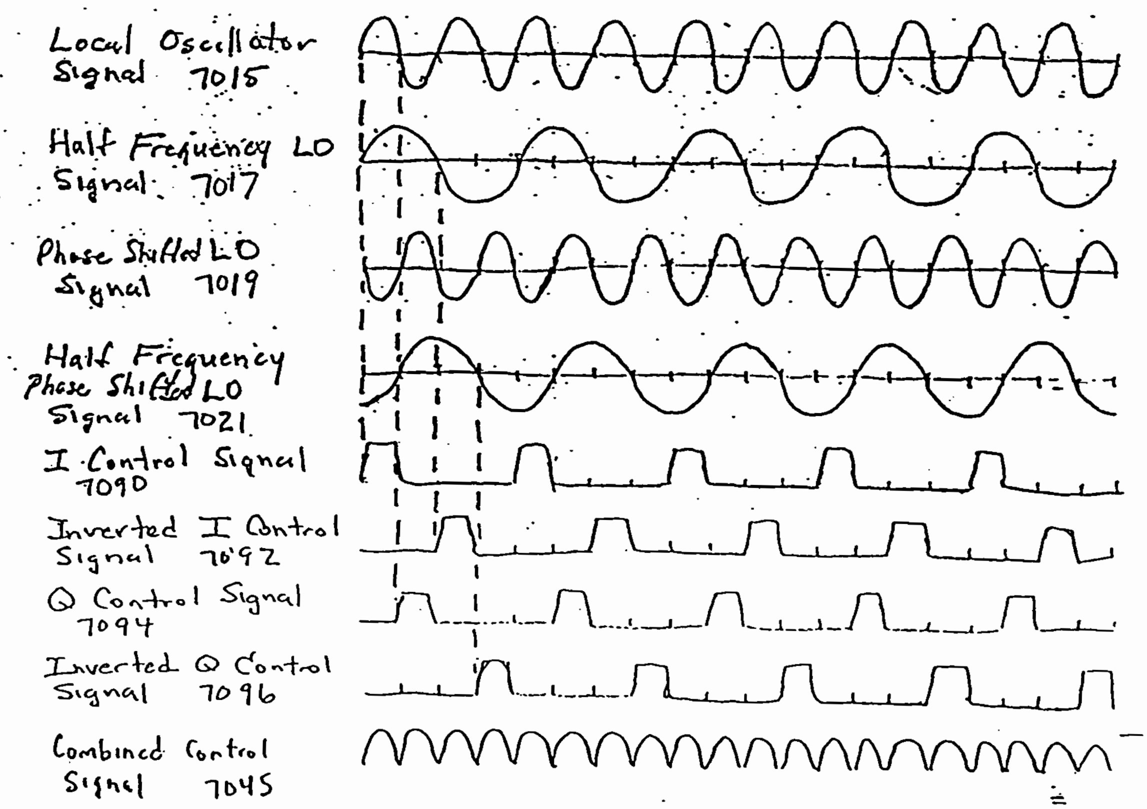
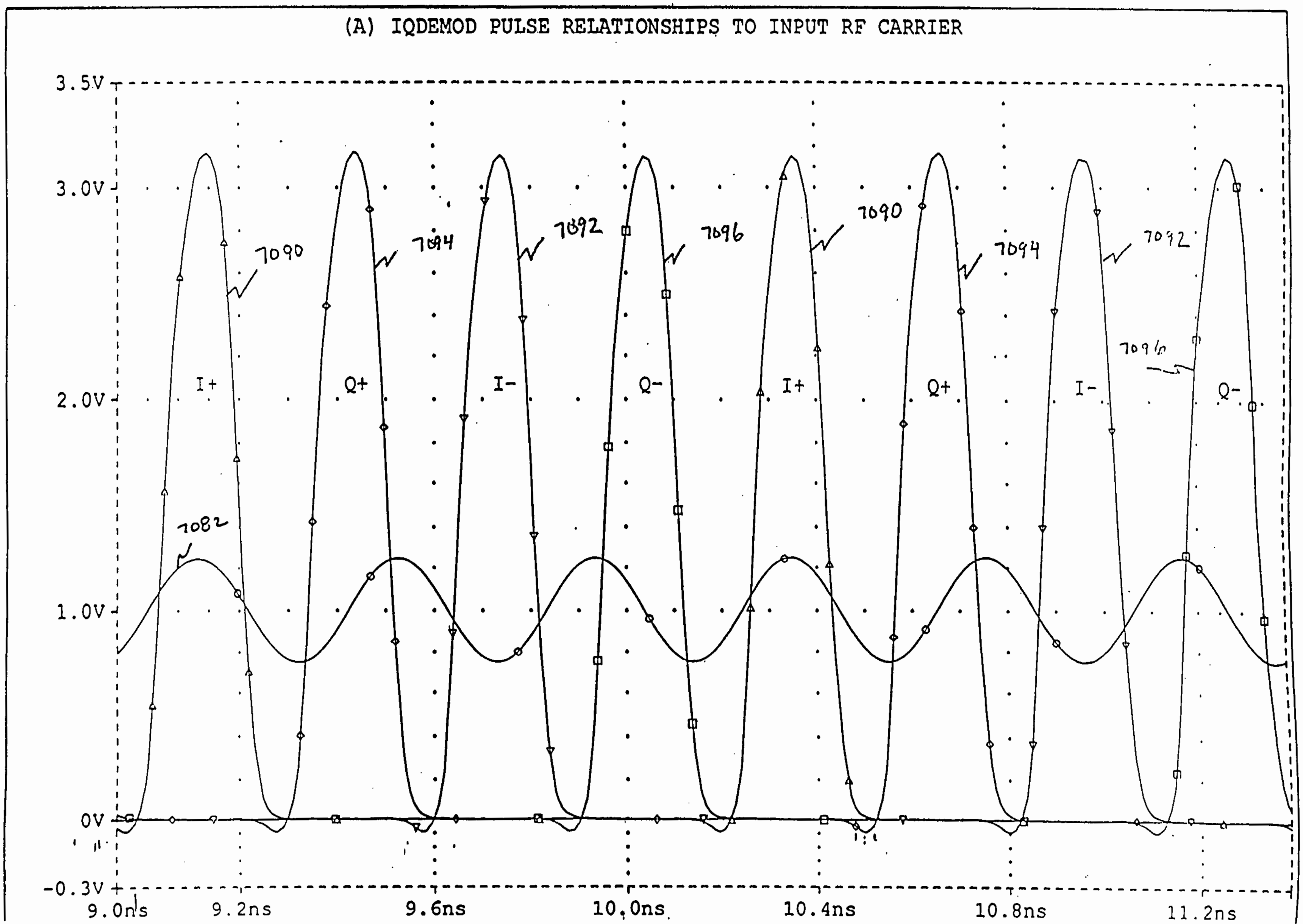


FIG. 70C



(A) IQDEMOD PULSE RELATIONSHIPS TO INPUT RF CARRIER
3.5V
3.0V
2.0V
1.0V
0V
-0.3V
9.0ns
9.2ns
9.6ns
10.0ns
10.4ns
10.8ns
11.2ns
I+
Q+
I-
Q-
I+
Q+
I-
Q-
7090
7094
7092
7096
7090
7094
7092
7096
7082

FIG. 70D

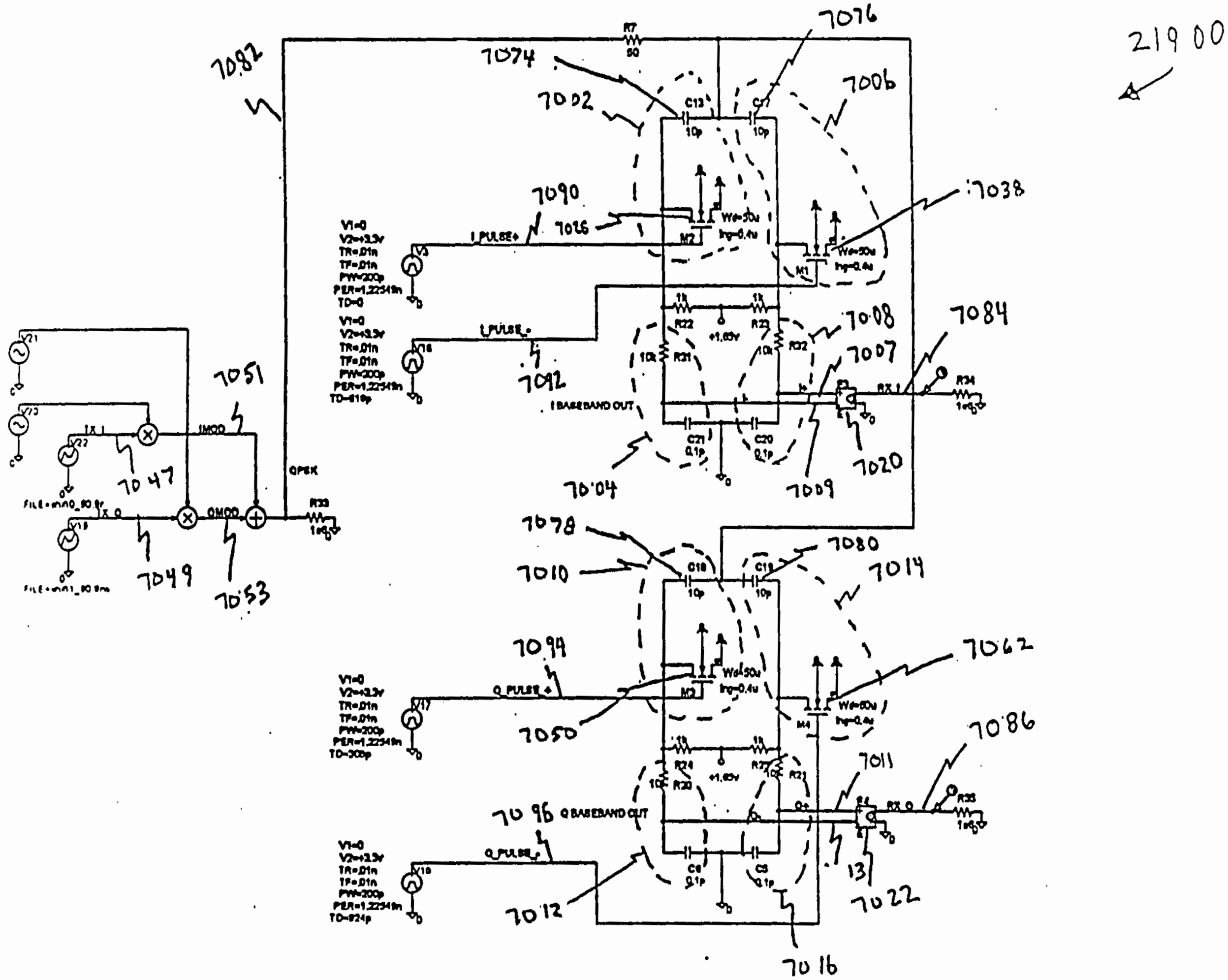
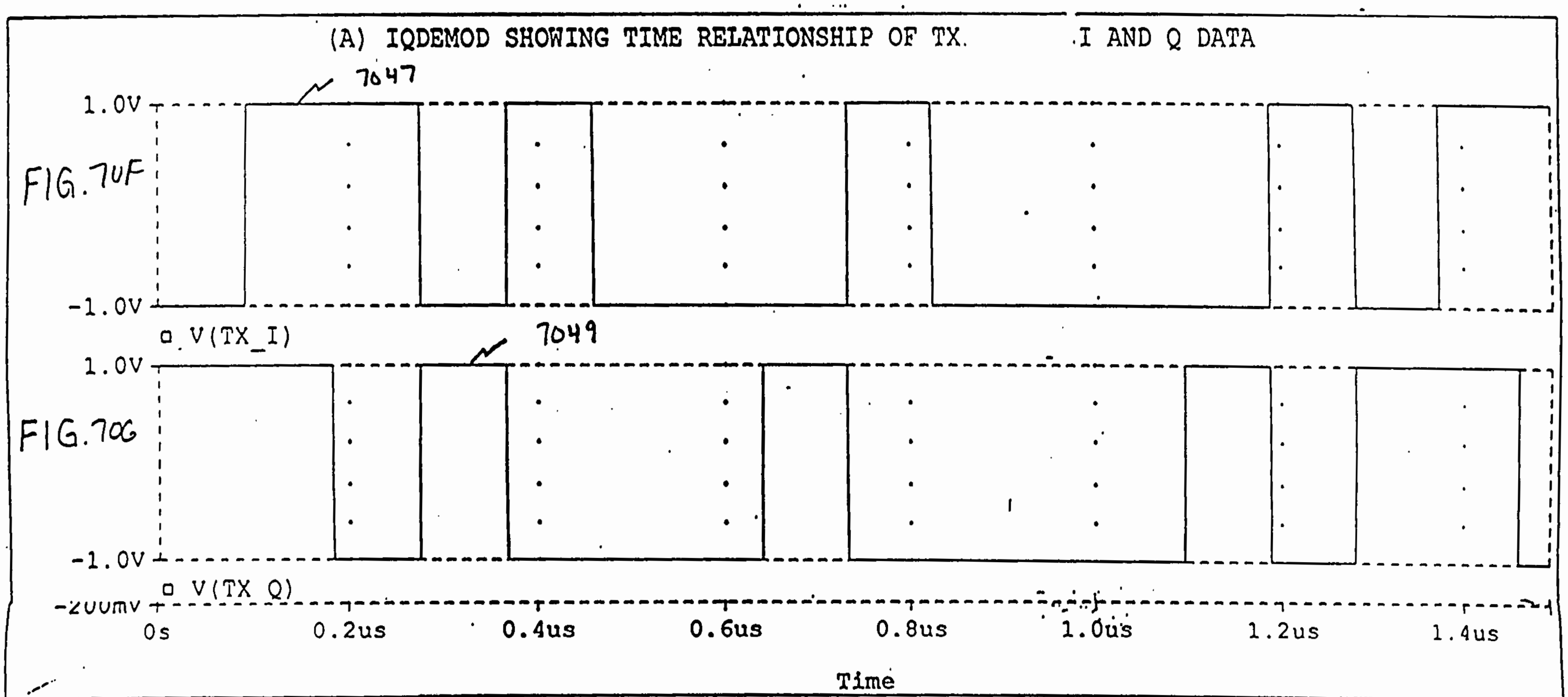
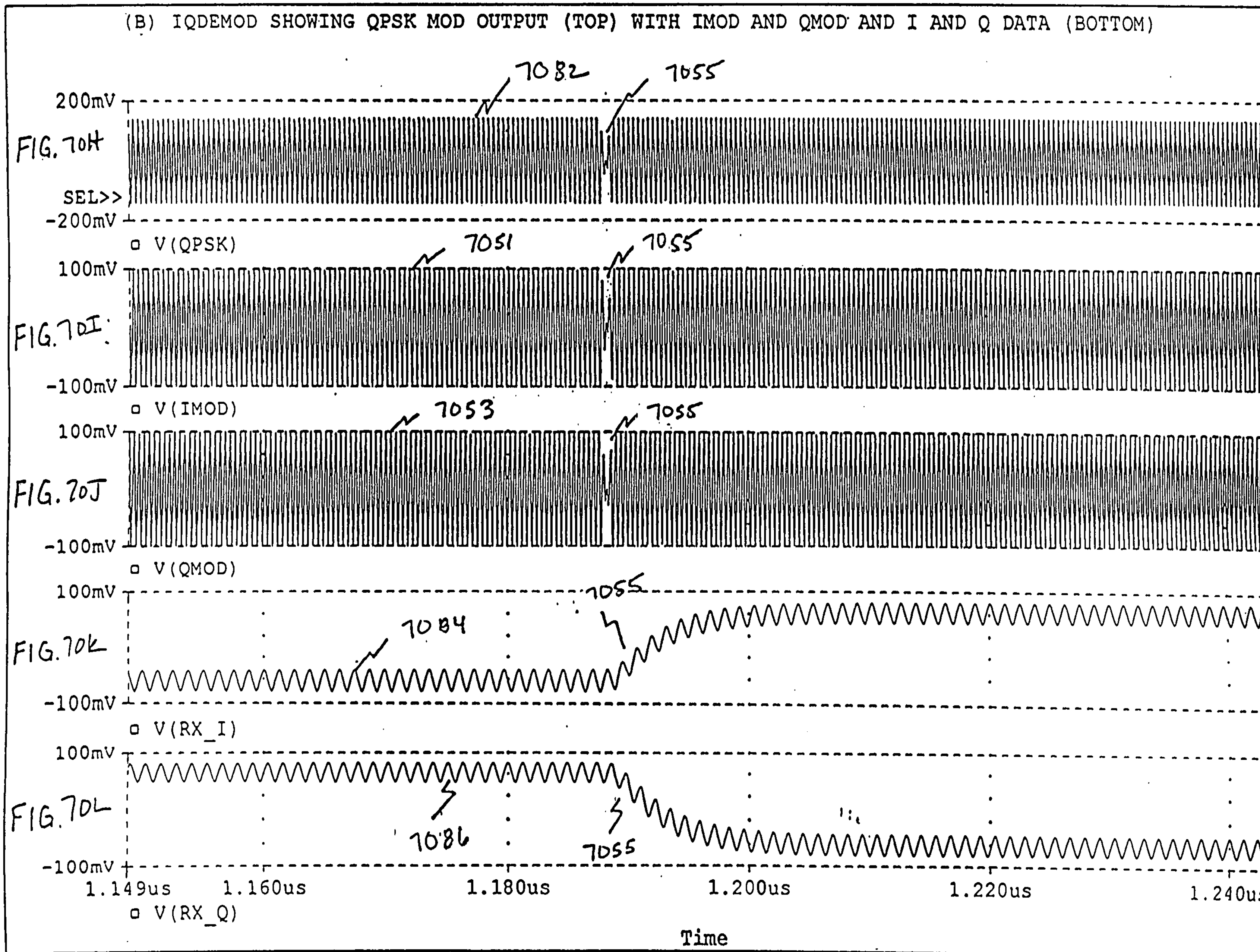

21900
7082
7074
7076
7002
7006
7090
7026
7038
7092
7008
7007
7084
7051
7047
7004
7009
7020
7049
7053
7078
7080
7010
7014
7094
7062
7050
7086
7011
7096
7012
7022
7016
I_PULSE+
I_PULSE-
Q_PULSE+
Q_PULSE-
I BASEBAND OUT
Q BASEBAND OUT
IMOD
QMOD
QPSK

FIG. 70E



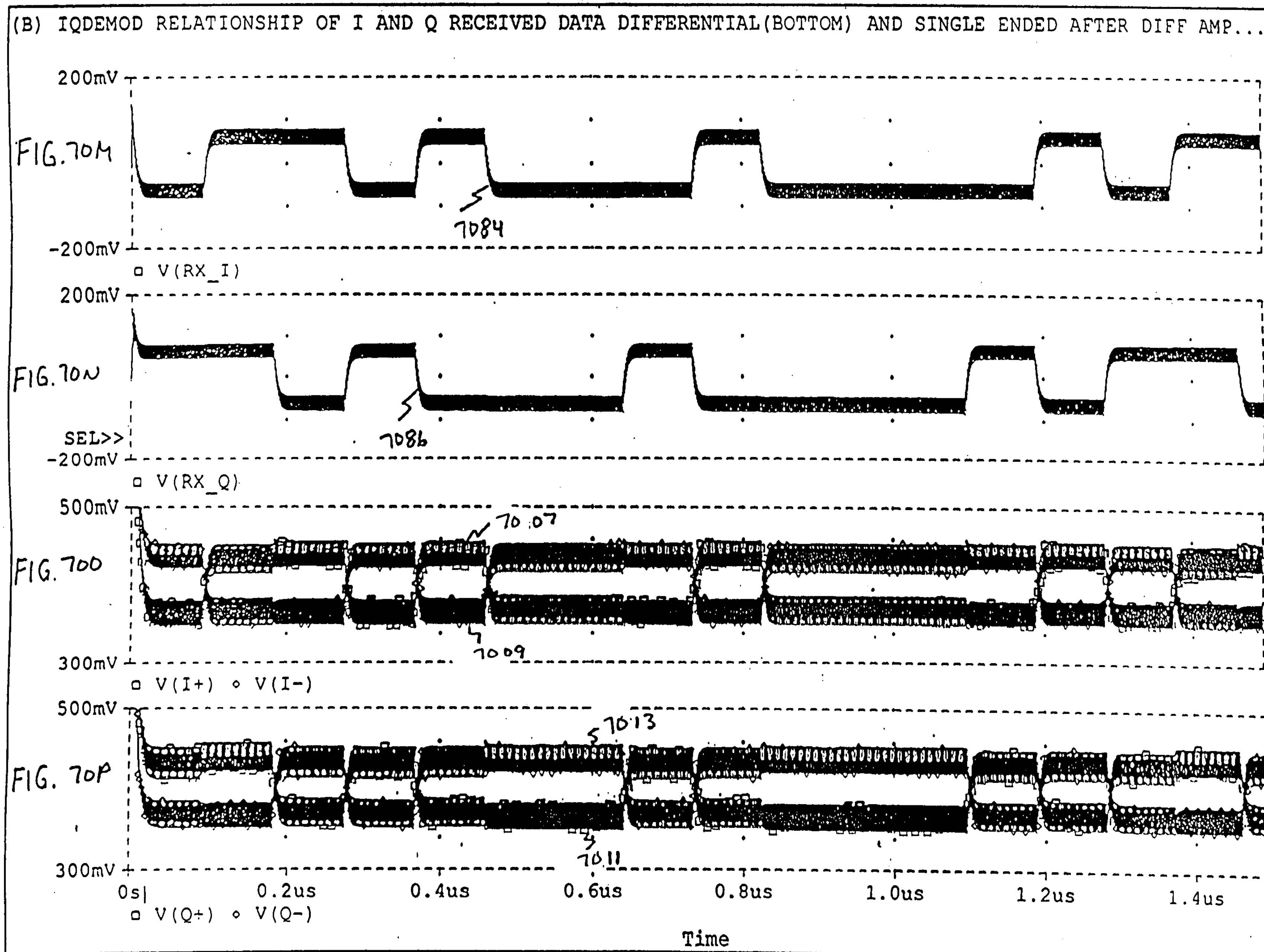
(A) IQDEMOD SHOWING TIME RELATIONSHIP OF TX I AND Q DATA
7047
1.0V
FIG. 70F
-1.0V
V(TX_I)
7049
1.0V
FIG. 70G
-1.0V
V(TX_Q)
-200mV
0s
0.2us
0.4us
0.6us
0.8us
1.0us
1.2us
1.4us
Time

Page 1



Page 1

09632356 .080400


(B) IQDEMOD RELATIONSHIP OF I AND Q RECEIVED DATA DIFFERENTIAL(BOTTOM) AND SINGLE ENDED AFTER DIFF AMP...
200mV
FIG. 70M
7084
-200mV
V(RX_I)
200mV
FIG. 70N
7086
SEL>>
-200mV
V(RX_Q)
500mV
FIG. 70O
7007
7009
300mV
V(I+) V(I-)
500mV
FIG. 70P
7013
7011
300mV
0s
0.2us
0.4us
0.6us
0.8us
1.0us
1.2us
1.4us
V(Q+) V(Q-)
Time
Page 1

7091

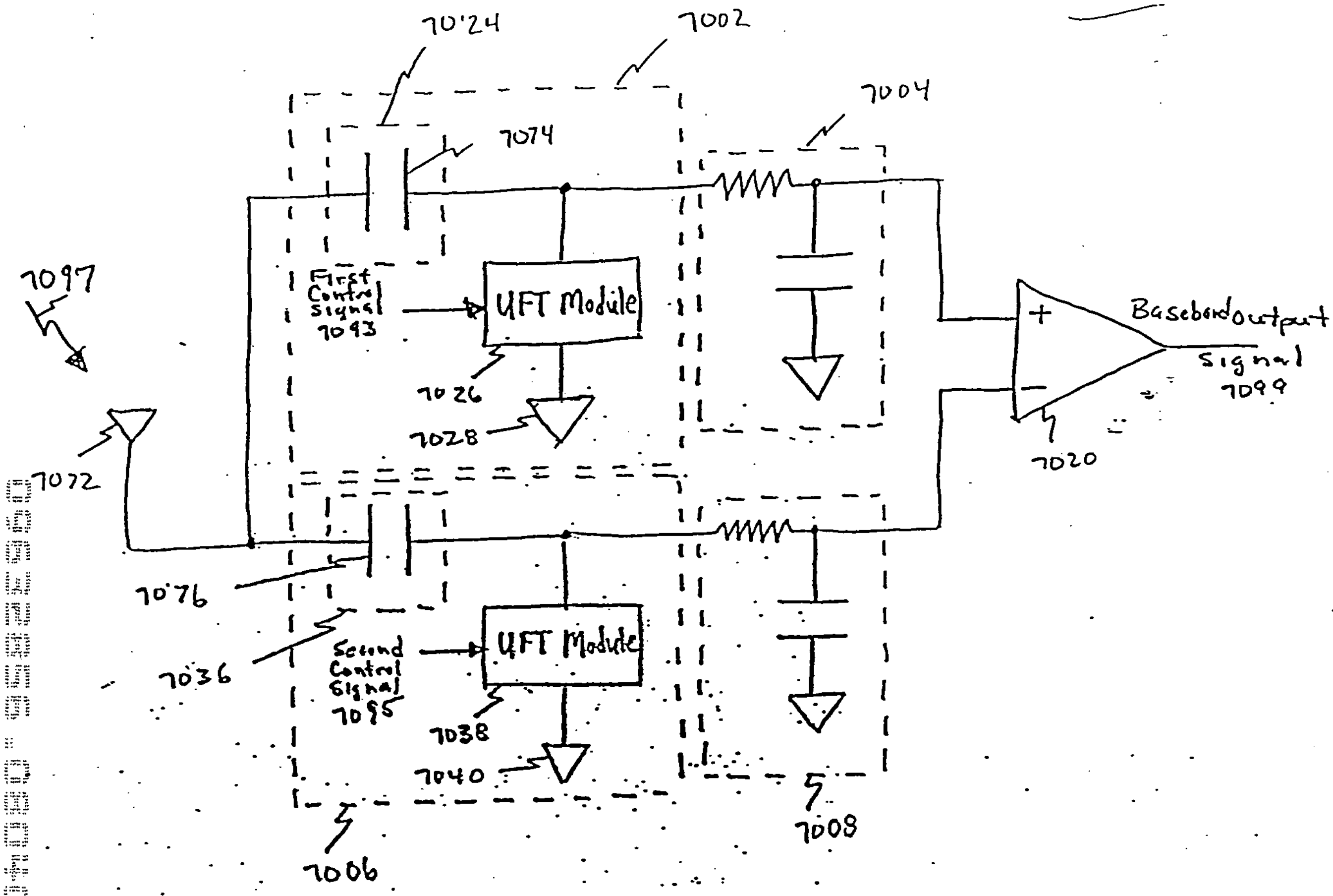

7024
7002
7004
7074
7097
First Control Signal 7093
UFT Module
7026
7028
7072
Baseband output signal 7099
7020
7076
7036
Second Control Signal 7095
UFT Module
7038
7040
7006
7008

FIG. 70Q

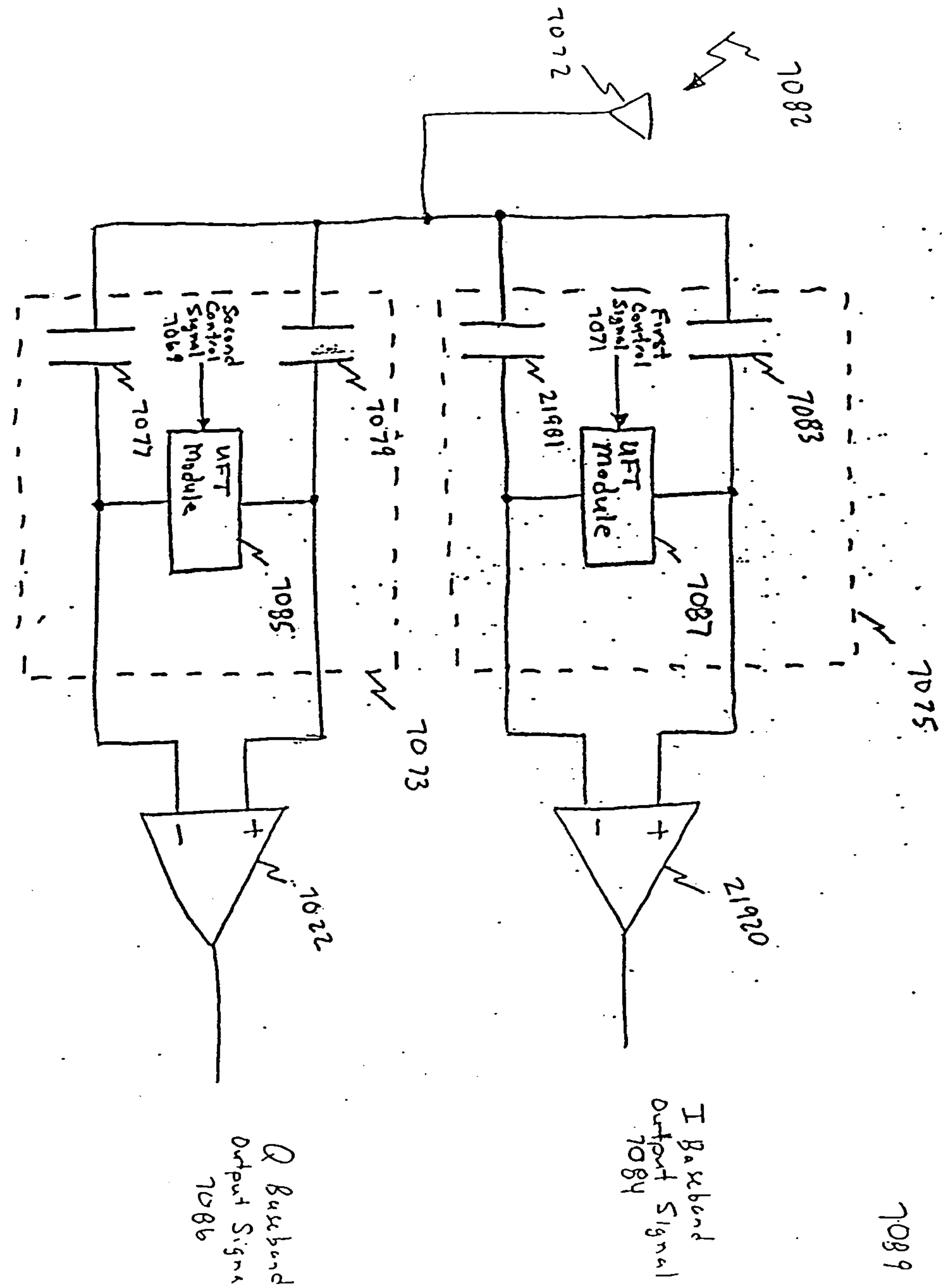
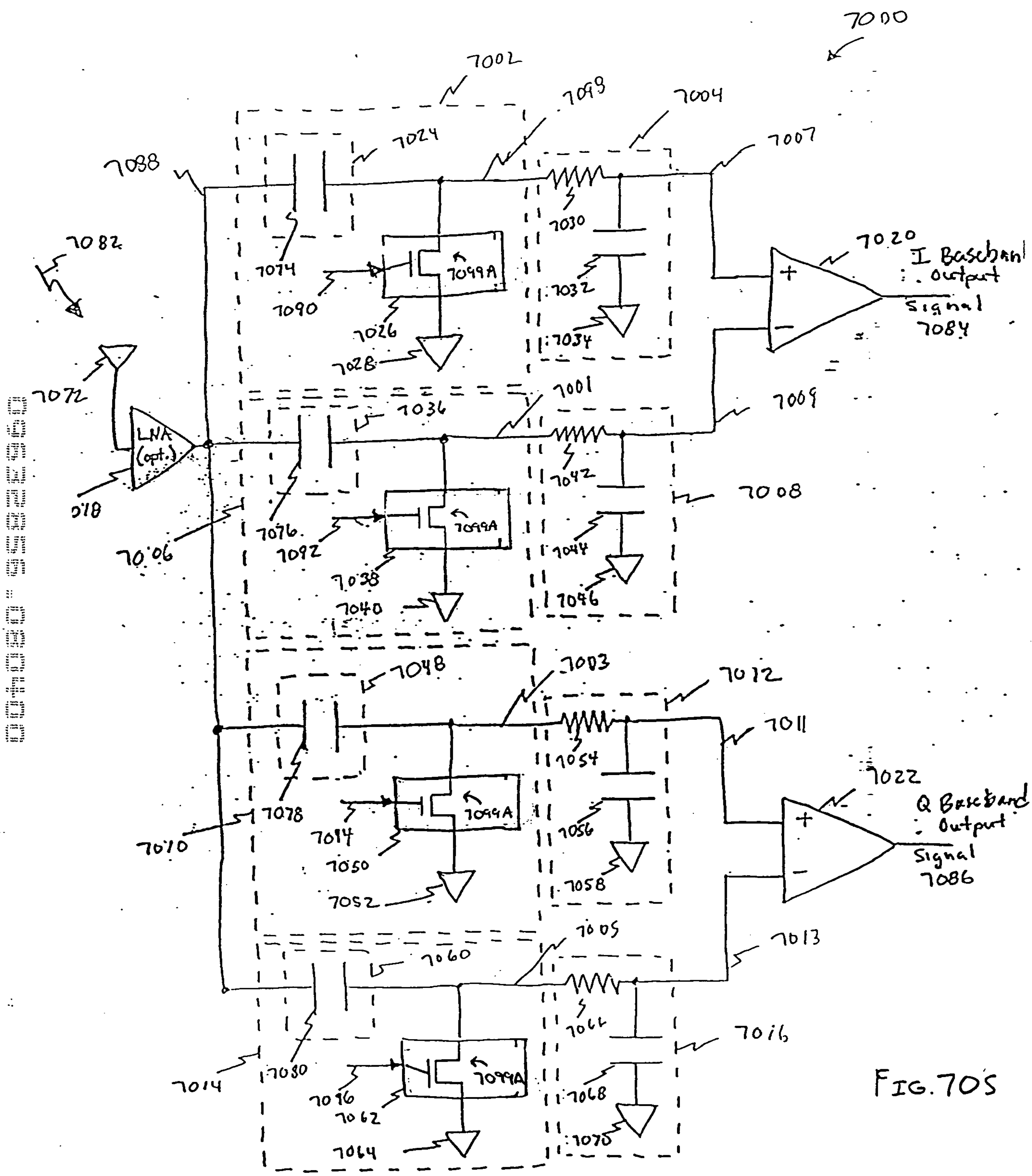

7072
7082
Second Control Signal 7069
7077
7079
UFT Module
7085
7073
7022
Q Baseband Output Signal 7086
First Control Signal 7071
21981
7083
UFT Module
7087
7075
21920
I Baseband Output Signal 7084
7089

FIG. 70 R



7000
7002
7098
7004
7024
7007
7088
7030
7082
7074
7099A
I Baseband Output Signal 7084
7020
7090
7032
7026
7034
7028
7072
7001
7036
7009
LNA (opt.)
7042
7018
7008
7076
7092
7099A
7006
7044
7038
7046
7040
7048
7003
7012
7011
7054
7022
7078
7099A
Q Baseband Output Signal 7086
7010
7094
7056
7050
7058
7052
7005
7013
7060
7066
7016
7014
7080
7099A
7096
7068
7062
7070
7064

FIG. 70S

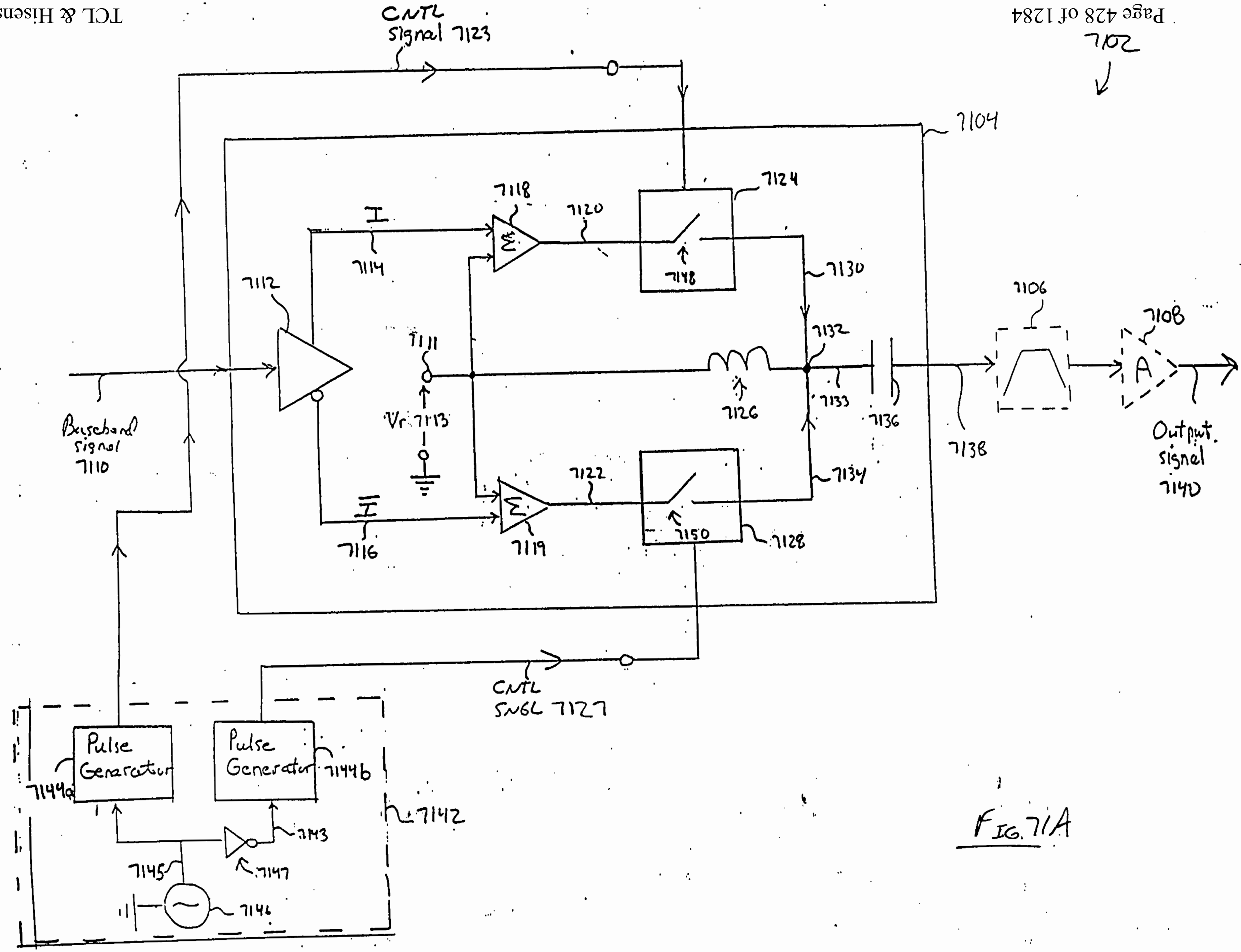


FIG. 71A

09632856.080400

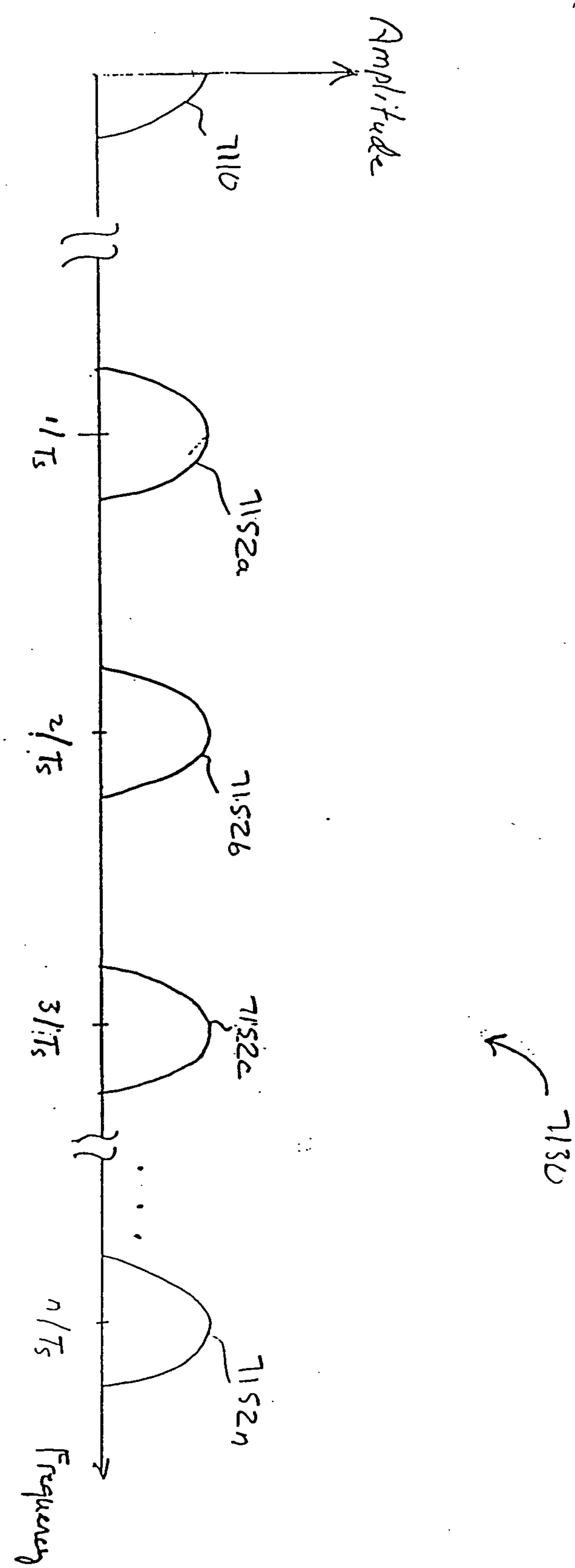

Amplitude
7110
1/Ts
7152a
2/Ts
7152b
3/Ts
7152c
n/Ts
7152n
Frequency
7130

FIG. 71B

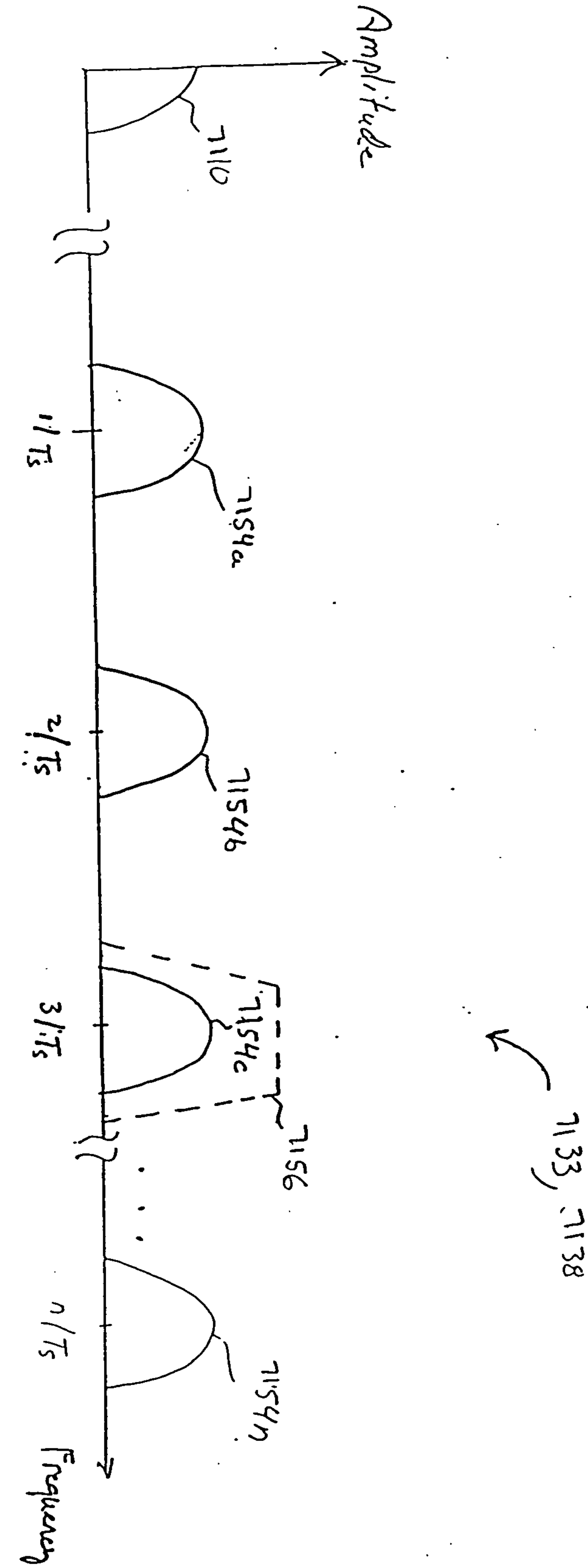

Amplitude
7110
1/Ts
7154a
2/Ts
7154b
3/Ts
7154c
7156
n/Ts
7154n
Frequency
7133, 7138

FIG. 71C

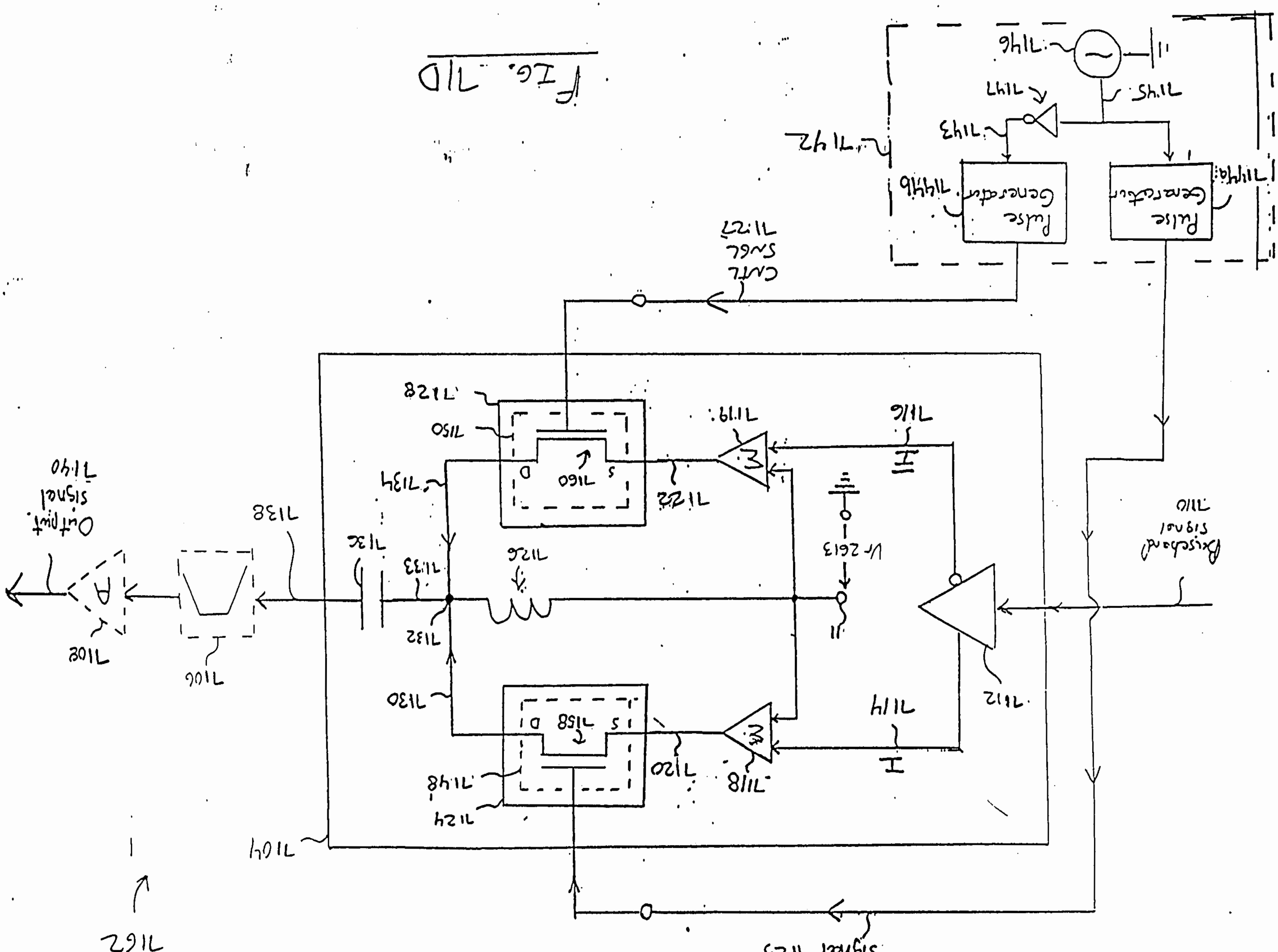


FIG. 71D
Pulse Generator 7144a
Pulse Generator 7144b
CNTL SNGL 7127
CNTL signal 7123
Baseband signal 7110
Output signal 7140

FIG. 72A

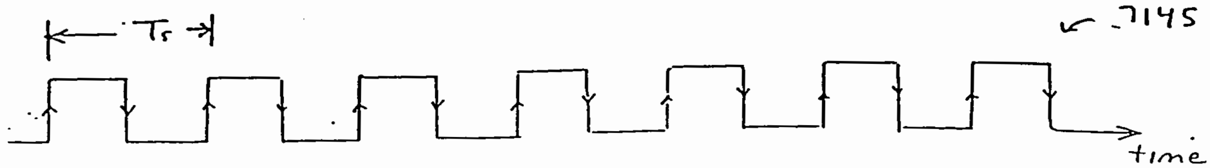


FIG. 72B

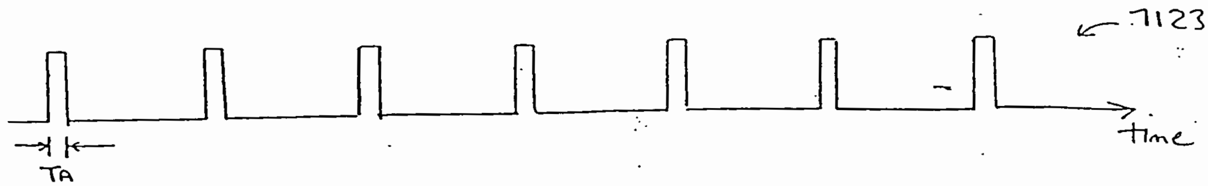


FIG. 72C

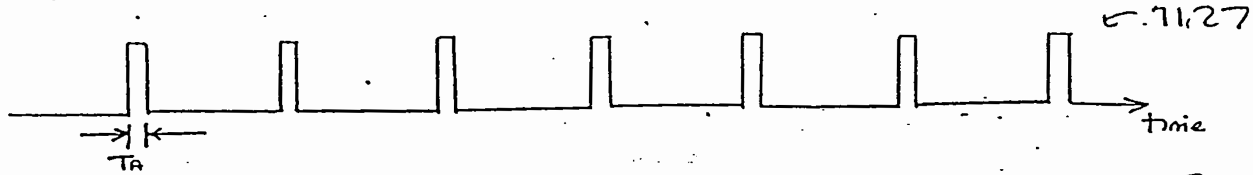


FIG. 72D

FIG. 72E

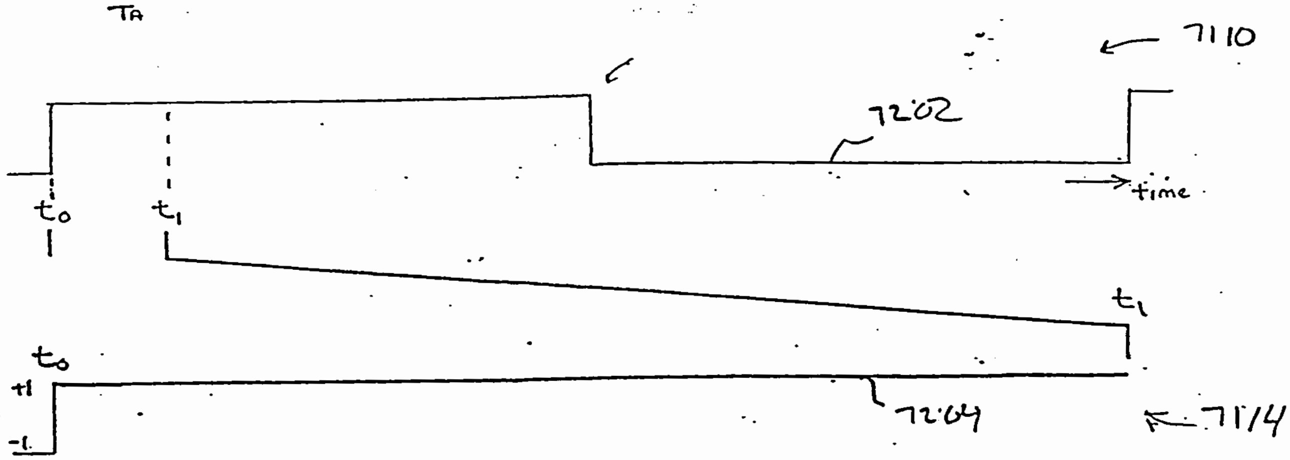


FIG. 72F

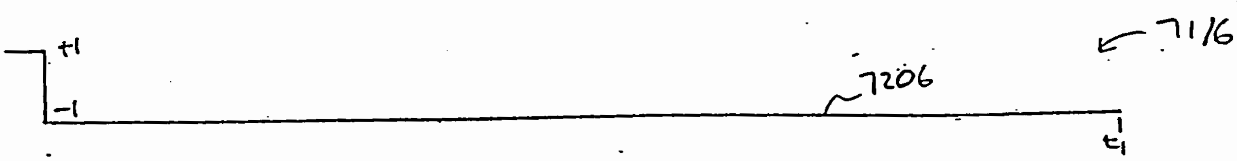


FIG. 72G

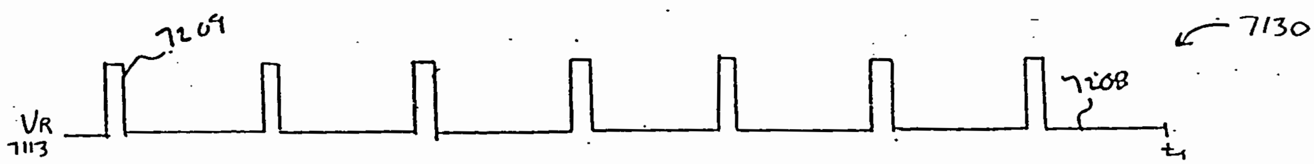


FIG. 72H

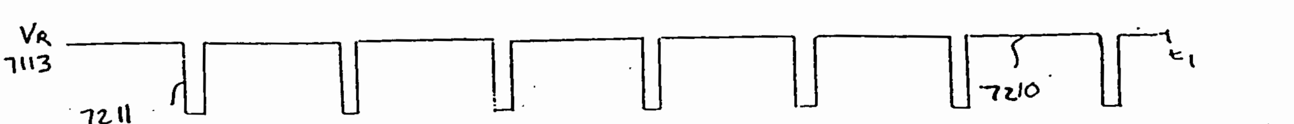
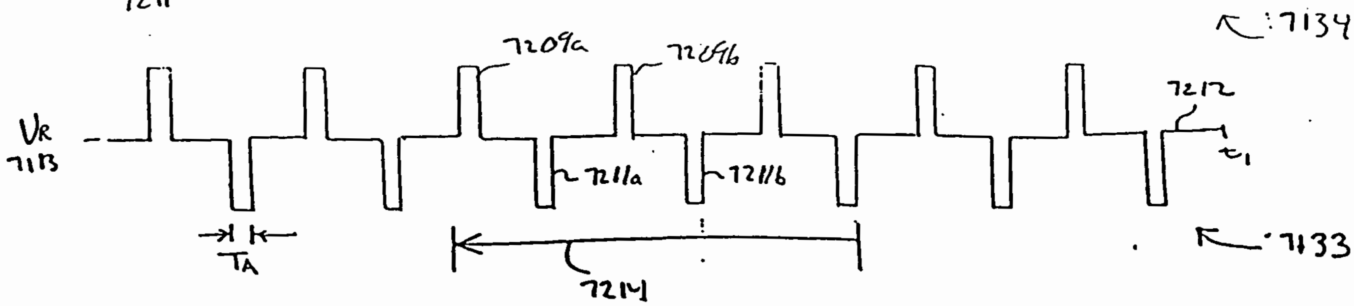


FIG. 72I



Aperture = 500ps
Fundamental Clock = 200Mhz (5th Subharmonic)

Square Wave Frequency = 200Mhz

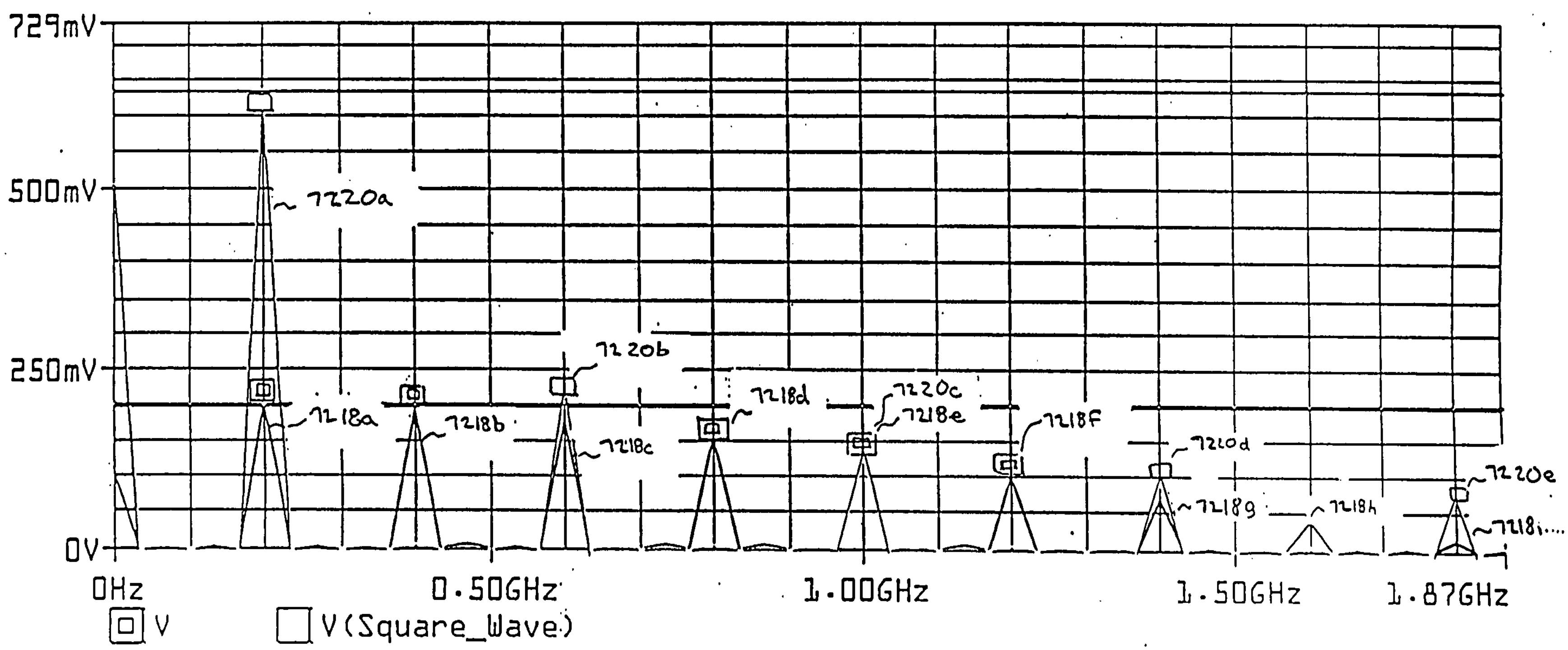
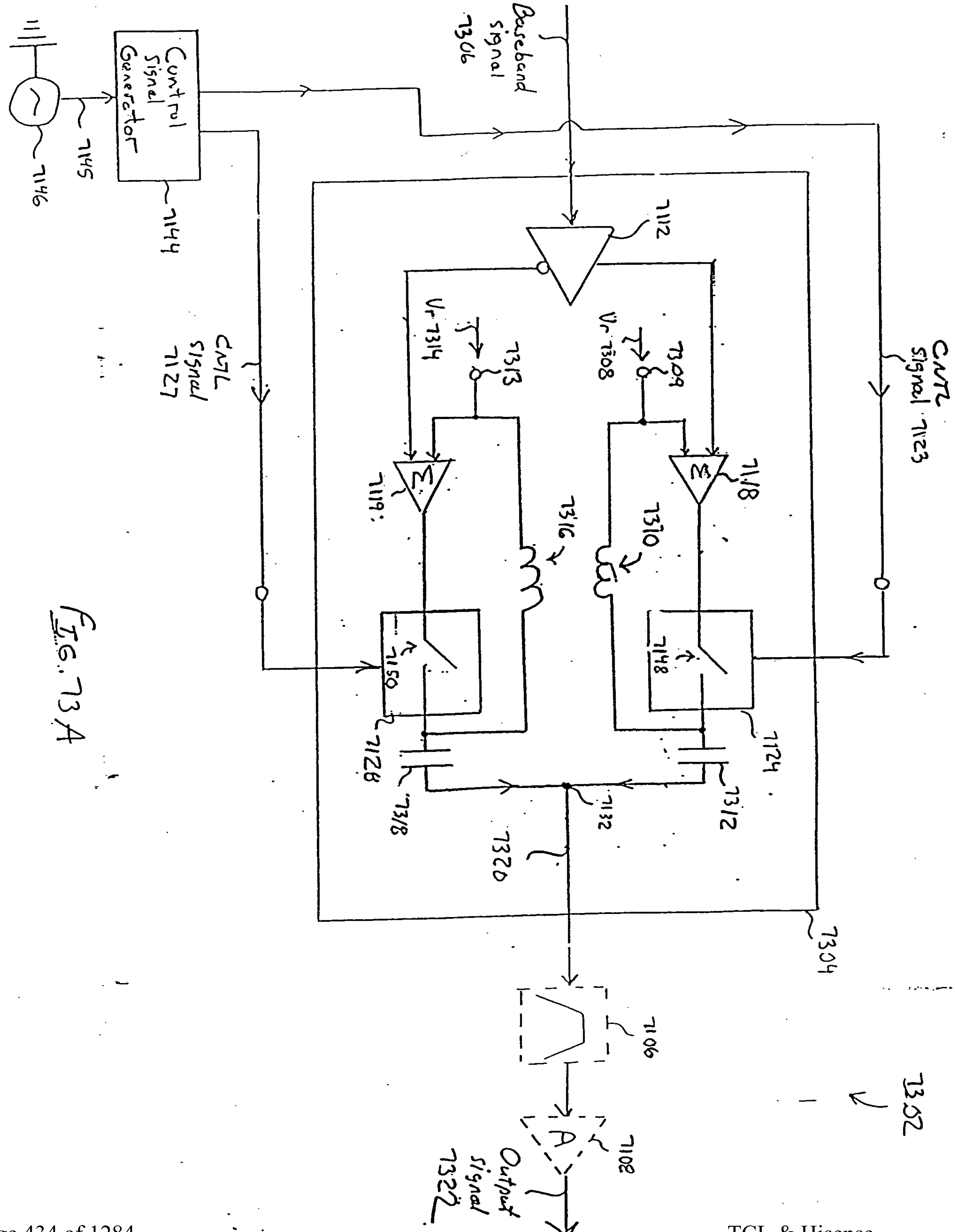
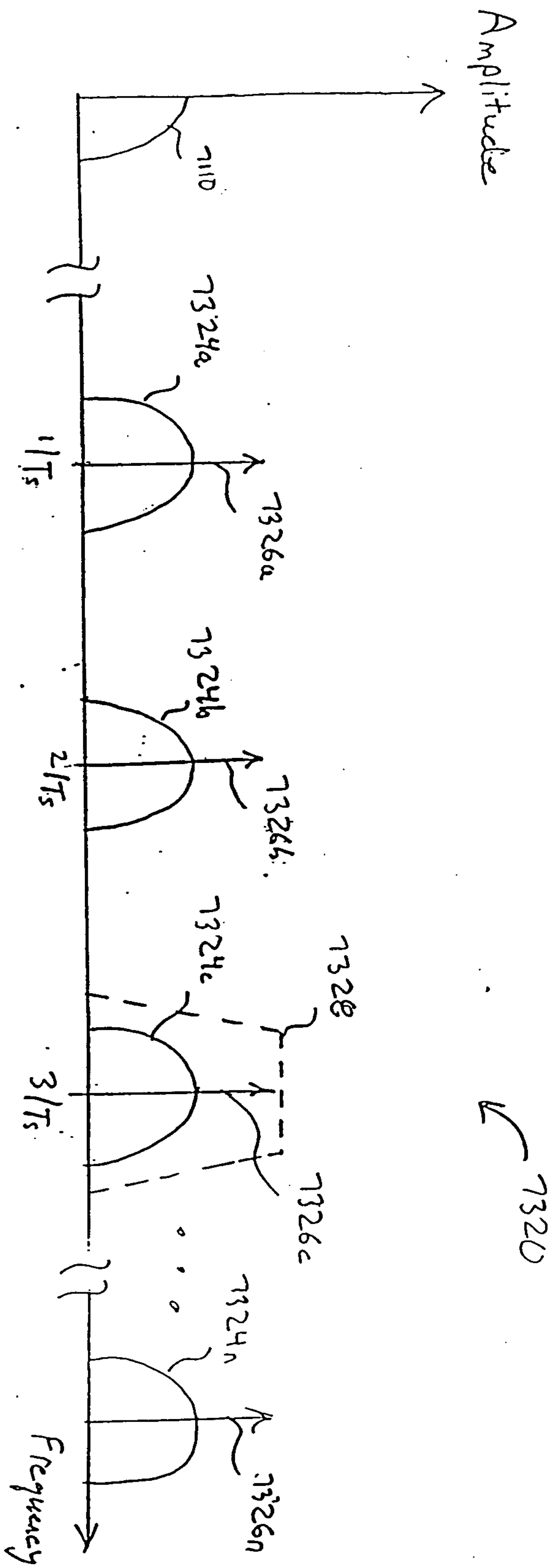


FIG. 72J



Baseband signal 7306
Control Signal Generator
7144
7145
7146
7112
Vr 7308
7309
Vr 7314
7313
7118
7119
7310
7316
7148
7150
7124
7128
7312
7318
7132
7320
7304
CNTL signal 7123
CNTL signal 7127
7106
7108
Output signal 7322
7302

FIG. 73A



Amplitude
7110
7324a
7326a
1/Ts
7324b
7326b
2/Ts
7324c
7328
3/Ts
7326c
7320
7324n
7326n
Frequency

FIG. 73B

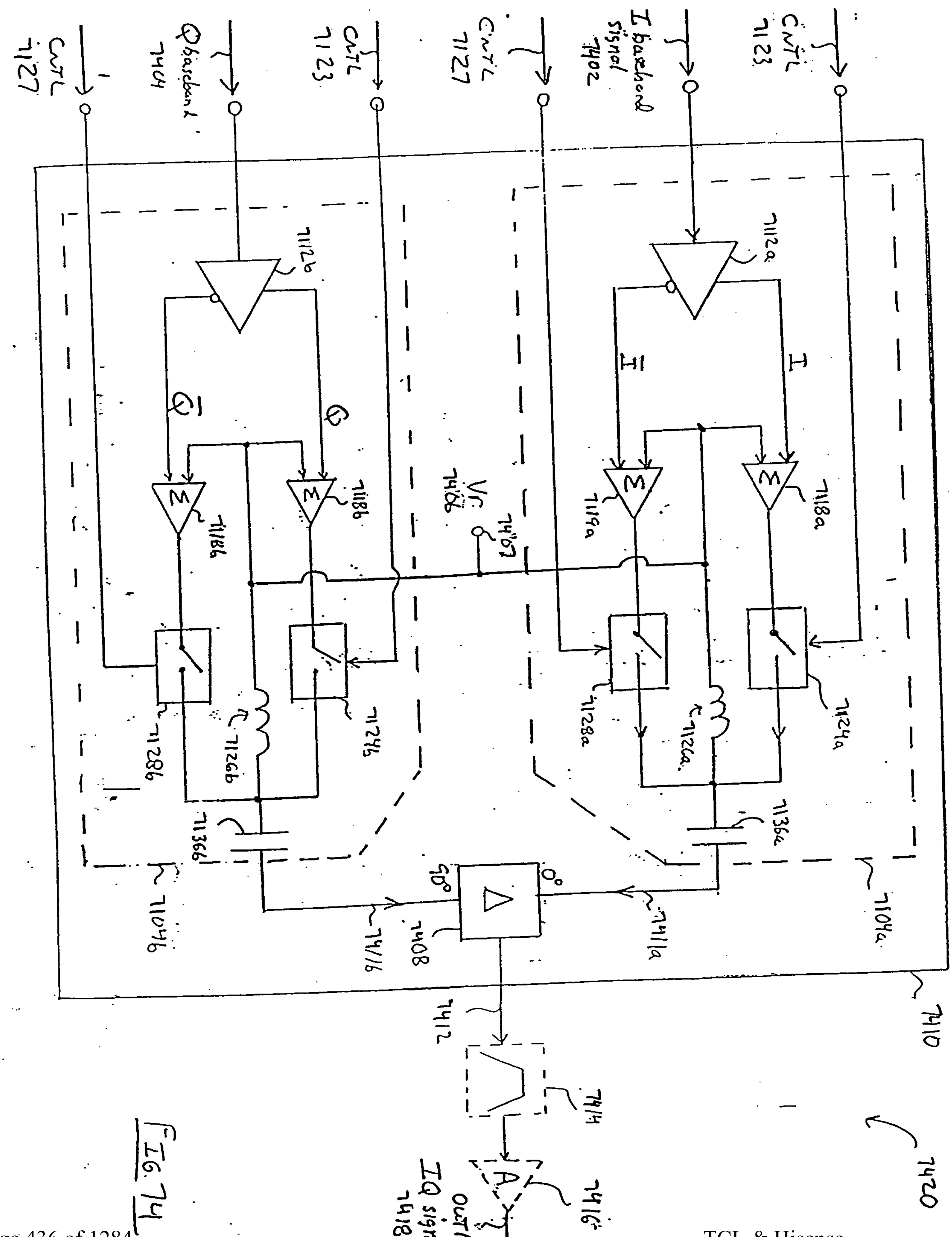

CNTL 7123
I baseband signal 7402
CNTL 7127
CNTL 7123
Q baseband 7404
CNTL 7127
7112a
7112b
I
Ī
Q
Q̄
M
7118a
7119a
7118b
Vr 7406
7407
7124a
7128a
7126a
7124b
7126b
7128b
7136a
7136b
7104a
7104b
0°
90°
7411a
7416
7408
7410
7412
7414
A
7416
7420
OUTPUT IQ signal 7418

FIG. 74

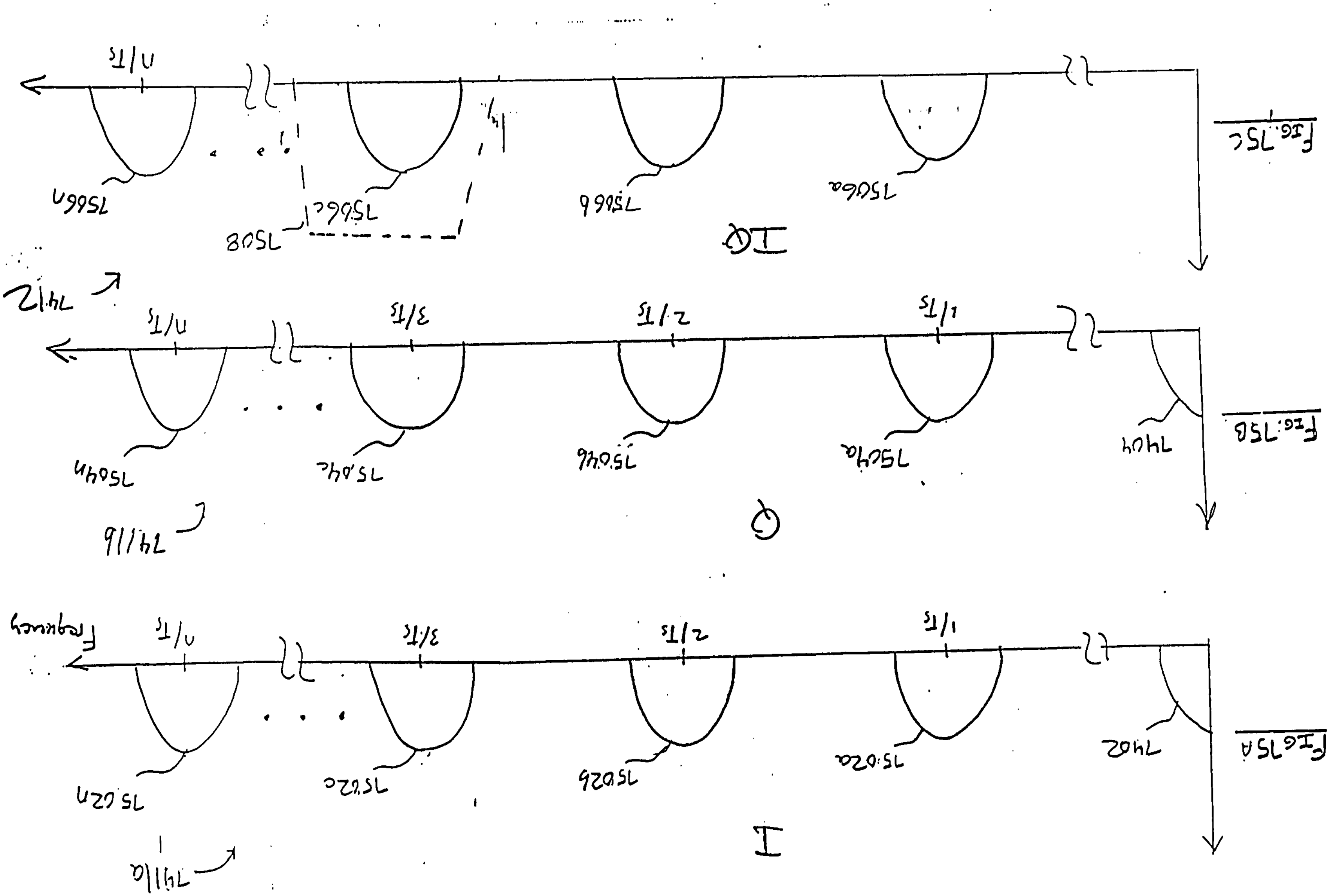


FIG. 15A
FIG. 15B
FIG. 15C
I
Q
IQ
Frequency
1/Ts
2/Ts
3/Ts
n/Ts
7402
7404
7412
7416
1502a
1502b
1502c
1502n
1504a
1504b
1504c
1504n
1506a
1506b
1506c
1506n
1508

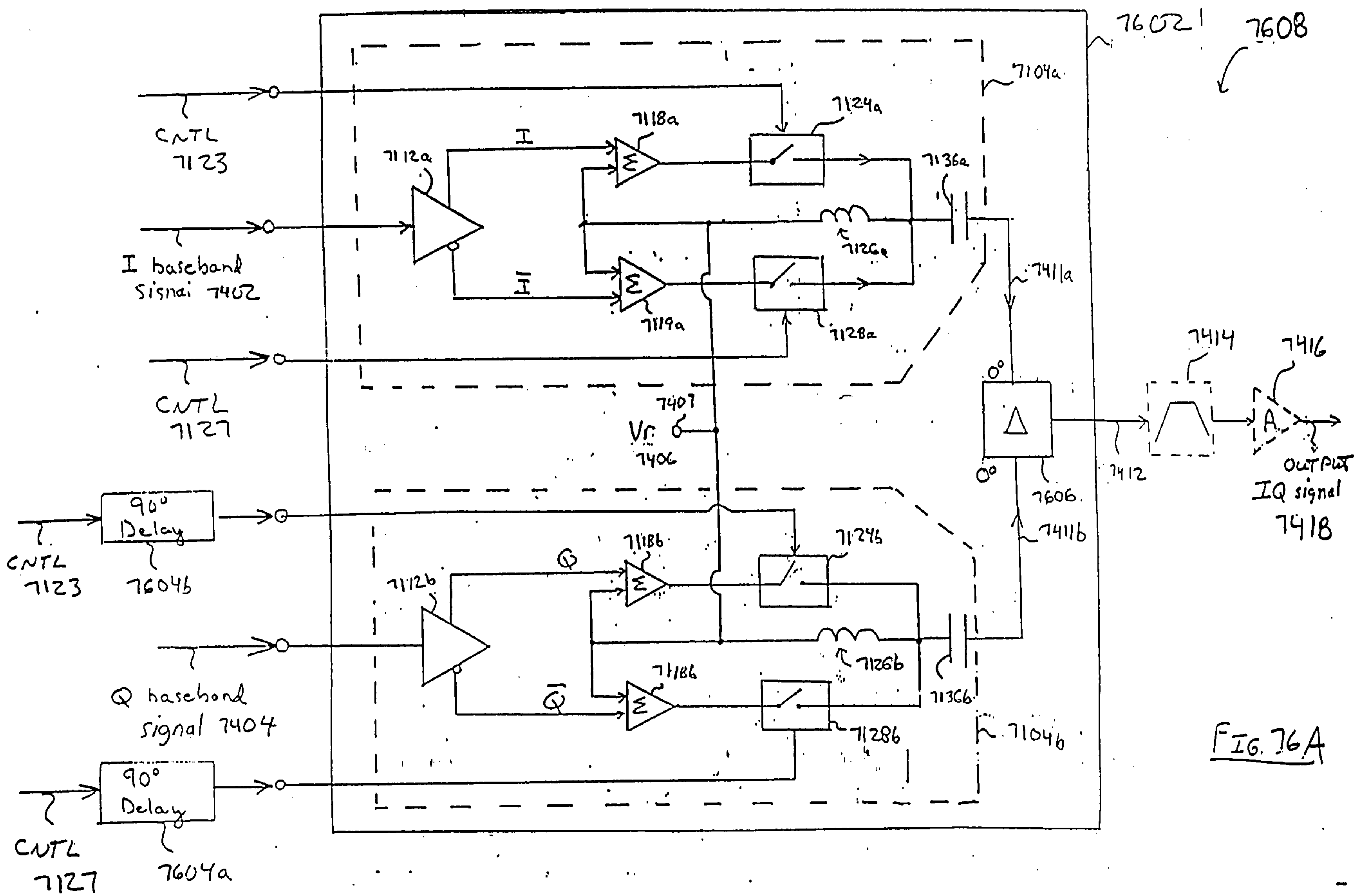
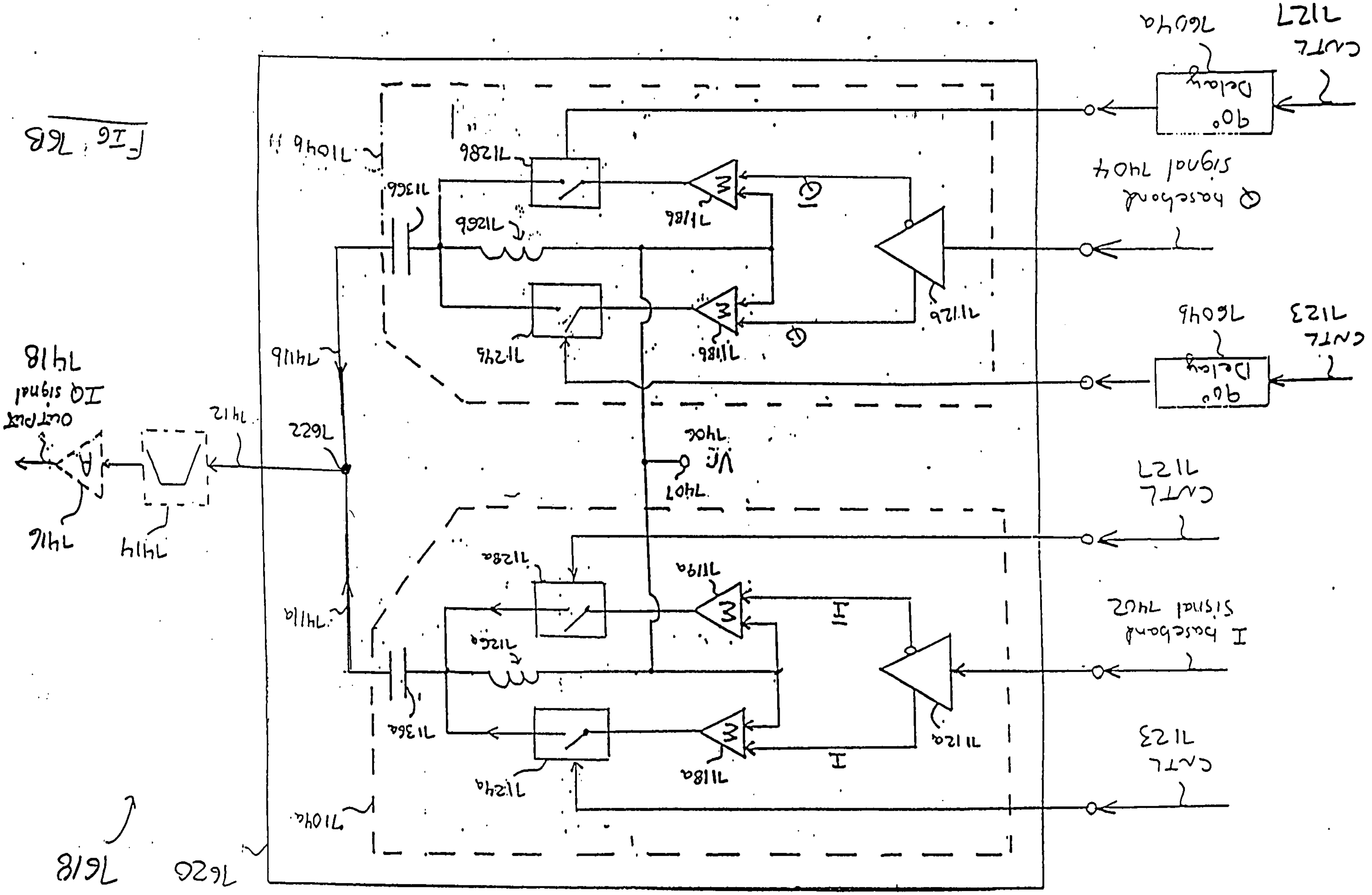

7602
7608
7104a
7124a
7118a
I
7112a
7136a
CNTL 7123
I baseband signal 7402
7126a
7119a
7128a
7411a
CNTL 7127
7407
Vr 7406
0°
7414
7416
7412
7606
OUTPUT IQ signal 7418
90° Delay
CNTL 7123
7604b
7124b
7118b
Q
7112b
7411b
Q baseband signal 7404
7126b
7136b
7104b
7128b
CNTL 7127
7604a

FIG. 76A

FIG 7B



CNTL 7127
90° Delay
7604a
Q baseband signal 7404
CNTL 7123
90° Delay
7604b
CNTL 7127
I baseband signal 7402
CNTL 7123
Output IQ signal
7418
7412
7414
7416
7622
Vi 7406
7407
7104b
7104a
7416b
7416a
7128b
7136b
7126b
7118b
7112b
7124b
7128a
7118a
7126a
7136a
7124a
7118a
7112a
7620
7618

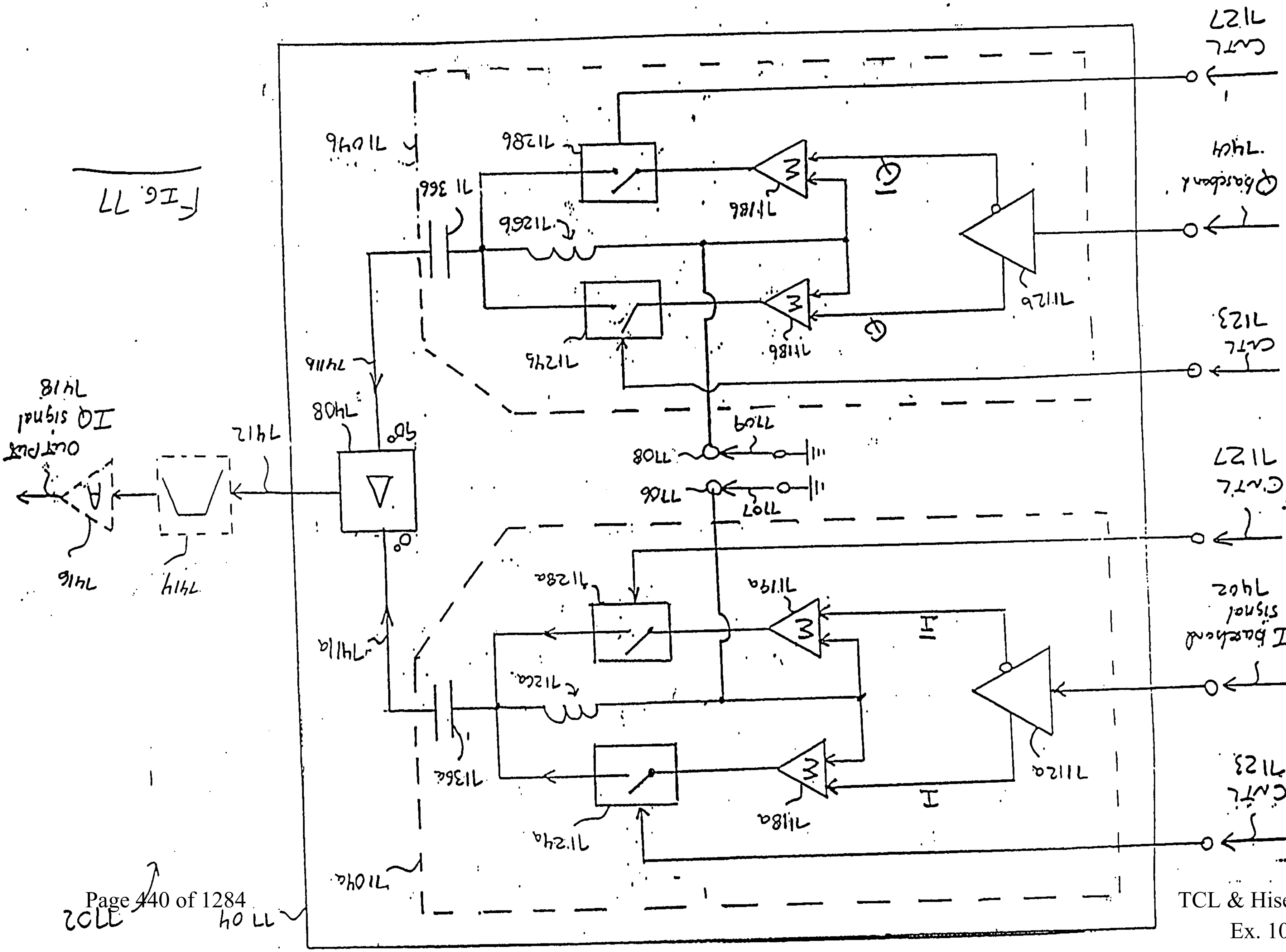

CNTL 7127
Q baseband 7404
CNTL 7123
I baseband signal 7402
Output IQ signal 7418
7412
7408
7414
7416
7104
7102

FIG. 77

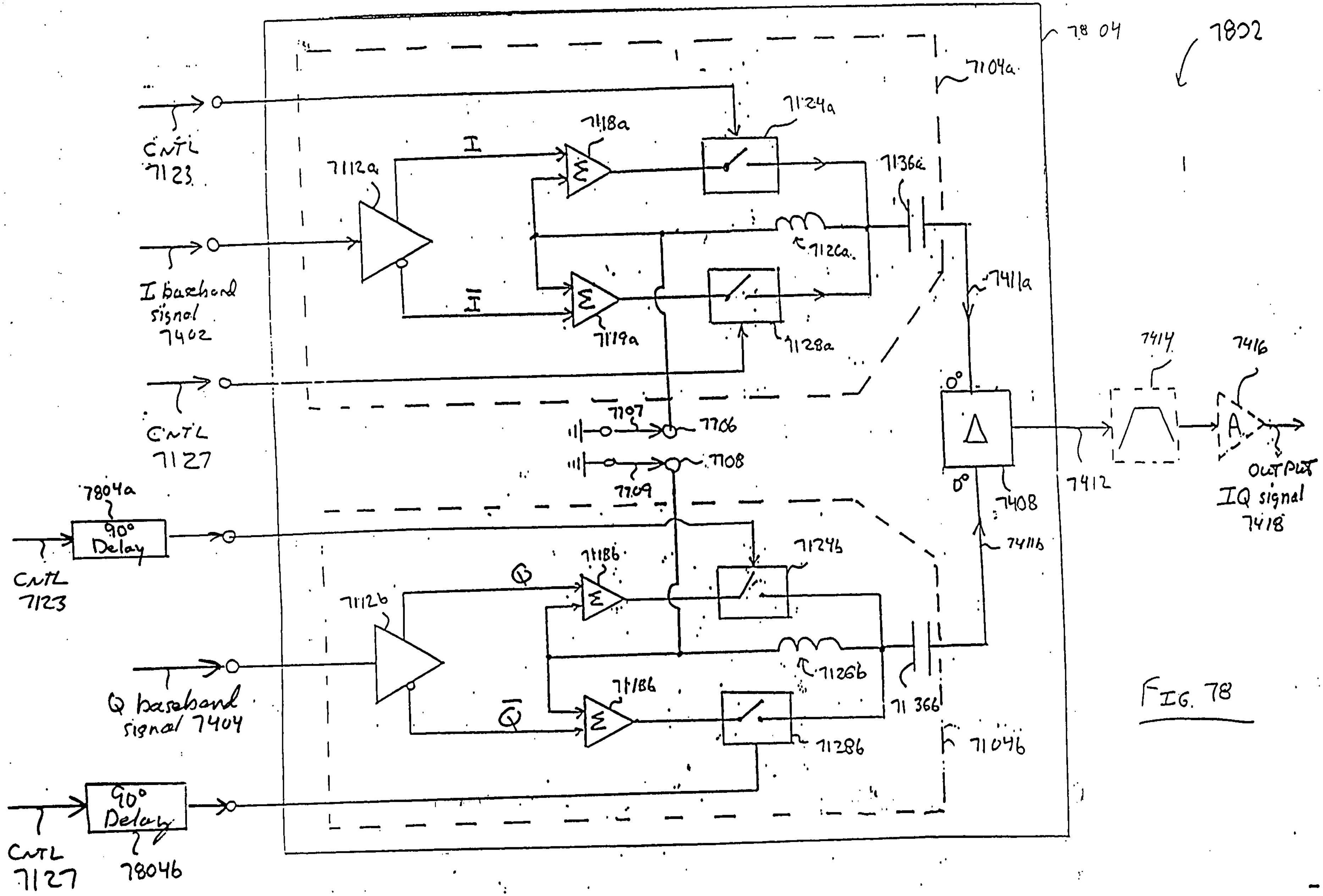
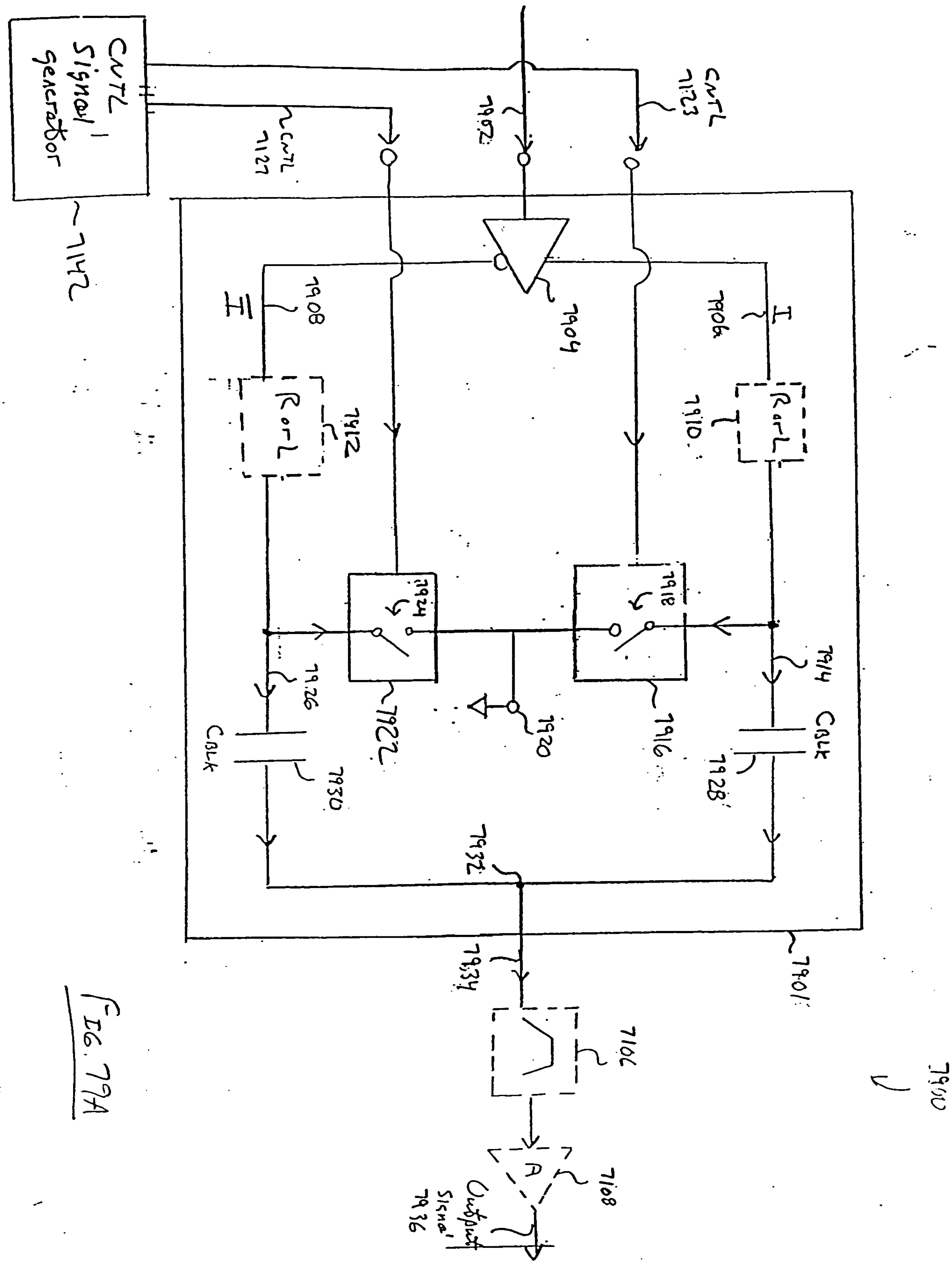

7802
7804
7104a
7124a
7118a
I
CNTL
7123
7112a
7136a
7126a
7411a
I baseband
signal
7402
Ī
7119a
7128a
7414
7416
0°
CNTL
7127
7107
7106
7108
7109
7412
OUTPUT
IQ signal
7418
7804a
90°
Delay
7408
CNTL
7123
7411b
7118b
7124b
Q
7112b
7126b
Q baseband
signal 7404
7136b
Q̄
7119b
7128b
7104b
90°
Delay
CNTL
7127
7804b

FIG. 78



CNTL Signal Generator
7142
CNTL 7127
7902
CNTL 7123
7904
7908
7906
R or L
7912
R or L
7910
7924
7918
7926
7922
7920
7916
7914
7930
7928
7932
7934
7901
7106
A
7108
Output Signal 7936
7900

FIG. 79A

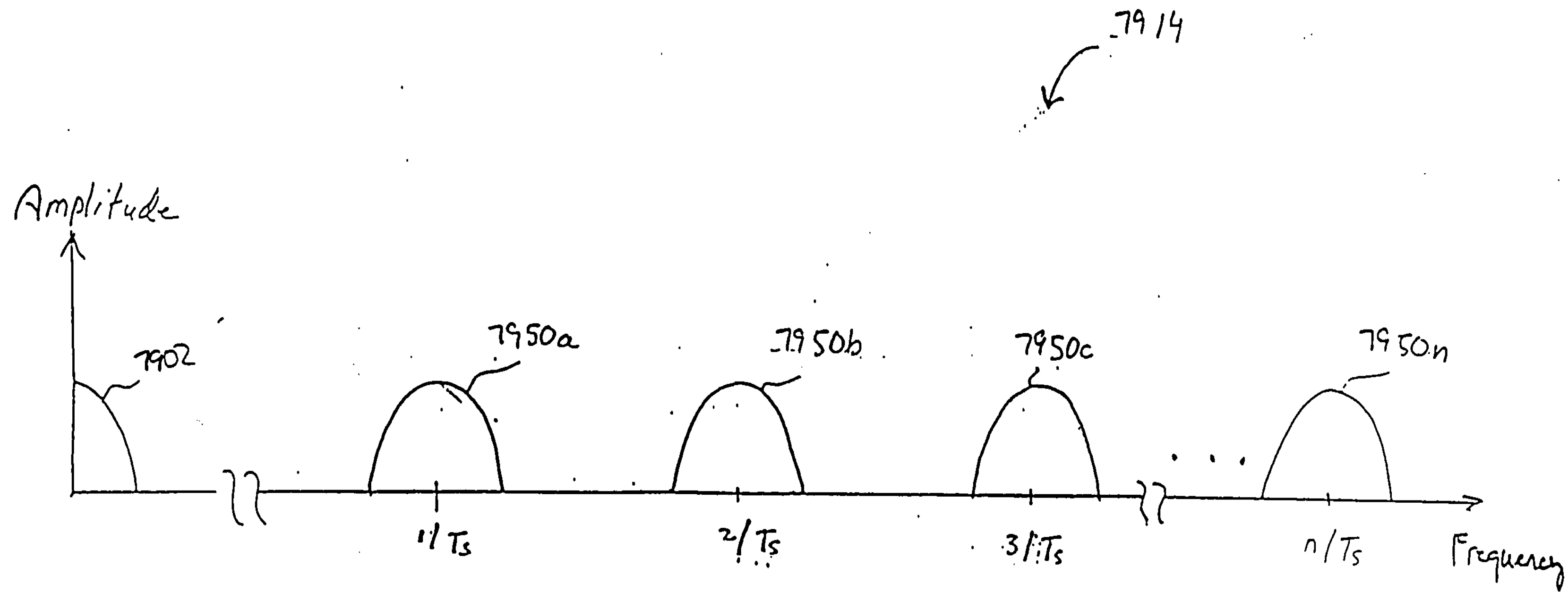
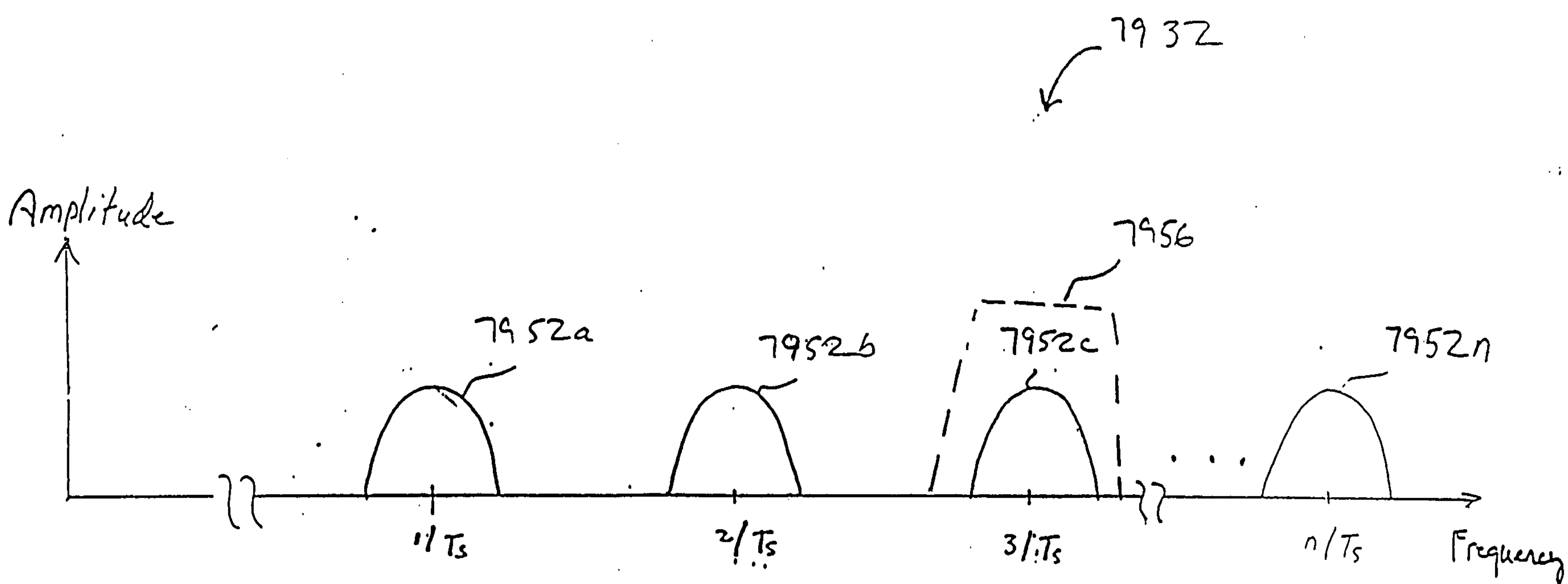


FIG. 79B

09632856 .080400



7932
Amplitude
7952a
7952b
7956
7952c
7952n
1/Ts
2/Ts
3/Ts
n/Ts
Frequency

FIG. 79c

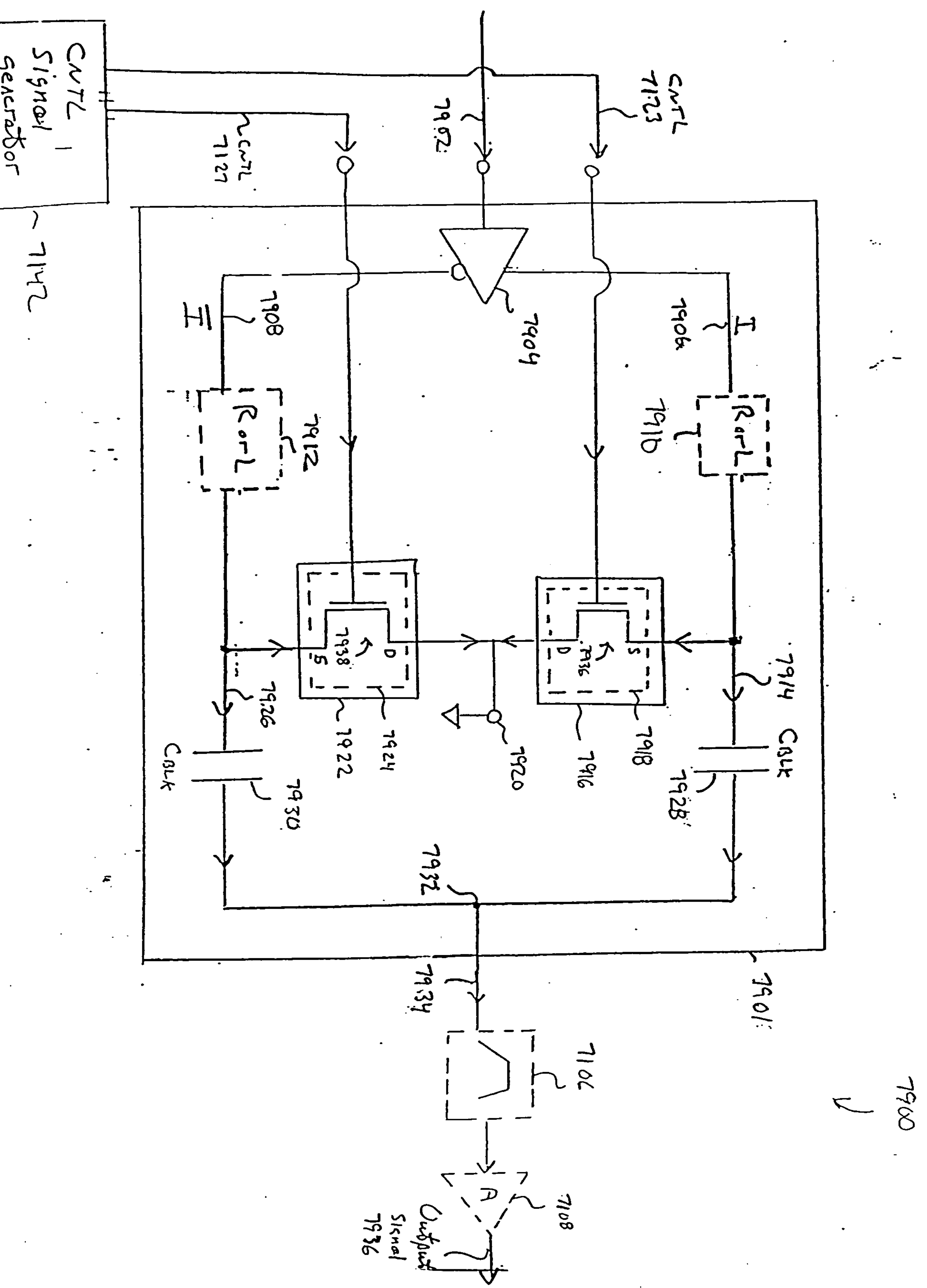


FIG. 79D

09632856.080400

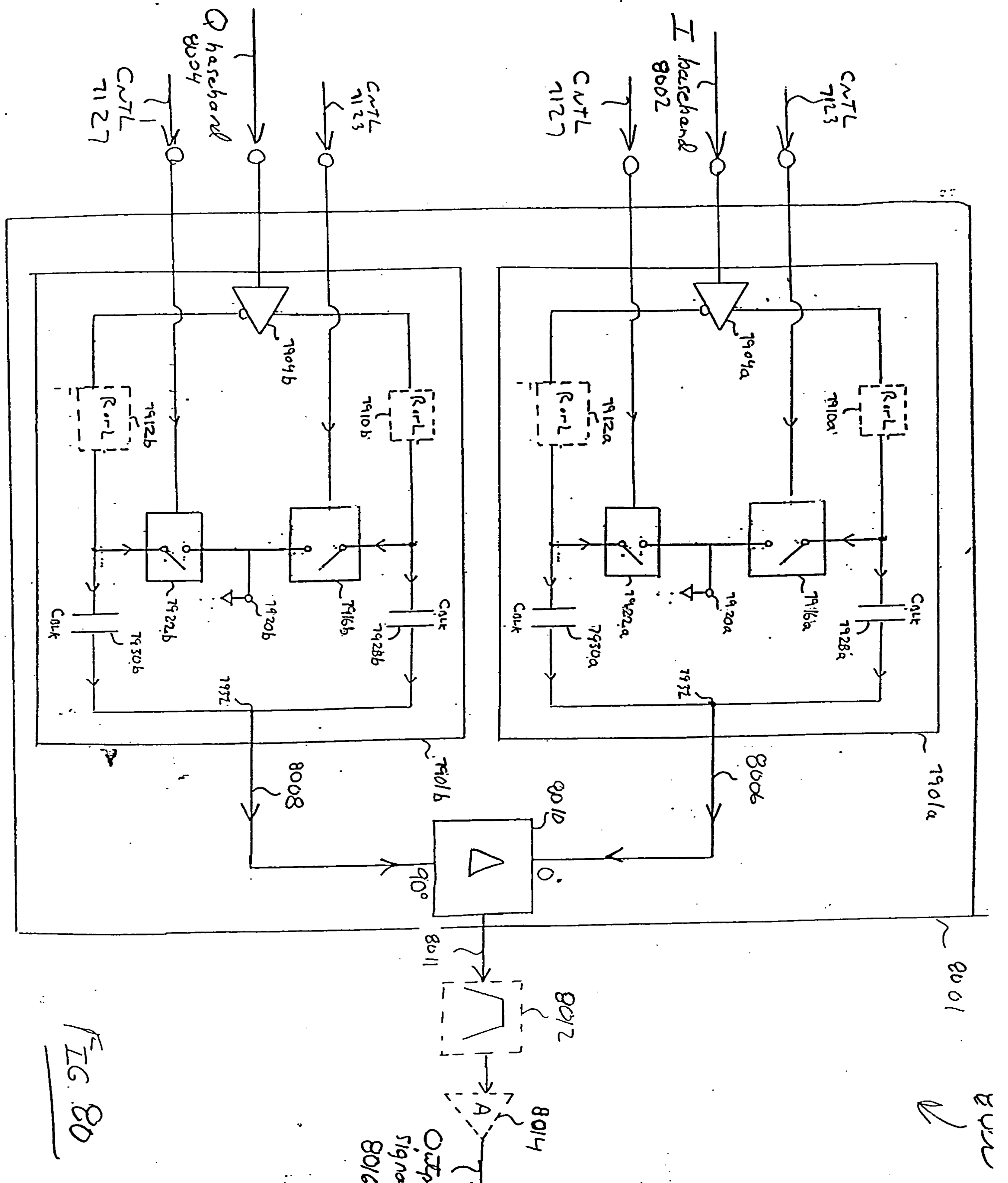

8000
I baseband 8002
Q baseband 8004
CNTL 7123
CNTL 7127
7904a
7904b
R or L
7910a
7910b
7912a
7912b
7916a
7916b
7920a
7920b
7922a
7922b
Cblk
7928a
7928b
7930a
7930b
7932
7901a
7901b
8006
8008
8010
0°
90°
8011
8012
8001
A
8014
Output signal 8016

FIG. 80

FIG. 81A

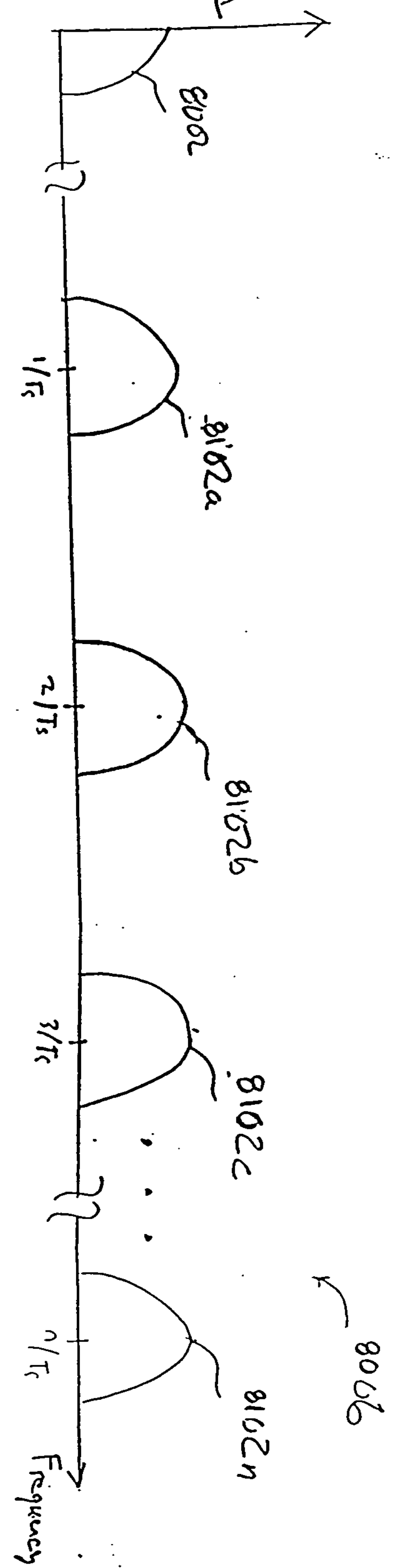


FIG. 81B

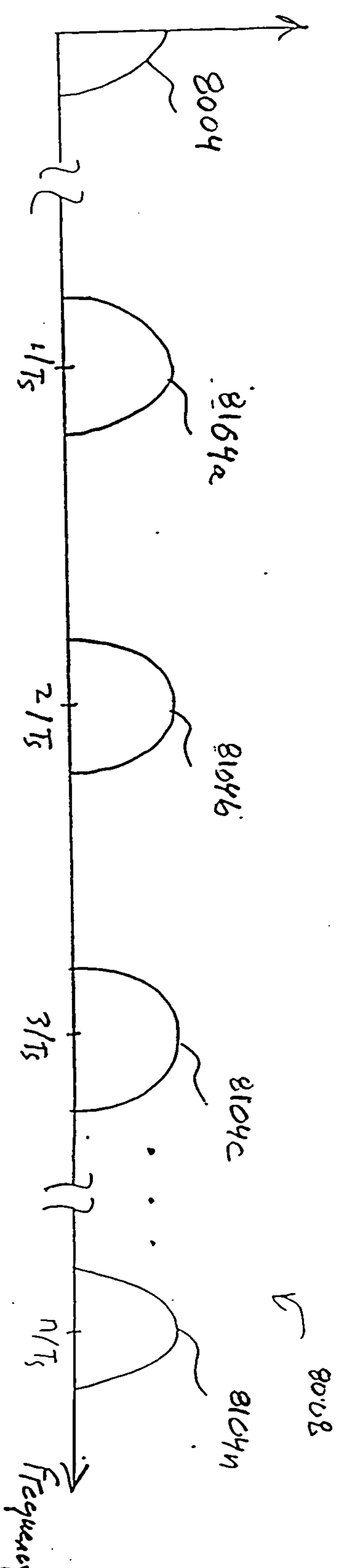
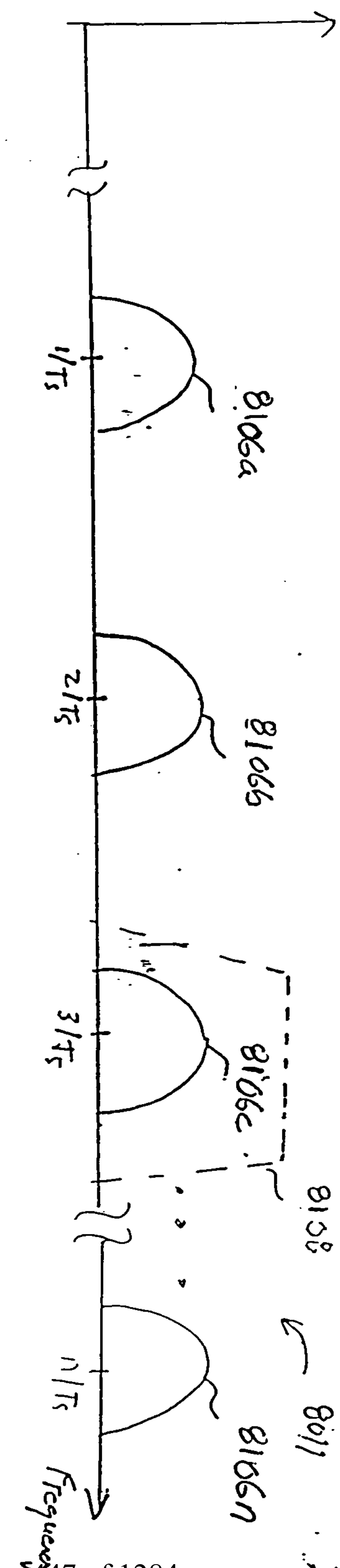
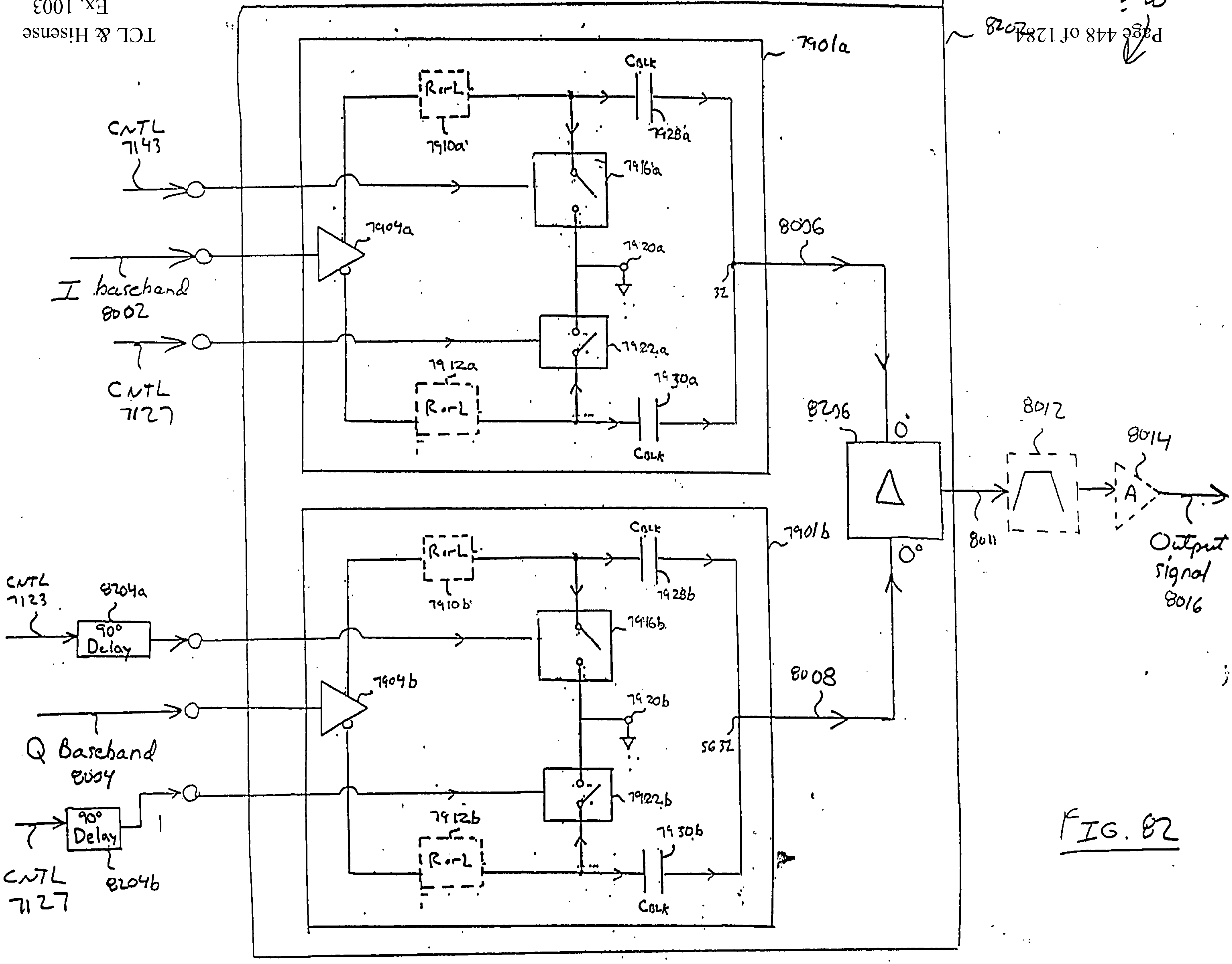


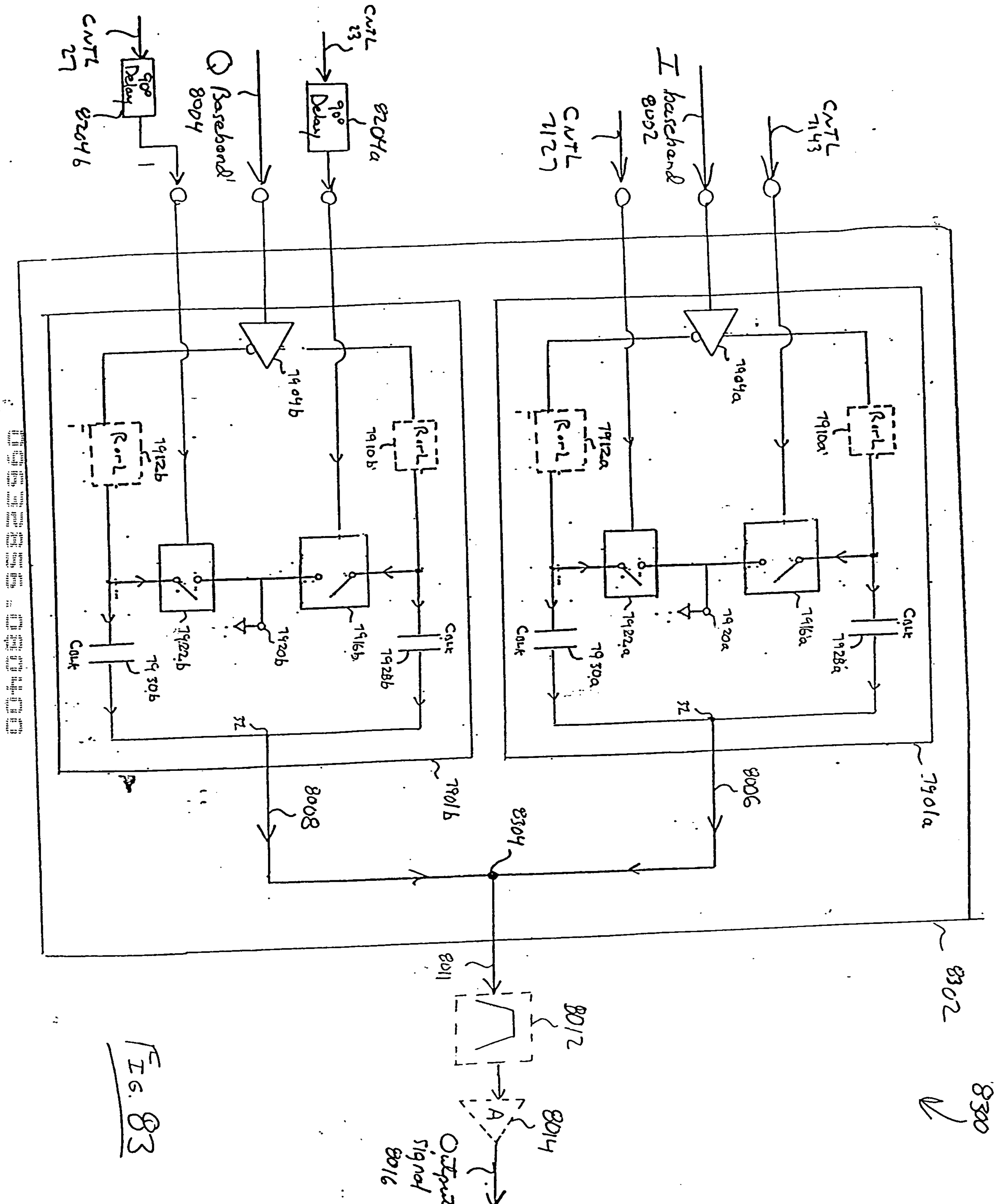
FIG. 81C





CNTL 7143
7910a'
7928a
7916a
7904a
I baseband 8002
7920a
8006
32
7922a
CNTL 7127
7912a
7930a
8206
Calk
Calk
7901a
R or L
R or L
8012
8014
A
Output signal 8016
8011
7901b
CNTL 7123
8204a
90° Delay
7910b'
7928b
7916b
7904b
7920b
8008
Q Baseband 8004
5632
7922b
7912b
7930b
90° Delay
CNTL 7127
8204b
8202

FIG. 82



CNTL 27
90° Delay
8204b
Q baseband' 8004
CNTL 13
90° Delay
8204a
I baseband 8002
CNTL 7127
CNTL 7143
7904b
7904a
R or L
7912b
7910b'
7912a
7910a'
7922b
7916b
7920b
7928b
7930b
7922a
7916a
7920a
7928a
7930a
Cblk
ZL
7901b
7901a
8008
8006
8304
8302
8011
8012
A
8014
Output signal 8016
8300

FIG. 83

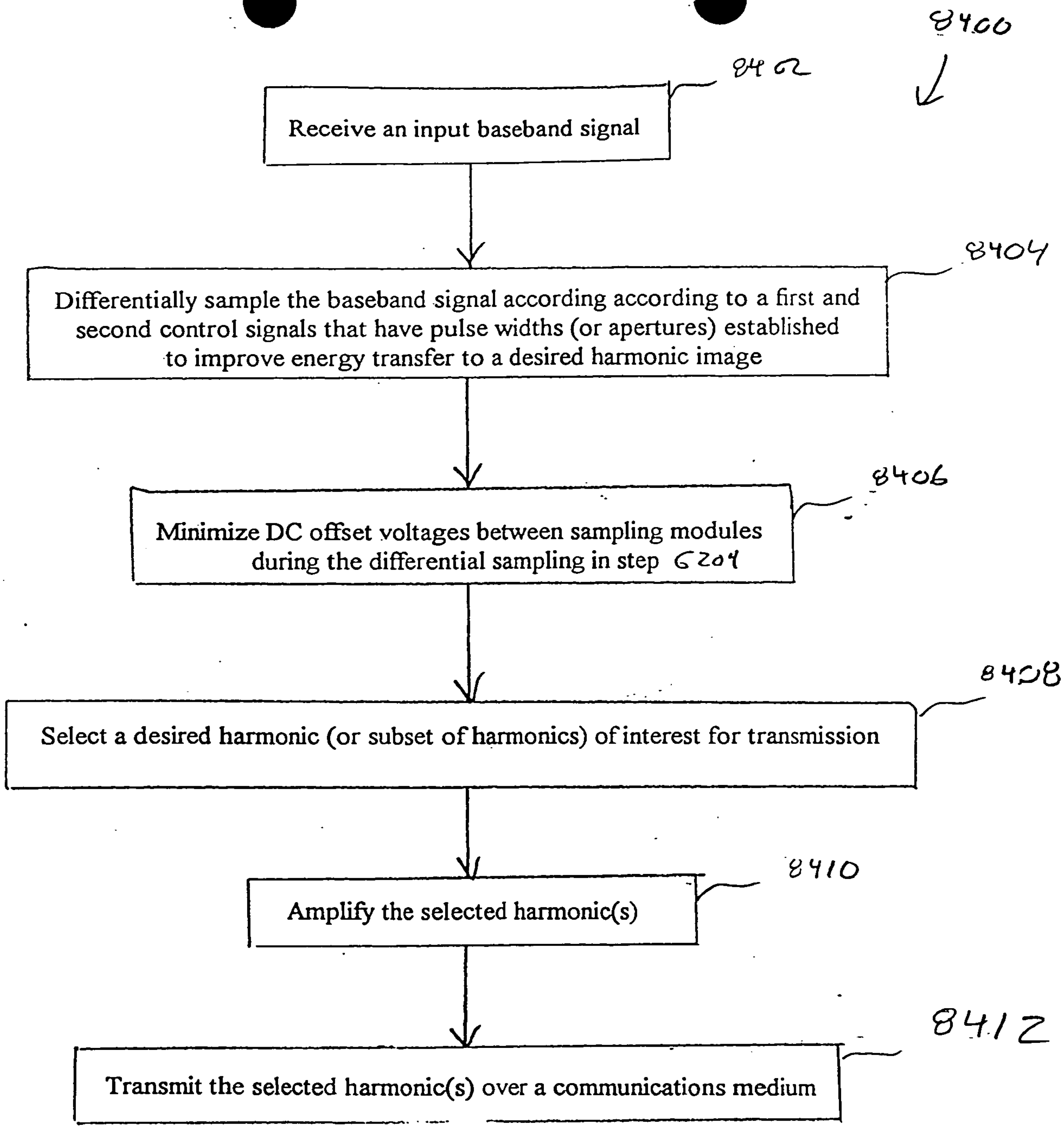

8400
8402
Receive an input baseband signal
8404
Differentially sample the baseband signal according according to a first and second control signals that have pulse widths (or apertures) established to improve energy transfer to a desired harmonic image
8406
Minimize DC offset voltages between sampling modules during the differential sampling in step 6204
8408
Select a desired harmonic (or subset of harmonics) of interest for transmission
8410
Amplify the selected harmonic(s)
8412
Transmit the selected harmonic(s) over a communications medium

FIG. 84

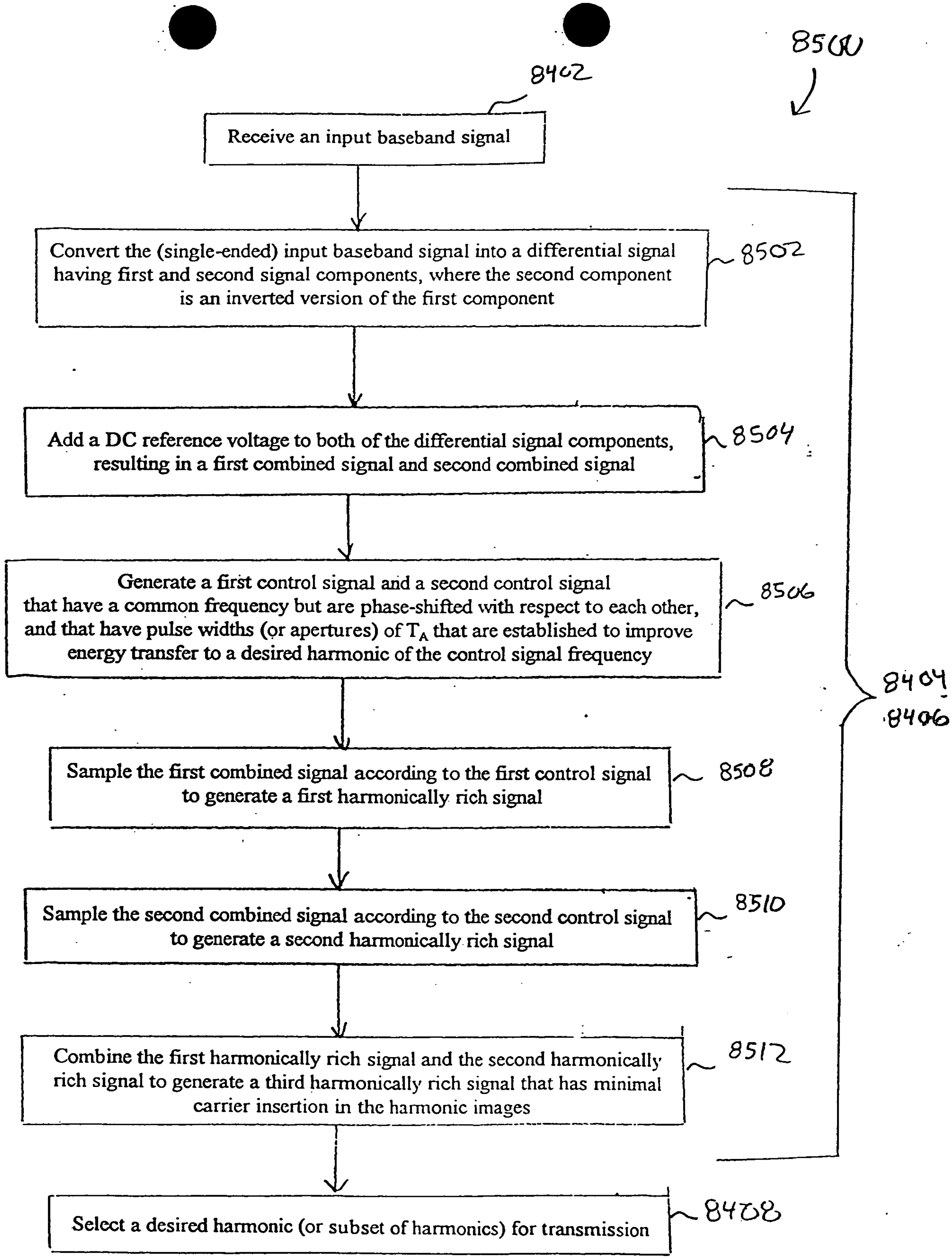

8500
8402
Receive an input baseband signal
Convert the (single-ended) input baseband signal into a differential signal having first and second signal components, where the second component is an inverted version of the first component
8502
Add a DC reference voltage to both of the differential signal components, resulting in a first combined signal and second combined signal
8504
Generate a first control signal and a second control signal that have a common frequency but are phase-shifted with respect to each other, and that have pulse widths (or apertures) of T_A that are established to improve energy transfer to a desired harmonic of the control signal frequency
8506
8404
8406
Sample the first combined signal according to the first control signal to generate a first harmonically rich signal
8508
Sample the second combined signal according to the second control signal to generate a second harmonically rich signal
8510
Combine the first harmonically rich signal and the second harmonically rich signal to generate a third harmonically rich signal that has minimal carrier insertion in the harmonic images
8512
Select a desired harmonic (or subset of harmonics) for transmission
8408

FIG. 85

8600

Receive an input baseband signal — 8402

Convert the (single-ended) input baseband signal into a differential signal having first and second signal components, where the second component is an inverted version of the first component — 8602

Generate a first control signal and a second control signal that have a common frequency but are phase-shifted with respect to each other, and that have pulse widths (or apertures) of T_A that are established to improve energy transfer to a desired harmonic of the control signal frequency — 8604

Shunt the first differential signal component to ground according to the first control signal to generate a first harmonically rich signal — 8606

Shunt the second differential signal component to ground according to the second control signal to generate a second harmonically rich signal — 8608

Combine the first harmonically rich signal and the second harmonically rich signal to generate a third harmonically rich signal that has minimal carrier insertion in the harmonic images — 8610

8404, 8406

Select a desired harmonic (or subset of harmonics) for transmission — 8408

FIG. 86

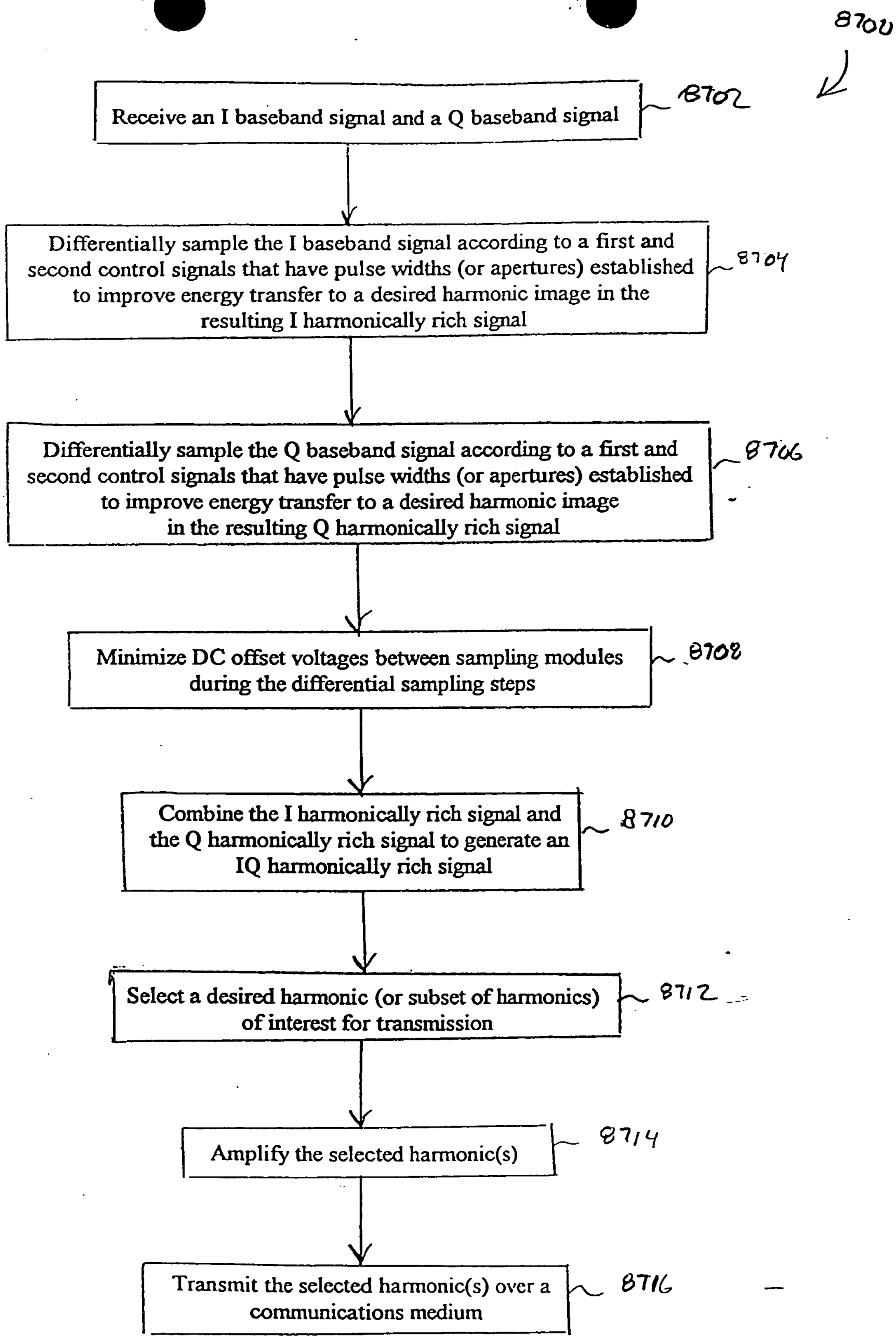

8700
Receive an I baseband signal and a Q baseband signal
8702
Differentially sample the I baseband signal according to a first and second control signals that have pulse widths (or apertures) established to improve energy transfer to a desired harmonic image in the resulting I harmonically rich signal
8704
Differentially sample the Q baseband signal according to a first and second control signals that have pulse widths (or apertures) established to improve energy transfer to a desired harmonic image in the resulting Q harmonically rich signal
8706
Minimize DC offset voltages between sampling modules during the differential sampling steps
8708
Combine the I harmonically rich signal and the Q harmonically rich signal to generate an IQ harmonically rich signal
8710
Select a desired harmonic (or subset of harmonics) of interest for transmission
8712
Amplify the selected harmonic(s)
8714
Transmit the selected harmonic(s) over a communications medium
8716

FIG. 87

8800

Receive an I baseband signal and a Q baseband signal 8802

↓

Differentially shunt the I baseband signal to ground according to first and second control signals that have pulse widths (or apertures) established to improve energy transfer to a desired harmonic image in the resulting I harmonically rich signal 8804

↓

Differentially shunt the Q baseband signal to ground according to first and second control signals that have pulse widths (or apertures) established to improve energy transfer to a desired harmonic image in the resulting Q harmonically rich signal 8806

↓

Combine the I harmonically rich signal and the Q harmonically rich signal to generate an IQ harmonically rich signal 8808

↓

Select a desired harmonic (or subset of harmonics) of interest for transmission 8810

↓

Amplify the selected harmonic(s) 8812

↓

Transmit the selected harmonic(s) over a communications medium 8814

FIG. 88

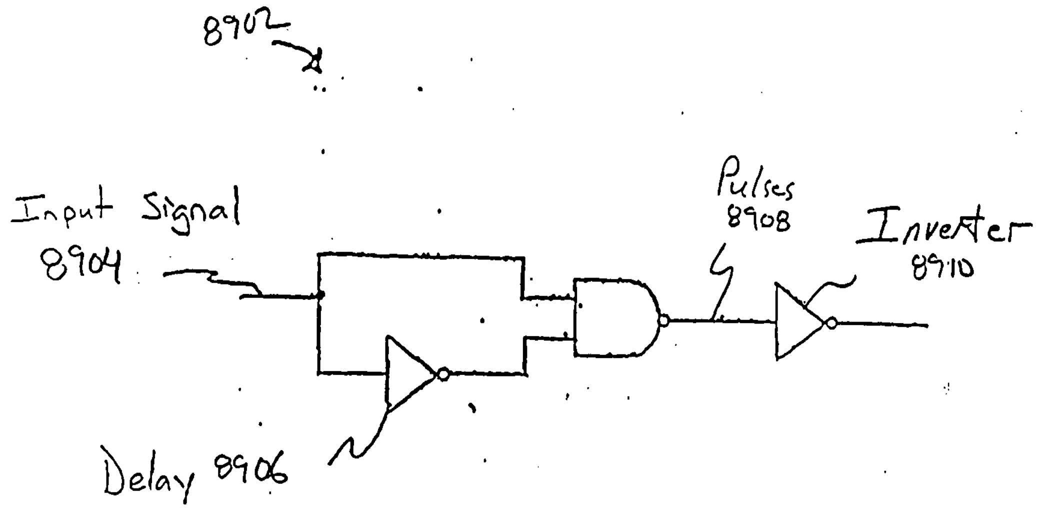


FIG. 89A

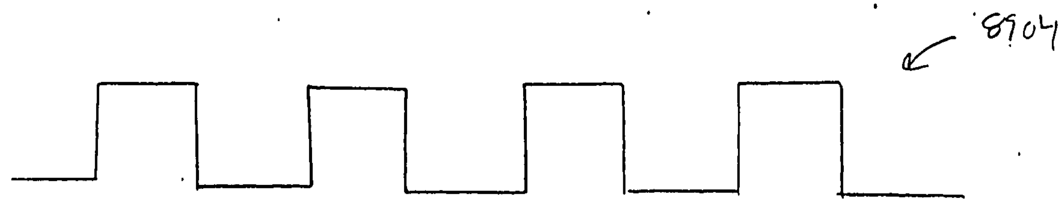


FIG. 89B

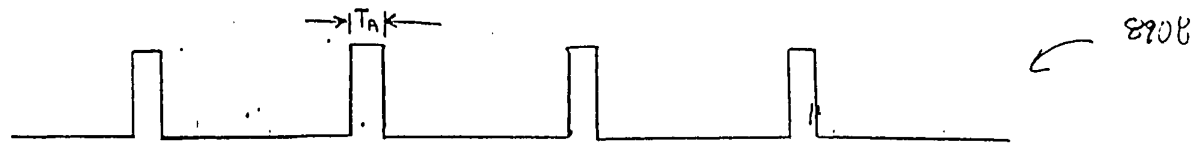
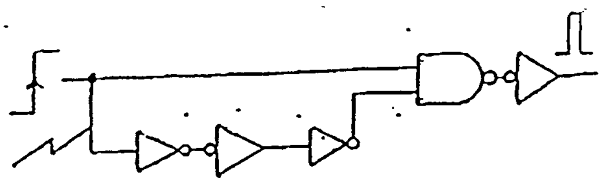


FIG. 89C

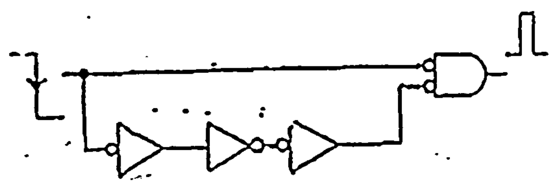
8912



A. rising edge pulse generator

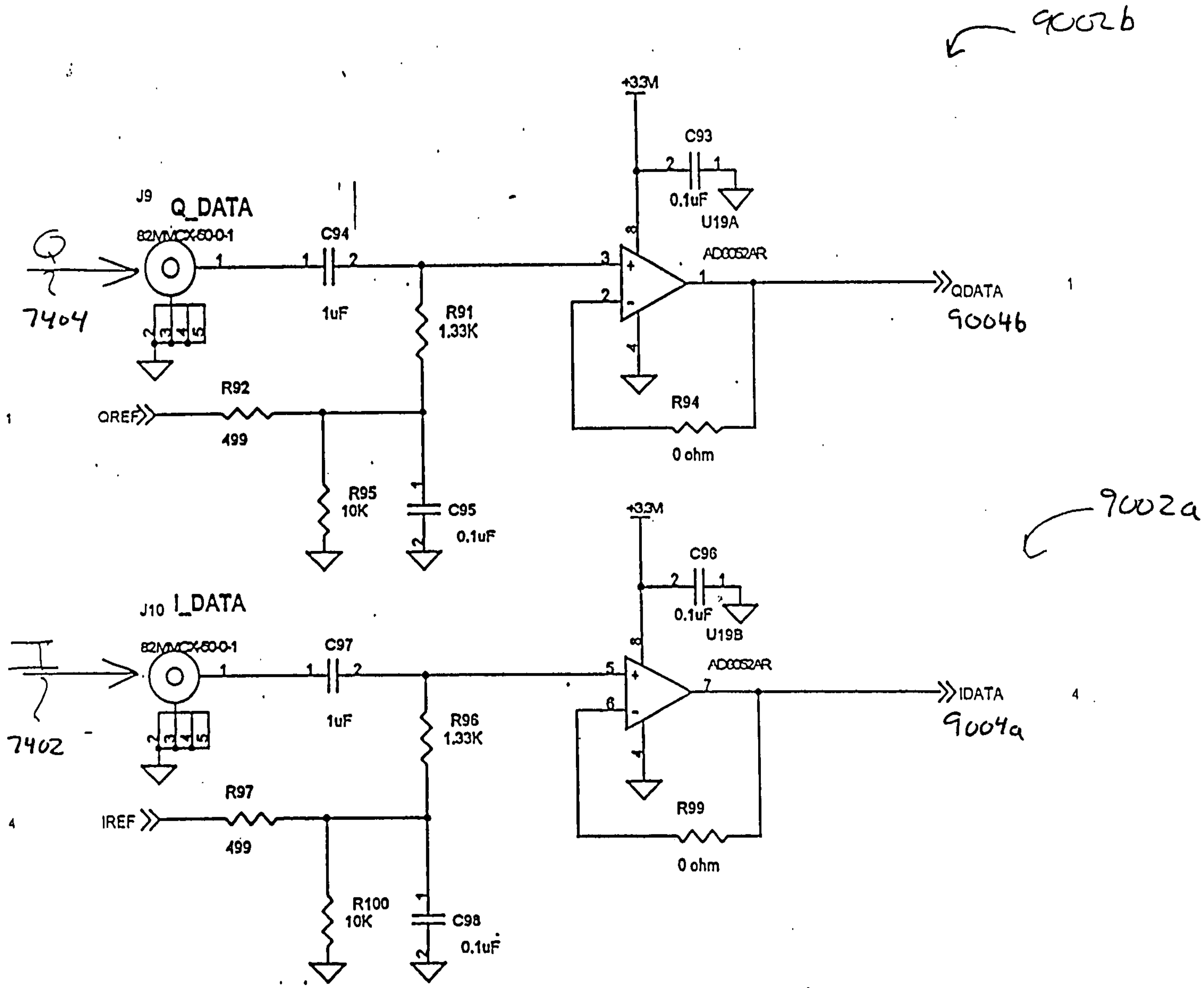
FIG. 89D

8916



B. falling-edge pulse generator

FIG. 89E



9002b
+3.3M
C93
2
1
0.1uF
U19A
J9
Q_DATA
82MMCX-50-0-1
Q
7404
1
C94
1
2
1uF
R91
1.33K
3
2
8
4
AD8052AR
1
QDATA
9004b
QREF
R92
499
R94
0 ohm
R95
10K
1
C95
2
0.1uF
9002a
+3.3M
C96
2
1
0.1uF
U19B
J10
I_DATA
82MMCX-50-0-1
I
7402
1
C97
1
2
1uF
R96
1.33K
5
6
8
4
AD8052AR
7
IDATA
9004a
IREF
R97
499
R99
0 ohm
R100
10K
1
C98
2
0.1uF

FIG. 90A

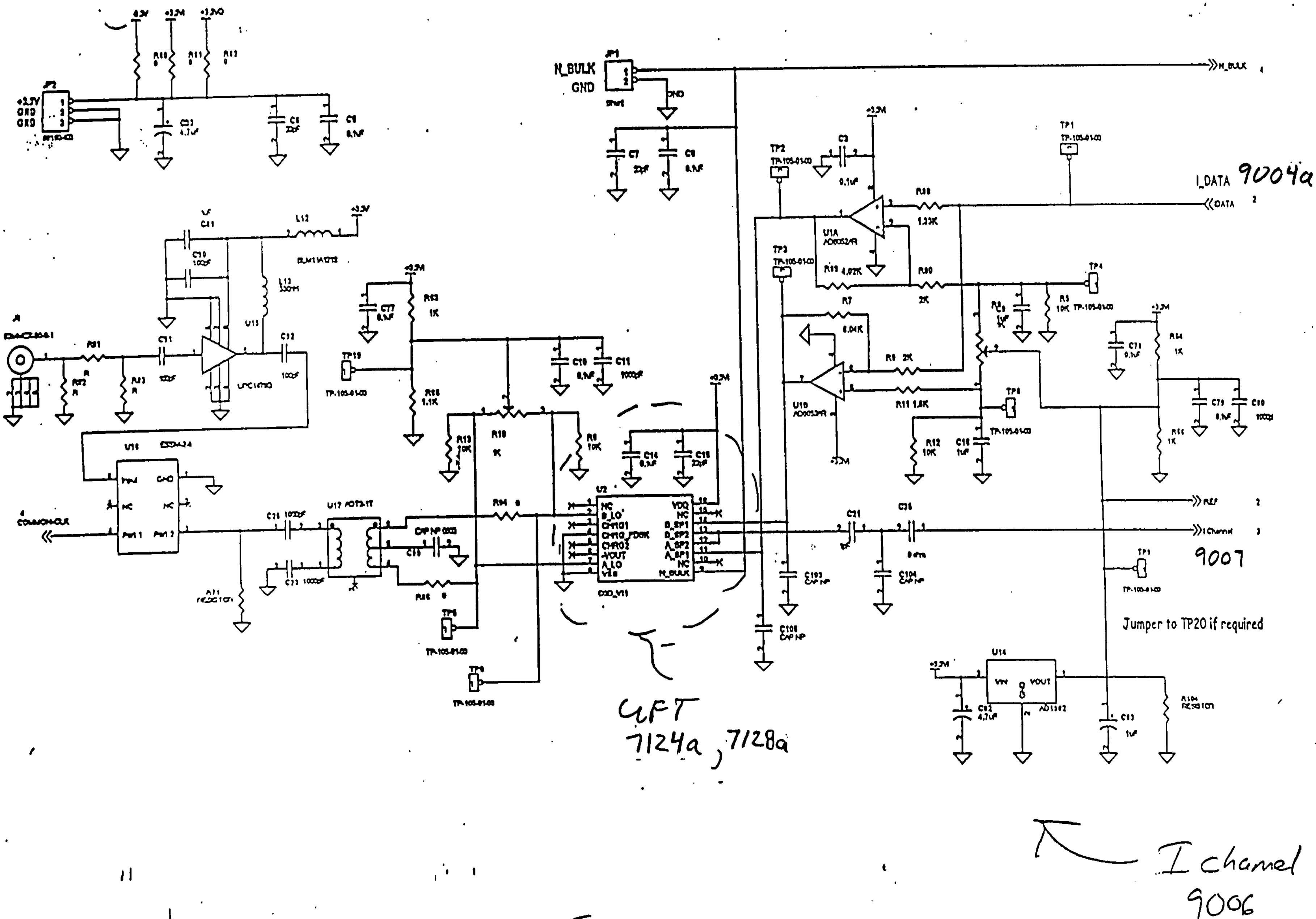
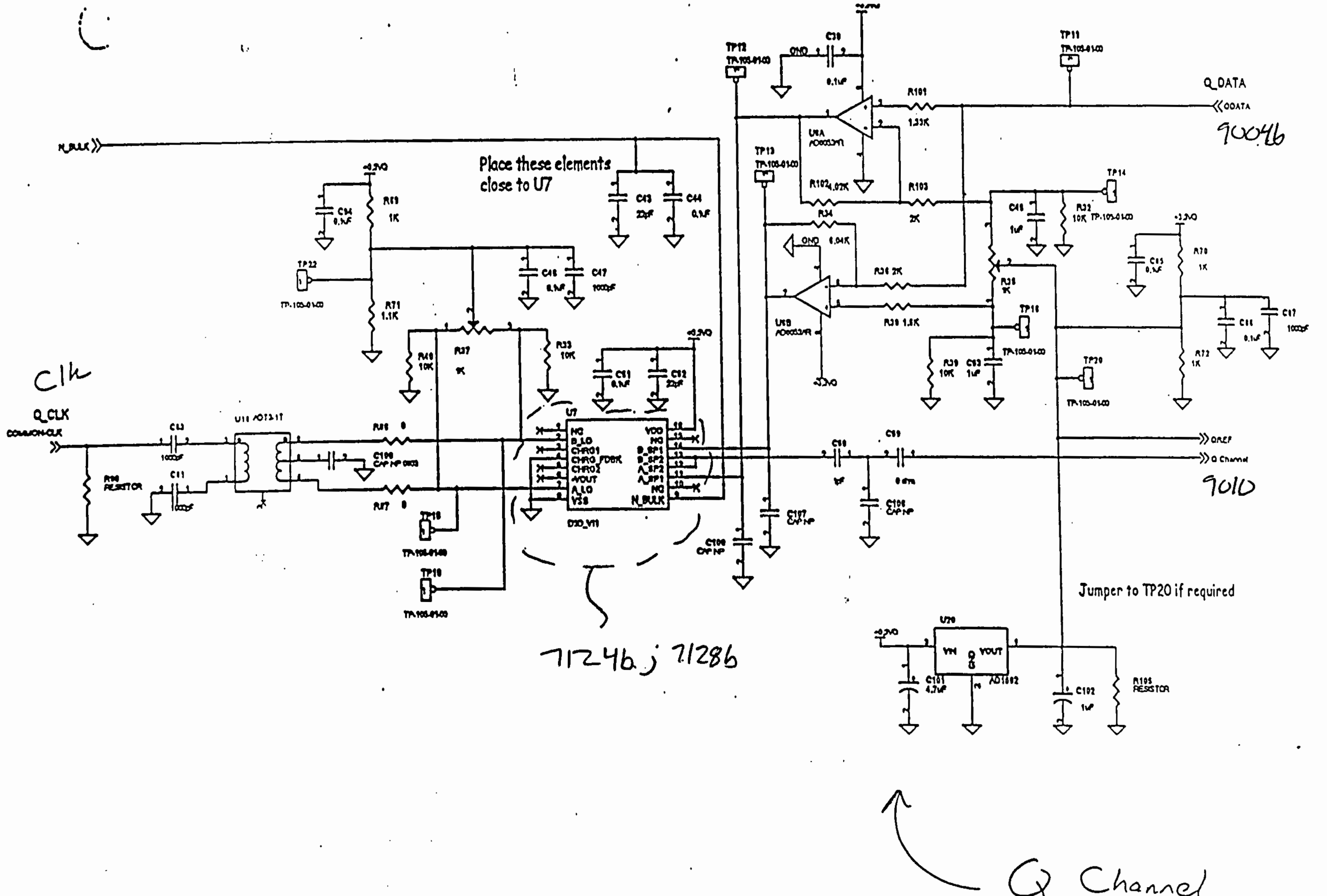

N_BULK
GND
I_DATA 9004a
9007
Jumper to TP20 if required
GFT
7124a, 7128a
I chanel
9006

FIG. 90B



Place these elements close to U7
Q_DATA
9004b
Clk
Q_CLK
COMMON-CLK
U7
NC
B_LO
CHRG1
CHRG_FDBK
CHRG2
AVOUT
A_LO
VSS
VDD
B_SP1
B_SP2
A_SP2
A_SP1
N_BULK
D2D_V11
N_BULK
Q Channel
9010
Jumper to TP20 if required
U20
VIN
VOUT
AD1582
7124b; 7128b
Q Channel
9008

FIG. 90C

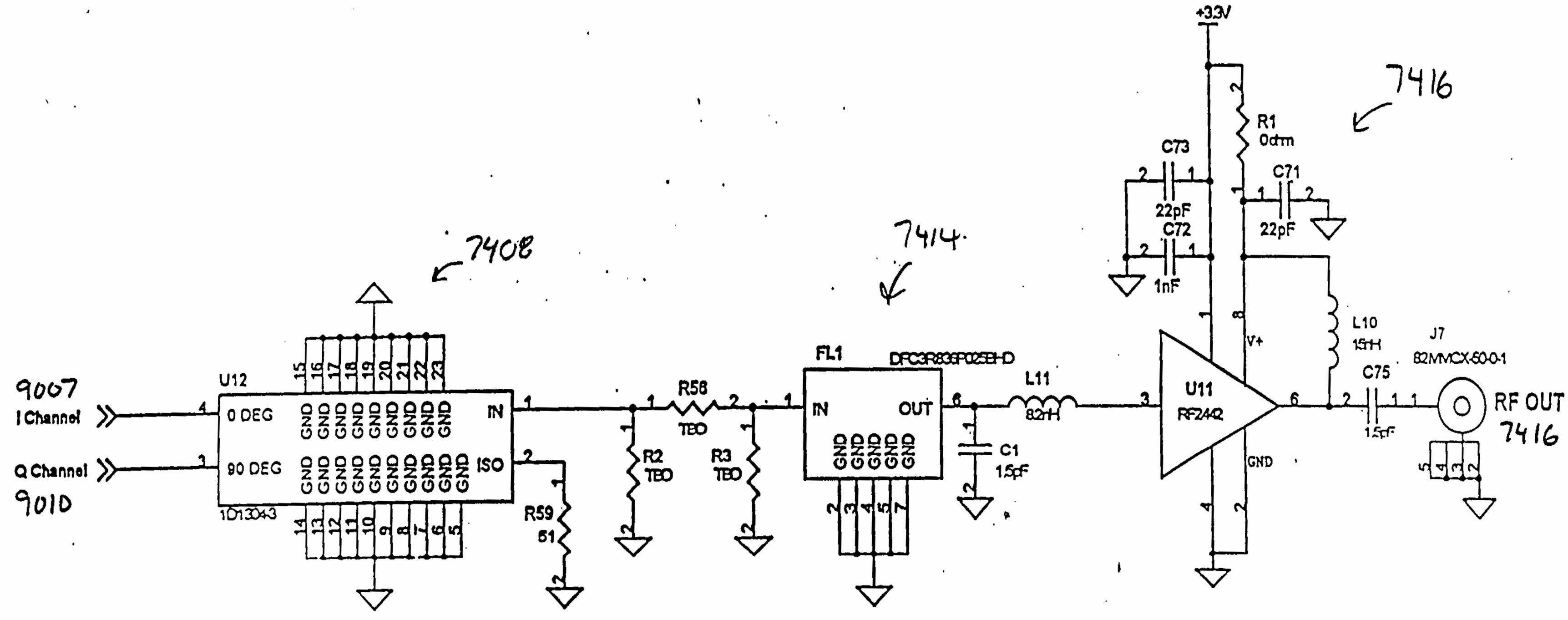


FIG. 90D

09632356 .080400

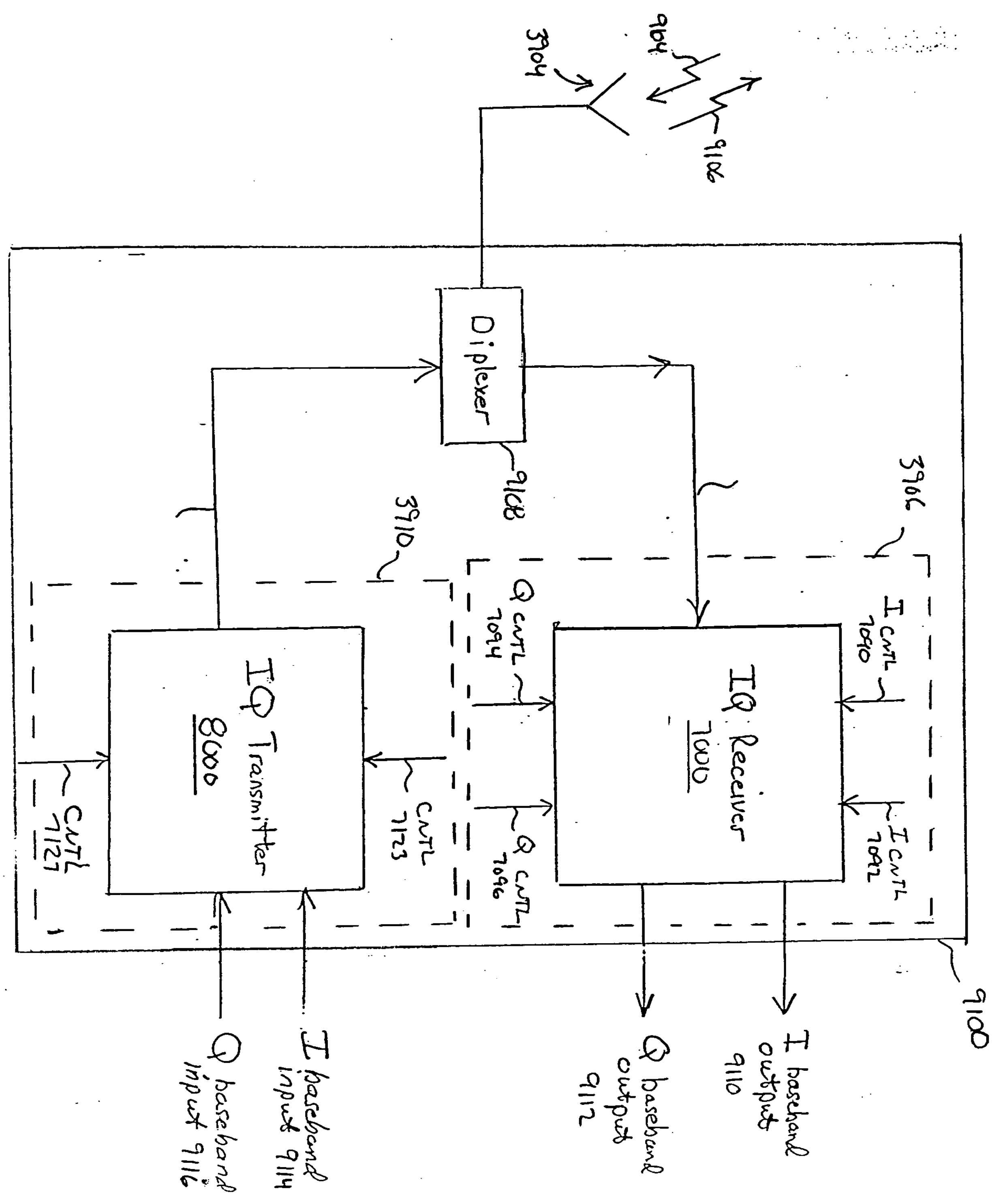
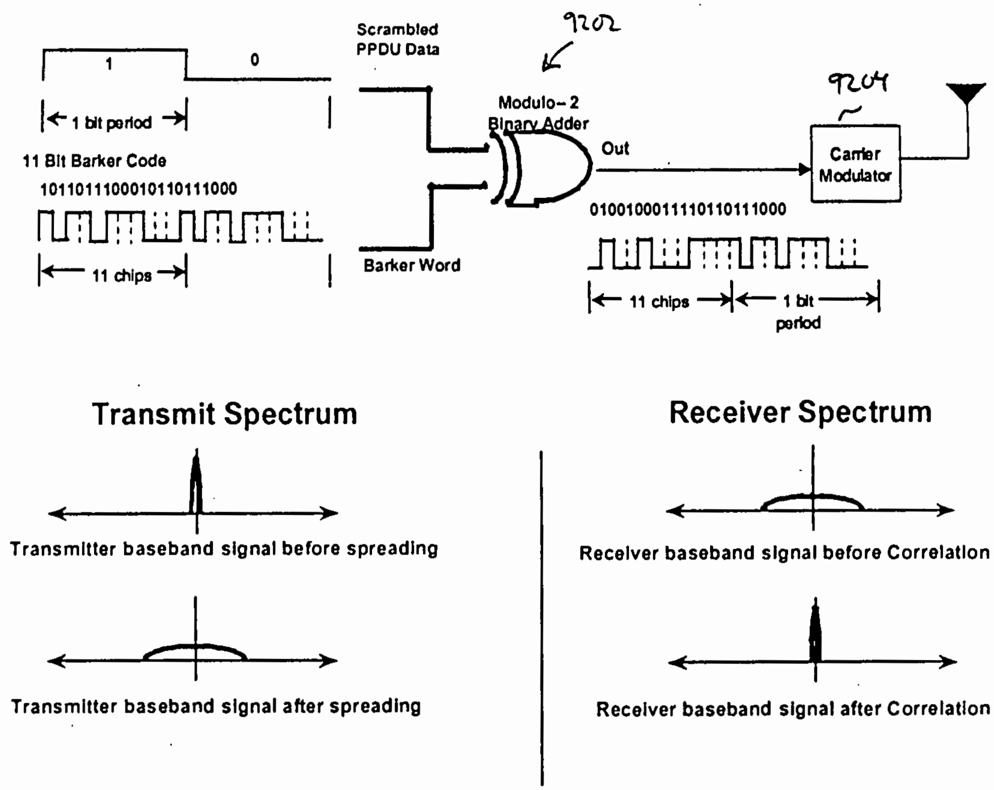

9104
3904
9106
Diplexer
9108
3910
3906
IQ Transmitter
8000
CNTL
7127
CNTL
7123
Q CNTL
7094
IQ Receiver
7000
I CNTL
7090
Q CNTL
7096
I CNTL
7092
9100
I baseband output 9110
Q baseband output 9112
I baseband input 9114
Q baseband input 9116

FIG. 91



9202
9204
Scrambled
PPDU Data
1
0
1 bit period
11 Bit Barker Code
10110111000101101110000
11 chips
Barker Word
Modulo-2
Binary Adder
Out
01001000111101101111000
11 chips
1 bit
period
Carrier
Modulator
Transmit Spectrum
Transmitter baseband signal before spreading
Transmitter baseband signal after spreading
Receiver Spectrum
Receiver baseband signal before Correlation
Receiver baseband signal after Correlation

FIG 92

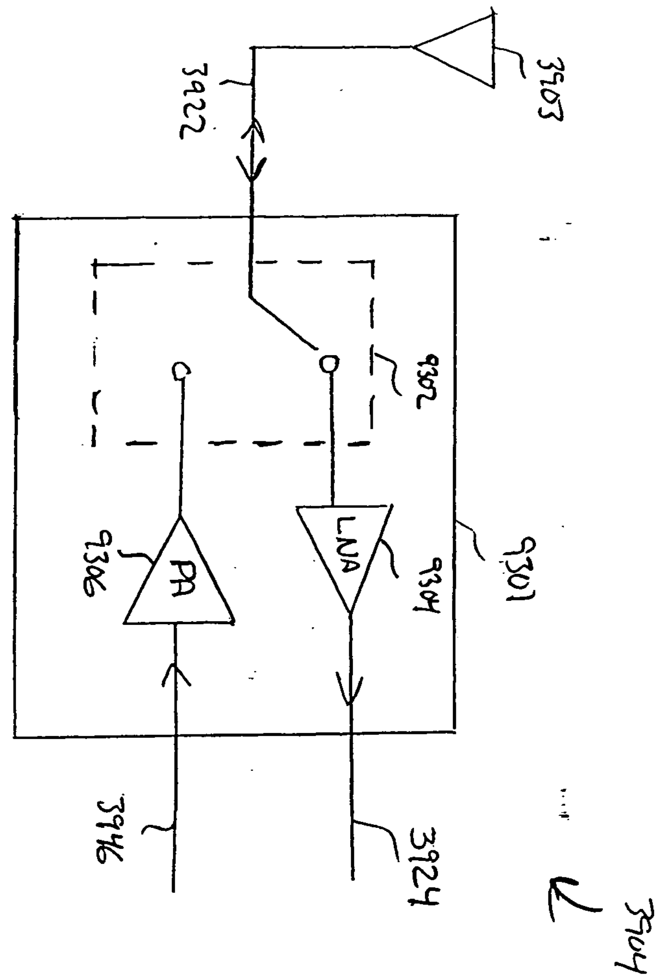
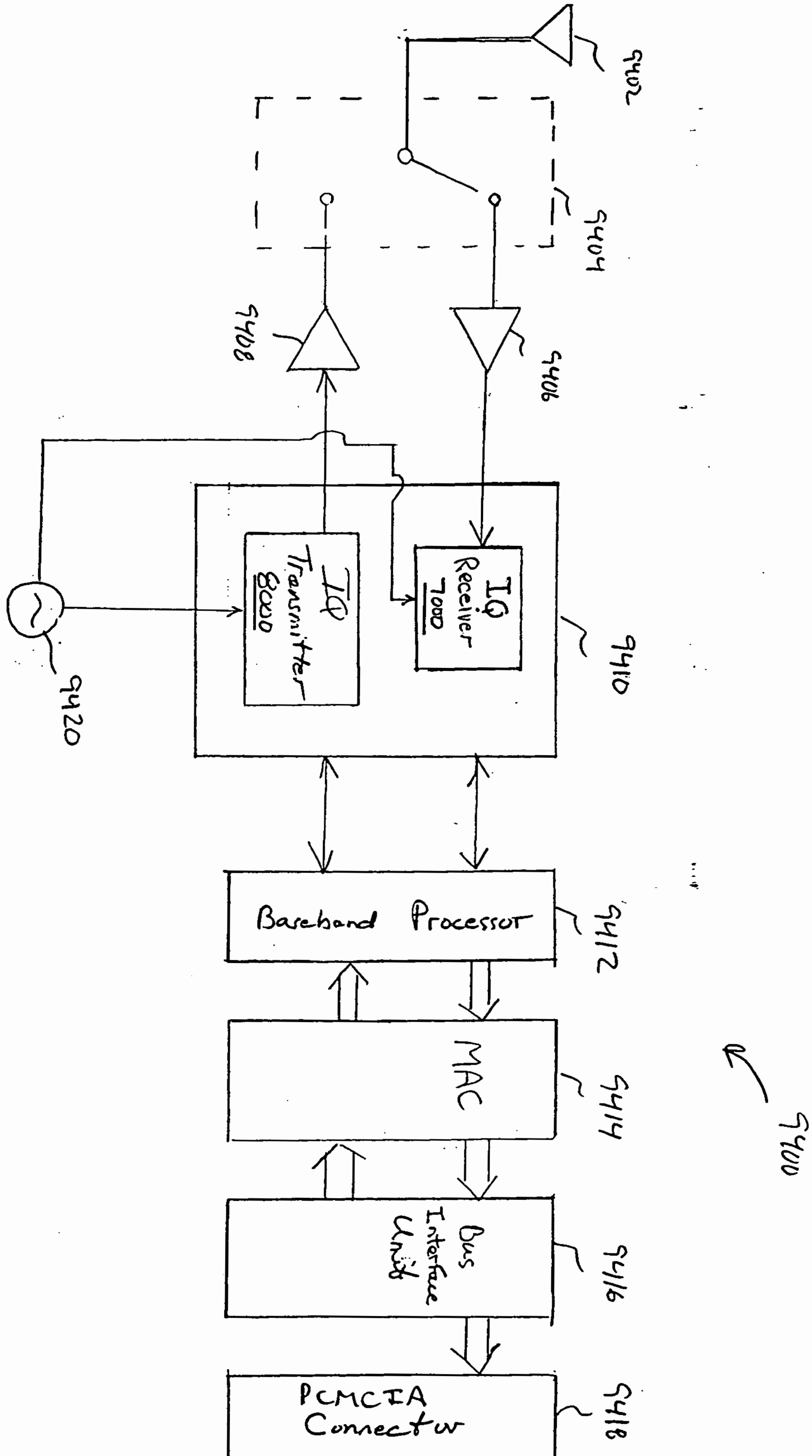


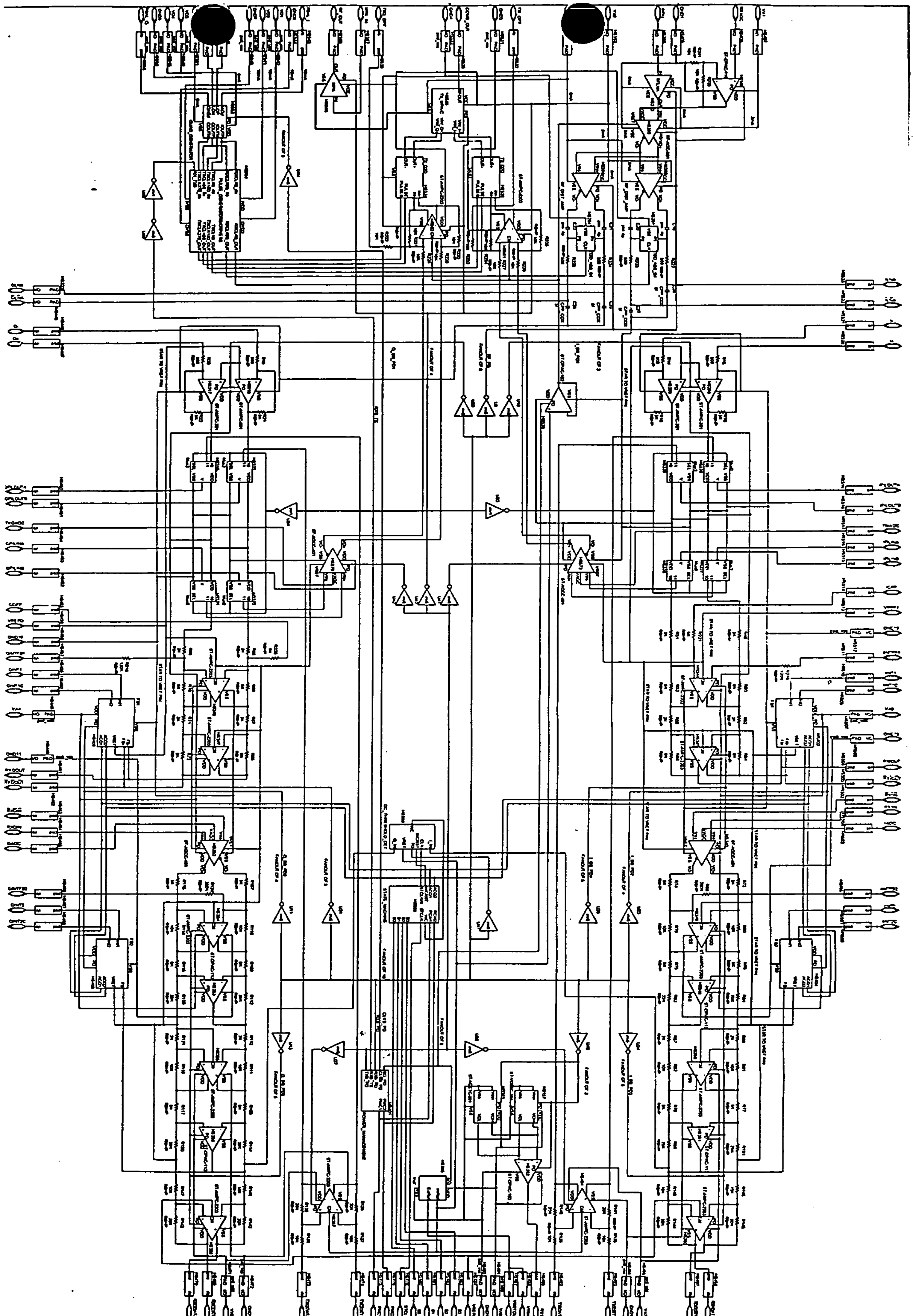
FIG. 93



9402
9404
9406
9408
IQ Transmitter 8000
IQ Receiver 7000
9410
9420
Baseband Processor
9412
MAC
9414
Bus Interface Unit
9416
PCMCIA Connector
9418
9400

FIG. 94

FIG. 95A



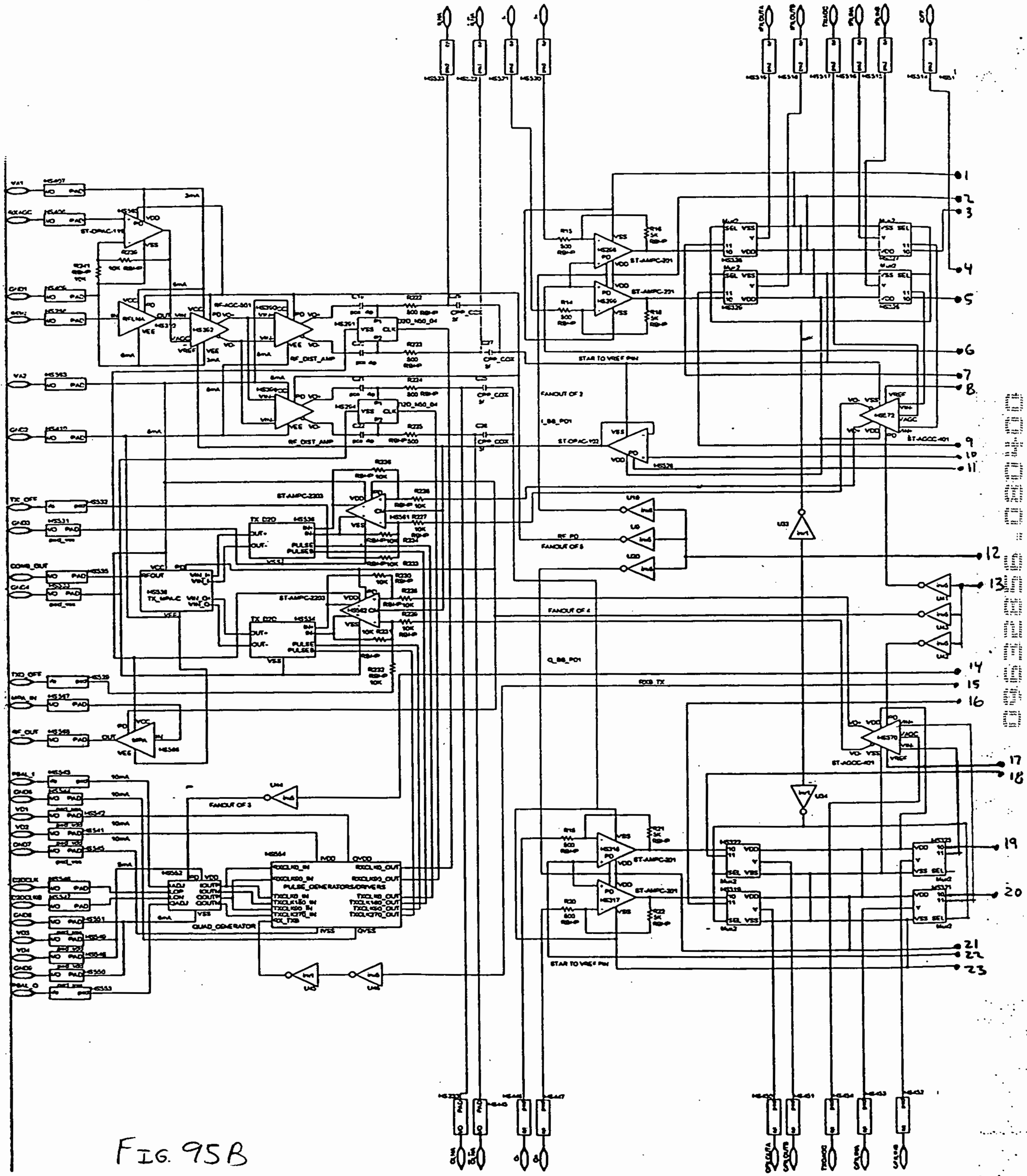


FIG. 95B

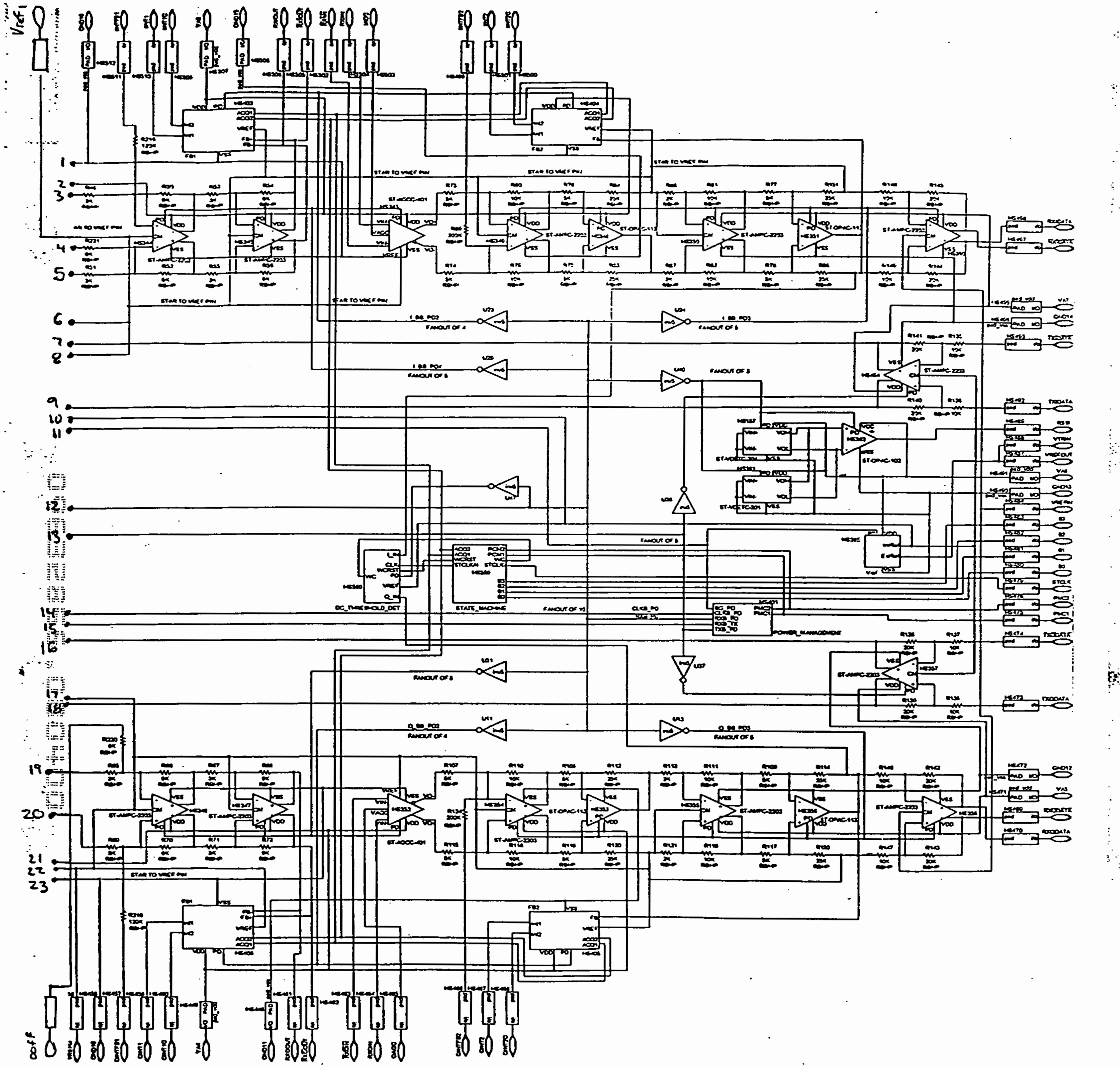

Vref1
STAR TO VREF PIN
FANOUT OF 4
FANOUT OF 5
FANOUT OF 8
FANOUT OF 15
DC_THRESHOLD_DET
STATE_MACHINE
POWER_MANAGEMENT
ST-AGCC-401
ST-AMPC-2203
ST-OPAC-112
ST-OPAC-102
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
ref

FIG. 95C

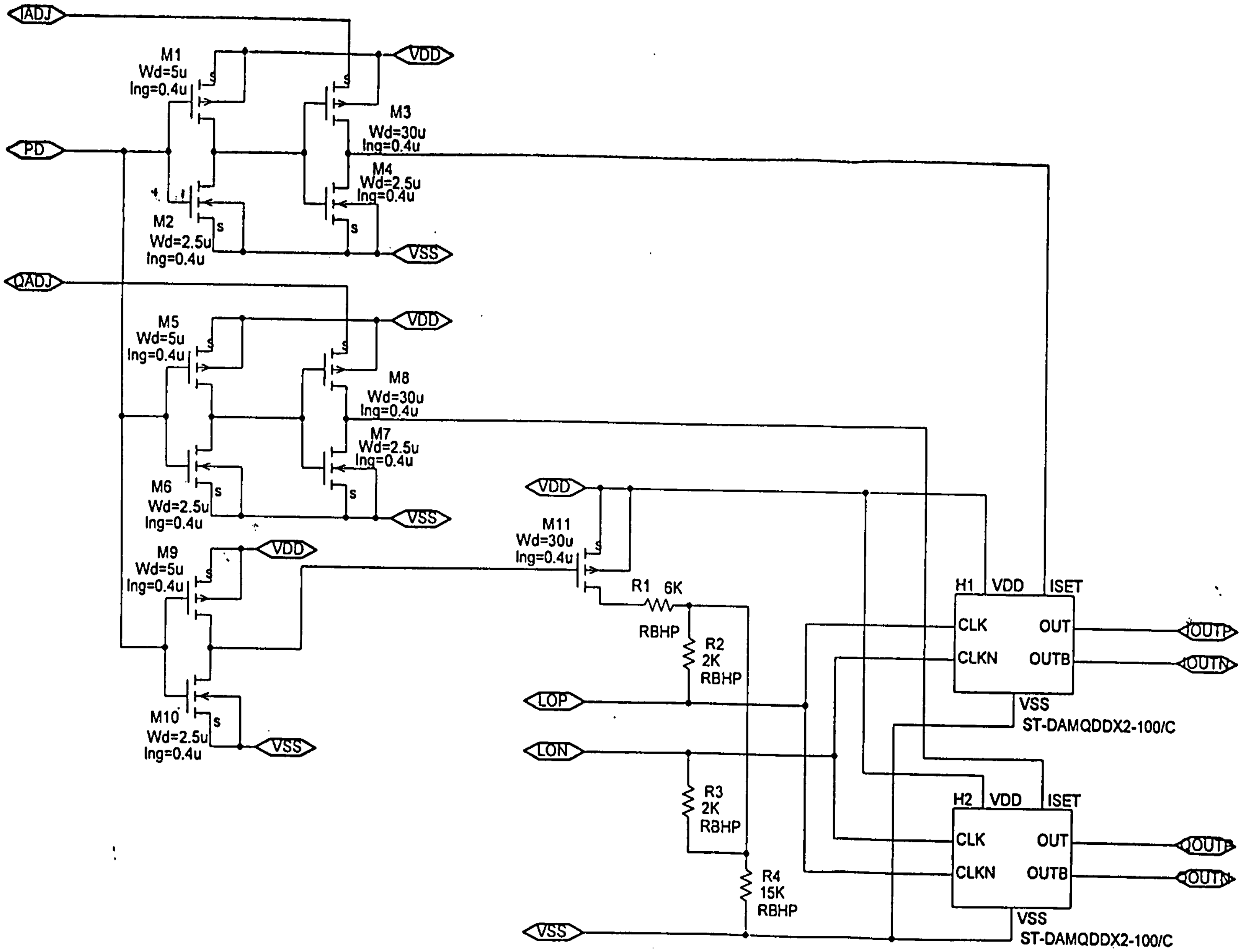

IADJ
VDD
M1
Wd=5u
lng=0.4u
M3
Wd=30u
lng=0.4u
PD
M4
Wd=2.5u
lng=0.4u
M2
Wd=2.5u
lng=0.4u
VSS
QADJ
VDD
M5
Wd=5u
lng=0.4u
M8
Wd=30u
lng=0.4u
M7
Wd=2.5u
lng=0.4u
M6
Wd=2.5u
lng=0.4u
VSS
VDD
M11
Wd=30u
lng=0.4u
M9
Wd=5u
lng=0.4u
VDD
R1 6K
RBHP
R2
2K
RBHP
M10
Wd=2.5u
lng=0.4u
VSS
LOP
LON
R3
2K
RBHP
R4
15K
RBHP
VSS
H1 VDD ISET
CLK OUT
CLKN OUTB
VSS
ST-DAMQDDX2-100/C
IOUTP
IOUTN
H2 VDD ISET
CLK OUT
CLKN OUTB
VSS
ST-DAMQDDX2-100/C
QOUTP
QOUTN

FIG. 96

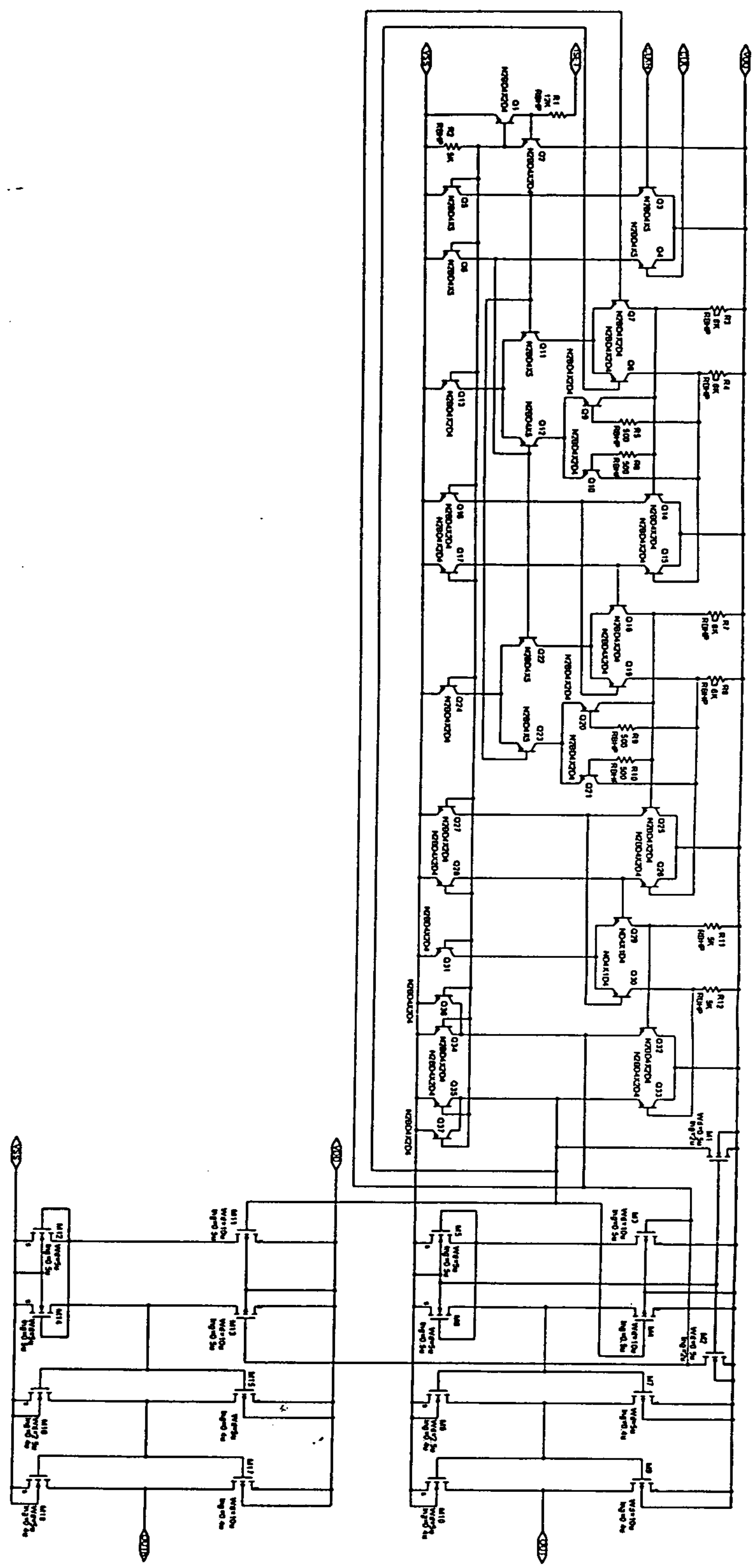


FIG. 17

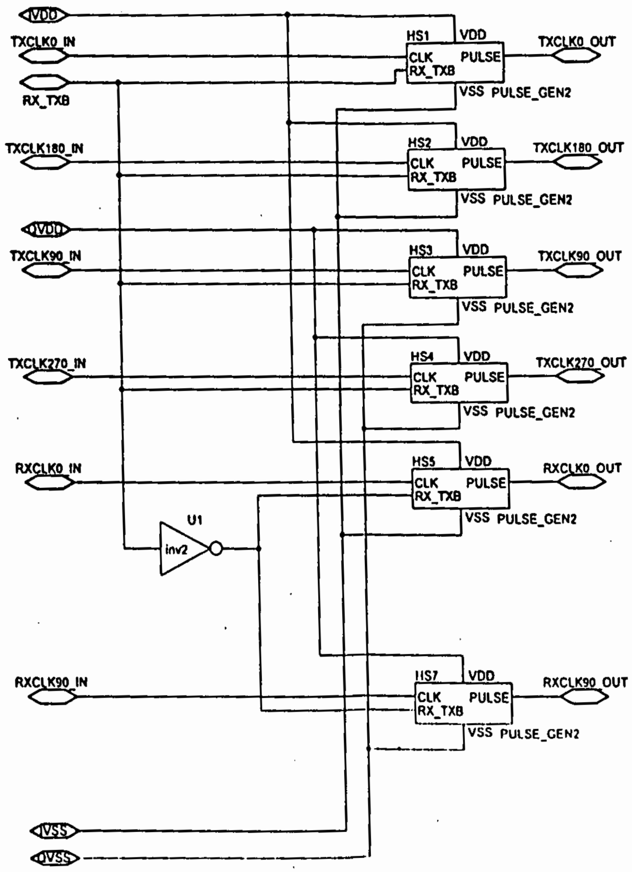


FIG. 98

09632856 .080400

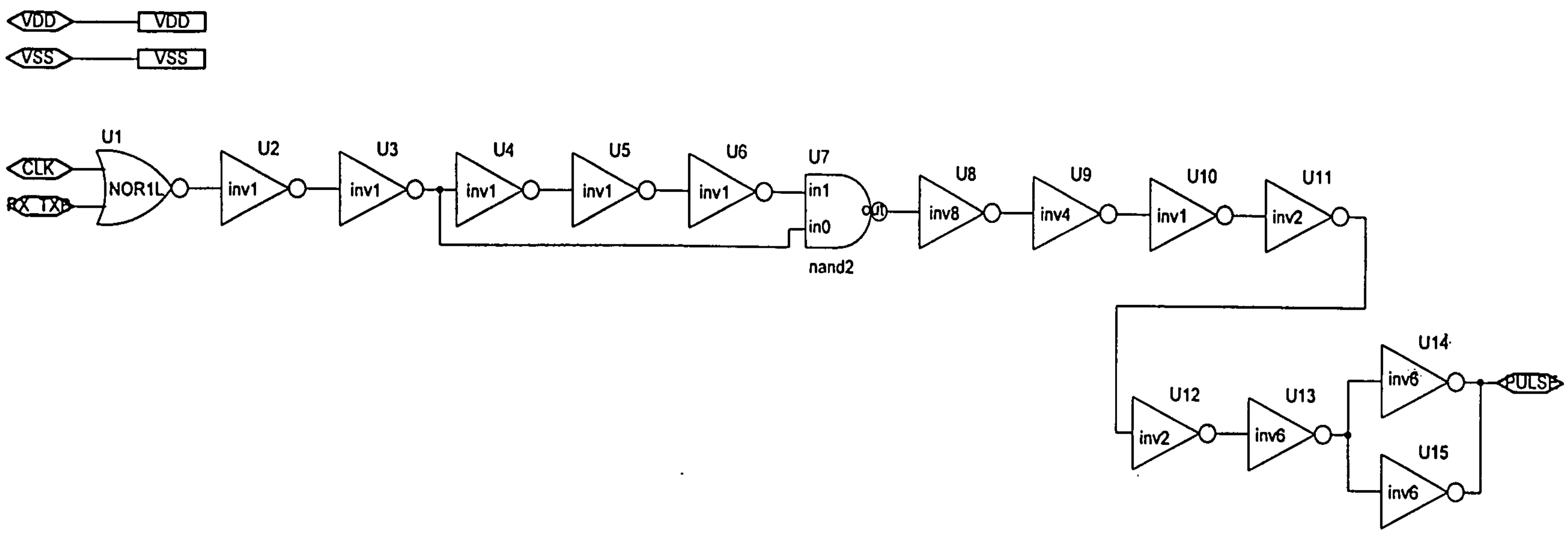

VDD
VDD
VSS
VSS
CLK
RX_TXB
U1
NOR1L
U2
inv1
U3
inv1
U4
inv1
U5
inv1
U6
inv1
U7
in1
in0
nand2
U8
inv8
U9
inv4
U10
inv1
U11
inv2
U12
inv2
U13
inv6
U14
inv6
U15
inv6
PULSE

FIG. 99

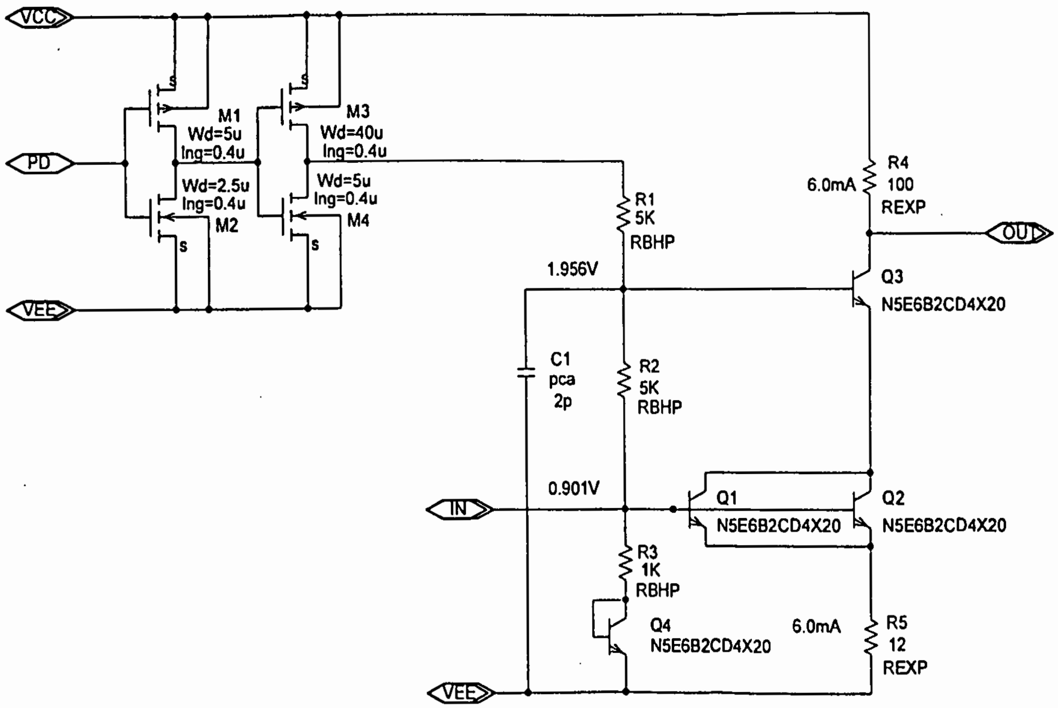

VCC
PD
VEE
M1
Wd=5u
lng=0.4u
Wd=2.5u
lng=0.4u
M2
M3
Wd=40u
lng=0.4u
Wd=5u
lng=0.4u
M4
R1
5K
RBHP
1.956V
C1
pca
2p
R2
5K
RBHP
IN
0.901V
Q1
N5E6B2CD4X20
Q2
N5E6B2CD4X20
R3
1K
RBHP
Q4
N5E6B2CD4X20
VEE
6.0mA
R5
12
REXP
6.0mA
R4
100
REXP
OUT
Q3
N5E6B2CD4X20

FIG. 10D

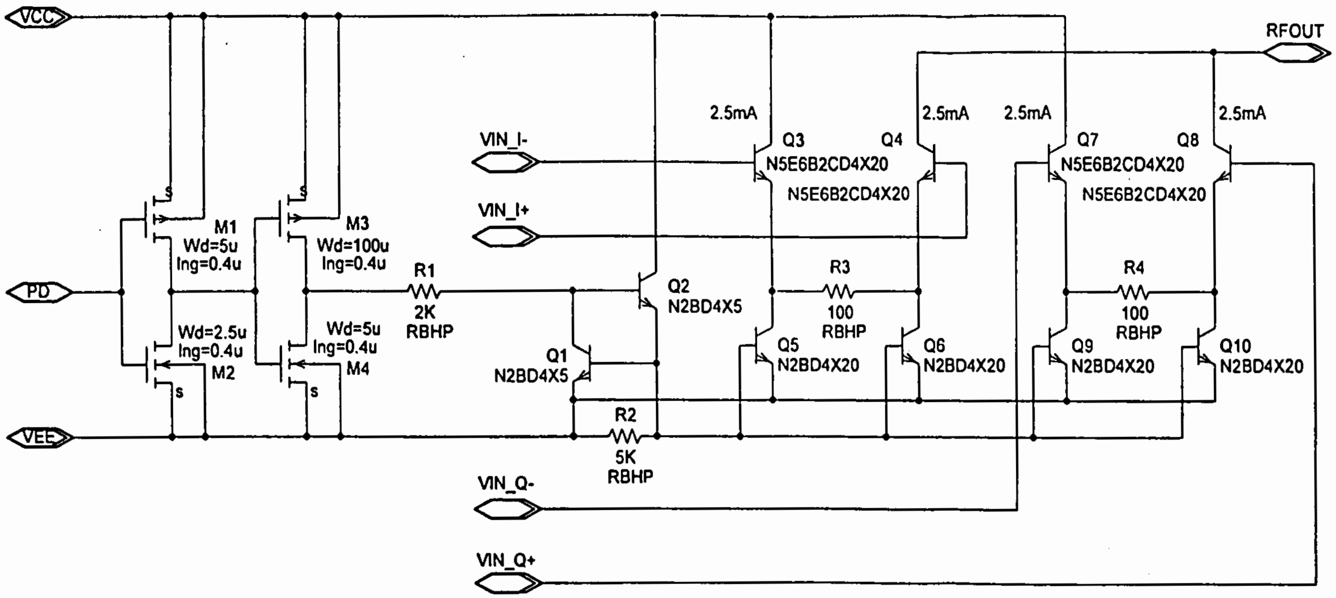

VCC
RFOUT
2.5mA
2.5mA
2.5mA
2.5mA
Q3
Q4
Q7
Q8
N5E6B2CD4X20
N5E6B2CD4X20
N5E6B2CD4X20
N5E6B2CD4X20
VIN_I-
VIN_I+
M1
Wd=5u
lng=0.4u
M3
Wd=100u
lng=0.4u
PD
R1
2K
RBHP
Q2
N2BD4X5
R3
100
RBHP
R4
100
RBHP
Wd=2.5u
lng=0.4u
M2
Wd=5u
lng=0.4u
M4
Q1
N2BD4X5
Q5
N2BD4X20
Q6
N2BD4X20
Q9
N2BD4X20
Q10
N2BD4X20
VEE
R2
5K
RBHP
VIN_Q-
VIN_Q+

FIG. 101

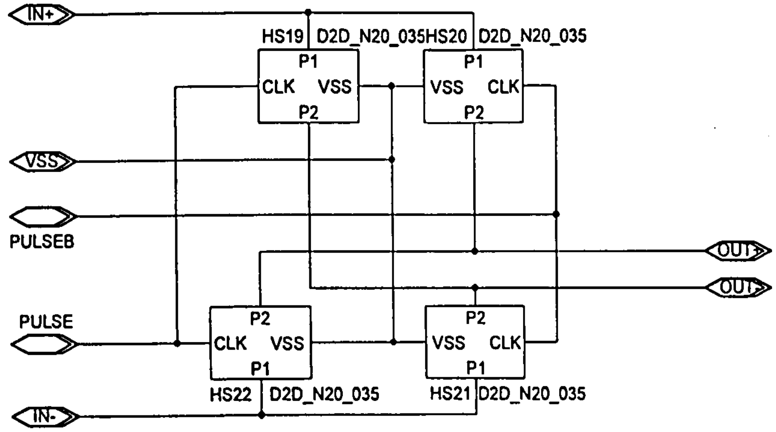

IN+
HS19
D2D_N20_035
HS20
D2D_N20_035
P1
CLK
VSS
P2
P1
VSS
CLK
P2
VSS
PULSEB
OUT+
OUT-
PULSE
P2
CLK
VSS
P1
HS22
D2D_N20_035
P2
VSS
CLK
P1
HS21
D2D_N20_035
IN-

FIG. 102

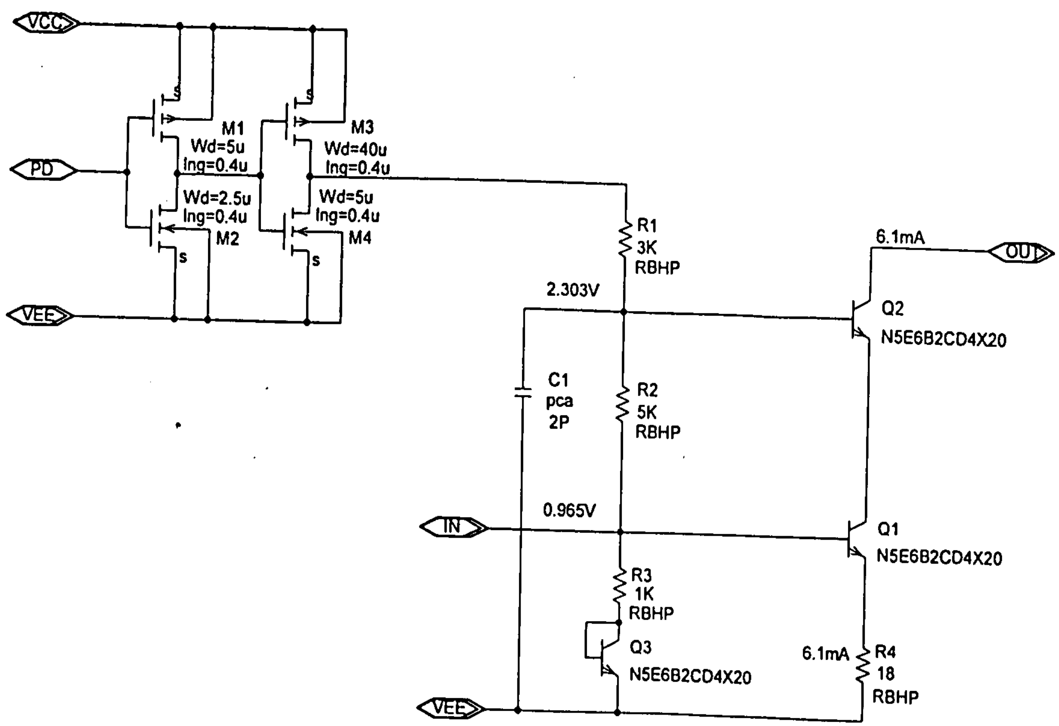


FIG. 103

09632856 .080400

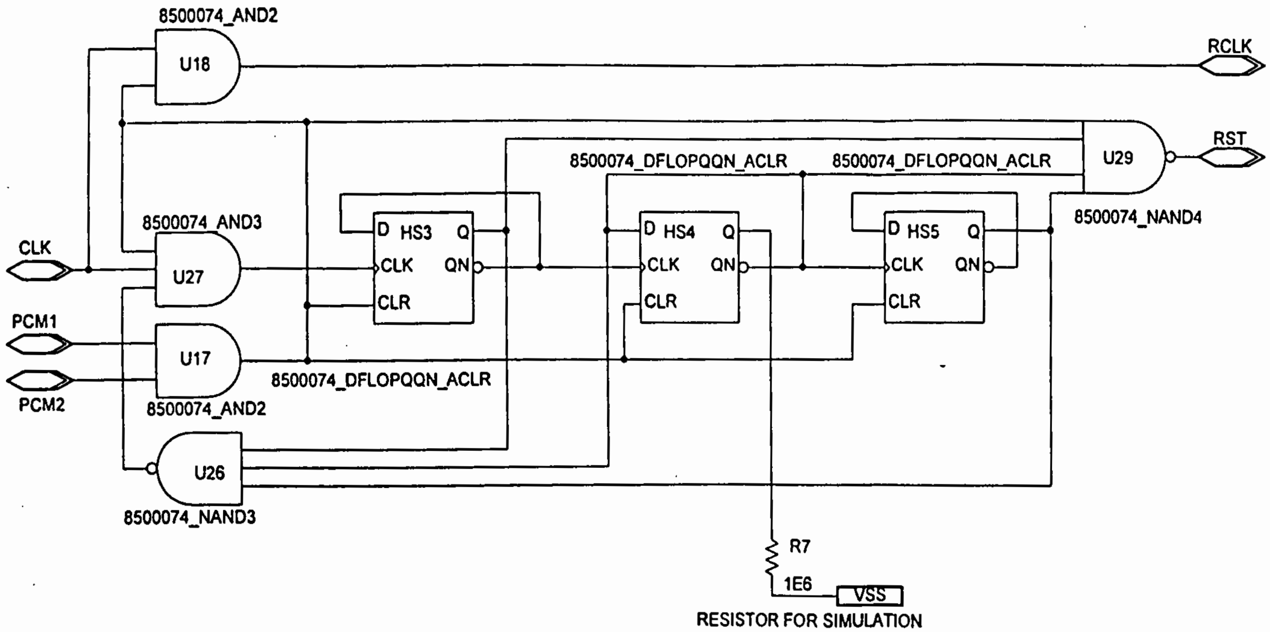

8500074_AND2
U18
RCLK
RST
U29
8500074_DFLOPQQN_ACLR
8500074_DFLOPQQN_ACLR
8500074_NAND4
8500074_AND3
CLK
U27
D HS3 Q
CLK QN
CLR
D HS4 Q
CLK QN
CLR
D HS5 Q
CLK QN
CLR
PCM1
U17
PCM2
8500074_DFLOPQQN_ACLR
8500074_AND2
U26
8500074_NAND3
R7
1E6
VSS
RESISTOR FOR SIMULATION

FIG. 104

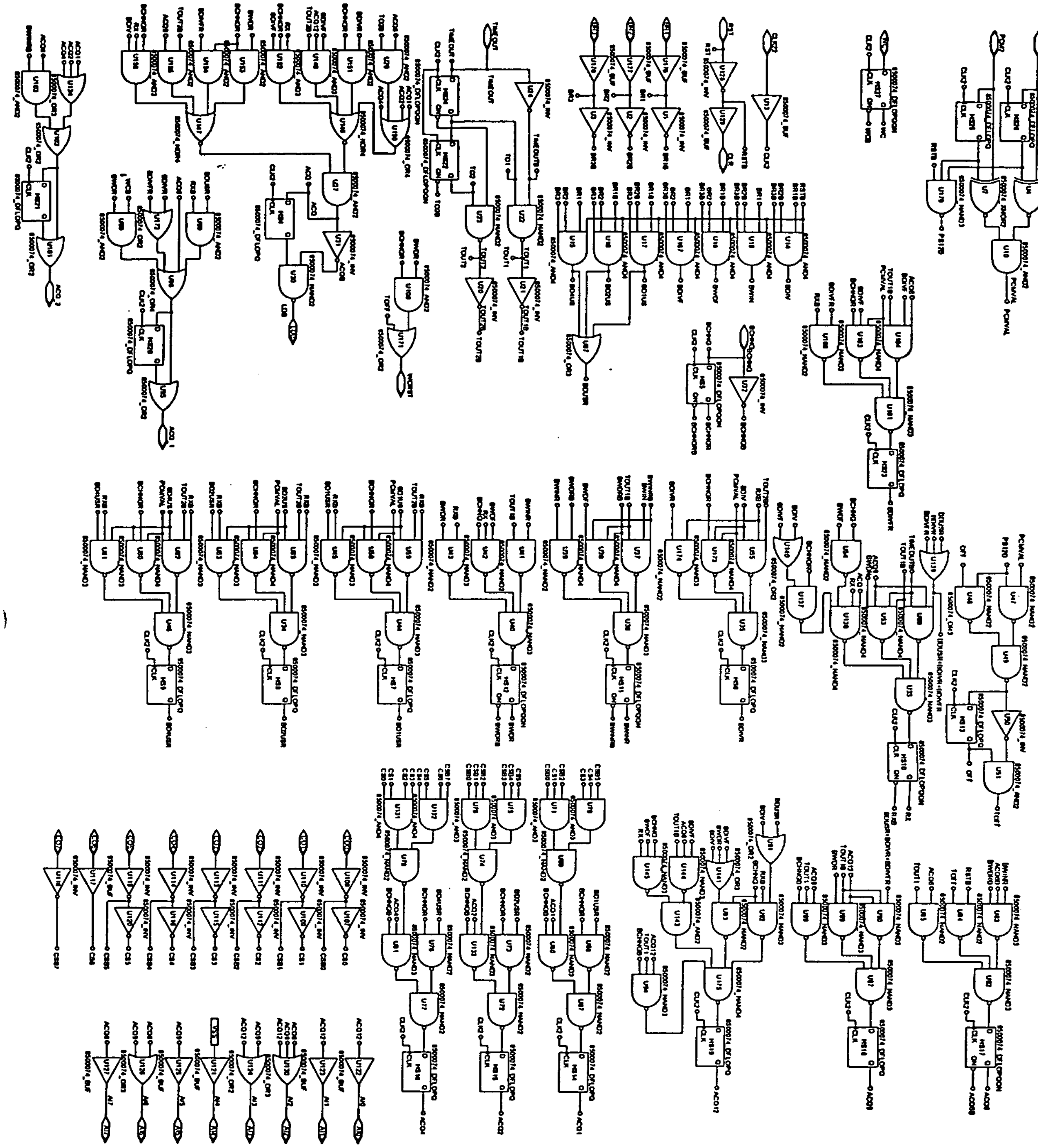


FIG. 105

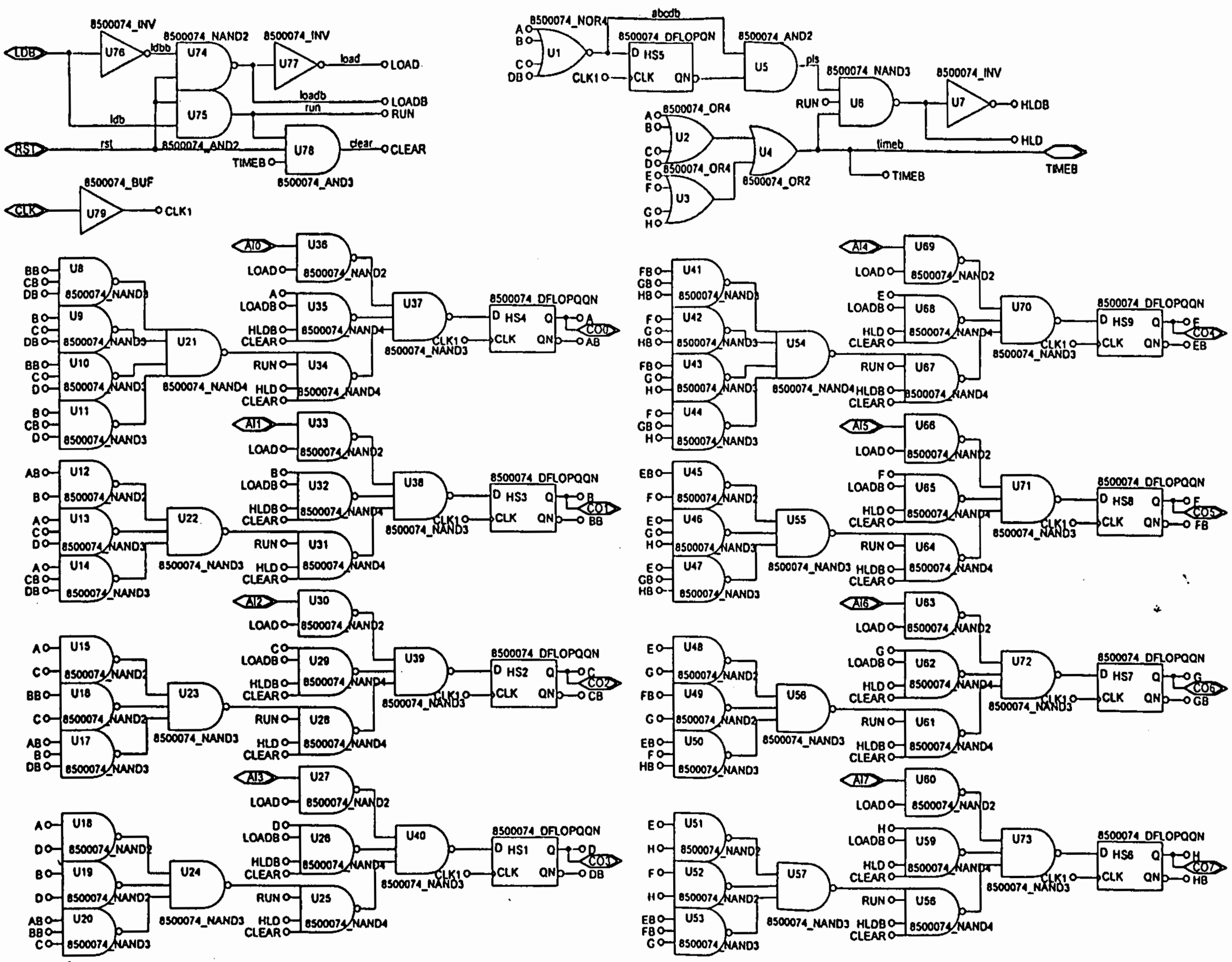


FIG. 10G

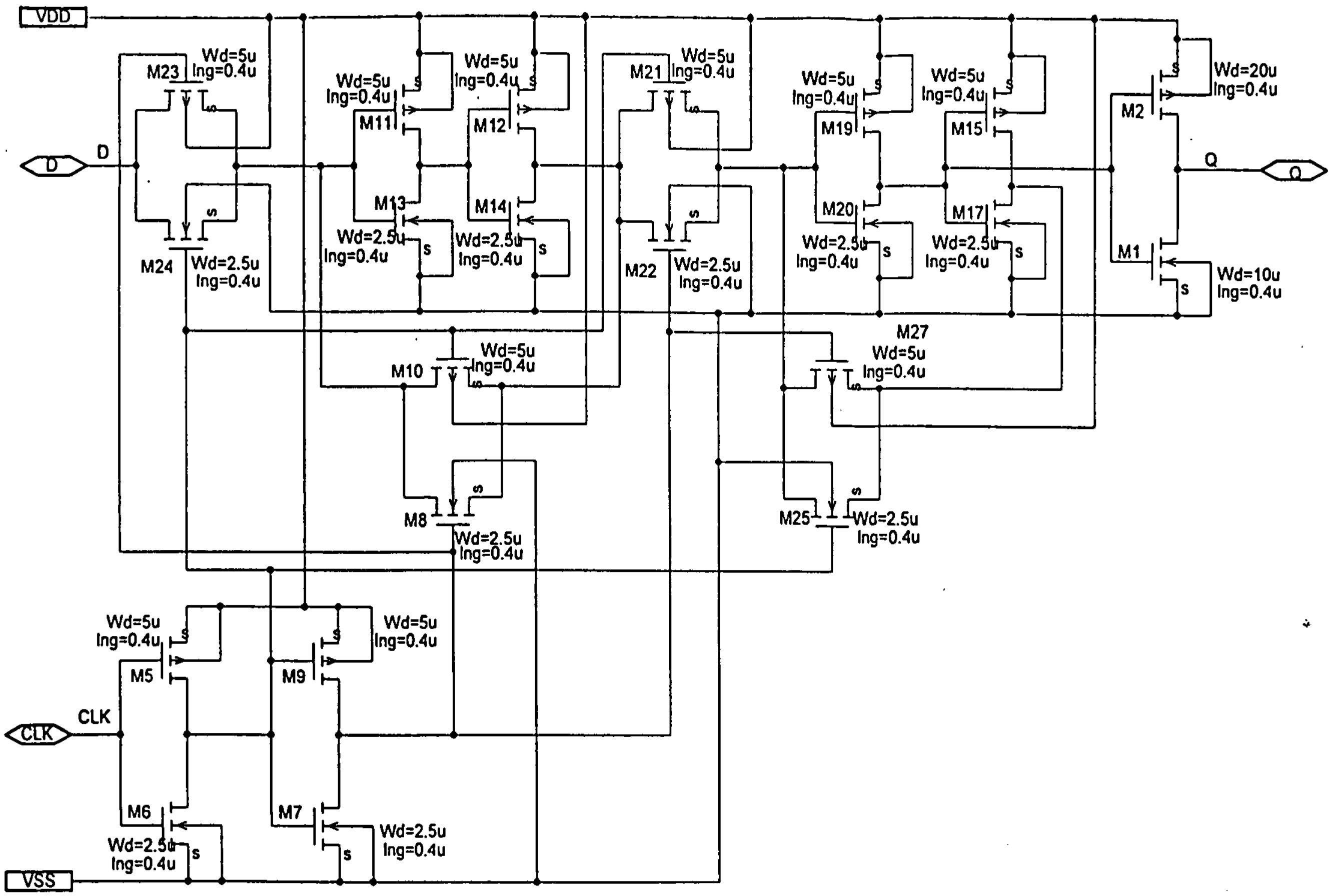

VDD
D
Q
CLK
VSS
M23
Wd=5u
lng=0.4u
M24
Wd=2.5u
lng=0.4u
M11
M12
M13
M14
M21
M22
M19
M20
M15
M17
M2
Wd=20u
lng=0.4u
M1
Wd=10u
lng=0.4u
M10
M27
M8
M25
M5
M9
M6
M7

FIG. 107

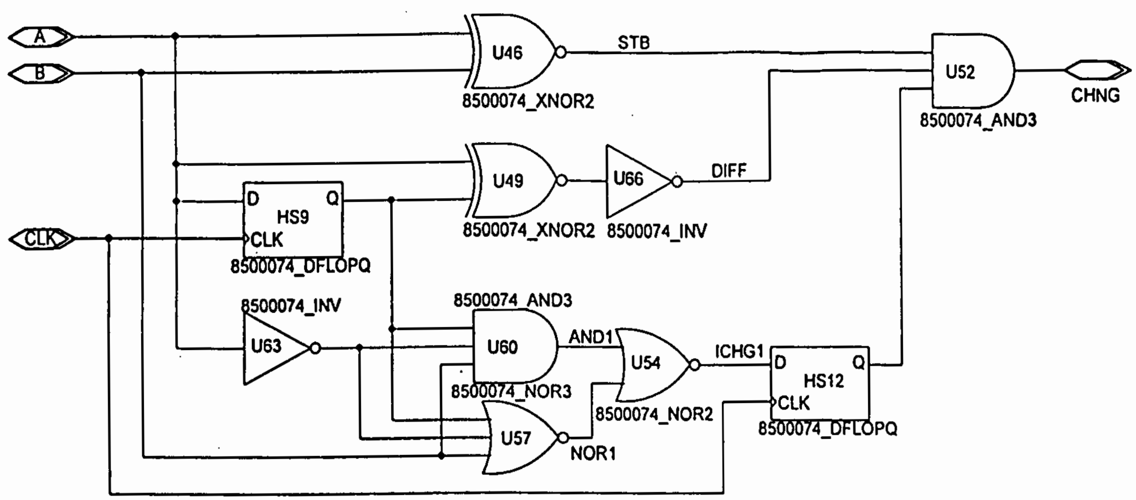

A
B
CLK
U46
8500074_XNOR2
STB
U52
8500074_AND3
CHNG
U49
8500074_XNOR2
U66
8500074_INV
DIFF
D
Q
HS9
CLK
8500074_DFLOPQ
8500074_INV
U63
8500074_AND3
U60
AND1
U54
8500074_NOR2
ICHG1
D
Q
HS12
CLK
8500074_DFLOPQ
8500074_NOR3
U57
NOR1

FIG. 108

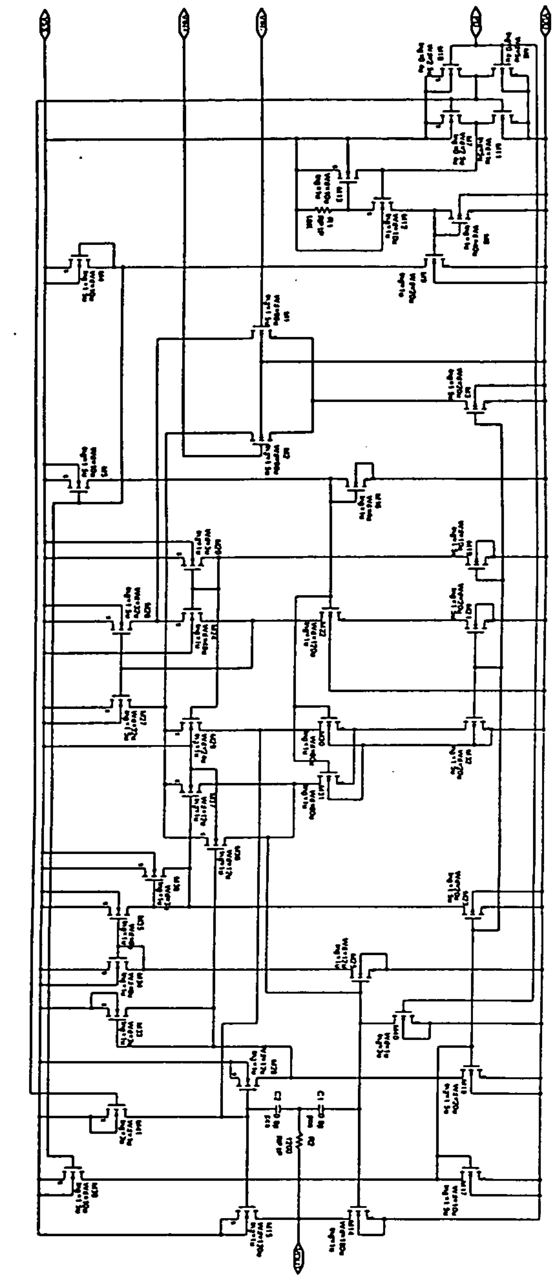


Fig. 109

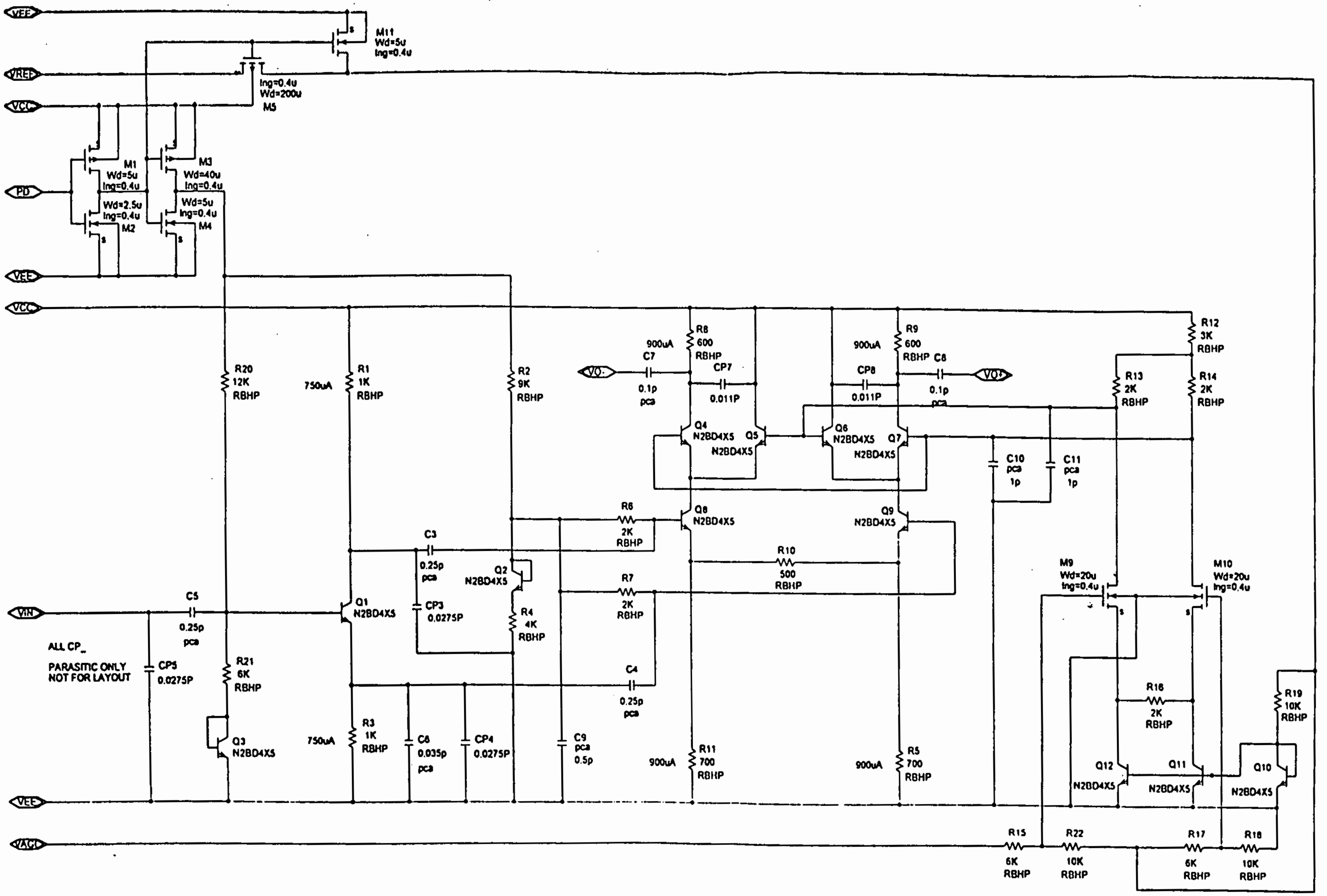

VEE
VREF
VCC
PD
VEE
VCC
VIN
VEE
VAGC
M11
Wd=5u
lng=0.4u
lng=0.4u
Wd=200u
M5
M1
Wd=5u
lng=0.4u
Wd=2.5u
lng=0.4u
M2
M3
Wd=40u
lng=0.4u
Wd=5u
lng=0.4u
M4
R20
12K
RBHP
R1
1K
RBHP
750uA
R2
9K
RBHP
R8
600
RBHP
900uA
C7
0.1p
pca
CP7
0.011P
VO-
R9
600
RBHP
900uA
C8
0.1p
pca
CP8
0.011P
VO+
R12
3K
RBHP
R13
2K
RBHP
R14
2K
RBHP
Q4
N2BD4X5
Q5
N2BD4X5
Q6
N2BD4X5
Q7
N2BD4X5
C10
pca
1p
C11
pca
1p
R6
2K
RBHP
Q8
N2BD4X5
Q9
N2BD4X5
C3
0.25p
pca
CP3
0.0275P
Q2
N2BD4X5
R10
500
RBHP
R7
2K
RBHP
R4
4K
RBHP
M9
Wd=20u
lng=0.4u
M10
Wd=20u
lng=0.4u
C5
0.25p
pca
Q1
N2BD4X5
ALL CP_
PARASITIC ONLY
NOT FOR LAYOUT
CP5
0.0275P
R21
6K
RBHP
C4
0.25p
pca
R16
2K
RBHP
R19
10K
RBHP
Q3
N2BD4X5
R3
1K
RBHP
750uA
C6
0.035p
pca
CP4
0.0275P
C9
pca
0.5p
R11
700
RBHP
900uA
R5
700
RBHP
900uA
Q12
N2BD4X5
Q11
N2BD4X5
Q10
N2BD4X5
R15
6K
RBHP
R22
10K
RBHP
R17
6K
RBHP
R18
10K
RBHP

FIG. 110

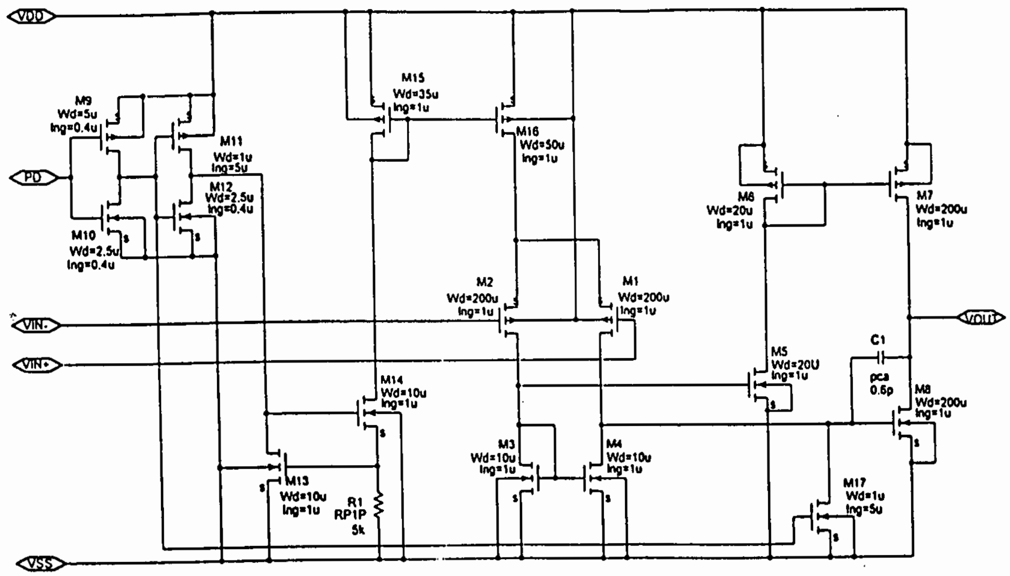

VDD
M9
Wd=5u
lng=0.4u
M11
Wd=1u
lng=5u
M12
Wd=2.5u
lng=0.4u
PD
M10
Wd=2.5u
lng=0.4u
M15
Wd=35u
lng=1u
M16
Wd=50u
lng=1u
M2
Wd=200u
lng=1u
M1
Wd=200u
lng=1u
VIN-
VIN+
M14
Wd=10u
lng=1u
M13
Wd=10u
lng=1u
R1
RP1P
5k
M3
Wd=10u
lng=1u
M4
Wd=10u
lng=1u
M6
Wd=20u
lng=1u
M7
Wd=200u
lng=1u
VOUT
M5
Wd=20U
lng=1u
C1
pca
0.6p
M8
Wd=200u
lng=1u
M17
Wd=1u
lng=5u
VSS

FIG. 111

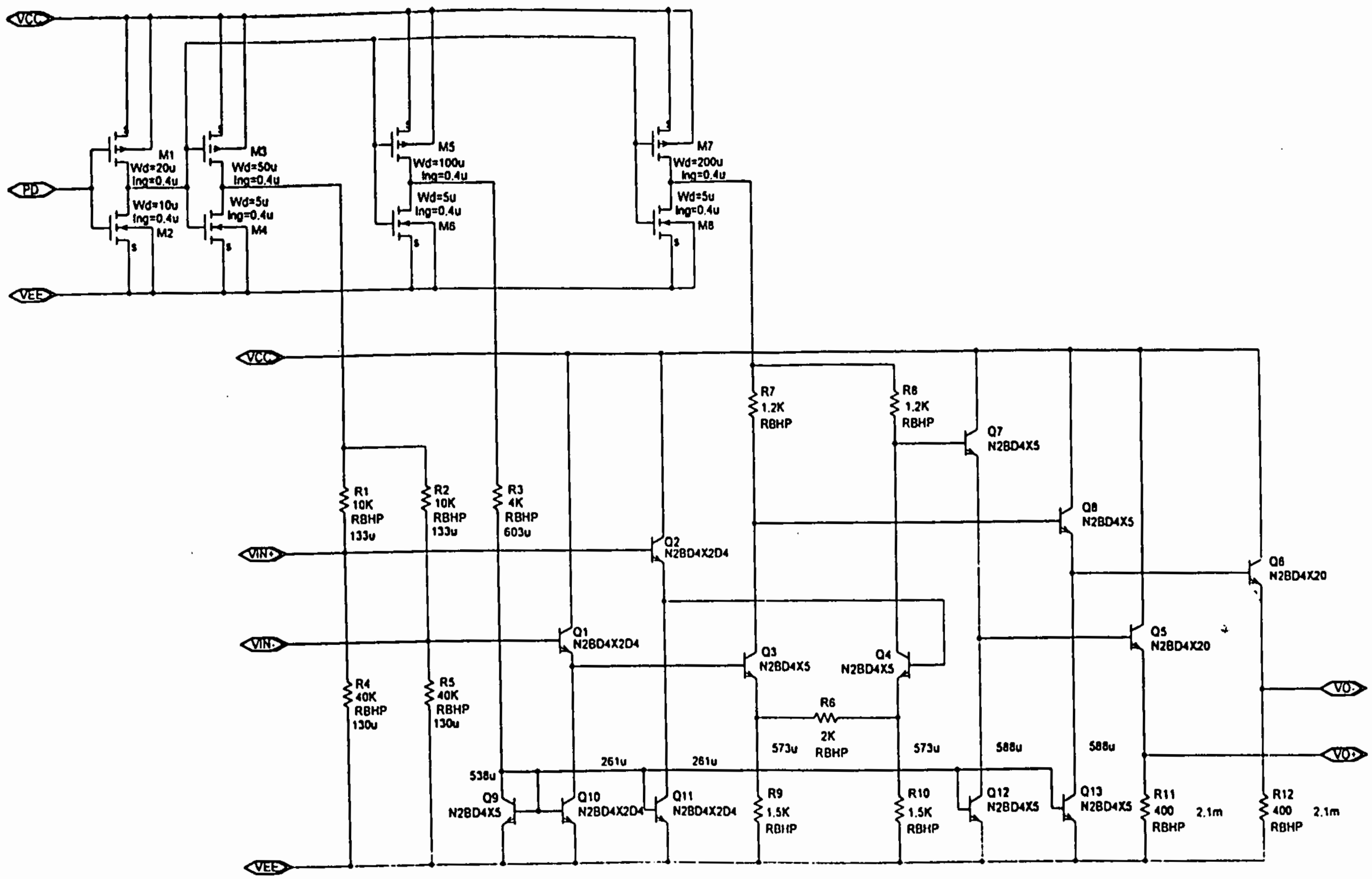
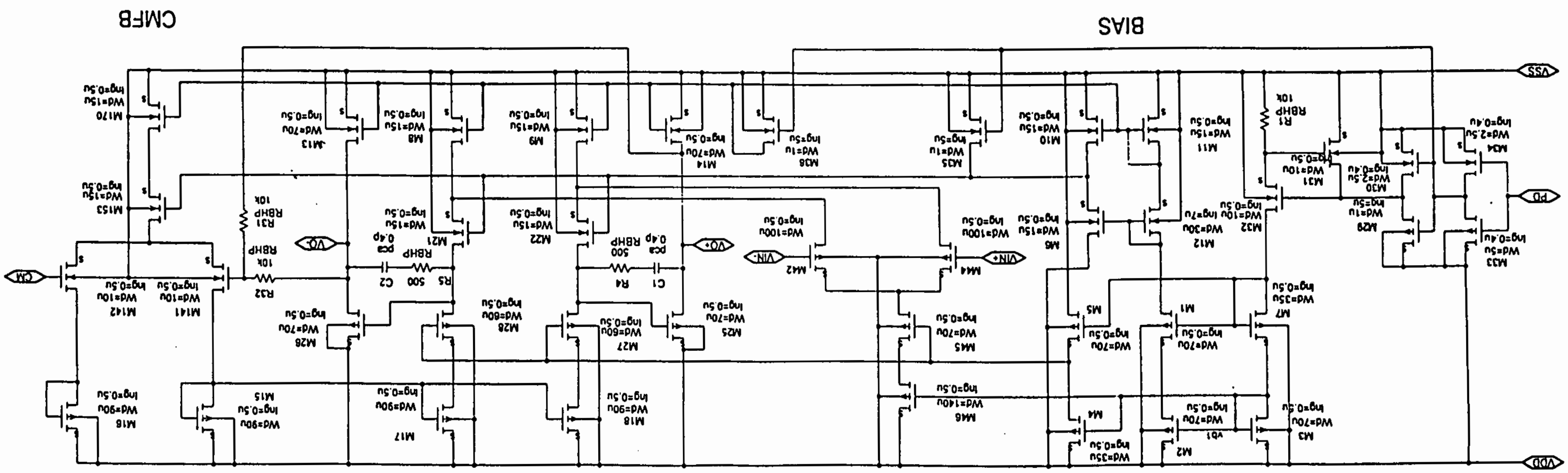
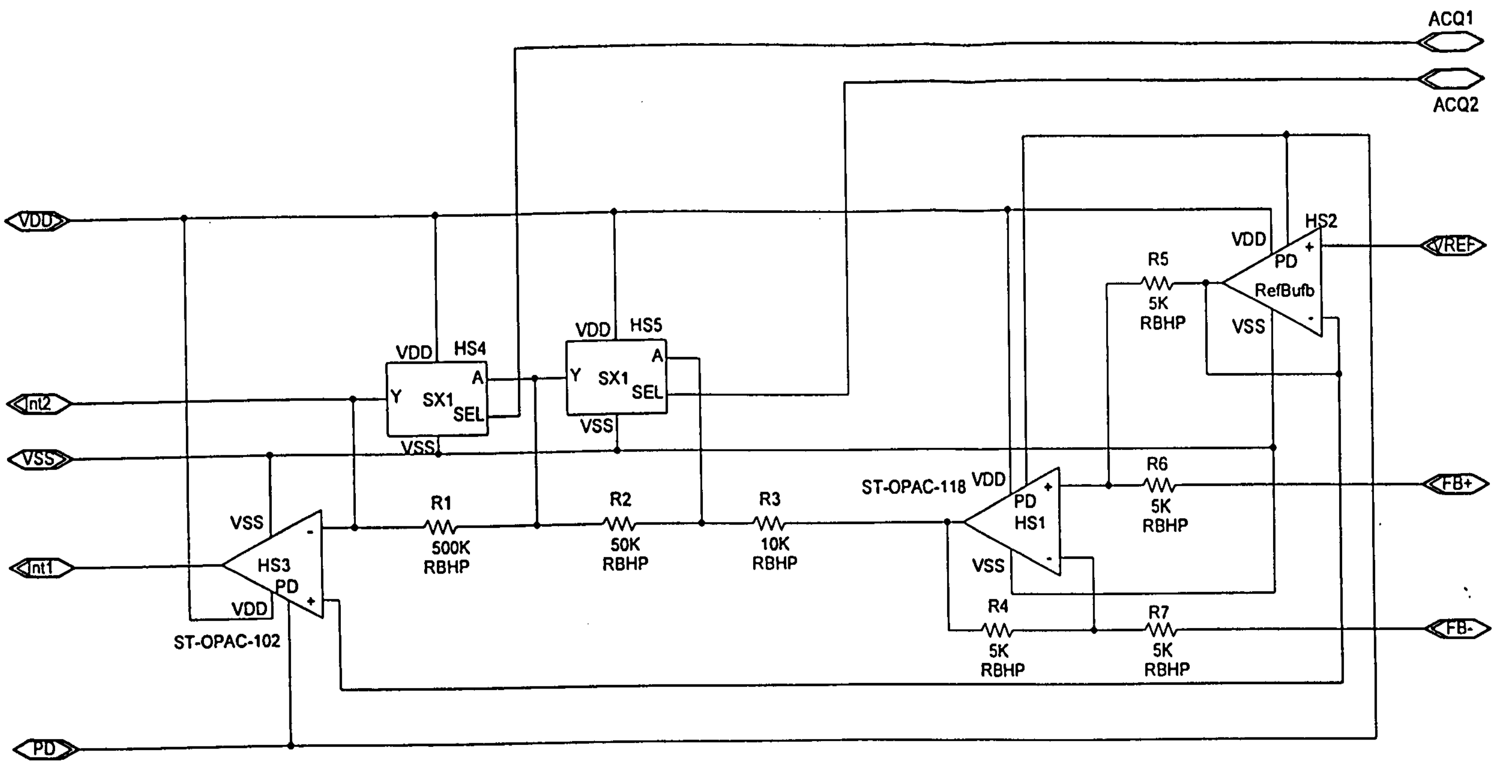

VCC
PD
VEE
M1
Wd=20u
lng=0.4u
Wd=10u
lng=0.4u
M2
M3
Wd=50u
lng=0.4u
Wd=5u
lng=0.4u
M4
M5
Wd=100u
lng=0.4u
Wd=5u
lng=0.4u
M6
M7
Wd=200u
lng=0.4u
Wd=5u
lng=0.4u
M8
VCC
R7
1.2K
RBHP
R8
1.2K
RBHP
Q7
N2BD4X5
Q8
N2BD4X5
Q6
N2BD4X20
R1
10K
RBHP
133u
R2
10K
RBHP
133u
R3
4K
RBHP
603u
VIN+
Q2
N2BD4X2D4
VIN-
Q1
N2BD4X2D4
Q3
N2BD4X5
Q4
N2BD4X5
Q5
N2BD4X20
R4
40K
RBHP
130u
R5
40K
RBHP
130u
R6
2K
RBHP
VO-
VO+
573u
573u
588u
588u
538u
261u
261u
Q9
N2BD4X5
Q10
N2BD4X2D4
Q11
N2BD4X2D4
R9
1.5K
RBHP
R10
1.5K
RBHP
Q12
N2BD4X5
Q13
N2BD4X5
R11
400
RBHP
2.1m
R12
400
RBHP
2.1m
VEE

FIG. 112

09635355 .080400

Fig. 113





ACQ1
ACQ2
VDD
VREF
HS2
PD
RefBufb
VSS
R5
5K
RBHP
VDD
HS4
SX1
Y
A
SEL
VSS
VDD
HS5
SX1
Y
A
SEL
VSS
Int2
VSS
R6
5K
RBHP
FB+
ST-OPAC-118
PD
HS1
VSS
R1
500K
RBHP
R2
50K
RBHP
R3
10K
RBHP
VSS
HS3
PD
VDD
Int1
ST-OPAC-102
R4
5K
RBHP
R7
5K
RBHP
FB-
PD

FIG. 114

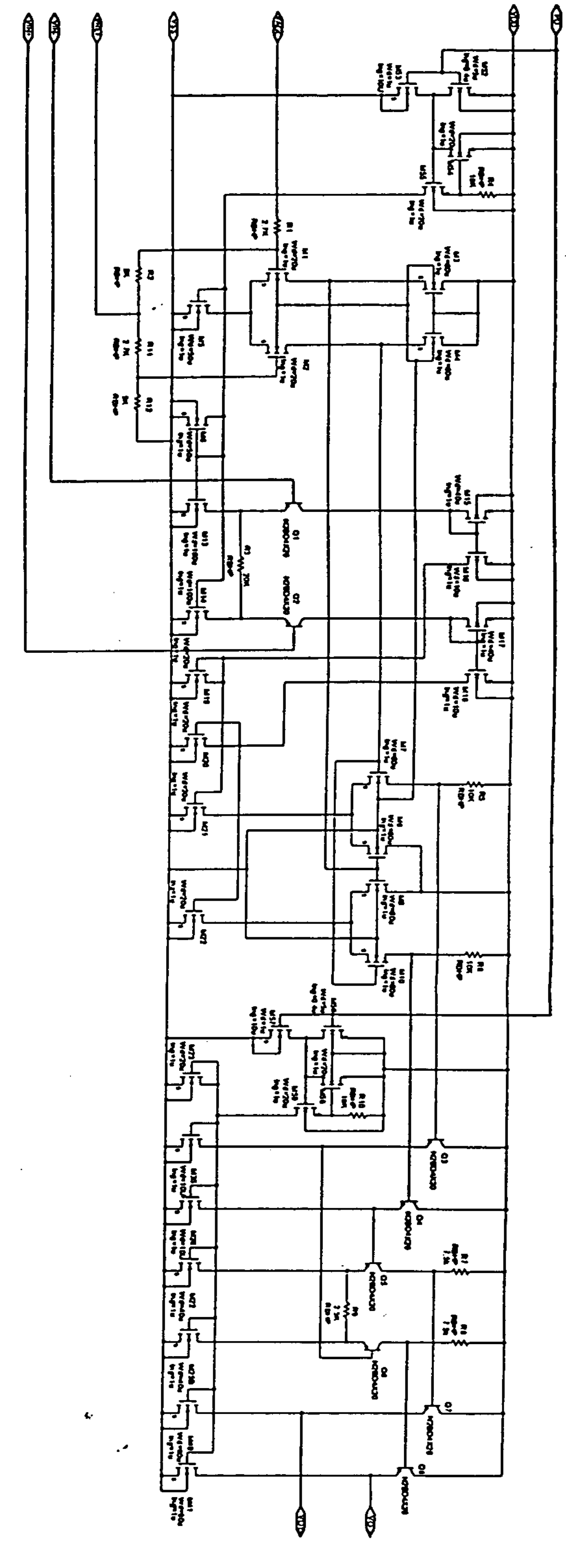


FIG. 115

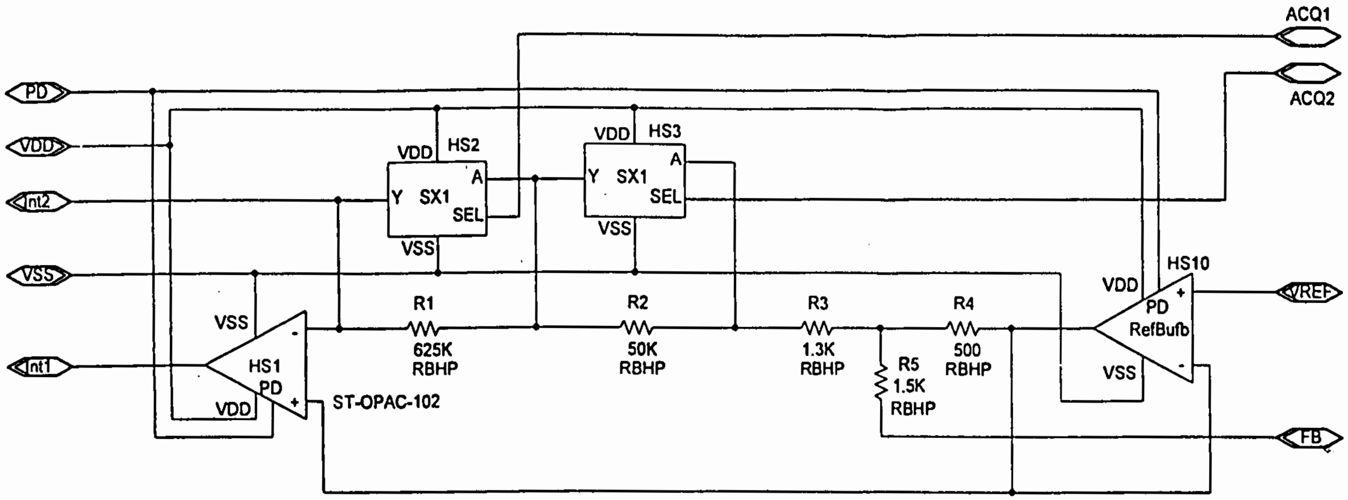

ACQ1
ACQ2
PD
VDD
Int2
VSS
Int1
HS2
VDD
Y SX1 A
SEL
VSS
HS3
VDD
Y SX1 A
SEL
VSS
R1
625K
RBHP
R2
50K
RBHP
R3
1.3K
RBHP
R4
500
RBHP
R5
1.5K
RBHP
VSS
HS1
PD
VDD
ST-OPAC-102
HS10
VDD
PD
RefBufb
VSS
VREF
FB

FIG. 116

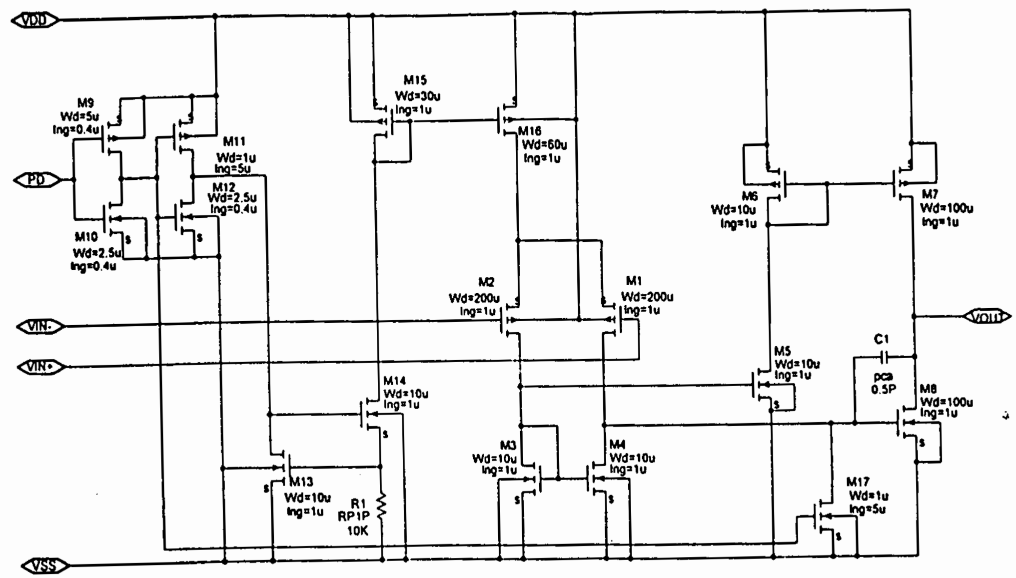


FIG. 117

09632856 .080400

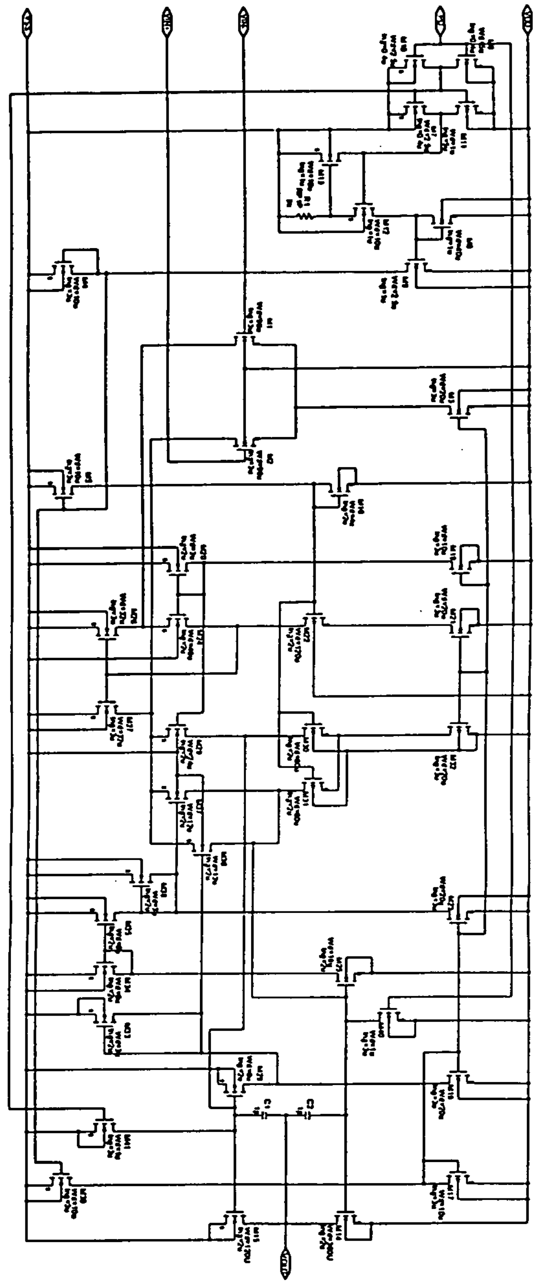


FIG 118

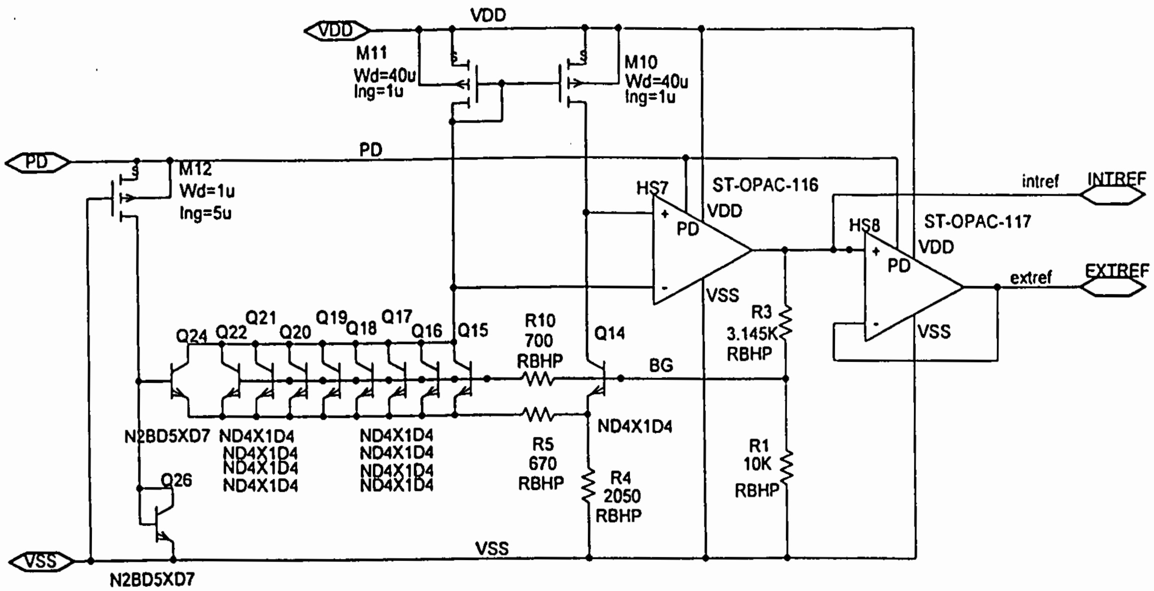

VDD
VDD
M11
Wd=40u
lng=1u
M10
Wd=40u
lng=1u
PD
PD
M12
Wd=1u
lng=5u
HS7
ST-OPAC-116
VDD
PD
VSS
HS8
ST-OPAC-117
VDD
PD
VSS
intref
INTREF
extref
EXTREF
Q24
Q22
Q21
Q20
Q19
Q18
Q17
Q16
Q15
R10
700
RBHP
Q14
BG
R3
3.145K
RBHP
N2BD5XD7
ND4X1D4
ND4X1D4
ND4X1D4
ND4X1D4
ND4X1D4
ND4X1D4
ND4X1D4
ND4X1D4
R5
670
RBHP
ND4X1D4
R4
2050
RBHP
R1
10K
RBHP
Q26
VSS
VSS
N2BD5XD7

FIG. 119

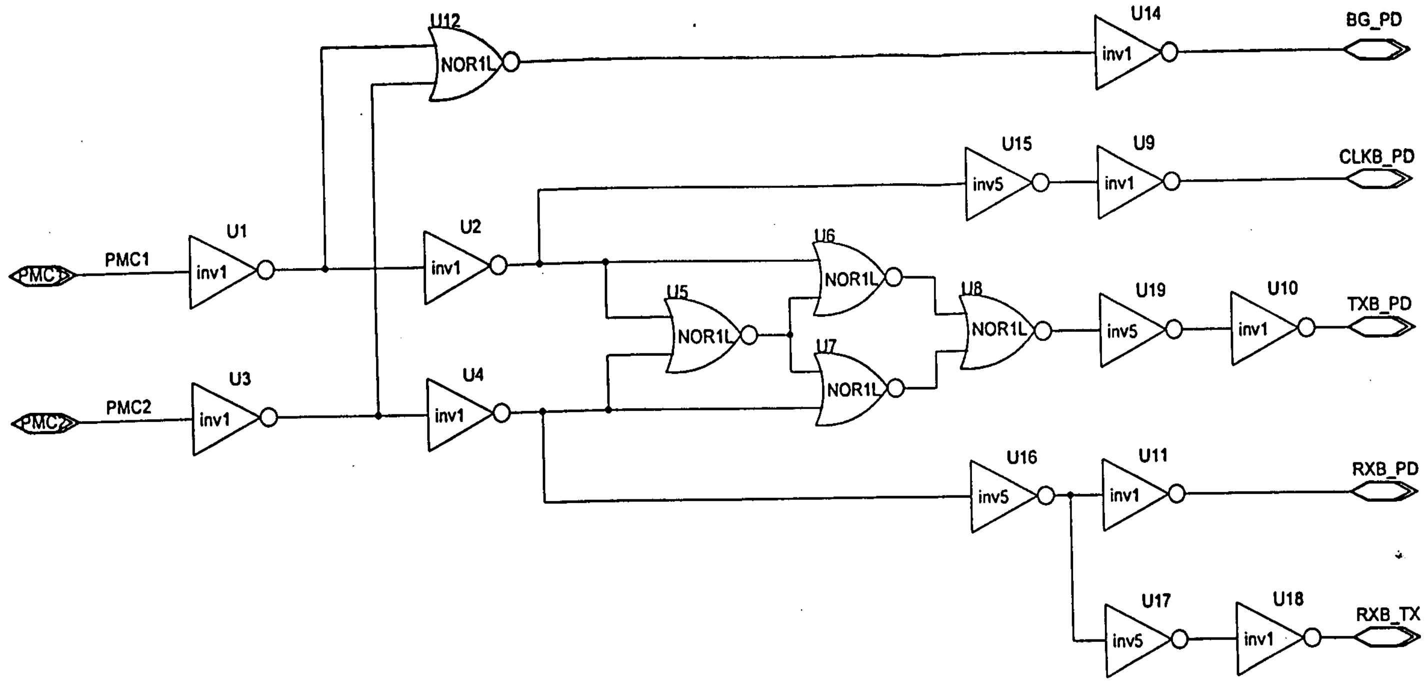
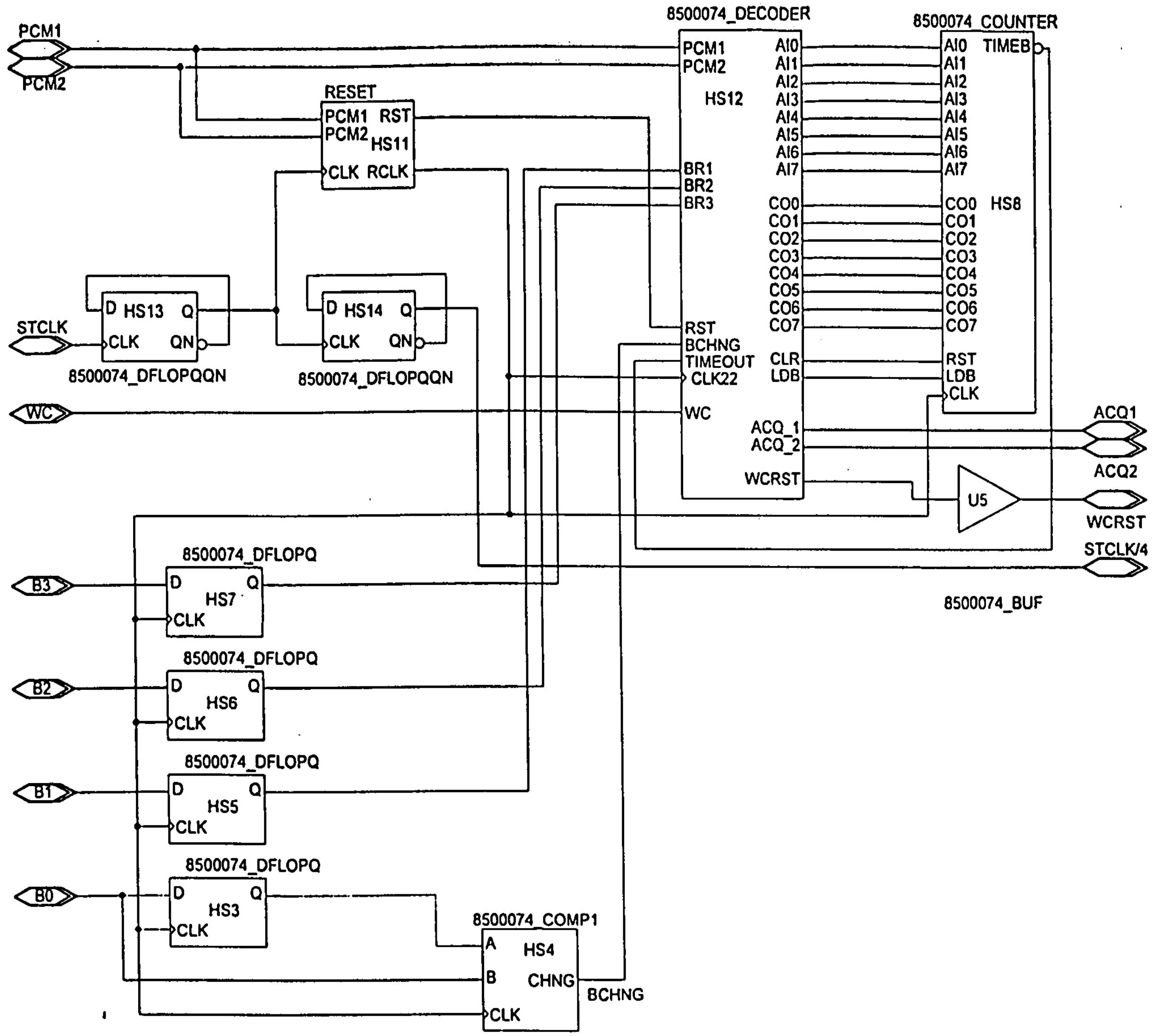
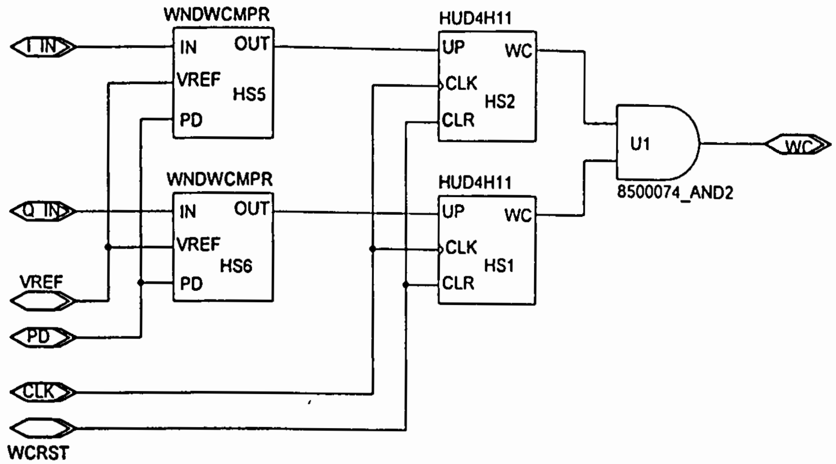

U12
NOR1L
U14
inv1
BG_PD
U15
inv5
U9
inv1
CLKB_PD
PMC1
PMC1
U1
inv1
U2
inv1
U6
NOR1L
U5
NOR1L
U8
NOR1L
U19
inv5
U10
inv1
TXB_PD
U7
NOR1L
PMC2
PMC2
U3
inv1
U4
inv1
U16
inv5
U11
inv1
RXB_PD
U17
inv5
U18
inv1
RXB_TX

FIG. 120



PCM1
PCM2
RESET
PCM1 RST
PCM2 HS11
CLK RCLK
8500074_DECODER
PCM1
PCM2
HS12
AI0
AI1
AI2
AI3
AI4
AI5
AI6
AI7
BR1
BR2
BR3
CO0
CO1
CO2
CO3
CO4
CO5
CO6
CO7
RST
BCHNG
TIMEOUT
CLK22
CLR
LDB
WC
ACQ_1
ACQ_2
WCRST
8500074_COUNTER
TIMEB
HS8
RST
LDB
CLK
ACQ1
ACQ2
U5
WCRST
STCLK/4
8500074_BUF
STCLK
D HS13 Q
CLK QN
8500074_DFLOPQQN
D HS14 Q
CLK QN
8500074_DFLOPQQN
WC
8500074_DFLOPQ
B3
D Q
HS7
CLK
8500074_DFLOPQ
B2
HS6
8500074_DFLOPQ
B1
HS5
8500074_DFLOPQ
B0
HS3
8500074_COMP1
A HS4
B CHNG
CLK
BCHNG

FIG. 121



WNDWCMPR
IN
OUT
VREF
HS5
PD
WNDWCMPR
IN
OUT
VREF
HS6
PD
HUD4H11
UP
WC
CLK
HS2
CLR
HUD4H11
UP
WC
CLK
HS1
CLR
U1
8500074_AND2
I IN
Q IN
VREF
PD
CLK
WCRST
WC

FIG. 122

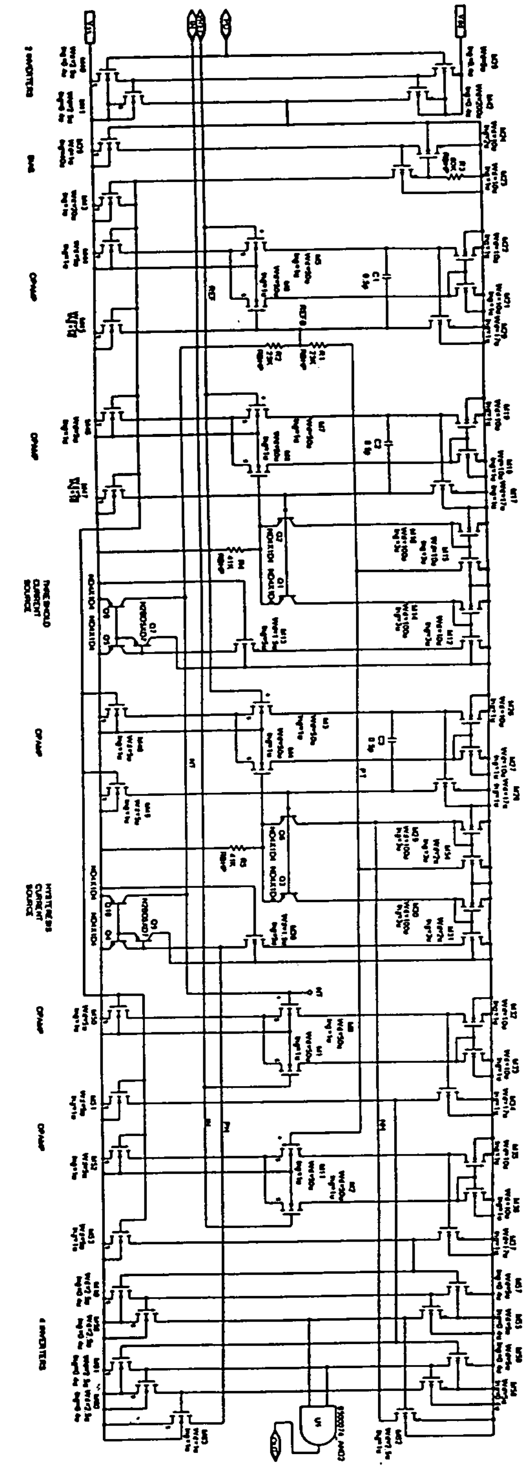


FIG. 123

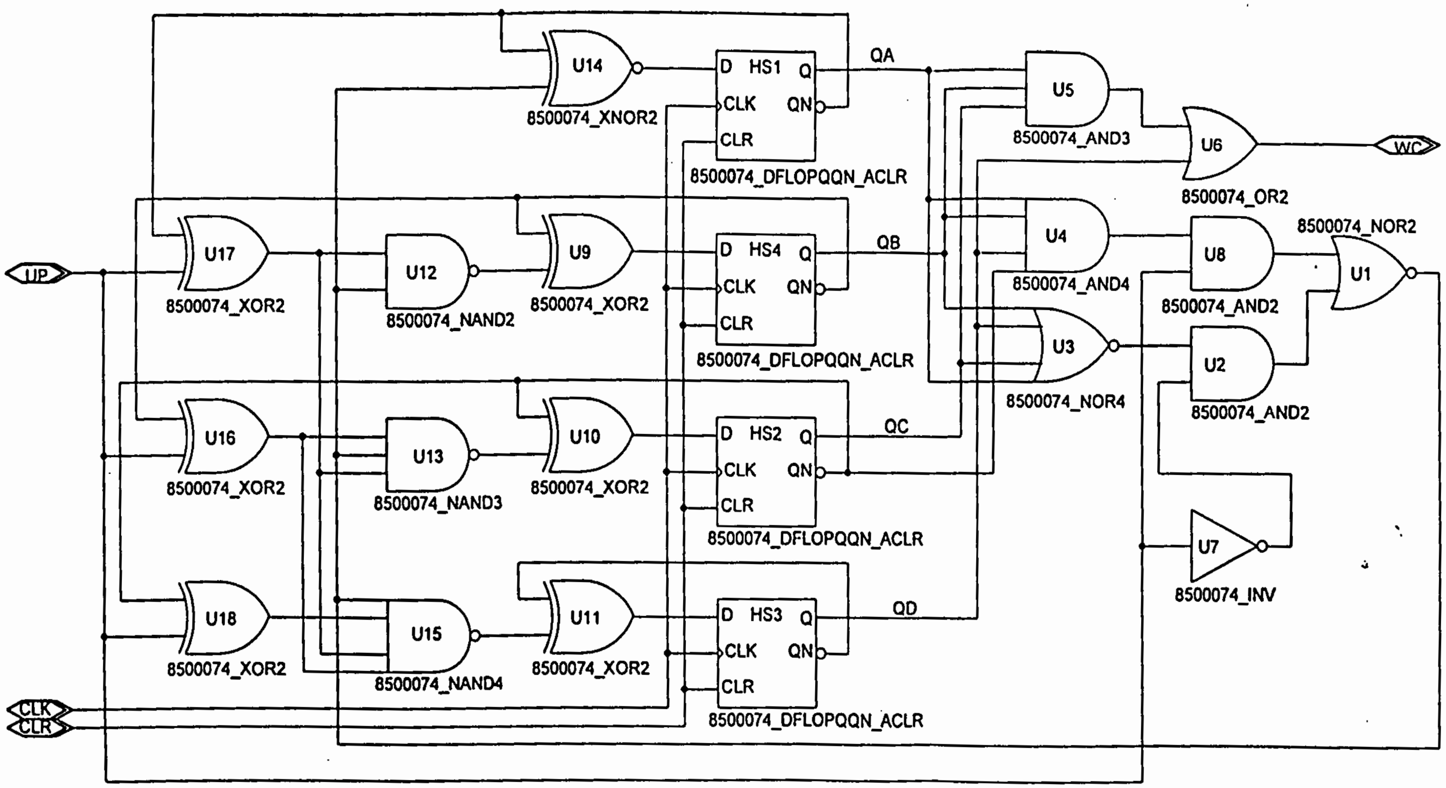

UP
CLK
CLR
U14
8500074_XNOR2
D HS1 Q
CLK QN
CLR
8500074_DFLOPQQN_ACLR
QA
U17
8500074_XOR2
U12
8500074_NAND2
U9
8500074_XOR2
D HS4 Q
CLK QN
CLR
8500074_DFLOPQQN_ACLR
QB
U16
8500074_XOR2
U13
8500074_NAND3
U10
8500074_XOR2
D HS2 Q
CLK QN
CLR
8500074_DFLOPQQN_ACLR
QC
U18
8500074_XOR2
U15
8500074_NAND4
U11
8500074_XOR2
D HS3 Q
CLK QN
CLR
8500074_DFLOPQQN_ACLR
QD
U5
8500074_AND3
U6
8500074_OR2
WC
U4
8500074_AND4
U8
8500074_AND2
8500074_NOR2
U1
U3
8500074_NOR4
U2
8500074_AND2
U7
8500074_INV

FIG. 124

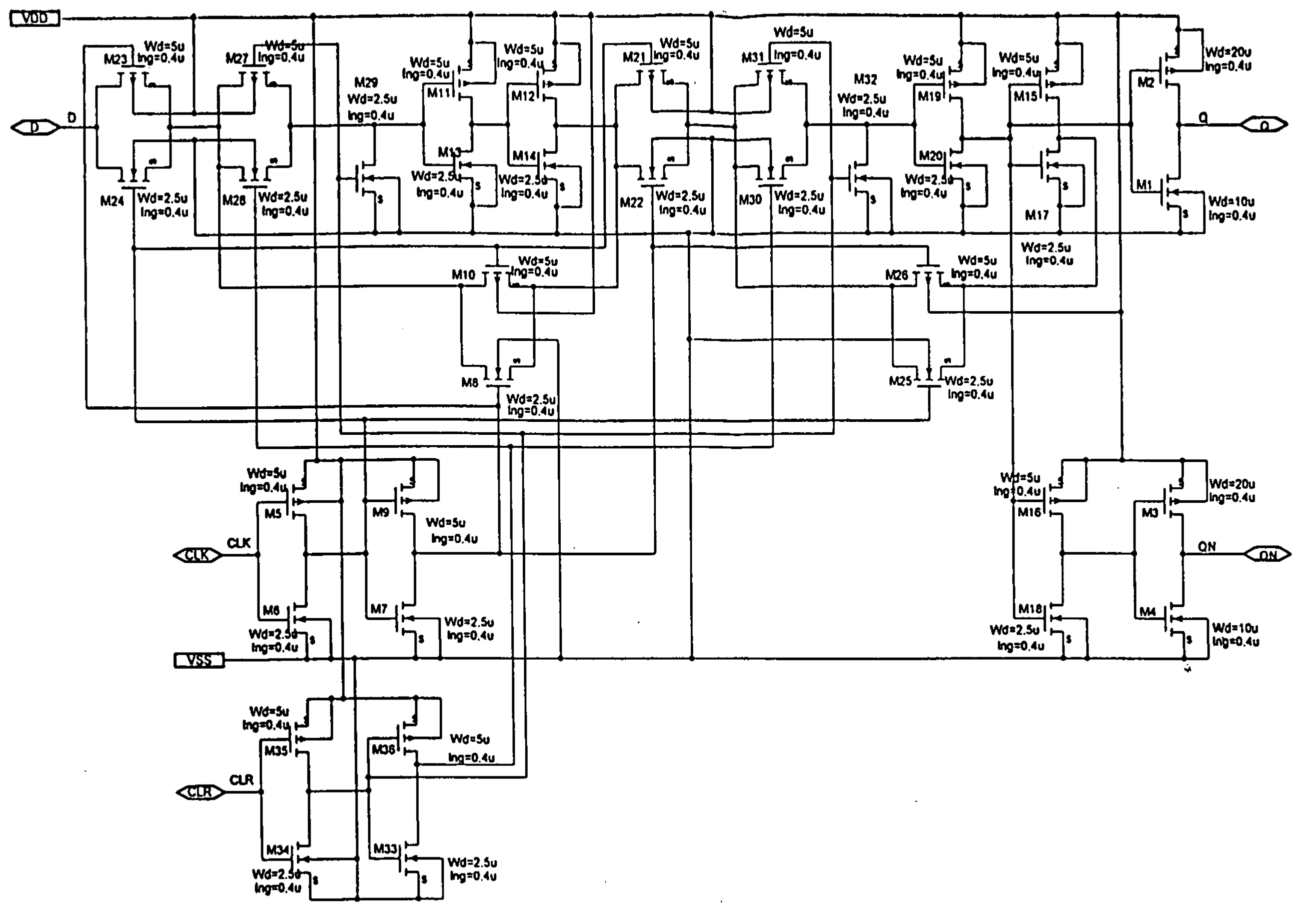


FIG. 125

09632856 .080400

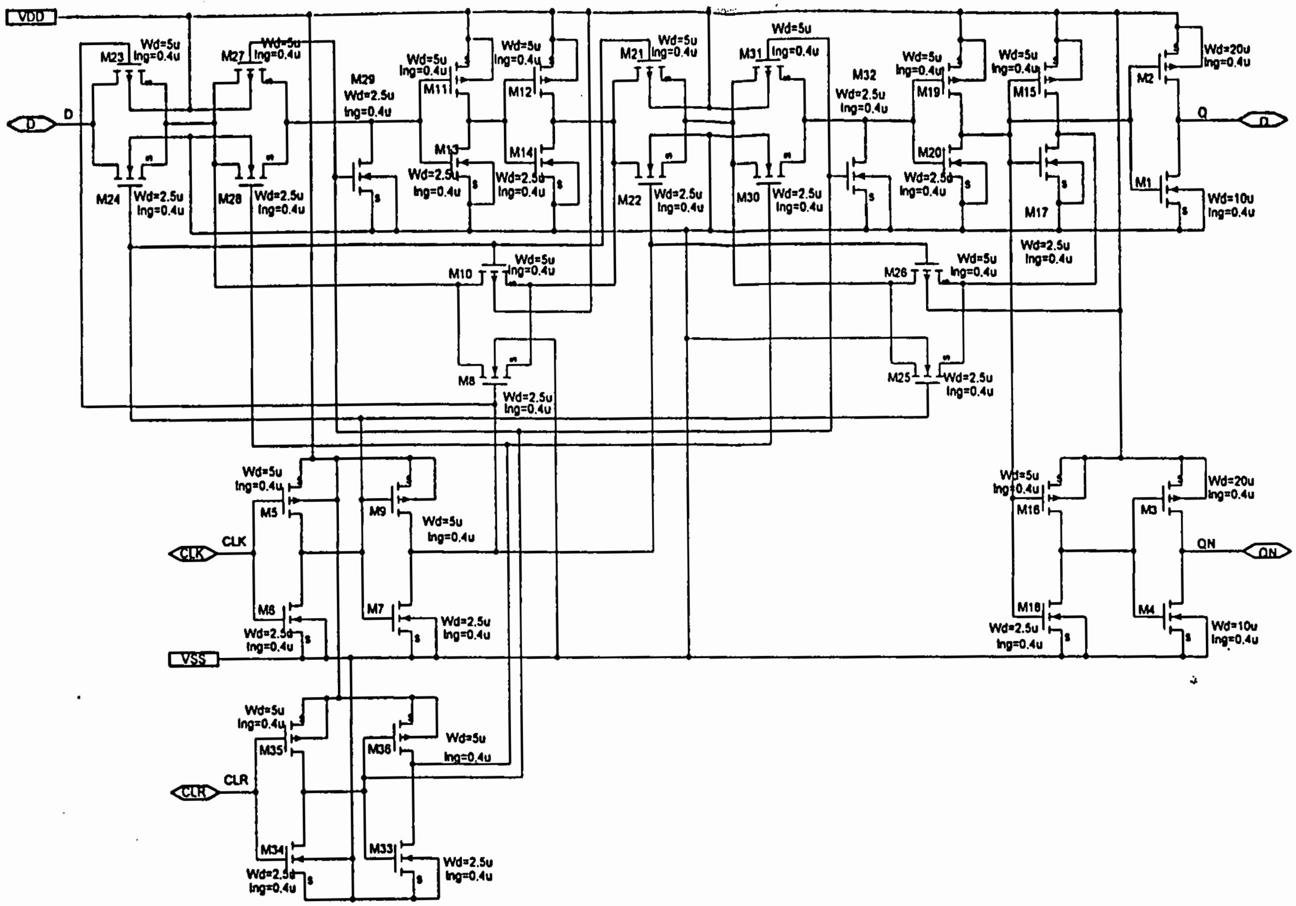


FIG 126

09632856 .080400

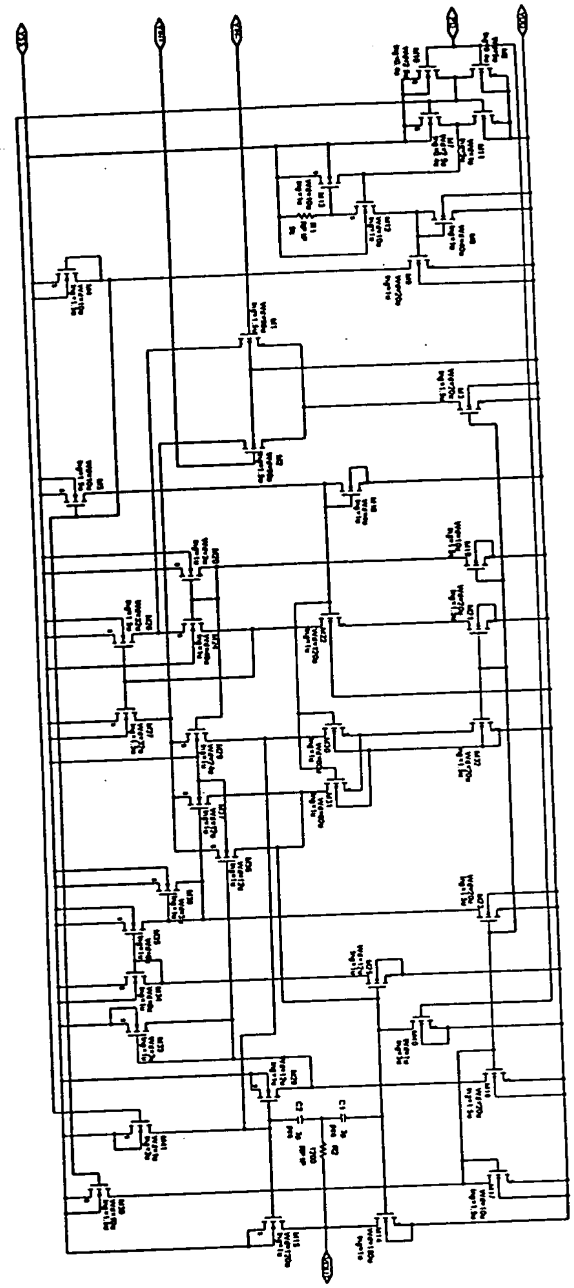


FIG. 127

09522856 . 080400

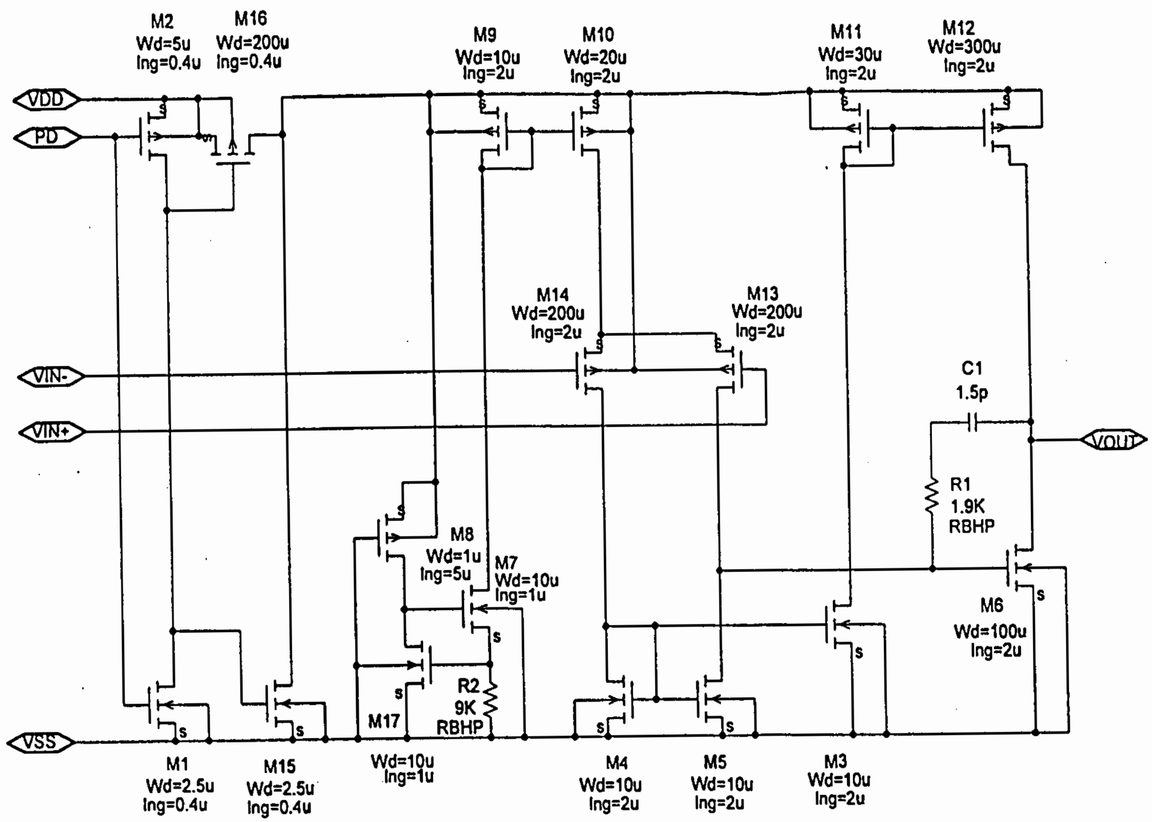

M2
Wd=5u
lng=0.4u
M16
Wd=200u
lng=0.4u
M9
Wd=10u
lng=2u
M10
Wd=20u
lng=2u
M11
Wd=30u
lng=2u
M12
Wd=300u
lng=2u
VDD
PD
M14
Wd=200u
lng=2u
M13
Wd=200u
lng=2u
VIN-
VIN+
C1
1.5p
VOUT
R1
1.9K
RBHP
M8
Wd=1u
lng=5u
M7
Wd=10u
lng=1u
M6
Wd=100u
lng=2u
R2
9K
RBHP
M17
VSS
M1
Wd=2.5u
lng=0.4u
M15
Wd=2.5u
lng=0.4u
Wd=10u
lng=1u
M4
Wd=10u
lng=2u
M5
Wd=10u
lng=2u
M3
Wd=10u
lng=2u

FIG. 128

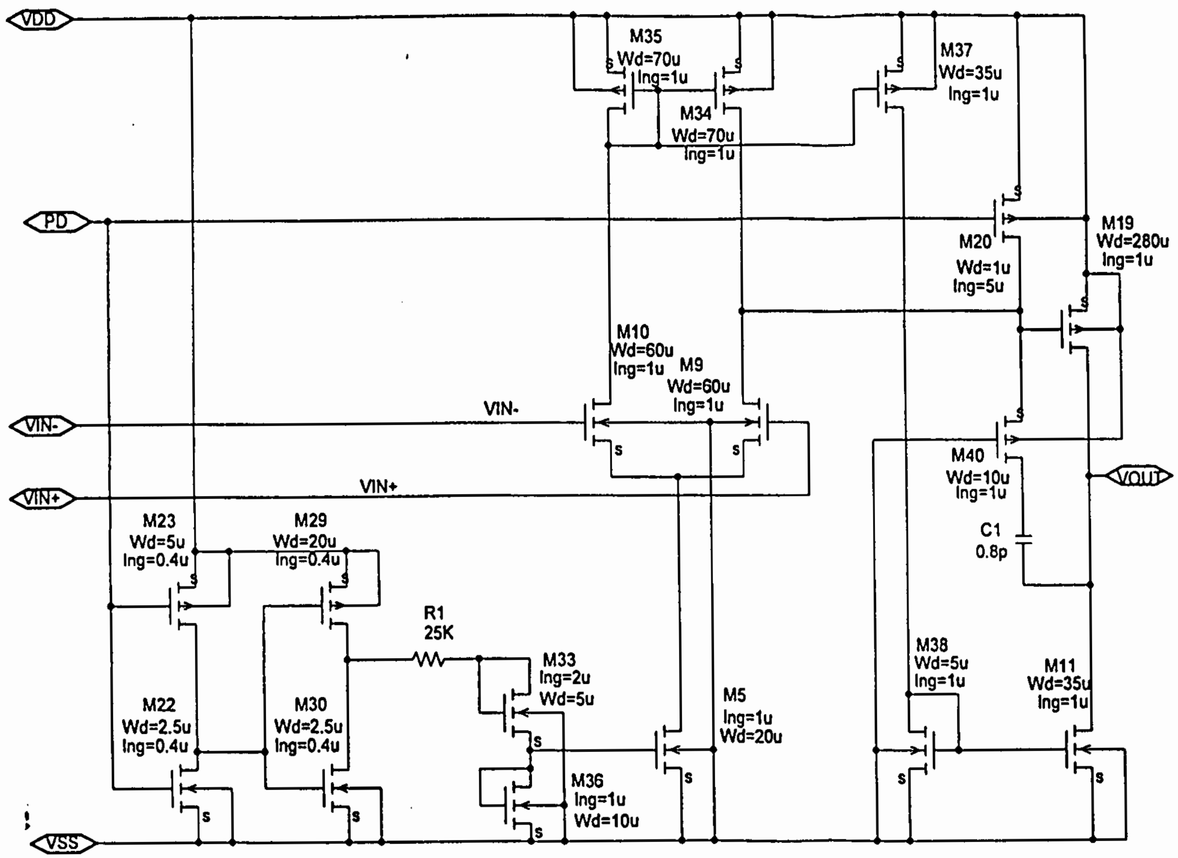

VDD
PD
VIN-
VIN+
VSS
VOUT
M35
Wd=70u
lng=1u
M34
Wd=70u
lng=1u
M37
Wd=35u
lng=1u
M19
Wd=280u
lng=1u
M20
Wd=1u
lng=5u
M10
Wd=60u
lng=1u
M9
Wd=60u
lng=1u
M40
Wd=10u
lng=1u
C1
0.8p
M23
Wd=5u
lng=0.4u
M29
Wd=20u
lng=0.4u
R1
25K
M33
lng=2u
Wd=5u
M22
Wd=2.5u
lng=0.4u
M30
Wd=2.5u
lng=0.4u
M36
lng=1u
Wd=10u
M5
lng=1u
Wd=20u
M38
Wd=5u
lng=1u
M11
Wd=35u
lng=1u

FIG. 129

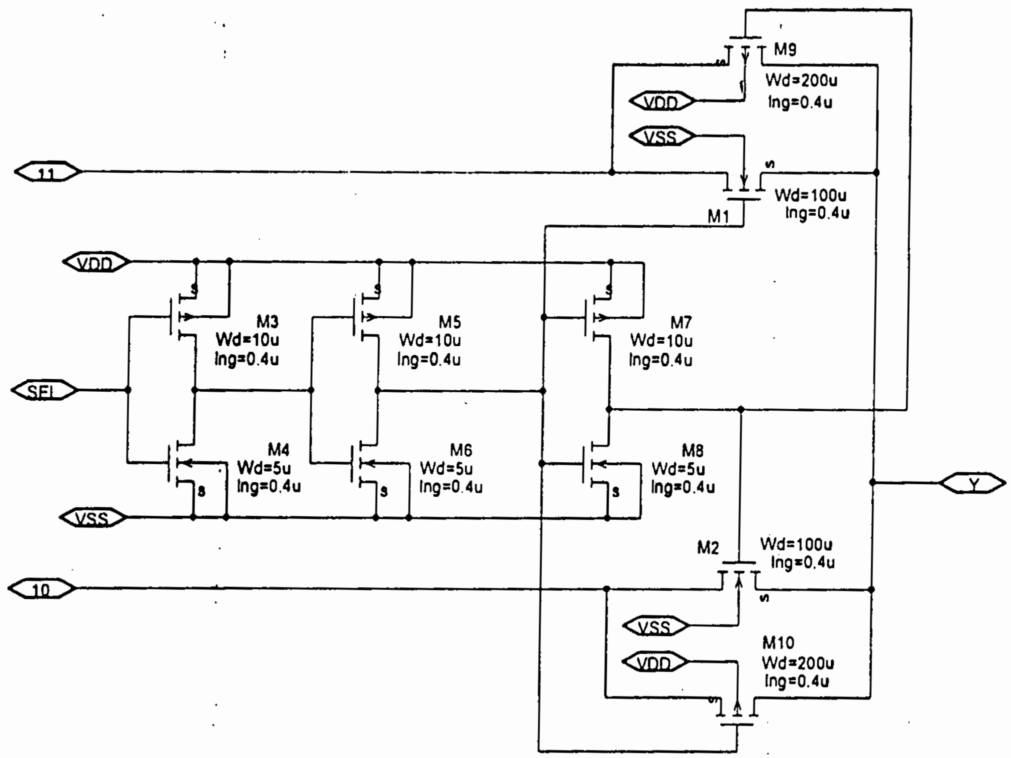


FIG 130

09632856 .080400

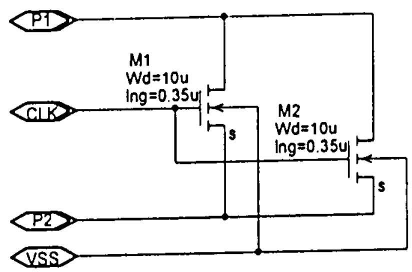
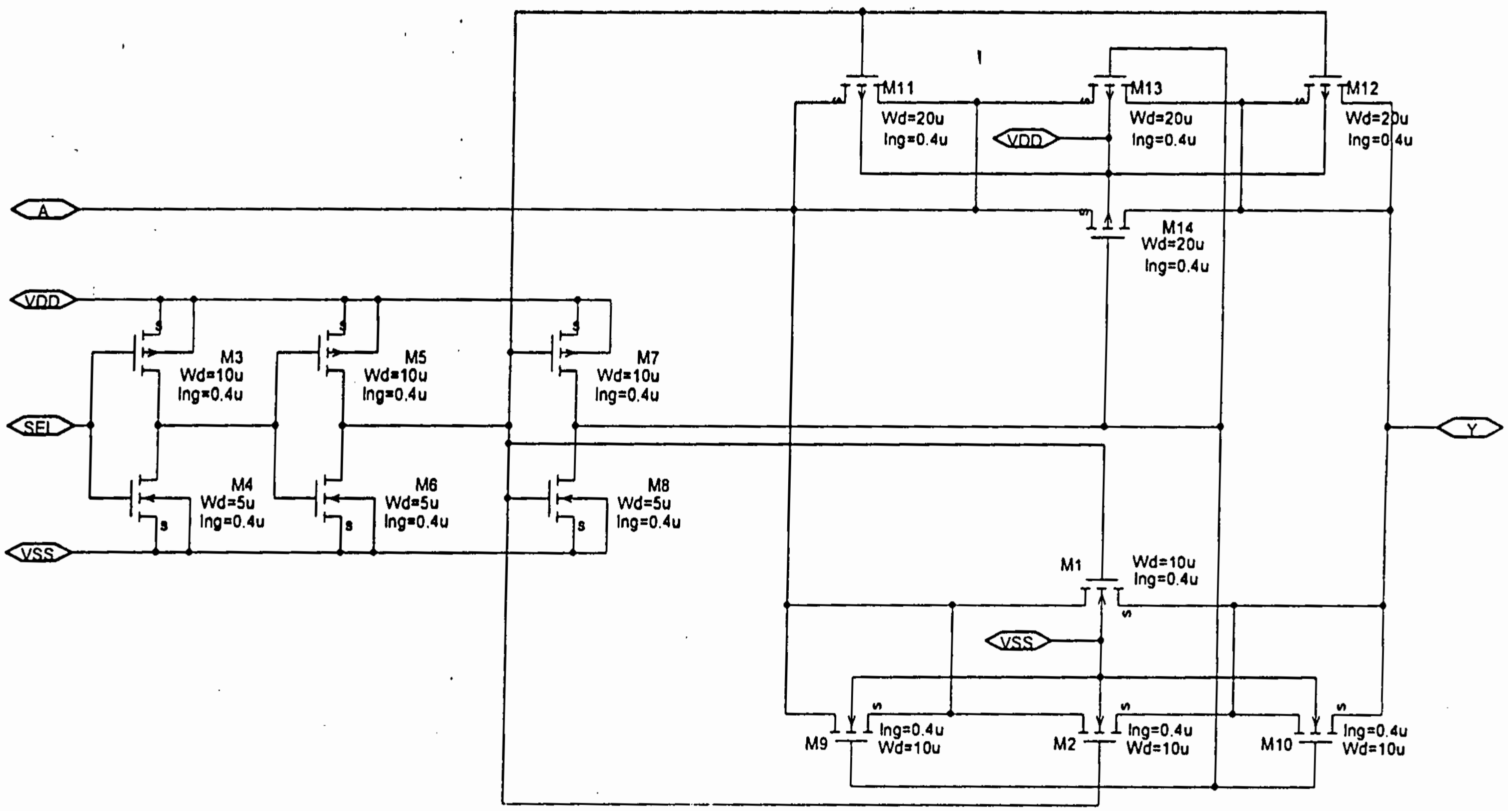


Fig. 131

09632856 .080400



A
VDD
SEL
VSS
Y
M11
Wd=20u
lng=0.4u
M13
Wd=20u
lng=0.4u
M12
Wd=20u
lng=0.4u
M14
Wd=20u
lng=0.4u
M3
Wd=10u
lng=0.4u
M5
Wd=10u
lng=0.4u
M7
Wd=10u
lng=0.4u
M4
Wd=5u
lng=0.4u
M6
Wd=5u
lng=0.4u
M8
Wd=5u
lng=0.4u
M1
Wd=10u
lng=0.4u
M9
lng=0.4u
Wd=10u
M2
lng=0.4u
Wd=10u
M10
lng=0.4u
Wd=10u

FIG. 132

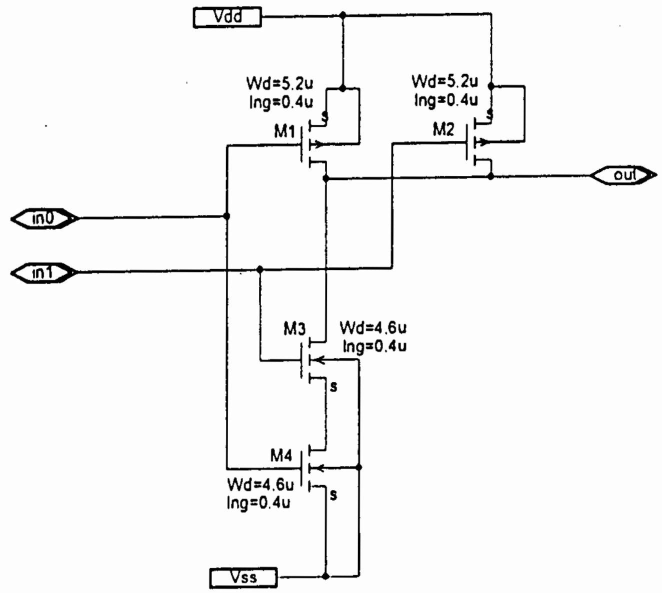

Vdd
Wd=5.2u
lng=0.4u
M1
s
Wd=5.2u
lng=0.4u
M2
s
out
in0
in1
M3
Wd=4.6u
lng=0.4u
s
M4
Wd=4.6u
lng=0.4u
s
Vss

FIG. 133

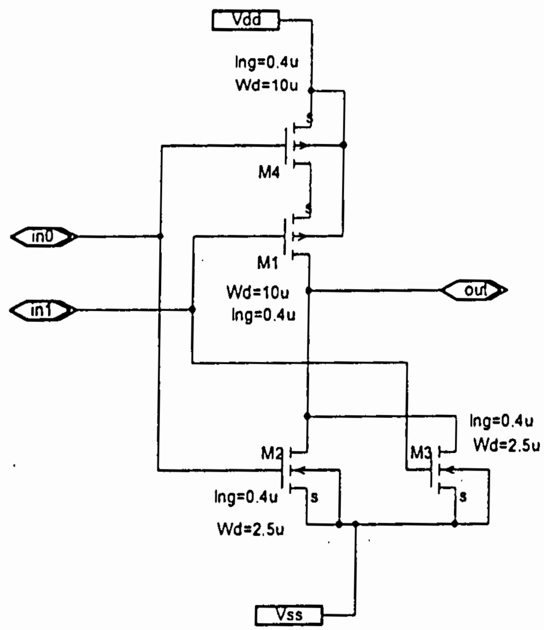


FIG. 134

09632356 .080400

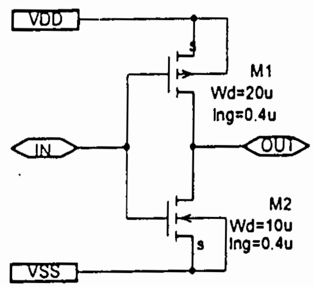


FIG. 135

09632856 .080400

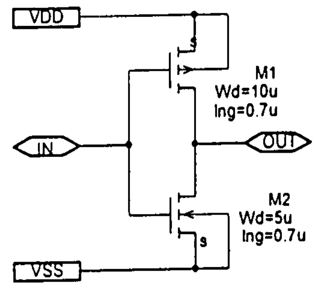


FIG. 136

09632856 .080400

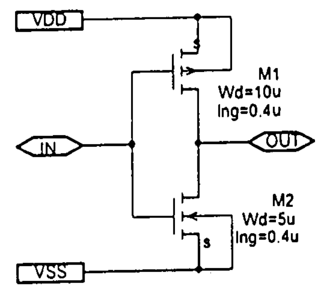


FIG 137

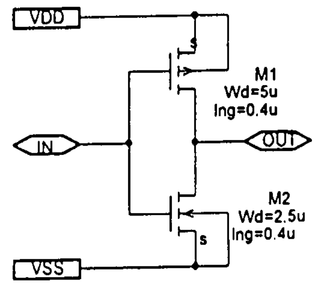


FIG. 138

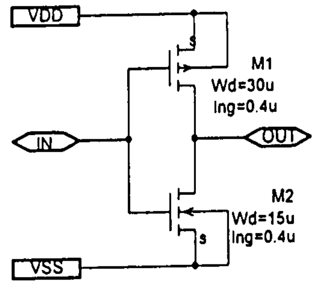


FIG. 139

09632856 .080400

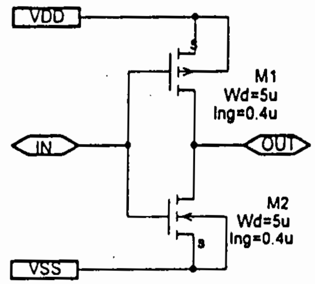


FIG. 140

09632856 .080400

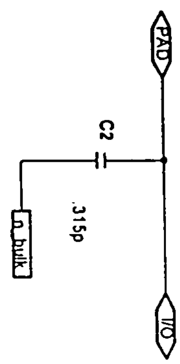


FIG. 141

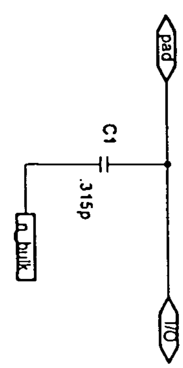


FIG. 142

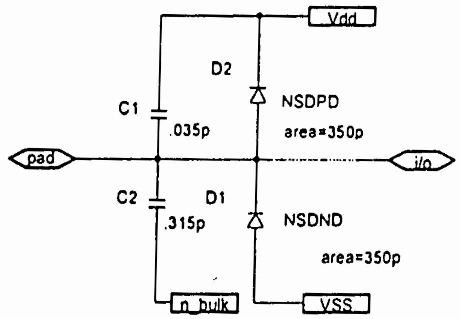
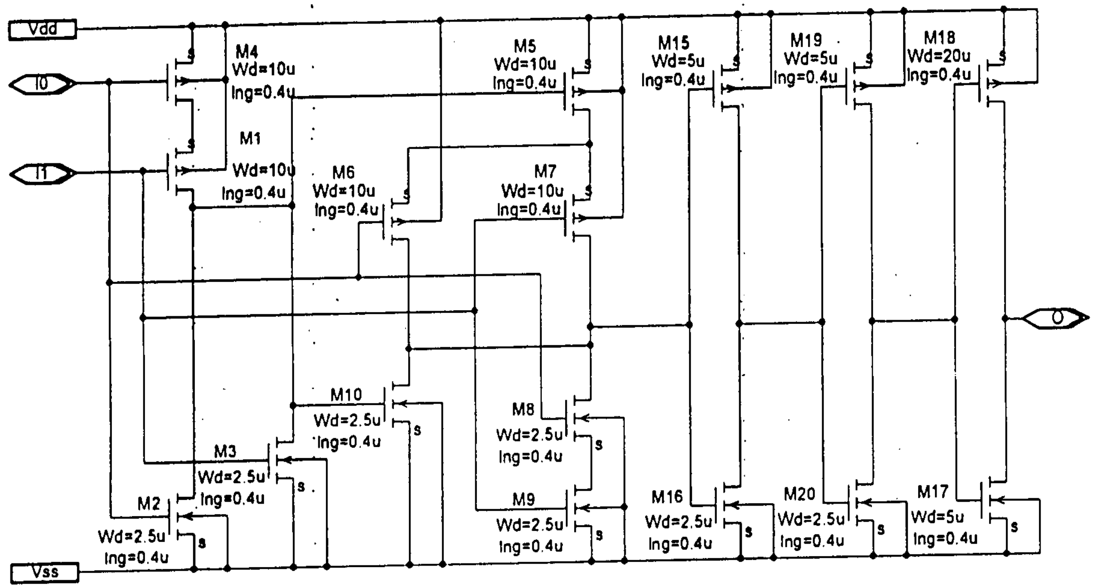


FIG 143

09632856 .080400



Vdd
I0
I1
Vss
O
M4
Wd=10u
lng=0.4u
M1
Wd=10u
lng=0.4u
M6
Wd=10u
lng=0.4u
M5
Wd=10u
lng=0.4u
M7
Wd=10u
lng=0.4u
M15
Wd=5u
lng=0.4u
M19
Wd=5u
lng=0.4u
M18
Wd=20u
lng=0.4u
M10
Wd=2.5u
lng=0.4u
M3
Wd=2.5u
lng=0.4u
M2
Wd=2.5u
lng=0.4u
M8
Wd=2.5u
lng=0.4u
M9
Wd=2.5u
lng=0.4u
M16
Wd=2.5u
lng=0.4u
M20
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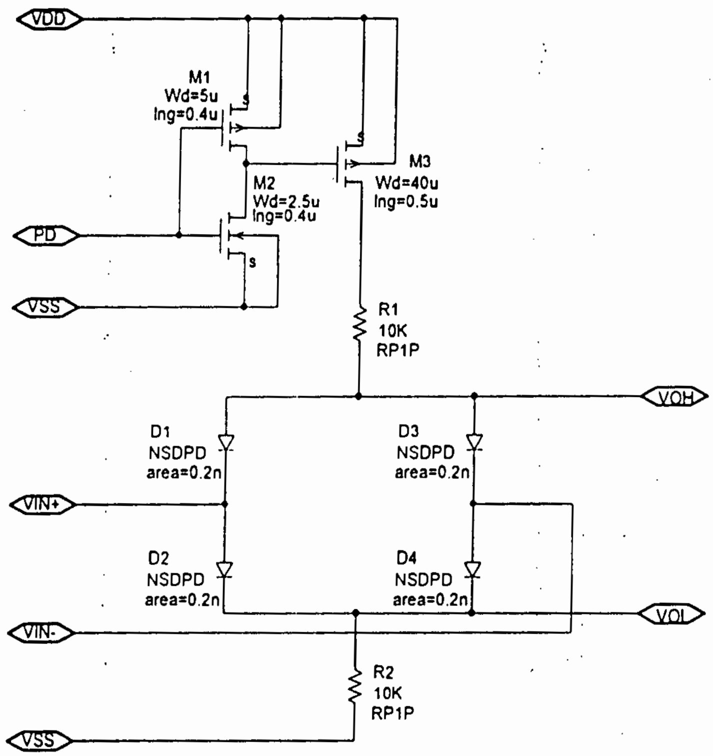
lng=0.4u
M17
Wd=5u
lng=0.4u

FIG 144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M1
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lng=0.4u
s
M3
Wd=40u
lng=0.5u
M2
Wd=2.5u
lng=0.4u
PD
s
VSS
R1
10K
RP1P
VOH
D1
NSDPD
area=0.2n
D3
NSDPD
area=0.2n
VIN+
D2
NSDPD
area=0.2n
D4
NSDPD
area=0.2n
VOL
VIN-
R2
10K
RP1P
VSS

FIG. 145

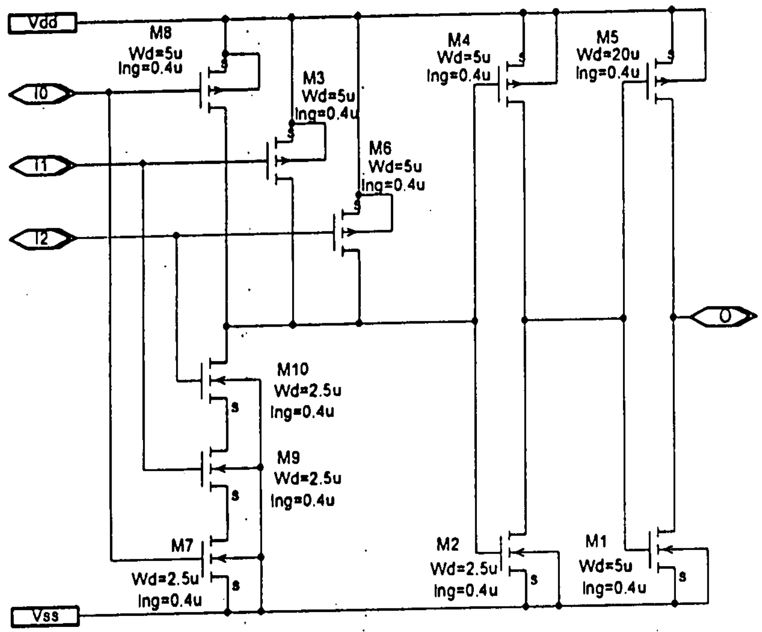

Vdd
I0
I1
I2
Vss
O
M8
Wd=5u
lng=0.4u
M3
Wd=5u
lng=0.4u
M6
Wd=5u
lng=0.4u
M4
Wd=5u
lng=0.4u
M5
Wd=20u
lng=0.4u
M10
Wd=2.5u
lng=0.4u
M9
Wd=2.5u
lng=0.4u
M7
Wd=2.5u
lng=0.4u
M2
Wd=2.5u
lng=0.4u
M1
Wd=5u
lng=0.4u

FIG. 146

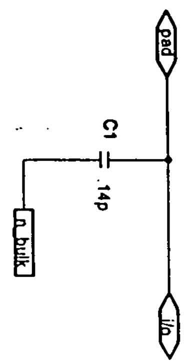


FIG. 147

09633856 .080400

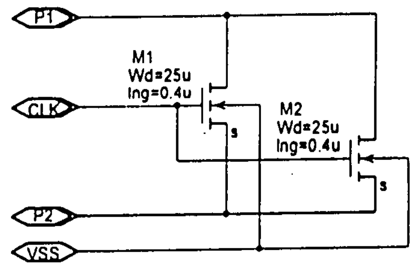
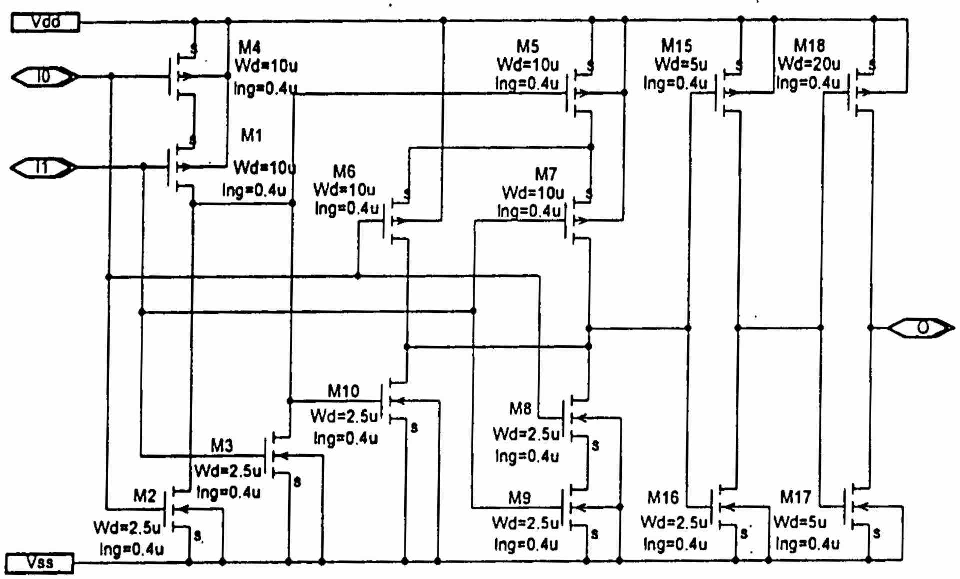


FIG. 148


Vdd
I0
I1
O
Vss
M4
Wd=10u
lng=0.4u
M1
Wd=10u
lng=0.4u
M6
Wd=10u
lng=0.4u
M5
Wd=10u
lng=0.4u
M7
Wd=10u
lng=0.4u
M15
Wd=5u
lng=0.4u
M18
Wd=20u
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M10
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M3
Wd=2.5u
lng=0.4u
M2
Wd=2.5u
lng=0.4u
M8
Wd=2.5u
lng=0.4u
M9
Wd=2.5u
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M16
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lng=0.4u
M17
Wd=5u
lng=0.4u

FIG. 149

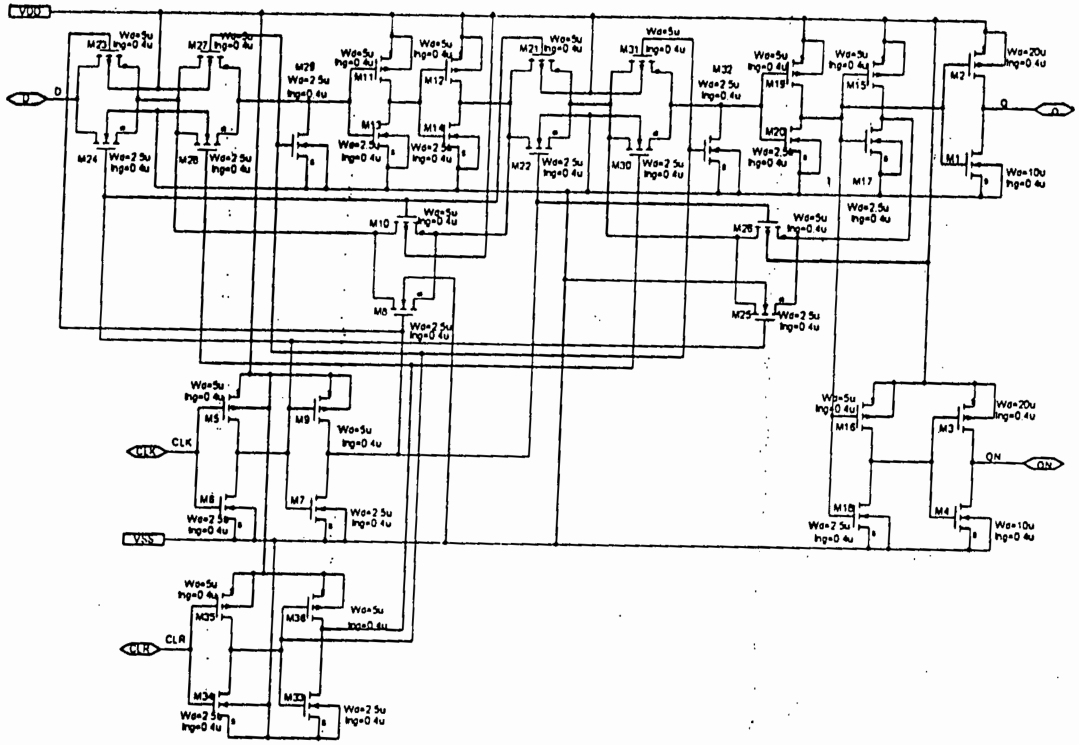

VDD
VSS
D
Q
QN
CLK
CLR
M1
M2
M3
M4
M5
M7
M8
M9
M10
M11
M12
M13
M14
M15
M16
M17
M18
M19
M20
M21
M22
M24
M25
M26
M27
M28
M29
M30
M31
M32
M33
M34
M35
M36

FIG. 150

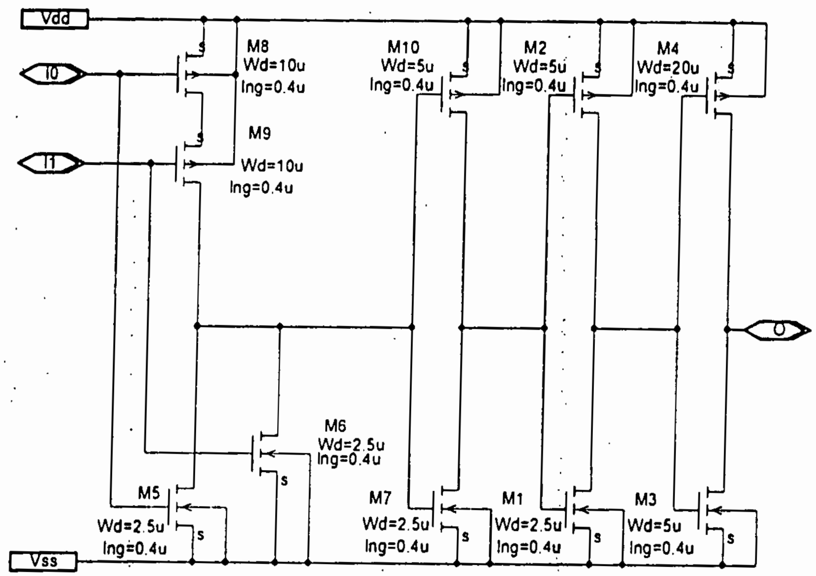
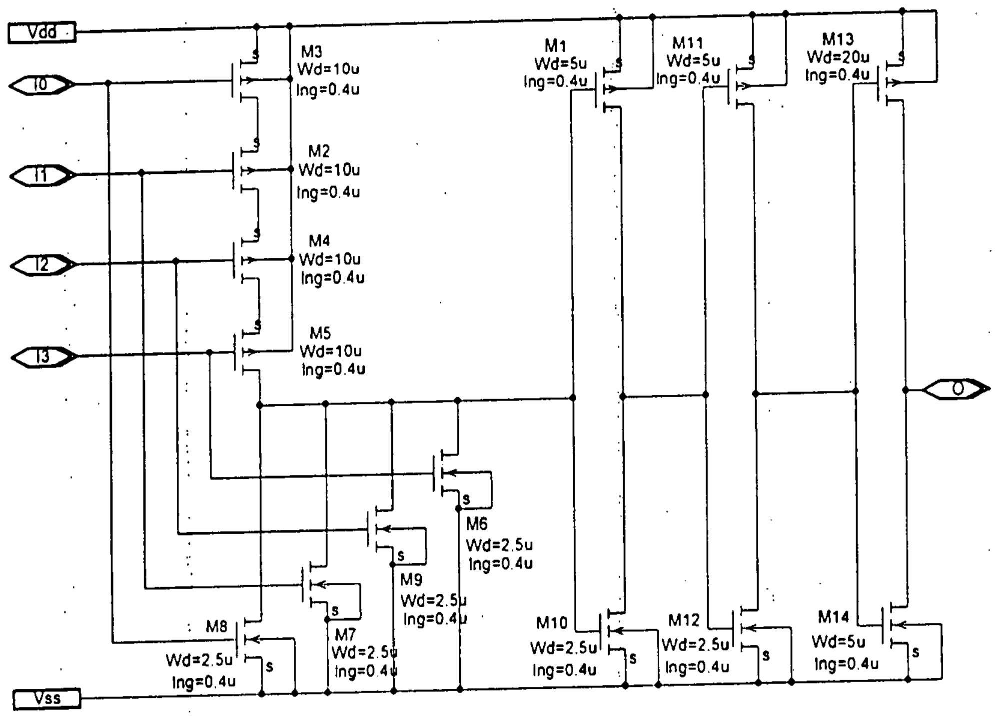

Vdd
I0
I1
M8
Wd=10u
lng=0.4u
M9
Wd=10u
lng=0.4u
M10
Wd=5u
lng=0.4u
M2
Wd=5u
lng=0.4u
M4
Wd=20u
lng=0.4u
O
M6
Wd=2.5u
lng=0.4u
M5
Wd=2.5u
lng=0.4u
M7
Wd=2.5u
lng=0.4u
M1
Wd=2.5u
lng=0.4u
M3
Wd=5u
lng=0.4u
Vss

FIG. 151



Vdd
I0
I1
I2
I3
M3
Wd=10u
lng=0.4u
M2
Wd=10u
lng=0.4u
M4
Wd=10u
lng=0.4u
M5
Wd=10u
lng=0.4u
M1
Wd=5u
lng=0.4u
M11
Wd=5u
lng=0.4u
M13
Wd=20u
lng=0.4u
O
M6
Wd=2.5u
lng=0.4u
M9
Wd=2.5u
lng=0.4u
M7
Wd=2.5u
lng=0.4u
M8
Wd=2.5u
lng=0.4u
M10
Wd=2.5u
lng=0.4u
M12
Wd=2.5u
lng=0.4u
M14
Wd=5u
lng=0.4u
Vss

FIG. 152

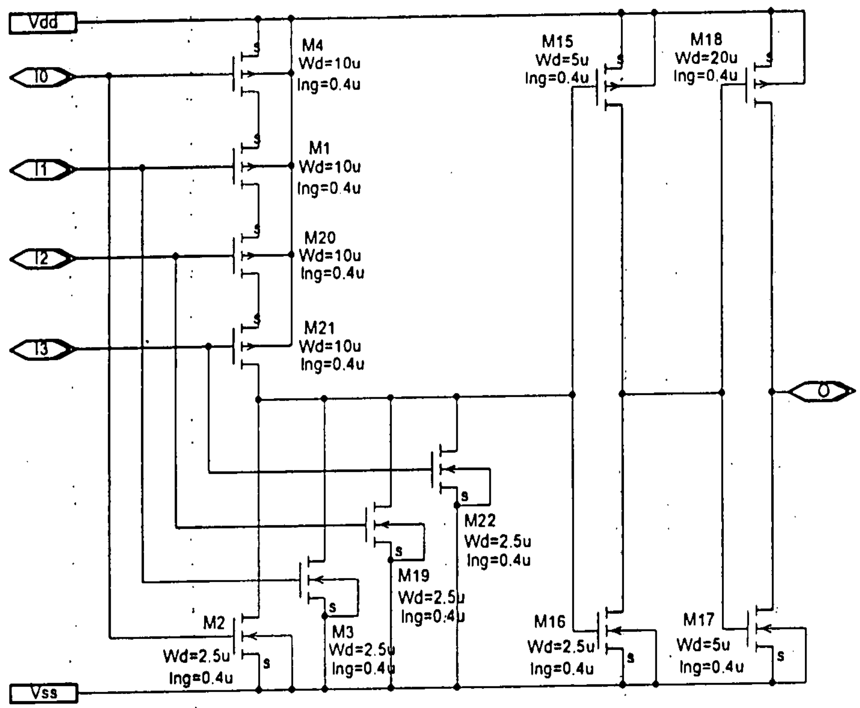


FIG. 153

09632856 .080400

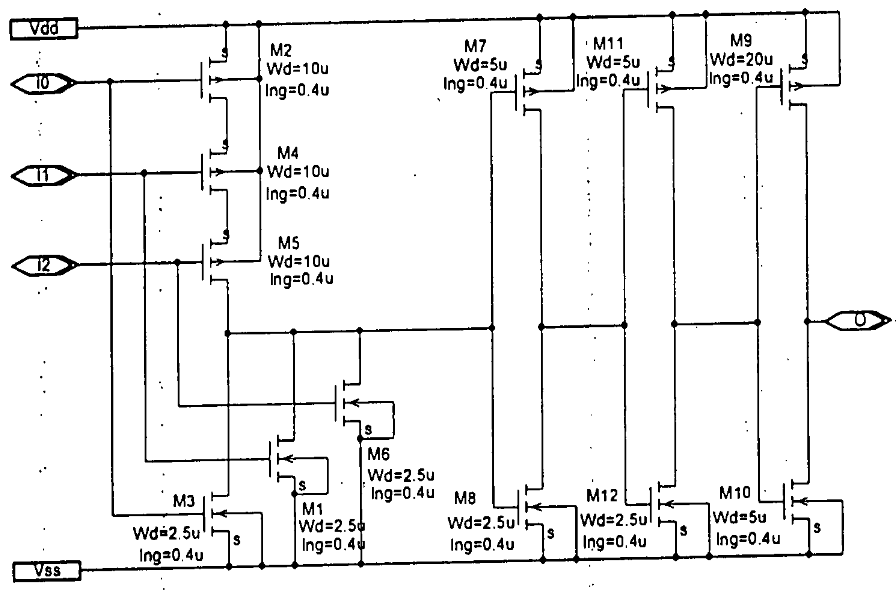

Vdd
I0
I1
I2
O
Vss
M2
Wd=10u
lng=0.4u
M4
Wd=10u
lng=0.4u
M5
Wd=10u
lng=0.4u
M7
Wd=5u
lng=0.4u
M11
Wd=5u
lng=0.4u
M9
Wd=20u
lng=0.4u
M6
Wd=2.5u
lng=0.4u
M3
Wd=2.5u
lng=0.4u
M1
Wd=2.5u
lng=0.4u
M8
Wd=2.5u
lng=0.4u
M12
Wd=2.5u
lng=0.4u
M10
Wd=5u
lng=0.4u

FIG. 154

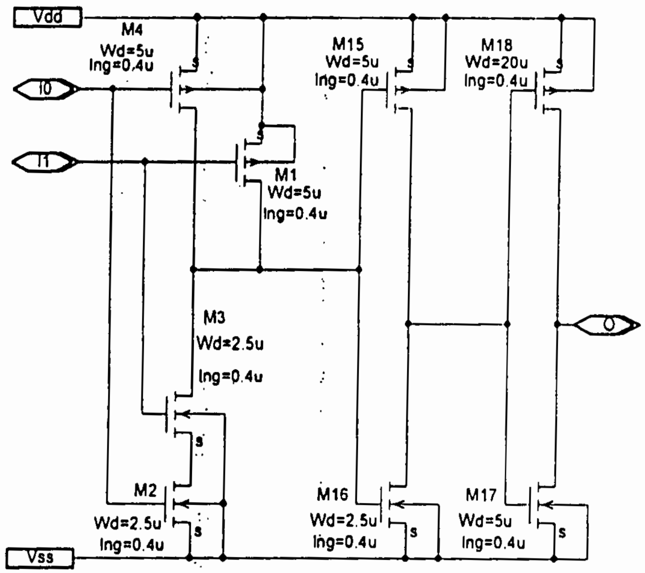


FIG. 155

09632856 .080400

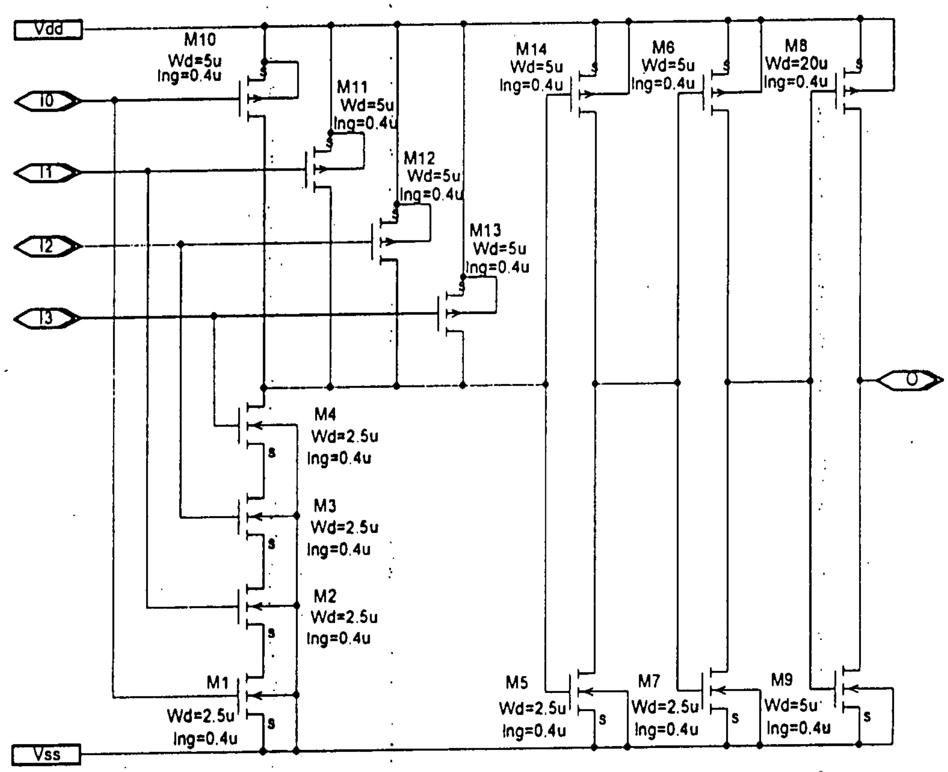


FIG. 156

09632856 .020400

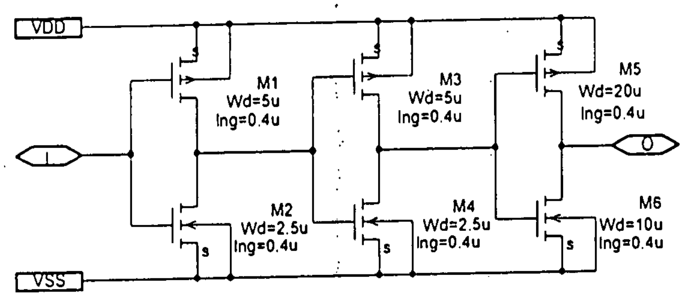


FIG. 157

09632856 .080400

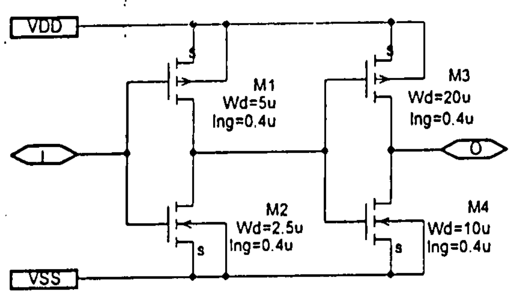


FIG. 158

08632256 .080400

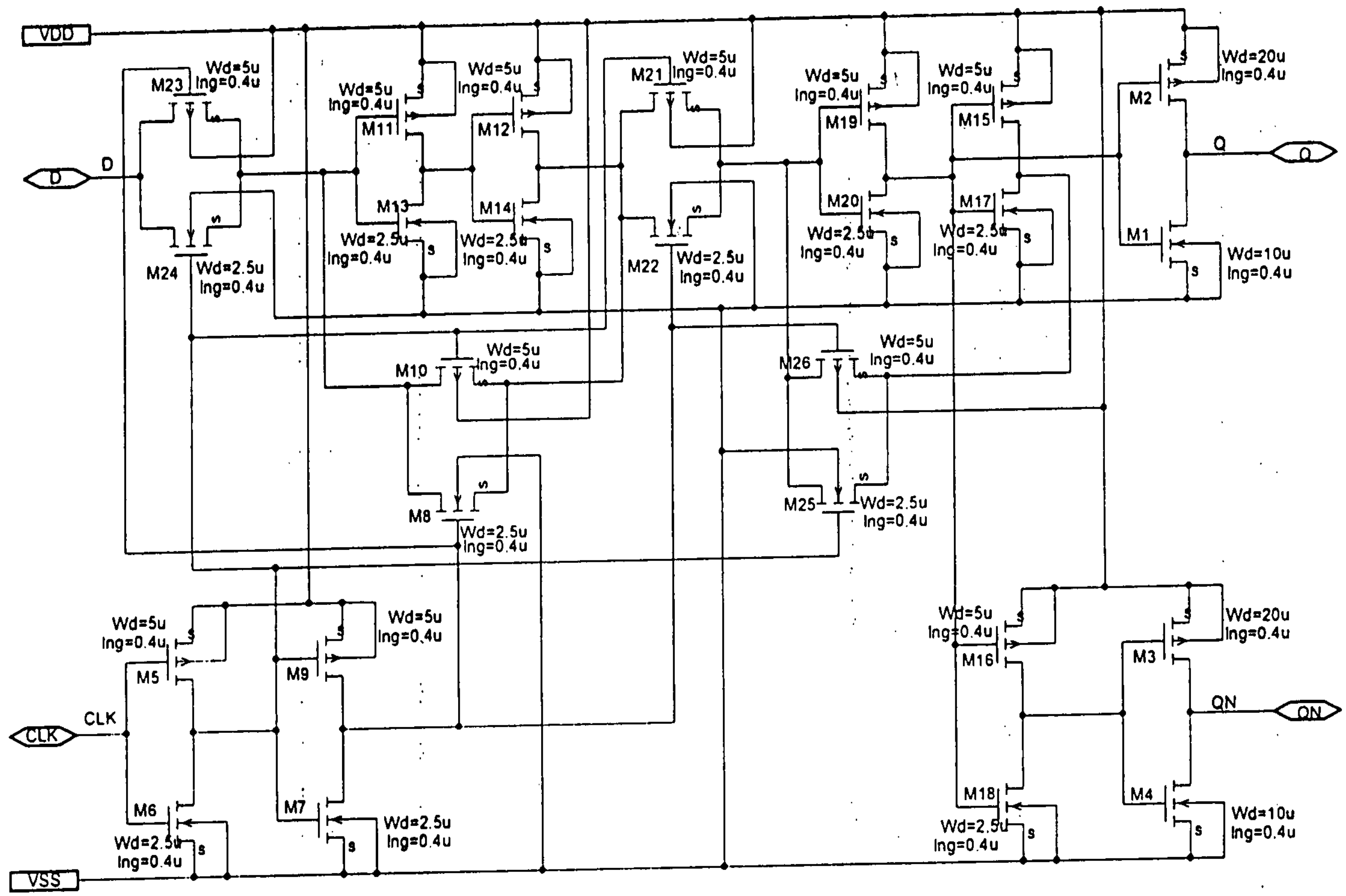


FIG 159

09632856 .080400

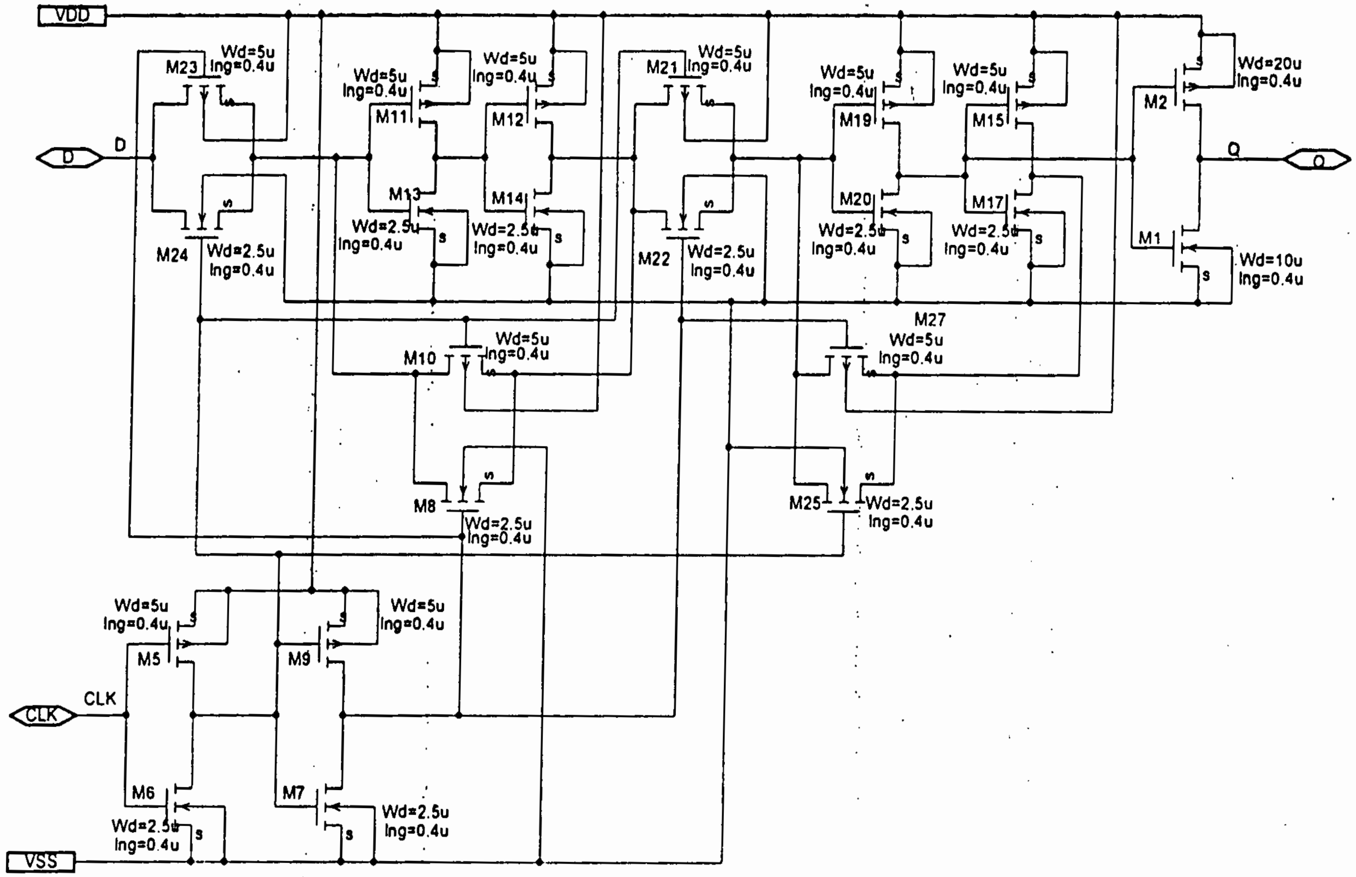


FIG. 160

09632256 .080400

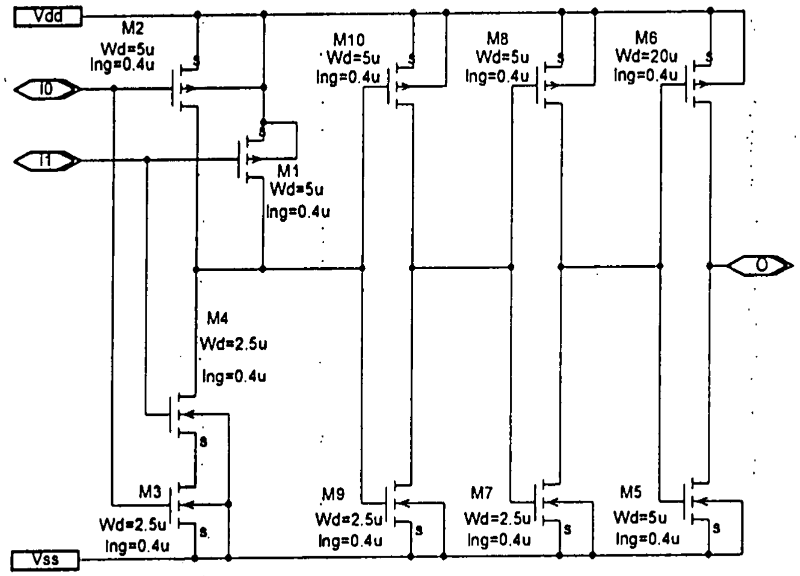


FIG 161

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The structure and operation of embodiments of the UFT module, and various applications of the same are described in detail in the following sections.

Further features and advantages of the invention, as well as the structure and operation of various embodiments of the invention, are described in detail below with reference to the accompanying drawings. The drawing in which an element first appears is typically indicated by the leftmost character(s) and/or digit(s) in the corresponding reference number.

Brief Description of the Figures

The present invention will be described with reference to the accompanying drawings, wherein:

FIG. 1A is a block diagram of a universal frequency translation (UFT) module according to an embodiment of the invention;

FIG. 1B is a more detailed diagram of a universal frequency translation (UFT) module according to an embodiment of the invention;

FIG. 1C illustrates a UFT module used in a universal frequency down-conversion (UFD) module according to an embodiment of the invention;

FIG. 1D illustrates a UFT module used in a universal frequency up-conversion (UFU) module according to an embodiment of the invention;

FIG. 2A-2B illustrate block diagrams of universal frequency translation (UFT) modules according to an embodiment of the invention;

FIG. 3 is a block diagram of a universal frequency up-conversion (UFU) module according to an embodiment of the invention;

FIG. 4 is a more detailed diagram of a universal frequency up-conversion (UFU) module according to an embodiment of the invention;

FIG. 5 is a block diagram of a universal frequency up-conversion (UFU) module according to an alternative embodiment of the invention;

FIGS. 6A-6I illustrate example waveforms used to describe the operation of the UFU module;

FIG. 7 illustrates a UFT module used in a receiver according to an embodiment of the invention;

FIG. 8 illustrates a UFT module used in a transmitter according to an embodiment of the invention;

FIG. 9 illustrates an environment comprising a transmitter and a receiver, each of which may be implemented using a UFT module of the invention;

FIG. 10 illustrates a transceiver according to an embodiment of the invention;

FIG. 11 illustrates a transceiver according to an alternative embodiment of the invention;

FIG. 12 illustrates an environment comprising a transmitter and a receiver, each of which may be implemented using enhanced signal reception (ESR) components of the invention;

FIG. 13 illustrates a UFT module used in a unified down-conversion and filtering (UDF) module according to an embodiment of the invention;

FIG. 14 illustrates an example receiver implemented using a UDF module according to an embodiment of the invention;

FIGS. 15A-15F illustrate example applications of the UDF module according to embodiments of the invention;

FIG. 16 illustrates an environment comprising a transmitter and a receiver, each of which may be implemented using enhanced signal reception (ESR) components of the invention, wherein the receiver may be further implemented using one or more UFD modules of the invention;

FIG. 17 illustrates a unified down-converting and filtering (UDF) module according to an embodiment of the invention;

FIG. 18 is a table of example values at nodes in the UDF module of FIG. 19;

FIG. 19 is a detailed diagram of an example UDF module according to an embodiment of the invention;

FIGS. 20A and 20A-1 are example aliasing modules according to embodiments of the invention;

FIGS. 20B-20F are example waveforms used to describe the operation of the aliasing modules of FIGS. 20A and 20A-1;

FIG. 21 illustrates an enhanced signal reception system according to an embodiment of the invention;

FIGS. 22A-22F are example waveforms used to describe the system of FIG. 21;

FIG. 23A illustrates an example transmitter in an enhanced signal reception system according to an embodiment of the invention;

FIGS. 23B and 23C are example waveforms used to further describe the enhanced signal reception system according to an embodiment of the invention;

FIG. 23D illustrates another example transmitter in an enhanced signal reception system according to an embodiment of the invention;

FIGS. 23E and 23F are example waveforms used to further describe the enhanced signal reception system according to an embodiment of the invention;

FIG. 24A illustrates an example receiver in an enhanced signal reception system according to an embodiment of the invention;

FIGS. 24B-24J are example waveforms used to further describe the enhanced signal reception system according to an embodiment of the invention;

FIG. 25 illustrates a block diagram of an example computer network;

FIG. 26 illustrates a block diagram of an example computer network;

FIG. 27 illustrates a block diagram of an example wireless interface;

FIG. 28 illustrates an example heterodyne implementation of the wireless interface illustrated in FIG. 27;

FIG. 29 illustrates an example in-phase/quadrature-phase (I/Q) heterodyne implementation of the interface illustrated in FIG. 27;

FIG. 30 illustrates an example high level block diagram of the interface illustrated in FIG. 27, in accordance with the present invention;

FIG. 31 illustrates a example block diagram of the interface illustrated in FIG. 29, in accordance with the invention;

FIG. 32 illustrates an example I/Q implementation of the interface illustrated in FIG.31;

FIGS. 33-38 illustrate example environments encompassed by the invention;

FIG. 39 illustrates a block diagram of a WLAN interface according to an embodiment of the invention;

FIG. 40 illustrates a WLAN receiver according to an embodiment of the invention;

FIG. 41 illustrates a WLAN transmitter according to an embodiment of the invention;

FIGS. 42-44 are example implementations of a WLAN interface;

FIGS. 45, 46A, and 46B relate to an example MAC interface for an example WLAN interface embodiment;

FIGS. 47, 48, 49A, and 49B relate to an example demodulator/modulator facilitation module for an example WLAN interface embodiment;

FIGS. 50, 51, 52A, 52B, and 52C relate to an example alternate demodulator/modulator facilitation module for an example WLAN interface embodiment;

FIGS. 53 and 54 relate to an example receiver for an example WLAN interface embodiment;

FIGS. 55, 56A, and 56B relate to an example synthesizer for an example WLAN interface embodiment;

FIGS. 57, 58, 59, 60, 61A, and 61B relate to an example transmitter for an example WLAN interface embodiment;

FIGS. 62 and 63 relate to an example motherboard for an example WLAN interface embodiment;

FIGS. 64-66 relate to example LNAs for an example WLAN interface embodiment;

FIGS. 67A-B illustrate IQ receivers having UFT modules in a series and shunt configurations, according to embodiments of the invention;

FIGS. 68A-B illustrate IQ receivers having UFT modules with delayed control signals for quadrature implementation, according to embodiments of the present invention;

FIGS. 69A-B illustrate IQ receivers having FET implementations, according to embodiments of the invention;

FIG. 70A illustrates an IQ receiver having shunt UFT modules according to embodiments of the invention;

FIG. 70B illustrates control signal generator embodiments for receiver 7000 according to embodiments of the invention;

FIGS. 70C-D illustrate various control signal waveforms according to embodiments of the invention;

FIG. 70E illustrates an example IQ modulation receiver embodiment according to embodiments of the invention;

FIGS. 70F-P illustrate example waveforms that are representative of the IQ receiver in FIG. 70E;

FIGS. 70Q-R illustrate single channel receiver embodiments according to embodiments of the invention;

FIG. 70S illustrates a FET configuration of an IQ receiver embodiment according to embodiments of the invention;

FIG. 71A illustrate a balanced transmitter 7102, according to an embodiment of the present invention;

FIGs. 71B-C illustrate example waveforms that are associated with the balanced transmitter 7102, according to an embodiment of the present invention;

FIG. 71D illustrates example FET configurations of the balanced transmitter 7102, according to embodiments of the present invention;

FIGs. 72A-I illustrate various example timing diagrams that are associated with the transmitter 7102, according to embodiments of the present invention;

FIG. 72J illustrates an example frequency spectrum that is associated with a modulator 7104, according to embodiments of the present invention;

FIG. 73A illustrate a transmitter 7302 that is configured for carrier insertion, according to embodiments of the present invention;

FIG. 73B illustrates example signals associated with the transmitter 7302, according to embodiments of the invention;

FIG. 74 illustrates an IQ balanced transmitter 7420, according to embodiments of the present invention;

FIGs. 75A-C illustrate various example signal diagrams associated with the balanced transmitter 7420 in FIG. 74;

FIG. 76A illustrates an IQ balanced transmitter 7608 according to embodiments of the invention;

FIG. 76B illustrates an IQ balanced modulator 7618 according to embodiments of the invention;

FIG. 77 illustrates an IQ balanced modulator 7702 configured for carrier insertion according to embodiments of the invention;

FIG. 78 illustrates an IQ balanced modulator 7802 configured for carrier insertion according to embodiments of the invention;

FIG. 79A illustrate a transmitter 7900, according to embodiments of the present invention;

FIGs. 79B-C illustrate various frequency spectrums that are associated with the transmitter 7900;

FIG. 79D illustrates a FET configuration for the transmitter 7900, according to embodiments of the present invention;

FIG. 80 illustrates an IQ transmitter 8000, according to embodiments of the present invention;

FIGs. 81A-C illustrate various frequency spectrums that are associated with the IQ transmitter 8000, according to embodiments of the present invention;

FIG. 82 illustrates an IQ transmitter 8200, according to embodiments of the present invention;

FIG. 83 illustrates an IQ transmitter 8300, according to embodiments of the invention;

FIG. 84 illustrates a flowchart 8400 that is associated with the transmitter 7102 in the FIG. 71A, according to embodiments of the invention;

FIG. 85 illustrates a flowchart 8500 that further defines the flowchart 8400 in the FIG. 84, and is associated with the transmitter 7102 according to embodiments of the invention;

FIG. 86 illustrates a flowchart 8600 that is associated with the transmitter 7900 and further defines the flowchart 8400 in the FIG. 84, according to embodiments of the invention;

FIG. 87 illustrates a flowchart 8700, that is associated with the transmitter 7420 in the FIG. 74, according to embodiments of the invention;

FIG. 88 illustrates a flowchart 8800 that is associated with the transmitter 8000, according to embodiments of the invention;

FIG. 89A illustrate a pulse generator according to embodiments of the invention;

FIGS. 89B-C illustrate various example signal diagrams associated with the pulse generator in FIG. 89A, according to embodiments of the invention;

FIG. 89D-E illustrate various example pulse generators according to embodiments of the present invention;

FIGS. 90A-D illustrates various implementation circuits for the modulator 7410, according to embodiments of the present invention;

FIG. 91 illustrates an IQ transceiver 9100 according to embodiments of the present invention;

FIG. 92 illustrates direct sequence spread spectrum according to embodiments of the present invention;

FIG. 93 illustrates the LNA/PA module 3904 according to embodiments of the present invention;

FIG. 94 illustrates a WLAN device 9400, according to embodiments of the invention of the present invention; and

FIGs. 95A-C, and FIGs. 96-161 illustrate schematics for an integrated circuit implementation example of the present invention.

Detailed Description of the Preferred Embodiments

Table of Contents

1. Universal Frequency Translation

The present invention is related to frequency translation, and applications of same. Such applications include, but are not limited to, frequency down-conversion, frequency up-conversion, enhanced signal reception, unified down-conversion and filtering, and combinations and applications of same.

FIG. 1A illustrates a universal frequency translation (UFT) module 102 according to embodiments of the invention. (The UFT module is also sometimes called a universal frequency translator, or a universal translator.)

As indicated by the example of FIG. 1A, some embodiments of the UFT module 102 include three ports (nodes), designated in FIG. 1A as Port 1, Port 2, and Port 3. Other UFT embodiments include other than three ports.

Generally, the UFT module 102 (perhaps in combination with other components) operates to generate an output signal from an input signal, where the frequency of the output signal differs from the frequency of the input signal. In other words, the UFT module 102 (and perhaps other components) operates to generate the output signal from the input signal by translating the frequency (and perhaps other characteristics) of the input signal to the frequency (and perhaps other characteristics) of the output signal.

An example embodiment of the UFT module 103 is generally illustrated in FIG. 1B. Generally, the UFT module 103 includes a switch 106 controlled by a control signal 108. The switch 106 is said to be a controlled switch.

As noted above, some UFT embodiments include other than three ports. For example, and without limitation, FIG. 2 illustrates an example UFT module 202. The example UFT module 202 includes a diode 204 having two ports, designated as Port 1 and Port 2/3. This embodiment does not include a third port, as indicated by the dotted line around the "Port 3" label.

The UFT module is a very powerful and flexible device. Its flexibility is illustrated, in part, by the wide range of applications in which it can be used. Its power is illustrated, in part, by the usefulness and performance of such applications.

For example, a UFT module 115 can be used in a universal frequency down-conversion (UFD) module 114, an example of which is shown in FIG. 1C. In this capacity, the UFT module 115 frequency down-converts an input signal to an output signal.

As another example, as shown in FIG. 1D, a UFT module 117 can be used in a universal frequency up-conversion (UFU) module 116. In this capacity, the UFT module 117 frequency up-converts an input signal to an output signal.

These and other applications of the UFT module are described below. Additional applications of the UFT module will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. In some applications, the UFT module is a required component. In other applications, the UFT module is an optional component.

2. *Frequency Down-Conversion*

The present invention is directed to systems and methods of universal frequency down-conversion, and applications of same.

In particular, the following discussion describes down-converting using a Universal Frequency Translation Module. The down-conversion of an EM signal by aliasing the EM signal at an aliasing rate is fully described in co-pending U.S. Patent Application entitled "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed October 21, 1998, issued as U.S. Patent No. 6,061,551 on May 9, 2000, the full disclosure of which is incorporated herein by reference. A relevant portion of the above mentioned patent application is summarized below to describe down-converting an input signal to produce a down-converted signal that exists at a lower frequency or a baseband signal.

FIG. 20A illustrates an aliasing module 2000 (also called a universal frequency down-conversion module) for down-conversion using a universal frequency translation (UFT) module 2002 which down-converts an EM input signal 2004. In particular embodiments, aliasing module 2000 includes a switch 2008 and a capacitor 2010. The electronic alignment of the circuit components is flexible. That is, in one implementation, the switch 2008 is in series with input signal 2004 and capacitor 2010 is shunted to ground (although it may be other than ground in configurations such as differential mode). In a second implementation (see FIG. 20A-1), the capacitor 2010 is in series with the input signal 2004 and the switch 2008 is shunted to ground (although it may be other than ground in configurations such as differential mode). Aliasing module 2000 with UFT module 2002 can be easily tailored to down-convert a wide variety of electromagnetic signals using aliasing frequencies that are well below the frequencies of the EM input signal 2004.

In one implementation, aliasing module 2000 down-converts the input signal 2004 to an intermediate frequency (IF) signal. In another implementation, the aliasing module 2000 down-converts the input signal 2004 to a demodulated baseband signal. In yet another implementation, the input signal 2004 is a frequency modulated (FM) signal, and the aliasing module 2000 down-converts it to a non-FM signal, such as a phase modulated (PM) signal or an amplitude modulated (AM) signal. Each of the above implementations is described below.

In an embodiment, the control signal 2006 includes a train of pulses that repeat at an aliasing rate that is equal to, or less than, twice the frequency of the input signal 2004. In this embodiment, the control signal 2006 is referred to herein as an aliasing signal because it is below the Nyquist rate for the frequency of the input signal 2004. Preferably, the frequency of control signal 2006 is much less than the input signal 2004.

A train of pulses 2018 as shown in FIG. 20D controls the switch 2008 to alias the input signal 2004 with the control signal 2006 to generate a down-converted output signal 2012. More specifically, in an embodiment, switch 2008 closes on a first edge of each pulse 2020 of FIG. 20D and opens on a second edge of each pulse. When the switch 2008 is closed, the input signal 2004 is coupled to the capacitor 2010, and charge is transferred from the input signal to the capacitor 2010. The charge stored during successive pulses forms down-converted output signal 2012.

Exemplary waveforms are shown in FIGS. 20B-20F.

FIG. 20B illustrates an analog amplitude modulated (AM) carrier signal 2014 that is an example of input signal 2004. For illustrative purposes, in FIG. 20C, an analog AM carrier signal portion 2016 illustrates a portion of the analog AM carrier signal 2014 on an expanded time scale. The analog AM carrier signal portion 2016 illustrates the analog AM carrier signal 2014 from time t_0 to time t_1.

FIG. 20D illustrates an exemplary aliasing signal 2018 that is an example of control signal 2006. Aliasing signal 2018 is on approximately the same time scale as the analog AM carrier signal portion 2016. In the example shown in FIG. 20D, the aliasing signal 2018 includes a train of pulses 2020 having negligible apertures that tend towards zero (the invention is not limited to this embodiment, as discussed below). The pulse aperture may also be referred to as the pulse width as will be understood by those skilled in the art(s). The pulses 2020 repeat at an aliasing rate, or pulse repetition rate of aliasing signal 2018. The aliasing rate is determined as described below, and further described in co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," Application No. 09/176,022, Attorney Docket Number 1744.0010000, issued as U.S. Patent No. 6,061,551 on May 9, 2000.

As noted above, the train of pulses 2020 (i.e., control signal 2006) control the switch 2008 to alias the analog AM carrier signal 2016 (i.e., input signal 2004) at the aliasing rate of the aliasing signal 2018. Specifically, in this embodiment, the switch 2008 closes on a first edge of each pulse and opens on a second edge of each pulse. When the switch 2008 is closed, input signal 2004 is coupled to the capacitor 2010, and charge is transferred from the input signal 2004 to the capacitor 2010. The charge transferred during a pulse is referred to herein as an under-sample. Exemplary under-samples 2022 form down-converted signal portion 2024 (FIG. 20E) that corresponds to the analog AM carrier signal portion 2016 (FIG. 20C) and the train of pulses 2020 (FIG. 20D). The charge stored during successive under-samples of AM carrier signal 2014 form the down-converted signal 2024 (FIG. 20E) that is an example of down-converted output signal 2012 (FIG. 20A). In FIG. 20F, a demodulated baseband signal 2026 represents the demodulated baseband signal 2024 after filtering on a compressed time scale. As illustrated, down-converted signal 2026 has substantially the same "amplitude envelope" as AM carrier signal 2014. Therefore, FIGS. 20B-20F illustrate down-conversion of AM carrier signal 2014.

The waveforms shown in FIGS. 20B-20F are discussed herein for illustrative purposes only, and are not limiting. Additional exemplary time domain and frequency domain drawings, and exemplary methods and systems of the invention relating thereto, are disclosed in co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," Application No. 09/176,022, Attorney Docket Number 1744.0010000, issued as U.S. Patent No. 6,061,551 on May 9, 2000.

The aliasing rate of control signal 2006 determines whether the input signal 2004 is down-converted to an IF signal, down-converted to a demodulated baseband signal, or down-converted from an FM signal to a PM or an AM signal. Generally, relationships between the input signal 2004, the aliasing rate of the control signal 2006, and the down-converted output signal 2012 are illustrated below:

$$\text{(Freq. of input signal 2004)} = n\bullet\text{(Freq. of control signal 2006)} \pm \text{(Freq. of down-converted output signal 2012)}$$

For the examples contained herein, only the "+" condition will be discussed. The value of n represents a harmonic or sub-harmonic of input signal 2004 (e.g., $n = 0.5, 1, 2, 3, \ldots$).

When the aliasing rate of control signal 2006 is off-set from the frequency of input signal 2004, or off-set from a harmonic or sub-harmonic thereof, input signal 2004 is down-converted to an IF signal. This is because the under-sampling pulses occur at different phases of subsequent cycles of input signal 2004. As a result, the under-samples form a lower frequency oscillating pattern. If the input signal 2004 includes lower frequency changes, such as amplitude, frequency, phase, etc., or any combination thereof, the charge stored during associated under-samples reflects the lower frequency changes, resulting in similar changes on the down-converted IF signal. For example, to down-convert a 901 MHZ input signal to a 1 MHZ IF signal, the frequency of the control signal 2006 would be calculated as follows:

$$(\text{Freq}_{\text{input}} - \text{Freq}_{\text{IF}})/n = \text{Freq}_{\text{control}}$$

$$(901\text{ MHZ} - 1\text{ MHZ})/n \quad = 900/n$$

For $n = 0.5, 1, 2, 3, 4$, etc., the frequency of the control signal 2006 would be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc.

Exemplary time domain and frequency domain drawings, illustrating down-conversion of analog and digital AM, PM and FM signals to IF signals, and exemplary methods and systems thereof, are disclosed in co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," Application No. 09/176,022, Attorney Docket Number 1744.0010000, issued as U.S. Patent No. 6,061,551 on May 9, 2000.

Alternatively, when the aliasing rate of the control signal 2006 is substantially equal to the frequency of the input signal 2004, or substantially equal to a harmonic or sub-harmonic thereof, input signal 2004 is directly down-converted to a demodulated baseband signal. This is because, without modulation, the under-sampling pulses occur at the same point of subsequent cycles of the input signal 2004. As a result, the under-samples form a constant output baseband signal. If the input signal 2004 includes lower frequency changes, such as amplitude, frequency, phase, etc., or any combination thereof, the charge stored during associated under-samples reflects the lower frequency changes, resulting in similar changes on the demodulated baseband signal. For example, to directly down-convert a 900 MHZ input signal to a demodulated baseband signal (i.e., zero IF), the frequency of the control signal 2006 would be calculated as follows:

$$(\text{Freq}_{\text{input}} - \text{Freq}_{\text{IF}})/n = \text{Freq}_{\text{control}}$$
$$(900\text{ MHZ} - 0\text{ MHZ})/n \quad = 900\text{ MHZ}/n$$

For $n = 0.5, 1, 2, 3, 4$, etc., the frequency of the control signal 2006 should be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc.

Exemplary time domain and frequency domain drawings, illustrating direct down-conversion of analog and digital AM and PM signals to demodulated baseband signals, and exemplary methods and systems thereof, are disclosed in the co-pending U.S. Patent

Application entitled "Method and System for Down-converting Electromagnetic Signals," Application No. 09/176,022, issued as U.S. Patent No. 6,061,551 on May 9, 2000.

Alternatively, to down-convert an input FM signal to a non-FM signal, a frequency within the FM bandwidth must be down-converted to baseband (i.e., zero IF). As an example, to down-convert a frequency shift keying (FSK) signal (a sub-set of FM) to a phase shift keying (PSK) signal (a subset of PM), the mid-point between a lower frequency F_1 and an upper frequency F_2 (that is, $[(F_1 + F_2) \div 2]$) of the FSK signal is down-converted to zero IF. For example, to down-convert an FSK signal having F_1 equal to 899 MHZ and F_2 equal to 901 MHZ, to a PSK signal, the aliasing rate of the control signal 2006 would be calculated as follows:

$$\begin{aligned} \text{Frequency of the input} &= (F_1 + F_2) \div 2 \\ &= (899\text{ MHZ} + 901\text{ MHZ}) \div 2 \\ &= 900\text{ MHZ} \end{aligned}$$

Frequency of the down-converted signal = 0 (i.e., baseband)

$$(\text{Freq}_{\text{input}} - \text{Freq}_{\text{IF}})/n = \text{Freq}_{\text{control}}$$

$$(900\text{ MHZ} - 0\text{ MHZ})/n = 900\text{ MHZ}/n$$

For $n = 0.5, 1, 2, 3$, etc., the frequency of the control signal 2006 should be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc. The frequency of the down-converted PSK signal is substantially equal to one half the difference between the lower frequency F_1 and the upper frequency F_2.

As another example, to down-convert a FSK signal to an amplitude shift keying (ASK) signal (a subset of AM), either the lower frequency F_1 or the upper frequency F_2 of the FSK signal is down-converted to zero IF. For example, to down-convert an FSK signal having F_1 equal to 900 MHZ and F_2 equal to 901 MHZ, to an ASK signal, the aliasing rate of the control signal 2006 should be substantially equal to:

(900 MHZ - 0 MHZ)/n = 900 MHZ/*n*, or
(901 MHZ - 0 MHZ)/n = 901 MHZ/*n*.

For the former case of 900 MHZ/*n*, and for *n* = 0.5, 1, 2, 3, 4, etc., the frequency of the control signal 2006 should be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc. For the latter case of 901 MHZ/*n*, and for *n* = 0.5, 1, 2, 3, 4, etc., the frequency of the control signal 2006 should be substantially equal to 1.802 GHz, 901 MHZ, 450.5 MHZ, 300.333 MHZ, 225.25 MHZ, etc. The frequency of the down-converted AM signal is substantially equal to the difference between the lower frequency F_1 and the upper frequency F_2 (i.e., 1 MHZ).

Exemplary time domain and frequency domain drawings, illustrating down-conversion of FM signals to non-FM signals, and exemplary methods and systems thereof, are disclosed in the co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," Application No. 09/176,022, issued as U.S. Patent No. 6,061,551 on May 9, 2000.

In an embodiment, the pulses of the control signal 2006 have negligible apertures that tend towards zero. This makes the UFT module 2002 a high input impedance device. This configuration is useful for situations where minimal disturbance of the input signal may be desired.

In another embodiment, the pulses of the control signal 2006 have non-negligible apertures that tend away from zero. This makes the UFT module 2002 a lower input impedance device. This allows the lower input impedance of the UFT module 2002 to be substantially matched with a source impedance of the input signal 2004. This also improves the energy transfer from the input signal 2004 to the down-converted output signal 2012, and hence the efficiency and signal to noise (s/n) ratio of UFT module 2002.

Exemplary systems and methods for generating and optimizing the control signal 2006 and for otherwise improving energy transfer and s/n ratio, are disclosed in the co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," Application No. 09/176,022, issued as U.S. Patent No. 6,061,551 on May 9, 2000.

3. Frequency Up-Conversion

The present invention is directed to systems and methods of frequency up-conversion, and applications of same.

An example frequency up-conversion system 300 is illustrated in FIG. 3. The frequency up-conversion system 300 is now described.

An input signal 302 (designated as "Control Signal" in FIG. 3) is accepted by a switch module 304. For purposes of example only, assume that the input signal 302 is a FM input signal 606, an example of which is shown in FIG. 6C. FM input signal 606 may have been generated by modulating information signal 602 onto oscillating signal 604 (FIGS. 6A and 6B). It should be understood that the invention is not limited to this embodiment. The information signal 602 can be analog, digital, or any combination thereof, and any modulation scheme can be used.

The output of switch module 304 is a harmonically rich signal 306, shown for example in FIG. 6D as a harmonically rich signal 608. The harmonically rich signal 608 has a continuous and periodic waveform.

FIG. 6E is an expanded view of two sections of harmonically rich signal 608, section 610 and section 612. The harmonically rich signal 608 may be a rectangular wave, such as a square wave or a pulse (although, the invention is not limited to this embodiment). For ease of discussion, the term "rectangular waveform" is used to refer to waveforms that are substantially rectangular. In a similar manner, the term "square wave" refers to those waveforms that are substantially square and it is not the intent of the present invention that a perfect square wave be generated or needed.

Harmonically rich signal 608 is comprised of a plurality of sinusoidal waves whose frequencies are integer multiples of the fundamental frequency of the waveform of the harmonically rich signal 608. These sinusoidal waves are referred to as the harmonics of the underlying waveform, and the fundamental frequency is referred to as the first harmonic. FIG. 6F and FIG. 6G show separately the sinusoidal components making up the first, third, and fifth harmonics of section 610 and section 612. (Note that in theory there may be an infinite number of harmonics; in this example, because harmonically rich signal 608 is shown as a square wave, there are only odd harmonics). Three harmonics are shown simultaneously (but not summed) in FIG. 6H.

The relative amplitudes of the harmonics are generally a function of the relative widths of the pulses of harmonically rich signal 306 and the period of the fundamental frequency, and can be determined by doing a Fourier analysis of harmonically rich signal 306. According to an embodiment of the invention, the input signal 606 may be shaped to ensure that the amplitude of the desired harmonic is sufficient for its intended use (e.g., transmission).

A filter 308 filters out any undesired frequencies (harmonics), and outputs an electromagnetic (EM) signal at the desired harmonic frequency or frequencies as an output signal 310, shown for example as a filtered output signal 614 in FIG. 6I.

FIG. 4 illustrates an example universal frequency up-conversion (UFU) module 401. The UFU module 401 includes an example switch module 304, which comprises a bias signal 402, a resistor or impedance 404, a universal frequency translator (UFT) 450, and a ground 408. The UFT 450 includes a switch 406. The input signal 302 (designated as "Control Signal" in FIG. 4) controls the switch 406 in the UFT 450, and causes it to close and open. Harmonically rich signal 306 is generated at a node 405 located between the resistor or impedance 404 and the switch 406.

Also in FIG. 4, it can be seen that an example filter 308 is comprised of a capacitor 410 and an inductor 412 shunted to a ground 414. The filter is designed to filter out the undesired harmonics of harmonically rich signal 306.

The invention is not limited to the UFU embodiment shown in FIG. 4.

For example, in an alternate embodiment shown in FIG. 5, an unshaped input signal 501 is routed to a pulse shaping module 502. The pulse shaping module 502 modifies the unshaped input signal 501 to generate a (modified) input signal 302 (designated as the "Control Signal" in FIG. 5). The input signal 302 is routed to the switch module 304, which operates in the manner described above. Also, the filter 308 of FIG. 5 operates in the manner described above.

The purpose of the pulse shaping module 502 is to define the pulse width of the input signal 302. Recall that the input signal 302 controls the opening and closing of the switch 406 in switch module 304. During such operation, the pulse width of the input signal 302 establishes the pulse width of the harmonically rich signal 306. As stated above, the relative amplitudes of the harmonics of the harmonically rich signal 306 are a function of at least the pulse width of the harmonically rich signal 306. As such, the pulse width of the input signal 302 contributes to setting the relative amplitudes of the harmonics of harmonically rich signal 306.

Further details of up-conversion as described in this section are presented in pending U.S. application "Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, filed October 21, 1998, incorporated herein by reference in its entirety.

4. Enhanced Signal Reception

The present invention is directed to systems and methods of enhanced signal reception (ESR), and applications of same.

Referring to FIG. 21, transmitter 2104 accepts a modulating baseband signal 2102 and generates (transmitted) redundant spectrums 2106a-n, which are sent over communications medium 2108. Receiver 2112 recovers a demodulated baseband signal 2114 from (received) redundant spectrums 2110a-n. Demodulated baseband signal 2114 is representative of the modulating baseband signal 2102, where the level of similarity between the modulating baseband signal 2114 and the modulating baseband signal 2102 is application dependent.

Modulating baseband signal 2102 is preferably any information signal desired for transmission and/or reception. An example modulating baseband signal 2202 is illustrated in FIG. 22A, and has an associated modulating baseband spectrum 2204 and image spectrum 2203 that are illustrated in FIG. 22B. Modulating baseband signal 2202 is illustrated as an analog signal in FIG. 22a, but could also be a digital signal, or combination thereof. Modulating baseband signal 2202 could be a voltage (or current) characterization of any number of real world occurrences, including for example and without limitation, the voltage (or current) representation for a voice signal.

Each transmitted redundant spectrum 2106a-n contains the necessary information to substantially reconstruct the modulating baseband signal 2102. In other words, each redundant spectrum 2106a-n contains the necessary amplitude, phase, and frequency information to reconstruct the modulating baseband signal 2102.

FIG. 22C illustrates example transmitted redundant spectrums 2206b-d. Transmitted redundant spectrums 2206b-d are illustrated to contain three redundant spectrums for illustration purposes only. Any number of redundant spectrums could be generated and transmitted as will be explained in following discussions.

Transmitted redundant spectrums 2206b-d are centered at f_1, with a frequency spacing f_2 between adjacent spectrums. Frequencies f_1 and f_2 are dynamically adjustable in real-time as will be shown below. FIG. 22D illustrates an alternate embodiment, where redundant spectrums 2208c,d are centered on unmodulated oscillating signal 2209 at f_1 (Hz). Oscillating signal 2209 may be suppressed if desired using, for example, phasing techniques or filtering techniques. Transmitted redundant spectrums are preferably above baseband frequencies as is represented by break 2205 in the frequency axis of FIGS. 22C and 22D.

Received redundant spectrums 2110a-n are substantially similar to transmitted redundant spectrums 2106a-n, except for the changes introduced by the communications medium 2108. Such changes can include but are not limited to signal attenuation, and signal interference. FIG. 22E illustrates example received redundant spectrums 2210b-d. Received redundant spectrums 2210b-d are substantially similar to transmitted redundant spectrums 2206b-d, except that redundant spectrum 2210c includes an undesired jamming signal spectrum 2211 in order to illustrate some advantages of the present invention. Jamming signal spectrum 2211 is a frequency spectrum associated with a jamming signal. For purposes of this invention, a "jamming signal" refers to any unwanted signal, regardless of origin, that may interfere with the proper reception and reconstruction of an intended signal. Furthermore, the jamming signal is not limited to tones as depicted by spectrum 2211, and can have any spectral shape, as will be understood by those skilled in the art(s).

As stated above, demodulated baseband signal 2114 is extracted from one or more of received redundant spectrums 2210b-d. FIG. 22F illustrates example demodulated baseband signal 2212 that is, in this example, substantially similar to modulating baseband signal 2202 (FIG. 22A); where in practice, the degree of similarity is application dependent.

An advantage of the present invention should now be apparent. The recovery of modulating baseband signal 2202 can be accomplished by receiver 2112 in spite of the fact that high strength jamming signal(s) (e.g. jamming signal spectrum 2211) exist on the communications medium. The intended baseband signal can be recovered because multiple redundant spectrums are transmitted, where each redundant spectrum carries the necessary information to reconstruct the baseband signal. At the destination, the redundant spectrums are isolated from each other so that the baseband signal can be recovered even if one or more of the redundant spectrums are corrupted by a jamming signal.

Transmitter 2104 will now be explored in greater detail. FIG. 23A illustrates transmitter 2301, which is one embodiment of transmitter 2104 that generates redundant spectrums configured similar to redundant spectrums 2206b-d. Transmitter 2301 includes generator 2303, optional spectrum processing module 2304, and optional medium interface module 2320. Generator 2303 includes: first oscillator 2302, second oscillator 2309, first stage modulator 2306, and second stage modulator 2310.

Transmitter 2301 operates as follows. First oscillator 2302 and second oscillator 2309 generate a first oscillating signal 2305 and second oscillating signal 2312, respectively. First stage modulator 2306 modulates first oscillating signal 2305 with modulating baseband signal 2202, resulting in modulated signal 2308. First stage modulator 2306 may implement any type of modulation including but not limited to: amplitude modulation, frequency modulation, phase modulation, combinations thereof, or any other type of modulation. Second stage modulator 2310 modulates modulated signal 2308 with second oscillating signal 2312, resulting in multiple redundant spectrums 2206a-n shown in FIG. 23B. Second stage modulator 2310 is preferably a phase modulator, or a frequency modulator, although other types of modulation may be implemented including but not limited to amplitude modulation. Each redundant spectrum

2206a-n contains the necessary amplitude, phase, and frequency information to substantially reconstruct the modulating baseband signal 2202.

Redundant spectrums 2206a-n are substantially centered around f_1, which is the characteristic frequency of first oscillating signal 2305. Also, each redundant spectrum 2206a-n (except for 2206c) is offset from f_1 by approximately a multiple of f_2 (Hz), where f_2 is the frequency of the second oscillating signal 2312. Thus, each redundant spectrum 2206a-n is offset from an adjacent redundant spectrum by f_2 (Hz). This allows the spacing between adjacent redundant spectrums to be adjusted (or tuned) by changing f_2 that is associated with second oscillator 2309. Adjusting the spacing between adjacent redundant spectrums allows for dynamic real-time tuning of the bandwidth occupied by redundant spectrums 2206a-n.

In one embodiment, the number of redundant spectrums 2206a-n generated by transmitter 2301 is arbitrary and may be unlimited as indicated by the "a-n" designation for redundant spectrums 2206a-n. However, a typical communications medium will have a physical and/or administrative limitations (i.e. FCC regulations) that restrict the number of redundant spectrums that can be practically transmitted over the communications medium. Also, there may be other reasons to limit the number of redundant spectrums transmitted. Therefore, preferably, the transmitter 2301 will include an optional spectrum processing module 2304 to process the redundant spectrums 2206a-n prior to transmission over communications medium 2108.

In one embodiment, spectrum processing module 2304 includes a filter with a passband 2207 (FIG. 23C) to select redundant spectrums 2206b-d for transmission. This will substantially limit the frequency bandwidth occupied by the redundant spectrums to the passband 2207. In one embodiment, spectrum processing module 2304 also up converts redundant spectrums and/or amplifies redundant spectrums prior to transmission over the communications medium 2108. Finally, medium interface module 2320 transmits redundant spectrums over the communications medium 2108. In one embodiment, communications medium 2108 is an over-the-air link and medium interface module 2320 is an antenna. Other embodiments for communications medium 2108 and medium interface module 2320 will be understood based on the teachings contained herein.

FIG. 23D illustrates transmitter 2321, which is one embodiment of transmitter 2104 that generates redundant spectrums configured similar to redundant spectrums 2208c-d and unmodulated spectrum 2209. Transmitter 2321 includes generator 2311, spectrum processing module 2304, and (optional) medium interface module 2320. Generator 2311 includes: first oscillator 2302, second oscillator 2309, first stage modulator 2306, and second stage modulator 2310.

As shown in FIG. 23D, many of the components in transmitter 2321 are similar to those in transmitter 2301. However, in this embodiment, modulating baseband signal 2202 modulates second oscillating signal 2312. Transmitter 2321 operates as follows. First stage modulator 2306 modulates second oscillating signal 2312 with modulating baseband signal 2202, resulting in modulated signal 2322. As described earlier, first stage modulator 2306 can effect any type of modulation including but not limited to: amplitude modulation frequency modulation, combinations thereof, or any other type of modulation. Second stage modulator 2310 modulates first oscillating signal 2304 with modulated signal 2322, resulting in redundant spectrums 2208a-n, as shown in FIG. 23E. Second stage modulator 2310 is preferably a phase or frequency modulator, although other modulators could used including but not limited to an amplitude modulator.

Redundant spectrums 2208a-n are centered on unmodulated spectrum 2209 (at f_1 Hz), and adjacent spectrums are separated by f_2 Hz. The number of redundant spectrums 2208a-n generated by generator 2311 is arbitrary and unlimited, similar to spectrums 2206a-n discussed above. Therefore, optional spectrum processing module 2304 may also include a filter with passband 2325 to select, for example, spectrums 2208c,d for transmission over communications medium 2108. In addition, optional spectrum processing module 2304 may also include a filter (such as a bandstop filter) to attenuate unmodulated spectrum 2209. Alternatively, unmodulated spectrum 2209 may be attenuated by using phasing techniques during redundant spectrum generation. Finally, (optional) medium interface module 2320 transmits redundant spectrums 2208c,d over communications medium 2108.

Receiver 2112 will now be explored in greater detail to illustrate recovery of a demodulated baseband signal from received redundant spectrums. FIG. 24A illustrates receiver 2430, which is one embodiment of receiver 2112. Receiver 2430 includes optional medium interface module 2402, down-converter 2404, spectrum isolation module 2408, and data extraction module 2414. Spectrum isolation module 2408 includes filters 2410a-c. Data extraction module 2414 includes demodulators 2416a-c, error check modules 2420a-c, and arbitration module 2424. Receiver 2430 will be discussed in relation to the signal diagrams in FIGS. 24B-24J.

In one embodiment, optional medium interface module 2402 receives redundant spectrums 2210b-d (FIG. 22E, and FIG. 24B). Each redundant spectrum 2210b-d includes the necessary amplitude, phase, and frequency information to substantially reconstruct the modulating baseband signal used to generated the redundant spectrums. However, in the present example, spectrum 2210c also contains jamming signal 2211, which may interfere with the recovery of a baseband signal from spectrum 2210c. Down-converter 2404 down-converts received redundant spectrums 2210b-d to lower intermediate frequencies, resulting in redundant spectrums 2406a-c (FIG. 24C). Jamming signal 2211 is also down-converted to jamming signal 2407, as it is contained within redundant spectrum 2406b. Spectrum isolation module 2408 includes filters 2410a-c that isolate redundant spectrums 2406a-c from each other (FIGS. 24D-24F, respectively). Demodulators 2416a-c independently demodulate spectrums 2406a-c, resulting in demodulated baseband signals 2418a-c, respectively (FIGS. 24G-24I). Error check modules 2420a-c analyze demodulate baseband signal 2418a-c to detect any errors. In one embodiment, each error check module 2420a-c sets an error flag 2422a-c whenever an error is detected in a demodulated baseband signal. Arbitration module 2424 accepts the demodulated baseband signals and associated error flags, and selects a substantially error-free demodulated baseband signal (FIG. 24J). In one embodiment, the substantially error-free demodulated baseband signal will be substantially similar to the modulating baseband signal used to generate the received redundant spectrums, where the degree of similarity is application dependent.

Referring to FIGS. 24G-I, arbitration module 2424 will select either demodulated baseband signal 2418a or 2418c, because error check module 2420b will set the error flag 2422b that is associated with demodulated baseband signal 2418b.

The error detection schemes implemented by the error detection modules include but are not limited to: cyclic redundancy check (CRC) and parity check for digital signals, and various error detections schemes for analog signal.

Further details of enhanced signal reception as described in this section are presented in pending U.S. application "Method and System for Ensuring Reception of a Communications Signal," Ser. No. 09/176,415, filed October 21, 1998, issued as U.S. Patent No. 6,061,555 on May 9, 2000.

5. Unified Down-Conversion and Filtering

The present invention is directed to systems and methods of unified down-conversion and filtering (UDF), and applications of same.

In particular, the present invention includes a unified down-converting and filtering (UDF) module that performs frequency selectivity and frequency translation in a unified (i.e., integrated) manner. By operating in this manner, the invention achieves high frequency selectivity prior to frequency translation (the invention is not limited to this embodiment). The invention achieves high frequency selectivity at substantially any frequency, including but not limited to RF (radio frequency) and greater frequencies. It should be understood that the invention is not limited to this example of RF and greater frequencies. The invention is intended, adapted, and capable of working with lower than radio frequencies.

FIG. 17 is a conceptual block diagram of a UDF module 1702 according to an embodiment of the present invention. The UDF module 1702 performs at least frequency translation and frequency selectivity.

The effect achieved by the UDF module 1702 is to perform the frequency selectivity operation prior to the performance of the frequency translation operation. Thus, the UDF module 1702 effectively performs input filtering.

According to embodiments of the present invention, such input filtering involves a relatively narrow bandwidth. For example, such input filtering may represent channel select filtering, where the filter bandwidth may be, for example, 50 KHz to 150 KHz. It should be understood, however, that the invention is not limited to these frequencies. The invention is intended, adapted, and capable of achieving filter bandwidths of less than and greater than these values.

In embodiments of the invention, input signals 1704 received by the UDF module 1702 are at radio frequencies. The UDF module 1702 effectively operates to input filter these RF input signals 1704. Specifically, in these embodiments, the UDF module 1702 effectively performs input, channel select filtering of the RF input signal 1704. Accordingly, the invention achieves high selectivity at high frequencies.

The UDF module 1702 effectively performs various types of filtering, including but not limited to bandpass filtering, low pass filtering, high pass filtering, notch filtering, all pass filtering, band stop filtering, etc., and combinations thereof.

Conceptually, the UDF module 1702 includes a frequency translator 1708. The frequency translator 1708 conceptually represents that portion of the UDF module 1702 that performs frequency translation (down conversion).

The UDF module 1702 also conceptually includes an apparent input filter 1706 (also sometimes called an input filtering emulator). Conceptually, the apparent input filter 1706 represents that portion of the UDF module 1702 that performs input filtering.

In practice, the input filtering operation performed by the UDF module 1702 is integrated with the frequency translation operation. The input filtering operation can be viewed as being performed concurrently with the frequency translation operation. This is a reason why the input filter 1706 is herein referred to as an "apparent" input filter 1706.

The UDF module 1702 of the present invention includes a number of advantages. For example, high selectivity at high frequencies is realizable using the UDF module 1702. This feature of the invention is evident by the high Q factors that are attainable. For example, and without limitation, the UDF module 1702 can be designed with a filter center frequency f_C on the order of 900 MHZ, and a filter bandwidth on the order of 50 KHz. This represents a Q of 18,000 (Q is equal to the center frequency divided by the bandwidth).

It should be understood that the invention is not limited to filters with high Q factors. The filters contemplated by the present invention may have lesser or greater Qs, depending on the application, design, and/or implementation. Also, the scope of the invention includes filters where Q factor as discussed herein is not applicable.

The invention exhibits additional advantages. For example, the filtering center frequency f_C of the UDF module 1702 can be electrically adjusted, either statically or dynamically.

Also, the UDF module 1702 can be designed to amplify input signals.

Further, the UDF module 1702 can be implemented without large resistors, capacitors, or inductors. Also, the UDF module 1702 does not require that tight tolerances be maintained on the values of its individual components, i.e., its resistors, capacitors, inductors, etc. As a result, the architecture of the UDF module 1702 is friendly to integrated circuit design techniques and processes.

The features and advantages exhibited by the UDF module 1702 are achieved at least in part by adopting a new technological paradigm with respect to frequency selectivity and translation. Specifically, according to the present invention, the UDF module 1702 performs the frequency selectivity operation and the frequency translation operation as a single, unified (integrated) operation. According to the invention, operations relating to frequency translation also contribute to the performance of frequency selectivity, and vice versa.

According to embodiments of the present invention, the UDF module generates an output signal from an input signal using samples/instances of the input signal and samples/instances of the output signal.

More particularly, first, the input signal is under-sampled. This input sample includes information (such as amplitude, phase, etc.) representative of the input signal existing at the time the sample was taken.

As described further below, the effect of repetitively performing this step is to translate the frequency (that is, down-convert) of the input signal to a desired lower frequency, such as an intermediate frequency (IF) or baseband.

Next, the input sample is held (that is, delayed).

Then, one or more delayed input samples (some of which may have been scaled) are combined with one or more delayed instances of the output signal (some of which may have been scaled) to generate a current instance of the output signal.

Thus, according to a preferred embodiment of the invention, the output signal is generated from prior samples/instances of the input signal and/or the output signal. (It is noted that, in some embodiments of the invention, current samples/instances of the input signal and/or the output signal may be used to generate current instances of the output signal.). By operating in this manner, the UDF module preferably performs input filtering and frequency down-conversion in a unified manner.

FIG. 19 illustrates an example implementation of the unified down-converting and filtering (UDF) module 1922. The UDF module 1922 performs the frequency translation operation and the frequency selectivity operation in an integrated, unified manner as described above, and as further described below.

In the example of FIG. 19, the frequency selectivity operation performed by the UDF module 1922 comprises a band-pass filtering operation according to EQ. 1, below, which is an example representation of a band-pass filtering transfer function.

$$VO = \alpha_1 z^{-1} VI - \beta_1 z^{-1} VO - \beta_0 z^{-2} VO \qquad \text{EQ. 1}$$

It should be noted, however, that the invention is not limited to band-pass filtering. Instead, the invention effectively performs various types of filtering, including but not limited to bandpass filtering, low pass filtering, high pass filtering, notch filtering, all pass filtering, band stop filtering, etc., and combinations thereof. As will be appreciated, there are many representations of any given filter type. The invention is applicable to these filter representations. Thus, EQ. 1 is referred to herein for illustrative purposes only, and is not limiting.

The UDF module 1922 includes a down-convert and delay module 1924, first and second delay modules 1928 and 1930, first and second scaling modules 1932 and 1934, an output sample and hold module 1936, and an (optional) output smoothing module

1938. Other embodiments of the UDF module will have these components in different configurations, and/or a subset of these components, and/or additional components. For example, and without limitation, in the configuration shown in FIG. 19, the output smoothing module 1938 is optional.

As further described below, in the example of FIG. 19, the down-convert and delay module 1924 and the first and second delay modules 1928 and 1930 include switches that are controlled by a clock having two phases, ϕ_1 and ϕ_2. ϕ_1 and ϕ_2 preferably have the same frequency, and are non-overlapping (alternatively, a plurality such as two clock signals having these characteristics could be used). As used herein, the term "non-overlapping" is defined as two or more signals where only one of the signals is active at any given time. In some embodiments, signals are "active" when they are high. In other embodiments, signals are active when they are low.

Preferably, each of these switches closes on a rising edge of ϕ_1 or ϕ_2, and opens on the next corresponding falling edge of ϕ_1 or ϕ_2. However, the invention is not limited to this example. As will be apparent to persons skilled in the relevant art(s), other clock conventions can be used to control the switches.

In the example of FIG. 19, it is assumed that α_1 is equal to one. Thus, the output of the down-convert and delay module 1924 is not scaled. As evident from the embodiments described above, however, the invention is not limited to this example.

The example UDF module 1922 has a filter center frequency of 900.2 MHZ and a filter bandwidth of 570 KHz. The pass band of the UDF module 1922 is on the order of 899.915 MHZ to 900.485 MHZ. The Q factor of the UDF module 1922 is approximately 1879 (i.e., 900.2 MHZ divided by 570 KHz).

The operation of the UDF module 1922 shall now be described with reference to a Table 1802 (FIG. 18) that indicates example values at nodes in the UDF module 1922 at a number of consecutive time increments. It is assumed in Table 1802 that the UDF module 1922 begins operating at time t-1. As indicated below, the UDF module 1922 reaches steady state a few time units after operation begins. The number of time units necessary for a given UDF module to reach steady state depends on the configuration of the UDF module, and will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

At the rising edge of ϕ_1 at time t-1, a switch 1950 in the down-convert and delay module 1924 closes. This allows a capacitor 1952 to charge to the current value of an input signal, VI_{t-1}, such that node 1902 is at VI_{t-1}. This is indicated by cell 1804 in FIG. 18. In effect, the combination of the switch 1950 and the capacitor 1952 in the down-convert and delay module 1924 operates to translate the frequency of the input signal VI to a desired lower frequency, such as IF or baseband. Thus, the value stored in the capacitor 1952 represents an instance of a down-converted image of the input signal VI.

The manner in which the down-convert and delay module 1924 performs frequency down-conversion is further described elsewhere in this application, and is additionally described in pending U.S. application "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed October 21, 1998, issued as U.S. Patent No. 6,061,551 on May 9, 2000, which is herein incorporated by reference in its entirety.

Also at the rising edge of ϕ_1 at time t-1, a switch 1958 in the first delay module 1928 closes, allowing a capacitor 1960 to charge to VO_{t-1}, such that node 1906 is at VO_{t-1}. This is indicated by cell 1806 in Table 1802. (In practice, VO_{t-1} is undefined at this point. However, for ease of understanding, VO_{t-1} shall continue to be used for purposes of explanation.)

Also at the rising edge of ϕ_1 at time t-1, a switch 1966 in the second delay module 1930 closes, allowing a capacitor 1968 to charge to a value stored in a capacitor 1964. At this time, however, the value in capacitor 1964 is undefined, so the value in capacitor 1968 is undefined. This is indicated by cell 1807 in table 1802.

At the rising edge of ϕ_2 at time t- 1, a switch 1954 in the down-convert and delay module 1924 closes, allowing a capacitor 1956 to charge to the level of the capacitor 1952. Accordingly, the capacitor 1956 charges to VI_{t-1}, such that node 1904 is at VI_{t-1}. This is indicated by cell 1810 in Table 1802.

The UDF module 1922 may optionally include a unity gain module 1990A between capacitors 1952 and 1956. The unity gain module 1990A operates as a current source to enable capacitor 1956 to charge without draining the charge from capacitor 1952. For a similar reason, the UDF module 1922 may include other unity gain modules 1990B-1990G. It should be understood that, for many embodiments and applications of the invention, these unity gain modules 1990A-1990G are optional. The structure and operation of the unity gain modules 1990 will be apparent to persons skilled in the relevant art(s).

Also at the rising edge of ϕ_2 at time t−1, a switch 1962 in the first delay module 1928 closes, allowing a capacitor 1964 to charge to the level of the capacitor 1960. Accordingly, the capacitor 1964 charges to VO_{t-1}, such that node 1908 is at VO_{t-1}. This is indicated by cell 1814 in Table 1802.

Also at the rising edge of ϕ_2 at time t-1, a switch 1970 in the second delay module 1930 closes, allowing a capacitor 1972 to charge to a value stored in a capacitor 1968. At this time, however, the value in capacitor 1968 is undefined, so the value in capacitor 1972 is undefined. This is indicated by cell 1815 in table 1802.

At time t, at the rising edge of ϕ_1, the switch 1950 in the down-convert and delay module 1924 closes. This allows the capacitor 1952 to charge to VI_t, such that node 1902 is at VI_t. This is indicated in cell 1816 of Table 1802.

Also at the rising edge of ϕ_1 at time t, the switch 1958 in the first delay module 1928 closes, thereby allowing the capacitor 1960 to charge to VO_t. Accordingly, node 1906 is at VO_t. This is indicated in cell 1820 in Table 1802.

Further at the rising edge of ϕ_1 at time t, the switch 1966 in the second delay module 1930 closes, allowing a capacitor 1968 to charge to the level of the capacitor 1964. Therefore, the capacitor 1968 charges to VO_{t-1}, such that node 1910 is at VO_{t-1}. This is indicated by cell 1824 in Table 1802.

At the rising edge of ϕ_2 at time t, the switch 1954 in the down-convert and delay module 1924 closes, allowing the capacitor 1956 to charge to the level of the capacitor 1952. Accordingly, the capacitor 1956 charges to VI_t, such that node 1904 is at VI_t. This is indicated by cell 1828 in Table 1802.

Also at the rising edge of ϕ_2 at time t, the switch 1962 in the first delay module 1928 closes, allowing the capacitor 1964 to charge to the level in the capacitor 1960. Therefore, the capacitor 1964 charges to VO_t, such that node 1908 is at VO_t. This is indicated by cell 1832 in Table 1802.

Further at the rising edge of ϕ_2 at time t, the switch 1970 in the second delay module 1930 closes, allowing the capacitor 1972 in the second delay module 1930 to charge to the level of the capacitor 1968 in the second delay module 1930. Therefore, the capacitor 1972 charges to VO_{t-1}, such that node 1912 is at VO_{t-1}. This is indicated in cell 1836 of FIG. 18.

At time t+1, at the rising edge of ϕ_1, the switch 1950 in the down-convert and delay module 1924 closes, allowing the capacitor 1952 to charge to VI_{t+1}. Therefore, node 1902 is at VI_{t+1}, as indicated by cell 1838 of Table 1802.

Also at the rising edge of ϕ_1 at time t+1, the switch 1958 in the first delay module 1928 closes, allowing the capacitor 1960 to charge to VO_{t+1}. Accordingly, node 1906 is at VO_{t+1}, as indicated by cell 1842 in Table 1802.

Further at the rising edge of ϕ_1 at time t+1, the switch 1966 in the second delay module 1930 closes, allowing the capacitor 1968 to charge to the level of the capacitor 1964. Accordingly, the capacitor 1968 charges to VO_t, as indicated by cell 1846 of Table 1802.

In the example of FIG. 19, the first scaling module 1932 scales the value at node 1908 (i.e., the output of the first delay module 1928) by a scaling factor of -0.1. Accordingly, the value present at node 1914 at time t+1 is $-0.1 * VO_t$. Similarly, the second scaling module 1934 scales the value present at node 1912 (i.e., the output of the second scaling module 1930) by a scaling factor of -0.8. Accordingly, the value present at node 1916 is $-0.8 * VO_{t-1}$ at time t+1.

At time t+1, the values at the inputs of the summer 1926 are: VI_t at node 1904, $-0.1 * VO_t$ at node 1914, and $-0.8 * VO_{t-1}$ at node 1916 (in the example of FIG. 19, the values at nodes 1914 and 1916 are summed by a second summer 1925, and this sum is presented to the summer 1926). Accordingly, at time t+1, the summer generates a signal equal to $VI_t - 0.1 * VO_t - 0.8 * VO_{t-1}$.

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At the rising edge of ϕ_1 at time t+1, a switch 1991 in the output sample and hold module 1936 closes, thereby allowing a capacitor 1992 to charge to VO_{t+1}. Accordingly, the capacitor 1992 charges to VO_{t+1}, which is equal to the sum generated by the adder 1926. As just noted, this value is equal to: $VI_t - 0.1 * VO_t - 0.8 * VO_{t-1}$. This is indicated in cell 1850 of Table 1802. This value is presented to the optional output smoothing module 1938, which smooths the signal to thereby generate the instance of the output signal VO_{t+1}. It is apparent from inspection that this value of VO_{t+1} is consistent with the band pass filter transfer function of EQ. 1.

Further details of unified down-conversion and filtering as described in this section are presented in pending U.S. application "Integrated Frequency Translation And Selectivity," Ser. No. 09/175,966, filed October 21, 1998, issued as U.S. Patent No. 6,049,706 on April 11, 2000, incorporated herein by reference in its entirety.

6. *Example Application Embodiments of the Invention*

As noted above, the UFT module of the present invention is a very powerful and flexible device. Its flexibility is illustrated, in part, by the wide range of applications in which it can be used. Its power is illustrated, in part, by the usefulness and performance of such applications.

Example applications of the UFT module were described above. In particular, frequency down-conversion, frequency up-conversion, enhanced signal reception, and unified down-conversion and filtering applications of the UFT module were summarized above, and are further described below. These applications of the UFT module are discussed herein for illustrative purposes. The invention is not limited to these example applications. Additional applications of the UFT module will be apparent to persons skilled in the relevant art(s), based on the teachings contained herein.

For example, the present invention can be used in applications that involve frequency down-conversion. This is shown in FIG. 1C, for example, where an example UFT module 115 is used in a down-conversion module 114. In this capacity, the UFT module 115 frequency down-converts an input signal to an output signal. This is also shown in FIG. 7, for example, where an example UFT module 706 is part of a down-conversion module 704, which is part of a receiver 702.

The present invention can be used in applications that involve frequency up-conversion. This is shown in FIG. 1D, for example, where an example UFT module 117 is used in a frequency up-conversion module 116. In this capacity, the UFT module 117 frequency up-converts an input signal to an output signal. This is also shown in FIG. 8, for example, where an example UFT module 806 is part of up-conversion module 804, which is part of a transmitter 802.

The present invention can be used in environments having one or more transmitters 902 and one or more receivers 906, as illustrated in FIG. 9. In such environments, one or more of the transmitters 902 may be implemented using a UFT module, as shown for example in FIG. 8. Also, one or more of the receivers 906 may be implemented using a UFT module, as shown for example in FIG. 7.

The invention can be used to implement a transceiver. An example transceiver 1002 is illustrated in FIG. 10. The transceiver 1002 includes a transmitter 1004 and a receiver 1008. Either the transmitter 1004 or the receiver 1008 can be implemented using a UFT module. Alternatively, the transmitter 1004 can be implemented using a UFT module 1006, and the receiver 1008 can be implemented using a UFT module 1010. This embodiment is shown in FIG. 10.

Another transceiver embodiment according to the invention is shown in FIG. 11. In this transceiver 1102, the transmitter 1104 and the receiver 1108 are implemented using a single UFT module 1106. In other words, the transmitter 1104 and the receiver 1108 share a UFT module 1106.

As described elsewhere in this application, the invention is directed to methods and systems for enhanced signal reception (ESR). Various ESR embodiments include an ESR module (transmit) in a transmitter 1202, and an ESR module (receive) in a receiver 1210. An example ESR embodiment configured in this manner is illustrated in FIG. 12.

The ESR module (transmit) 1204 includes a frequency up-conversion module 1206. Some embodiments of this frequency up-conversion module 1206 may be implemented using a UFT module, such as that shown in FIG. 1D.

The ESR module (receive) 1212 includes a frequency down-conversion module 1214. Some embodiments of this frequency down-conversion module 1214 may be implemented using a UFT module, such as that shown in FIG. 1C.

As described elsewhere in this application, the invention is directed to methods and systems for unified down-conversion and filtering (UDF). An example unified down-conversion and filtering module 1302 is illustrated in FIG. 13. The unified down-conversion and filtering module 1302 includes a frequency down-conversion module 1304 and a filtering module 1306. According to the invention, the frequency down-conversion module 1304 and the filtering module 1306 are implemented using a UFT module 1308, as indicated in FIG. 13.

Unified down-conversion and filtering according to the invention is useful in applications involving filtering and/or frequency down-conversion. This is depicted, for example, in FIGS. 15A-15F. FIGS. 15A-15C indicate that unified down-conversion and filtering according to the invention is useful in applications where filtering precedes, follows, or both precedes and follows frequency down-conversion. FIG. 15D indicates that a unified down-conversion and filtering module 1524 according to the invention can be utilized as a filter 1522 (i.e., where the extent of frequency down-conversion by the down-converter in the unified down-conversion and filtering module 1524 is minimized). FIG. 15E indicates that a unified down-conversion and filtering module 1528 according to the invention can be utilized as a down-converter 1526 (i.e., where the filter in the unified down-conversion and filtering module 1528 passes substantially all frequencies). FIG. 15F illustrates that the unified down-conversion and filtering module 1532 can be used as an amplifier. It is noted that one or more UDF modules can be used in applications that involve at least one or more of filtering, frequency translation, and amplification.

For example, receivers, which typically perform filtering, down-conversion, and filtering operations, can be implemented using one or more unified down-conversion and filtering modules. This is illustrated, for example, in FIG. 14.

The methods and systems of unified down-conversion and filtering of the invention have many other applications. For example, as discussed herein, the enhanced signal reception (ESR) module (receive) operates to down-convert a signal containing a plurality of spectrums. The ESR module (receive) also operates to isolate the spectrums in the down-converted signal, where such isolation is implemented via filtering in some embodiments. According to embodiments of the invention, the ESR module (receive) is implemented using one or more unified down-conversion and filtering (UDF) modules. This is illustrated, for example, in FIG. 16. In the example of FIG. 16, one or more of the UDF modules 1610, 1612, 1614 operates to down-convert a received signal. The UDF modules 1610, 1612, 1614 also operate to filter the down-converted signal so as to isolate the spectrum(s) contained therein. As noted above, the UDF modules 1610, 1612, 1614 are implemented using the universal frequency translation (UFT) modules of the invention.

The invention is not limited to the applications of the UFT module described above. For example, and without limitation, subsets of the applications (methods and/or structures) described herein (and others that would be apparent to persons skilled in the relevant art(s) based on the herein teachings) can be associated to form useful combinations.

For example, transmitters and receivers are two applications of the UFT module. FIG. 10 illustrates a transceiver 1002 that is formed by combining these two applications of the UFT module, i.e., by combining a transmitter 1004 with a receiver 1008.

Also, ESR (enhanced signal reception) and unified down-conversion and filtering are two other applications of the UFT module. FIG. 16 illustrates an example where ESR and unified down-conversion and filtering are combined to form a modified enhanced signal reception system.

The invention is not limited to the example applications of the UFT module discussed herein. Also, the invention is not limited to the example combinations of applications of the UFT module discussed herein. These examples were provided for illustrative purposes only, and are not limiting. Other applications and combinations of such applications will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such applications and combinations include, for example and without limitation, applications/combinations comprising and/or involving one or more of: (1) frequency translation; (2) frequency down-conversion; (3) frequency up-conversion;

(4) receiving; (5) transmitting; (6) filtering; and/or (7) signal transmission and reception in environments containing potentially jamming signals.

Additional example applications are described below.

6.1 Data Communication

The invention is directed to data communication among data processing devices. For example, and without limitation, the invention is directed to computer networks such as, for example, local area networks (LANs), wide area networks (WANs), including wireless LANs (WLANs) and wireless WANs, modulator/demodulators (modems), including wireless modems, etc.

FIG. 25 illustrates an example environment 2502 wherein computers 2504, 2512, and 2526 communicate with one another via a computer network 2534. It is noted that the invention is not limited to computers, but encompasses any data processing and/or communications device or other device where communications with external devices is desired. Also, the invention includes but si not limited to WLAN client (also called mobile terminals, and/or stations) and infrastructure devices (also called access points). In the example of FIG. 25, computer 2504 is communicating with the network 2534 via a wired link, whereas computers 2512 and 2526 are communicating with the network 2534 via wireless links.

In the teachings contained herein, for illustrative purposes, a link may be designated as being a wired link or a wireless link. Such designations are for example purposes only, and are not limiting. A link designated as being wireless may alternatively be wired. Similarly, a link designated as being wired may alternatively be wireless. This is applicable throughout the entire application.

The computers 2504, 2512 and 2526 each include an interface 2506, 2514, and 2528, respectively, for communicating with the network 2534. The interfaces 2506, 2514, and 2528 include transmitters 2508, 2516, and 2530 respectively. Also, the interfaces 2506, 2514 and 2528 include receivers 2510, 2518, and 2532 respectively. In embodiments of the invention, the transmitters 2508, 2516 and 2530 are implemented using UFT modules for performing frequency up-conversion operations (see, for example, FIG. 8). In embodiments, the receivers 2510, 2518 and 2532 are implemented using UFT modules for performing frequency down-conversion operations (see, for example, FIG. 7).

As noted above, the computers 2512 and 2526 interact with the network 2534 via wireless links. In embodiments of the invention, the interfaces 2514, 2528 in computers 2512, 2526 represent modulator/demodulators (modems).

In embodiments, the network 2534 includes an interface or modem 2520 for communicating with the modems 2514, 2528 in the computers 2512, 2526. In embodiments, the interface 2520 includes a transmitter 2522, and a receiver 2524. Either or both of the transmitter 2522, and the receiver 2524 are implemented using UFT modules for performing frequency translation operations (see, for example, FIGS. 7 and 8).

In alternative embodiments, one or more of the interfaces 2506, 2514, 2520, and 2528 are implemented using transceivers that employ one or more UFT modules for performing frequency translation operations (see, for example, FIGS. 10 and 11).

FIG. 26 illustrates another example data communication embodiment 2602. Each of a plurality of computers 2604, 2612, 2614 and 2616 includes an interface, such as an interface 2606 shown in the computer 2604. It should be understood that the other computers 2612, 2614, 2616 also include an interface such as an interface 2606. The computers 2604, 2612, 2614 and 2616 communicate with each other via interfaces 2606 and wireless or wired links, thereby collectively representing a data communication network.

The interfaces 2606 may represent any computer interface or port, such as but not limited to a high speed internal interface, a wireless serial port, a wireless PS2 port, a wireless USB port, PCMCIA port, etc.

The interface 2606 includes a transmitter 2608 and a receiver 2610. In embodiments of the invention, either or both of the transmitter 2608 and the receiver 2610 are implemented using UFT modules for frequency up-conversion and down-conversion (see, for example, FIGS. 7 and 8). Alternatively, the interfaces 2806 can be implemented using a transceiver having one or more UFT modules for performing frequency translation operations (see, for example, FIGS. 10 and 11).

FIGS. 33-38 illustrate other scenarios envisioned and encompassed by the invention. FIG. 33 illustrates a data processing environment 3302 wherein a wired network, such as an Ethernet network 3304, is linked to another network, such as a WLAN 3306, via a wireless link 3308. The wireless link 3308 is established via interfaces 3310, 3312 which are preferably implemented using universal frequency translation modules.

FIGS 35-38 illustrate that the present invention supports WLANs that are located in one or more buildings or over any defined geographical area, as shown in FIGs. 35-38.

The invention includes multiple networks linked together. The invention also envisions wireless networks conforming to any known or custom standard or specification. This is shown in FIG. 34, for example, where any combination of WLANs conforming to any WLAN standard or configuration, such as IEEE 802.11 and Bluetooth (or other relatively short range communication specification or standard), any WAN cellular or telephone standard or specification, any type of radio links, any custom standard or specification, etc., or combination thereof, can be implemented using the universal frequency translation technology described herein. Also, any combination of these networks may be coupled together, as illustrated in FIG. 34.

The invention supports WLANs that are located in one or multiple buildings, as shown in FIGS. 35 and 36. The invention also supports WLANs that are located in an area including and external to one or more buildings, as shown in FIG. 37. In fact, the invention is directed to networks that cover any defined geographical area, as shown in FIG. 38. In the embodiments described above, wireless links are preferably established using WLAN interfaces as described herein.

More generally, the invention is directed to WLAN client devices and WLAN infrastructure devices. "WLAN Client Devices" refers to, for example, any data processing and/or communication devices in which wired or wireless communication functionality is desired, such as but not limited to computers, personal data assistants (PDAs), automatic identification data collection devices (such as bar code scanners/readers, electronic article surveillance readers, and radio frequency identification readers), telephones, network devices, etc., and combinations thereof. "WLAN Infrastructure Devices" refers to, for example, Access Points and other devices used to provide the ability for WLAN Client Devices (as well as potentially other devices) to connect to wired and/or wireless networks and/or to provide the network functionality of a WLAN. "WLAN" refers to, for example, a Wireless Local Area Network that is implemented according to and that operates within WLAN standards and/or specifications, such as but not limited to IEEE 802.11, IEEE 802.11a, IEEE 802.11b, HomeRF, Proxim Range LAN, Proxim Range LAN2, Symbol Spectrum 1, Symbol Spectrum 24 as it existed prior to adoption of IEEE 802.11, HiperLAN1, or HiperLAN2. WLAN client devices and/or WLAN infrastructure devices may operate in a multi-mode capacity. For example, a device may include WLAN and WAN functionality. Another device may include WLAN and short range communication (such as but not limited to Blue Tooth) functionality. Another device may include WLAN and WAN and short range communication functionality. It is noted that the above definitions and examples are provided for illustrative purposes, and are not limiting. Equivalents to that described above will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

6.1.1. Example Implementations: Interfaces, Wireless Modems, Wireless LANs, etc.

The present invention is now described as implemented in an interface, such as a wireless modem or other device (such as client or infrastructure device) , which can be utilized to implement or interact with a wireless local area network (WLAN) or wireless wide area network (WWAN), for example. In an embodiment, the present invention is implemented in a WLAN to support IEEE WLAN Standard 802.11, but this embodiment is mentioned for illustrative purposes only. The invention is not limited to this standard.

Conventional wireless modems are described in, for example, U.S. Patent 5,764,693, titled, "Wireless Radio Modem with Minimal Inter-Device RF Interference," incorporated herein by reference in its entirety. The present invention replaces a substantial portion of conventional wireless modems with one or more universal frequency translators (UFTs). The resultant improved wireless modem consumes less power that conventional wireless modems and is easier and less expensive to design and build. A wireless modem in accordance with the present invention can be implemented in a PC-MCIA card or within a main housing of a computer, for example.

FIG. 27 illustrates an example block diagram of a computer system 2710, which can be wirelessly coupled to a LAN, as illustrated in FIGS. 25 and 26. The computer system 2710 includes an interface 2714 and an antenna 2712. The interface 2714 includes a transmitter module 2716 that receives information from a digital signal processor (DSP) 2720, and modulates and up-converts the information for transmission from the antenna 2712. The interface 2714 also includes a receiver module 2718 that receives modulated carrier signals via the antenna 2712. The receiver module 2718 down-converts and demodulates the modulated carrier signals to baseband information, and provides the baseband information to the DSP 2720. The DSP 2720 can include a central processing unit (CPU) and other components of the computer 2712. Conventionally, the interface 2714 is implemented with heterodyne components.

FIG. 28 illustrates an example interface 2810 implemented with heterodyne components. The interface 2810 includes a transmitter module 2812 and a receiver module 2824. The receiver module 2824 includes an RF section 2830, one or more IF sections 2828, a demodulator section 2826, an optional analog to digital (A/D) converter 2834, and a frequency generator/synthesizer 2832. The transmitter module 2812 includes an optional digital to analog (D/A) converter 2822, a modulator \section 2818, one or more IF sections 2816, an RF section 2814, and a frequency generator/synthesizer 2820. Operation of the interface 2810 will be apparent to one skilled in the relevant art(s), based on the description herein.

FIG. 29 illustrates an example in-phase/quadrature-phase (I/Q) interface 2910 implemented with heterodyne components. I/Q implementations allow two channels of information to be communicated on a carrier signal and thus can be utilized to increase data transmission.

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The interface 2910 includes a transmitter module 2912 and a receiver module 2934. The receiver module 2934 includes an RF section 2936, one or more IF sections 2938, an I/Q demodulator section 2940, an optional A/D converter 2944, and a frequency generator/synthesizer 2942. The I/Q demodulator section 2940 includes a signal splitter 2946, mixers 2948, and a phase shifter 2950. The signal splitter 2946 provides a received signal to the mixers 2948. The phase shifter 2950 operates the mixers 2948 ninety degrees out of phase with one another to generate I and Q information channels 2952 and 2954, respectively, which are provided to a DSP 2956 through the optional A/D converter 2944.

The transmitter module 2912 includes an optional D/A converter 2922, an I/Q modulator section 2918, one or more IF sections 2916, an RF section 2914, and a frequency generator/synthesizer 2920. The I/Q modulator section 2918 includes mixers 2924, a phase shifter 2926, and a signal combiner 2928. The phase shifter 2926 operates the mixers 2924 ninety degrees out of phase with one another to generate I and Q modulated information signals 2930 and 2932, respectively, which are combined by the signal combiner 2928. The IF section(s) 2916 and RF section 2914 up-convert the combined I and Q modulated information signals 2930 and 2932 to RF for transmission by the antenna, in a manner well known in the relevant art(s).

Heterodyne implementations, such as those illustrated in FIGS. 28 and 29, are expensive and difficult to design, manufacture and tune. In accordance with the present invention, therefore, the interface 2714 (FIG. 27) is preferably implemented with one or more universal frequency translation (UFT) modules, such as the UFT module 102 (FIG. 1A). Thus previously described benefits of the present invention are obtained in wireless modems, WLANs, etc.

FIG. 30 illustrates an example block diagram embodiment of the interface 2714 that is associated with a computer or any other data processing and/or communications device. In FIG. 30, the receiver module 2718 includes a universal frequency down-converter (UFD) module 3014 and an optional analog to digital (A/D) converter 3016, which converts an analog output from the UFD 3014 to a digital format for the DSP 2720. The transmitter module 2716 includes an optional modulator 3012 and a universal frequency up-converter (UFU) module 3010. The optional modulator 3012 can be a variety of types of modulators, including conventional modulators. Alternatively, the UFU module 3010 includes modulator functionality. The example implementation of FIG. 30 operates substantially as described above and in co-pending U.S. Patent Applications titled, "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed October 21, 1998, issued as U.S. Patent No. 6,061,551 on May 9, 2000, and "Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, filed October 21, 1998, issued as U.S. Patent No. 6,091,940 on July 18, 2000, as well as other cited documents.

FIG. 31 illustrates an example implementation of the interface 2714 illustrated in FIG. 30, wherein the receiver UFD 3014 includes a UFT module 3112, and the transmitter UFU 3010 includes a universal frequency translation (UFT) module 3110. This example implementation operates substantially as described above and in co-pending U.S. Patent Applications titled, "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed October 21, 1998,issued as U.S. Patent No. 6,061,551 on May 9, 2000, and "Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, filed October 21, 1998, "Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, filed October 21, 1998, issued as U.S. Patent No. 6,091,940 on July 18, 2000, as well as other cited documents.

FIG. 32 illustrates an example I/Q implementation of the interface module 2710. Other I/Q implementations are also contemplated and are within the scope of the present invention.

In the example of FIG. 32, the receiver UFD module 3014 includes a signal divider 3228 that provides a received I/Q modulated carrier signal 3230 between a third UFT module 3224 and a fourth UFT module 3226. A phase shifter 3232, illustrated here as a 90 degree phase shifter, controls the third and fourth UFT modules 3224 and 3226 to operate 90 degrees out of phase with one another. As a result, the third and fourth UFT modules 3224 and 3226 down-convert and demodulate the received I/Q modulated carrier signal 3230, and output I and Q channels 3234 and 3236, respectively, which are provided to the DSP 2720 through the optional A/D converter 3016.

In the example of FIG. 32, the transmitter UFU module 3010 includes first and second UFT modules 3212 and 3214 and a phase shifter 3210, which is illustrated here as a 90 degree phase shifter. The phase shifter 3210 receives a lower frequency modulated carrier signal 3238 from the modulator 3012. The phase shifter 3210 controls the first and second UFT modules 3212 and 3214 to operate 90 degrees out of phase with one another. The first and second UFT modules 3212 and 3214 up-convert the lower frequency modulated carrier signal 3238, which are output as higher frequency modulated I and Q carrier channels 3218 and 3220, respectively. A signal combiner 3216 combines the higher frequency modulated I and Q carrier channels 3218 and 3220 into a single higher frequency modulated I/Q carrier signal 3222 for transmitting by the antenna 2712.

The example implementations of the interfaces described above, and variations thereof, can also be used to implement network interfaces, such as the network interface 2520 illustrated in FIG. 25.

6.1.2. Example Modifications

The RF modem applications, WLAN applications, etc., described herein, can be modified by incorporating one or more of the enhanced signal reception (ESR) techniques described herein. Use of ESR embodiments with the network embodiments described herein will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

The RF modem applications, WLAN applications, etc., described herein can be enhanced by incorporating one or more of the unified down-conversion and filtering (UDF) techniques described herein. Use of UDF embodiments with the network embodiments described herein will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

6.2. Other Example Applications

The application embodiments described above are provided for purposes of illustration. These applications and embodiments are not intended to limit the invention. Alternate and additional applications and embodiments, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. For example, such alternate and additional applications and embodiments include combinations of those described above. Such combinations will be apparent to persons skilled in the relevant art(s) based on the herein teachings.

7.0. Example WLAN Implementation Embodiments

7.1 Architecture

FIG. 39 is a block diagram of a WLAN interface 3902 (also referred to as a WLAN modem herein) according to an embodiment of the invention. The WLAN interface/modem 3902 includes an antenna 3904, a low noise amplifier or power amplifier (LNA/PA) 3904, a receiver 3906, a transmitter 3910, a control signal generator 3908, a demodulator/modulator facilitation module 3912, and a media access controller (MAC) interface 3914. Other embodiments may include different elements. The MAC interface 3914 couples the WLAN interface/modem 3902 to a computer 3916 or other data processing device. The computer 3916 preferably includes a MAC 3918.

The WLAN interface/modem 3902 represents a transmit and receive application that utilizes the universal frequency translation technology described herein. It also represents a zero IF (or direct-to-data) WLAN architecture.

The WLAN interface/modem 3902 also represents a vector modulator and a vector demodulator using the universal frequency translation (UFT) technology described herein. Use of the UFT technology enhances the flexibility of the WLAN application (i.e., makes it universal).

In the embodiment shown in FIG. 39, the WLAN interface/modem 3902 is compliant with WLAN standard IEEE 802.11. However, the invention is not limited to this standard. The invention is applicable to any communication standard or specification, as will be appreciated by persons skilled in the relevant art(s) based on the teachings contained herein. Any modifications to the invention to operate with other standards or specifications will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

In the embodiment shown in FIG. 39, the WLAN interface/modem 3902 provides half duplex communication. However, the invention is not limited to this communication mode. The invention is applicable and directed to other communication modes, as will be appreciated by persons skilled in the relevant art(s) based on the teachings contained herein.

In the embodiment shown in FIG. 39, the modulation/demodulation performed by the WLAN interface/modem 3902 is preferably direct sequence spread spectrum QPSK (quadrature phase shift keying) with differential encoding. However, the invention is not limited to this modulation/demodulation mode. The invention is applicable and directed to other modulation and demodulation modes, such as but not limited to those described herein, as well as frequency hopping according to IEEE 802.11, OFDM (orthogonal frequency division multiplexing), as well as others. These modulation/demodulation modes will be appreciated by persons skilled in the relevant art(s) based on the teachings contained herein.

The operation of the WLAN interface/modem 3902 when receiving shall now be described.

Signals 3922 received by the antenna 3903 are amplified by the LNA/PA 3904. The amplified signals 3924 are down-converted and demodulated by the receiver 3906. The receiver 3906 outputs I signal 3926 and Q signal 3928.

FIG. 40 illustrates an example receiver 3906 according to an embodiment of the invention. It is noted that the receiver 3906 shown in FIG. 40 represents a vector modulator. The "receiving" function performed by the WLAN interface/modem 3902 can be considered to be all processing performed by the WLAN interface/modem 3902 from the LNA/PA 3904 to generation of baseband information.

Signal 3924 is split by a 90 degree splitter 4001 to produce an I signal 4006A and Q signal 4006B that are preferably 90 degrees apart in phase. I and Q signals 4006A, 4006B are down-converted by UFD (universal frequency down-conversion) modules 4002A, 4002B. The UDF modules 4002A, 4002B output down-converted I and Q signals 3926, 3928. The UFD modules 4002A, 4002B each includes at least one UFT (universal frequency translation) module 4004A. UFD and UFT modules are described above. An example implementation of the receiver 3906 (vector demodulator) is shown in FIG. 53. An example BOM list for the receiver 3906 of FIG. 53 is shown in FIG. 54.

The demodulator/modulator facilitation module 3912 receives the I and Q signals 3926, 3928. The demodulator/modulator facilitation module 3912 amplifies and filters the I and Q signals 3926, 3928. The demodulator/modulator facilitation module 3912 also performs automatic gain control (AGC) functions. The AGC function is coupled with the universal frequency translation technology described herein. The demodulator/modulator facilitation module 3912 outputs processed I and Q signals 3930, 3932.

The MAC interface 3914 receives the processed I and Q signals 3930, 3932. The MAC interface 3914 preferably includes a baseband processor. The MAC interface 3914 preferably performs functions such as combining the I and Q signals 3930, 3932, and arranging the data according to the protocol/file formal being used. Other functions performed by the MAC interface 3914 and the baseband processor contained therein will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The MAC interface 3914 outputs the baseband information signal, which is received and processed by the computer 3916 in an implementation and application specific manner.

In the example embodiment of FIG. 39, the demodulation function is distributed among the receiver 3906, the demodulator/modulator facilitation module 3912, and a baseband processor contained in the MAC interface 3914. The functions collectively performed by these components include, but are not limited to, despreading the information, differentially decoding the information, tracking the carrier phase, descrambling, recreating the data clock, and combining the I and Q signals. The invention is not limited to this arrangement. These demodulation-type functions can be centralized in a single component, or distributed in other ways.

The operation of the WLAN interface/modem 3902 when transmitting shall now be described.

A baseband information signal 3936 is received by the MAC interface 3914 from the computer 3916. The MAC interface 3914 preferably performs functions such as splitting the baseband information signal to form I and Q signals 3930, 3932, and arranging the data according to the protocol/file formal being used. Other functions performed by the MAC interface 3914 and the baseband processor contained therein will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

The demodulator/modulator facilitation module 3912 filters and amplifies the I and Q signals 3930, 3932. The demodulator/modulator facilitation module 3912 outputs processed I and Q signals 3942, 3944. Preferably, at least some filtering and/or amplifying components in the demodulator/modulator facilitation module 3912 are used for both the transmit and receive paths.

The transmitter 3910 up-converts the processed I and Q signals 3942, 3944, and combines the up-converted I and Q signals. This up-converted/combined signal is amplified by the LNA/PA 3904, and then transmitted via the antenna 3904.

FIG. 41 illustrates an example transmitter 3910 according to an embodiment of the invention. The device in FIG. 41 can also be called a vector modulator. In an embodiment, the "transmit" function performed by the WLAN interface/modem 3902 can be considered to be all processing performed by the WLAN interface/modem 3902 from receipt of baseband information through the LNA/PA 3904. An example implementation of the transmitter 3910 (vector modulator) is shown in FIGS. 57-60. The data conditioning interfaces 5802 in FIG. 58 effectively pre-process the I and Q signals 3942, 3944 before being received by the UFU modules 4102. An example BOM list for the transmitter 3910 of FIGS. 57-60 is shown in FIGS. 61A and 61B.

I and Q signals 3942, 3944 are received by UFU (universal frequency up-conversion) modules 4102A, 4102B. The UFU modules 4102A, 4102B each includes at least one UFT module 4104A, 4104B. The UFU modules 4102A, 4102B up-convert I and Q signals 3942, 3944. The UFU modules 4102A, 4102B output up-converted I and Q signals 4106, 4108. The 90 degree combiner 4110 effectively phase shifts either the I signal 4106 or the Q signal 4108 by 90 degrees, and then combines the phase shifted signal with the unshifted signal to generate a combined, up-converted I/Q signal 3946.

In the example embodiment of FIG. 39, the modulation function is distributed among the transmitter 3910, the demodulator/modulator facilitation module 3912, and a baseband processor contained in the MAC interface 3914. The functions collectively performed by these components include, but are not limited to, differentially encoding data, splitting the baseband information signal into I and Q signals, scrambling data, and data spreading. The invention is not limited to this arrangement. These modulation-type functions can be centralized in a single component, or distributed in other ways.

An example implementation of the transmitter 3910 (vector modulator) is shown in FIGS. 57-60. The data conditioning interfaces 5802 in FIG. 58 effectively pre-process the I and Q signals 3942, 3944 before being received by the UFU modules 4102. An example BOM list for the transmitter 3910 of FIGS. 57-60 is shown in FIGS. 61A and 61B.

The components in the WLAN interface/modem 3902 are preferably controlled by the MAC interface 3914 in operation with the MAC 3918 in the computer 3916. This is represented by the distributed control arrow 3940 in FIG. 39. Such control includes setting the frequency, data rate, whether receiving or transmitting, and other communication characteristics/modes that will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. In embodiments, control signals are sent over the corresponding wireless medium and received by the antenna 3904, and sent to the MAC 3918.

FIG. 42 illustrates an example implementation of the WLAN interface/modem 3902. It is noted that in this implementation example, the MAC interface 3914 is located on a different board. FIG. 62 is an example motherboard corresponding to FIG. 42. FIG.

63 is an example bill-of-materials (BOM) list for the motherboard of FIG. 62. This and other implementations are provided herein for example purposes only. Other implementations will be apparent to persons skilled in the relevant art(s), and the invention is directed to such other implementations.

FIG. 102 illustrates an alternate example PCMCIA test bed assembly for a WLAN interface/modem 3902 according to an embodiment of the invention. In this embodiment, the baseband processor 10202 is separate from the MAC interface 3914.

In some applications, it is desired to separate the receive path and the transmit path. FIG. 43 illustrates an example receive implementation, and FIG. 44 illustrates an example transmit implementation.

7.2 Receiver

Example embodiments and implementations of the IQ receiver 3906 will be discussed as follows. The example embodiments and implementations include multi-phase embodiments that are useful for reducing or eliminating unwanted DC offsets and circuit re-radiation. The invention is not limited to these example receiver embodiments. Other receiver embodiments will be understood by those skilled in the relevant arts based on the discussion given herein. These other embodiments are within the scope and spirit of the present invention.

7.2.1 IQ Receiver

An example embodiment of the receiver 3906 is shown in FIG. 67A. Referring to FIG. 67A, the UFD module 4002A (FIG. 40) is configured so that the UFT module 4004A is coupled to a storage module 6704A. The UFT module 4004A is a controlled switch 6702A that is controlled by the control signal 3920A. The storage module 6704A is a capacitor 6706A. However, other storage modules could be used including an inductor, as will be understood by those skilled in the relevant arts. Likewise, the UFD module 4002B (FIG. 40) is configured so that the UFT module 4004B is coupled to a storage module 6704B. The UFT module 4004B is a controlled switch 6702B that is controlled by the control signal 3920B. The storage module 6704B is a capacitor 6706B. However, other storage modules could be used including an inductor, as will be understood by those skilled in the relevant arts. The operation of the receiver 3906 is discussed as follows.

The 90 degree splitter 4001 receives the received signal 3924 from the LNA/PA module 3904. The 90 degree splitter 4001 divides the signal 3924 into an I signal 4006A and a Q signal 4006B.

The UFD module 4002A receives the I signal 4006A and down-converts the I signal 4006A using the control signal 3920A to a lower frequency signal I 3926. More specifically, the controlled switch 6702A samples the I signal 4006A according to the control signal 3920A, transferring charge (or energy) to the storage module 6704A. The charge stored during successive samples of the I signal 4006A, results in the down-converted signal I signal 3926. Likewise, UFD module 4002B receives the Q signal 4006B and down-converts the Q signal 4006B using the control signal 3920B to a lower frequency signal Q 3928. More specifically, the controlled switch 6702B samples the Q signal 4006B according to the control signal 3920B, resulting in charge (or energy) that is stored in the storage module 6704B. The charge stored during successive samples of the I signal 4006A, results in the down-converted signal Q signal 3928.

Down-conversion utilizing a UFD module (also called an aliasing module) is further described in the above referenced applications, such as "Method and System for Down-converting Electromagnetic Signals," Ser. No. 09/176,022, now U.S. Patent No. 6,061,551. As discussed in the '551 patent, the control signals 3920A,B can be configured as a plurality of pulses that are established to improve energy transfer from the signals 4006A,B to the down-converted signals 3926 and 3928, respectively. In other words, the pulse widths of the control signals 3920 can be adjusted to increase and/or optimize the energy transfer from the signals 4006 to the down-converted output signals 3926 and 3938, respectively. Additionally, matched filter principles can be implemented to shape the sampling pulses of the control signal 3920, and therefore further improve energy transfer to the down-converted output signal 3106. Matched filter principle and energy transfer are further described in the above referenced applications, such as U.S. patent application titled, "Method and System for Down-Converting an Electromagnetic Signal, Transforms For Same, and Aperture Relationships", Ser. No. 09/550,644, filed on April 14, 2000.

The configuration of the UFT based receiver 3906 is flexible. In FIG. 67A, the controlled switches 6702 are in a series configuration relative to the signals 4006. Alternatively, FIG 67B illustrates the controlled switches 6702 in a shunt configuration so that the switches 6702 shunt the signals 4006 to ground.

Additionally in FIGs. 67A-B, the 90 degree phase shift between the I and Q channels is realized with the 90 degree splitter 4001. Alternatively, FIG. 68A illustrates a receiver 6806 in series configuration, where the 90 degree phase shift is realized by shifting the control signal 3920B by 90 degrees relative to the control signal 3920A. More specifically, the 90 degree shifter 6804 is added to shift the control signal 3920B by 90 degrees relative to the control signal 3920A. As such, the splitter 6802 is an in-phase (i.e. 0 degree) signal splitter. FIG. 68B illustrates an embodiment of the receiver 3906 of the receiver 3906 in a shunt configuration with 90 degree delays on the control signal.

Furthermore, the configuration of the controlled switch 6702 is also flexible. More specifically, the controlled switches 6702 can be implemented in many different ways, including transistor switches. FIG. 69A illustrates the UFT modules 6702 in a series configuration and implemented as FETs 6902, where the gate of each FET 6902 is controlled by the respective control signal 3920. As such, the FET 6902 samples the respective signal 4006, according to the respective control signal 3920. FIG. 69B illustrates the shunt configuration.

7.2.2 Multi-Phase IQ Receiver

FIG. 70A illustrates an exemplary I/Q modulation receiver 7000, according to an embodiment of the present invention. I/Q modulation receiver 7000 has additional advantages of reducing or eliminating unwanted DC offsets and circuit re-radiation. As will be apparent, the IQ receiver 7000 can be described as a multi-phase receiver to those skilled in the arts.

I/Q modulation receiver 7000 comprises a first UFD module 7002, a first optional filter 7004, a second UFD module 7006, a second optional filter 7008, a third UFD module 7010, a third optional filter 7012, a fourth UFD module 7014, a fourth filter 7016, an optional LNA 7018, a first differential amplifier 7020, a second differential amplifier 7022, and an antenna 7072.

I/Q modulation receiver 7000 receives, down-converts, and demodulates a I/Q modulated RF input signal 7082 to an I baseband output signal 7084, and a Q baseband output signal 7086. I/Q modulated RF input signal 7082 comprises a first information signal and a second information signal that are I/Q modulated onto an RF carrier signal. I baseband output signal 7084 comprises the first baseband information signal. Q baseband output signal 7086 comprises the second baseband information signal.

Antenna 7072 receives I/Q modulated RF input signal 7082. I/Q modulated RF input signal 7082 is output by antenna 7072 and received by optional LNA 7018. When present, LNA 7018 amplifies I/Q modulated RF input signal 7082, and outputs amplified I/Q signal 7088.

First UFD module 7002 receives amplified I/Q signal 7088. First UFD module 7002 down-converts the I-phase signal portion of amplified input I/Q signal 7088 according to an I control signal 7090. First UFD module 7002 outputs an I output signal 7098.

In an embodiment, first UFD module 7002 comprises a first storage module 7024, a first UFT module 7026, and a first voltage reference 7028. In an embodiment, a switch contained within first UFT module 7026 opens and closes as a function of I control signal 7090. As a result of the opening and closing of this switch, which respectively couples and de-couples first storage module 7024 to and from first voltage reference 7028, a down-converted signal, referred to as I output signal 7098, results. First voltage reference 7028 may be any reference voltage, and is preferably ground. I output signal 7098 is stored by first storage module 7024.

In an embodiment, first storage module 7024 comprises a first capacitor 7074. In addition to storing I output signal 7098, first capacitor 7074 reduces or prevents a DC offset voltage resulting from charge injection from appearing on I output signal 7098.

I output signal 7098 is received by optional first filter 7004. When present, first filter 7004 is in some embodiments a high pass filter to at least filter I output signal 7098 to remove any carrier signal "bleed through". In a preferred embodiment, when present, first filter 7004 comprises a first resistor 7030, a first filter capacitor 7032, and a first filter voltage reference 7034. Preferably, first resistor 7030 is coupled between I output signal 7098 and a filtered I output signal 7007, and first filter capacitor 7032 is coupled between filtered I output signal 7007 and first filter voltage reference 7034. Alternately, first filter 7004 may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant art(s). First filter 7004 outputs filtered I output signal 7007.

Second UFD module 7006 receives amplified I/Q signal 7088. Second UFD module 7006 down-converts the inverted I-phase signal portion of amplified input I/Q signal 7088 according to an inverted I control signal 7092. Second UFD module 7006 outputs an inverted I output signal 7001.

In an embodiment, second UFD module 7006 comprises a second storage module 7036, a second UFT module 7038, and a second voltage reference 7040. In an embodiment, a switch contained within second UFT module 7038 opens and closes as a function of inverted I control signal 7092. As a result of the opening and closing of this switch, which respectively couples and de-couples second storage module 7036 to and from second voltage reference 7040, a down-converted signal, referred to as inverted I output signal 7001, results. Second voltage reference 7040 may be any reference voltage, and is preferably ground. Inverted I output signal 7001 is stored by second storage module 7036.

In an embodiment, second storage module 7036 comprises a second capacitor 7076. In addition to storing inverted I output signal 7001, second capacitor 7076 reduces or prevents a DC offset voltage resulting from charge injection from appearing on inverted I output signal 7001.

Inverted I output signal 7001 is received by optional second filter 7008. When present, second filter 7008 is a high pass filter to at least filter inverted I output signal 7001 to remove any carrier signal "bleed through". In a preferred embodiment, when present, second filter 7008 comprises a second resistor 7042, a second filter capacitor

7044, and a second filter voltage reference 7046. Preferably, second resistor 7042 is coupled between inverted I output signal 7001 and a filtered inverted I output signal 7009, and second filter capacitor 7044 is coupled between filtered inverted I output signal 7009 and second filter voltage reference 7046. Alternately, second filter 7008 may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant art(s). Second filter 7008 outputs filtered inverted I output signal 7009.

First differential amplifier 7020 receives filtered I output signal 7007 at its non-inverting input and receives filtered inverted I output signal 7009 at its inverting input. First differential amplifier 7020 subtracts filtered inverted I output signal 7009 from filtered I output signal 7007, amplifies the result, and outputs I baseband output signal 7084. Because filtered inverted I output signal 7009 is substantially equal to an inverted version of filtered I output signal 7007, I baseband output signal 7084 is substantially equal to filtered I output signal 7009, with its amplitude doubled. Furthermore, filtered I output signal 7007 and filtered inverted I output signal 7009 may comprise substantially equal noise and DC offset contributions from prior down-conversion circuitry, including first UFD module 7002 and second UFD module 7006, respectively. When first differential amplifier 7020 subtracts filtered inverted I output signal 7009 from filtered I output signal 7007, these noise and DC offset contributions substantially cancel each other.

Third UFD module 7010 receives amplified I/Q signal 7088. Third UFD module 7010 down-converts the Q-phase signal portion of amplified input I/Q signal 7088 according to an Q control signal 7094. Third UFD module 7010 outputs an Q output signal 7003.

In an embodiment, third UFD module 7010 comprises a third storage module 7048, a third UFT module 7050, and a third voltage reference 7052. In an embodiment, a switch contained within third UFT module 7050 opens and closes as a function of Q control signal 7094. As a result of the opening and closing of this switch, which respectively couples and de-couples third storage module 7048 to and from third voltage reference 7052, a down-converted signal, referred to as Q output signal 7003, results.

Third voltage reference 7052 may be any reference voltage, and is preferably ground. Q output signal 7003 is stored by third storage module 7048.

In an embodiment, third storage module 7048 comprises a third capacitor 7078. In addition to storing Q output signal 7003, third capacitor 7078 reduces or prevents a DC offset voltage resulting from charge injection from appearing on Q output signal 7003.

Q output signal 7003 is received by optional third filter 7012. When present, in an embodiment, third filter 7012 is a high pass filter to at least filter Q output signal 7003 to remove any carrier signal "bleed through". In an embodiment, when present, third filter 7012 comprises a third resistor 7054, a third filter capacitor 7056, and a third filter voltage reference 7058. Preferably, third resistor 7054 is coupled between Q output signal 7003 and a filtered Q output signal 7011, and third filter capacitor 7056 is coupled between filtered Q output signal 7011 and third filter voltage reference 7058. Alternately, third filter 7012 may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant art(s). Third filter 7012 outputs filtered Q output signal 7011.

Fourth UFD module 7014 receives amplified I/Q signal 7088. Fourth UFD module 7014 down-converts the inverted Q-phase signal portion of amplified input I/Q signal 7088 according to an inverted Q control signal 7096. Fourth UFD module 7014 outputs an inverted Q output signal 7005.

In an embodiment, fourth UFD module 7014 comprises a fourth storage module 7060, a fourth UFT module 7062, and a fourth voltage reference 7064. In an embodiment, a switch contained within fourth UFT module 7062 opens and closes as a function of inverted Q control signal 7096. As a result of the opening and closing of this switch, which respectively couples and de-couples fourth storage module 7060 to and from fourth voltage reference 7064, a down-converted signal, referred to as inverted Q output signal 7005, results. Fourth voltage reference 7064 may be any reference voltage, and is preferably ground. Inverted Q output signal 7005 is stored by fourth storage module 7060.

In an embodiment, fourth storage module 7060 comprises a fourth capacitor 7080. In addition to storing inverted Q output signal 7005, fourth capacitor 7080 reduces or prevents a DC offset voltage resulting from charge injection from appearing on inverted Q output signal 7005.

Inverted Q output signal 7005 is received by optional fourth filter 7016. When present, fourth filter 7016 is a high pass filter to at least filter inverted Q output signal 7005 to remove any carrier signal "bleed through". In a preferred embodiment, when present, fourth filter 7016 comprises a fourth resistor 7066, a fourth filter capacitor 7068, and a fourth filter voltage reference 7070. Preferably, fourth resistor 7066 is coupled between inverted Q output signal 7005 and a filtered inverted Q output signal 7013, and fourth filter capacitor 7068 is coupled between filtered inverted Q output signal 7013 and fourth filter voltage reference 7070. Alternately, fourth filter 7016 may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant art(s). Fourth filter 7016 outputs filtered inverted Q output signal 7013.

Second differential amplifier 7022 receives filtered Q output signal 7011 at its non-inverting input and receives filtered inverted Q output signal 7013 at its inverting input. Second differential amplifier 7022 subtracts filtered inverted Q output signal 7013 from filtered Q output signal 7011, amplifies the result, and outputs Q baseband output signal 7086. Because filtered inverted Q output signal 7013 is substantially equal to an inverted version of filtered Q output signal 7011, Q baseband output signal 7086 is substantially equal to filtered Q output signal 7013, with its amplitude doubled. Furthermore, filtered Q output signal 7011 and filtered inverted Q output signal 7013 may comprise substantially equal noise and DC offset contributions of the same polarity from prior down-conversion circuitry, including third UFD module 7010 and fourth UFD module 7014, respectively. When second differential amplifier 7022 subtracts filtered inverted Q output signal 7013 from filtered Q output signal 7011, these noise and DC offset contributions substantially cancel each other.

Additional embodiments relating to addressing DC offset and re-radiation concerns, applicable to the present invention, are described in co-pending Patent Application No. 09/526,041,entitled "DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," Attorney Docket No. 1744.0880000, which is herein incorporated by reference in its entirety.

7.2.2.1 Example I/Q Modulation Control Signal Generator Embodiments

FIG. 70B illustrates an exemplary block diagram for I/Q modulation control signal generator 7023, according to an embodiment of the present invention. I/Q modulation control signal generator 7023 generates I control signal 7090, inverted I control signal 7092, Q control signal 7094, and inverted Q control signal 7096 used by I/Q modulation receiver 7000 of FIG. 70A. I control signal 7090 and inverted I control signal 7092 operate to down-convert the I-phase portion of an input I/Q modulated RF signal. Q control signal 7094 and inverted Q control signal 7096 act to down-convert the Q-phase portion of the input I/Q modulated RF signal. Furthermore, I/Q modulation control signal generator 7023 has the advantage of generating control signals in a manner such that resulting collective circuit re-radiation is radiated at one or more frequencies outside of the frequency range of interest. For instance, potential circuit re-radiation is radiated at a frequency substantially greater than that of the input RF carrier signal frequency.

I/Q modulation control signal generator 7023 comprises a local oscillator 7025, a first divide-by-two module 7027, a 180 degree phase shifter 7029, a second divide-by-two module 7031, a first pulse generator 7033, a second pulse generator 7035, a third pulse generator 7037, and a fourth pulse generator 7039.

Local oscillator 7025 outputs an oscillating signal 7015. FIG. 70C shows an exemplary oscillating signal 7015.

First divide-by-two module 7027 receives oscillating signal 7015, divides oscillating signal 7015 by two, and outputs a half frequency LO signal 7017 and a half frequency inverted LO signal 7041. FIG. 70C shows an exemplary half frequency LO signal 7017. Half frequency inverted LO signal 7041 is an inverted version of half frequency LO signal 7017. First divide-by-two module 7027 may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant art(s).

180 degree phase shifter 7029 receives oscillating signal 7015, shifts the phase of oscillating signal 7015 by 180 degrees, and outputs phase shifted LO signal 7019. 180 degree phase shifter 7029 may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant art(s). In alternative embodiments, other amounts of phase shift may be used.

Second divide-by two module 7031 receives phase shifted LO signal 7019, divides phase shifted LO signal 7019 by two, and outputs a half frequency phase shifted LO signal 7021 and a half frequency inverted phase shifted LO signal 7043. FIG. 70C shows an exemplary half frequency phase shifted LO signal 7021. Half frequency inverted phase shifted LO signal 7043 is an inverted version of half frequency phase shifted LO signal 7021. Second divide-by-two module 7031 may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant art(s).

First pulse generator 7033 receives half frequency LO signal 7017, generates an output pulse whenever a rising edge is received on half frequency LO signal 7017, and outputs I control signal 7090. FIG. 70C shows an exemplary I control signal 7090.

Second pulse generator 7035 receives half frequency inverted LO signal 7041, generates an output pulse whenever a rising edge is received on half frequency inverted LO signal 7041, and outputs inverted I control signal 7092. FIG. 70C shows an exemplary inverted I control signal 7092.

Third pulse generator 7037 receives half frequency phase shifted LO signal 7021, generates an output pulse whenever a rising edge is received on half frequency phase shifted LO signal 7021, and outputs Q control signal 7094. FIG. 70C shows an exemplary Q control signal 7094.

Fourth pulse generator 7039 receives half frequency inverted phase shifted LO signal 7043, generates an output pulse whenever a rising edge is received on half frequency inverted phase shifted LO signal 7043, and outputs inverted Q control signal 7096. FIG. 70C shows an exemplary inverted Q control signal 7096.

In an embodiment, control signals 7090, 7021, 7041 and 7043 include pulses having a width equal to one-half of a period of I/Q modulated RF input signal 7082. The invention, however, is not limited to these pulse widths, and control signals 7090, 7021, 7041, and 7043 may comprise pulse widths of any fraction of, or multiple and fraction of, a period of I/Q modulated RF input signal 7082.

First, second, third, and fourth pulse generators 7033, 7035, 7037, and 7039 may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant art(s).

As shown in FIG. 70C, in an embodiment, control signals 7090, 7021, 7041, and 7043 comprise pulses that are non-overlapping in other embodiments the pulses may overlap. Furthermore, in this example, pulses appear on these signals in the following order: I control signal 7090, Q control signal 7094, inverted I control signal 7092, and inverted Q control signal 7096. Potential circuit re-radiation from I/Q modulation receiver 7000 may comprise frequency components from a combination of these control signals.

For example, FIG. 70D shows an overlay of pulses from I control signal 7090, Q control signal 7094, inverted I control signal 7092, and inverted Q control signal 7096. When pulses from these control signals leak through first, second, third, and/or fourth UFD modules 7002, 7006, 7010, and 7014 to antenna 7072 (shown in FIG. 70A), they may be radiated from I/Q modulation receiver 7000, with a combined waveform that appears to have a primary frequency equal to four times the frequency of any single one of control signals 7090, 7021, 7041, and 7043. FIG. 70 shows an example combined control signal 7045.

FIG. 70D also shows an example I/Q modulation RF input signal 7082 overlaid upon control signals 7090, 7094, 7092, and 7096. As shown in FIG. 70D, pulses on I control signal 7090 overlay and act to down-convert a positive I-phase portion of I/Q modulation RF input signal 7082. Pulses on inverted I control signal 7092 overlay and act to down-convert a negative I-phase portion of I/Q modulation RF input signal 7082. Pulses on Q control signal 7094 overlay and act to down-convert a rising Q-phase portion of I/Q modulation RF input signal 7082. Pulses on inverted Q control signal 7096 overlay and act to down-convert a falling Q-phase portion of I/Q modulation RF input signal 7082.

As FIG. 70D further shows in this example, the frequency ratio between the combination of control signals 7090, 7021, 7041, and 7043 and I/Q modulation RF input signal 7082 is approximately 4:3. Because the frequency of the potentially re-radiated signal, i.e., combined control signal 7045, is substantially different from that of the signal being down-converted, i.e., I/Q modulation RF input signal 7082, it does not interfere with signal down-conversion as it is out of the frequency band of interest, and hence may be filtered out. In this manner, I/Q modulation receiver 7000 reduces problems due to circuit re-radiation. As will be understood by persons skilled in the relevant art(s) from the teachings herein, frequency ratios other than 4:3 may be implemented to achieve similar reduction of problems of circuit re-radiation.

It should be understood that the above control signal generator circuit example is provided for illustrative purposes only. The invention is not limited to these embodiments. Alternative embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) for I/Q modulation control signal generator 7023 will be apparent to persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the present invention.

FIG. 70S illustrates the receiver 7000, where the UFT modules 7028, 7038, 7050, and 7062 are configured with FETs 7099a-d.

Additional embodiments relating to addressing DC offset and re-radiation concerns, applicable to the present invention, are described in co-pending patent application no. 09/526, 041, entitled "DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," which is herein incorporated by reference in its entirety.

7.2.2.2 Implementation of Multi-phase I/Q Modulation Receiver Embodiment with Exemplary Waveforms

FIG. 70E illustrates a more detailed example circuit implementation of I/Q modulation receiver 7000, according to an embodiment of the present invention. FIGS.

70F-P show example waveforms related to an example implementation of I/Q modulation receiver 7000 of FIG. 70E.

FIGS. 70F and 70G show first and second input data signals 7047 and 7049 to be I/Q modulated with a RF carrier signal frequency as the I-phase and Q-phase information signals, respectively.

FIGS. 70I and 70J show the signals of FIG. 70F and 70G after modulation with a RF carrier signal frequency, respectively, as I-modulated signal 7051 and Q-modulated signal 7053.

FIG. 70H shows an I/Q modulation RF input signal 7082 formed from I-modulated signal 7051 and Q-modulated signal 7053 of FIGS. 70I and 70J, respectively.

FIG. 70O shows an overlaid view of filtered I output signal 7007 and filtered inverted I output signal 7009.

FIG. 70P shows an overlaid view of filtered Q output signal 7011 and filtered inverted Q output signal 7013.

FIGS. 70K and 70L show I baseband output signal 7084 and Q baseband output signal 7086, respectfully. A data transition 7055 is indicated in both I baseband output signal 7084 and Q baseband output signal 7086. The corresponding data transition 7055 is indicated in I-modulated signal 7051 of FIG. 70I, Q-modulated signal 7053 of FIG. 70J, and I/Q modulation RF input signal 7082 of FIG. 70H.

FIGS. 70M and 70N show I baseband output signal 7084 and Q baseband output signal 7086 over a wider time interval.

7.2.2.3 Example Single Channel Receiver Embodiment

FIG. 70Q illustrates an example single channel receiver 7091, corresponding to either the I or Q channel of I/Q modulation receiver 7000, according to an embodiment of the present invention. Single channel receiver 7091 can down-convert an input RF signal 7097 modulated according to AM, PM, FM, and other modulation schemes. Refer to section 7.2.1 above for further description on the operation of single channel receiver

7091. In other words, the single channel receiver 7091 is a one channel of the IQ receiver 7000 that was discussed in section 7.2.1.

7.2.2.4 Alternative Example I/Q Modulation Receiver Embodiment

FIG. 70R illustrates an exemplary I/Q modulation receiver 7089, according to an embodiment of the present invention. I/Q modulation receiver 7089 receives, down-converts, and demodulates an I/Q modulated RF input signal 7082 to an I baseband output signal 7084, and a Q baseband output signal 7086. I/Q modulation receiver 7089 has additional advantages of reducing or eliminating unwanted DC offsets and circuit re-radiation, in a similar fashion to that of I/Q modulation receiver 7000 described above.

7.3 Transmitter

Example embodiments and implementations of the IQ transmitter 3910 will be discussed as follows. The example embodiments and implementations include multi-phase embodiments that are useful for reducing or eliminating unwanted DC offsets that can result in unwanted carrier insertion.

7.3.1 Universal Transmitter with 2 UFT Modules

FIG. 71A illustrates a transmitter 7102 according to embodiments of the present invention. Transmitter 7102 includes a balanced modulator/up-converter 7104, a control signal generator 7142, an optional filter 7106, and an optional amplifier 7108. Transmitter 7102 up-converts a baseband signal 7110 to produce an output signal 7140 that is conditioned for wireless or wire line transmission. In doing so, the balanced modulator 7104 receives the baseband signal 7110 and samples the baseband signal in a differential and balanced fashion to generate a harmonically rich signal 7138. The harmonically rich signal 7138 includes multiple harmonic images, where each image contains the baseband information in the baseband signal 7110. The optional bandpass filter 7106 may be included to select a harmonic of interest (or a subset of harmonics) in the signal 7138 for transmission. The optional amplifier 7108 may be included to amplify the selected harmonic prior to transmission. The universal transmitter is further described at a high level by the flowchart 8400 that is shown in FIG. 84. A more detailed structural and operational description of the balanced modulator follows thereafter.

Referring to flowchart 8400, in step 8402, the balanced modulator 7104 receives the baseband signal 7110.

In step 8404, the balanced modulator 7104 samples the baseband signal in a differential and balanced fashion according to a first and second control signals that are phase shifted with respect to each other. The resulting harmonically rich signal 7138 includes multiple harmonic images that repeat at harmonics of the sampling frequency, where each image contains the necessary amplitude and frequency information to reconstruct the baseband signal 7110.

In embodiments of the invention, the control signals include pulses having pulse widths (or apertures) that are established to improve energy transfer to a desired harmonic of the harmonically rich signal 7138. In further embodiments of the invention, DC offset voltages are minimized between sampling modules as indicated in step 8406, thereby minimizing carrier insertion in the harmonic images of the harmonically rich signal 7138.

In step 8408, the optional bandpass filter 7106 selects the desired harmonic of interest (or a subset of harmonics) in from the harmonically rich signal 7138 for transmission.

In step 8410, the optional amplifier 7108 amplifies the selected harmonic(s) prior to transmission.

In step 8412, the selected harmonic(s) is transmitted over a communications medium.

7.3.1.1 Balanced Modulator Detailed Description

Referring to the example embodiment shown in FIG. 71A, the balanced modulator 7104 includes the following components: a buffer/inverter 7112; summer amplifiers 7118, 7119; UFT modules 7124 and 7128 having controlled switches 7148 and 7150, respectively; an inductor 7126; a blocking capacitor 7136; and a DC terminal 7111. As stated above, the balanced modulator 7104 differentially samples the baseband signal 7110 to generate a harmonically rich signal 7138. More specifically, the UFT modules 7124 and 7128 sample the baseband signal in differential fashion according to control signals 7123 and 7127, respectively. A DC reference voltage 7113 is applied to terminal 7111 and is uniformly distributed to the UFT modules 7124 and 7128. The distributed DC voltage 7113 prevents any DC offset voltages from developing between the UFT modules, which can lead to carrier insertion in the harmonically rich signal 7138. The operation of the balanced modulator 7104 is discussed in greater detail with reference to flowchart 8500 (FIG. 85), as follows.

In step 8402, the buffer/inverter 7112 receives the input baseband signal 7110 and generates input signal 7114 and inverted input signal 7116. Input signal 7114 is substantially similar to signal 7110, and inverted signal 7116 is an inverted version of signal 7114. As such, the buffer/inverter 7112 converts the (single-ended) baseband signal 7110 into differential input signals 7114 and 7116 that will be sampled by the UFT modules. Buffer/inverter 7112 can be implemented using known operational amplifier (op amp) circuits, as will be understood by those skilled in the arts, although the invention is not limited to this example.

In step 8504, the summer amplifier 7118 sums the DC reference voltage 7113 applied to terminal 7111 with the input signal 7114, to generate a combined signal 7120. Likewise, the summer amplifier 7119 sums the DC reference voltage 7113 with the inverted input signal 7116 to generate a combined signal 7122. Summer amplifiers 7118 and 7119 can be implemented using known op amp summer circuits, and can be designed to have a specified gain or attenuation, including unity gain, although the invention is not

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limited to this example. The DC reference voltage 7113 is also distributed to the outputs of both UFT modules 7124 and 7128 through the inductor 7126 as is shown.

In step 8506, the control signal generator 7142 generates control signals 7123 and 7127 that are shown by way of example in FIG. 72B and FIG. 72C, respectively. As illustrated, both control signals 7123 and 7127 have the same period T_S as a master clock signal 7145 (FIG.72A), but have a pulse width (or aperture) of T_A. In the example, control signal 7123 triggers on the rising pulse edge of the master clock signal 7145, and control signal 7127 triggers on the falling pulse edge of the master clock signal 7145. Therefore, control signals 7123 and 7127 are shifted in time by 180 degrees relative to each other. In embodiments of invention, the master clock signal 7145 (and therefore the control signals 7123 and 7127) have a frequency that is a sub-harmonic of the desired output signal 7140. The invention is not limited to the example of FIGs. 72A-72C.

In one embodiment, the control signal generator 7142 includes an oscillator 7146, pulse generators 7144a and 7144b, and an inverter 7147 as shown. In operation, the oscillator 7146 generates the master clock signal 7145, which is illustrated in FIG. 72A as a periodic square wave having pulses with a period of T_S. Other clock signals could be used including but not limited to sinusoidal waves, as will be understood by those skilled in the arts. Pulse generator 7144a receives the master clock signal 7145 and triggers on the rising pulse edge, to generate the control signal 7123. Inverter 7147 inverts the clock signal 7145 to generate an inverted clock signal 7143. The pulse generator 7144b receives the inverted clock signal 7143 and triggers on the rising pulse edge (which is the falling edge of clock signal 7145), to generate the control signal 7127.

FIG 89A-E illustrate example embodiments for the pulse generator 7144. FIG. 89A illustrates a pulse generator 8902. The pulse generator 8902 generates pulses 8908 having pulse width T_A from an input signal 8904. Example input signals 8904 and pulses 8908 are depicted in FIGs 89B and 89C, respectively. The input signal 8904 can be any type of periodic signal, including, but not limited to, a sinusoid, a square wave, a saw-tooth wave etc. The pulse width (or aperture) T_A of the pulses 8908 is determined by delay 8906 of the pulse generator 8902. The pulse generator 8902 also includes an optional inverter 8910, which is optionally added for polarity considerations as understood by those skilled in the arts. The example logic and implementation shown for the pulse generator 8902 is provided for illustrative purposes only, and is not limiting. The actual logic employed can take many forms. Additional examples of pulse generation logic are shown in FIGs. 89D and 89E. FIG. 89D illustrates a rising edge pulse generator 8912 that triggers on the rising edge of input signal 8904. FIG. 89E illustrates a falling edge pulse generator 8916 that triggers on the falling edge of the input signal 8904.

In step 8508, the UFT module 7124 samples the combined signal 7120 according to the control signal 7123 to generate harmonically rich signal 7130. More specifically, the switch 7148 closes during the pulse widths T_A of the control signal 7123 to sample the combined signal 7120 resulting in the harmonically rich signal 7130. FIG. 71B illustrates an exemplary frequency spectrum for the harmonically rich signal 7130 having harmonic images 7152a-n. The images 7152 repeat at harmonics of the sampling frequency $1/T_S$, at infinitum, where each image 7152 contains the necessary amplitude, frequency, and phase information to reconstruct the baseband signal 7110. As discussed further below, the relative amplitude of the frequency images is generally a function of the harmonic number and the pulse width T_A. As such, the relative amplitude of a particular harmonic 7152 can be increased (or decreased) by adjusting the pulse width T_A of the control signal 7123. In general, shorter pulse widths of T_A shift more energy into the higher frequency harmonics, and longer pulse widths of T_A shift energy into the lower frequency harmonics. The generation of harmonically rich signals by sampling an input signal according to a controlled aperture have been described earlier in this application in the section titled, "Frequency Up-conversion Using Universal Frequency Translation", and is illustrated by FIGs. 3-6. A more detailed discussion of frequency up-conversion using a switch with a controlled sampling aperture is discussed in the co-pending patent application titled, "Method and System for Frequency Up-Conversion," Ser. No./09/176,154, field on October 21, 1998, and incorporated herein by reference.

In step 8510, the UFT module 7128 samples the combined signal 7122 according to the control signal 7127 to generate harmonically rich signal 7134. More specifically, the switch 7150 closes during the pulse widths T_A of the control signal 7127 to sample the combined signal 7122 resulting in the harmonically rich signal 7134. The harmonically rich signal 7134 includes multiple frequency images of baseband signal 7110 that repeat at harmonics of the sampling frequency ($1/T_S$), similar to that for the harmonically rich signal 7130. However, the images in the signal 7134 are phase-shifted compared to those in signal 7130 because of the inversion of signal 7116 compared to signal 7114, and because of the relative phase shift between the control signals 7123 and 7127.

In step 8512, the node 7132 sums the harmonically rich signals 7130 and 7134 to generate harmonically rich signal 7133. FIG. 71C illustrates an exemplary frequency spectrum for the harmonically rich signal 7133 that has multiple images 7154a-n that repeat at harmonics of the sampling frequency $1/T_S$. Each image 7154 includes the necessary amplitude, frequency and phase information to reconstruct the baseband signal 7110. The capacitor 7136 operates as a DC blocking capacitor and substantially passes the harmonics in the harmonically rich signal 7133 to generate harmonically rich signal 7138 at the output of the modulator 7104.

In step 8408, the optional filter 7106 can be used to select a desired harmonic image for transmission. This is represented for example by a passband 7156 that selects the harmonic image 7154c for transmission in FIG. 71C.

An advantage of the modulator 7104 is that it is fully balanced, which substantially minimizes (or eliminates) any DC voltage offset between the two UFT modules 7124 and 7128. DC offset is minimized because the reference voltage 7113 contributes a consistent DC component to the input signals 7120 and 7122 through the summing amplifiers 7118 and 7119, respectively. Furthermore, the reference voltage 7113 is also directly coupled to the outputs of the UFT modules 7124 and 7128 through the inductor 7126 and the node 7132. The result of controlling the DC offset between the UFT modules is that carrier insertion is minimized in the harmonic images of the harmonically rich signal 7138. As discussed above, carrier insertion is substantially wasted energy because the information for a modulated signal is carried in the sidebands of the modulated signal and not in the carrier. Therefore, it is often desirable to minimize the energy at the carrier frequency by controlling the relative DC offset.

7.3.1.2 Balanced Modulator Example Signal Diagrams and Mathematical Description

In order to further describe the invention, FIGs. 72D-72I illustrate various example signal diagrams (vs. time) that are representative of the invention. These signal diagrams are meant for example purposes only and are not meant to be limiting. FIG. 72D illustrates a signal 7202 that is representative of the input baseband signal 7110 (FIG. 71A). FIG. 72E illustrates a step function 7204 that is an expanded portion of the signal 7202 from time t_0 to t_1, and represents signal 7114 at the output of the buffer/inverter 7112. Similarly, FIG. 72F illustrates a signal 7206 that is an inverted version of the signal 7204, and represents the signal 7116 at the inverted output of buffer/inverter 7112. For analysis purposes, a step function is a good approximation for a portion of a single bit of data (for the baseband signal 7110) because the clock rates of the control signals 7123 and 7127 are significantly higher than the data rates of the baseband signal 7110. For example, if the data rate is in the KHz frequency range, then the clock rate will preferably be in MHZ frequency range in order to generate an output signal in the Ghz frequency range.

Still referring to FIGs. 72D-I, FIG. 72G illustrates a signal 7208 that an example of the harmonically rich signal 7130 when the step function 7204 is sampled according to the control signal 7123 in FIG. 72B. The signal 7208 includes positive pulses 7209 as referenced to the DC voltage 7113. Likewise, FIG. 72H illustrates a signal 7210 that is an example of the harmonically rich signal 7134 when the step function 7206 is sampled according to the control signal 7127. The signal 7210 includes negative pulses 7211 as referenced to the DC voltage 7113, which are time-shifted relative the positive pulses 7209 in signal 7208.

Still referring to FIGs. 72D-I, the FIG. 72I illustrates a signal 7212 that is the combination of signal 7208 (FIG. 72G) and the signal 7210 (FIG. 72H), and is an example of the harmonically rich signal 7133 at the output of the summing node 7132. As illustrated, the signal 7212 spends approximately as much time above the DC reference voltage 7113 as below the DC reference voltage 7113 over a limited time period. For example, over a time period 7214, the energy in the positive pulses 7209a-b is canceled out by the energy in the negative pulses 7211a-b. This is indicative of minimal (or zero) DC offset between the UFT modules 7124 and 7128, which results in minimal carrier insertion during the sampling process.

Still referring to FIG. 72I, the time axis of the signal 7212 can be phased in such a manner to represent the waveform as an odd function. For such an arrangement, the Fourier series is readily calculated to obtain:

$$I_c(t) = \sum_{n=1}^{\infty} \left(\frac{4 \sin\left(\frac{n\pi T_A}{T_s}\right) \cdot \sin\left(\frac{n\pi}{2}\right)}{n\pi} \right) \cdot \sin\left(\frac{2n\pi t}{T_s}\right) \quad \textbf{\textit{Equation 1.}}$$

where: T_S = period of the master clock 7145

T_A = pulse width of the control signals 7123 and 7127

n= harmonic number

As shown by Equation 1, the relative amplitude of the frequency images is generally a function of the harmonic number *n*, and the ratio of T_A/T_S. As indicated, the T_A/T_S ratio represents the ratio of the pulse width of the control signals relative to the period of the sub-harmonic master clock. The T_A/T_S ratio can be optimized in order to maximize the amplitude of the frequency image at a given harmonic. For example, if a passband waveform is desired to be created at 5x the frequency of the sub-harmonic clock, then a baseline power for that harmonic extraction may be calculated for the fifth harmonic (n=5) as:

$$I_c(t) = \left(\frac{4 \sin\left(\frac{5\pi T_A}{T_s}\right)}{5\pi} \right) \cdot \sin(5\omega_s t) \qquad \textbf{\textit{Equation 2.}}$$

As shown by Equation 2, $I_C(t)$ for the fifth harmonic is a sinusoidal function having an amplitude that is proportional to the sin $(5\pi T_A/T_S)$. The signal amplitude can be maximized by setting $T_A = (1/10 \cdot T_S)$ so that $\sin(5\pi T_A/T_S) = \sin(\pi/2) = 1$. Doing so results in the equation:

$$I_c(t)\big|_{n=5} = \frac{4}{5\pi}\left(\sin\left(5\omega_s t\right)\right) \qquad \textbf{\textit{Equation 3.}}$$

This component is a frequency at 5x of the sampling frequency of sub-harmonic clock, and can be extracted from the Fourier series via a bandpass filter (such as bandpass filter 7106) that is centered around $5f_S$. The extracted frequency component can then be optionally amplified by the amplifier 7108 prior to transmission on a wireless or wire-line communications channel or channels.

Equation 3 can be extended to reflect the inclusion of a message signal as illustrated by equation 4 below:

$$m(t) \cdot I_c(t)\big|_{\substack{n=5 \\ \theta=\theta(t)}} = \frac{4 \cdot m(t)}{5\pi}\left(\sin\left(5\omega_s t + 5\theta(t)\right)\right) \qquad \textbf{\textit{Equation 4.}}$$

Equation 4 illustrates that a message signal can be carried in harmonically rich signals 7133 such that both amplitude and phase can be modulated. In other words, m(t) is modulated for amplitude and θ(t) is modulated for phase. In such cases, it should be noted that θ(t) is augmented modulo *n* while the amplitude modulation *m(t)* is simply scaled.

Therefore, complex waveforms may be reconstructed from their Fourier series with multiple aperture UFT combinations.

As discussed above, the signal amplitude for the 5th harmonic was maximized by setting the sampling aperture width T_A= 1/10 T_S, where T_S is the period of the master clock signal. This can be restated and generalized as setting T_A= ½ the period (or π radians) at the harmonic of interest. In other words, the signal amplitude of any harmonic *n* can be maximized by sampling the input waveform with a sampling aperture of T_A= ½ the period of the harmonic of interest (*n*). Based on this discussion, it is apparent that varying the aperture changes the harmonic and amplitude content of the output waveform. For example, if the sub-harmonic clock has a frequency of 200 MHZ, then the fifth harmonic is at 1Ghz. The amplitude of the fifth harmonic is maximized by setting the aperture width T_A= 500 picoseconds, which equates to ½ the period (or π radians) at 1 Ghz.

FIG. 72J depicts a frequency plot 7216 that graphically illustrates the effect of varying the sampling aperture of the control signals on the harmonically rich signal 7133 given a 200 MHZ harmonic clock. The frequency plot 7216 compares two frequency spectrums 7218 and 7220 for different control signal apertures given a 200 MHZ clock. More specifically, the frequency spectrum 7218 is an example spectrum for signal 7133 given the 200 MHZ clock with the aperture T_A = 500 psec (where 500 psec is π radians at the 5th harmonic of 1GHz). Similarly, the frequency spectrum 7220 is an example spectrum for signal 7133 given a 200 MHZ clock that is a square wave (so T_A = 5000 psec). The spectrum 7218 includes multiple harmonics 7218a-I, and the frequency spectrum 7220 includes multiple harmonics 7220a-e. [It is noted that spectrum 7220 includes only the odd harmonics as predicted by Fourier analysis for a square wave.] At 1 Ghz (which is the 5th harmonic), the signal amplitude of the two frequency spectrums 7218e and 7220c are approximately equal. However, at 200 MHZ, the frequency spectrum 7218a has a much lower amplitude than the frequency spectrum 7220a, and therefore the frequency spectrum 7218 is more efficient than the frequency spectrum 7220, assuming the desired harmonic is the 5th harmonic. In other words, assuming 1 Ghz is the desired harmonic, the frequency spectrum 7218 wastes less energy at the 200 MHZ fundamental than does the frequency spectrum 7218.

7.3.1.3 Balanced Modulator Having a Shunt Configuration

FIG. 79A illustrates a universal transmitter 7900 that is a second embodiment of a universal transmitter having two balanced UFT modules in a shunt configuration. (In contrast, the balanced modulator 7104 can be described as having a series configuration based on the orientation of the UFT modules.) Transmitter 7900 includes a balanced modulator 7901, the control signal generator 7142, the optional bandpass filter 7106, and the optional amplifier 7108. The transmitter 7900 up-converts a baseband signal 7902 to produce an output signal 7936 that is conditioned for wireless or wire line transmission. In doing so, the balanced modulator 7901 receives the baseband signal 7902 and shunts the baseband signal to ground in a differential and balanced fashion to generate a harmonically rich signal 7934. The harmonically rich signal 7934 includes multiple harmonic images, where each image contains the baseband information in the baseband signal 7902. In other words, each harmonic image includes the necessary amplitude, frequency, and phase information to reconstruct the baseband signal 7902. The optional bandpass filter 7106 may be included to select a harmonic of interest (or a subset of harmonics) in the signal 7934 for transmission. The optional amplifier 7108 may be included to amplify the selected harmonic prior to transmission, resulting in the output signal 7936.

The balanced modulator 7901 includes the following components: a buffer/inverter 7904; optional impedances 7910, 7912; UFT modules 7916 and 7922 having controlled switches 7918 and 7924, respectively; blocking capacitors 7928 and 7930; and a terminal 7920 that is tied to ground. As stated above, the balanced modulator 7901 differentially shunts the baseband signal 7902 to ground, resulting in a harmonically rich signal 7934. More specifically, the UFT modules 7916 and 7922 alternately shunts the baseband signal to terminal 7920 according to control signals 7123 and 7127, respectively. Terminal 7920 is tied to ground and prevents any DC offset voltages from developing between the UFT modules 7916 and 7922. As described above, a DC offset voltage can lead to undesired carrier insertion. The operation of the balanced modulator 7901 is described in greater detail according to the flowchart 8600 (FIG. 86) as follows.

In step 8402, the buffer/inverter 7904 receives the input baseband signal 7902 and generates I signal 7906 and inverted I signal 7908. I signal 7906 is substantially similar to the baseband signal 7902, and the inverted I signal 7908 is an inverted version of signal 7902. As such, the buffer/inverter 7904 converts the (single-ended) baseband signal 7902 into differential signals 7906 and 7908 that are sampled by the UFT modules. Buffer/inverter 7904 can be implemented using known operational amplifier (op amp) circuits, as will be understood by those skilled in the arts, although the invention is not limited to this example.

In step 8604, the control signal generator 7142 generates control signals 7123 and 7127 from the master clock signal 7145. Examples of the master clock signal 7145, control signal 7123, and control signal 7127 are shown in FIGs. 72A-C, respectively. As illustrated, both control signals 7123 and 7127 have the same period T_S as a master clock signal 7145, but have a pulse width (or aperture) of T_A. Control signal 7123 triggers on the rising pulse edge of the master clock signal 7145, and control signal 7127 triggers on the falling pulse edge of the master clock signal 7145. Therefore, control signals 7123 and 7127 are shifted in time by 180 degrees relative to each other. A specific embodiment of the control signal generator 7142 is illustrated in FIG. 71A, and was discussed in detail above.

In step 8606, the UFT module 7916 shunts the signal 7906 to ground according to the control signal 7123, to generate a harmonically rich signal 7914. More specifically, the switch 7918 closes and shorts the signal 7906 to ground (at terminal 7920) during the aperture width T_A of the control signal 7123, to generate the harmonically rich signal 7914. FIG. 79B illustrates an exemplary frequency spectrum for the harmonically rich signal 7918 having harmonic images 7950a-n. The images 7950 repeat at harmonics of the sampling frequency $1/T_S$, at infinitum, where each image 7950 contains the necessary amplitude, frequency, and phase information to reconstruct the baseband signal 7902. The generation of harmonically rich signals by sampling an input signal according to a controlled aperture have been described earlier in this application in the section titled, "Frequency Up-conversion Using Universal Frequency Translation", and is illustrated by FIGs. 3-6. A more detailed discussion of frequency up-conversion using a switch with a controlled sampling aperture is discussed in the co-pending patent application titled, "Method and System for Frequency Up-Conversion," Ser. No./09/176,154, field on October 21, 1998, and incorporated herein by reference.

The relative amplitude of the frequency images 7950 are generally a function of the harmonic number and the pulse width T_A. As such, the relative amplitude of a particular harmonic 7950 can be increased (or decreased) by adjusting the pulse width T_A of the control signal 7123. In general, shorter pulse widths of T_A shift more energy into the higher frequency harmonics, and longer pulse widths of T_A shift energy into the lower frequency harmonics, as described by equations 1-4 above. Additionally, the relative amplitude of a particular harmonic 7950 can also be adjusted by adding/tuning an optional impedance 7910. Impedance 7910 operates as a filter that emphasizes a particular harmonic in the harmonically rich signal 7914.

In step 8608, the UFT module 7922 shunts the inverted signal 7908 to ground according to the control signal 7127, to generate a harmonically rich signal 7926. More specifically, the switch 7924 closes during the pulse widths T_A and shorts the inverted I signal 7908 to ground (at terminal 7920), to generate the harmonically rich signal 7926. At any given time, only one of input signals 7906 or 7908 is shorted to ground because the pulses in the control signals 7123 and 7127 are phase shifted with respect to each other, as shown in FIGs. 72B and 72C.

The harmonically rich signal 7926 includes multiple frequency images of baseband signal 7902 that repeat at harmonics of the sampling frequency ($1/T_S$), similar to that for the harmonically rich signal 7914. However, the images in the signal 7926 are phase-shifted compared to those in signal 7914 because of the inversion of the signal 7908 compared to the signal 7906, and because of the relative phase shift between the control signals 7123 and 7127. The optional impedance 7912 can be included to emphasis a particular harmonic of interest, and is similar to the impedance 7910 above.

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In step 8610, the node 7932 sums the harmonically rich signals 7914 and 7926 to generate the harmonically rich signal 7934. The capacitors 7928 and 7930 operate as blocking capacitors that substantially pass the respective harmonically rich signals 7914 and 7926 to the node 7932. (The capacitor values may be chosen to substantially block baseband frequency components as well.) FIG. 79C illustrates an exemplary frequency spectrum for the harmonically rich signal 7934 that has multiple images 7952a-n that repeat at harmonics of the sampling frequency $1/T_S$. Each image 7952 includes the necessary amplitude, frequency, and phase information to reconstruct the baseband signal 7902. The optional filter 7106 can be used to select the harmonic image of interest for transmission. This is represented by a passband 7956 that selects the harmonic image 7932c for transmission.

An advantage of the modulator 7901 is that it is fully balanced, which substantially minimizes (or eliminates) any DC voltage offset between the two UFT modules 7912 and 7914. DC offset is minimized because the UFT modules 7916 and 7922 are both connected to ground at terminal 7920. The result of controlling the DC offset between the UFT modules is that carrier insertion is minimized in the harmonic images of the harmonically rich signal 7934. As discussed above, carrier insertion is substantially wasted energy because the information for a modulated signal is carried in the sidebands of the modulated signal and not in the carrier. Therefore, it is often desirable to minimize the energy at the carrier frequency by controlling the relative DC offset.

7.3.1.4 Balanced Modulator FET Configuration

As described above, the balanced modulators 7104 and 7901 utilize two balanced UFT modules to sample the input baseband signals to generate harmonically rich signals that contain the up-converted baseband information. More specifically, the UFT modules include controlled switches that sample the baseband signal in a balanced and differential fashion. FIGs. 71D and 79D illustrate embodiments of the controlled switch in the UFT module.

FIG. 71D illustrates an example embodiment of the modulator 7104 (FIG. 71B) where the controlled switches in the UFT modules are field effect transistors (FET). More specifically, the controlled switches 7148 and 7128 are embodied as FET 7158 and FET 7160, respectively. The FET 7158 and 7160 are oriented so that their gates are controlled by the control signals 7123 and 7127, so that the control signals control the FET conductance. For the FET 7158, the combined baseband signal 7120 is received at the source of the FET 7158 and is sampled according to the control signal 7123 to produce the harmonically rich signal 7130 at the drain of the FET 7158. Likewise, the combined baseband signal 7122 is received at the source of the FET 7160 and is sampled according to the control signal 7127 to produce the harmonically rich signal 7134 at the drain of FET 7160. The source and drain orientation that is illustrated is not limiting, as the source and drains can be switched for most FETs. In other words, the combined baseband signal can be received at the drain of the FETs, and the harmonically rich signals can be taken from the source of the FETs, as will be understood by those skilled in the relevant arts.

FIG. 79D illustrates an embodiment of the modulator 7900 (FIG. 79A) where the controlled switches in the UFT modules are field effect transistors (FET). More specifically, the controlled switches 7918 and 7924 are embodied as FET 7936 and FET 7938, respectively. The FETs 7936 and 7938 are oriented so that their gates are controlled by the control signals 7123 and 7127, respectively, so that the control signals determine FET conductance. For the FET 7936, the baseband signal 7906 is received at the source of the FET 7936 and shunted to ground according to the control signal 7123, to produce the harmonically rich signal 7914. Likewise, the baseband signal 7908 is received at the source of the FET 7938 and is shunted to grounding according to the control signal 7127, to produce the harmonically rich signal 7926. The source and drain orientation that is illustrated is not limiting, as the source and drains can be switched for most FETs, as will be understood by those skilled in the relevant arts.

7.3.1.5 Universal Transmitter Configured for Carrier Insertion

As discussed above, the transmitters 7102 and 7900 have a balanced configuration that substantially eliminates any DC offset and results in minimal carrier insertion in the output signal 7140. Minimal carrier insertion is generally desired for most applications because the carrier signal carries no information and reduces the overall transmitter efficiency. However, some applications require the received signal to have sufficient carrier energy for the receiver to extract the carrier for coherent demodulation. In support thereof, the present invention can be configured to provide the necessary carrier insertion by implementing a DC offset between the two sampling UFT modules.

FIG. 73A illustrates a transmitter 7302 that up-converts a baseband signal 7306 to an output signal 7322 having carrier insertion. As is shown, the transmitter 7302 is similar to the transmitter 7102 (FIG. 71A) with the exception that the up-converter/modulator 7304 is configured to accept two DC references voltages. In contrast, modulator 7104 was configured to accept only one DC reference voltage. More specifically, the modulator 7304 includes a terminal 7309 to accept a DC reference voltage 7308, and a terminal 7313 to accept a DC reference voltage 7314. Vr 7308 appears at the UFT module 7124 though summer amplifier 7118 and the inductor 7310. Vr 7314 appears at UFT module 7128 through the summer amplifier 7119 and the inductor 7316. Capacitors 7312 and 7318 operate as blocking capacitors. If Vr 7308 is different from Vr 7314 then a DC offset voltage will be exist between UFT module 7124 and UFT module 7128, which will be up-converted at the carrier frequency in the harmonically rich signal 7320. More specifically, each harmonic image in the harmonically rich signal 7320 will include a carrier signal as depicted in FIG. 73B.

FIG. 73B illustrates an exemplary frequency spectrum for the harmonically rich signal 7320 that has multiple harmonic images 7324a-n. In addition to carrying the baseband information in the sidebands, each harmonic image 7324 also includes a carrier signal 7326 that exists at respective harmonic of the sampling frequency $1/T_S$. The amplitude of the carrier signal increases with increasing DC offset voltage. Therefore, as the difference between Vr 7308 and Vr 7314 widens, the amplitude of each carrier signal 7326 increases. Likewise, as the difference between Vr 7308 and Vr 7314 shrinks, the amplitude of each carrier signal 7326 shrinks. As with transmitter 7302, the optional bandpass filter 7106 can be included to select a desired harmonic image for transmission. This is represented by passband 7328 in FIG. 73B.

7.3.2 Universal Transmitter In I Q Configuration:

As described above, the balanced modulators 7104 and 7901 up-convert a baseband signal to a harmonically rich signal having multiple harmonic images of the baseband information. By combining two balanced modulators, IQ configurations can be formed for up-converting I and Q baseband signals. In doing so, either the (series type) balanced modulator 7104 or the (shunt type) balanced modulator 7901 can be utilized. IQ modulators having both series and shunt configurations are described below.

7.3.2.1 IQ Transmitter Using Series-Type Balanced Modulator

FIG. 74 illustrates an IQ transmitter 7420 with an in-phase (I) and quadrature (Q) configuration according to embodiments of the invention. The transmitter 7420 includes an IQ balanced modulator 7410, an optional filter 7414, and an optional amplifier 7416. The transmitter 7420 is useful for transmitting complex I Q waveforms and does so in a balanced manner to control DC offset and carrier insertion. In doing so, the modulator 7410 receives an I baseband signal 7402 and a Q baseband signal 7404 and up-converts these signals to generate a combined harmonically rich signal 7412. The harmonically rich signal 7412 includes multiple harmonics images, where each image contains the baseband information in the I signal 7402 and the Q signal 7404. The optional bandpass filter 7414 may be included to select a harmonic of interest (or subset of harmonics) from the signal 7412 for transmission. The optional amplifier 7416 may be included to amplify the selected harmonic prior to transmission, to generate the IQ output signal 7418.

As stated above, the balanced IQ modulator 7410 up-converts the I baseband signal 7402 and the Q baseband signal 7404 in a balanced manner to generate the combined harmonically rich signal 7412 that carriers the I and Q baseband information. To do so, the modulator 7410 utilizes two balanced modulators 7104 from FIG. 71A, a signal combiner 7408, and a DC terminal 7407. The operation of the balanced modulator 7410 and other circuits in the transmitter is described according to the flowchart 8700 in FIG. 87, as follows.

In step 8702, the IQ modulator 7410 receives the I baseband signal 7402 and the Q baseband signal 7404.

In step 8704, the I balanced modulator 7104a samples the I baseband signal 7402 in a differential fashion using the control signals 7123 and 7127 to generate a harmonically rich signal 7411a. The harmonically rich signal 7411a contains multiple harmonic images of the I baseband information, similar to the harmonically rich signal 7130 in FIG. 71B.

In step 8706, the balanced modulator 7104b samples the Q baseband signal 7404 in a differential fashion using control signals 7123 and 7127 to generate harmonically rich signal 7411b, where the harmonically rich signal 7411b contains multiple harmonic images of the Q baseband signal 7404. The operation of the balanced modulator 7104 and the generation of harmonically rich signals was fully described above and illustrated in FIGs. 71A-C, to which the reader is referred for further details.

In step 8708, the DC terminal 7407 receives a DC voltage 7406 that is distributed to both modulators 7104a and 7104b. The DC voltage 7406 is distributed to both the input and output of both UFT modules 7124 and 7128 in each modulator 7104. This minimizes (or prevents) DC offset voltages from developing between the four UFT modules, and thereby minimizes or prevents any carrier insertion during the sampling steps 8704 and 8706.

In step 8710, the 90 degree signal combiner 7408 combines the harmonically rich signals 7411a and 7411b to generate IQ harmonically rich signal 7412. This is further illustrated in FIGs. 75A-C. FIG. 75A depicts an exemplary frequency spectrum for the harmonically rich signal 7411a having harmonic images 7502a-n. The images 7502 repeat at harmonics of the sampling frequency $1/T_S$, where each image 7502 contains the necessary amplitude and frequency information to reconstruct the I baseband signal 7402. Likewise, FIG. 75B depicts an exemplary frequency spectrum for the harmonically rich signal 7411b having harmonic images 7504a-n. The harmonic images 7504a-n also repeat at harmonics of the sampling frequency $1/T_S$, where each image 7504 contains the necessary amplitude, frequency, and phase information to reconstruct the Q baseband signal 7404. FIG.75C illustrates an exemplary frequency spectrum for the combined harmonically rich signal 7412 having images 7506. Each image 7506 carries the I baseband information and the Q baseband information from the corresponding images 7502 and 7504, respectively, without substantially increasing the frequency bandwidth occupied by each harmonic 7506. This can occur because the signal combiner 7408 phase shifts the Q signal 7411b by 90 degrees relative to the I signal 7411a. The result is that the images 7502a-n and 7504a-n effectively share the signal bandwidth do to their orthogonal relationship. For example, the images 7502a and 7504a effectively share the frequency spectrum that is represented by the image 7506a.

In step 8712, the optional filter 7414 can be included to select a harmonic of interest, as represented by the passband 7508 selecting the image 7506c in FIG. 75c.

In step 8714, the optional amplifier 7416 can be included to amplify the harmonic (or harmonics) of interest prior to transmission.

In step 8716, the selected harmonic (or harmonics) is transmitted over a communications medium.

FIG. 76A illustrates a transmitter 7608 that is a second embodiment for an I Q transmitter having a balanced configuration. Transmitter 7608 is similar to the transmitter 7420 except that the 90 degree phase shift between the I and Q channels is achieved by phase shifting the control signals instead of using a 90 degree signal combiner to combine the harmonically rich signals. More specifically, delays 7604a and 7604b delay the control signals 7123 and 7127 for the Q channel modulator 7104b by 90 degrees relative the control signals for the I channel modulator 7104a. As a result, the Q modulator 7104b samples the Q baseband signal 7404 with 90 degree delay relative to the sampling of the I baseband signal 7402 by the I channel modulator 7104a. Therefore, the Q harmonically rich signal 7411b is phase shifted by 90 degrees relative to the I harmonically rich signal.

Since the phase shift is achieved using the control signals, an in-phase signal combiner 7606 combines the harmonically rich signals 7411a and 7411b, to generate the harmonically rich signal 7412.

FIG. 76B illustrates a transmitter 7618 that is similar to transmitter 7608 in FIG. 76A. The difference being that the transmitter 7618 has a modulator 7620 that utilizes a summing node 7622 to sum the signals 7411a and 7411b instead of the in-phase signal combiner 7606 that is used in modulator 7602 of transmitter 7608.

FIG. 90A-90D illustrate various detailed circuit implementations of the transmitter 7420 in FIG. 74. These circuit implementations are meant for example purposes only, and are not meant to be limiting.

FIG. 90A illustrates I input circuitry 9002a and Q input circuitry 9002b that receive the I and Q input signals 7402 and 7404, respectively.

FIG. 90B illustrates the I channel circuitry 9006 that processes an I data 9004a from the I input circuit 9002a.

FIG. 90C illustrates the Q channel circuitry 9008 that processes the Q data 9004b from the Q input circuit 9002b.

FIG. 90D illustrates the output combiner circuit 9012 that combines the I channel data 9007 and the Q channel data 9010 to generate the output signal 7418.

7.3.2.2 IQ Transmitter Using Shunt-Type Balanced Modulator

FIG. 80 illustrates an IQ transmitter 8000 that is another IQ transmitter embodiment according to the present invention. The transmitter 8000 includes an IQ balanced modulator 8001, an optional filter 8012, and an optional amplifier 8014. During operation, the modulator 8001 up-converts an I baseband signal 8002 and a Q baseband signal 8004 to generate a combined harmonically rich signal 8011. The harmonically rich signal 8011 includes multiple harmonics images, where each image contains the baseband information in the I signal 8002 and the Q signal 8004. The optional bandpass filter 8012 may be included to select a harmonic of interest (or subset of harmonics) from the harmonically rich signal 8011 for transmission. The optional amplifier 8014 may be included to amplify the selected harmonic prior to transmission, to generate the IQ output signal 8016.

The IQ modulator 8001 includes two shunt balanced modulators 7901 from FIG. 79A, and a 90 degree signal combiner 8010 as shown. The operation of the IQ modulator 8001 is described in reference to the flowchart 8800 (FIG. 88), as follows. The order of the steps in flowchart 8800 is not limiting.

In step 8802, the balanced modulator 8001 receives the I baseband signal 8002 and the Q baseband signal 8004.

In step 8804, the balanced modulator 7901a differentially shunts the I baseband signal 8002 to ground according the control signals 7123 and 7127, to generate a harmonically rich signal 8006. More specifically, the UFT modules 7916a and 7922a alternately shunt the I baseband signal 8002 and an inverted version of the I baseband signal 8002 to ground according to the control signals 7123 and 7127, respectively. The operation of the balanced modulator 7901 and the generation of harmonically rich signals was fully described above and is illustrated in FIGs. 79A-C, to which the reader is referred for further details. As such, the harmonically rich signal 8006 contains multiple harmonic images of the I baseband information as described above.

In step 8806, the balanced modulator 7901b differentially shunts the Q baseband signal 8004 to ground according to control signals 7123 and 7127, to generate harmonically rich signal 8008. More specifically, the UFT modules 7916b and 7922b alternately shunt the Q baseband signal 8004 and an inverted version of the Q baseband signal 8004 to ground, according to the control signals 7123 and 7127, respectively. As such, the harmonically rich signal 8008 contains multiple harmonic images that contain the Q baseband information.

In step 8808, the 90 degree signal combiner 8010 combines the harmonically rich signals 8006 and 8008 to generate IQ harmonically rich signal 8011. This is further illustrated in FIGs. 81A-C. FIG. 81A depicts an exemplary frequency spectrum for the harmonically rich signal 8006 having harmonic images 8102a-n. The harmonic images 8102 repeat at harmonics of the sampling frequency $1/T_S$, where each image 8102 contains the necessary amplitude, frequency, and phase information to reconstruct the I baseband signal 8002. Likewise, FIG. 81B depicts an exemplary frequency spectrum for the harmonically rich signal 8008 having harmonic images 8104a-n. The harmonic images 8104a-n also repeat at harmonics of the sampling frequency $1/T_S$, where each image 8104 contains the necessary amplitude, frequency, and phase information to reconstruct the Q baseband signal 8004. FIG.81C illustrates an exemplary frequency spectrum for the IQ harmonically rich signal 8011 having images 8106a-n. Each image 8106 carries the I baseband information and the Q baseband information from the corresponding images 8102 and 8104, respectively, without substantially increasing the frequency bandwidth occupied by each image 8106. This can occur because the signal combiner 8010 phase shifts the Q signal 8008 by 90 degrees relative to the I signal 8006.

In step 8810, the optional filter 8012 may be included to select a harmonic of interest, as represented by the passband 8108 selecting the image 8106c in FIG. 81C.

In step 8812, the optional amplifier 8014 can be included to amplify the selected harmonic image 8106 prior to transmission.

In step 8814, the selected harmonic (or harmonics) is transmitted over a communications medium.

FIG. 82 illustrates a transmitter 8200 that is another embodiment for an IQ transmitter having a balanced configuration. Transmitter 8200 is similar to the transmitter 8000 except that the 90 degree phase shift between the I and Q channels is achieved by phase shifting the control signals instead of using a 90 degree signal combiner to combine the harmonically rich signals. More specifically, delays 8204a and 8204b delay the control signals 7123 and 7127 for the Q channel modulator 7901b by 90 degrees relative the control signals for the I channel modulator 7901a. As a result, the Q modulator 7901b samples the Q baseband signal 8004 with a 90 degree delay relative to the sampling of the I baseband signal 8002 by the I channel modulator 7901a. Therefore, the Q harmonically rich signal 8008 is phase shifted by 90 degrees relative to the I harmonically rich signal 8006. Since the phase shift is achieved using the control signals, an in-phase signal combiner 8206 combines the harmonically rich signals 8006 and 8008, to generate the harmonically rich signal 8011.

FIG.83 illustrates a transmitter 8300 that is similar to transmitter 8200 in FIG. 82. The difference being that the transmitter 8300 has a balanced modulator 8302 that utilizes a summing node 8304 to sum the I harmonically rich signal 8006 and the Q harmonically rich signal 8008 instead of the in-phase signal combiner 8206 that is used in the modulator 8202 of transmitter 8200. The 90 degree phase shift between the I and Q channels is implemented by delaying the Q clock signals using 90 degree delays 8204, as shown.

7.3.2.3 IQ Transmitters Configured for Carrier Insertion

The transmitters 7420 (FIG. 74) and 7608 (FIG. 76A) have a balanced configuration that substantially eliminates any DC offset and results in minimal carrier insertion in the IQ output signal 7418. Minimal carrier insertion is generally desired for most applications because the carrier signal carries no information and reduces the overall transmitter efficiency. However, some applications require the received signal to have sufficient carrier energy for the receiver to extract the carrier for coherent demodulation. In support thereof, FIG. 77 illustrates a transmitter 7702 to provide any necessary carrier insertion by implementing a DC offset between the two sets of sampling UFT modules.

Transmitter 7702 is similar to the transmitter 7420 with the exception that a modulator 7704 in transmitter 7702 is configured to accept two DC reference voltages so that the I channel modulator 7104a can be biased separately from the Q channel modulator 7104b. More specifically, modulator 7704 includes a terminal 7706 to accept a DC voltage reference 7707, and a terminal 7708 to accept a DC voltage reference 7709. Voltage 7707 biases the UFT modules 7124a and 7128a in the I channel modulator 7104a. Likewise, voltage 7709 biases the UFT modules 7124b and 7128b in the Q channel modulator 7104b. When voltage 7707 is different from voltage 7709, then a DC offset will appear between the I channel modulator 7104a and the Q channel modulator 7104b, which results in carrier insertion in the IQ harmonically rich signal 7412. The relative amplitude of the carrier frequency energy increases in proportion to the amount of DC offset.

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FIG. 78 illustrates a transmitter 7802 that is a second embodiment of an IQ transmitter having two DC terminals to cause DC offset, and therefore carrier insertion. Transmitter 7802 is similar to transmitter 7702 except that the 90 degree phase shift between the I and Q channels is achieved by phase shifting the control signals, similar to that done in transmitter 7608. More specifically, delays 7804a and 7804b phase shift the control signals 7123 and 7127 for the Q channel modulator 7104b relative to those of the I channel modulator 7104a. As a result, the Q modulator 7104b samples the Q baseband signal 7404 with 90 degree delay relative to the sampling of the I baseband signal 7402 by the I channel modulator 7104a. Therefore, the Q harmonically rich signal 7411b is phase shifted by 90 degrees relative to the I harmonically rich signal 7411a, which are combined by the in-phase combiner 7806.

7.4 Transceiver Embodiments

Referring to FIG. 39, in embodiments the receiver 3906, transmitter 3910, and LNA/PA 3904 are configured as a transceiver, such as but not limited to transceiver 9100, that is shown in FIG. 91.

Referring to FIG. 91, the transceiver 9100 includes a diplexer 9108, the IQ receiver 7000, and the IQ transmitter 8000. Transceiver 9100 up-converts an I baseband signal 9114 and a Q baseband signal 9116 using the IQ transmitter 8000 (FIG. 80) to generate an IQ RF output signal 9106. A detailed description of the IQ transmitter 8000 is included for example in section 7.3.2.2, to which the reader is referred for further details. Additionally, the transceiver 9100 also down-converts a received RF signal 9104 using the IQ Receiver 7000, resulting in I baseband output signal 9110 and a Q baseband output signal 9112. A detailed description of the IQ receiver 7000 is included in section 7.2.2, to which the reader is referred for further details.

7.5 Demodulator/Modulator Facilitation Module

An example demodulator/modulator facilitation module 3912 is shown in FIGS. 47 and 48. A corresponding BOM list is shown in FIGS. 49A and 49B.

An alternate example demodulator/modulator facilitation module 3912 is shown in FIGS. 50 and 51. A corresponding BOM list is shown in FIGS. 52A and 52B.

FIG. 52C illustrates an exemplary demodulator/modulator facilitation module 5201. Facilitation module 5201 includes the following: de-spread module 5204, spread module 5206, de-modulator 5210, and modulator 5212.

For receive, the de-spread module 5204 de-spreads received spread signals 3926 and 3928 using a spreading code 5202. Separate spreading codes can be used for the I and Q channels as will be understood by those skilled in the arts. The demodulator 5210 uses a signal 5208 to demodulate the de-spread received signals from the de-spread module 5204, to generate the I baseband signal 3930a and the Q baseband signal 3932a.

For transmit, the modulator 5212 modulates the I baseband signal 3930b and the Q baseband signal 3932b using a modulation signal 5208. The resulting modulated signals are then spread by the spread module 5206, to generate I spread signal 3942 and Q spread signal 3944.

In embodiments, the modulation scheme that is utilized is differential binary phase shift keying (DBPSK) or differential quadrature phase shift keying (DQPSK), and is compliant with the various versions of IEEE 802.11. Other modulation schemes could be utilized besides DBPSK or DQPSK, as will understood by those skilled in arts based on the discussion herein.

In embodiments, the spreading code 5202 is a Barker spreading code, and is compliant with the various versions of IEEE 802.11. More specifically, in embodiments, an 11-bit Barker word is utilized for spreading/de-spreading. Other spreading codes could be utilized as will be understood by those skilled in the arts based on the discussion herein.

7.6 MAC Interface

An example MAC interface 3914 is shown in FIG. 45. A corresponding BOM list is shown in FIGS. 46A and 46B.

In embodiments, the MAC 3918 and MAC interface 3914 supply the functionality required to provide a reliable delivery mechanism for user data over noisy, and unreliable wireless media. This is done this while also providing advanced LAN services, equal to or beyond those of existing wired LANs.

The first functionality of the MAC is to provide a reliable data delivery service to users of the MAC. Through a frame exchange protocol at the MAC level, the MAC significantly improves on the reliability of data delivery services over wireless media, as compared to earlier WLANs. More specifically, the MAC implements a frame exchange protocol to allow the source of a frame to determine when the frame has been successfully received at the destination. This frame exchange protocol adds some overhead beyond that of other MAC protocols, like IEEE 802.3, because it is not sufficient to simply transmit a frame and expect that the destination has received it correctly on the wireless media. In addition, it cannot be expected that every station in the WLAN is able to communicate with every other station in the WLAN. If the source does not receive this acknowledgment, then the source will attempt to transmit the frame again. This retransmission of frame by the source effectively reduces the effective error rate of the medium at the cost of additional bandwidth consumption.

The minimal MAC frame exchange protocol consists of two frames, a frame sent from the source to the destination and an acknowledgment from the destination that the frame was received correctly. The frame and its acknowledgment are an atomic unit of the MAC protocol. As such, they cannot be interrupted by the transmission from any other station. Additionally, a second set of frames may be added to the minimal MAC frame exchange. The two added frames are a request to send frame and a clear to send frame. The source sends a request to send to the destination. The destination returns a clear to send to the source. Each of these frames contains information that allows other stations receiving them to be notified of the upcoming frame transmission, and therefore to delay any transmission their own. The request to send and clear frames serve to announce to all stations in the neighborhood of both the source and the destination about the pending transmission from the source to the destination. When the source receives the clear to send from the destination, the real frame that the source wants delivered to the destination is sent. If the frame is correctly received at the destination, then the destination will return an acknowledgment. completing the frame exchange protocol. While this four way frame exchange protocol is a required function of the MAC, it may be disabled by an attribute in the management information base.

The second functionality of the MAC is to fairly control access to the shared wireless medium. It performs this function through two different access mechanisms: the basic access mechanism, call the distribution coordination system function, and a centrally controlled access mechanism, called the point coordination function.

The basic access mechanism is a carrier sense multiple access with collision avoidance (CSMA/CA) with binary exponential backoff.. This access mechanism is similar to that used for IEEE 802.3, with some variations. CSMA/CA is a "listen before talk" (LBT) access mechanism. In this type of access mechanism, a station will listen to the medium before beginning a transmission. If the medium is already carrying a transmission, then the station that listening will not begin its own transmission. More specifically , if a listening station detects an existing transmission in progress, the listening station enters a transmit deferral period determined by the binary exponential backoff algorithm. The binary exponential backoff mechanism chooses a random number which represents the amount of time that must elapse while there are not any transmission. In other words, the medium is idle before the listening station may attempt to begin its transmission again. The MAC may also implement a network allocation vector (NAV). The NAV is the value that indicates to a station that amount of time that remains before a medium becomes available. The NAV is kept current through duration values that are transmitted in all frames. By examining the NAV, a station may avoid transmitting, even when the medium does not appear to be carrying a transmission in the physical sense.

The centrally controlled access mechanism uses a poll and response protocol to eliminate the possibility of contention for the medium. This access mechanism is called the point coordination function (PCF). A point coordinator (PC) controls the PCF. The PC is always located in an AP. Generally, the PCF operates by stations requesting that the PC register them on a polling list, and the PC then regularly polls the stations for traffic while also delivering traffic to the stations. With proper planning, the PCF is able to deliver near isochronous service to the stations on the polling list.

The third function of the MAC is to protect the data that it delivers. Because it is difficult to contain wireless WLAN signals to a particular physical area, the MAC provides a privacy service, called Wired Equivalent Privacy (WEP), which encrypts the data sent over the wireless medium. The level of encryption chosen approximates the level of protection data might have on a wireless LAN in a building with controlled access that prevents physically connecting to the LAN without authorization.

7.7 Control Signal Generator - Synthesizer

In an embodiment, the control signal generator 3908 is preferably implemented using a synthesizer. An example synthesizer is shown in FIG. 55. A corresponding BOM list is shown in FIGS. 56A and 56B.

7.8 LNA/PA

An example LNA/PA 3904 is shown in FIGS. 64 and 65. A corresponding BOM list is shown in FIG. 66.

Additionally, FIG. 93 illustrates a LNA/PA module 9301 that is another embodiment of the LNA/PA 3904. LNA/PA module 9301 includes a switch 9302, a LNA 9304, and a PA 9306. The switch 9302 connects either the LNA 9304 or the PA 9306 to the antenna 3903, as shown. The switch 9302 can be controlled by an on -board processor that is not shown.

8.0 802.11 Physical Layer Configurations

The 802.11 WLAN standard specifies two RF physical layers: frequency hopped spread spectrum (FHSS) and direct sequence spread spectrum (DSSS). The invention is not limited to these specific examples. Both DSSS and FHSS support 1 Mbps and 2 Mbps data rates and operate in the 2.400-2.835 GHz band for wireless communications in accordance to FCC part 15 and ESTI-300 rules. Additionally, 802.11 has added an 11 Mbps standard that operates at 5 GHz and utilizes OFDM modulation.

The DSSS configuration supports the 1 MBPS data rate utilizing differential binary phase shift keying (DBPSK) modulation, and supports 2 MBPS utilizing differential quadrature phase shift keying modulation. In embodiments, an 11-bit Barker word is used as the spreading sequence that is utilized by the stations in the 802.11 network. A Barker word has a relatively short sequence, and is known to have very good correlation properties, and includes the following sequence: +1, -1, +1, +1, -1, +1, +1, +1, -1, -1, -1. The Barker word used for 802.11 is not to be confused with the spreading codes used for code division multiple access (CDMA) and global positioning system (GPS). CDMA and GPS use orthogonal spreading codes, which allow multiple users to operate on the same channel frequency. Generally, CDMA codes have longer sequences and have richer correlation properties.

During transmission, the 11-bit barker word is exclusive-ored (EX-OR) with each of the information bits using a modulo-2 adder, as illustrated by modulo-2 adder 9202 in FIG. 92 . Referring to FIG. 92, the11-bit (at 11 MBPS) Barker word is applied to a modulo-2 adder together with each one (at 1 MBPS) of the information bits (in the PPDU data). The Ex-OR function combines both signals by performing a modulo-2 addition of each information bit with each Barker bit (or chip). The output of the modulo-2 adder results in a signal with a data rate that is 10x higher than the information rate. The result in the frequency domain signal is a signal that is spread over a wider bandwidth at a reduced RF power level. At the receiver, the DSSS signal is convolved with an 11-bit Barker word and correlated. As shown in FIG. 92, the correlation recovers the information bits at the transmitted information rate, and the undesired interfering in-band signals are spread out-of-band. The spreading and despreading of narrowband to wideband signal is commonly referred to as processing gain and is measured in decibels (dB). Processing gain is the ratio of DSSS signal rate information rate. In embodiments, the minimum requirement for processing gain is 10 dB.

The second RF physical layer that is specified by the IEEE 802.11 standard is frequency hopping spread spectrum (FHSS). A set of hop sequences is defined in IEEE 802.11 for use in the 2.4 GHz frequency band. The channels are evenly spaced across the band over a span of 83.5 MHz. During the development of IEEE 802.11, the hop sequences listed in the standard were pre-approved for operation in North America, Europe, and Japan. In North America and Europe (excluding Spain and France), the required number of hop channels is 79. The number of hopped channels for Spain and France is 23 and 35, respectively. In Japan, the required number of hopped channels is 23. The hopped center channels are spaced uniformly across the 2.4 GHz frequency band occupying a bandwidth of 1MHz. In North America and Europe (excluding Spain and France), the hopped channels operate from 2.402 GHz to 2.480 GHz. In Japan, the hopped channels operate from 2.447 GHz to 2.473 GHz. The modulation scheme called out for FHSS by 802.11 is 2-level Gaussian Phase Shift Keying (GFSK) for the 1 MBps data rate, and 4-level GFSK for the 2 MBps data rate.

In addition to DSSS and FHSS RF layer standards, the IEEE 802.11 Executive Committee approved two projects for higher rate physical layer extensions. The first extension, IEEE 802.11a defines requirements for a physical layer operating in the 5.0 GHz frequency band, and data rates ranging from 6 MBps to 54 MBps. This 802.11a draft standard is based on Orthogonal Frequency Division Multiplexing (OFDM) and uses 48 carriers as a phase reference (so coherent), with 20 MHZ spacing between the channels. The second extension, IEEE 802.11b, defines a set of physical layer specifications operating in the 2.4 GHz ISM frequency band. This 802.11b utilizes complementary code keying (CCK), and extends the data rate up to 5.5 Mbps and 11 Mbps.

The transmitter and receiver circuits described herein can be operated in all of the WLAN physical layer embodiments described herein, including the DSSS and FHSS embodiments described herein. However, the present invention is not limited to being operated in WLAN physical layer embodiments that were described herein, as the invention could be configured in other physical layer embodiments.

Figure 94 illustrates a block diagram of an IEEE 802.11 DSSS radio transceiver 9400 using UFT Zero IF technology. DSSS transceiver 9400 includes: antenna 9402, switch 9404, amplifiers 9406 and 9408, transceivers 9410, baseband processor 9412, MAC 9414, bus interface unit 9416, and PCMCIA connector 9418. The DSSS transceiver 9400 includes an IQ receiver 7000 and an IQ transmitter 8000, which are described herein. UFT technology interfaces directly to the baseband processor 9412 of the physical layer. In the receive path, the IQ receiver 7000 transforms a 2.4GHz RF signal-of-interest into I/Q analog baseband signals in a single step and passes the signals to the baseband processor 9412, where the baseband processor is then responsible for de-spreading and demodulating the signal. In embodiments, the IQ receiver 7000 includes all of the circuitry necessary for accommodating AGC, baseband filtering and baseband amplification. In the transmit path, the transmitter 8000 transforms the I/Q analog baseband signals to a 2.4GHz RF carrier directly in a single step. The signal conversion clock is derived from a single synthesized local oscillator (LO) 9420. The selection of the clock frequency is determined by choosing a sub-harmonic of the carrier frequency. For example, a 5th harmonic of 490 MHZ was used, which corresponds to a RF channel frequency of 2.450GHz. Using UFT technology simplifies the requirements and complexity of the synthesizer design.

9. Appendix

The attached Appendix contained in FIGS. 95A-C, 96-161, which forms part of this patent application, includes schematics of an integrated circuit (IC) implementation example of the present invention. This example embodiment is provided solely for illustrative purposes , and is not limiting. Other embodiments will be apparent to persons skilled in the relevant art(s) based on the teachings herein. FIG. 95A illustrates a schematic for a WLAN modulator/demodulator IC according to embodiments of the invention. FIGs. 95B and 95C illustrate an expanded view of the circuit in FIG. 95A. FIGs. 96-161 further illustrate detailed circuit schematics of the WLAN modulator/demodulator integrated circuit.

10. Conclusions

Example implementations of the systems and components of the invention have been described herein. As noted elsewhere, these example implementations have been described for illustrative purposes only, and are not limiting. Other implementation embodiments are possible and covered by the invention, such as but not limited to software and software/hardware implementations of the systems and components of the invention. Such implementation embodiments will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

While various application embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

What Is Claimed Is:

1. A wireless modem apparatus, comprising:

a balanced transmitter for up-converting a baseband signal, including,

an inverter, to receive said baseband signal and generate an inverted baseband signal;

a first controlled switch, coupled to a non-inverting output of said inverter, said first controlled switch to sample said baseband signal according to a first control signal, resulting in a first harmonically rich signal;

a second controlled switch, coupled to an inverting output of said inverter, said second controlled switch to sample said inverted baseband signal according to a second control signal, resulting in a second harmonically rich signal; and

a combiner, coupled to an output of said first controlled switch and an output of said second controlled switch, said combiner to combine said first harmonically rich signal and said second harmonically rich signal, resulting in a third harmonically rich signal.

2. The apparatus of claim 1, wherein said second control signal is phase shifted with respect to said first control signal.

3. The apparatus of claim 1, wherein said second control signal is phase shifted by 180 degrees with respect to said first control signal.

4. The apparatus of claim 1, wherein said first control signal and said second control signal each comprise a plurality of pulses having an associated pulse width T_A that operates to improve energy transfer to a desired harmonic image in said harmonically rich signal.

5. The apparatus ~~of claim~~ 4, wherein said pulse width T_A is approximately ½ of a period of said desired harmonic.

6. The apparatus of claim 1, further comprising a filter attached to an output of said combiner, wherein said filter selects a desired harmonic from said third harmonically rich signal.

7. The apparatus of claim 1, further comprising:

a balanced receiver, coupled to said balanced modulator, said receiver including,

a first universal frequency down-conversion module to down-convert an input signal, wherein said first universal frequency down-conversion module down-converts said input signal according to a third control signal and outputs a first down-converted signal;

a second universal frequency down-conversion module to down-convert said input signal, wherein said second universal frequency down-conversion module down-converts said input signal according to a fourth control signal and outputs a second down-converted signal; and

a subtractor module that subtracts said second down-converted signal from said first down-converted signal and outputs a down-converted signal.

8. The apparatus of claim 7, wherein said fourth control signal is delayed relative to said third control signal by .5 + n cycles of said input signal, wherein n may be any integer greater than or equal to 1.

9. The apparatus of claim 7, wherein said first universal frequency down-conversion module under-samples said input signal according to said third control signal, and said second universal frequency down-conversion module under-samples said input signal according to said fourth control signal.

10. The apparatus of claim 7, wherein said third and said fourth control signals each comprise a train of pulses having pulse widths that are established to improve energy transfer from said input signal to said first and said second down-converted signals, respectively.

11. The apparatus of claim 10, wherein said train of pulses have a pulse width that is approximately a fraction of a period of said input signal.

12. The apparatus of claim 10, wherein said train of pulses have pulse width that is approximately multiple periods and a fraction of a period of said input signal.

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13. The apparatus of claim 10, wherein said first and said second universal frequency down-conversion modules each comprise a switch and a storage element.

14. The apparatus of claim 13, wherein said storage element comprises a capacitor that reduces a DC offset voltage ~~in said~~ first down-converted signal and said second down-converted signal.

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15. The apparatus of claim 7, wherein said subtractor module comprises a differential amplifier.

16. The apparatus of claim 7, further comprising an antenna coupled to said balanced transmitter and said balanced receiver.

17. The apparatus of claim 16, further comprising a switch, said switch connecting either said transmitter or said receiver to said antenna.

18. The apparatus of claim 7, further comprising a baseband processor coupled to said transmitter and said receiver.

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19. The apparatus of claim 7, further comprising a media access controller (MAC) coupled to said transmitter and said receiver.

20. The apparatus of claim 19, wherein said MAC comprises a means for controlling accessing to a WLAN medium.

21. The apparatus of claim 20, wherein said means for controlling includes carrier sense multiple access with collision avoidance (CSMA/CA).

22. The apparatus of claim 7, further comprising a demodulator/modulator facilitation module coupled to said transmitter and receiver.

23. The apparatus of claim 22, wherein said demodulator/modulator facilitation module comprises a means for modulating said baseband signal using differential binary phase shift keying (DBPSK).

24. The apparatus of claim 22, wherein said demodulator/modulator facilitation module comprises a means for de-modulating said down-converted signal using differential binary phase shift keying (DBPSK).

25. The apparatus of claim 22, wherein said demodulator/modulator facilitation module comprises a means for spreading said baseband signal.

26. The apparatus of claim 25, wherein said means for spreading comprises a means for spreading said baseband signal using a Barker code.

27. The apparatus of claim 22, wherein said demodulator/modulator facilitation module comprises a means for de-spreading said down-converted signal.

28. The apparatus of claim 27, wherein said means for de-spreading comprises a means for de-spreading said down-converted signal using a Barker code.

29. The apparatus of claim 1, wherein said apparatus is an infrastructure device.

30. The apparatus of claim 1, wherein said apparatus is a client device.

31. The apparatus of claim 1, wherein said first controlled switch shunts said baseband signal to a reference potential according to said first control signal, and wherein said second controlled switch shunts said inverted baseband signal to said reference potential according to said second control signal.

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32. A method of transmitting a baseband signal over a wireless LAN, comprising the steps of:

(1) spreading the baseband signal using a spreading code, resulting in a spread baseband signal; and

(2) differentially sampling the spread baseband signal according to a first control signal and a second control signal resulting in a plurality of harmonic images that are each representative of the baseband signal, wherein said first and second control signals have pulse widths that improve energy transfer to a desired harmonic image of said plurality of harmonics.

33. The method of claim 32, further comprising the step of:

(3) modulating the baseband signal using phase shift keying prior to step (1).

34. The method of claim 32, further comprising the steps of:

(3) determining availability of a WLAN medium; and

(4) transmitting said desired harmonic over said WLAN medium if said medium is available.

35. The method of claim 34, wherein step (3) comprises the step of determining availability of said WLAN medium using carrier sense multiple access (CSMA) protocol.

36. The method of claim 32, wherein said step (2) comprises the step of:

(a) converting said baseband signal into a differential baseband signal having a first differential baseband component and a second differential baseband component;

(b) sampling said first differential component according to said first control signal to generate a first harmonically rich signal, and sampling said second differential component according to said second control signal to generate a second harmonically rich signal, wherein said second control signal is phase shifted relative to said first control signal; and

(c) combining said first harmonically rich signal and said second harmonically rich signal to generate said harmonic images.

37. The method of claim 32, further comprising the step of:

(3) minimizing DC offset voltages between sampling modules during step (2), and thereby minimizing carrier insertion in said harmonic images.

38. The method of claim 32, wherein said pulse widths are approximately ½ of a period of said desired harmonic.

39. In a wireless LAN device, a method of down-converting a received RF signal, comprising the steps of:

down-converting said received RF signal according to a first control signal and a second control signal, resulting in a down-converted signal, wherein said second control signal is delayed relative to said first control signal by .5 + n cycles of said received RF signal, wherein n may be any integer greater than or equal to 1;

de-spreading said down-converted signal using a spreading code, resulting in a de-spread signal; and

de-modulating said de-spread signal, resulting in a de-modulated signal;

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wherein said ~~first~~ and said second control signals each comprise a train of pulses having pulse widths that are established to improve energy transfer from said received RF signal to said down-converted signal.

40. The method of claim 39, wherein said pulse widths are approximately ½ of a period of said received RF signal.

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Bib Data Sheet

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/632,856	08/04/2000 RULE –	455	2745	1744.0630003

APPLICANTS

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Michael W. Rawlins, Lake Mary, FL ;

** CONTINUING DATA *************************

THIS APPLN CLAIMS BENEFIT OF 60/147,129 08/04/1999 O.K.

** FOREIGN APPLICATIONS ********************

IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 09/26/2000

	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
Foreign Priority claimed ☐ yes ☑ no 35 USC 119 (a-d) conditions met ☐ yes ☐ no ☐ Met after Allowance Verified and Acknowledged ______ Examiner's Signature ______ Initials	FL	208	40	3

ADDRESS

Sterne Kessler Goldstein & Fox P L L C
Suite 600 1100 New York Avenue N W
Washington ,DC 20005-3934

TITLE

Wireless local area network (WLAN) using universal frequency translation technology including multi-phase embodiments and circuit implementations

FILING FEE RECEIVED		
1200	FEES: Authority has been given in Paper No. _________ to charge/credit DEPOSIT ACCOUNT No. _________ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other ____________ ☐ Credit

PATENT APPLICATION FEE DETERMINATION RECORD
Effective December 29, 1999

Application or Docket Number

CLAIMS AS FILED - PART I

FOR	NUMBER FILED (Column 1)	NUMBER EXTRA (Column 2)	SMALL ENTITY RATE	SMALL ENTITY FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY FEE
BASIC FEE				345.00	OR		690.00
TOTAL CLAIMS	40 minus 20=	* 20	X$ 9=		OR	X$18=	360
INDEPENDENT CLAIMS	3 minus 3 =	* —	X39=		OR	X78=	—
MULTIPLE DEPENDENT CLAIM PRESENT			+130=		OR	+260=	—
			TOTAL		OR	TOTAL	1050

SMALL ENTITY TYPE ☐ OR OTHER THAN SMALL ENTITY

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

AMENDMENT A

A	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	SMALL ENTITY RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	ADDITIONAL FEE
Total	* 33	Minus	** 40	=	X$ 9=		OR	X$18=	
Independent	* 3	Minus	*** 3	=	X39=		OR	X78=	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					+130=		OR	+260=	
					TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

B	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	SMALL ENTITY RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	ADDITIONAL FEE
Total	* 38	Minus	** 40	=	X$ 9=		OR	X$18=	
Independent	* 3	Minus	*** 3	=	X39=		OR	X78=	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					+130=		OR	+260=	
					TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	SMALL ENTITY RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	ADDITIONAL FEE
Total	*	Minus	**	=	X$ 9=		OR	X$18=	
Independent	*	Minus	***	=	X39=		OR	X78=	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					+130=		OR	+260=	
					TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20"
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

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APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
09/632,856	08/04/2000	David F. Sorrells	1744.0630003

Sterne Kessler Goldstein & Fox P L L C
Suite 600 1100 New York Avenue N W
Washington, DC 20005-3934

FORMALITIES LETTER

OC000000005428327

Date Mailed: 09/26/2000

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given TWO MONTHS from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
  Applicant must submit **$ 690** *to complete the basic filing fee and/or file a small entity statement claiming such status (37 CFR 1.27).*
- Total additional claim fee(s) for this application is $360.
  - **$360** for **20** total claims over 20.
- The oath or declaration is missing.
  A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.

- **The balance due by applicant is $ 1180.**

A copy of this notice MUST be returned with the reply.

E. B

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PART 3 - OFFICE COPY

09/26/00

Section 1

#3

FEE TRANSMITTAL for FY 2001

Patent fees are subject to annual revision.

OIPE JC100 NOV 2 0 2000 PATENT & TRADEMARK OFFICE

Complete if Known	
Application Number	09/632,856
Filing Date	August 4, 2000
First Named Inventor	David F. Sorrells
Examiner Name	To be Assigned
Group Art Unit	2745
Attorney Docket No.	1744.0630003/MQL/JTH

TOTAL AMOUNT OF PAYMENT ($) 1,200.00

METHOD OF PAYMENT (check one)

1. ☐ The Commissioner is hereby authorized to charge indicated fees and credit any overpayment to:

Deposit Account Number	19-0036
Deposit Account Name	Sterne, Kessler, Goldstein & Fox P.L.L.C.

☒ Charge Any Additional Fee Required Under 37 CFR §§ 1.16 and 1.17

☐ Applicant claims small entity status See 37 CFR 1.27

2. ☒ Payment Enclosed:

☒ Check ☐ Credit card ☐ Money Order ☒ Other*

*Charge any deficiencies or credit any overpayments in the fees or fee calculations of Parts 1, 2 and 3 below to Deposit Account No. 19-0036.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	710	201	355	Utility filing fee	$710.00
106	320	206	160	Design filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 710.00

2. EXTRA CLAIM FEES

			Extra	Fee from below	Fee Paid
Total Claims	40	- 20** =	20	X $18.00	= $360.00
Indep. Claims	3	- 3** =	0	X $80.00	= 0.00
Multiple Dependent					=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim
108	80	209	40	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 360.00

** *or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee paid
105	130	205	65	Surcharge - late filing fee or oath	130.00
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for *ex parte* reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	390	216	195	Extension for reply within second month	
117	890	217	445	Extension for reply within third month	
118	1,390	218	695	Extension for reply within fourth month	
128	1,890	228	945	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,240	241	620	Petition to revive - unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	130	123	130	Petitions related to provisional applications	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	481	40	Recording each patent assignment per property (times number of properties)	
146	710	246	355	Filing a submission after final rejection (37 CFR 1.129(a))	
149	710	249	355	For each additional invention to be examined (37 CFR 1.129(b))	
179	710	279	355	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) :

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 130.00

SUBMITTED BY				Complete (*If applicable*)	
Name (*Print/Type*)	Michael Q. Lee	Registration No. (*Attorney/Agent*)	35,239	Telephone	202-371-2600
Signature				Date	11/20/00

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

173

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
09/632,856	08/04/2000	David F. Sorrells	1744.0630003

Sterne Kessler Goldstein & Fox P L L C
Suite 600 1100 New York Avenue N W
Washington, DC 20005-3934

OIPE JC100
NOV 2 0 2000
PATENT & TRADEMARK OFFICE

FORMALITIES LETTER

OC000000005428327

Date Mailed: 09/26/2000

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given TWO MONTHS from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
  Applicant must submit **$ 690** *to complete the basic filing fee and/or file a small entity statement claiming such status (37 CFR 1.27).*
- Total additional claim fee(s) for this application is $360.
  - **$360** for **20** total claims over 20.
- The oath or declaration is missing.
  A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.

- **The balance due by applicant is $ 1180.**

A copy of this notice MUST be returned with the reply.

11/21/2000 HKDOR1 00000018 09632856
01 FC:101 710.00 OP
02 FC:105 130.00 OP
03 FC:103 360.00 OP

E. Bn

Customer Service Center
Initial Patent Examination Division (703) 308-1202

PART 2 - COPY TO BE RETURNED WITH RESPONSE

P-3

OIPE JC100 NOV 2 0 2000 PATENT & TRADEMARK OFFICE

Declaration for Patent Application

Docket Number: 1744.0050003/MQL/JTH

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter that is claimed and for which a patent is sought on the invention entitled **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations**, the specification of which is attached hereto unless the following box is checked:

☒ was filed on August 4, 2000;
as United States Application Number or PCT International Application Number 09/632,856; and
was amended on ___________________ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information that is material to patentability as defined in 37 C.F.R. § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT international application, which designated at least one country other than the United States listed below, and have also identified below any foreign application for patent or inventor's certificate, or PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s) Priority Claimed

			Priority Claimed	
___________ (Application No.)	___________ (Country)	___________ (Day/Month/Year Filed)	☐ Yes	☐ No
___________ (Application No.)	___________ (Country)	___________ (Day/Month/Year Filed)	☐ Yes	☐ No

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

60/147,129 (Application No.)	August 4, 1999 (Filing Date)
___________ (Application No.)	___________ (Filing Date)

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or under § 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information that is material to patentability as defined in 37 C.F.R. § 1.56 that became available between the filing date of the prior application and the national or PCT international filing date of this application.

09/525,615 (Application No.)	March 14, 2000 (Filing Date)	Pending (Status - patented, pending, abandoned)
09/526,041 (Application No.)	March 14, 2000 (Filing Date)	Pending (Status - patented, pending, abandoned)

Send Correspondence to:

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 New York Avenue, N.W.
Suite 600
Washington, D.C. 20005-3934

Direct Telephone Calls to:

(202) 371-2600

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor David F. Sorrells	
Signature of sole or first inventor David F. Sorrells	Date 10/05/00
Residence Middleburg, Florida	
Citizenship U.S.A.	
Post Office Address 3129 Rideout Lane, Middleburg, Florida 32068	
Full name of second inventor Michael J. Bultman	
Signature of second inventor M J Bultman	5 Oct 00 Date
Residence Jacksonville, Florida	
Citizenship U.S.A.	
Post Office Address 2244 Aztec Drive West, Jacksonville, Florida 32246	

Full name of third inventor Robert W. Cook		
Signature of third inventor	Robert W Cook 10/5/00	Date
Residence Switzerland, Florida		
Citizenship U.S.A.		
Post Office Address 1432 Roberts Road, Switzerland, Florida 32259		

Full name of fourth inventor Richard C. Looke		
Signature of fourth inventor	R C Looke 10/7/00	Date
Residence Jacksonville, Florida		
Citizenship U.S.A.		
Post Office Address 3170 Ricky Drive, Jacksonville, Florida 32223		

Full name of fifth inventor Charley D. Moses, Jr.		
Signature of fifth inventor	Charley D. Moses 10/05/00	Date
Residence Jacksonville, Florida		
Citizenship U.S.A.		
Post Office Address 4314 Naranja Drive, Jacksonville, Florida 32217		

Appl. No. 09/632,856
Docket No.1744.0630003/MQL/JTH

Full name of sixth inventor Gregory S. Rawlins	10/6/00
Signature of sixth inventor	Date
Residence Lake Mary, Florida	
Citizenship U.S.A.	
Post Office Address 299 Leslie Lane, Lake Mary, Florida 32746	

Full name of seventh inventor Michael W. Rawlins	
Signature of seventh inventor	Date 10/5/00
Residence Lake Mary, Florida	
Citizenship U.S.A.	
Post Office Address 665 Brightview Drive, Lake Mary, Florida 32746	

F:\USERS\SWILLIAMS\JTH Folder (New)\1744.0630003\dec.cwly

(Supply similar information and signature for subsequent joint inventors, if any)

OIPE JC100 NOV 2 0 2000 PATENT & TRADEMARK OFFICE

POWER OF ATTORNEY FROM ASSIGNEE

ParkerVision, Inc. , a corporation of Jacksonville, FL, having a principal place of business at 8493 Baymeadows Way, Jacksonville, FL 32256 , is assignee of the entire right, title and interest for the United States of America (as defined in 35 U.S.C. § 100), by reason of an Assignment to the Assignee executed on (1) 10-5-00 , (2) 10-5-00 , (3) 10-5-00, (4) 10-9-00 , (5) 10-5-00 , (6) 10-6-00 , (7) 10-5-00 , of an invention known as Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations (Attorney Docket No. 1744.0630003/MQL/JTH), which is disclosed and claimed in a patent application of the same title by the inventors (1) David F. Sorrells,(2) Michael J. Bultman, (3) Robert W. Cook, (4) Richard C. Looke, (5) Charley D. Moses, Jr., (6) Gregory S. Rawlins, (7) Michael W. Rawlins, (said application filed on August 4, 2000 at the U.S. Patent and Trademark Office, having Application Number 09/632,856).

The Assignee hereby appoints the following U.S. attorneys to prosecute this application and any continuation, divisional, continuation-in-part, or reissue application thereof, and to transact all business in the U.S. Patent and Trademark Office connected therewith: Robert Greene Sterne, Esq., Reg. No. 28,912; Edward J. Kessler, Esq., Reg. No. 25,688; Jorge A. Goldstein, Esq., Reg. No. 29,021; Samuel L. Fox, Esq., Reg. No. 30,353; David K.S. Cornwell, Esq., Reg. No. 31,944; Robert W. Esmond, Esq., Reg. No. 32,893; Tracy-Gene G. Durkin, Esq., Reg. No. 32,831; Michele A. Cimbala, Esq., Reg. No. 33,851; Michael B. Ray, Esq., Reg. No. 33,997; Robert E. Sokohl, Esq., Reg. No. 36,013; Eric K. Steffe, Esq., Reg. No. 36,688, Michael Q. Lee, Esq., Reg. No. 35,239; Steven R. Ludwig, Esq., Reg. No. 36,203; John M. Covert, Esq., Reg. No. 38,759; and Linda E. Alcorn, Esq., Reg. No. 39,588. The Assignee hereby grants said attorneys the power to insert on this Power of Attorney any further identification that may be necessary or desirable in order to comply with the rules of the U.S. Patent and Trademark Office.

Send correspondence to:

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 New York Avenue, N.W.
Suite 600
Washington, D.C. 20005-3934
U.S.A.

Direct phone calls to 202-371-2600.

FOR: ParkerVision, Inc.

SIGNATURE: [signature]

BY: Jeffrey L. Parker

TITLE: Chairman and Chief Executive Officer

DATE: 10-12-00

P:\USERS\SWILLIAM\JTH Folder (New)\1744.0630003\poa

Certificate Under 37 C.F.R. § 3.73(b)

Applicant: Sorrells *et al.*

Application No.: 09/632,856 Filed/Issue Date: August 4, 2000

Entitled: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations

ParkerVision, Inc., a corporation,
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency,etc.)

states that it is:

1. [X] the assignee of the entire right, title, and interest, or

2. [ ] an assignee of an undivided part interest

in the patent application/patent identified above by virtue of either:

A. [X] An Assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the Patent and Trademark Office at Reel _____, Frame ____, or for which a copy thereof is attached.

OR

B. [ ] A chain of title from the inventor(s) of the patent application/patent identified above to the current assignee as shown below:

1. From: ____________________ To: ________________________
The document was recorded in the Patent and Trademark Office at
Reel _________, Frame _________, or for which a copy thereof is attached.

2. From: ____________________ To: ________________________
The document was recorded in the Patent and Trademark Office at
Reel _________, Frame _________, or for which a copy thereof is attached.

3. From: ____________________ To: ________________________
The document was recorded in the Patent and Trademark Office at
Reel _________, Frame _________, or for which a copy thereof is attached.

[ ] Additional documents in the chain of title are listed on a supplemental sheet.

[X] Copies of assignments or other documents in the chain of title are attached.
[**NOTE:** A separate copy (*i.e.*, the original assignment document or a true copy of the original document) must be submitted to Assignment Division in accordance with 37 CFR Part 3, if the assignment is to be recorded in the records of the PTO. See MPEP 302-302.8]

The undersigned (whose title is supplied below) is empowered to act on behalf of the assignee.

Date: 10-12-00

Name: Jeffrey L. Parker

Title: Chairman and Chief Executive Officer

Signature:

P:\USERS\SWILLIAM\JTH Folder (New)\1744.0630003\cert 3
SKGF Rev.3/31/00 mac

ASSIGNMENT

In consideration of the sum of One Dollar ($1.00) or equivalent and other good and valuable consideration paid to each of the undersigned inventors: **(1) David F. Sorrells, (2) Michael J. Bultman, (3) Robert W. Cook, (4) Richard C. Looke, (5) Charley D. Moses, Jr., (6) Gregory S. Rawlins, (7) Michael W. Rawlins,** the undersigned inventor(s) hereby sell(s) and assigns to **ParkerVision, Inc.** (the Assignee) his/her entire right, title and interest, including the right to sue for past infringement and to collect for all past, present and future damages:

check applicable box(es) ⊠ for the United States of America (as defined in 35 U.S.C. § 100),
⊠ and throughout the world,

(a) in the invention known as **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations** for which application for patent in the United States of America has been executed by the undersigned on (1) 10-5-00, (2) 10-5-00, (3) 10-5-00, (4) 10-4-00, (5) 10-5-00, (6) 10-6-00 (7) 10-5-00 (also known as United States Application No. **09/632,856**, filed **August 4, 2000,** in any and all applications thereon, in any and all Letters Patent(s) therefor, and

(b) in any and all applications that claim the benefit of the patent application listed above in part (a), including continuing applications, reissues, extensions, renewals and reexaminations of the patent application or Letters Patent therefor listed above in part (a), to the full extent of the term or terms for which Letters Patents issue, and

(c) in any and all inventions described in the patent application listed above in part (a), and in any and all forms of intellectual and industrial property protection derivable from such patent application, and that are derivable from any and all continuing applications, reissues, extensions, renewals and reexaminations of such patent application, including, without limitation, patents, applications, utility models, inventor's certificates, and designs together with the right to file applications therefor; and including the right to claim the same priority rights from any previously filed applications under the International Agreement for the Protection of Industrial Property, or any other international agreement, or the domestic laws of the country in which any such application is filed, as may be applicable;

all such rights, title and interest to be held and enjoyed by the above-named Assignee, its successors, legal representatives and assigns to the same extent as all such rights, title and interest would have been held and enjoyed by the Assignor had this assignment and sale not been made.

The undersigned inventor(s) agree(s) to execute all papers necessary in connection with the application(s) and any continuing (continuation, divisional, or continuation-in-part), reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such application(s) as the Assignee may deem necessary or expedient.

The undersigned inventor(s) agree(s) to execute all papers necessary in connection with any interference or patent enforcement action (judicial or otherwise) related to the application(s) or any continuing (continuation, divisional, or continuation-in-part), reissue or reexamination application(s) thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such interference or patent enforcement action.

The undersigned inventor(s) hereby represent(s) that he/she has full right to convey the entire interest herein assigned, and that he/she has not executed, and will not execute, any agreement in conflict therewith.

The undersigned inventor(s) hereby grant(s) Robert Greene Sterne, Esquire, Registration No. 28,912; Edward J. Kessler, Esquire, Registration No. 25,688; Jorge A. Goldstein, Esquire, Registration No. 29,021; Samuel L. Fox, Esquire, Registration No. 30,353; David K.S. Cornwell, Esquire, Registration No. 31,944; Robert W. Esmond, Esquire, Registration No. 32,893; Tracy-Gene G. Durkin, Esquire, Registration No. 32,831; Michele A. Cimbala, Esquire, Registration No. 33,851; Michael B. Ray, Esquire, Registration No. 33,997; Robert E. Sokohl, Esquire, Registration No. 36,013; Eric K. Steffe, Esquire, Registration No. 36,688; Michael Q. Lee, Esquire, Registration No. 35,239; Steven R. Ludwig, Esquire, Registration No. 36,203; John M. Covert, Esquire, Registration No. 38,759; and Linda E. Alcorn, Esquire, Registration No. 39,588; all of STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C., 1100 New York Avenue, N.W., Suite 600, Washington, D.C. 20005-3934, power to insert in this assignment any further identification that may be necessary or desirable in order to comply with the rules of the United States Patent and Trademark Office for recordation of this document.

IN WITNESS WHEREOF, executed by the undersigned inventor(s) on the date opposite his/her name.

Date: 10/05/00 Signature of Inventor: David F. Sorrells
David F. Sorrells

Date: 5 Oct 00 Signature of Inventor: M J Bultman
Michael J. Bultman

Date: 10/05/00 Signature of Inventor: Robert W Cook
Robert W. Cook

Date: 10/9/00 Signature of Inventor: R C Looke
Richard C. Looke

Date: 10/05/00 Signature of Inventor: Charley D. Moses
Charley D. Moses, Jr.

Date: ____________ Signature of Inventor: ____________
Gregory S. Rawlins

Date: ____________ Signature of Inventor: ____________
Michael W. Rawlins

DO NOT FORWARD TO ASSIGNMENT BRANCH NOT FOR RECORDATION

The undersigned inventor(s) hereby grant(s) Robert Greene Sterne, Esquire, Registration No. 28,912; Edward J. Kessler, Esquire, Registration No. 25,688; Jorge A. Goldstein, Esquire, Registration No. 29,021; Samuel L. Fox, Esquire, Registration No. 30,353; David K.S. Cornwell, Esquire, Registration No. 31,944; Robert W. Esmond, Esquire, Registration No. 32,893; Tracy-Gene G. Durkin, Esquire, Registration No. 32,831; Michele A. Cimbala, Esquire, Registration No. 33,851; Michael B. Ray, Esquire, Registration No. 33,997; Robert E. Sokohl, Esquire, Registration No. 36,013; Eric K. Steffe, Esquire, Registration No. 36,688; Michael Q. Lee, Esquire, Registration No. 35,239; Steven R. Ludwig, Esquire, Registration No. 36,203; John M. Covert, Esquire, Registration No. 38,759; and Linda E. Alcorn, Esquire, Registration No. 39,588; all of STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C., 1100 New York Avenue, N.W., Suite 600, Washington, D.C. 20005-3934, power to insert in this assignment any further identification that may be necessary or desirable in order to comply with the rules of the United States Patent and Trademark Office for recordation of this document.

IN WITNESS WHEREOF, executed by the undersigned inventor(s) on the date opposite his/her name.

Date: ____________ Signature of Inventor: ____________
David F. Sorrells

Date: ____________ Signature of Inventor: ____________
Michael J. Bultman

Date: ____________ Signature of Inventor: ____________
Robert W. Cook

Date: ____________ Signature of Inventor: ____________
Richard C. Looke

Date: ____________ Signature of Inventor: ____________
Charley D. Moses, Jr.

Date: 10/6/00 Signature of Inventor: [signature]
Gregory S. Rawlins

Date: 10/5/00 Signature of Inventor: [signature]
Michael W. Rawlins

DO NOT FORWARD TO ASSIGNMENT BRANCH NOT FOR RECORDATION

D. J
#4 4-4-01
CF

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
ATTORNEYS AT LAW
1100 NEW YORK AVENUE, N.W., SUITE 600
WASHINGTON, D.C. 20005-3934

www.skgf.com
PHONE: (202) 371-2600 FACSIMILE: (202) 371-2540

FILE COPY

January 8, 2001

WRITER'S DIRECT NUMBER:
(202) 371-2674
INTERNET ADDRESS:
MLEE@SKGF.COM

Commissioner for Patents
Washington, D.C. 20231

Attn: Office of Initial Patent Examination
Customer Service Center

Re: U.S. Utility Patent Application
Appl. No. 09/632,856; Filed: August 4, 2000
For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations**
Inventors: Sorrells *et al.*
Our Ref: 1744.0630003/MQL/JTH

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Request for Corrected Official Filing Receipt;

2. A photocopy of the Official Filing Receipt, with corrections indicated in "red ink"; and

3. Return postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

Commissioner for Patents
January 8, 2001
Page 2

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036. A duplicate copy of this letter is enclosed.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

JTH/slw
Enclosures

P:\USERS\SWILLIAM\JTH Folder (New)\1744.0630003\correct.ptoltr

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Sorrells *et al.*

Appl. No. 09/632,856

Filed: August 4, 2000

For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations**

OIPE
JAN 08 2001
JC98
PATENT & TRADEMARK OFFICE

Art Unit: 2745

Examiner: To be Assigned

Atty. Docket: 1744.0630003/MQL/JTH

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MAR 27 2001
Technology Center 2600

Request for Corrected Official Filing Receipt

Commissioner for Patents
Washington, D.C. 20231

Attn: Office of Initial Patent Examination
Customer Service Center

Sir:

Applicants hereby request that a corrected Official Filing Receipt be issued and sent to the undersigned representative. Specifically, the following corrections to the Official Filing Receipt are requested:

In the Continuing Data section, after "08/04/1999, " insert --, 09/525,615 03/14/2000, and 09/526,041 03/14/2000.--

In support of the above request, a photocopy of the instant Official Filing Receipt is enclosed with the corrections noted in red. It is requested that a corrected Official Filing Receipt be issued, and sent to the undersigned at the earliest possible time.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

Date: 1/8/01

1100 New York Avenue, N.W.
Suite 600
Washington, D.C. 20005-3934
(202) 371-2600

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UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
09/632,856	08/04/2000	2745	1200	1744.0630003	208	40	3

FILING RECEIPT

OC000000005609237

Sterne Kessler Goldstein & Fox P L L C
Suite 600 1100 New York Avenue N W
Washington, DC 20005-3934

Date Mailed: 12/11/2000

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Customer Service Center. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the PTO processes the reply to the Notice, the PTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

David F. Sorrells, Middleburg, FL ;
Michael J. Bultman, Jacksonville, FL ;
Robert W. Cook, Switzerland, FL ;
Richard C. Looke, Jacksonville, FL ;
Charley D. Moses JR., Jacksonville, FL ;
Gregory S. Rawlins, Lake Mary, FL ;
Michael W. Rawlins, Lake Mary, FL ;

DEC 28 2000

AA 12/28

Continuing Data as Claimed by Applicant

THIS APPLN CLAIMS BENEFIT OF 60/147,129 08/04/1999 and
09/525,615 03/14/2000 and
09/526,041 03/14/2000

ze 12/28

Foreign Applications

RECEIVED
MAR 27 2001
Technology

If Required, Foreign Filing License Granted 09/26/2000

Title

Wireless local area network (WLAN) using universal frequency translation technology including multi-phase embodiments and circuit implementations

RECEIVED
MAR 27 2001
Technology Center 2600

Preliminary Class

455

Data entry by : BURNS, ERIC **Team :** OIPE **Date:** 12/11/2000

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CRF 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 36 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Office of Export Administration, Department of Commerce (15 CFR 370.10 (j)); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

PLEASE NOTE the following information about the Filing Receipt:

- The articles such as "**a**," "**an**" and "**the**" are not included as the first words in the title of an application. They are considered to be unnecessary to the understanding of the title.
- The words "**new**," "**improved**," "**improvements in**" or "**relating to**" are not included as first words in the title of an application because a patent application, by nature, is a new idea or improvement.
- The title may be truncated if it consists of more than 600 characters (letters and spaces combined).
- The docket number allows a maximum of 25 characters.
- If your application was submitted under 37 CFR 1.10, your filing date should be the "date in" found on the Express Mail label. If there is a discrepancy, you should submit a request for a corrected Filing Receipt along with a copy of the Express Mail label showing the "date in."
- The title is recorded in sentence case.

Any corrections that may need to be done to your Filing Receipt should be directed to:

Assistant Commissioner for Patents
Office of Initial Patent Examination
Customer Service Center
Washington, DC 20231

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COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

Bib Data Sheet

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/632,856	08/04/2000 RULE	455	2745	1744.0630003

APPLICANTS

David F. Sorrells, Middleburg, FL ;
Michael J. Bultman, Jacksonville, FL ;
Robert W. Cook, Switzerland, FL ;
Richard C. Looke, Jacksonville, FL ;
Charley D. Moses JR., Jacksonville, FL ;
Gregory S. Rawlins, Lake Mary, FL ;
Michael W. Rawlins, Lake Mary, FL ;

** **CONTINUING DATA** *************************
THIS APPLN CLAIMS BENEFIT OF 60/147,129 08/04/1999
WHICH IS A CON OF 09/525,615 03/14/2000

** **FOREIGN APPLICATIONS** ********************

IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 09/26/2000

		STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
Foreign Priority claimed 35 USC 119 (a-d) conditions met Verified and Acknowledged	☐ yes ☐ no ☐ yes ☐ no ☐ Met after Allowance Examiner's Signature Initials	FL	208	40	3

ADDRESS

Sterne Kessler Goldstein & Fox P L L C
Suite 600 1100 New York Avenue N W
Washington ,DC 20005-3934

TITLE

Wireless local area network (WLAN) using universal frequency translation technology including multi-phase embodiments and circuit implementations

FILING FEE RECEIVED		
1200	FEES: Authority has been given in Paper No. ________ to charge/credit DEPOSIT ACCOUNT No. ________ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other ________ ☐ Credit

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
ATTORNEYS AT LAW
1100 NEW YORK AVENUE, N.W. • WASHINGTON, D.C. 20005-3934
PHONE: (202) 371-2600 • FACSIMILE: (202) 371-2540 • www.skgf.com

June 6, 2001

WRITER'S DIRECT NUMBER:
(202) 371-2674
INTERNET ADDRESS:
MLEE@SKGF.COM

Commissioner for Patents
Washington, D.C. 20231

Art Unit: 2634

Re: U.S. Utility Patent Application
Appl. No. 09/632,856; Filed: August 4, 2000
For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations**
Inventors: Sorrells *et al.*
Our Ref: 1744.0630003/MQL/JTH

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Preliminary Amendment; and

2. Return postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036. A duplicate copy of this letter is enclosed.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

JTH/slw
Enclosures

P:\USERS\SWILLIAM\JTH Folder (New)\1744.0630003\amend.ptoltr

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

OIPE JC177
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PATENT & TRADEMARK OFFICE

In re Application of:

Sorrells *et al.*

Appl. No.: 09/632,856

Filed: August 4, 2000

For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations**

Art Unit: 2634

Examiner: TBD

Atty Docket: 1744.0630003

RECEIVED
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Preliminary Amendment

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

Prior to Examination of the captioned application, Applicants submit the following Preliminary Amendment.

It is not believed that extensions of time or fees for net addition of claims are required, beyond those which may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, then such extensions of time are hereby petitioned under 37 CFR § 1.136(a), and any fees required therefore (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Kindly enter the following amendments:

In the Specification:

On page 1, lines 12-15, replace with the following:

This application claims the benefit of U.S. Provisional Application No.60/147,129, filed on August 4, 1999; and this application is a continuation-in-part of U.S. Application No. 09/525,615, filed on March 14, 2000; and this application is a continuation-in-part of U.S. Application No. 09/526,041, filed on March 14, 2000, all of which are incorporated herein by reference in their entireties.

a1

In the Claims:

Please cancel claims 4-5,10-12, 38, and 40.

Please amend claims 13, 32, and 39 as follows:

a2

13. (Once Amended) The apparatus of claim 7, wherein said first and said second universal frequency down-conversion modules each comprise a switch and a storage element.

a3

32. (Once Amended) A method of transmitting a baseband signal over a wireless LAN, comprising the steps of:

(1) spreading the baseband signal using a spreading code, resulting in a spread baseband signal; and

(2) differentially sampling the spread baseband signal according to a first control signal and a second control signal resulting in a plurality of harmonic images that are each representative of the baseband signal, wherein said first and second control signals have pulse widths.

a4

39. (Once Amended) In a wireless LAN device, a method of down-converting a received RF signal, comprising the steps of:

down-converting said received RF signal according to a first control signal and a second control signal, resulting in a down-converted signal, wherein said second control signal is delayed relative to said first control signal by .5 + n cycles of said received RF signal, wherein n may be any integer greater than or equal to 1;

a4

de-spreading said down-converted signal using a spreading code, resulting in a de-spread signal; and

de-modulating said de-spread signal, resulting in a de-modulated signal;

wherein said first and said second control signals each comprise a train of pulses having pulse widths.

Remarks

Claims 1-3, 6-9, 13-37, and 39 are pending in this application. By the foregoing amendment, Applicants seek to cancel claims 4-5, 10-12, 38, and 40, and amend claims 13, 32, and 39. Furthermore, the specification has been amended to correct the priority claim. These changes are believed to be fully supported by the specification and are not believed to introduce new matter. Thus, it is respectfully requested that the amendments be entered by the Examiner. The Examiner is invited to telephone the undersigned representative if it is believe that an interview might be useful for any reason.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicant
Registration No. 35,239

Date: 6/4/01

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

P103-74.wpd

Version with markings to show changes made

In the Specification:

Page 1, lines 12-15:

This application claims the benefit of [the following:] U.S. Provisional Application No.60/147,129, filed on August 4, 1999; and this application is a continuation-in-part of U.S. Application No. 09/525,615, filed on March 14, 2000; and this application is a continuation-in-part of U.S. Application No. 09/526,041, filed on March 14, 2000, all of which are incorporated herein by reference in their entireties.

In the Claims:

13. (Once Amended) The apparatus of claim [10] 7, wherein said first and said second universal frequency down-conversion modules each comprise a switch and a storage element.

32. (Once Amended) A method of transmitting a baseband signal over a wireless LAN, comprising the steps of:

(1) spreading the baseband signal using a spreading code, resulting in a spread baseband signal; and

(2) differentially sampling the spread baseband signal according to a first control signal and a second control signal resulting in a plurality of harmonic images that are each representative of the baseband signal, wherein said first and second control signals have pulse widths [that improve energy transfer to a desired harmonic image of said plurality of harmonics].

39. In a wireless LAN device, a method of down-converting a received RF signal, comprising the steps of:

down-converting said received RF signal according to a first control signal and a second control signal, resulting in a down-converted signal, wherein said second control signal is delayed relative to said first control signal by .5 + n cycles of said received RF signal, wherein n may be any integer greater than or equal to 1;

de-spreading said down-converted signal using a spreading code, resulting in a de-spread signal; and

de-modulating said de-spread signal, resulting in a de-modulated signal;

wherein said first and said second control signals each comprise a train of pulses having pulse widths [that are established to improve energy transfer from said received RF signal to said down-converted signal].

Claims 4-5,10-12, 38, and 40 have been canceled.

8/B
RS
6-11-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
David F. SORRELLS *et al.*
Appl. No. 09/632,856
Filed: August 4, 2000
For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations**

Confirmation No.: 2377
Art Unit: 2634
Examiner: Chin, Stephen
Atty. Docket: 1744.0630004

Second Preliminary Amendment Under 37 C.F.R. § 1.115 in the Revised Format of the Pre-OG Notice Dated January 31, 2003

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

In advance of prosecution, Applicants submit the following amendments and remarks. This Second Preliminary Amendment is provided in the format approved in the pre-OG Notice dated January 31, 2003, entitled, "Amendments In A Revised Format Now Permitted," and in the following format:

(A) Each section begins on a separate sheet;

(B) Starting on a separate sheet, amendments to the specification by presenting replacement paragraphs marked up to show changes made;

(C) Starting on a separate sheet, a complete listing of all of the claims:

- in ascending order;
- with status identifiers; and
- with markings in the currently amended claims;

(D) Starting on a separate sheet, the Remarks.

It is not believed that extensions of time or fees for net addition of claims are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Amendments to the Claims

Please cancel claims 1-3, 6-9, 13-37 and 39.

Please add the following new claims:

B1

41. A wireless modem apparatus, comprising:

a balanced receiver for frequency down-converting an input signal including,

a first frequency down-conversion module to down-convert the input signal, wherein said first frequency down-conversion module down-converts said input signal according to a first control signal and outputs a first down-converted signal;

a second frequency down-conversion module to down-convert said input signal, wherein said second frequency down-conversion module down-converts said input signal according to a second control signal and outputs a second down-converted signal; and

a subtractor module that subtracts said second down-converted signal from said first down-converted signal and outputs a down-converted signal.

42. The apparatus of claim 41, wherein said second control signal is delayed relative to said first control signal by (.5 + n) cycles of said input signal, wherein n is an integer greater than or equal to 1.

43. The apparatus of claim 41, wherein said first frequency down-conversion module under-samples said input signal according to said first control signal, and said

second frequency down-conversion module under-samples said input signal according to said second control signal.

B1

44. The apparatus of claim 41, wherein said first and said second frequency down-conversion modules each comprise a switch and a storage element.

45. The apparatus of claim 44, wherein said storage elements comprises a capacitor that reduces a DC offset voltage in said first down-converted signal and said second down-converted signal.

46. The apparatus of claim 41, wherein said subtractor module comprises a differential amplifier.

CONT

47. The apparatus of claim 41, further comprising:

a balanced transmitter for up-converting a baseband signal and coupled to said balanced receiver, including,

an inverter, to receive said baseband signal and generate an inverted baseband signal;

a first controlled switch, coupled to a non-inverting output of said inverter, said first controlled switch to sample said baseband signal according to a third control signal, resulting in a first harmonically rich signal;

a second controlled switch, coupled to an inverting output of said inverter, said second controlled switch to sample said inverted baseband signal according to a fourth control signal, resulting in a second harmonically rich signal; and

B1

a combiner, coupled to an output of said first controlled switch and an output of said second controlled switch, said combiner to combine said first harmonically rich signal and said second harmonically rich signal, resulting in a third harmonically rich signal.

48. The apparatus of claim 47, wherein said fourth control signal is phase shifted with respect to said third control signal.

CONT

49. The apparatus of claim 47, wherein said fourth control signal is phase shifted by 180 degrees with respect to said third control signal.

50. The apparatus of claim 47, further comprising a filter coupled to an output of said combiner, wherein said filter outputs a desired harmonic from said third harmonically rich signal.

51. The apparatus of claim 47, wherein said apparatus is an infrastructure device.

52. The apparatus of claim 47, wherein said apparatus is a client device.

53. The apparatus of claim 47, wherein said third controlled switch shunts said baseband signal to a reference potential according to said first control signal, and wherein

said fourth controlled switch shunts said inverted baseband signal to said reference potential according to said second control signal.

54. The apparatus of claim 47, further comprising an antenna coupled to said balanced transmitter and said balanced receiver.

B1

55. The apparatus of claim 54, further comprising a switch, said switch selectively connecting said transmitter or said receiver to said antenna.

56. The apparatus of claim 47, further comprising a baseband processor coupled to said transmitter and said receiver.

CONT

57. The apparatus of claim 47, further comprising a media access controller (MAC) coupled to said transmitter and said receiver.

58. The apparatus of claim 57, wherein said MAC comprises a means for controlling accessing to a WLAN medium.

59. The apparatus of claim 58, wherein said means for controlling includes carrier sense multiple access with collision avoidance (CSMA/CA).

60. The apparatus of claim 47, further comprising a demodulator/modulator facilitation module coupled to said transmitter and receiver.

61. The apparatus of claim 60, wherein said demodulator/modulator facilitation module comprises a means for modulating said baseband signal using differential binary phase shift keying (DBPSK).

B1

62. The apparatus of claim 60, wherein said demodulator/modulator facilitation module comprises a means for de-modulating said down-converted signal using differential binary phase shift keying (DBPSK).

63. The apparatus of claim 60, wherein said demodulator/modulator facilitation module comprises a means for spreading said baseband signal.

CONT

64. The apparatus of claim 63, wherein said means for spreading comprises a means for spreading said baseband signal using a Barker code.

65. The apparatus of claim 60, wherein said demodulator/modulator facilitation module comprises a means for de-spreading said down-converted signal.

66. The apparatus of claim 65, wherein said means for de-spreading comprises a means for de-spreading said down-converted signal using a Barker code.

67. The apparatus of claim 60, wherein said demodulator/modulator facilitation module comprises a means for modulating said baseband signal using Gaussian phase shift keying (GFSK).

68. The apparatus of claim 60, wherein said demodulator/modulator facilitation module comprises a means for de-modulating said down converted signal using Gaussian phase shift keying (GFSK).

B1

69. The apparatus of claim 60, wherein said demodulator/modulator facilitation module comprises a means for modulating said baseband signal using Orthogonal Frequency Division Multiplexing (OFDM).

70. The apparatus of claim 60, wherein said demodulator/modulator facilitation module comprises a means for de-modulating said down converted signal using Orthogonal Frequency Division Multiplexing (OFDM).

CONT

71. The apparatus of claim 60, wherein said demodulator/modulator facilitation module comprises a means for modulating said baseband signal using Complimentary Code Keying (CCK).

72. The apparatus of claim 60, wherein said demodulator/modulator facilitation module comprises a means for de-modulating said down converted signal using Complimentary Code Keying (CCK).

73. A method of receiving a wireless LAN signal, comprising:

(1) splitting the wireless LAN signal into I and Q components;

(2) down-converting said I signal component and said Q signal component;

(3) de-spreading said down-converted I and Q signals using a spreading code;

B1

(4) differentially demodulating information encoded in said I and Q signals;

(5) sending said demodulated information in said I and Q signals to a Media Access Controller (MAC) Interface wherein said I and Q signals are de-scrambled and combined to a single output signal.

CONT

74. The method of claim 73, wherein separate spreading codes are used for the I and Q signal components in step (3).

75. The method of claim 73, wherein step (4) comprises using Binary Phase Shift Keying (BPSK) to demodulate said I and Q signals.

76. The method of claim 73, wherein step (4) comprises using Quadrature Phase Shift Keying (QPSK) to demodulate said I and Q signals.

77. In a wireless LAN device, a method of down-converting a received RF signal, comprising:

down-converting said received RF signal according to a first control signal and a second control signal, resulting in a down-converted signal, wherein said second control

B1

signal is delayed relative to said first control signal by (.5 + n) cycles of said received RF signal, wherein n is an integer greater than or equal to 1;

de-spreading said down-converted signal using a spreading code, resulting in a de-spread signal; and

CONT

de-modulating said de-spread signal, resulting in a de-modulated signal.

Remarks

Upon entry of the foregoing amendment, claims 41-77 are pending in the application, with 41, 73 and 77 being the independent claims. Claims 1-3, 6-9, 13-37 and 39 are sought to be cancelled without prejudice to or disclaimer of the subject matter therein. New claims 41-77 are sought to be added. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Conclusion

Prompt and favorable consideration of this Preliminary Amendment is respectfully requested. Applicants believe the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

Date: June 9, 2003

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/632,856	08/04/2000	David F. Sorrells	1744.0630003	2377

7590 12/01/2003

Sterne Kessler Goldstein & Fox P L L C
Suite 600 1100 New York Avenue N W
Washington, DC 20005-3934

EXAMINER	
KIM, KEVIN	

ART UNIT	PAPER NUMBER
2634	9

DATE MAILED: 12/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)
	09/632,856	SORRELLS ET AL.
	Examiner	Art Unit
	Kevin Y Kim	2634

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 04 August 2000.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 41-77 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) 41-77 are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.

4) ☐ Interview Summary (PTO-413) Paper No(s). _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 41-72, 77, drawn to a wireless modem , classified in class 455, subclass 313.

   II. Claim 73-76, drawn to a spread spectrum demodulation, classified in class 375, subclass 147.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions I and II are unrelated. Inventions are unrelated if it can be shown that they are not disclosed as capable of use together and they have different modes of operation, different functions, or different effects (MPEP § 806.04, MPEP § 808.01). In the instant case the different inventions. The wireless mode comprising frequency downconverters is not discloses as capable of use together with the spread spectrum demodulator. The two inventions operate differently since the former use (parallel) frequency down converters and the latter employs a dispreading operation.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. A telephone call was made to Mr. Michael Lee on November 5, 2003 to request an oral election to the above restriction requirement, but did not result in an election being made.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Y Kim whose telephone number is 703-305-4082. The examiner can normally be reached on 8AM --5PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

kvk

STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

PE DEC 3 0 2003 JC22 PATENT & TRADEMARK OFFICE

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Election 1.904

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
Sorrells *et al.*

Appl. No. 09/632,856

Filed: August 4, 2000

For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementation

Confirmation No. 2377

Art Unit: 2634

Examiner: Kevin Kim

Atty. Docket: 1744.0630003

Reply To Restriction Requirement

Commissioner for Patents
Washington, D.C. 20231

Sir:

In reply to the Office Action mailed December 1, 2003, requesting an election of a single disclosed invention for prosecution in the above-referenced patent application, Applicants hereby submit the following Reply to the Restriction Requirement.

Applicants elect to prosecute **Invention I**, represented by **claims 41-72, and 77**. This election is made without prejudice to, or disclaimer of, the other claims, species or inventions disclosed. Applicants respectfully request reconsideration and withdrawal of the Restriction Requirement, and consideration of all the pending claims.

It is not believed that extensions of time or fees for net addition of claims are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefore (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 19-0036.

If the Examiner believes, for any reason, that a personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

Date: 12/30/03

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2634

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December 30, 2003

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Art Unit 2634

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Re: U.S. Utility Patent Application
Application No. 09/632,856; Filed: August 4, 2000
For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementation**
Inventors: Sorrells *et al.*
Our Ref: 1744.0630003

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Reply to Restriction Requirement; and
2. Return postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

MQL/JTH/agj
SKGF\DC1\214271.1

L Number	Hits	Search Text	DB	Time stamp
-	32346	subtractor	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/03/11 12:03
-	37	"differental amplifier"	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/03/11 12:04
-	67405	"differential amplifier"	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/03/11 12:04
-	282	subtractor with "differential amplifier"	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/03/11 12:04
-	137	subtractor near3 "differential amplifier"	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/03/11 12:04

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/632,856	08/04/2000	David F. Sorrells	1744.0630003	2377

7590 03/30/2004

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Suite 600 1100 New York Avenue N W
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EXAMINER	
KIM, KEVIN	
ART UNIT	**PAPER NUMBER**
2634	

DATE MAILED: 03/30/2004

11

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)
	09/632,856	SORRELLS ET AL.
	Examiner	**Art Unit**
	Kevin Y Kim	2634

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *41-77* is/are pending in the application.

4a) Of the above claim(s) *73-76* is/are withdrawn from consideration.

5)☒ Claim(s) *77* is/are allowed.

6)☒ Claim(s) *41 and 46* is/are rejected.

7)☒ Claim(s) *42-45,47-72* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I in Paper No. 10 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 41 is rejected under 35 U.S.C. 102(e) as being anticipated by Sanielevici et al (US 6,018,553).

Referring to Fig.2, Sanielevici et al discloses a balanced receiver, comprising

"a first frequency down-conversion module" (201) for down-converting an input signal according to a first control signal (5KHz, 0DEG),

"a second frequency down-conversion module" (204) for down-converting the input signal according to a second control signal (5KHz, -90 DEG) and

"a subtractor module" (213) that subtracts the down-converted signal of the " second frequency down-conversion module" (204) from the down-converted signal of the "first frequency down-conversion module" (201).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claim 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sanielevici et al (US 6,018,553) in view of Nash (US 6,317,589).

Sanielevici et al disclose all the subject matter claimed except for the subtractor being a differential amplifier. Nash teaches that a subtractor is typically a differential amplifier. Col.4, lines 45-46. Thus, it would have been obvious to one skilled in the art at the time the invention was made to implement the function unit of the subtractor (213) with a differential amplifier as taught by Nash.

Allowable Subject Matter

7. Claims 42-45, 47-72 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claim 77 is allowed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Y Kim whose telephone number is 703-305-4082. The examiner can normally be reached on 8AM --5PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

kvk

STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Notice of References Cited	Application/Control No. 09/632,856	Applicant(s)/Patent Under Reexamination SORRELLS ET AL.	
	Examiner Kevin Y Kim	Art Unit 2634	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,018,553	01-2000	Sanielevici et al.	375/334
	B	US-6,317,589	11-2001	Nash, Adrian Philip	455/245.2
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 2377
Sorrells *et al.*	Art Unit: 2634
Appl. No.: 09/632,856	Examiner: Kim, Kevin
Filed: August 4, 2000	Atty. Docket: 1744.0630003
For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementation**	

Amendment and Reply Under 37 C.F.R. § 1.111

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the Office Action dated March 30, 2004, Applicants submit the following Amendment and Remarks. This Amendment is provided in the following format:

(A) Each section begins on a separate sheet;

(B) Starting on a separate sheet, a complete listing of all of the claims:

- in ascending order;
- with status identifiers; and
- with markings in the currently amended claims;

(C) Starting on a separate sheet, the Remarks.

It is not believed that extensions of time or fees for net addition of claims are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefore (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

1 - 41. (canceled).

42. (currently amended) A wireless modem apparatus, comprising:

a receiver for frequency down-converting an input signal including,

a first frequency down-conversion module to down-convert the input signal, wherein said first frequency down-conversion module down-converts said input signal according to a first control signal and outputs a first down-converted signal;

a second frequency down-conversion module to down-convert said input signal, wherein said second frequency down-conversion module down-converts said input signal according to a second control signal and outputs a second down-converted signal; and

a subtractor module that subtracts said second down-converted signal from said first down-converted signal and outputs a down-converted signal;

~~The apparatus of claim 41,~~ wherein said second control signal is delayed relative to said first control signal by (.5 + n) cycles of said input signal, wherein n is an integer greater than or equal to 1.

43. (currently amended) A wireless modem apparatus, comprising:

a receiver for frequency down-converting an input signal including, a first frequency down-conversion module to down-convert the input signal, wherein said first frequency down-conversion module down-converts said input signal according to a first control signal and outputs a first down-converted signal;

a second frequency down-conversion module to down-convert said input signal, wherein said second frequency down-conversion module down-converts said input signal according to a second control signal and outputs a second down-converted signal; and

a subtractor module that subtracts said second down-converted signal from said first down-converted signal and outputs a down-converted signal;

~~The apparatus of claim 41,~~ wherein said first frequency down-conversion module under-samples said input signal according to said first control signal, and said second frequency down-conversion module under-samples said input signal according to said second control signal.

44. (currently amended) A wireless modem apparatus, comprising:

a receiver for frequency down-converting an input signal including,

a first frequency down-conversion module to down-convert the input signal, wherein said first frequency down-conversion module down-converts said input signal according to a first control signal and outputs a first down-converted signal;

a second frequency down-conversion module to down-convert said input signal, wherein said second frequency down-conversion module down-converts said input signal according to a second control signal and outputs a second down-converted signal; and a subtractor module that subtracts said second down-converted signal from said first down-converted signal and outputs a down-converted signal;

~~The apparatus of claim 41,~~ wherein said first and said second frequency down-conversion modules each comprise a switch and a storage element.

45. (previously presented) The apparatus of claim 44, wherein said storage elements comprises a capacitor that reduces a DC offset voltage in said first down-converted signal and said second down-converted signal.

46. (currently amended) The apparatus of claim 42 [[41]], wherein said subtractor module comprises a differential amplifier.

47. (currently amended) A wireless modem apparatus, comprising:

a receiver for frequency down-converting an input signal including,

a first frequency down-conversion module to down-convert the input signal, wherein said first frequency down-conversion module down-converts said input signal according to a first control signal and outputs a first down-converted signal;

a second frequency down-conversion module to down-convert said input signal, wherein said second frequency down-conversion module down-converts said input signal according to a second control signal and outputs a second down-converted signal;

a subtractor module that subtracts said second down-converted signal from said first down-converted signal and outputs a down-converted signal;

~~The apparatus of claim 41, further comprising:~~

a [balanced] transmitter for up-converting a baseband signal and coupled to said [balanced] receiver, including,

an inverter, to receive said baseband signal and generate an inverted baseband signal;

a first controlled switch, coupled to a non-inverting output of said inverter, said first controlled switch to sample said baseband signal according to a third control signal, resulting in a first harmonically rich signal;

a second controlled switch, coupled to an inverting output of said inverter, said second controlled switch to sample said inverted baseband signal according to a fourth control signal, resulting in a second harmonically rich signal; and

a combiner, coupled to an output of said first controlled switch and an output of said second controlled switch, said combiner to combine said first harmonically rich signal and said second harmonically rich signal, resulting in a third harmonically rich signal.

48. (previously presented) The apparatus of claim 47, wherein said fourth control signal is phase shifted with respect to said third control signal.

49. (previously presented) The apparatus of claim 47, wherein said fourth control signal is phase shifted by 180 degrees with respect to said third control signal.

50. (previously presented) The apparatus of claim 47, further comprising a filter coupled to an output of said combiner, wherein said filter outputs a desired harmonic from said third harmonically rich signal.

51. (previously presented) The apparatus of claim 47, wherein said apparatus is an infrastructure device.

52. (previously presented) The apparatus of claim 47, wherein said apparatus is a client device.

53. (currently amended) The apparatus of claim 47, wherein said ~~third~~ first controlled switch shunts said baseband signal to a reference potential according to said ~~first~~ third control signal, and wherein said ~~fourth~~ second controlled switch shunts said inverted baseband signal to said reference potential according to said ~~second~~ fourth control signal.

54. (previously presented) The apparatus of claim 47, further comprising an antenna coupled to said balanced transmitter and said balanced receiver.

55. (previously presented) The apparatus of claim 54, further comprising a switch, said switch selectively connecting said transmitter or said receiver to said antenna.

56. (previously presented) The apparatus of claim 47, further comprising a baseband processor coupled to said transmitter and said receiver.

57. (previously presented) The apparatus of claim 47, further comprising a media access controller (MAC) coupled to said transmitter and said receiver.

58. (previously presented) The apparatus of claim 57, wherein said MAC comprises a means for controlling accessing to a WLAN medium.

59. (previously presented) The apparatus of claim 58, wherein said means for controlling includes carrier sense multiple access with collision avoidance (CSMA/CA).

60. (previously presented) The apparatus of claim 47, further comprising a demodulator/modulator facilitation module coupled to said transmitter and receiver.

61. (previously presented) The apparatus of claim 60, wherein said demodulator/modulator facilitation module comprises a means for modulating said baseband signal using differential binary phase shift keying (DBPSK).

62. (previously presented) The apparatus of claim 60, wherein said demodulator/modulator facilitation module comprises a means for de-modulating said down-converted signal using differential binary phase shift keying (DBPSK).

63. (previously presented) The apparatus of claim 60, wherein said demodulator/modulator facilitation module comprises a means for spreading said baseband signal.

64. (previously presented) The apparatus of claim 63, wherein said means for spreading comprises a means for spreading said baseband signal using a Barker code.

65. (previously presented) The apparatus of claim 60, wherein said demodulator/modulator facilitation module comprises a means for de-spreading said down-converted signal.

66. (previously presented) The apparatus of claim 65, wherein said means for de-spreading comprises a means for de-spreading said down-converted signal using a Barker code.

67. (previously presented) The apparatus of claim 60, wherein said demodulator/modulator facilitation module comprises a means for modulating said baseband signal using Gaussian phase shift keying (GFSK).

68. (previously presented) The apparatus of claim 60, wherein said demodulator/modulator facilitation module comprises a means for de-modulating said down converted signal using Gaussian phase shift keying (GFSK).

69. (previously presented) The apparatus of claim 60, wherein said demodulator/modulator facilitation module comprises a means for modulating said baseband signal using Orthogonal Frequency Division Multiplexing (OFDM).

70. (previously presented) The apparatus of claim 60, wherein said demodulator/modulator facilitation module comprises a means for de-modulating said down converted signal using Orthogonal Frequency Division Multiplexing (OFDM).

71. (previously presented) The apparatus of claim 60, wherein said demodulator/modulator facilitation module comprises a means for modulating said baseband signal using Complimentary Code Keying (CCK).

72. (previously presented) The apparatus of claim 60, wherein said demodulator/modulator facilitation module comprises a means for de-modulating said down converted signal using Complimentary Code Keying (CCK).

73. (withdrawn) A method of receiving a wireless LAN signal, comprising:

(1) splitting the wireless LAN signal into I and Q components;

(2) down-converting said I signal component and said Q signal component;

(3) de-spreading said down-converted I and Q signals using a spreading code;

(4) differentially demodulating information encoded in said I and Q signals;

(5) sending said demodulated information in said I and Q signals to a Media Access Controller (MAC) Interface wherein said I and Q signals are de-scrambled and combined to a single output signal.

74. (withdrawn) The method of claim 73, wherein separate spreading codes are used for the I and Q signal components in step (3).

75. (withdrawn) The method of claim 73, wherein step (4) comprises using Binary Phase Shift Keying (BPSK) to demodulate said I and Q signals.

76. (withdrawn) The method of claim 73, wherein step (4) comprises using Quadrature Phase Shift Keying (QPSK) to demodulate said I and Q signals.

77. (previously presented) In a wireless LAN device, a method of down-converting a received RF signal, comprising:

down-converting said received RF signal according to a first control signal and a second control signal, resulting in a down-converted signal, wherein said second control signal is delayed relative to said first control signal by (.5 + n) cycles of said received RF signal, wherein n is an integer greater than or equal to 1;

de-spreading said down-converted signal using a spreading code, resulting in a de-spread signal; and

de-modulating said de-spread signal, resulting in a de-modulated signal.

Remarks

Upon entry of the foregoing amendment, claims 42-77 are pending in the application, with claims 42-44, 47, and 77 being the independent claims. Claims 73-76 have been previously withdrawn from consideration. By the foregoing amendment, claims 42-44 and 46-47, and 53 are currently amended, and claim 41 is canceled without prejudice to or disclaimer of the subject matter therein. These changes are believed to introduce no new matter, and their entry is respectfully requested. Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Rejections under 35 U.S.C. §§ 102 and 103

The Office Action indicates that claim 41 is rejected under 35 U.S.C. § 102(e) as being unpatentable over U.S. patent number 6,018,553 to Sanielevici (hereinafter "Sanielevici"). Further, the Office Action indicates that claim 46 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Sanielevici. Claims 42-45 and 47-72 are indicated to be allowable over the cited art if rewritten in independent form. Claim 77 is allowed.

Claims 42-44 and 47 have been re-written in independent form to include the features of claim 41. Claim 41 has been canceled. Independent claims 42, 43, 44 and 47 have been further amended to delete the word "balanced," to more distinctly claim the invention. Accordingly, independent claims 42-44 and 47 and their respective dependent claims are allowable over the cited art. Claim 46 has been amended to depend from claim 42. Therefore, Applicants request that the rejections under 35 U.S.C. §§ 102 and 103 be removed and that these claims be passed to allowance.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

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2634 # 41

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Judith U. Kim
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Patrick E. Garrett
Heidi L. Kraus
Edward W. Yee
Albert L. Ferro*
Donald R. Banowit
Peter A. Jackman
Teresa U. Medler
Jeffrey S. Weaver
Kendrick P. Patterson
Vincent L. Capuano
Eldora Ellison Floyd
Thomas C. Fiala
Brian J. Del Buono
Virgil Lee Beaston
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Joseph S. Ostroff
Frank R. Cottingham
Christine M. Lhulier
Rae Lynn Prengaman
Jane Shershenovich*
George S. Bardmesser
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Andrea J. Kamage
Tracy L. Muller*
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Ann E. Summerfield
Tiera S. Coston
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Jessica L. Parezo
Timothy A. Doyle*
Gaby L. Longsworth*
Nicole D. Dretar*
Ted J. Ebersole
Jyoti C. Iyer*

Registered Patent Agents•
Karen R. Markowicz
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Katrina Y. Pei Quach
Bryan L. Skelton
Robert A. Schwartzman
Teresa A. Colella
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Victoria S. Rutherford
Eric D. Hayes
Michelle K. Holoubek
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Simon J. Elliott
Julie A. Heider
Mita Mukherjee
Scott M. Woodhouse

Of Counsel
Kenneth C. Bass III
Evan R. Smith
Marvin C. Guthrie

*Admitted only in Maryland
*Admitted only in Virginia
•Practice Limited to Federal Agencies

OIPE JUL 2 7 2004 PATENT & TRADEMARK OFFICE

July 27, 2004

WRITER'S DIRECT NUMBER:
(202) 772-8674
INTERNET ADDRESS:
MLEE@SKGF.COM

RECEIVED
AUG 0 3 2004
Technology Center 2600

Art Unit 2634

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Re: U.S. Utility Patent Application
Appl. No. 09/632,856; Filed: August 4, 2000
For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementation**
Inventors: Sorrells *et al.*
Our Ref: 1744.0630003

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Fee Transmittal (Form PTO/SB/17);
2. Petition for Extension of Time Under 37 C.F.R. § 1.136(a)(1);
3. Amendment and Reply Under 37 C.F.R. § 1.111;
4. Return postcard; and
5. PTO-2038 Credit Card Payment Form for $282.00 to cover:
   $172.00 for additional claims fee; and
   $110.00 for extension of time fees.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

MQL/JTH/JP/agj
282300_1.DOC

OIPE JC60 JUL 2 7 2004 PATENT & TRADEMARK OFFICE

PTO/SB/17 (10-03)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 282.00

Complete if Known	
Application Number	09/632,856
Filing Date	August 4, 2000
First Named Inventor	David F. Sorrells
Examiner Name	Kim, Kevin
Art Unit	2634
Attorney Docket No.	1744.0630003

RECEIVED AUG 0 3 2004 Technology Center 2600

METHOD OF PAYMENT (check all that apply)

☐ Check ☒ Credit card ☐ Money Order ☒ Other** ☐ None

☐ Deposit Account: **Charge any deficiencies or credit any overpayments in the fees to Deposit Acct. No. 19-0036.*

Deposit Account Number: 19-0036

Deposit Account Name: Sterne, Kessler, Goldstein & Fox P.L.L.C.

The Director is authorized to: *(check all that apply)*

☐ Charge fee(s) indicated below ☐ Credit any overpayments

☐ Charge any additional fee(s) or any underpayment of fee(s)

☐ Charge fee(s) indicated below, **except for the filing fee**

to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 0.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims		Fee from below		Fee Paid
Total Claims	32	- 40 **=	0	X	$18.00	=	$0.00
Independent Claims	5	- 3 **=	2	X	$86.00	=	$172.00
Multiple Dependent					$290.00	=	$0.00

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 172.00

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	$110.00
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) ____________

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 110.00

SUBMITTED BY		(Complete *(if applicable)*)			
Name *(Print/Type)*	Michael Q. Lee	Registration No. *(Attorney/Agent)*	35,239	Telephone	(202) 371-2600
Signature				Date	

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.17 and 1.27. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 2377
Sorrells *et al.*	Art Unit: 2634
Appl. No.: 09/632,856	Examiner: Kim, Kevin
Filed: August 4, 2000	Atty. Docket: 1744.0630003
For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementation**	

Petition for Extension of Time Under 37 C.F.R. § 1.136(a)(1)

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

It is hereby requested that the period for replying to the outstanding Office Action be extended one (1) month from June 30, 2004 to July 30, 2004 by the filing of this Petition and fee payment.

The petition fee (37 C.F.R. § 1.17(a)) is believed to be $110.00 for a one (1) month for a large entity. Fee payment is provided in our accompanying PTO-2038 Credit Card Payment Form. However, if extensions of time under 37 C.F.R. § 1.136 other than those provided herewith are required to prevent abandonment of the present patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

Date: July 27, 2004

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600
MQL/JTH/JP/agj
288072_1.DOC

PATENT APPLICATION FEE DETERMINATION RECORD
Effective December 29, 1999

Application or Docket Number
09/632856

CLAIMS AS FILED - PART I

FOR	NUMBER FILED (Column 1)		NUMBER EXTRA (Column 2)	SMALL ENTITY TYPE RATE	FEE	OR	OTHER THAN SMALL ENTITY RATE	FEE
BASIC FEE					345.00	OR		690.00
TOTAL CLAIMS	40	minus 20=	* 20	X$ 9=		OR	X$18=	360
INDEPENDENT CLAIMS	3	minus 3 =	* /	X39=		OR	X78=	—
MULTIPLE DEPENDENT CLAIM PRESENT				+130=		OR	+260=	—
				TOTAL		OR	TOTAL	1050

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

AMENDMENT A

A	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	SMALL ENTITY RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	ADDITIONAL FEE
Total	* 33	Minus	** 40	=	X$ 9=		OR	X$18=	
Independent	* 3	Minus	*** 3	=	X39=		OR	X78=	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					+130=		OR	+260=	
					TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

B	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	SMALL ENTITY RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	ADDITIONAL FEE
Total	* 38	Minus	** 40	= /	X$ 9=		OR	X$18=	
Independent	* 3	Minus	*** 3	= /	X39=		OR	X78=	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					+130=		OR	+260=	
					TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	SMALL ENTITY RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	ADDITIONAL FEE
Total	* 38	Minus	** 40	= /	X$ 9=		OR	X$18=	
Independent	* 6	Minus	*** 3	= 3	X39=		OR	~~X78=~~ 86	258
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					+130=		OR	+260=	
					TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	258 pd

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20"
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

FORM PTO-875
(Rev. 12/99)

Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

7590 09/10/2004

Sterne Kessler Goldstein & Fox P L L C
Suite 600 1100 New York Avenue N W
Washington, DC 20005-3934

EXAMINER	
KIM, KEVIN	
ART UNIT	**PAPER NUMBER**
2634	

DATE MAILED: 09/10/2004

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/632,856	08/04/2000	David F. Sorrells	1744.0630003	2377

TITLE OF INVENTION: WIRELESS LOCAL AREA NETWORK (WLAN) USING UNIVERSAL FREQUENCY TRANSLATION TECHNOLOGY INCLUDING MULTI-PHASE EMBODIMENTS AND CIRCUIT IMPLEMENTATIONS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1330	$0	$1330	12/10/2004

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

or Fax **(703) 746-4000**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

7590 09/10/2004

Sterne Kessler Goldstein & Fox P L L C
Suite 600 1100 New York Avenue N W
Washington, DC 20005-3934

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (703) 746-4000, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/632,856	08/04/2000	David F. Sorrells	1744.0630003	2377

TITLE OF INVENTION: WIRELESS LOCAL AREA NETWORK (WLAN) USING UNIVERSAL FREQUENCY TRANSLATION TECHNOLOGY INCLUDING MULTI-PHASE EMBODIMENTS AND CIRCUIT IMPLEMENTATIONS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1330	$0	$1330	12/10/2004

EXAMINER	ART UNIT	CLASS-SUBCLASS
KIM, KEVIN	2634	375-222000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 ____________

2 ____________

3 ____________

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

☐ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies ____________

4b. Payment of Fee(s):

☐ A check in the amount of the fee(s) is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number ____________ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.
NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature ____________ Date ____________

Typed or printed name ____________ Registration No. ____________

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/632,856	08/04/2000	David F. Sorrells	1744.0630003	2377

7590 09/10/2004

Sterne Kessler Goldstein & Fox P L L C
Suite 600 1100 New York Avenue N W
Washington, DC 20005-3934

EXAMINER	
KIM, KEVIN	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 09/10/2004

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 737 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 737 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (703) 305-1383. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

PTOL-85 (Rev. 09/04) Approved for use through 04/30/2007.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/632,856	08/04/2000	David F. Sorrells	1744.0630003	2377

7590 09/10/2004

Sterne Kessler Goldstein & Fox P L L C
Suite 600 1100 New York Avenue N W
Washington, DC 20005-3934

EXAMINER	
KIM, KEVIN	
ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 09/10/2004

Notice of Fee Increase on October 1, 2004

If a reply to a "Notice of Allowance and Fee(s) Due" is filed in the Office on or after October 1, 2004, then the amount due will be higher than that set forth in the "Notice of Allowance and Fee(s) Due" because some fees will increase effective October 1, 2004. See Revision of Patent Fees for Fiscal Year 2005; Final Rule, 69 Fed. Reg. 52604, 52606 (May 10, 2004).

The current fee schedule is accessible from WEB site (http://www.uspto.gov/main/howtofees.htm).

If the fee paid is the amount shown on the "Notice of Allowance and Fee(s) Due" but not the correct amount in view of the fee increase, a "Notice of Pay Balance of Issue Fee" will be mailed to applicant. In order to avoid processing delays associated with mailing of a "Notice of Pay Balance of Issue Fee," if the response to the Notice of Allowance is to be filed on or after October 1, 2004 (or mailed with a certificate of mailing on or after October 1, 2004), the issue fee paid should be the fee that is required at the time the fee is paid. See Manual of Patent Examining Procedure (MPEP), Section 1306 (Eighth Edition, Rev. 2, May 2004). If the issue fee was previously paid, and the response to the "Notice of Allowance and Fee(s) Due" includes a request to apply a previously-paid issue fee to the issue fee now due, then the difference between the issue fee amount at the time the response is filed and the previously-paid issue fee should be paid. See MPEP Section 1308.01.

Effective October 1, 2004, 37 CFR 1.18 is amended by revising paragraphs (a) through (c) to read as set forth below.

Section 1.18 Patent post allowance (including issue) fees.

(a) Issue fee for issuing each original or reissue patent, except a design or plant patent:
By a small entity (Sec. 1.27(a))...................... $685.00
By other than a small entity......................... $1,370.00
(b) Issue fee for issuing a design patent:
By a small entity (Sec. 1.27(a))...................... $245.00
By other than a small entity........................... $490.00
(c) Issue fee for issuing a plant patent:
By a small entity (Sec. 1.27(a))...................... $330.00
By other than a small entity........................... $660.00

Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

Notice of Allowability	Application No.	Applicant(s)
	09/632,856	SORRELLS ET AL.
	Examiner	Art Unit
	Kevin Y Kim	2634

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to amendment filed on 07-27-2004.

2. ☒ The allowed claim(s) is/are 42-72,77 renumbered as 1-32.

3. ☒ The drawings filed on 08-04-2004 are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
   1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Jeffrey Helvey (Reg. # 44757) on September 7, 2004.

The application has been amended as follows:

In **claim 54**, on line 2, delete "balanced" before "transmitter" and delete "balanced" before "receiver"

In **claim 67**, on line 3, change "GFSK" to –GPSK—

In **claim 68**, on line 3, change "GFSK" to –GPSK—

Cancel **claims 73-76**.

End of Examiner's amendment.

2. This application is in condition for allowance except for the presence of claims 73-76 to an invention non-elected without traverse. Accordingly, claims 73-76 have been cancelled.

REASONS FOR ALLOWANCE

3. The following is an examiner's statement of reasons for allowance: No prior art has been found to disclose or suggest a frequency down converter that down converts a received input signal in accordance with two control signals that are delayed relative to each other by (.5 + n) cycles of the input signal, wherein n is an integer greater than or equal to 1.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Y Kim whose telephone number is 703-305-4082. The examiner can normally be reached on 8AM --5PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

kvk

Chieh M. Fan

CHIEH M. FAN
PRIMARY EXAMINER

Issue Classification	**Application No.** 09/632,856	**Applicant(s)** SORRELLS ET AL.	
	Examiner Kevin Y Kim	**Art Unit** 2634	

ISSUE CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)							
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)						
375	222	375	328						
INTERNATIONAL CLASSIFICATION		455	137						
H 0 4 L	5/16								
	/								
	/								
	/								
	/								

Kevin Kim 09/07/2004 (Assistant Examiner) (Date)	CHIEH M. FAN PRIMARY EXAMINER	Total Claims Allowed: 32
L. Mack 9.7.04 (Legal Instruments Examiner) (Date)	9/7/04 (Primary Examiner) (Date)	O.G. Print Claim(s): 1 — O.G. Print Fig.: 70Q

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		31		61		91		121		151		181
	2		32		62		92		122		152		182
	3		33		63		93		123		153		183
	4		34		64		94		124		154		184
	5		35		65		95		125		155		185
	6		36		66		96		126		156		186
	7		37		67		97		127		157		187
	8		38		68		98		128		158		188
	9		39		69		99		129		159		189
	10		40		70		100		130		160		190
	11		41		71		101		131		161		191
	12		42		72		102		132		162		192
	13		43		73		103		133		163		193
	14		44		74		104		134		164		194
	15		45		75		105		135		165		195
	16		46		76		106		136		166		196
	17		47		77		107		137		167		197
	18		48		78		108		138		168		198
	19		49		79		109		139		169		199
	20		50		80		110		140		170		200
	21		51		81		111		141		171		201
	22		52		82		112		142		172		202
	23		53		83		113		143		173		203
	24		54		84		114		144		174		204
	25		55		85		115		145		175		205
	26		56		86		116		146		176		206
	27		57		87		117		147		177		207
	28		58		88		118		148		178		208
	29		59		89		119		149		179		209
	30		60		90		120		150		180		210

Search Notes	Application No. 09/632,856	Applicant(s) SORRELLS ET AL.
	Examiner Kevin Y Kim	Art Unit 2634

SEARCHED			
Class	Subclass	Date	Examiner
375	222 328	8/21/04	Kim
455	131		
	137		

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
"EAST" update	8/21/04	Kim

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
375	222	8/21/04	Kim
	328		

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Sorrells *et al*	Confirmation No.: 2377
Appl. No.: 09/632,856	Art Unit: 2634
Filed: August 4, 2000	Examiner: Kevin Y. Kim
For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations**	Atty. Docket: 1744.0630003

Amendment Under 37 C.F.R. § 1.312

Mail Stop Issue Fee

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herein is an Amendment Under 37 C.F.R. § 1.312. As payment of the issue fee has not yet been made or is filed herewith, Applicants respectfully submit that filing under 37 C.F.R. § 1.312 is proper. (M.P.E.P. § 714.16.)

It is believed that extensions of time are not required beyond those that may otherwise be provided for in documents accompanying this Amendment. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor are hereby authorized to be charged to our Deposit Account No. 19-0036.

This Amendment is provided in the following format:

(A) Each section begins on a separate sheet;

(B) Starting on a separate sheet, amendments to the specification by presenting replacement paragraphs marked up to show changes made;

(C) Starting on a separate sheet, a complete listing of all of the claims:

- in ascending order;
- with status identifiers; and
- with markings in the currently amended claims;

(D) Starting on a separate sheet, the Remarks.

Amendments to the Specification:

On page 7, line 9, please amend the paragraph as follows:

FIGs. 42-44 are example implementations of a WLAN interface; FIG. 42 includes FIGs. 42A and 42B and should be referred to for all references to FIG. 42 in the specification. FIG. 43 includes FIGs. 43A and 43B and should be referred to for all references to FIG. 43 in the specification. FIG. 44 includes FIGs. 44A and 44B and should be referred to for all references to FIG. 44 in the specification.

On page 7, line 10, please amend the paragraph as follows:

FIGS. 45, 46A, and 46B and 46C relate to an example MAC interface for an example WLAN interface embodiment;

On page 7, line,12, please amend the specification as follows:

FIGS. 47, 48, 49A, and 49B and 49C relate to an example demodulator/modulator facilitation module for an example WLAN interface embodiment; FIG. 47 includes FIGs. 47A-D and should be referred to for all references to FIG. 47 in the specification. FIG. 48 includes FIGs. 48A-B and should be referred to for all references to FIG. 47 in the specification.

On page 7, line 14, please amend the specification as follows:

FIGS. 50, 51, 52A, 52B, and 52C relate to an example alternate demodulator/modulator facilitation module for an example WLAN interface embodiment; FIG. 50 includes FIGs. 50A-D and should be referred to for all references to FIG.50 in the specification. FIG. 51 includes FIGs. 51A-B and should be referred to for all references to FIG. 51 in the specification. FIG. 52B includes FIG. 52B-1 and should be referred to for all references to FIG. 52B in the specification.

On page 7, line 16, please amend the specification as follows:

FIGS. 53 and 54 relate to an example receiver for an example WLAN interface embodiment; FIG. 53 includes FIGs. 53A-C and should be referred to for all references to FIG. 53 in the specification.

On page 7, line 18, please amend the specification as follows:

FIGS. 55, 56A, and 56B relate to an example synthesizer for an example WLAN interface embodiment; FIG. 55 includes FIGs. 55A-C and should be referred to for all references to FIG. 55 in the specification.

On page 7, line 20, please amend the specification as follows:

FIGS. 57, 58, 59, 60, 61A, and 61B relate to an example transmitter for an example WLAN interface embodiment; FIG. 57 includes FIGs. 57A-D and should be referred to for all references to FIG. 57 in the specification. FIG. 60 includes FIGs. 60A-D and should be referred to for all references to FIG. 60 in the specification.

On page 7, lines 22, please amend the specification as follows:

FIGS. 62 and 63 relate to an example motherboard for an example WLAN interface embodiment; FIG. 62 includes FIGs. 62A-I and should be referred to for all references to FIG. 62 in the specification.

On page 7, lines 24-25, please amend the specification as follows:

FIGS. 64-66 relate to example LNAs for an example WLAN interface embodiment; FIG. 64 includes FIGs. 64A-C and should be referred to for all references to FIG. 64 in the specification. FIG. 65 includes FIGs. 65A-E and should be referred to for all references to FIG. 65 in the specification. FIG. 66 includes FIGs. 66A-B and should be referred to for all references to FIG. 66 in the specification.

On page 8, line 3, please amend the specification as follows:

FIG. 70A illustrates an IQ receiver having shunt UFT modules according to embodiments of the invention; FIG. 70A includes FIGs. 70A-1 and should be referred to for all references to FIG. 70A in the specification.

On page 8, line 9, please amend the specification as follows:

FIG. 70E illustrates an example IQ modulation receiver embodiment according to embodiments of the invention; FIG. 70E includes FIG. 70E1 and FIG. 70E2 and should be referred to for all references to FIG. 70E in the specification.

On page 8, line 15, please amend the specification as follows:

FIG. 70S illustrates a FET configuration of an IQ receiver embodiment according to embodiments of the invention; FIG. 70S includes FIGs. 70S-1 and should be referred to for all references to FIG. 70S in the specification.

On page 10, line 16, please amend the specification as follows:

FIGS. 90A-D illustrate[[s]] various implementation circuits for the modulator 7410, according to embodiments of the present invention; FIG. 90B includes FIGs. 90B-1, 90B-2, 90B-3, and 90B-4 and should be referred to for all references to FIG. 90B in the specification. FIG. 90C includes FIGs. 90C-1, 90C-2, 90C-3, and 90C-4 and should be referred to for all references to FIG. 90C in the specification.

On page 10, line 26, please amend the specification as follows:

FIGs. 95A-C, and FIGs. 96-161 illustrate schematics for an integrated circuit implementation example of the present invention. FIG. 97 includes FIGs. 97A-D and should be referred to for all references to FIG. 97 in the specification. FIG 105 includes FIGs. 105A-D, 105 E1-E2, and 105F-V, and should be referred to for all references to FIG. 105 in the specification. FIG. 106 includes FIGs. 106A-F and should be referred to for all references to FIG. 106 in the specification. FIG. 107 includes FIGs. 107A-D and should be referred to for all references to FIG. 107 in the specification. FIG. 109 includes FIGs. 109A-D and should be referred to for all references to FIG. 109 in the specification. FIG. 110 includes FIGs. 110A-D and should be referred to for all references to FIG. 110 in the specification. FIG. 112 includes FIGs. 112A-D and should be referred to for all references to FIG. 112 in the specification. FIG. 113 includes FIGs. 113A-F and should be referred to for all references to FIG. 113 in the specification. FIG. 115 includes FIGs. 115A-F and should be referred to for all references to FIG. 115 in the specification. FIG. 118 includes FIGs. 118A-D and should be referred to for all references to FIG. 118 in the specification. FIG. 123 includes FIGs. 123A-H and should be referred to for all references to FIG. 123 in the specification. FIG. 125 includes FIGs. 125A-H and should be referred to for all references to FIG. 125 in the specification. FIG.

126 includes FIGs. 126A-H and should be referred to for all references to FIG. 126 in the specification. FIG. 127 includes FIGs. 127A-D and should be referred to for all references to FIG. 127 in the specification. FIG. 150 includes FIGs. 150A-H and should be referred to for all references to FIG. 150 in the specification. FIG. 159 includes FIGs. 159A-D and should be referred to for all references to FIG. 159 in the specification. FIG. 160 includes FIGs. 160A-D and should be referred to for all references to FIG. 160 in the specification.

Remarks

Formal drawings are filed herewith. Due to the detailed nature of the drawings, some of the drawings (as filed) were divided into multiple sheets to comply with the formal drawing requirements. Note that any added sheets are labeled as "New Sheets" on the formal drawings. Accordingly, the "Brief Description of the Figures" section of the specification has been amended herein so as to be consistent with the formal drawings. None of the amendments add new matter or change the scope of the claims. Accordingly, Applicants respectfully request that this Amendment be entered.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Jeff Helvey

Jeffrey T. Helvey
Attorney for Applicants
Registration No. 44,757

Date: 12/10/04

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Sterne Kessler Goldstein Fox
ATTORNEYS AT LAW

December 10, 2004

WRITER'S DIRECT NUMBER:
(202) 772-8675
INTERNET ADDRESS:
JHELVEY@SKGF.COM

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Mail Stop Issue Fee

Re: Allowed U.S. Utility Patent Application
Appl. No. 09/632,856; Filed: August 4, 2000
For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations**
Inventors: Sorrells *et al.*
Our Ref: 1744.0630003

Sir:

In response to the **Notice of Allowance and Issue Fee Due** dated September 10, 2004, the following documents are forwarded for appropriate action by the U.S. Patent and Trademark Office:

1. Issue Fee Transmittal (Form PTOL-85B);

2. Fee Transmittal (Form PTO/SB/17);

3. Amendment Under 37 C.F.R. § 1.312

4. Submission of Drawings;

5. 349 sheets of Drawings, approval of which is respectfully requested;

6. Return postcard; and

7. PTO-2038 Credit Card Payment Form for $1,403.00 to cover:
$1,400.00 Issue Fee; and
$ 3.00 Advance copies of patent.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036. If extensions of time under 37 C.F.R. § 1.136 other than those otherwise provided for herewith are required to prevent abandonment of the present patent application, then such extensions of time are hereby petitioned, and any fees therefor are hereby authorized to be charged to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

JTH Helvey

Jeffrey T. Helvey
Attorney for Applicants
Registration No. 44,757

Enclosures

JTH/agj
335548_1.DOC

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Sorrells *et al.*

Appl. No.: 09/632,856

Filed: August 4, 2000

For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations**

Confirmation No.: 2377

Art Unit: 2634

Examiner: Kim, Kevin

Atty. Docket: 1744.0630003

Submission of Drawings

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith are three-hundred forty-nine (349) sheets of drawings with Figures 1A, 1B, 1C, 1D, 2A, 2B, 3, 4, 5, 6A, 6B, 6C, 6D, 6E, 6F, 6G, 6H, 6I, 7, 8, 9, 10, 11, 12, 13, 14, 15A, 15B, 15C, 15D, 15E, 15F, 16, 17, 18, 19, 20A, 20A-1, 20B, 20C, 20D, 20E, 20F, 21, 22A, 22B, 22C, 22D, 22E, 22F, 23A, 23B, 23C, 23D, 23E, 23F, 24A, 24B, 24C, 24D, 24E, 24F, 24G, 24H, 24I, 24J, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42A, 42B, 43A, 43B, 44A, 44B, 45, 46A, 46B, 46C, 47, 47A, 47B, 47C, 47D, 48A, 48B, 49A, 49B, 49C, 50, 50A, 50B, 50C, 50D, 51A, 51B, 52A, 52B, 52B-1, 52C, 53, 53A, 53B, 53C, 54, 55, 55A, 55B, 55C, 56A, 56B, 57, 57A, 57B, 57C, 57D, 58, 59, 60, 60A, 60B, 60C, 60D, 61A, 61B, 62, 62A, 62B, 62C, 62D, 62E, 62F, 62G, 62H, 62I, 63, 64, 64A, 64B, 64C, 65, 65A, 65B, 65C, 65D, 65E, 66A, 66B, 67A, 67B, 68A, 68B, 69A, 69B, 70A, 70A-1, 70B, 70C, 70D, 70E1, 70E2, 70F, 70G, 70H, 70I, 70J, 70K, 70L, 70M, 70N, 70O, 70P, 70Q, 70R, 70S, 70S-1, 71A, 71B, 71C, 71D, 72A, 72B, 72C, 72D, 72E, 72F, 72G, 72H, 72I, 72J, 73A, 73B, 74, 75A, 75B, 75C, 76A, 76B, 77, 78, 79A, 79B, 79C, 79D, 80, 81A, 81B, 81C, 82, 83, 84, 85, 86, 87, 88, 89A, 89B, 89C, 89D, 89E, 90A, 90B, 90B-1, 90B-2, 90B-3, 90B-4, 90C, 90C-1, 90C-2, 90C-3, 90C-4, 90D, 91, 92, 93, 94, 95A, 95B, 95C, 96, 97A, 97B, 97C, 97D, 98, 99, 100, 101, 102, 103, 104, 105, 105A, 105B, 105C, 105D, 105E-1, 105E-2, 105F, 105G, 105H, 105I, 105J, 105K, 105L, 105M, 105N, 105O, 105P, 105Q, 105R, 105S, 105T, 105U, 105V, 106A, 106B, 106C, 106D, 106E, 106F, 107A, 107B, 107C, 107D, 108, 109A, 109B, 109C, 109D, 110A, 110B, 110C, 110D, 111, 112A, 112B, 112C, 112D, 113A, 113B, 113C. 113D, 113E, 113F, 114, 115A, 115B, 115C, 115D, 115E, 115F, 116, 117, 118A, 118B, 118C, 118D, 119, 120, 121, 122, 123A, 123B, 123C. 123D, 123E, 123F, 123G, 123H, 124, 125A, 125B, 125C, 125D, 125E, 125F, 125G, 125H, 126A, 126B, 126C, 126D, 126E, 126F, 126G, 126H, 127A, 127B, 127C, 127D, 128, 129, 130, 131, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 143, 144, 145, 146, 147, 148, 149, 150A, 150B, 150C, 150D, 150E, 150F, 150G, 150H, 151, 152, 153, 154, 155, 156, 157, 158, 159A, 159B, 159C, 159D, 160A, 160B, 160C, 160D, 161, corresponding to the above-captioned application. Identification of the drawings is provided in accordance with 37 C.F.R. § 1.84(c). Acknowledgment of the receipt, approval, and entry of these drawings into this application is respectfully requested.

It is not believed that an extension of time is required, other than any already provided herewith. However, if an extension of time is needed to prevent abandonment of the application, then such extension of time is hereby petitioned. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Jeffrey T. Helvey
Attorney for Applicants
Registration No. 44,757

Date: 12/10/04

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600
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335567_1.DOC

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

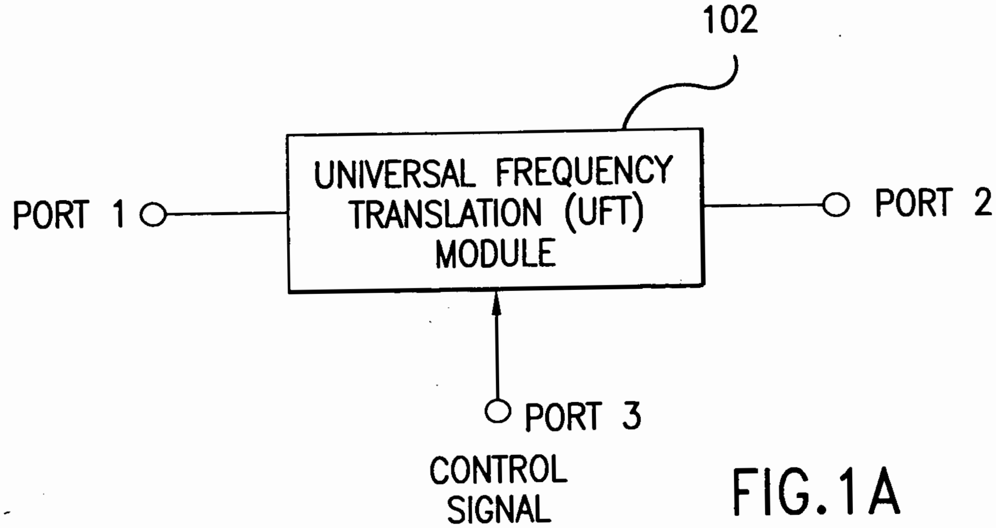

FIG.1A

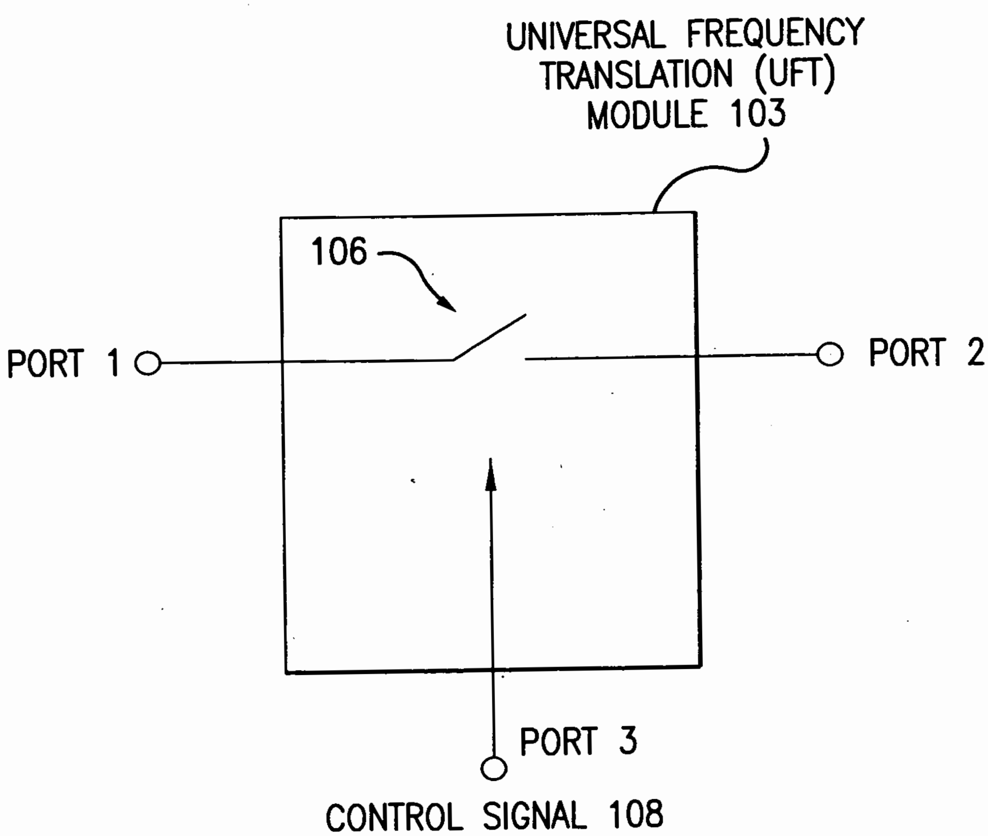

FIG.1B

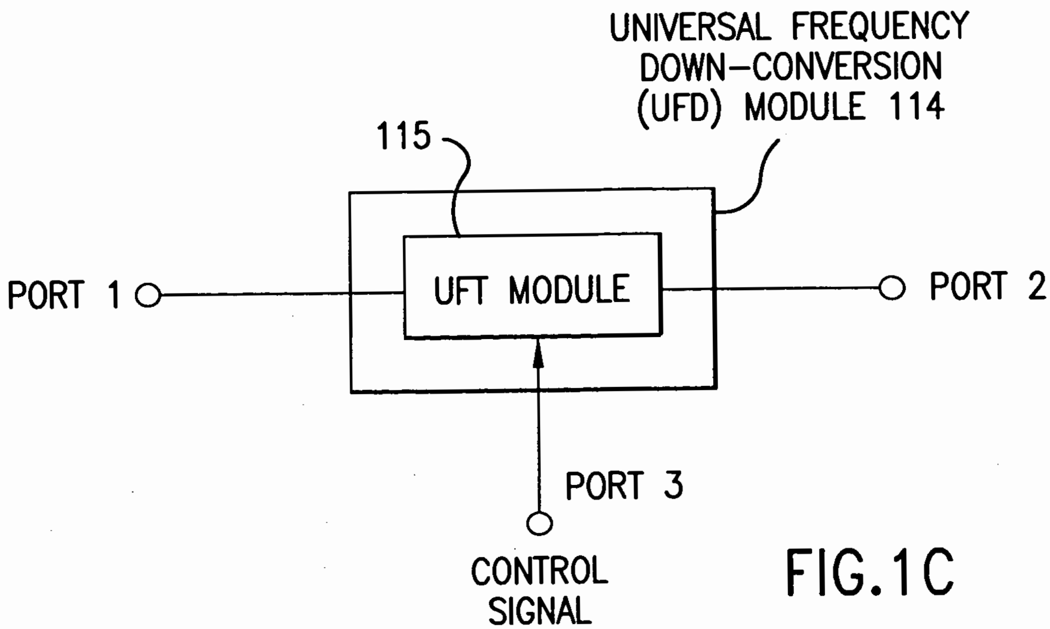
UNIVERSAL FREQUENCY
DOWN-CONVERSION
(UFD) MODULE 114
115
UFT MODULE
PORT 1
PORT 2
PORT 3
CONTROL
SIGNAL

FIG.1C

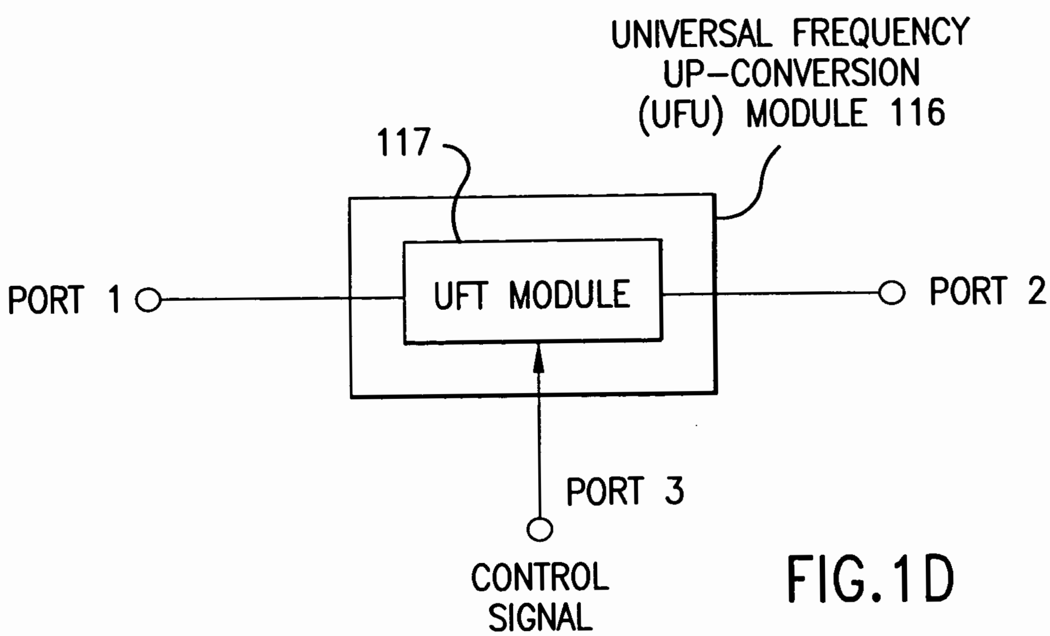
UNIVERSAL FREQUENCY
UP-CONVERSION
(UFU) MODULE 116
117
UFT MODULE
PORT 1
PORT 2
PORT 3
CONTROL
SIGNAL

FIG.1D

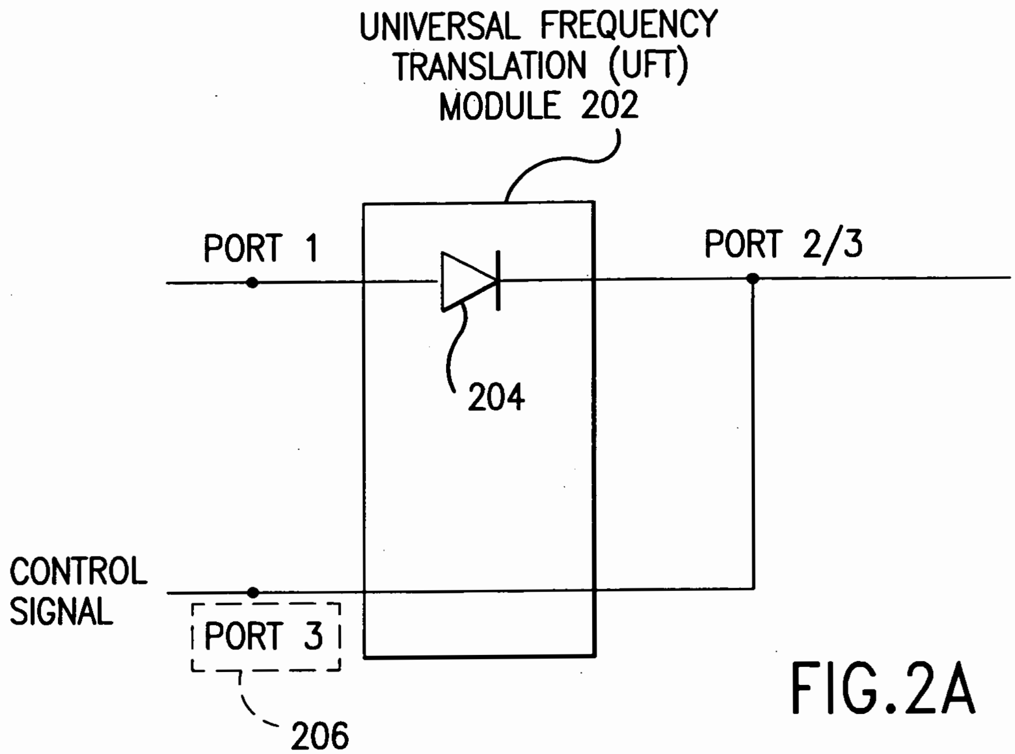
UNIVERSAL FREQUENCY
TRANSLATION (UFT)
MODULE 202
PORT 1
PORT 2/3
204
CONTROL
SIGNAL
PORT 3
206

FIG.2A

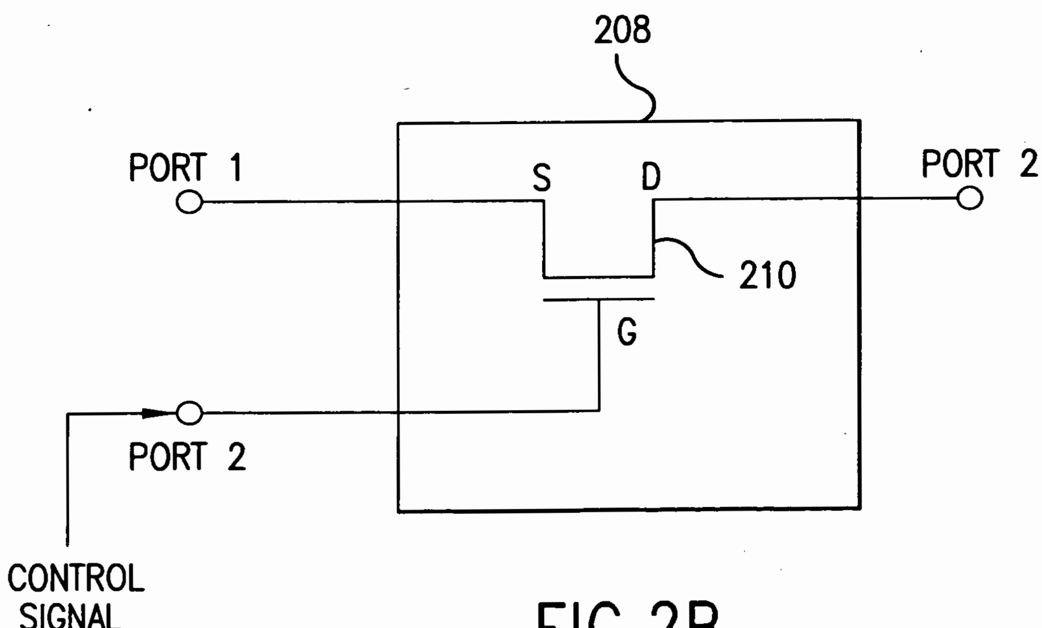
208
PORT 1
S
D
PORT 2
210
G
PORT 2
CONTROL
SIGNAL

FIG.2B

Replacement Sheet
Sheet 4 of 349
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Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

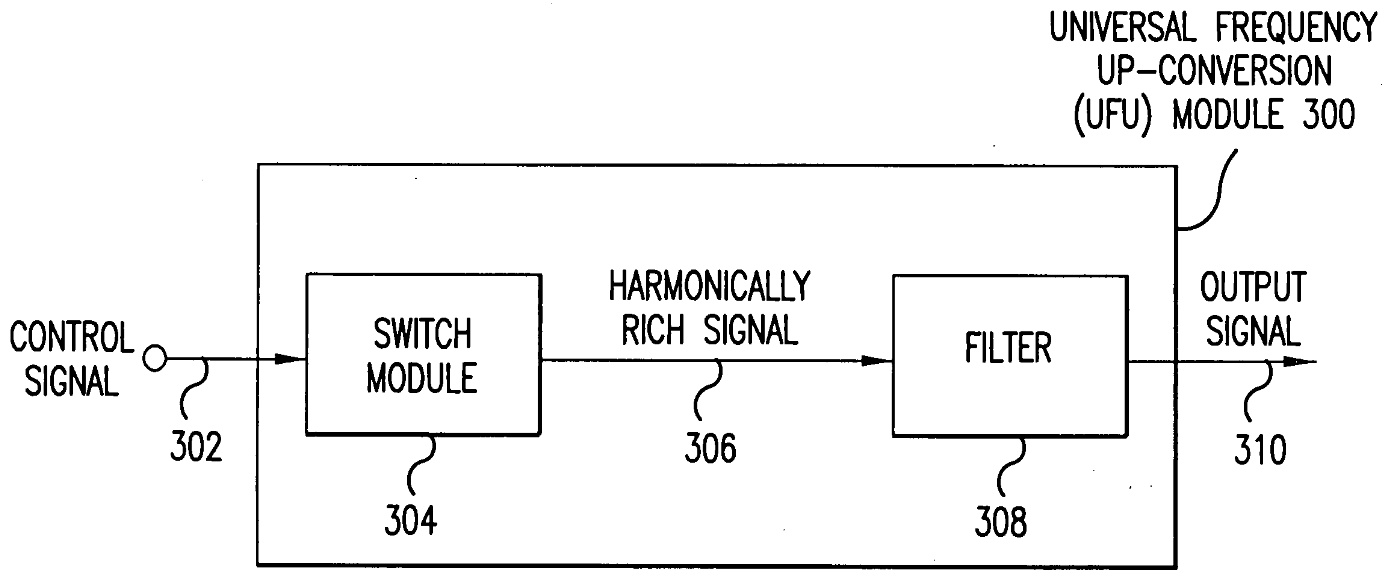

FIG.3

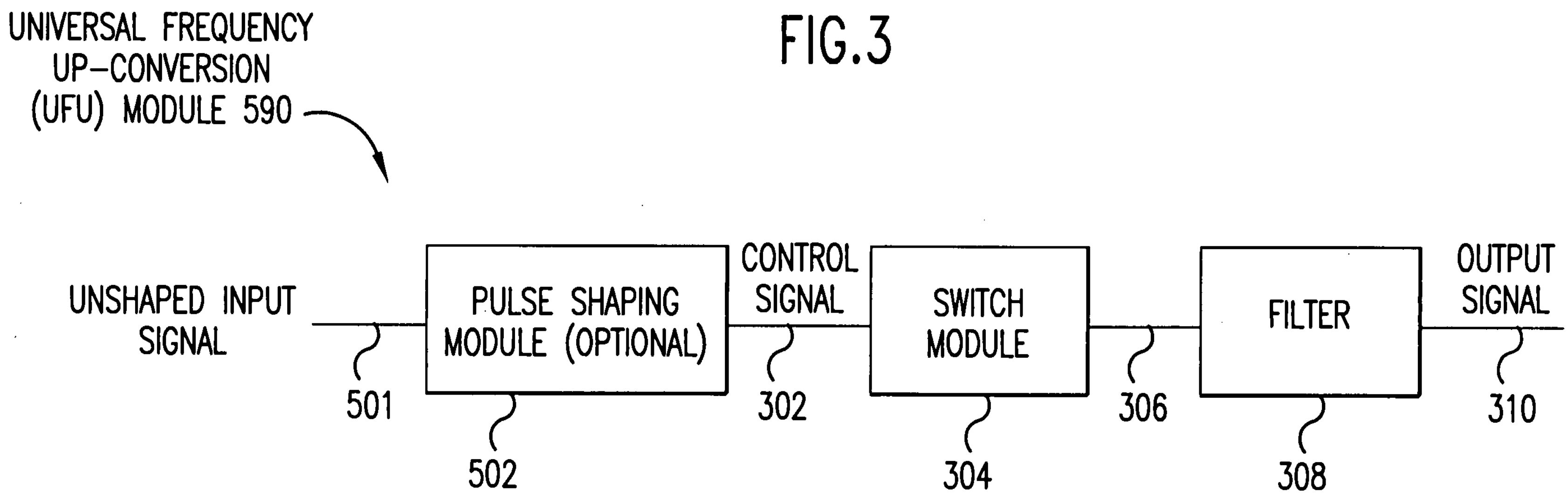

FIG.5

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Inventors: Sorrells et al.
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For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

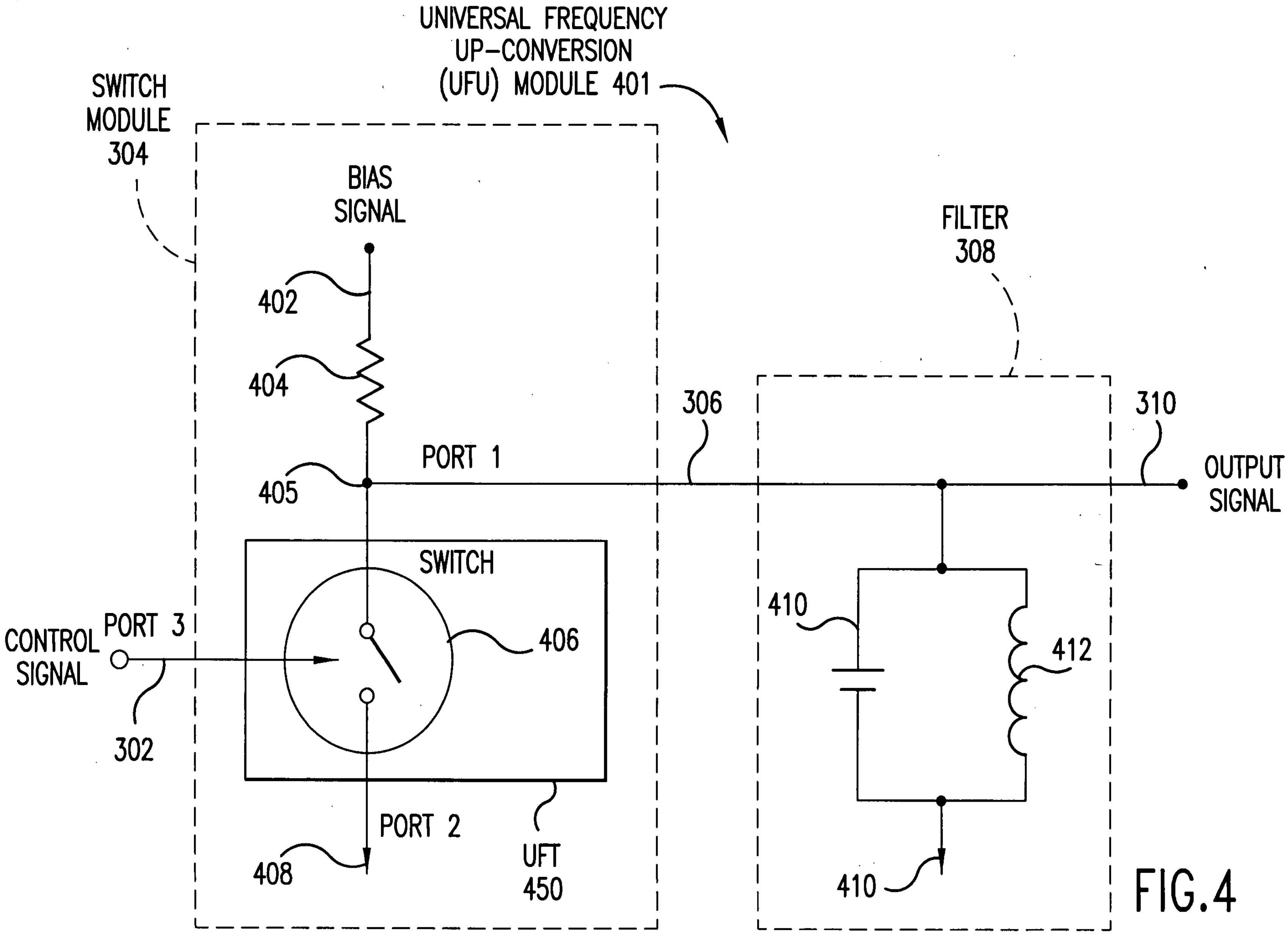

FIG.4

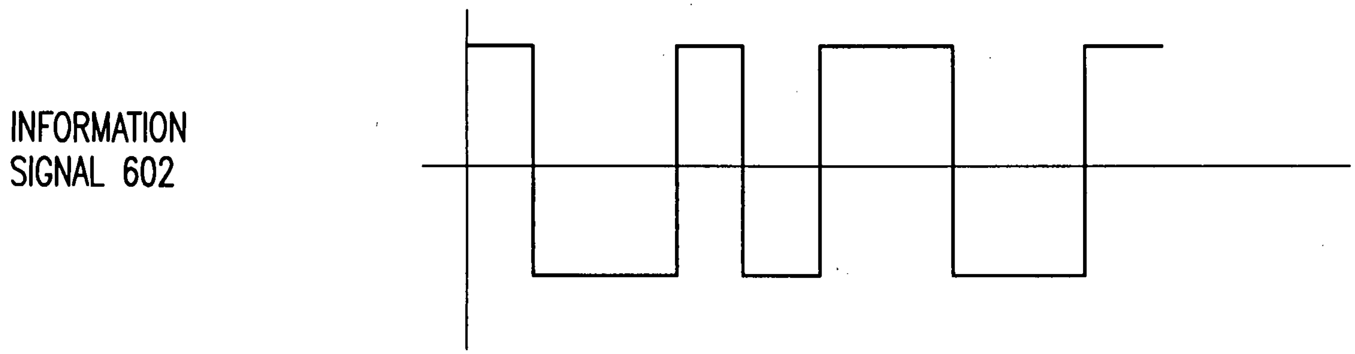

FIG.6A

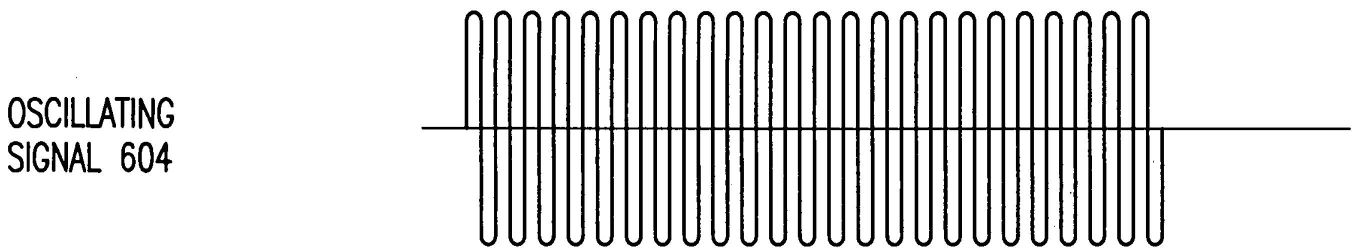

FIG.6B

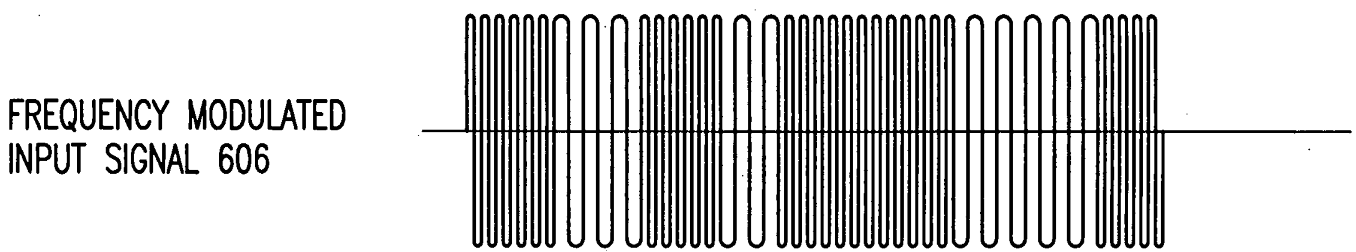

FIG.6C

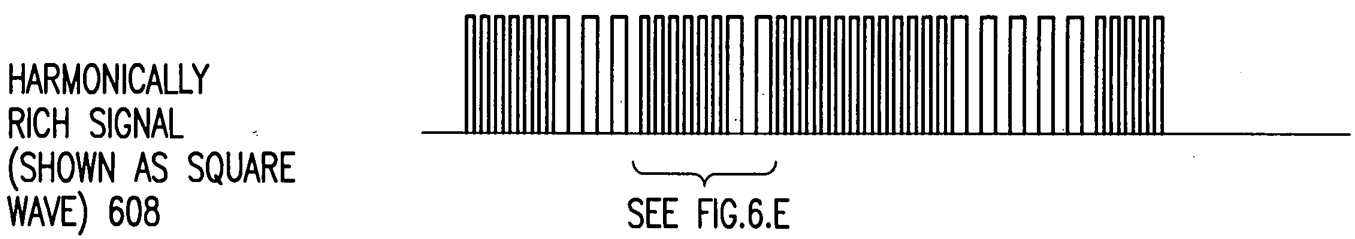

FIG.6D

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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

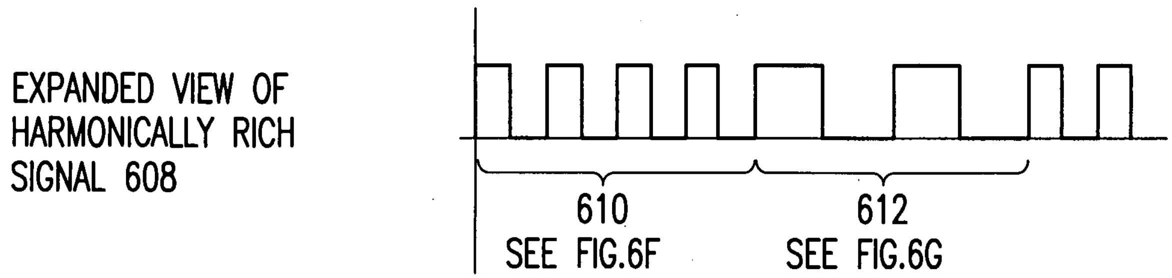

FIG.6E

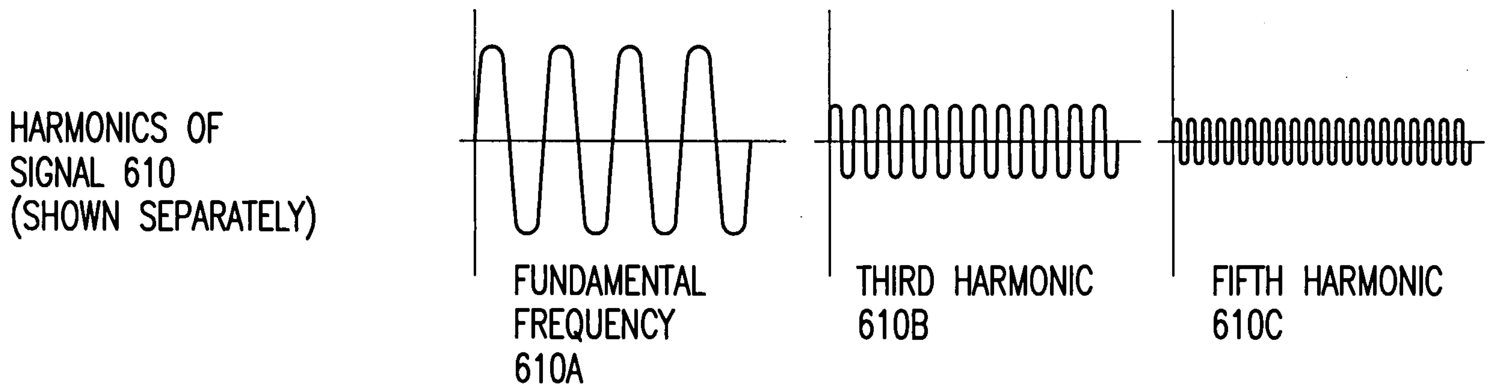

FIG.6F

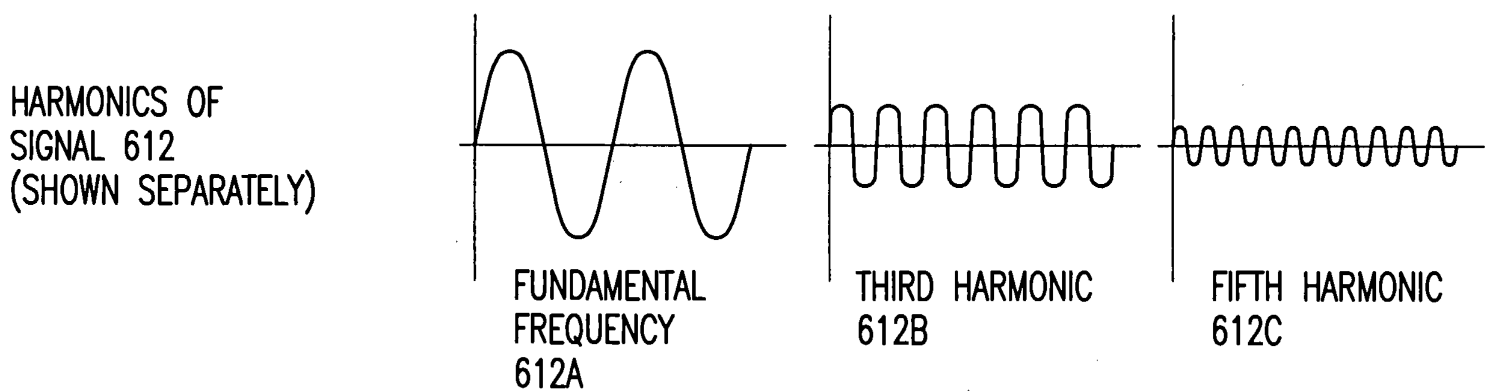

FIG.6G

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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
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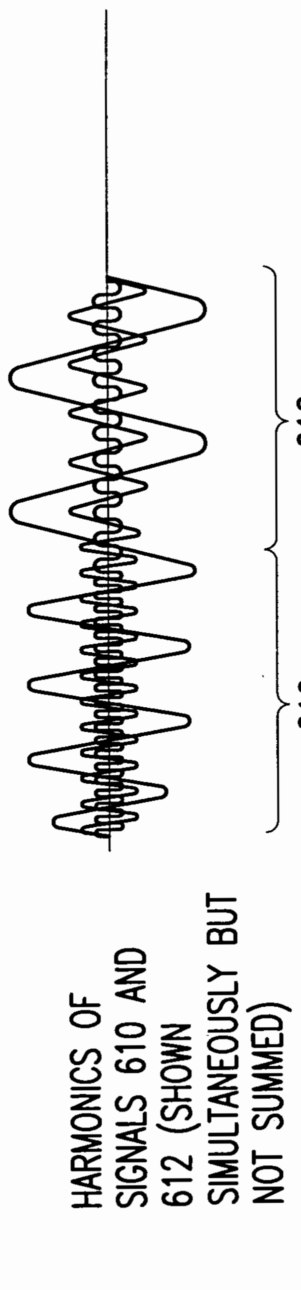
612
610
HARMONICS OF SIGNALS 610 AND 612 (SHOWN SIMULTANEOUSLY BUT NOT SUMMED)

FIG.6H

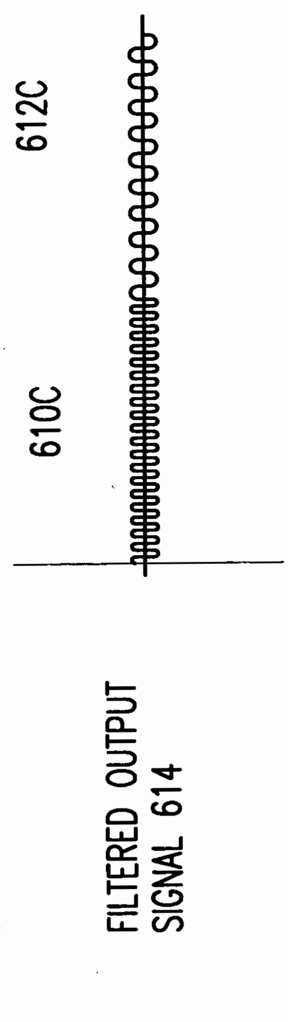
612C
610C
FILTERED OUTPUT SIGNAL 614

FIG.6I

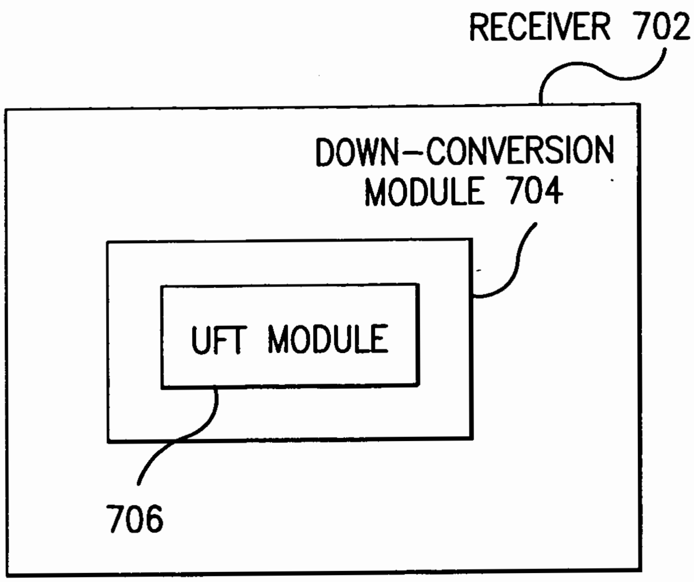

FIG.7

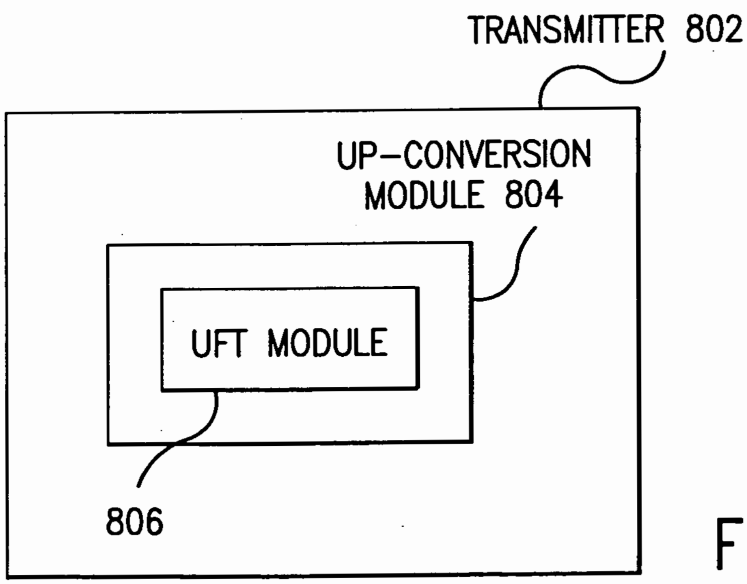

FIG.8

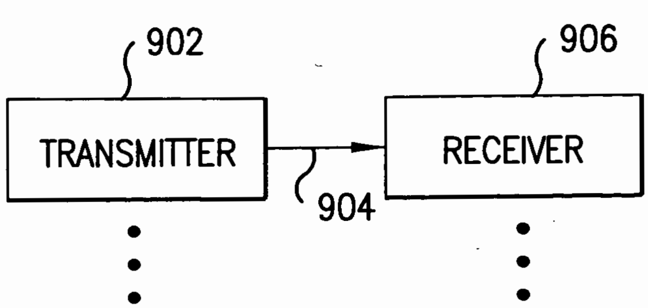

FIG.9

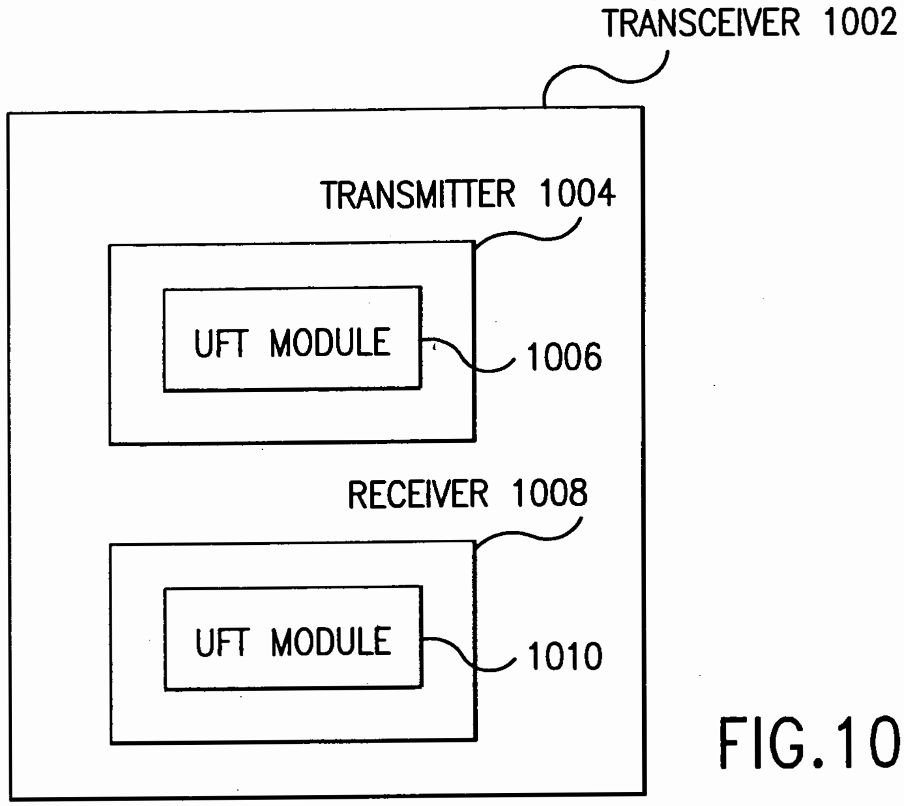
TRANSCEIVER 1002
TRANSMITTER 1004
UFT MODULE
1006
RECEIVER 1008
UFT MODULE
1010

FIG.10

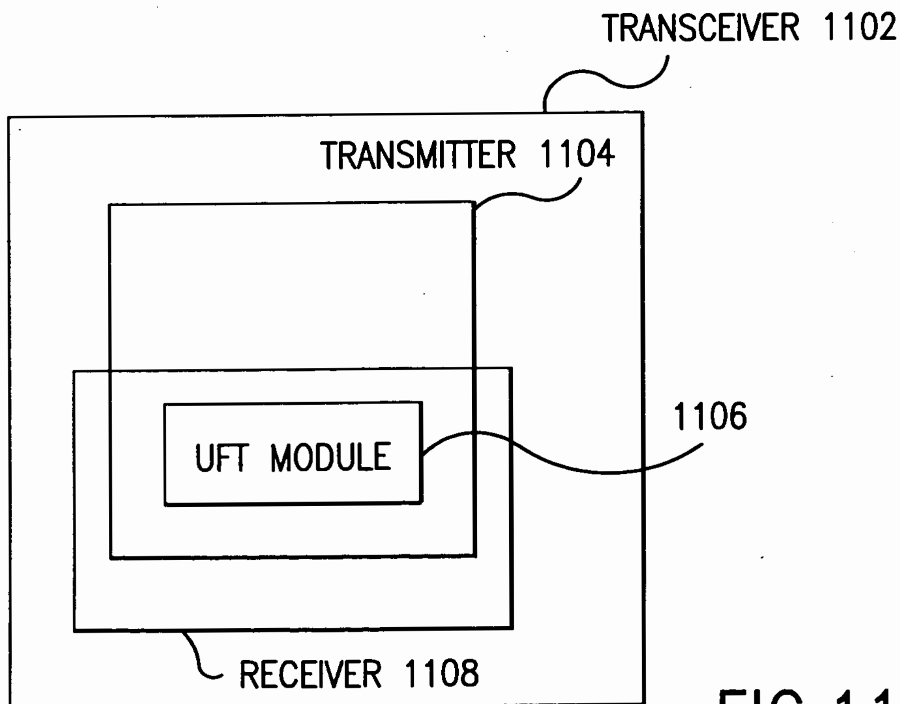
TRANSCEIVER 1102
TRANSMITTER 1104
UFT MODULE
1106
RECEIVER 1108

FIG.11

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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

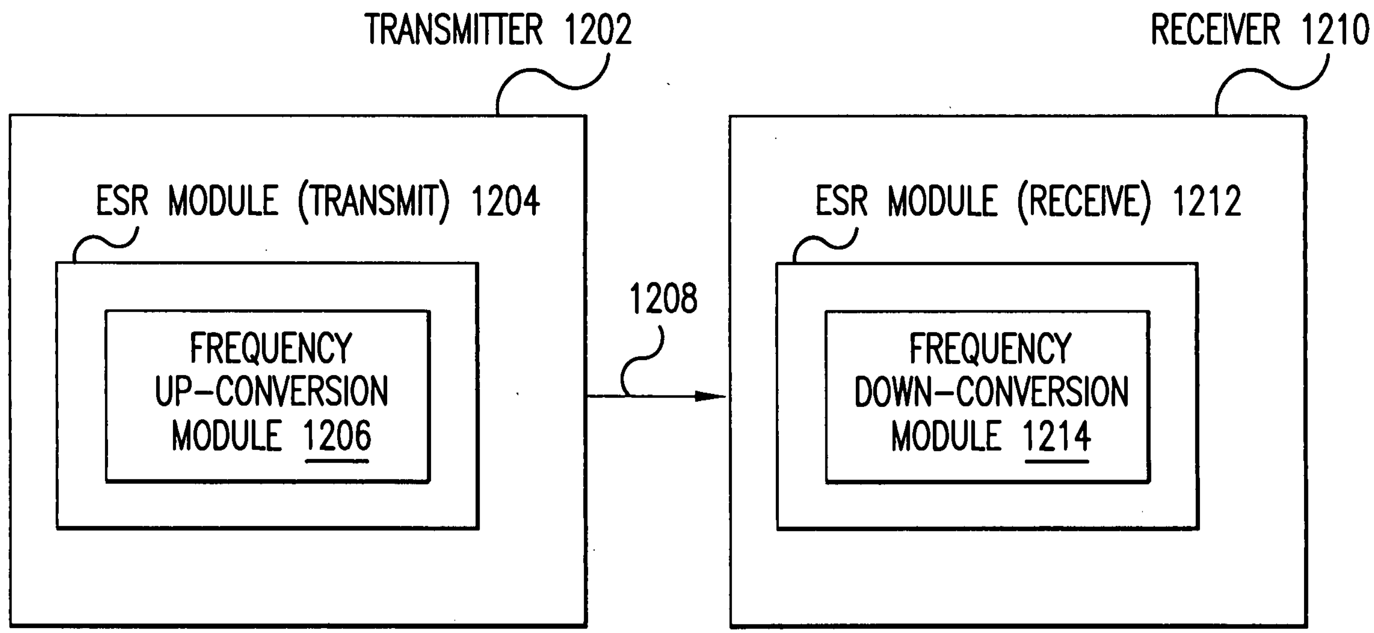

FIG.12

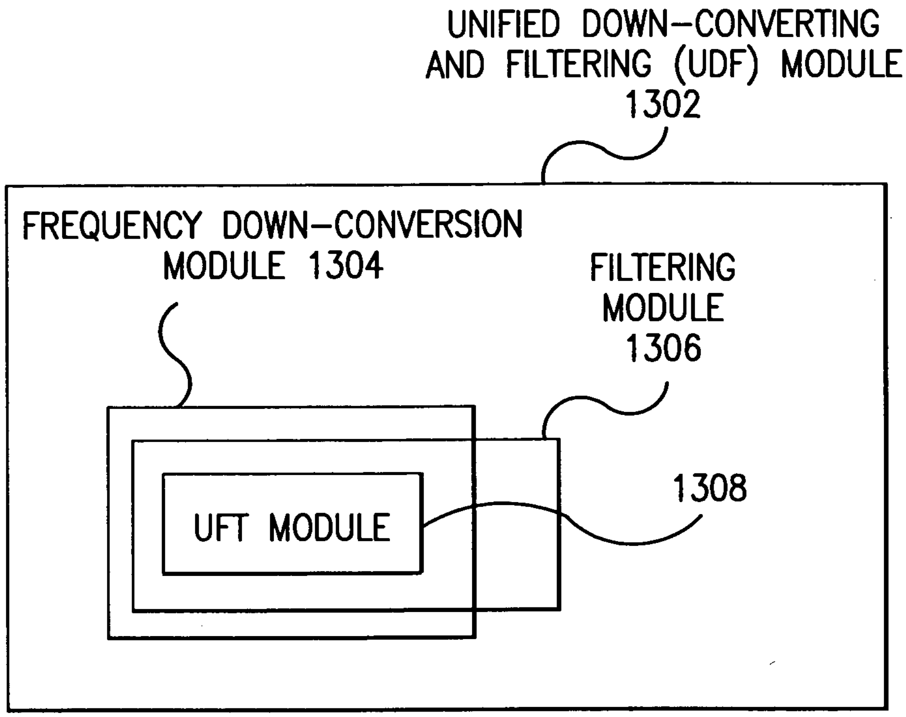
UNIFIED DOWN-CONVERTING
AND FILTERING (UDF) MODULE
1302
FREQUENCY DOWN-CONVERSION
MODULE 1304
FILTERING
MODULE
1306
1308
UFT MODULE

FIG.13

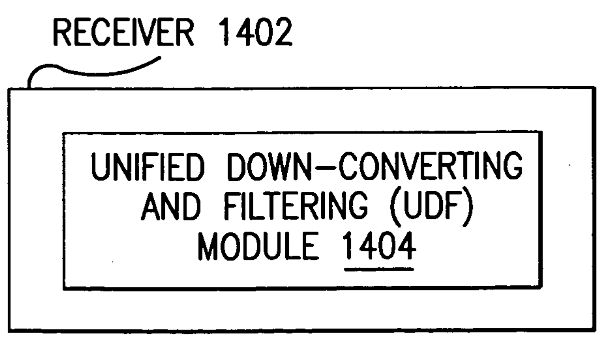
RECEIVER 1402
UNIFIED DOWN-CONVERTING
AND FILTERING (UDF)
MODULE 1404

FIG.14

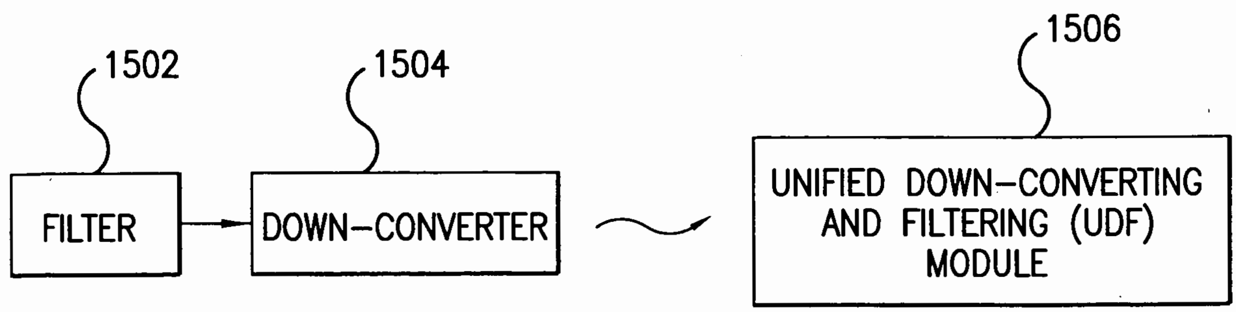

FIG.15A

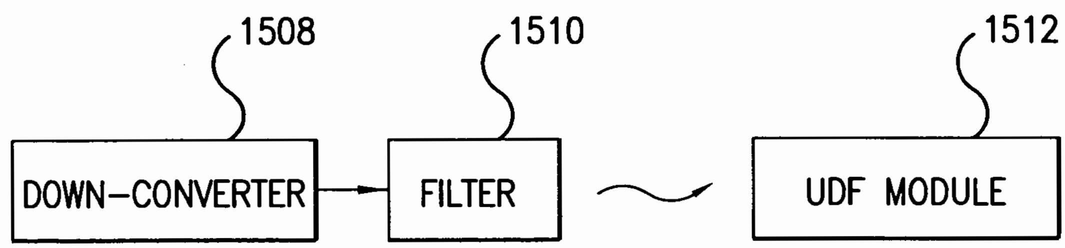

FIG.15B

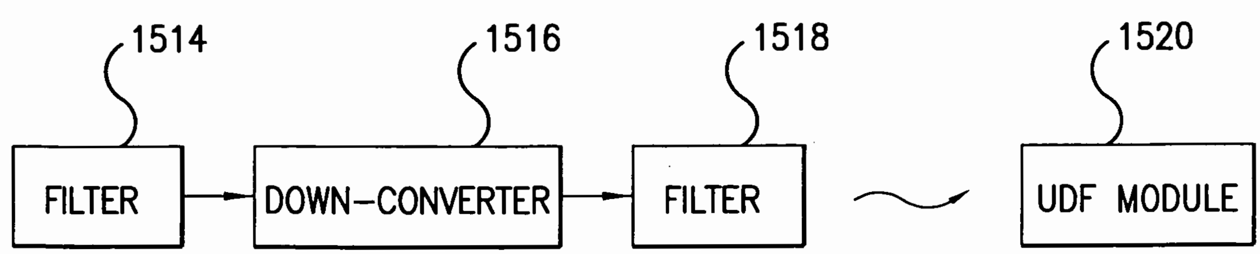

FIG.15C

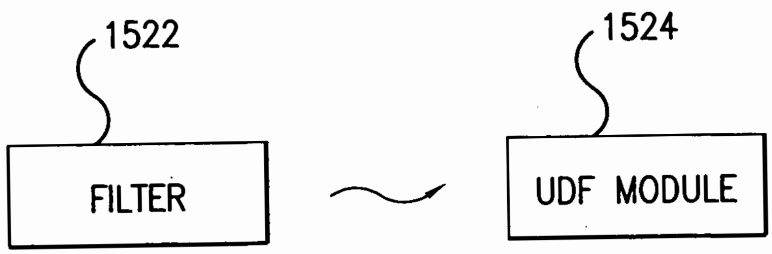

FIG.15D

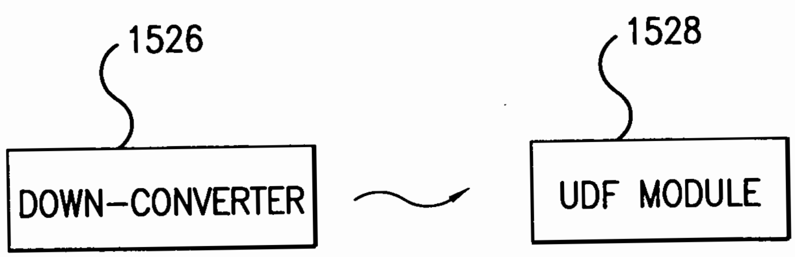

FIG.15E

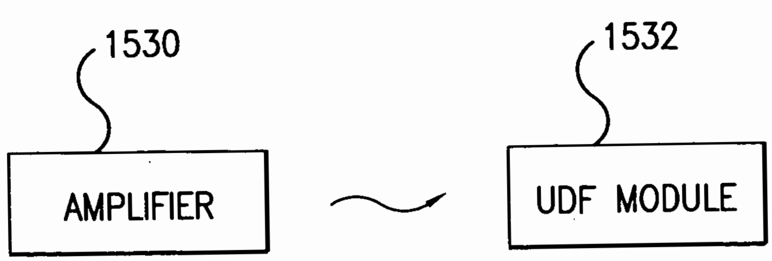

FIG.15F

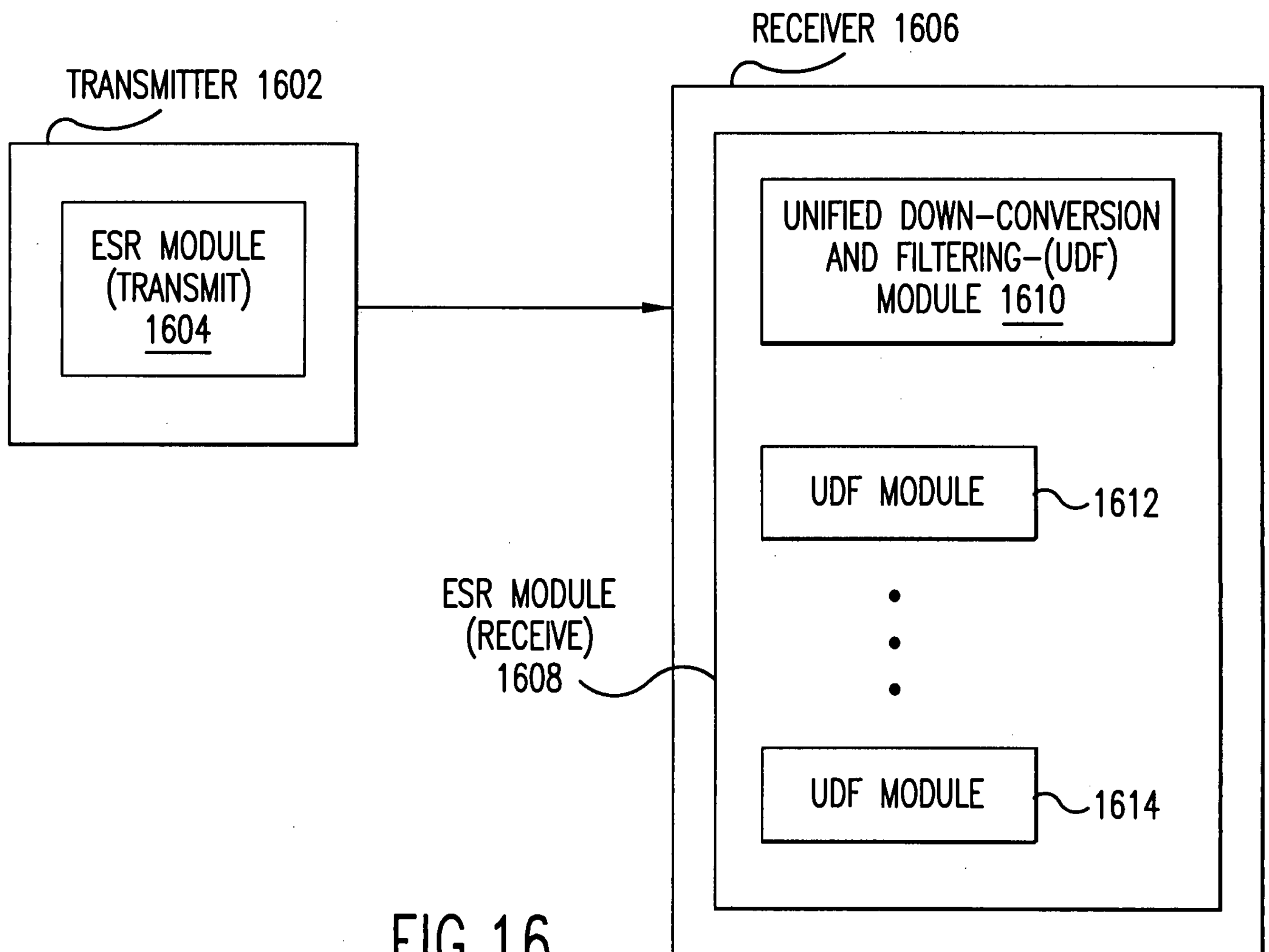

FIG.16

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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
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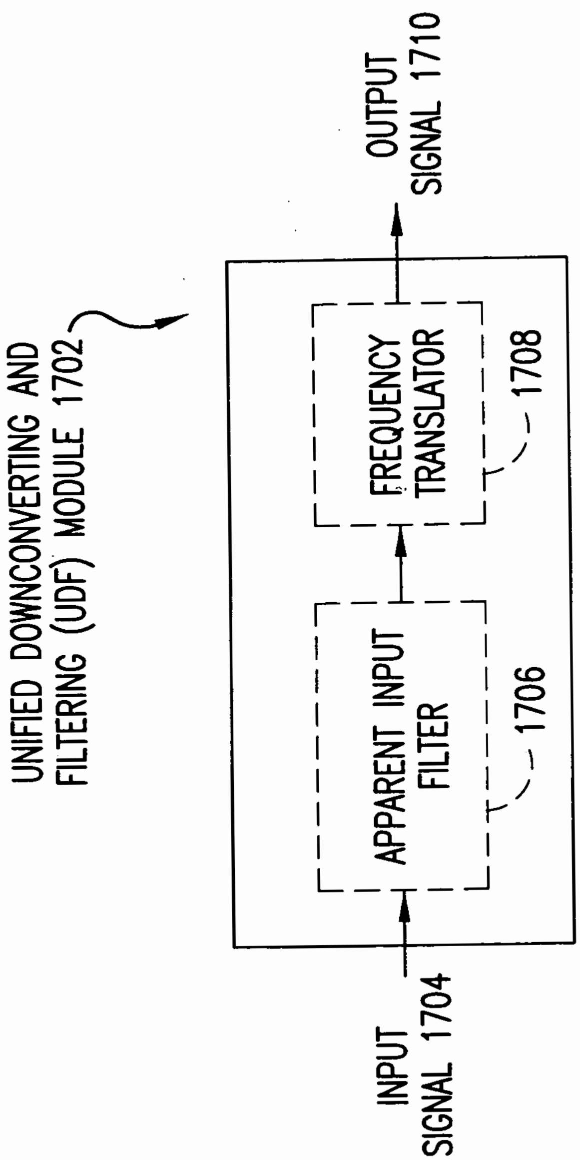

FIG.17

1802

TIME / NODE	t−1 (RISING EDGE OF ϕ_1)	t−1 (RISING EDGE OF ϕ_2)	t (RISING EDGE OF ϕ_1)	t (RISING EDGE OF ϕ_2)	t+1 (RISING EDGE OF ϕ_1)
1902	VI_{t-1} 1804	VI_{t-1} 1808	VI_t 1816	VI_t 1826	VI_{t+1} 1838
1904	—	VI_{t-1} 1810	VI_{t-1} 1818	VI_t 1828	VI_t 1840
1906	VO_{t-1} 1806	VO_{t-1} 1812	VO_t 1820	VO_t 1830	VO_{t+1} 1842
1908	—	VO_{t-1} 1814	VO_{t-1} 1822	VO_t 1832	VO_t 1844
1910	— 1807	—	VO_{t-1} 1824	VO_{t-1} 1834	VO_t 1846
1912	—	— 1815	—	VO_{t-1} 1836	VO_{t-1} 1848
1918	—	—	—	—	VI_t − 0.1 * VO_t − 0.8 * VO_{t-1} 1850

FIG.18

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Inventors: Sorrells et al.
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For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

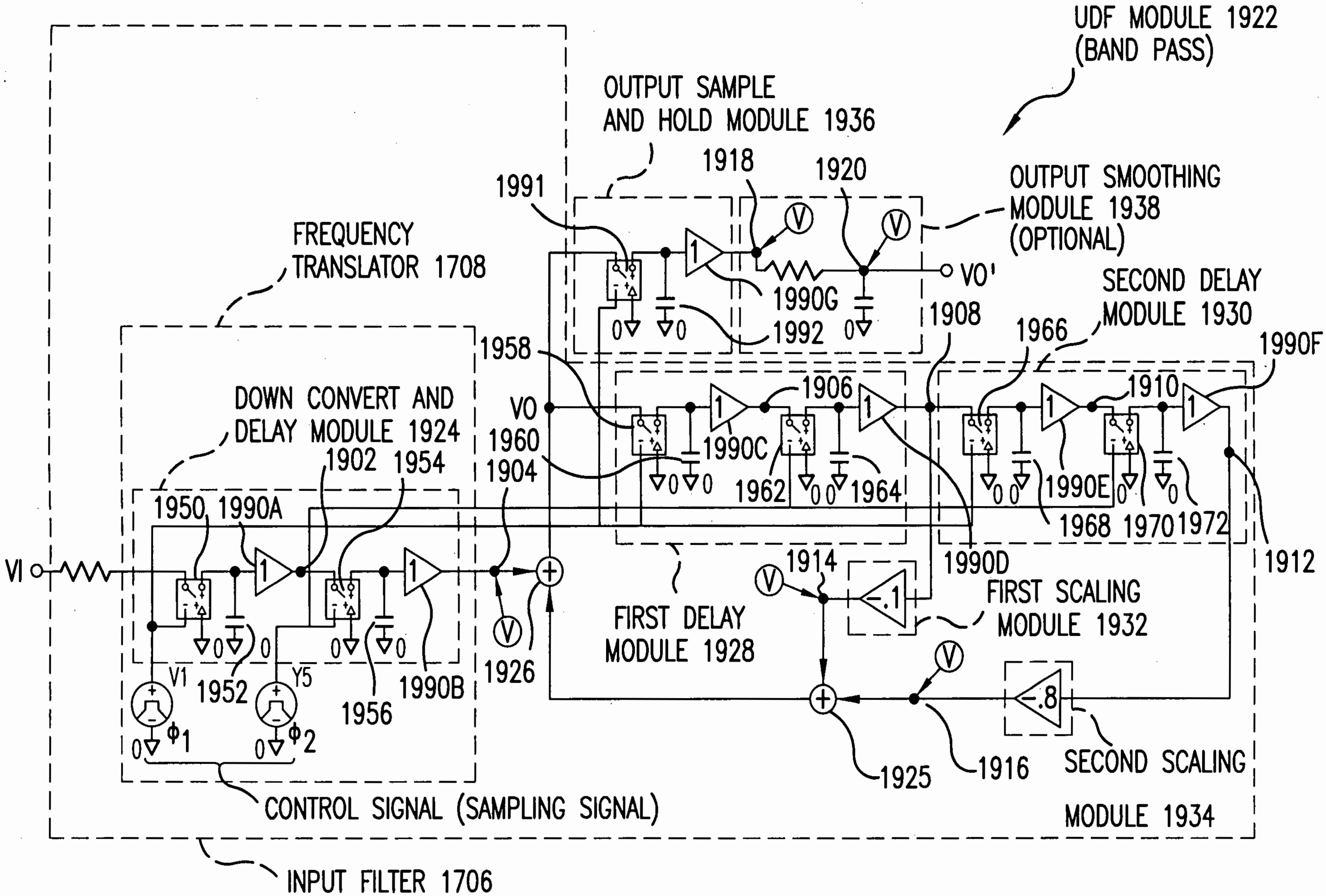

FIG. 19

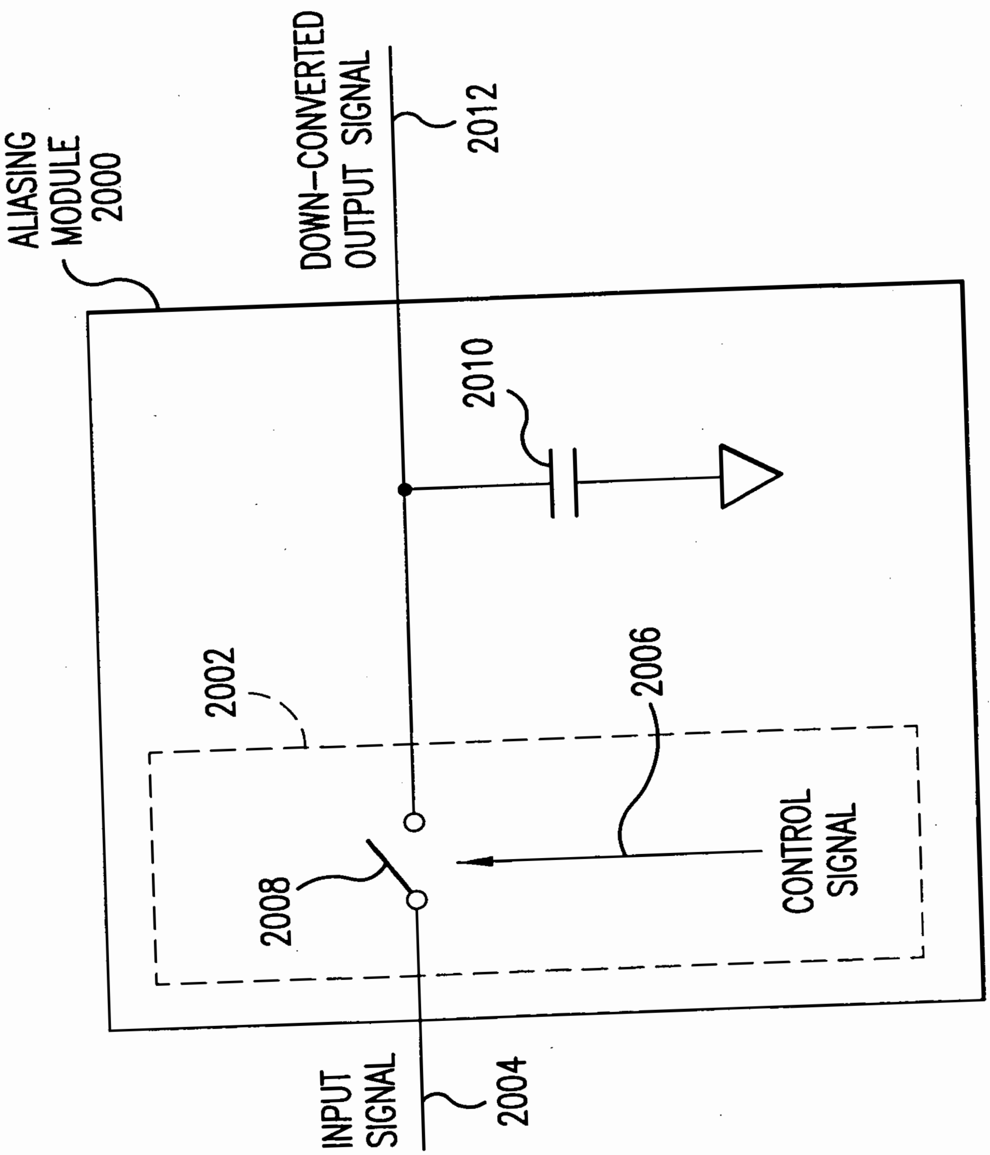
ALIASING MODULE 2000
DOWN-CONVERTED OUTPUT SIGNAL
2012
2010
2002
2006
2008
CONTROL SIGNAL
INPUT SIGNAL
2004

FIG.20A

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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

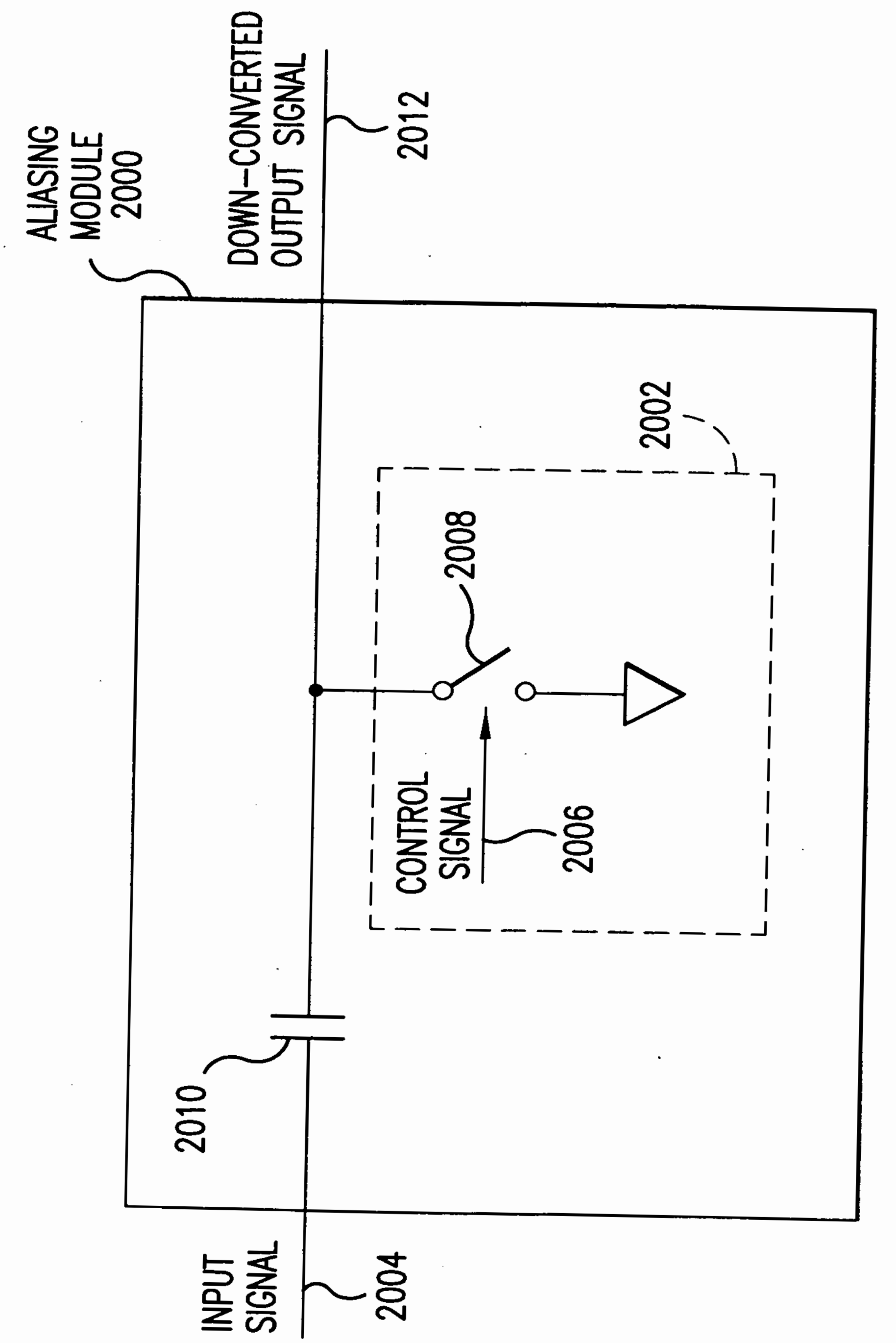

FIG.20A-1

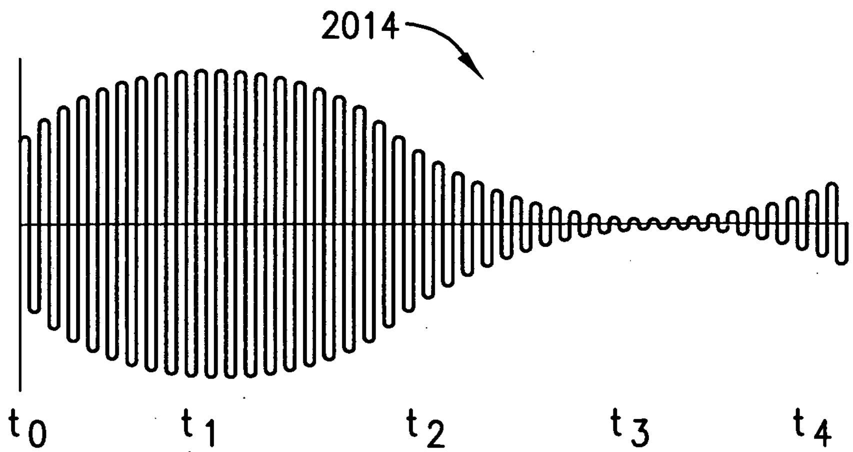

FIG.20B

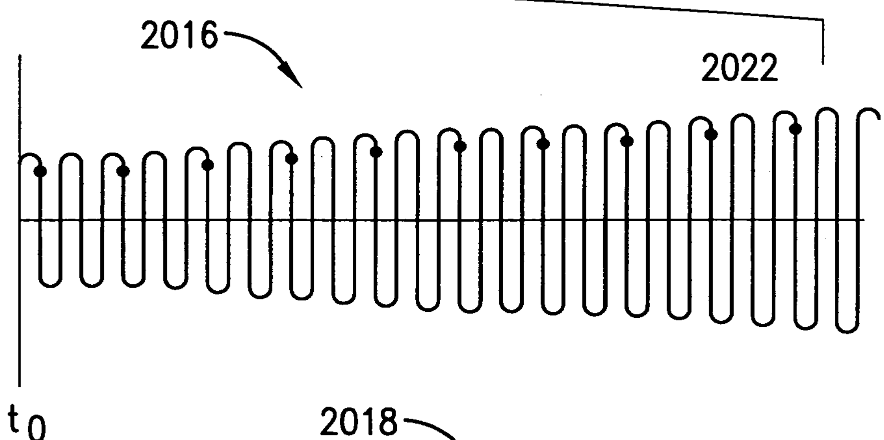

FIG.20C

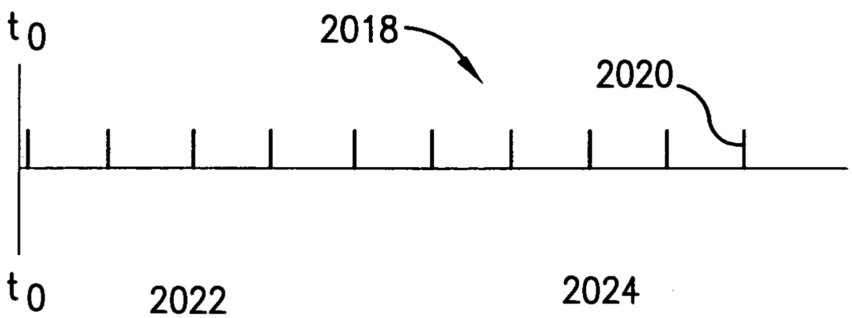

FIG.20D

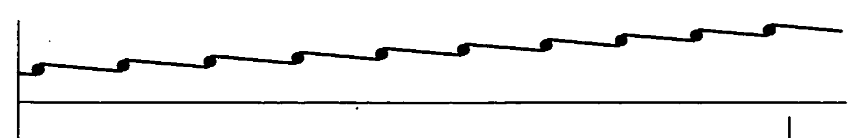

FIG.20E

FIG.20F

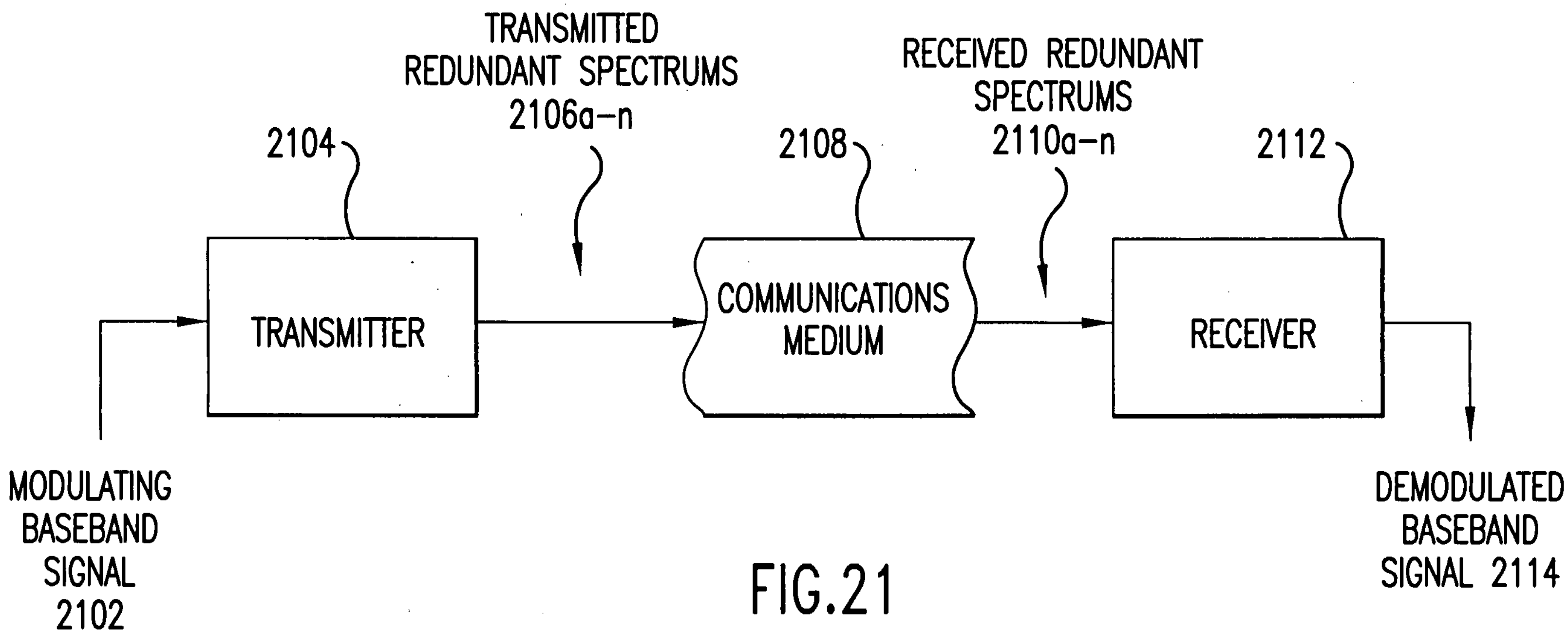

FIG.21

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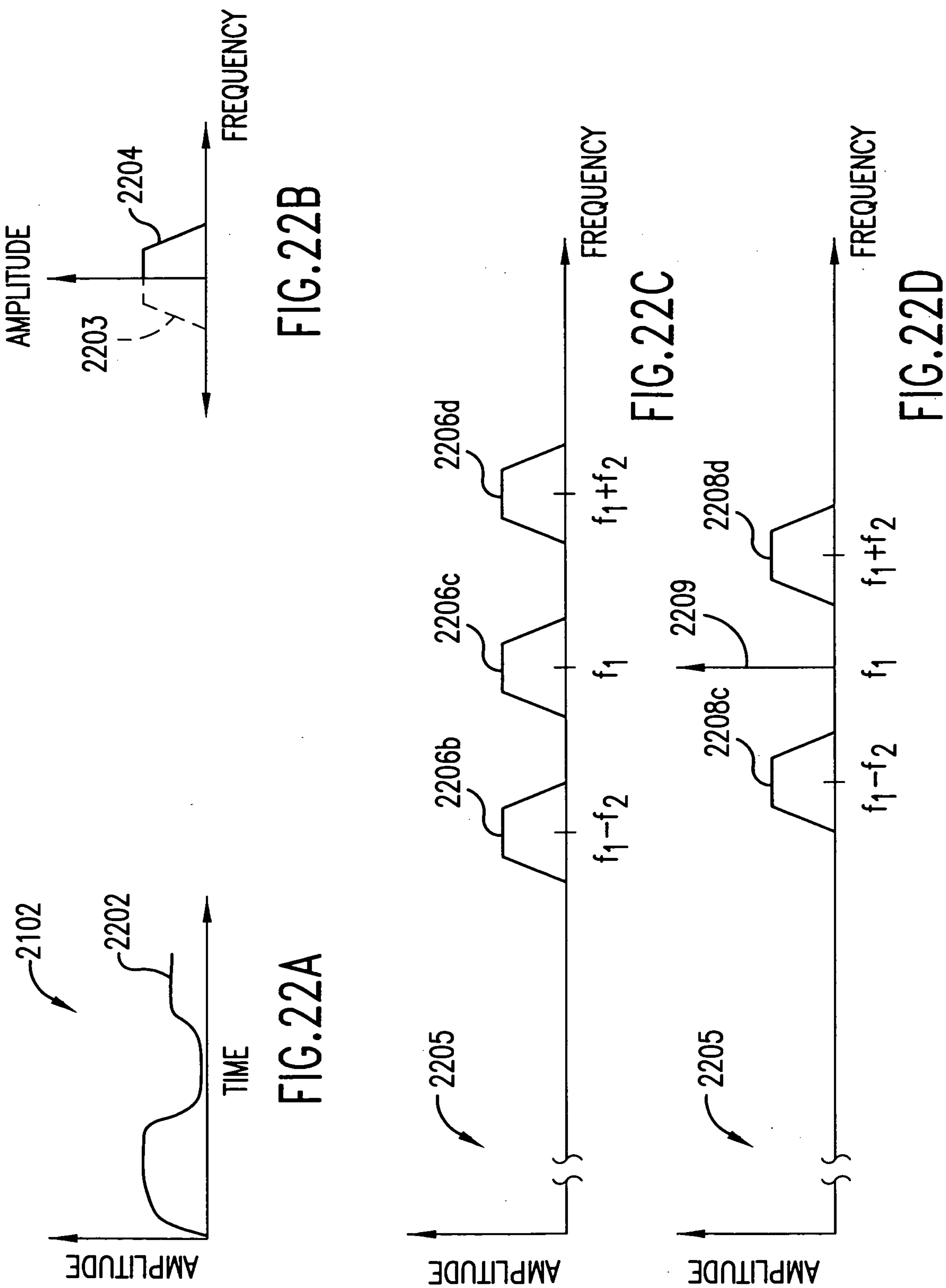

FIG.22A

FIG.22B

FIG.22C

FIG.22D

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Inventors: Sorrells et al.
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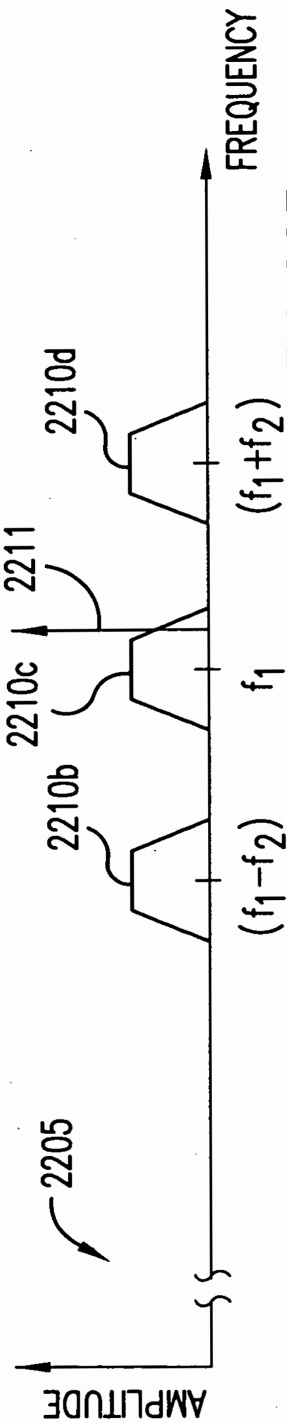

FIG.22E

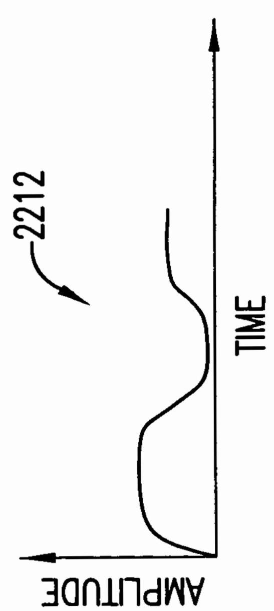

FIG.22F

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Inventors: Sorrells et al.
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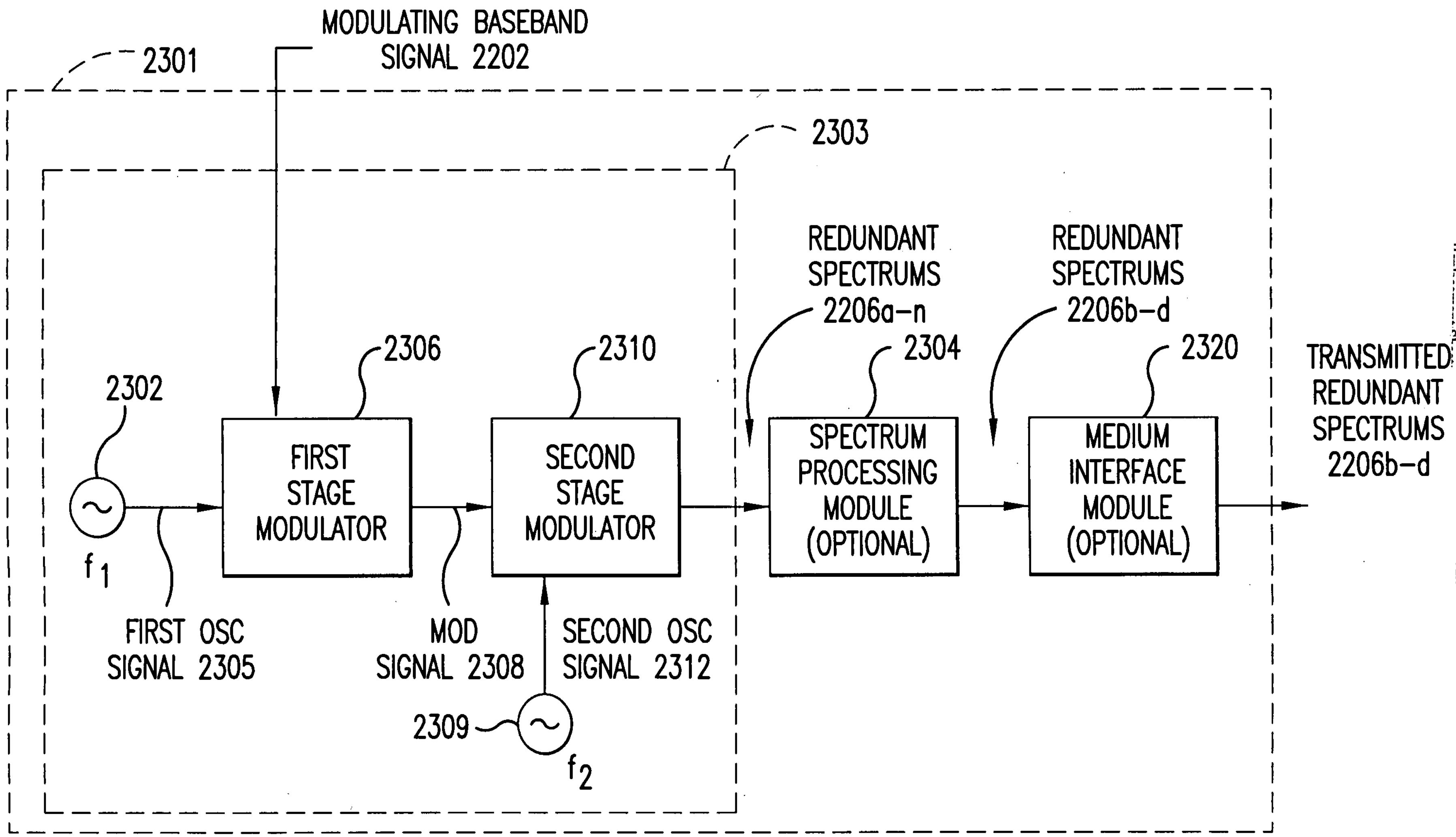

FIG.23A

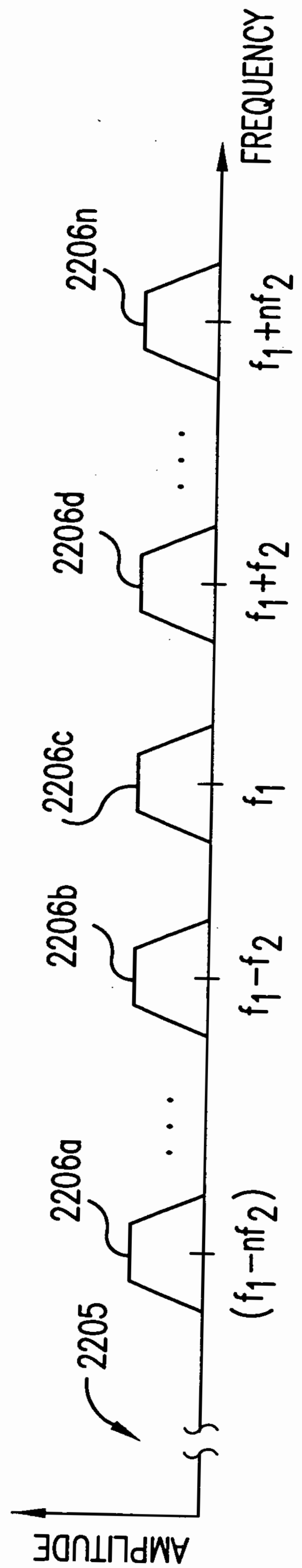

FIG.23B

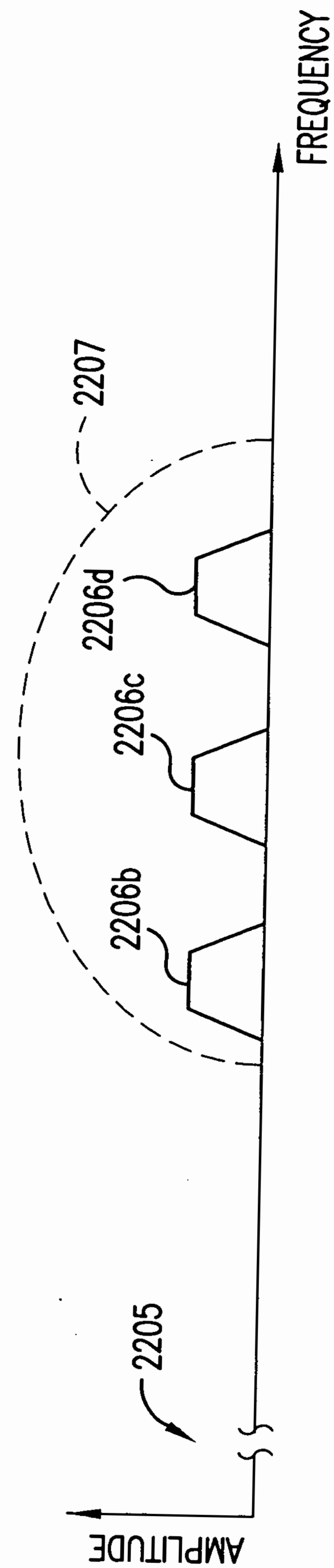

FIG.23C

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Inventors: Sorrells et al.
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For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
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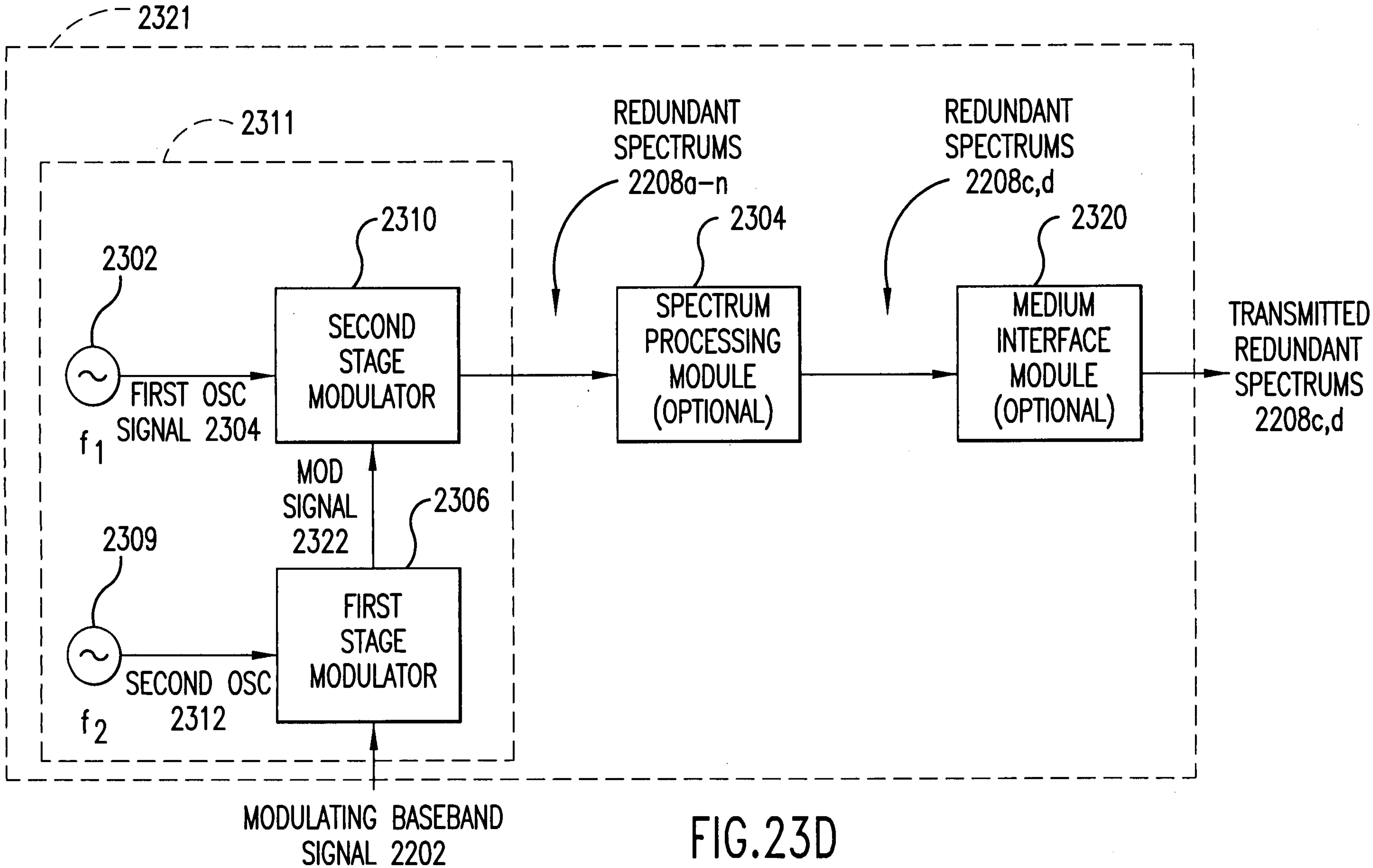

FIG.23D

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Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

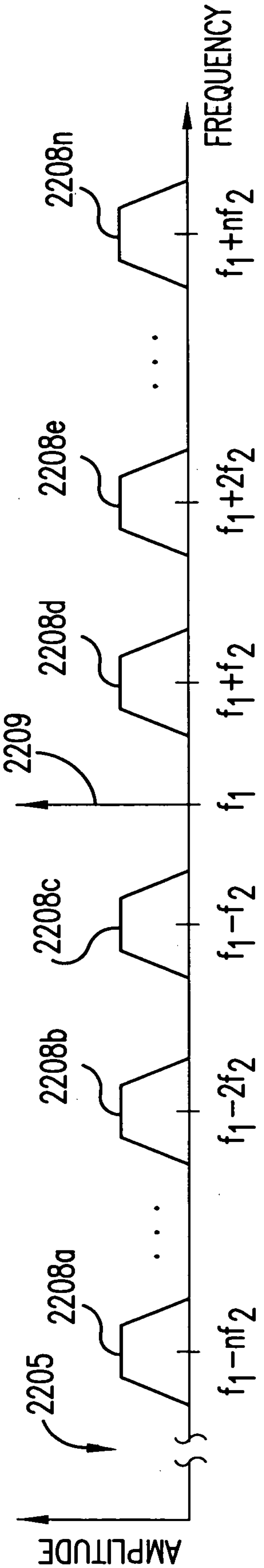

FIG.23E

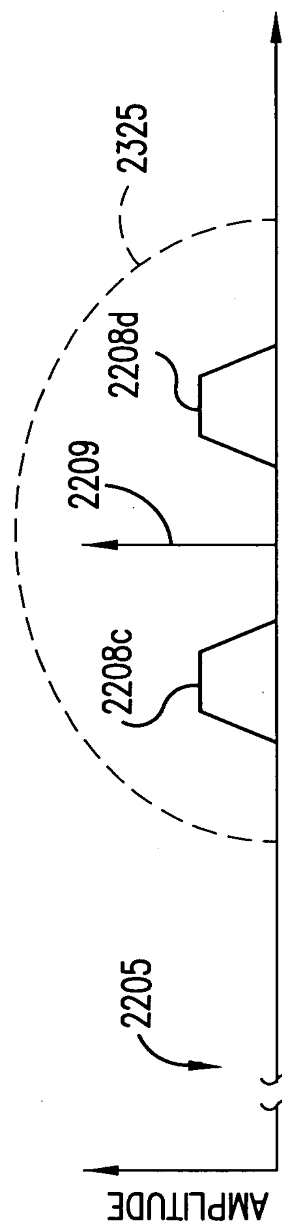

FIG.23F

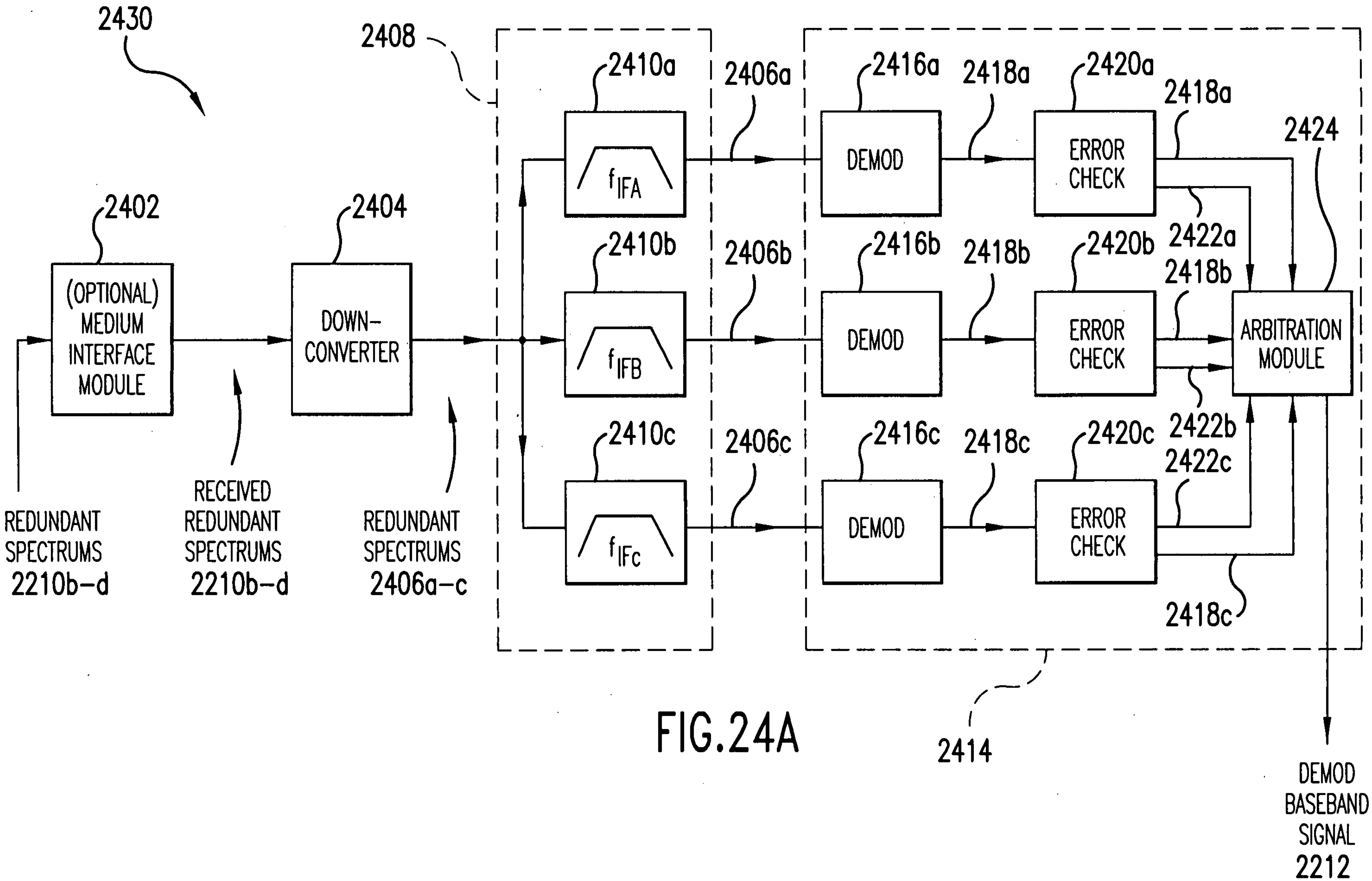

FIG.24A

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Inventors: Sorrells et al.
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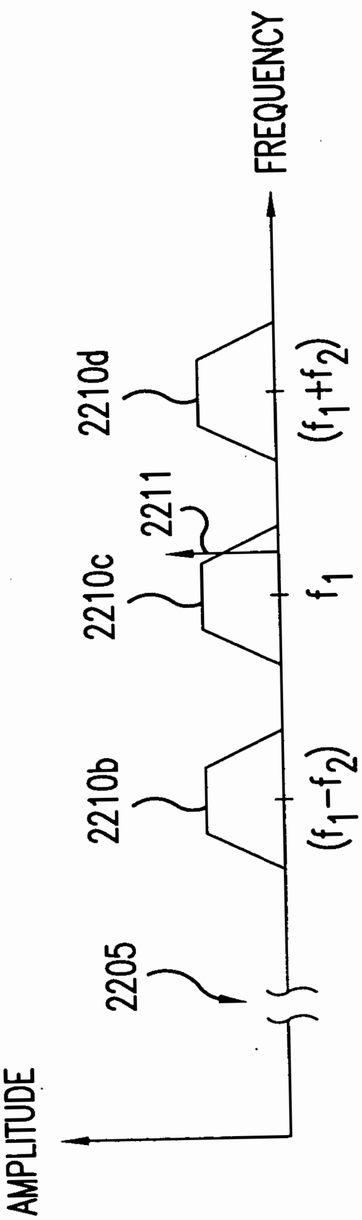

FIG.24B

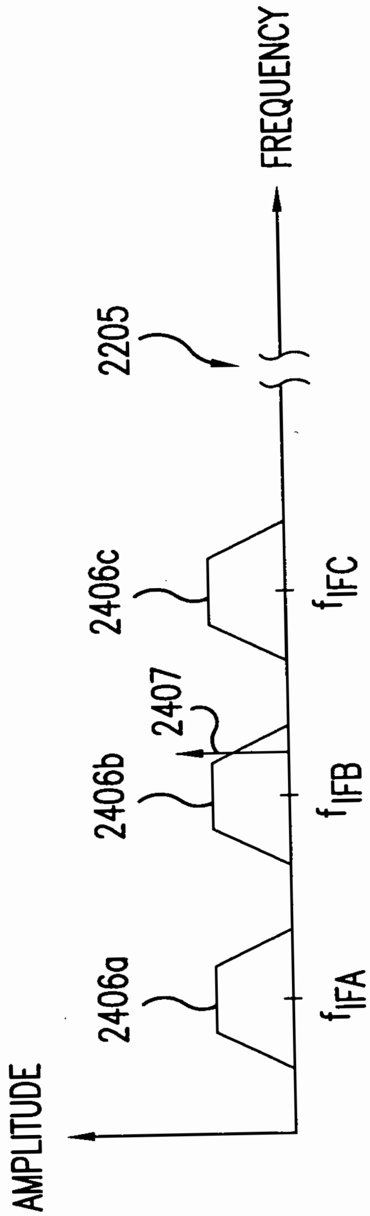

FIG.24C

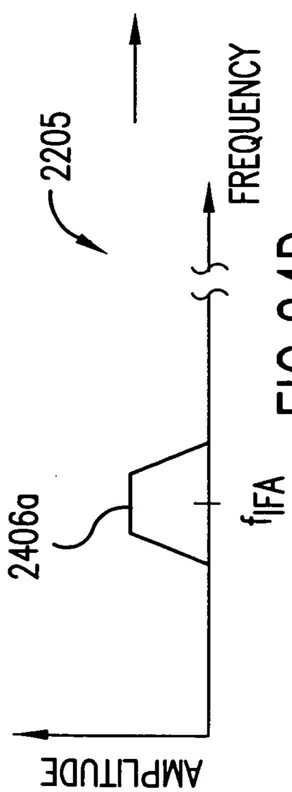

FIG.24D

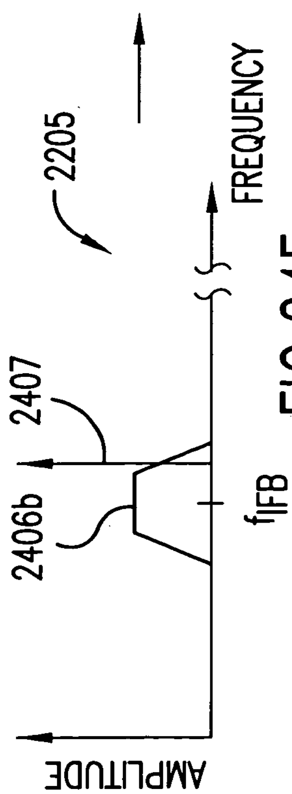

FIG.24E

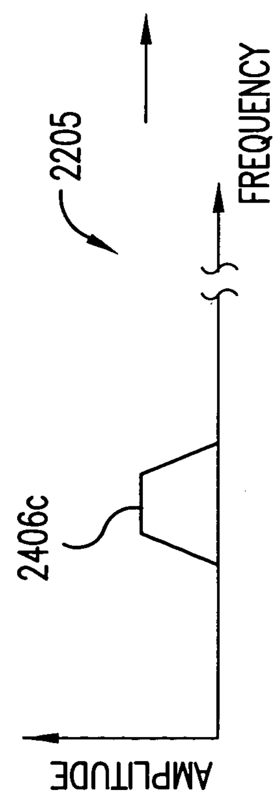

FIG.24F

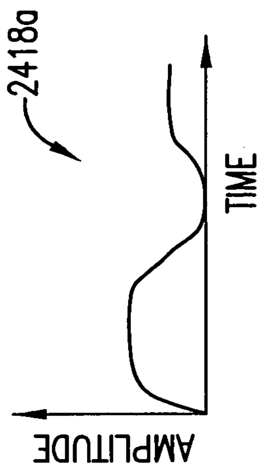

FIG.24G

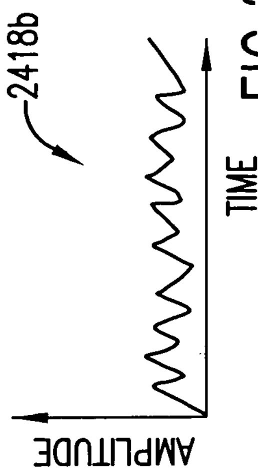

FIG.24H

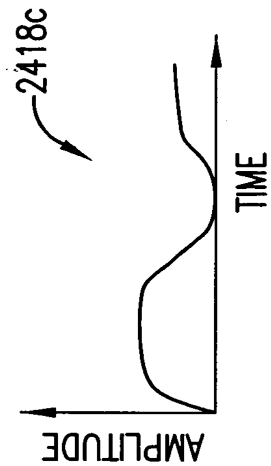

FIG.24I

Replacement Sheet
Sheet 32 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

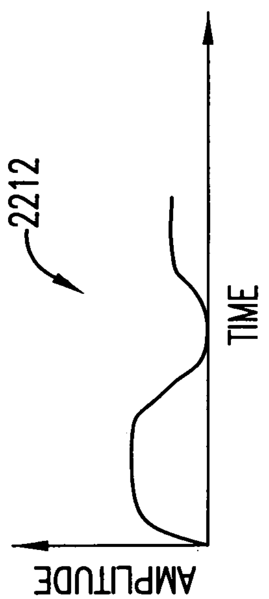

FIG. 24J

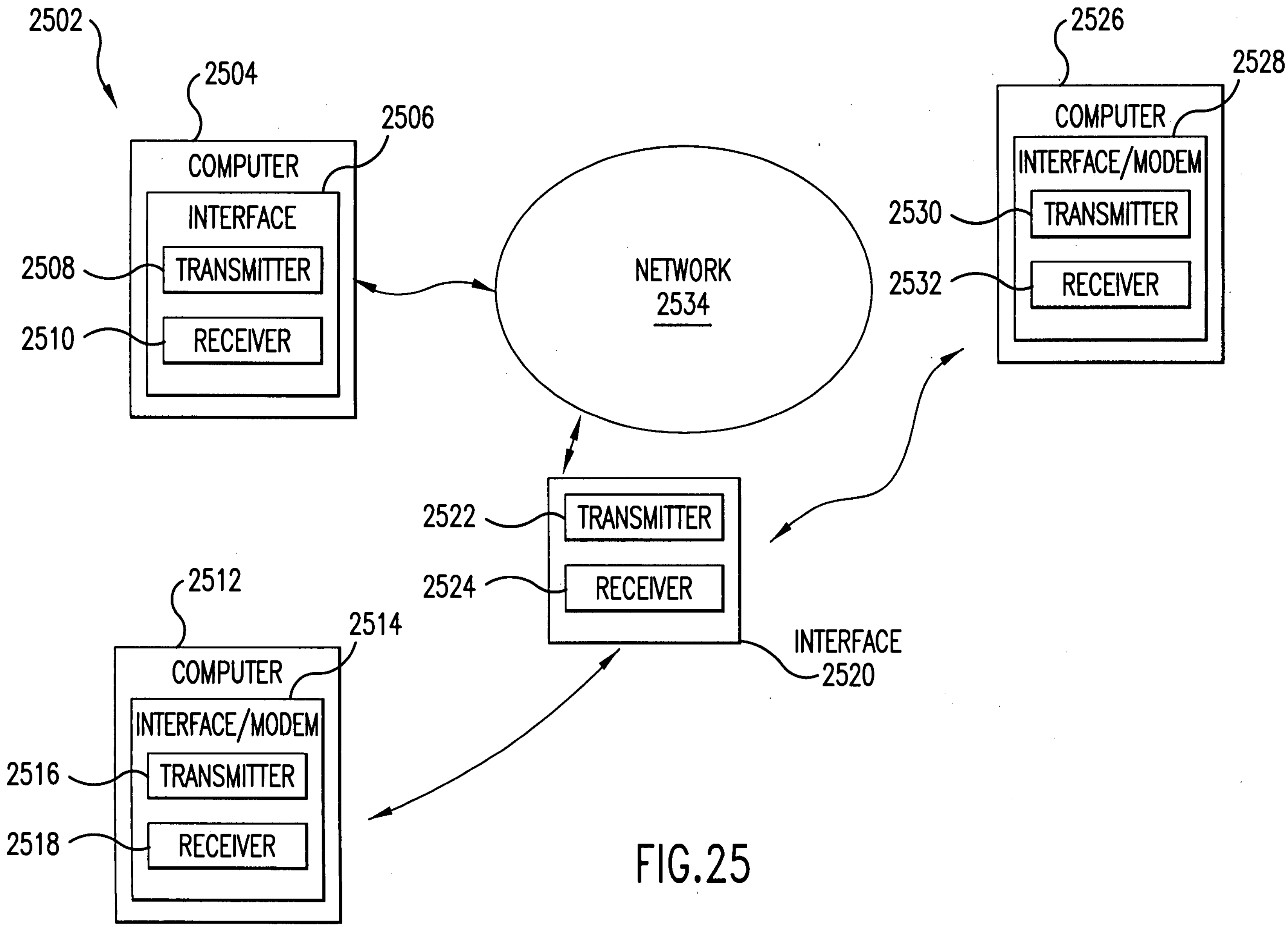

FIG.25

Replacement Sheet
Sheet 33 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

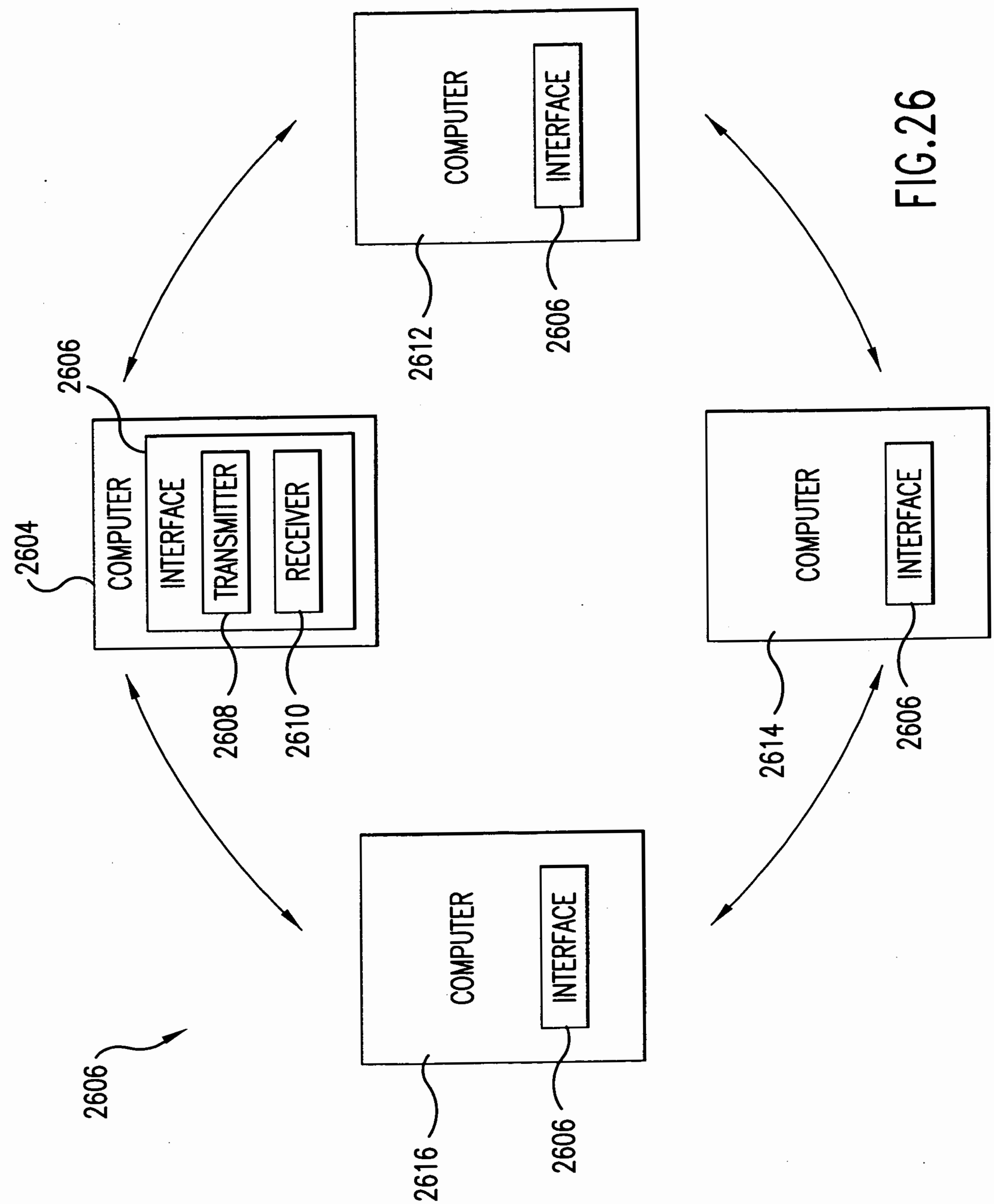
COMPUTER
INTERFACE
2612
2606
2606
2604
COMPUTER
INTERFACE
TRANSMITTER
RECEIVER
2608
2610
COMPUTER
INTERFACE
2614
2606
COMPUTER
INTERFACE
2616
2606
2606

FIG.26

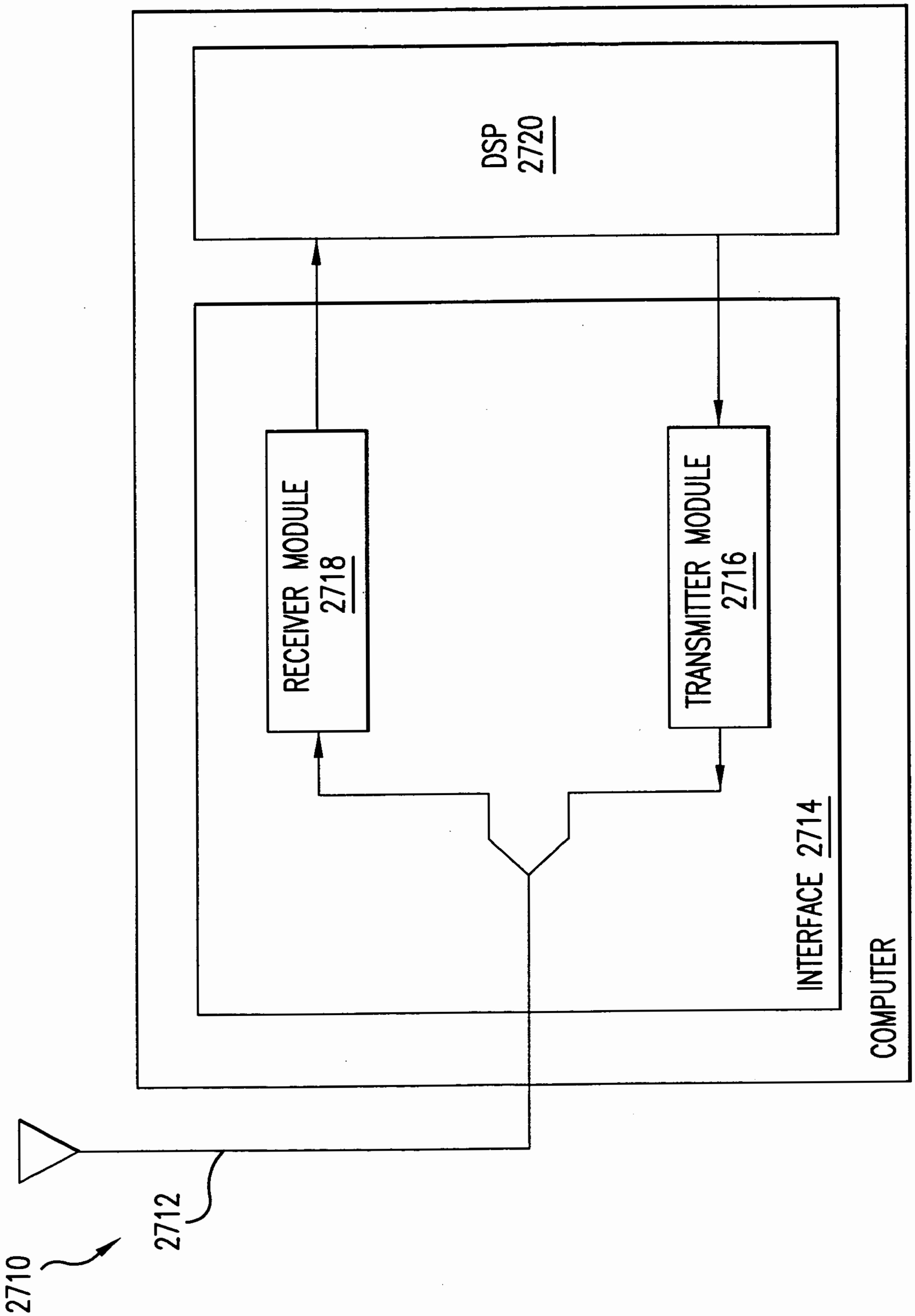
DSP
2720
RECEIVER MODULE
2718
TRANSMITTER MODULE
2716
INTERFACE 2714
COMPUTER
2712
2710

FIG.27

Replacement Sheet
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Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

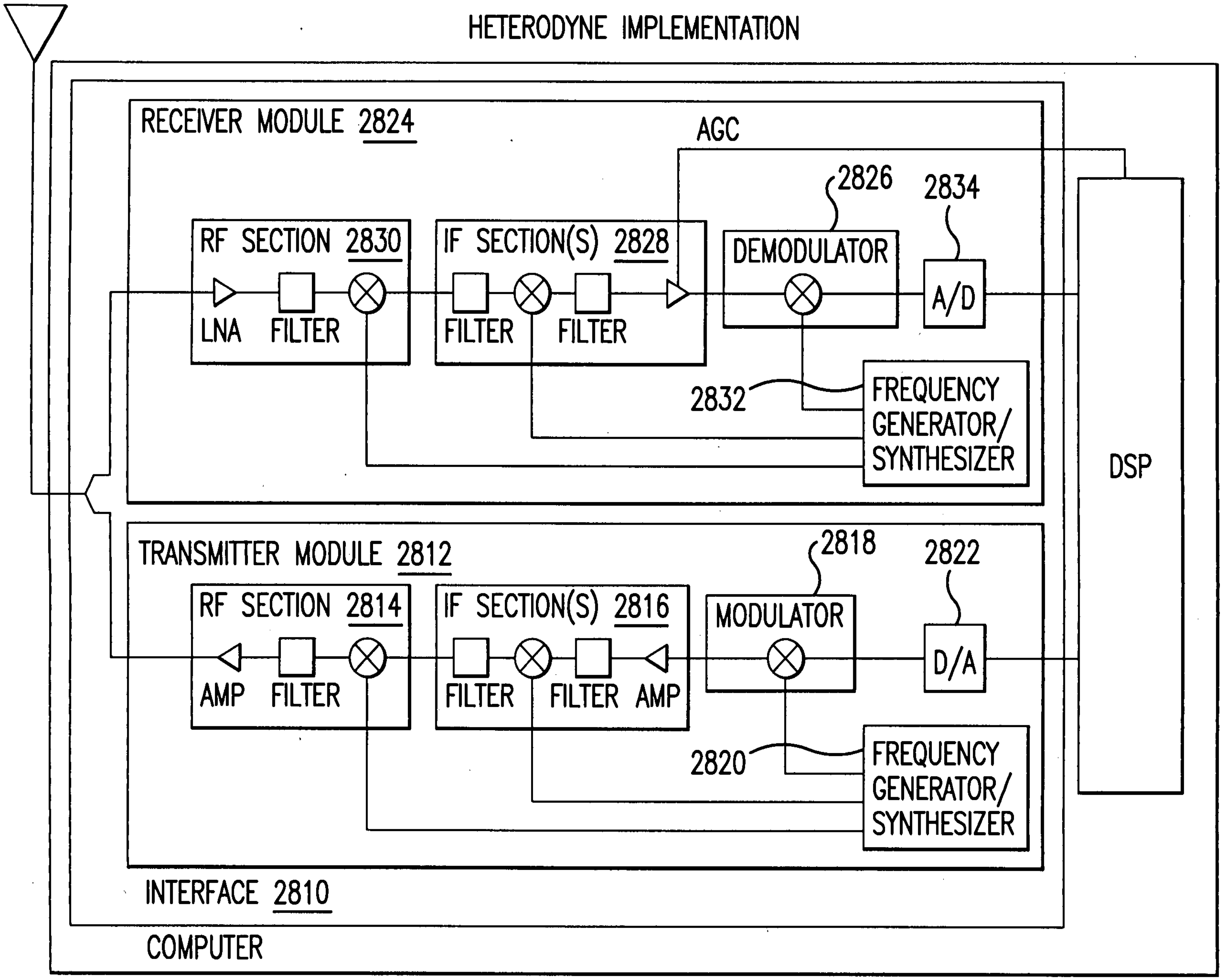
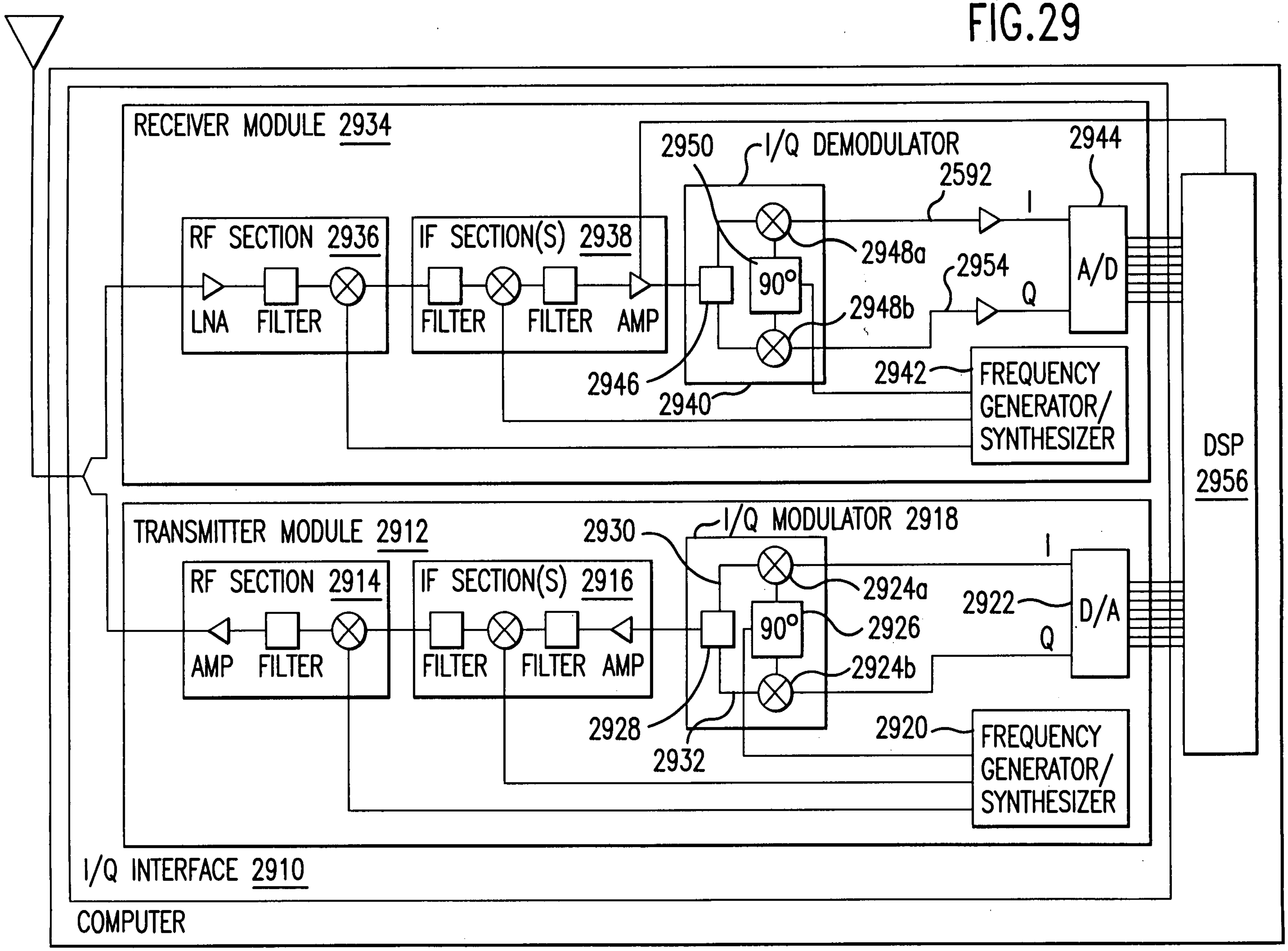


FIG.28

Replacement Sheet
Sheet 37 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

FIG.29



Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

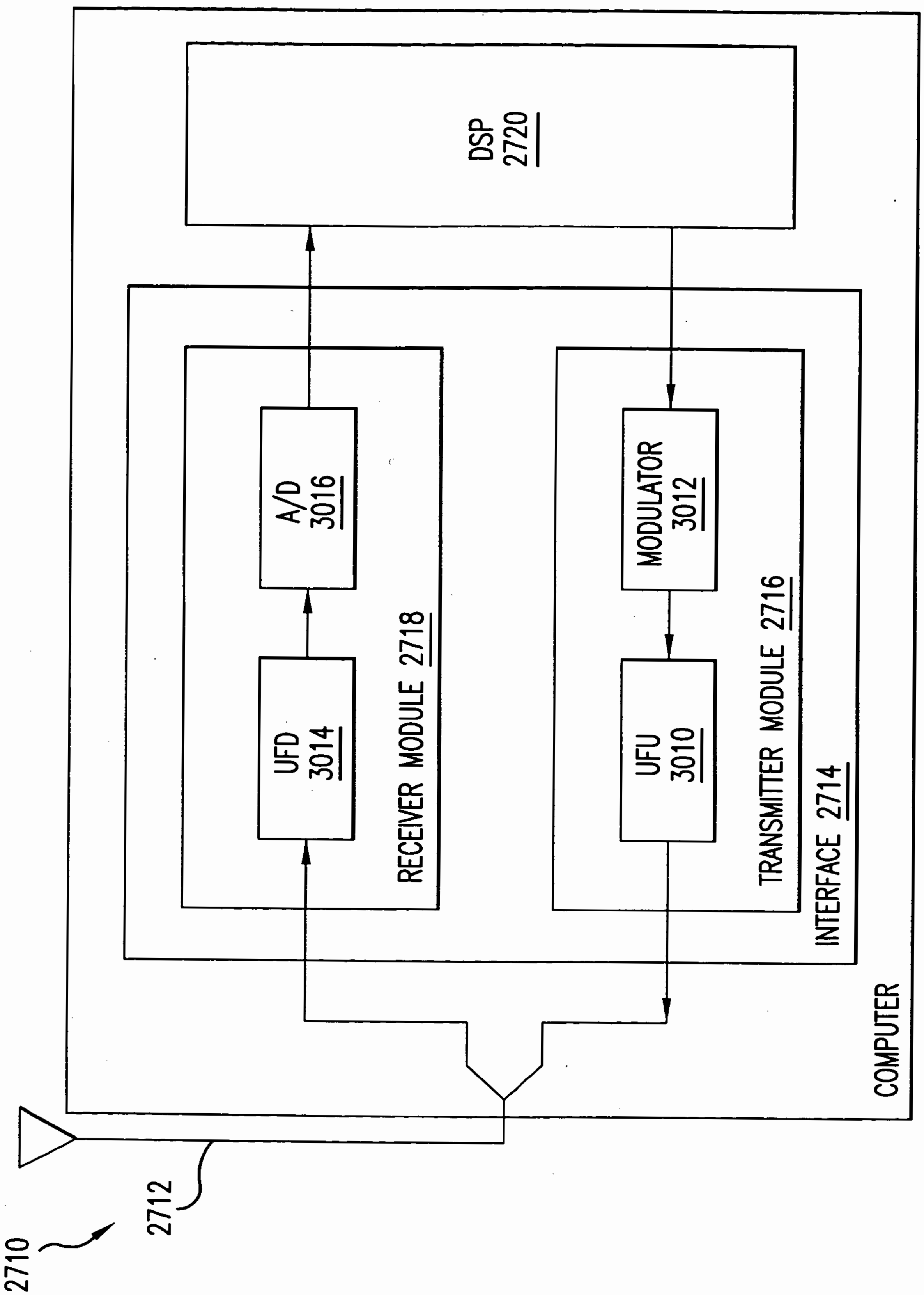


FIG.30

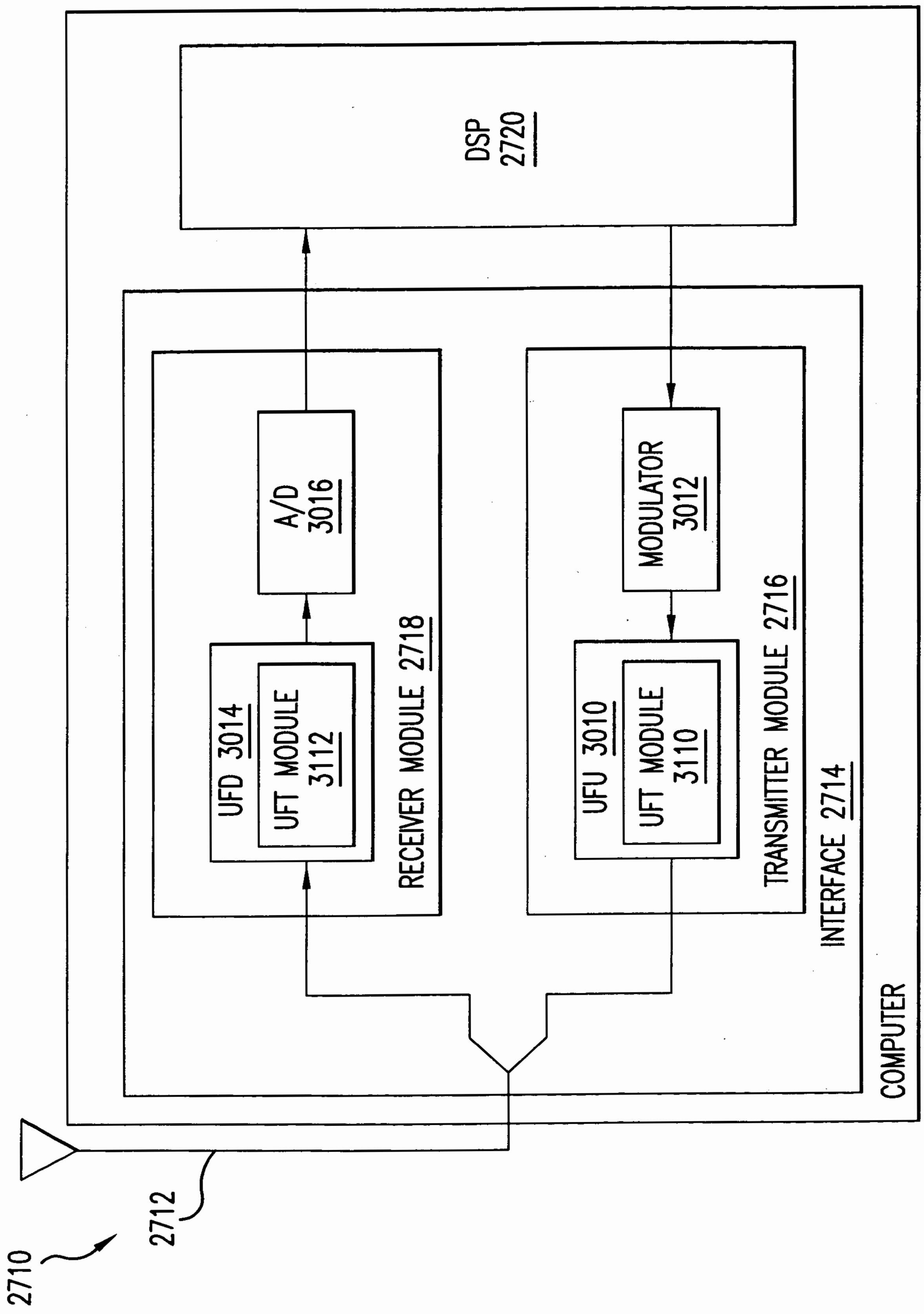

DSP
2720
A/D
3016
MODULATOR
3012
UFD 3014
UFT MODULE
3112
RECEIVER MODULE 2718
UFU 3010
UFT MODULE
3110
TRANSMITTER MODULE 2716
INTERFACE 2714
COMPUTER
2712
2710

FIG.31

Replacement Sheet
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Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

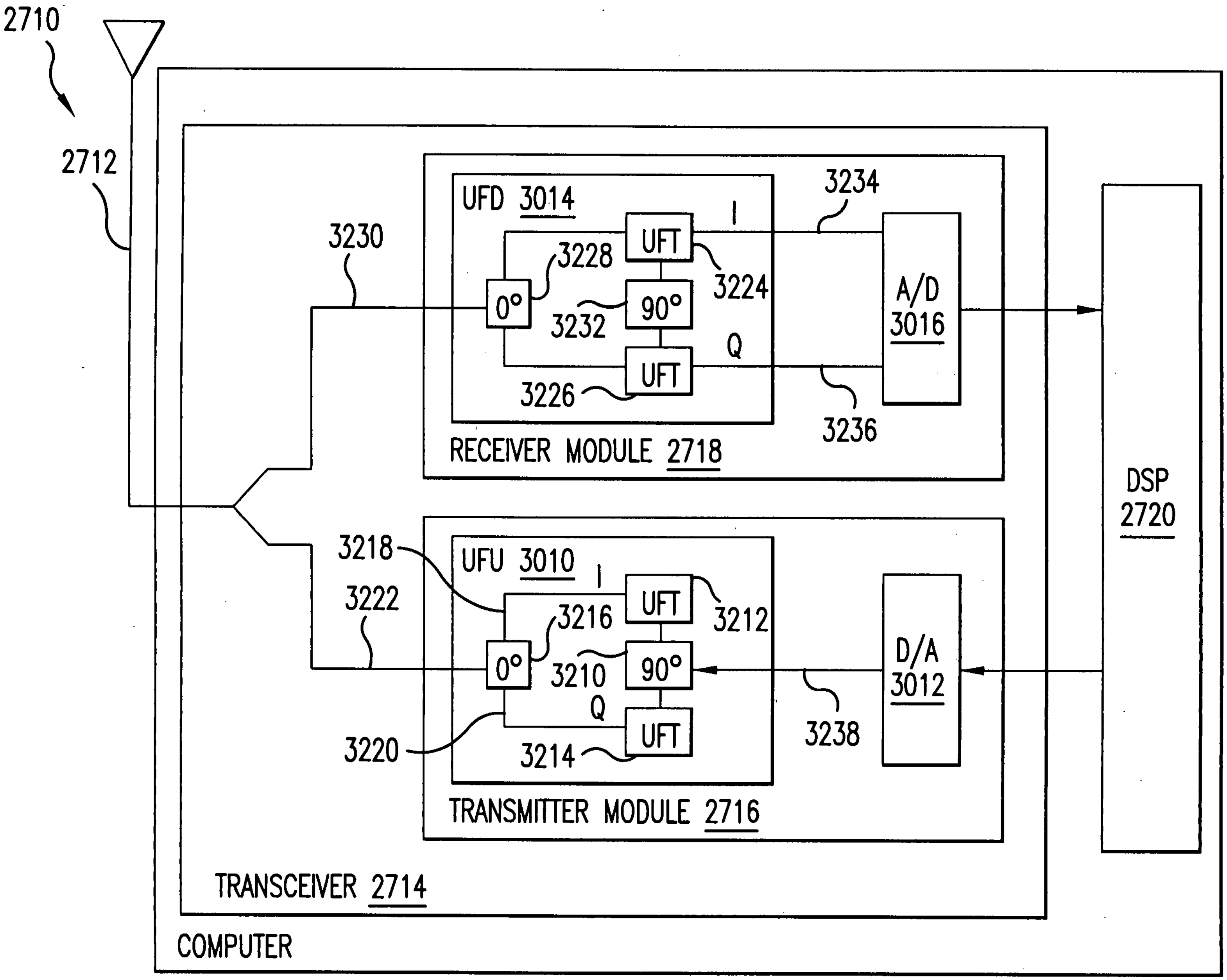

FIG.32

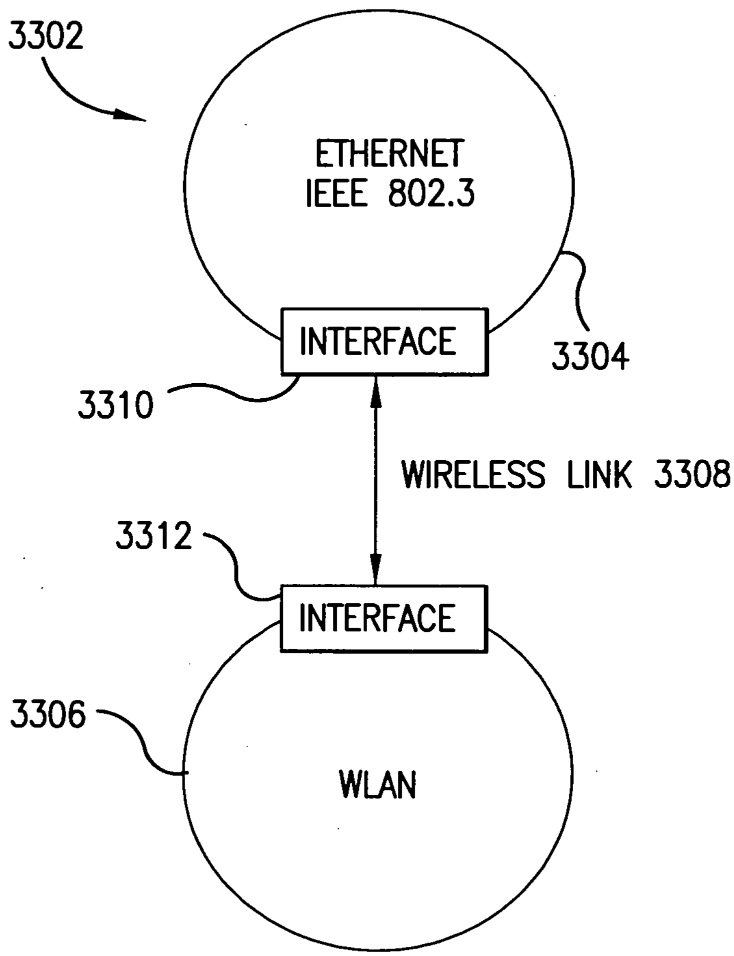
3302
ETHERNET
IEEE 802.3
3304
INTERFACE
3310
WIRELESS LINK 3308
3312
INTERFACE
3306
WLAN

FIG.33

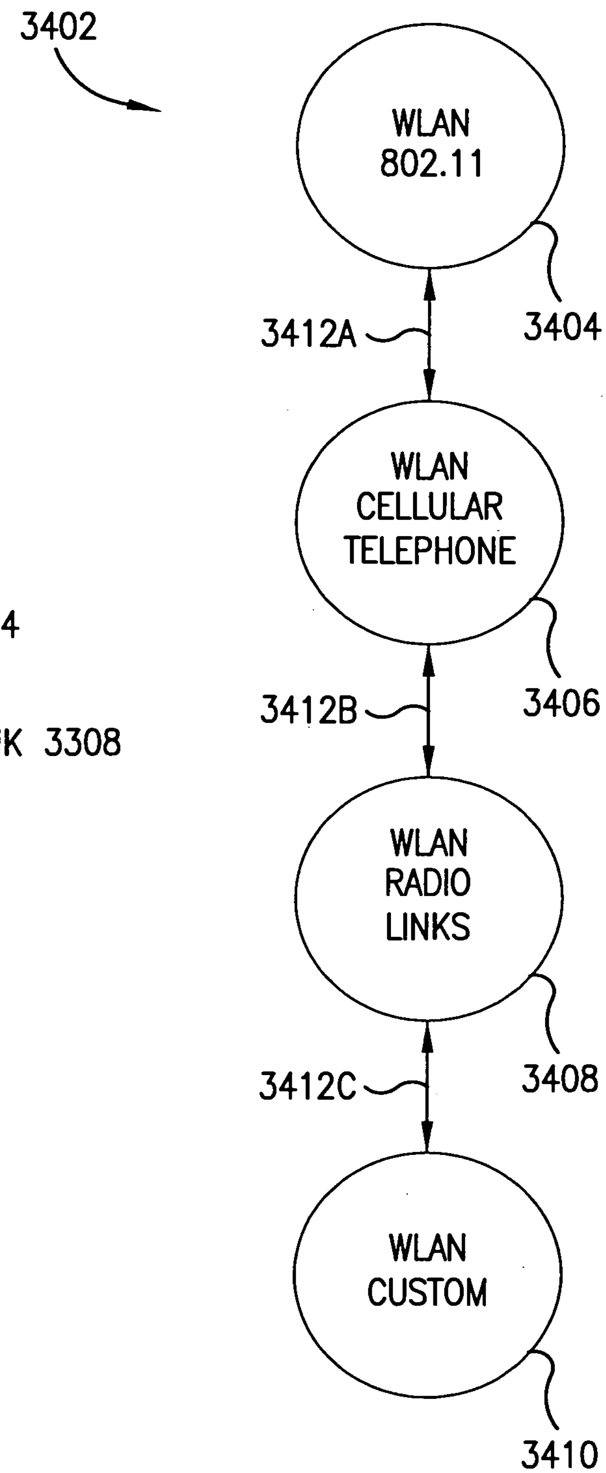
3402
WLAN
802.11
3404
3412A
WLAN
CELLULAR
TELEPHONE
3406
3412B
WLAN
RADIO
LINKS
3408
3412C
WLAN
CUSTOM
3410

FIG.34

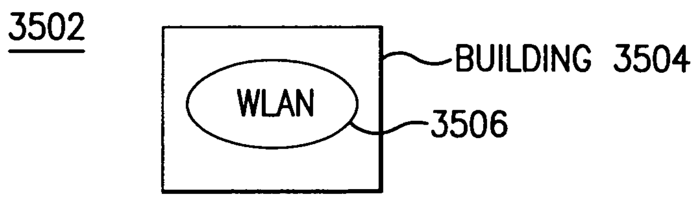

FIG.35

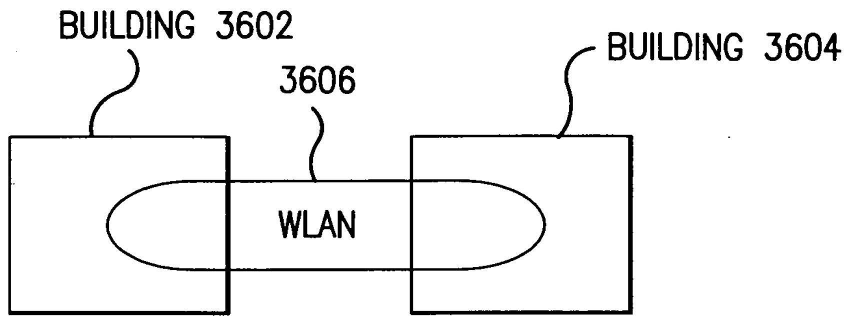

FIG.36

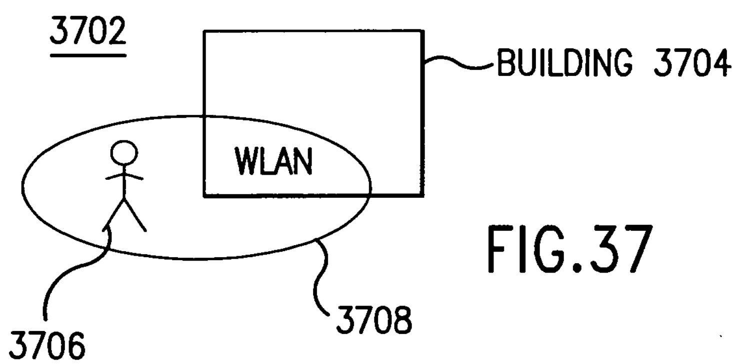

FIG.37

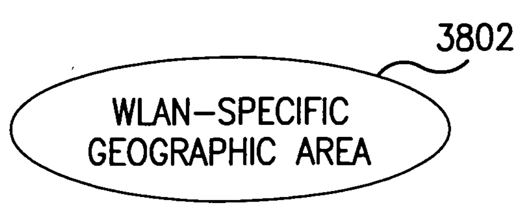

FIG.38

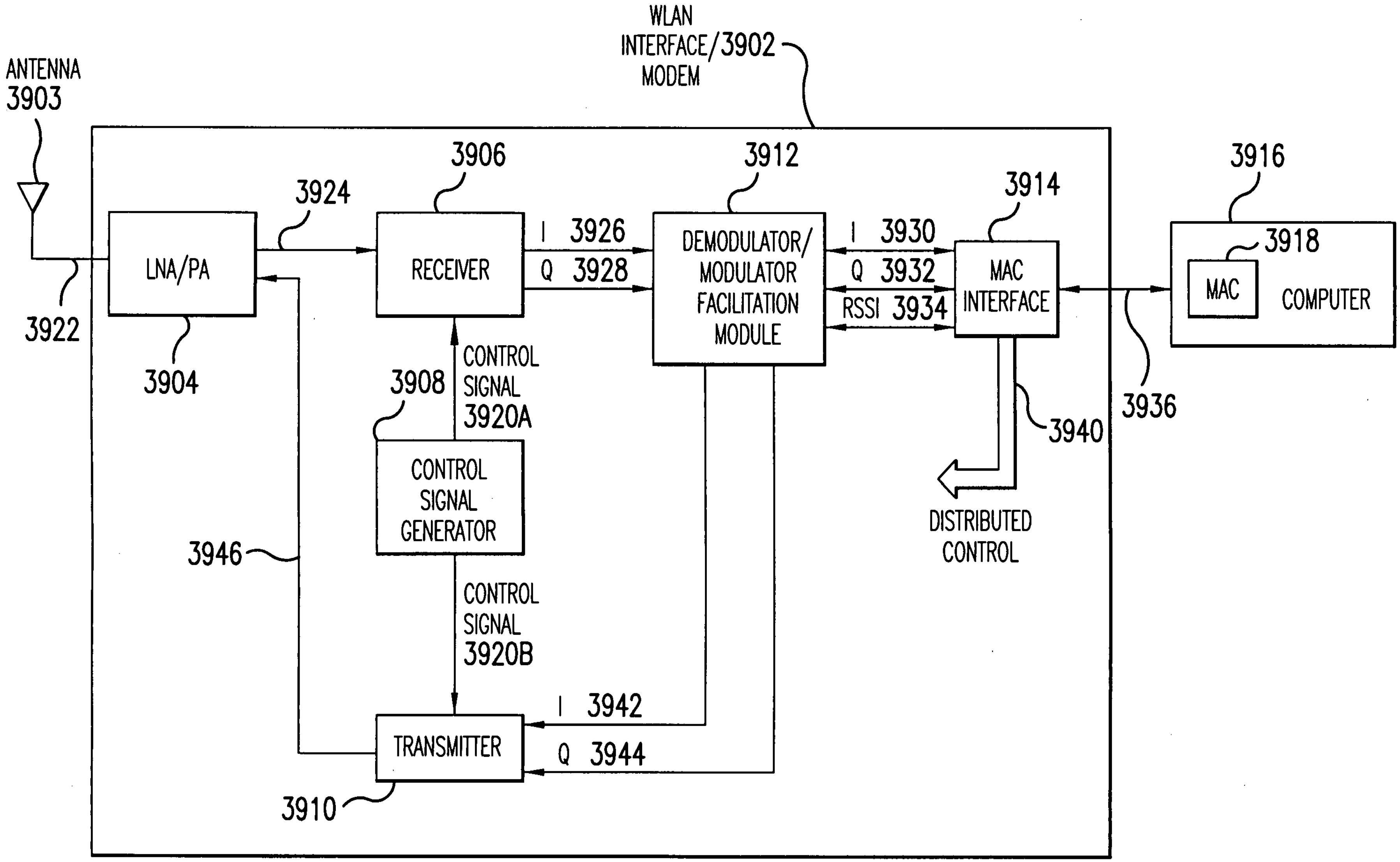

FIG.39

Replacement Sheet
Sheet 43 of 349
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Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

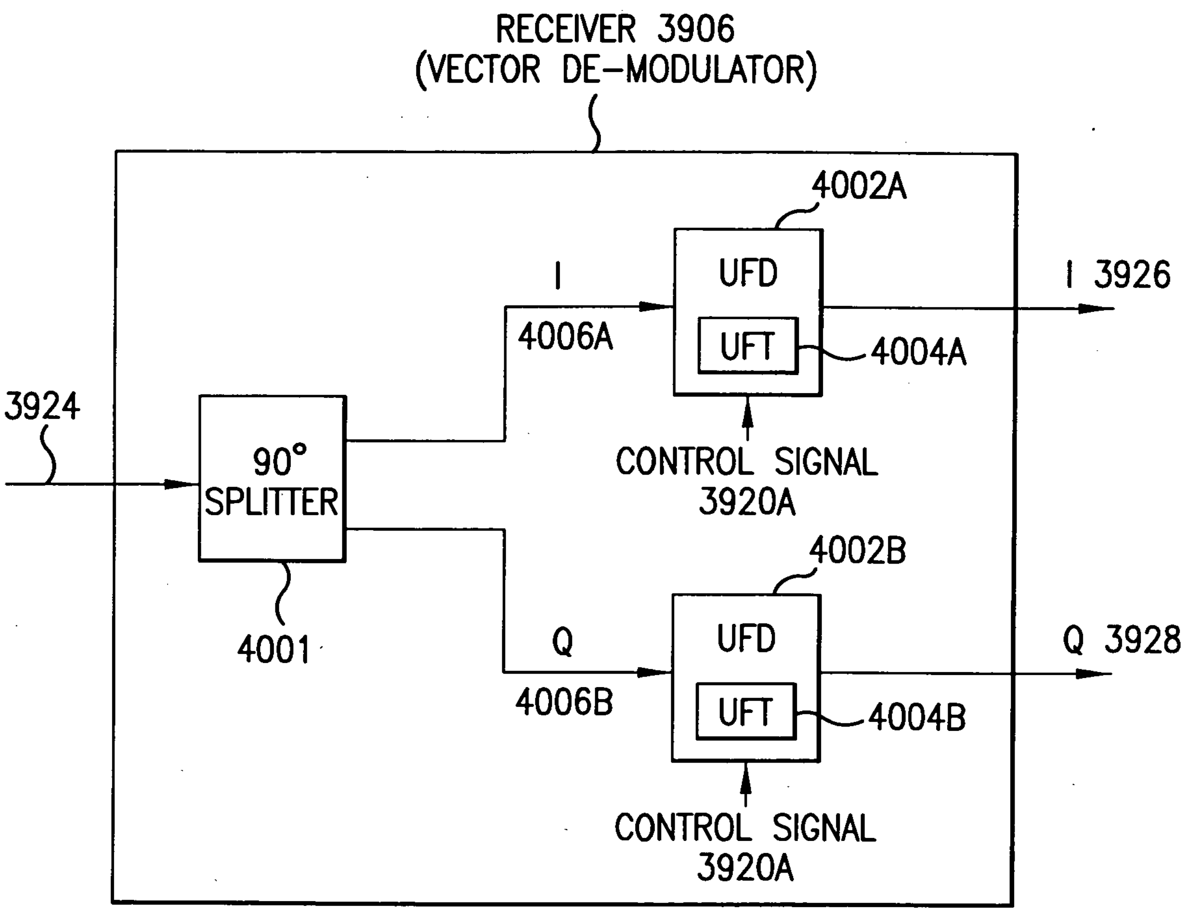
RECEIVER 3906
(VECTOR DE-MODULATOR)
3924
90°
SPLITTER
4001
I
4006A
Q
4006B
4002A
UFD
UFT
4004A
CONTROL SIGNAL
3920A
4002B
UFD
UFT
4004B
CONTROL SIGNAL
3920A
I 3926
Q 3928

FIG.40

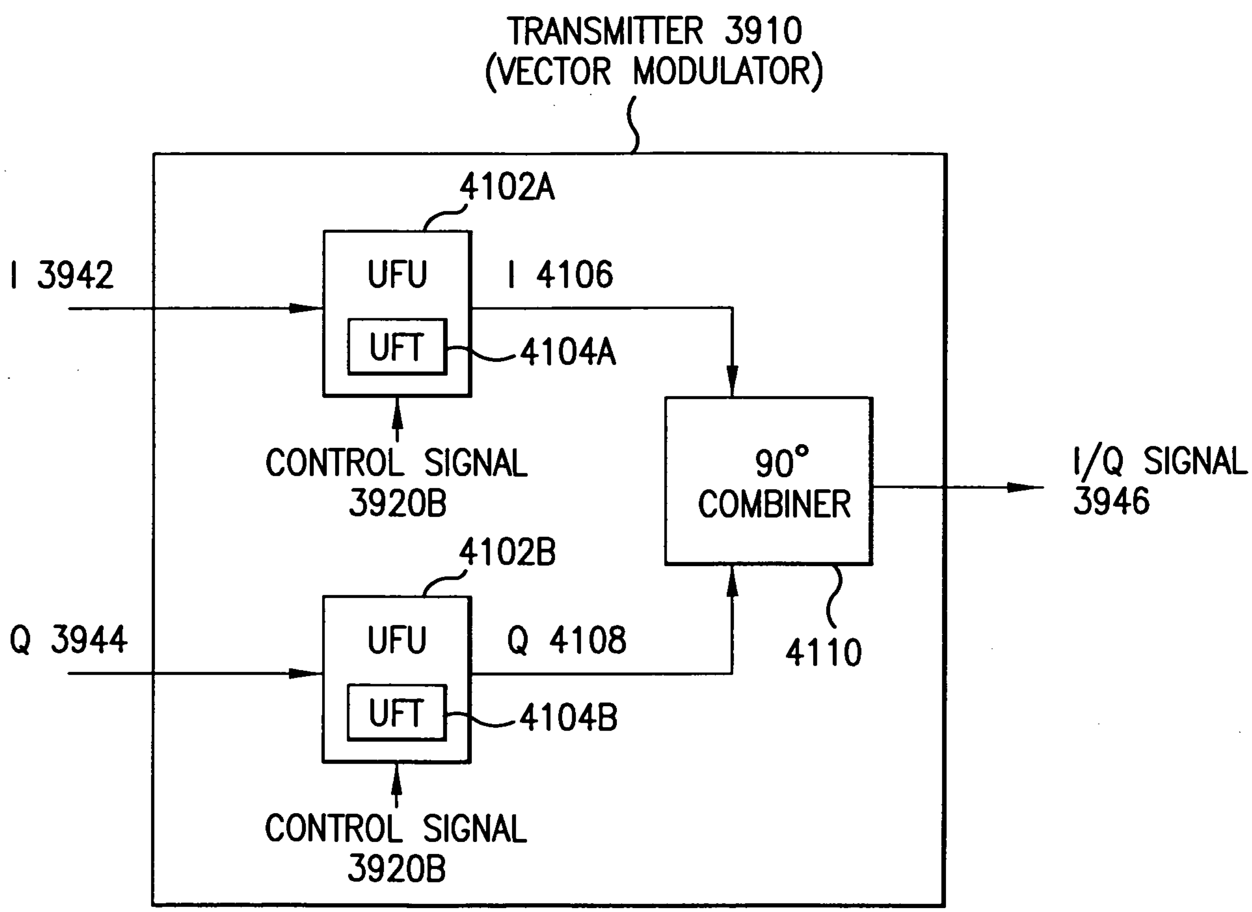
TRANSMITTER 3910
(VECTOR MODULATOR)
4102A
I 3942
UFU
UFT
I 4106
4104A
CONTROL SIGNAL
3920B
90°
COMBINER
I/Q SIGNAL
3946
4110
4102B
Q 3944
UFU
UFT
Q 4108
4104B
CONTROL SIGNAL
3920B

FIG.41

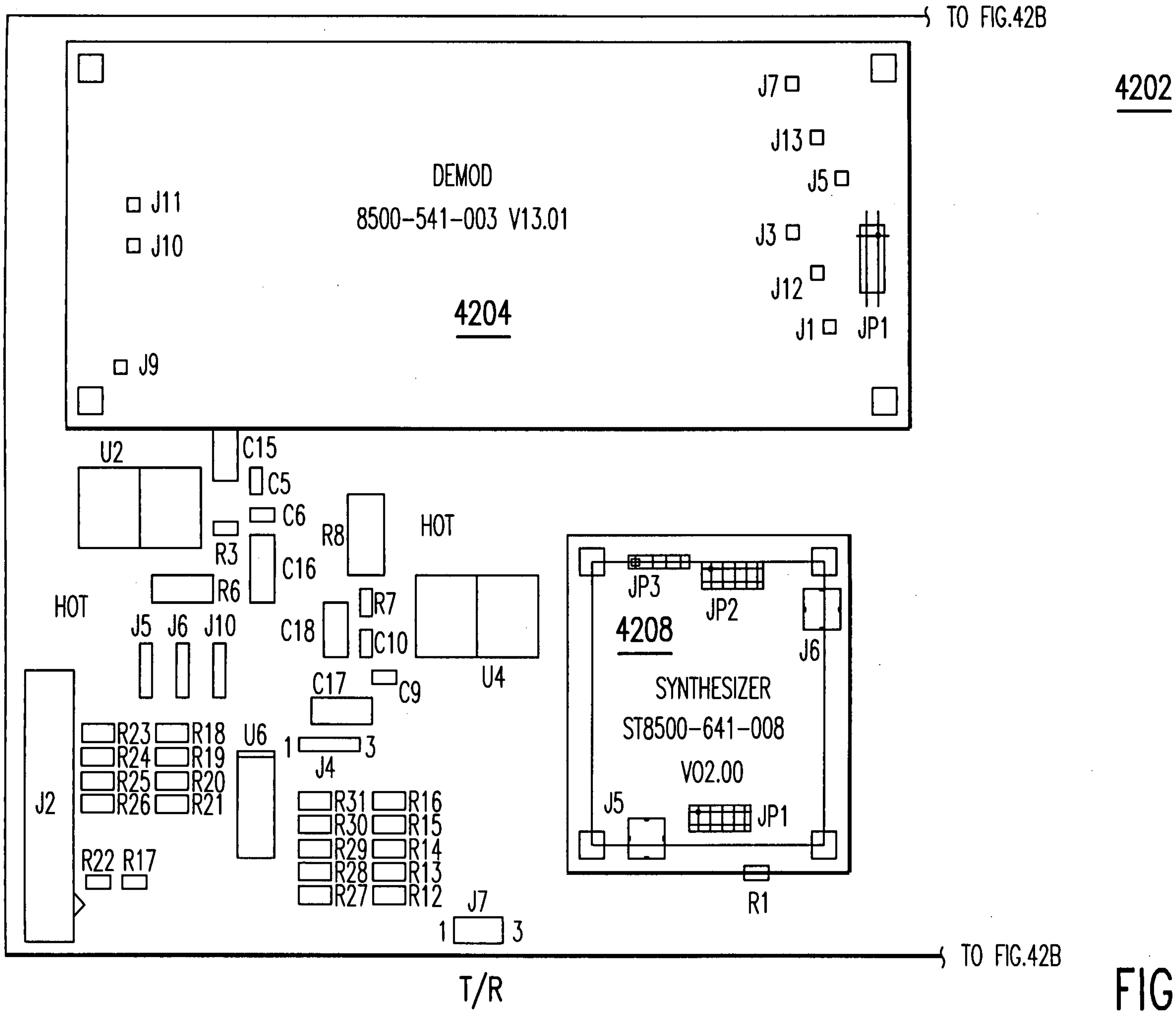

FIG.42A

Replacement Sheet
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Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

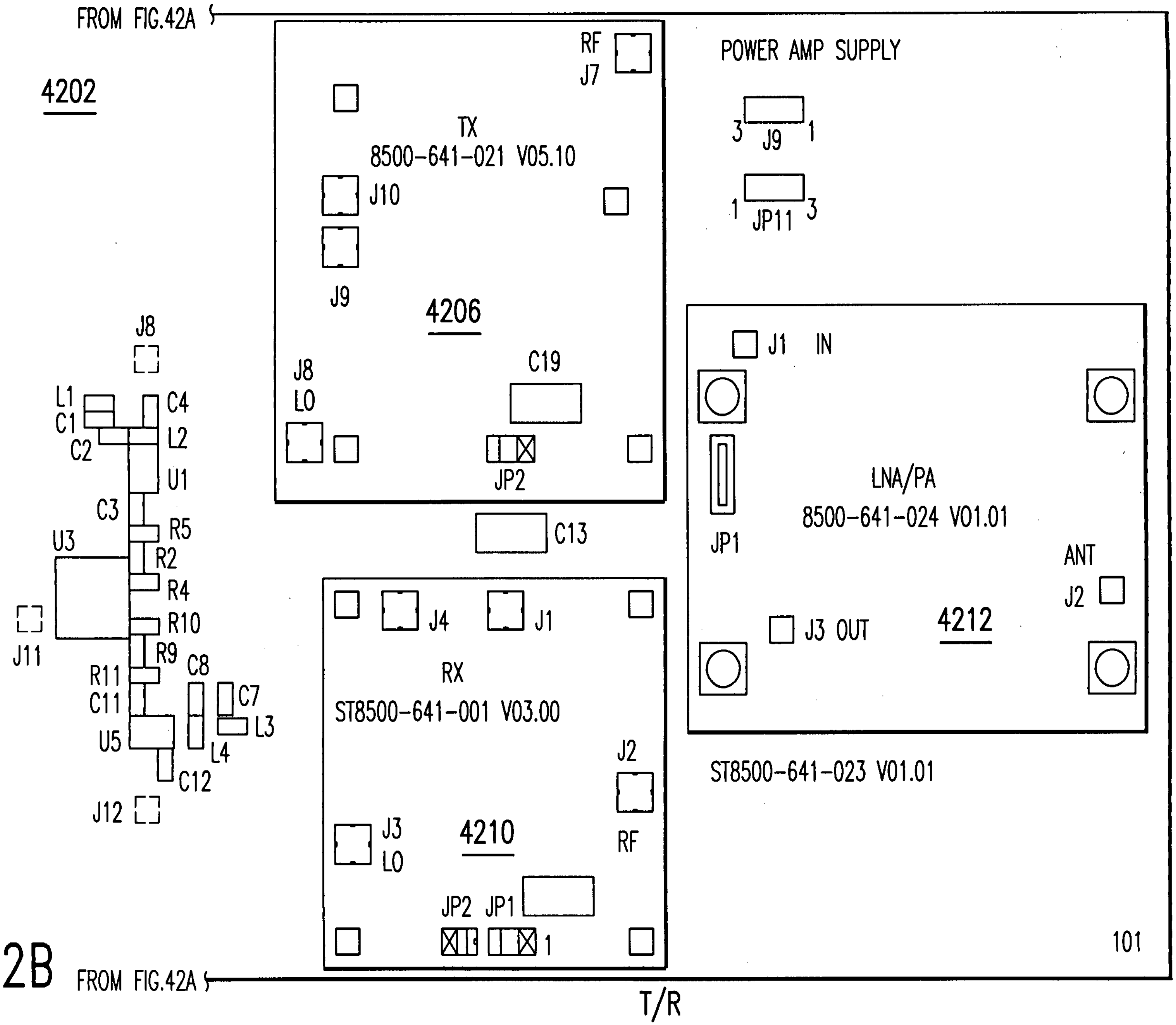

FIG.42B

New Sheet
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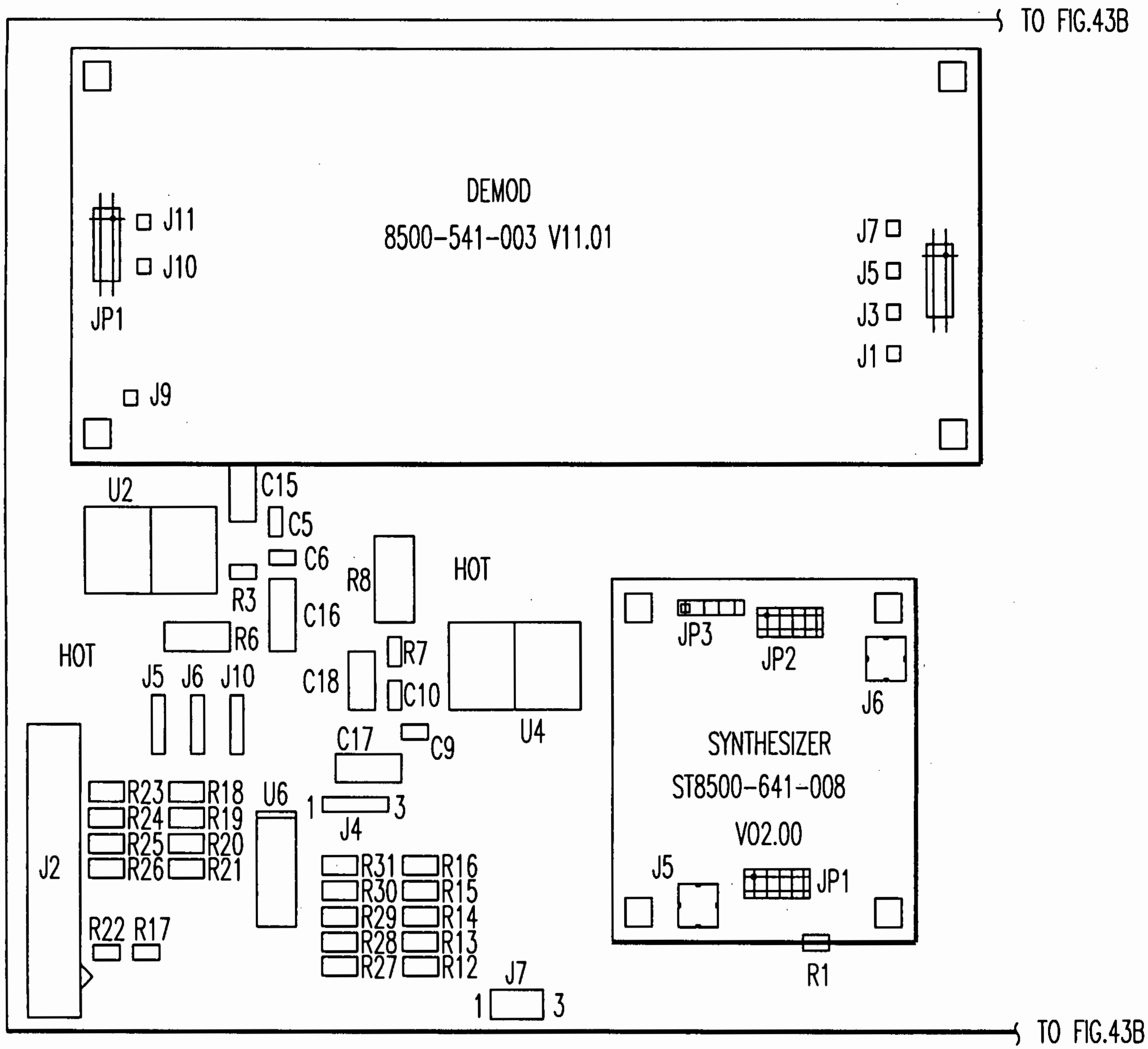
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit



RECEIVE ONLY

4302

FIG.43A

Replacement Sheet
Sheet 48 of 349
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Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

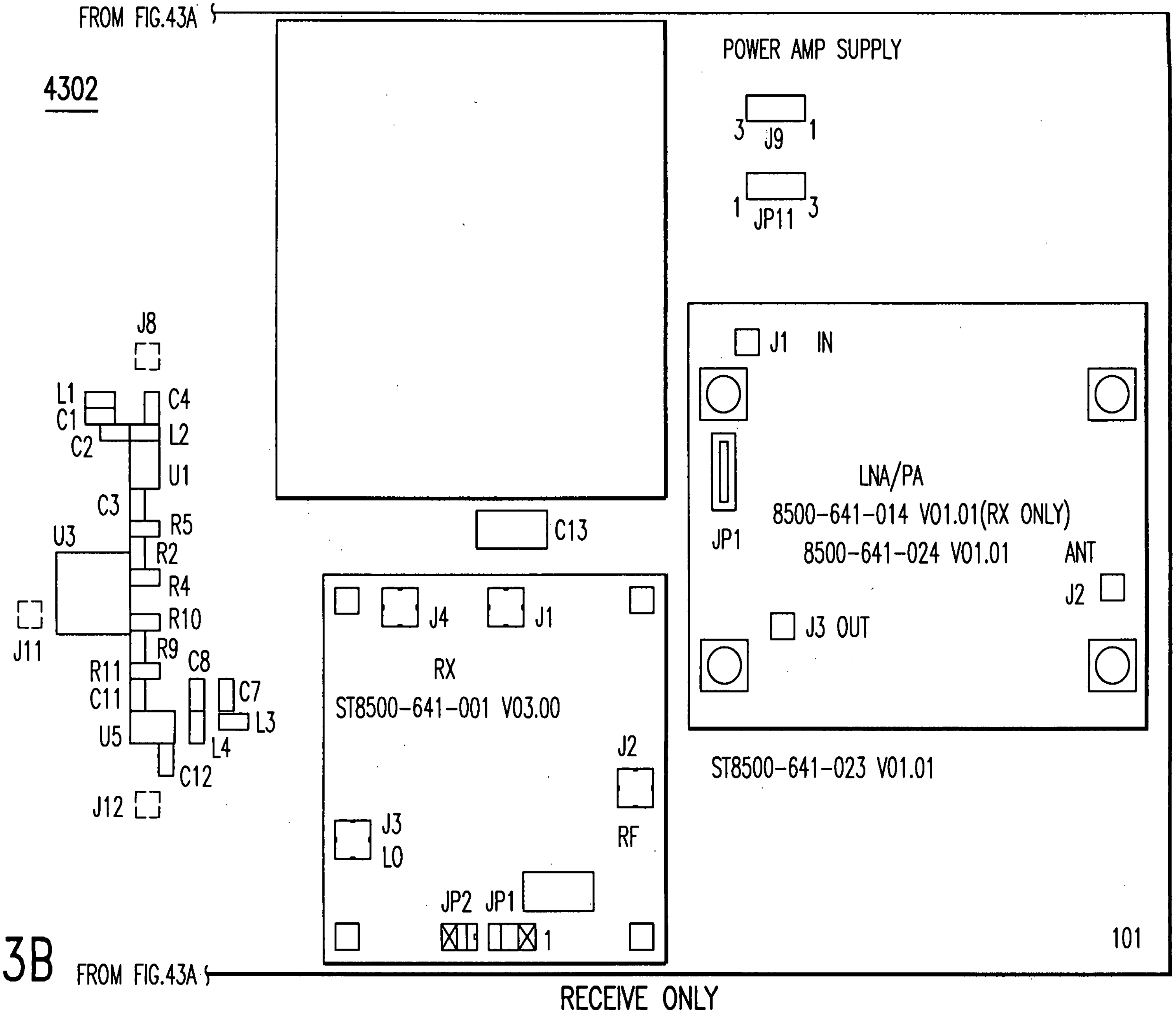

FIG.43B

New Sheet
Sheet 49 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

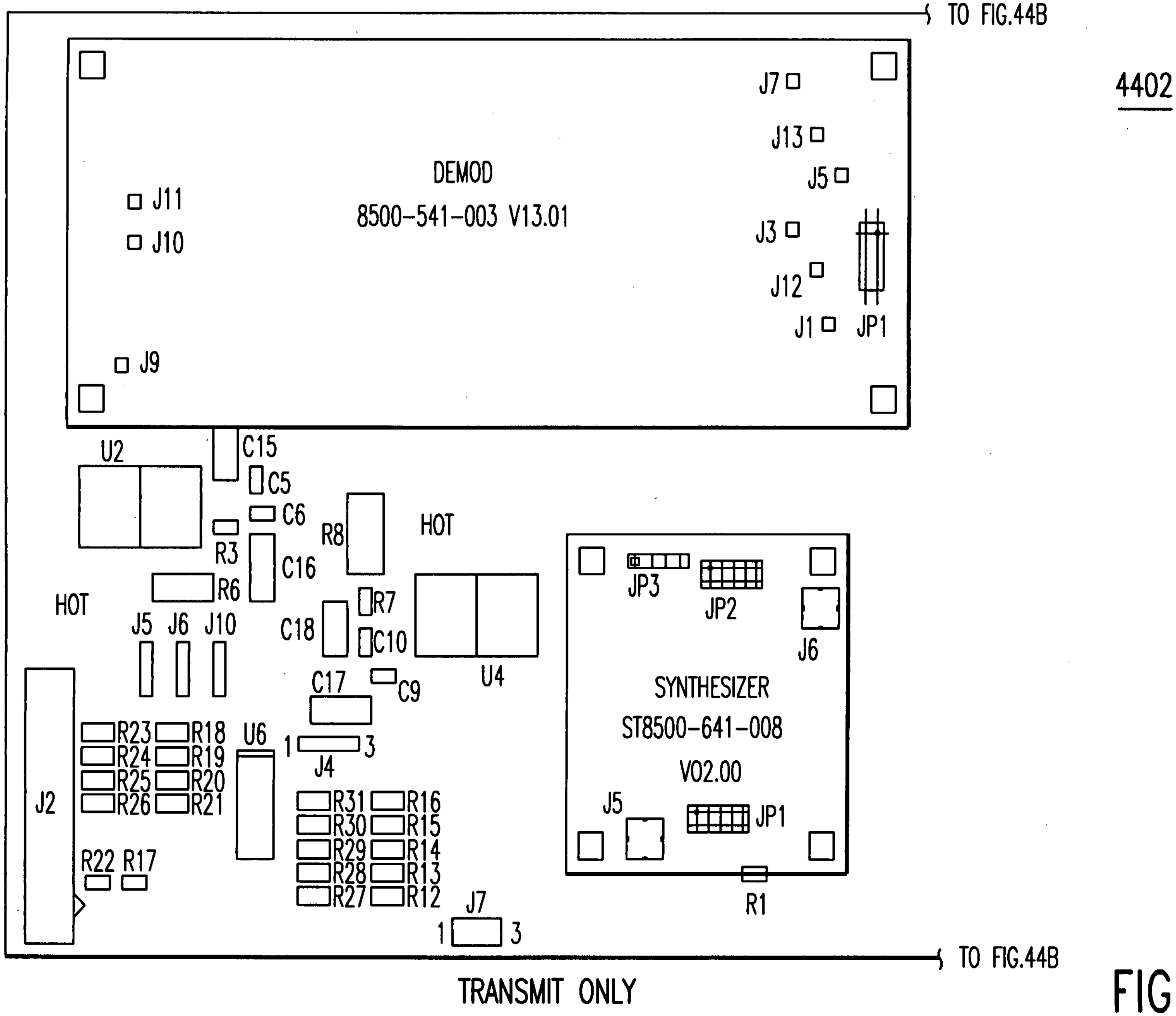
TO FIG.44B
4402
DEMOD
8500-541-003 V13.01
J7
J13
J5
J3
J12
J1
JP1
J11
J10
J9
U2
C15
C5
C6
R8
HOT
R3
C16
R6
HOT
J5 J6 J10
C18
R7
C10
U4
C17
C9
SYNTHESIZER
ST8500-641-008
V02.00
JP3
JP2
J6
J5
JP1
R1
J2
R23 R18
R24 R19
R25 R20
R26 R21
U6
1 J4 3
R31 R16
R30 R15
R29 R14
R28 R13
R27 R12
R22 R17
J7
1 3
TO FIG.44B
TRANSMIT ONLY

FIG.44A

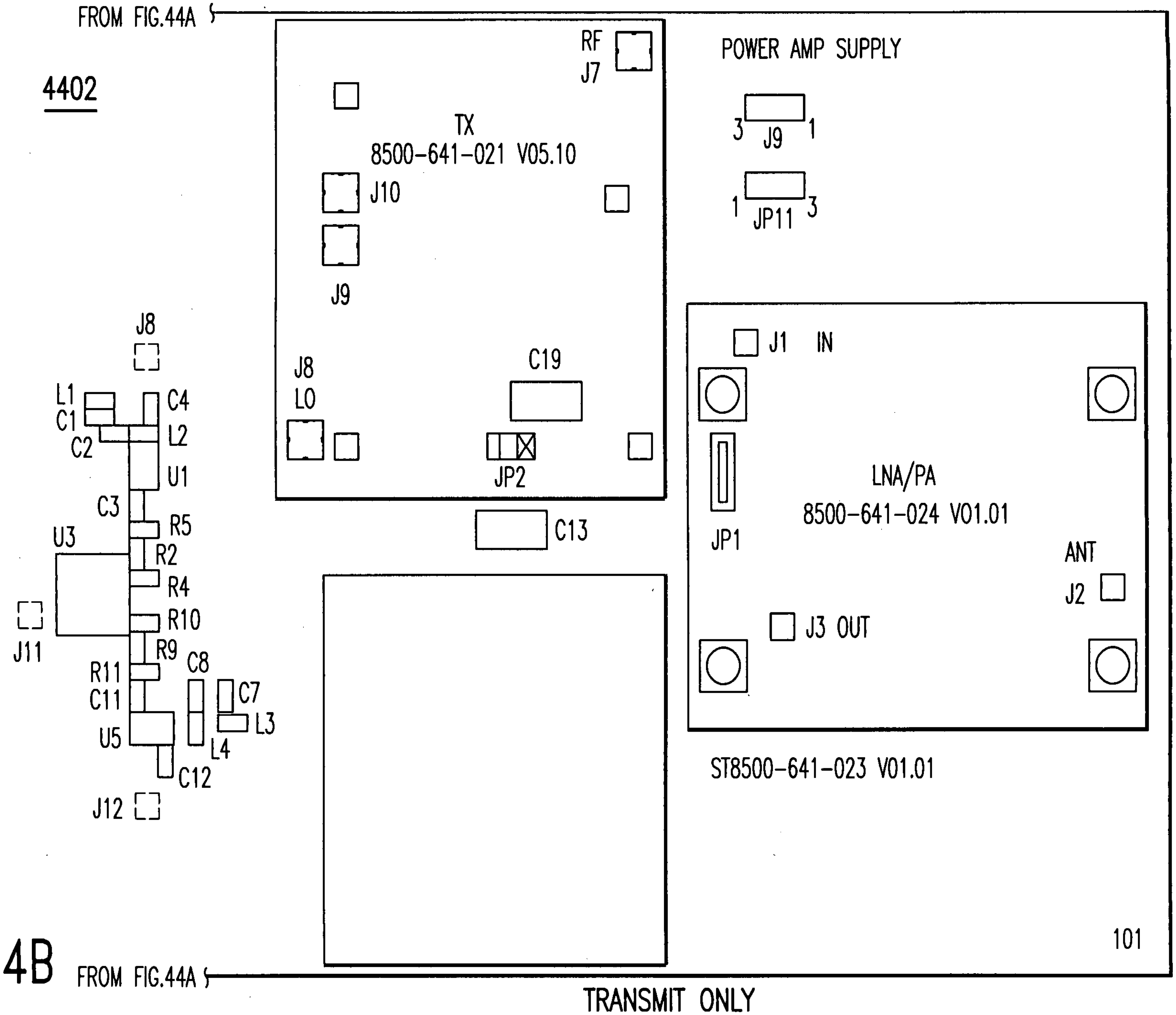

FIG.44B

New Sheet
Sheet 51 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

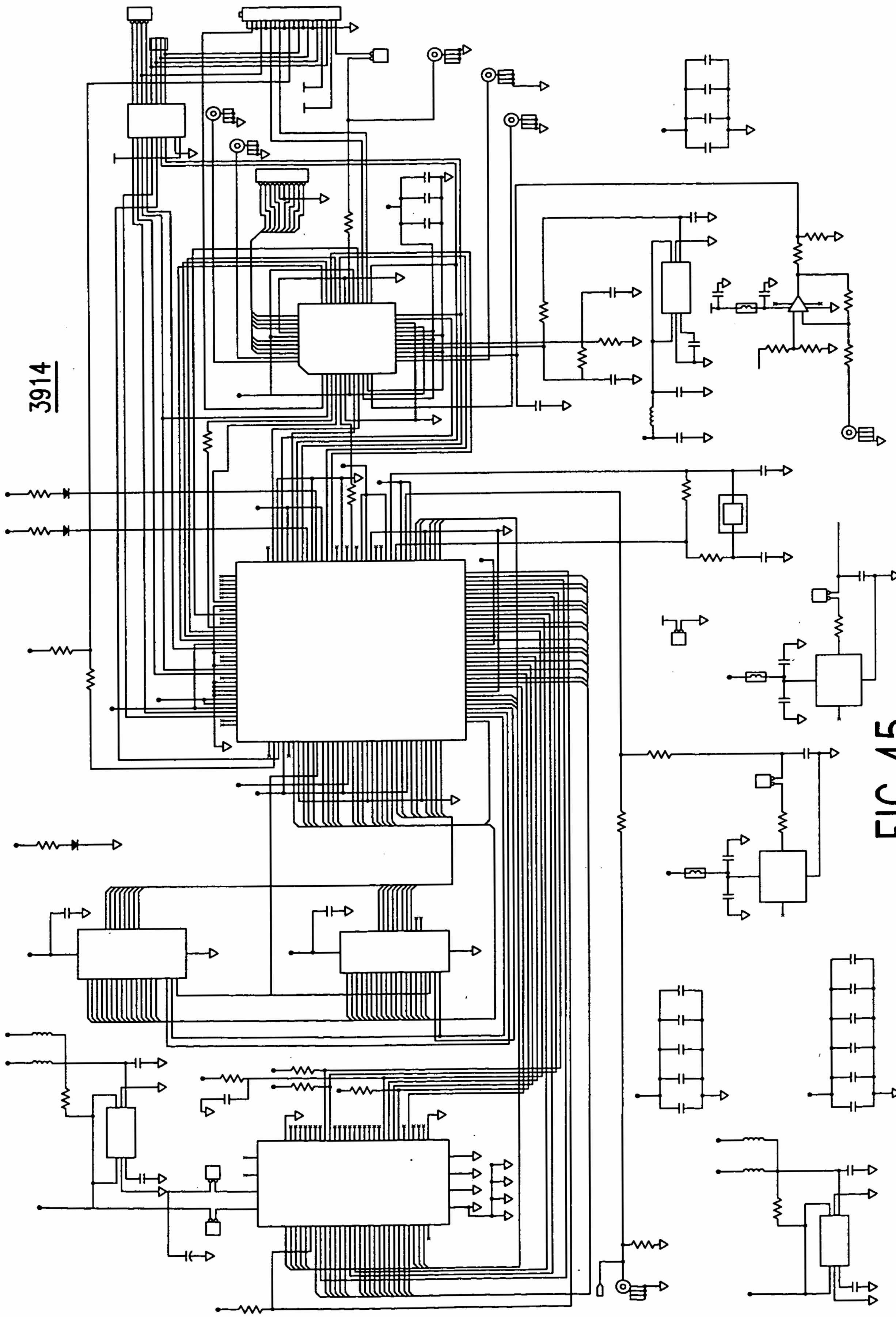

FIG.45

Item	Quantity	Reference	Part Description	Part Number	Manufacturer
1	1	C123	10uF CAP 6032, TANTALUM,20%	TAJT106K010R	KEMET
2	3	C263, C273, C275, C282	4.7uF CAP 6032, TANTALUM,20%	T491A475M006AS	KEMET
3	25	C120, C125, C126, C127, C128, C136, C137, C138, C139, C140, C141, C142, C143, C144, C145, C147, C148, C149, C264, C272, C274, C279, C280, C281, C283	0.1uF CAP 0603,X7R,10%	GRM39X7R104K050AD	MURATA
4	3	C146, C269, C276	.01uF CAP 0603,X7R,10%	GRM39X7R103K050AD	MURATA
5	5	C124, C132, C133, C271, C278	100pF CAP 0603,X7R,10%	GRM39C0G101K050AD	MURATA
6	1	C129	47pF CAP 0603,X7R,10%	GRM39C0G470J100AD	MURATA
7	2	C270, C277	27pF CAP 0603,X7R,10%	GRM39C0G270K050AD	MURATA
8	1	C130	22pF CAP 0603,X7R,10%	GRM39C0G220K050AD	MURATA
9	1	C131	10pF CAP 0603,X7R,10%	GMR39C0G100D050AD	MURATA
10	1	DS1	LED GREEN	597-3311-420	DIALIGHT
11	1	DS2	LED YELLOW	597-3401-420	DIALIGHT
12	1	DS3	LED RED	597-3111-420	DIALIGHT
13	6	JP12, JP13, JP14, JP15, JP16, JP17	CONNECTOR HEADER 2PIN	2MS-19-33-01	SPECIALITY ELECTRONICS
14	1	JP11	CONNECTOR HEADER 4PIN	100/VH/TM1SQ/W.100/4	BLKCON

FIG.46A

15	7	J16, J20, J21, J22, J23, J24, J25	CONNECTOR 82MMCX	82MMCX-50-0-1	HUBER/SHUNER
16	1	J18	CONNECTOR HEADER 10	TMS-110-01-G-S	SAMTEC
17	1	J19	CONNECTOR WITH EJECTOR	EHT-1-10-01-S-D	SAMTEC
18	1	P1	CONNECTOR 34X2PCMCIA	DICMJ-68S-SPC-M08	ITT CANON
19	7	L59, L60, L61, L63, L64, L65, L66	FERRITE BEAD	BLM11A121S	MURATA
20					
21	1	R112	10M, RESISTOR,0603,5%		
22	1	R114	390K, RESISTOR,0603,5%	ERJ-3GSYJ394V	PANASONIC
23	1	R105	100K, RESISTOR,0603,5%	ERJ-3GSYJ104V	PANASONIC
24	4	R106, R107,R108, R111	15K, RESISTOR, 0603,5%	ERJ-3GSYJ153V	PANASONIC
25	1	R116	9.1K, RESISTOR, 0603,5%	ERJ-3GSYJ912V	PANASONIC
26	1	R115	8.2K, RESISTOR, 0603,5%	ERJ-3GSYJ822V	PANASONIC
27	1	R113	3.9K, RESISTOR, 0603,5%	ERJ-3GSYJ392V	PANASONIC
28	1	R101	750, RESISTOR, 0630,5%	ERJ-3GSYJ751V	PANASONIC
29	1	R110	560, RESISTOR, 0603,5%	ERJ-3GSYJ561V	PANASONIC
30	2	R99, R100	330, RESISTOR, 0603,5%	ERJ-3GSYJ331V	PANASONIC
31	1	R119	50, RESISTOR, 0603,5%	ERJ-3GSYJ500V	PANASONIC
32	2	R128, R129	10, RESISTOR, 0603,5%	ERJ-3GSYJ100V	PANASONIC
33	8	R102, R103, R104, R109, R117, R118, R120, R127,	0, RESISTOR, 0603,5%	RM732Z1J000ZT 3GSYJ000V	ERJ KOA PANASONIC
34	6	R121, R122, R123, R124, R125, R126	TBD, RESISTOR, 0603,5%	R	PANASONIC
35	1	U10	SRAM	KM62256DLTG-5L M5M5256CVP-55LL	SAMSUNG MITSUBUSHI
36	1	U12	MAC	AM79C930	AMD

FIG.46B

37	1	U13	BASEBAND PROCESSOR	HFA3842A1	HARRIS
38	1	U14	FLASH RAM	AM29F010-55EC	AMD
39	1	U15	32 KHz CRYSTAL	CX-6V-SM2-32.768KHzC/1	STATEK
40	2	U45	BUS BUFFER	DS3862	NATIONAL
41	1	U48	REGULATOR 3.5 V	TK11235BMC	TOKO
42	1	U49	22MHz OSCILLATOR	FOX F3346-22MHz	FOX
43	1	U50	2 VOLT REFERENCE	TK11220BMC	TOKO
44	1	U51	40MHz OSCILLATOR	CXO-M-10N-40MHz A/1	STATEK

FIG.46C

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

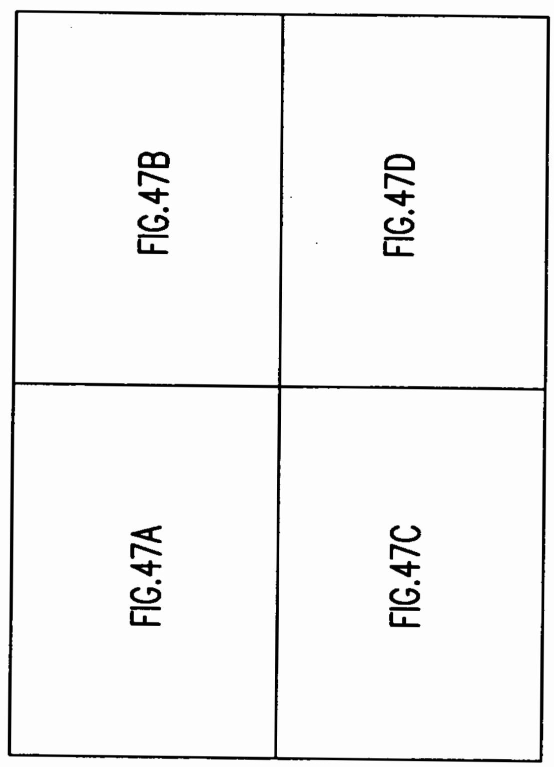

FIG. 47

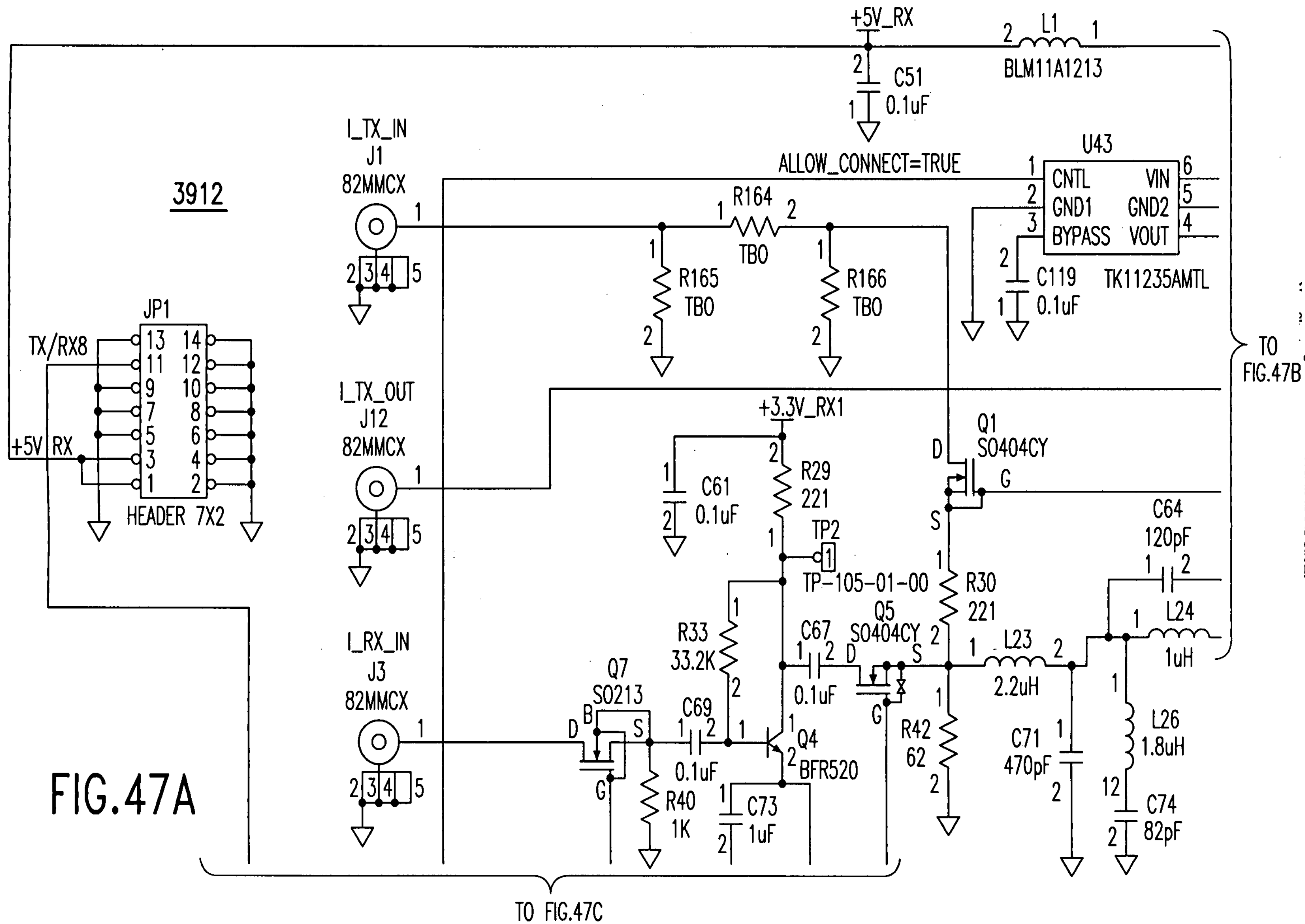

FIG.47A

New Sheet
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Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

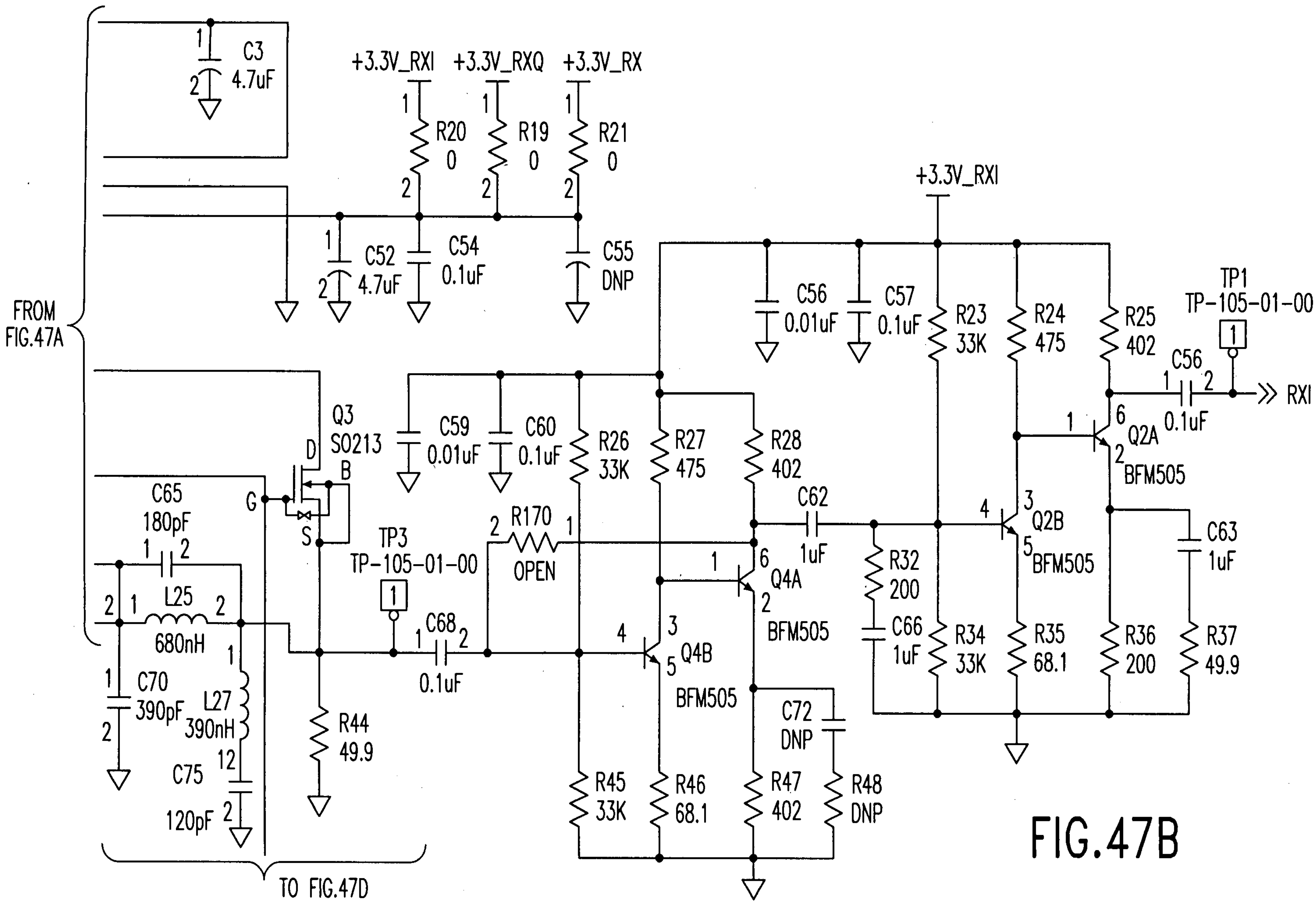

FIG.47B

New Sheet
Sheet 58 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

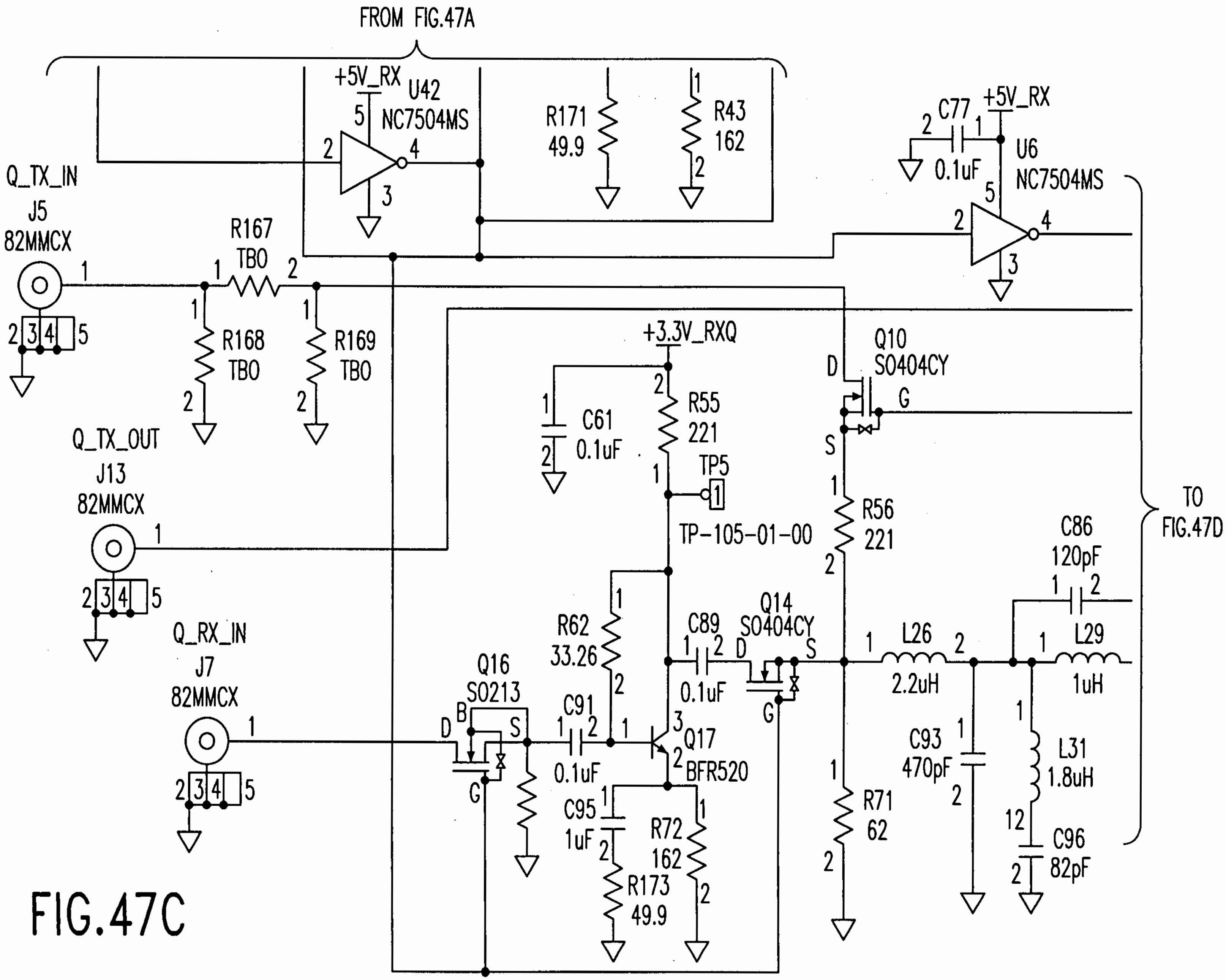

FIG.47C

New Sheet
Sheet 59 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
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New Sheet
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Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

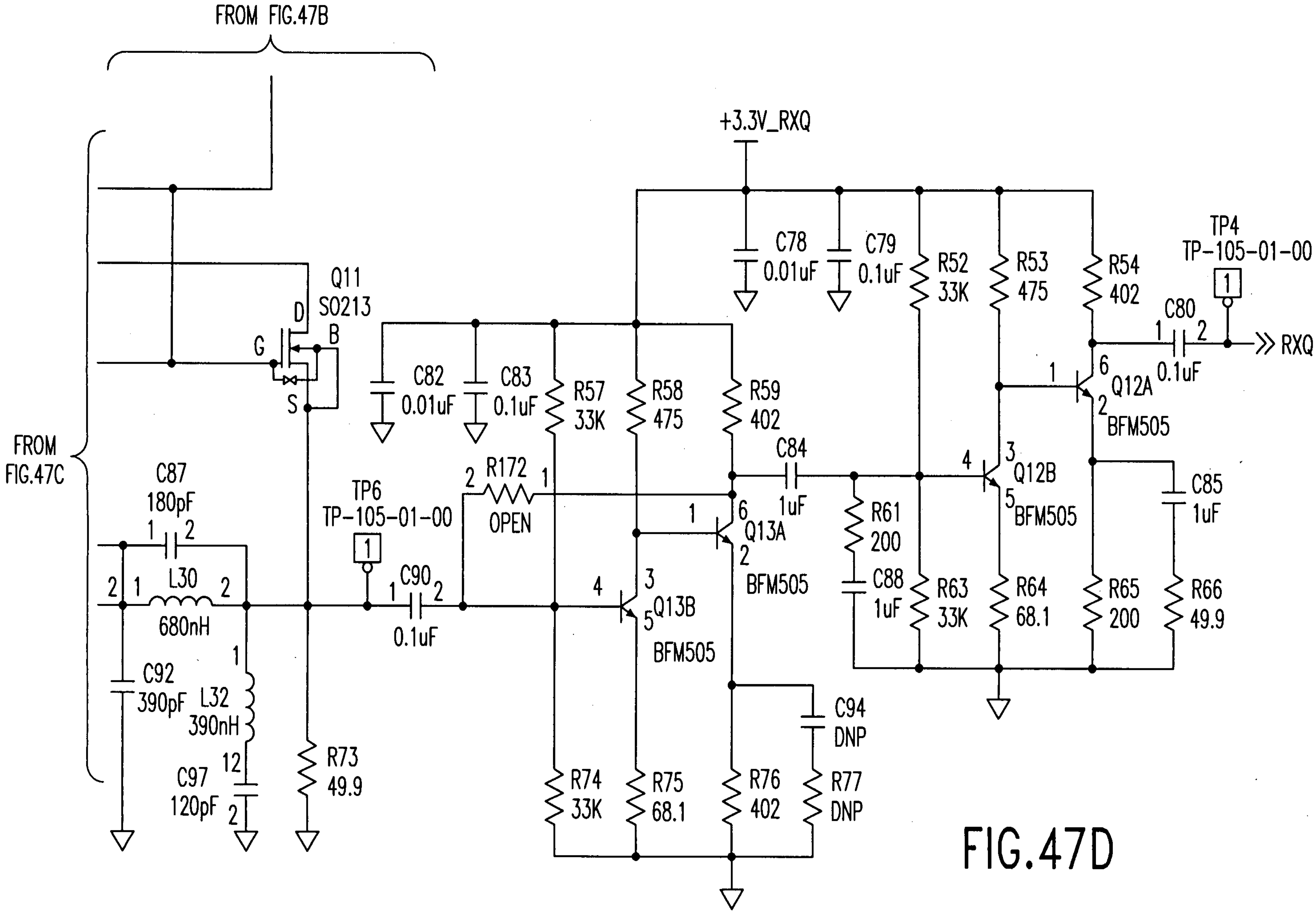

FIG.47D

Replacement Sheet
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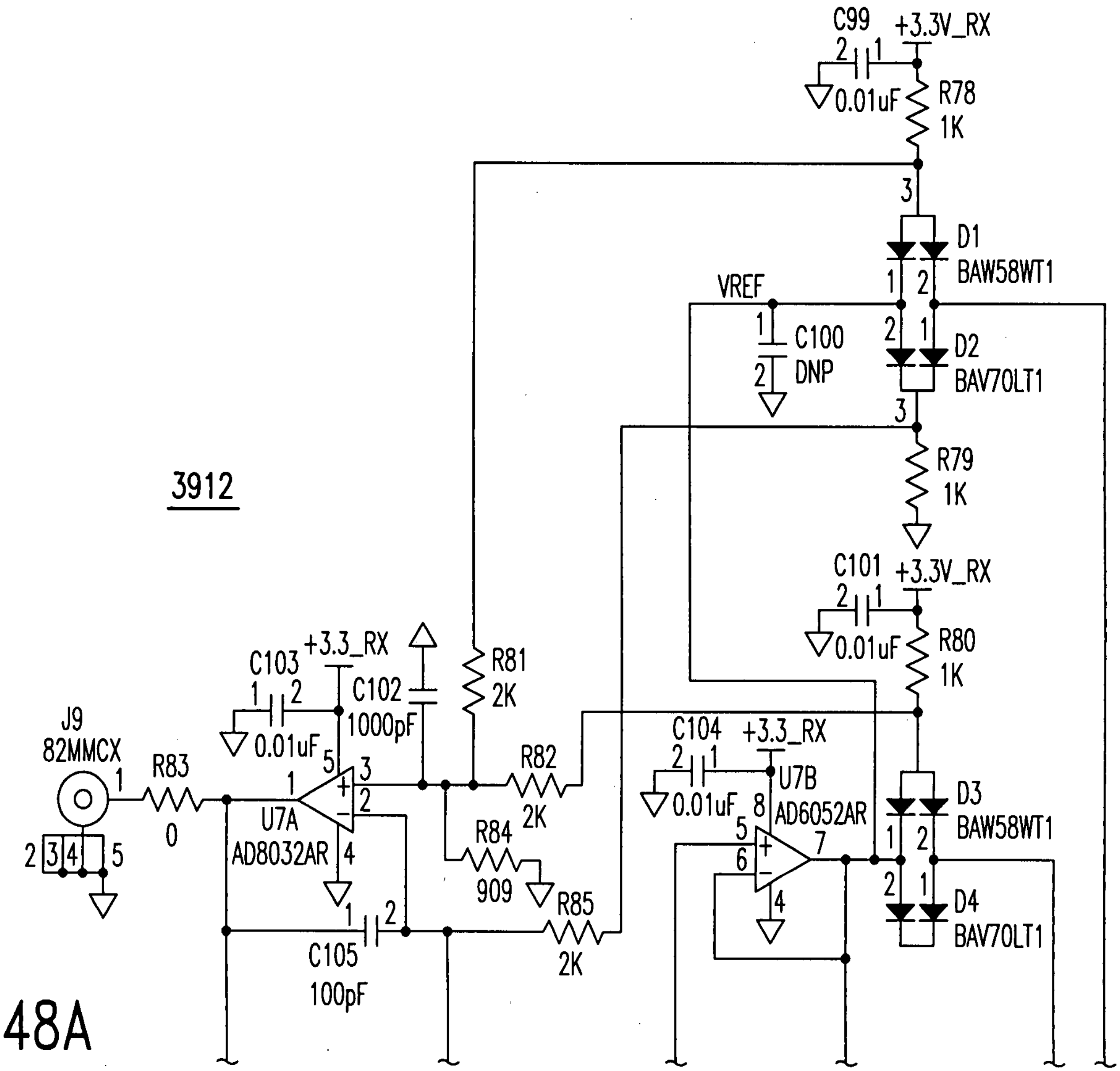
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit



TO FIG.48B

FIG. 48A

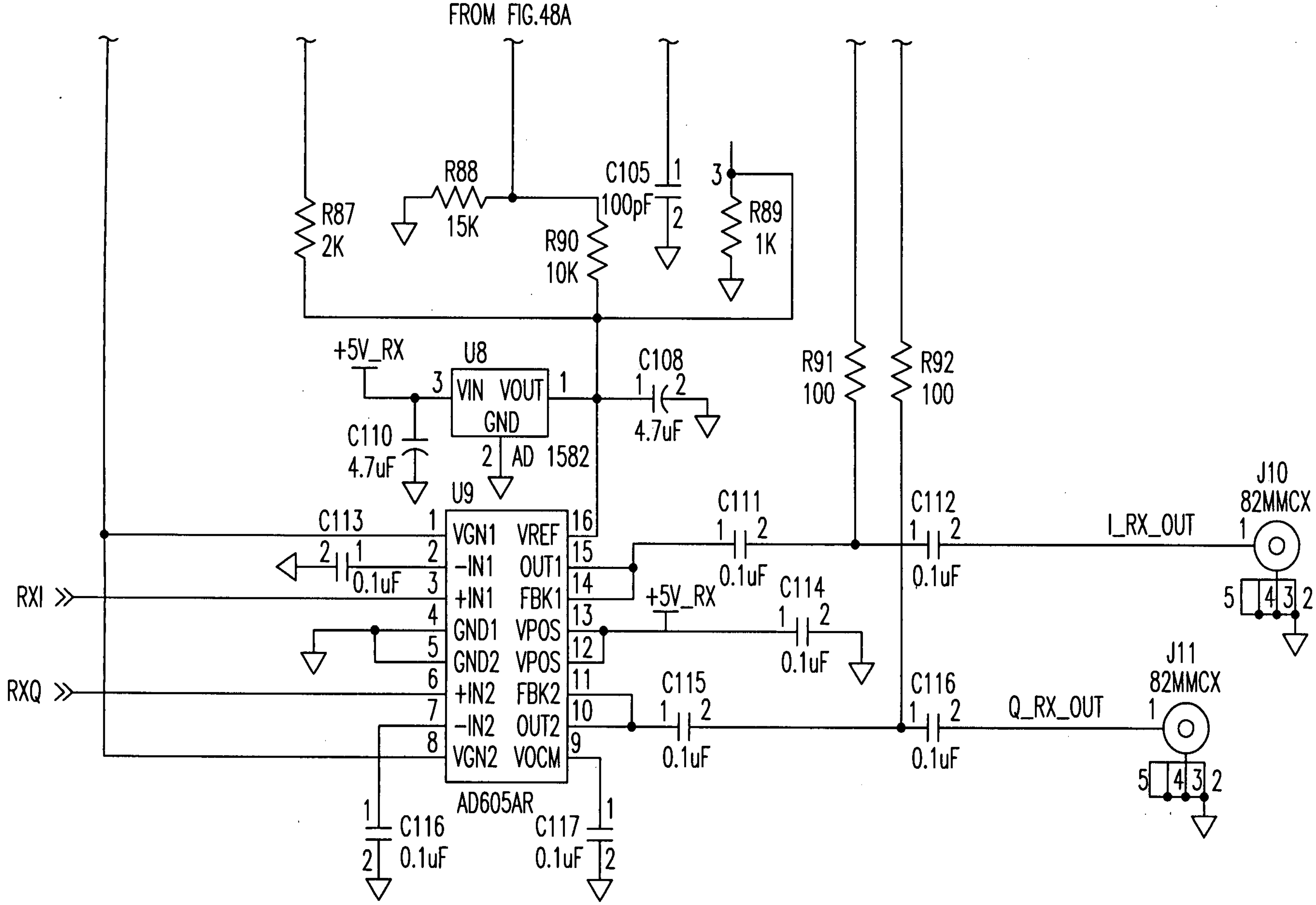


FIG. 48B

New Sheet
Sheet 62 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

ITEM	QUANT.	REFERENCE	PART	PART NUMBER	MANUFACTURER
1	4	C3,C52,C108,C110	4.7uF	T491A475K006AS	KEMET
2	26	C51,C54,C57,C58,C60,C61,	0.1uF	GRM39Y5V104Z016	MURATA
		C67,C68,C69,C77,C79,C80,			
		C81,C83,C89,C90,C91,C111,			
		C112,C113,C114,C115,C116,			
		C117,C118,C119			
3	1	C55	DNP	T491A475K006AS	KEMET
4	8	C56,C59,C78,C82,C99,C101,	0.01uF	GRM39X7R103K050	MURATA
		C103,C104			
5	8	C62,C63,C66,C73,C84,C85,	1uF	GRM40Y5V105Z016	MURATA
		C88,C95			
6	4	C64,C75,C86,C97	120pF	GRM39COG121J050	MURATA
7	2	C65,C87	180pF	GRM39COG181J050	MURATA
8	2	C70,C92	390pF	GRM39COG391J050	MURATA
9	2	C71,C93	470pF	GRM39COG471J050	MURATA
10	2	C72,C94	DNP	GRM40Y5V105Z016	MURATA
11	2	C74,C96	82pF	GRM39COG820J050	MURATA
12	2	C100,C106	DNP	DNP	MURATA
13	2	C105,C102	1000pF	GRM39COG102K050	MURATA
14	2	D3,D1	BAW56WT1	BAW56WT1	MOTOROLA
15	2	D4,D2	BAV70LT1	BAV70LT1	MOTOROLA
16	1	JP1	HEADER 7X2	FTSH-107-02-L-D	SAMTEC
17	9	J1,J3,J5,J7,J9,J10,J11,	82MMCX	82MMCX-50-0-1	SUHNER
		J12,J13			
18	1	L1	BLM11A121S	BLM11A121S	MURATA
19	2	L23,L28	2.2uH	LQG21N2R2K10	MURATA
20	2	L29,L24	1uH	LQG21N1R0K10	MURATA
21	2	L30,L25	680nH	LQG21NR68K10	MURATA

FIG.49A

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

22	2	L26,L31	1.8uH	LQG21N1R8K10	MURATA
23	2	L32,L27	390nH	LQG21NR39K10	MURATA
24	4	Q1,Q5,Q10,Q14	SD404CY	SD404CY	CALOGIC
25	4	Q2,Q4,Q12,Q13	BFM505	BFM505	PHILIPS
26	4	Q3,Q7,Q11,Q16	SD213	SD213	CALOGIC
27	2	Q17,Q8	BFR520	BFR520	PHILIPS
28	4	R19,R20,R21,R83	0	ERJ3GSY0R00	PANASONIC
29	8	R23,R26,R34,R45,R52,R57,	33K	ERJ3GSYJ333	PANASONIC
		R63,R74			
30	4	R24,R27,R53,R58	475	ERJ3EKF4750	PANASONIC
31	6	R25,R28,R47,R54,R59,R76	402	ERJ3EKF4020	PANASONIC
32	4	R29,R30,R55,R56	221	ERJ3EKF2210	PANASONIC
33	2	R32,R61	200	ERJ3GSYJ201	PANASONIC
34	2	R33,R62	33.2K	ERJ3GSYJ333	PANASONIC
35	4	R35,R46,R64,R75	68.1	ERJ3EKF68R1	PANASONIC
36	2	R36,R65	200	ERJ3EKF2000	PANASONIC
37	6	R37,R44,R66,R73,R171,	49.9	ERJ3EKF49R9	PANASONIC
		R173			
38	6	R40,R68,R78,R79,R80,R89	1K	ERJ3EKF1001	PANASONIC
39	2	R42,R71	62	ERJEGSYJ620	PANASONIC
40	2	R43,R72	162	ERJ3EKF1620	PANASONIC
41	2	R77,R48	DNP	ERJ3GSYJ330	PANASONIC
42	4	R81,R82,R85,R87	2K	ERJ3EKF2001	PANASONIC
43	1	R84	909	ERJ3EKF9090	PANASONIC
44	1	R88	15K	ERJ3EJF1502	PANASONIC
45	1	R90	10K	ERJ3EKF1002	PANASONIC
46	2	R91,R92	100	ERJ3EKF1000	PANASONIC
47	6	R164,R165,R166,R167,R168,	TBD		PANASONIC
		R169			
48	2	R170,R172	OPEN		PANASONIC

FIG.49B

Replacement Sheet
Sheet 64 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

49	6	TP1,TP2,TP3,TP4,TP5,TP6	TP-105-01-00		
50	2	U42,U6	NC7S04M5	NC7S04M5	NATIONAL SEMICONDUCTOR
51	1	U7	AD8052AR	AD8052AR	ANALOG DEVICES
52	1	U8	AD1582	AD1582	ANALOG DEVICES
53	1	U9	AD605AR	AD605AR	ANALOG DEVICES
54	1	U43	TK11235AMTL	TK11235BM	TOKO
55	1		BOARD	8500.541.003.V13.01	

FIG.49C

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

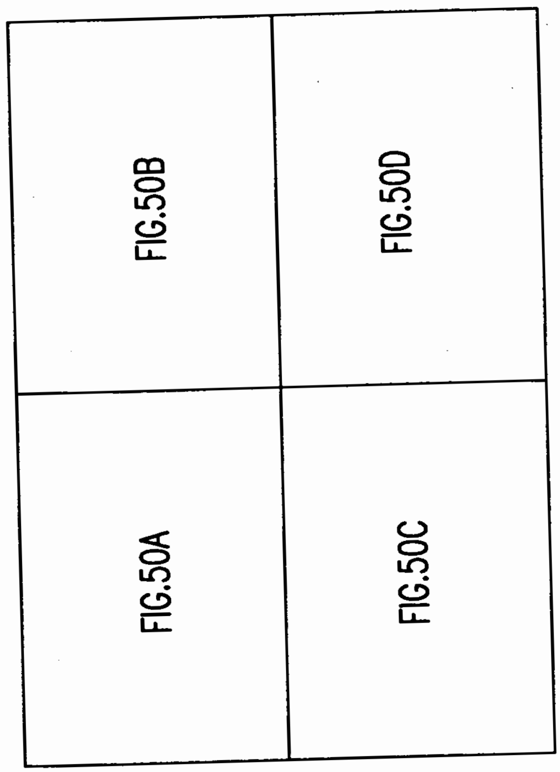


FIG. 50

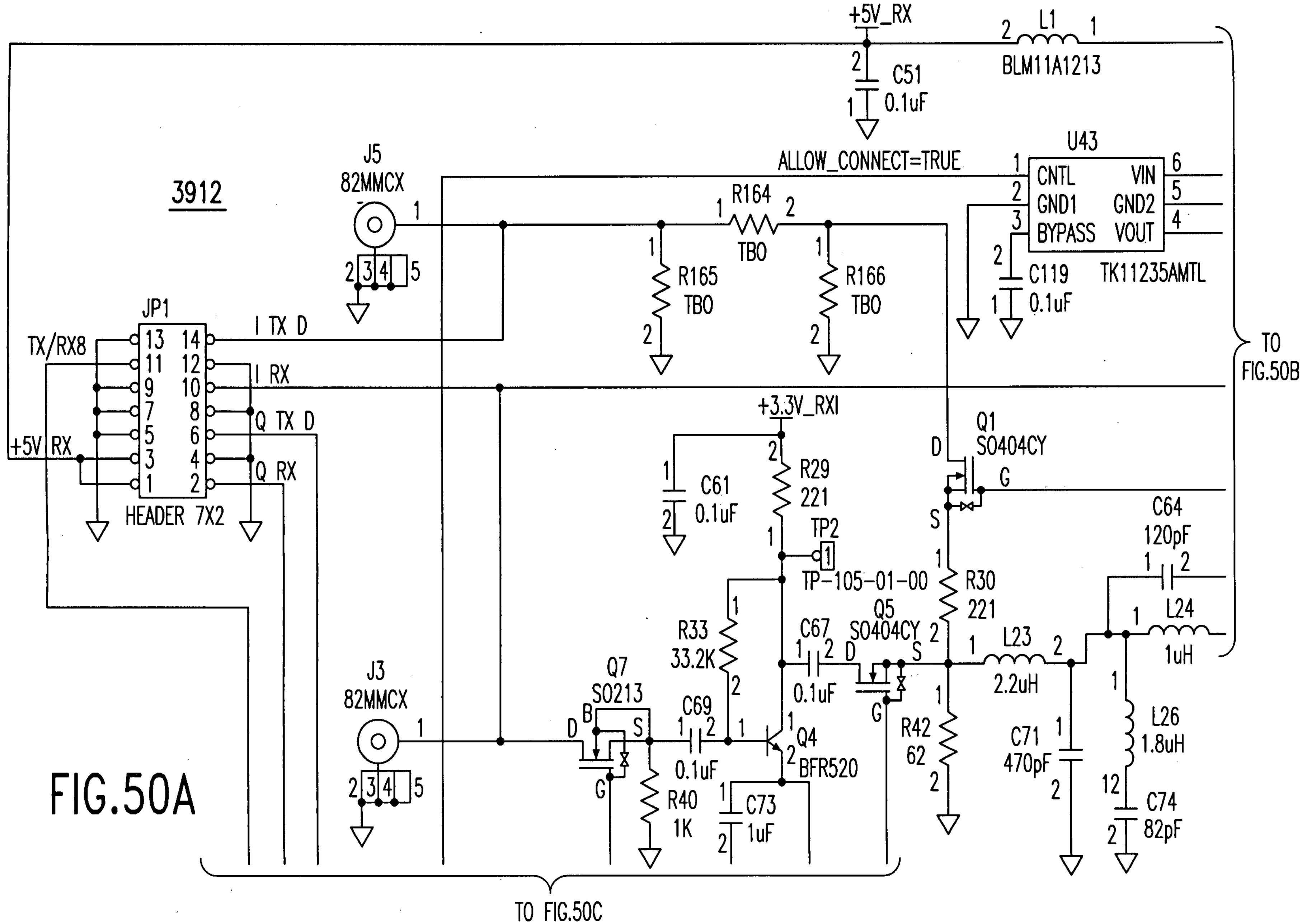

3912
+5V_RX
C51
0.1uF
L1
BLM11A1213
U43
CNTL
VIN
GND1
GND2
BYPASS
VOUT
TK11235AMTL
C119
0.1uF
ALLOW_CONNECT=TRUE
J5
82MMCX
R164
TBO
R165
TBO
R166
TBO
JP1
HEADER 7X2
TX/RX8
+5V_RX
I TX D
I RX
Q TX D
Q RX
+3.3V_RXI
C61
0.1uF
R29
221
TP2
TP-105-01-00
Q1
S0404CY
R30
221
C64
120pF
L24
1uH
TO FIG.50B
R33
33.2K
C67
0.1uF
Q5
S0404CY
L23
2.2uH
J3
82MMCX
Q7
S0213
C69
0.1uF
Q4
BFR520
R40
1K
C73
1uF
R42
62
C71
470pF
L26
1.8uH
C74
82pF
TO FIG.50C

FIG.50A

New Sheet
Sheet 68 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

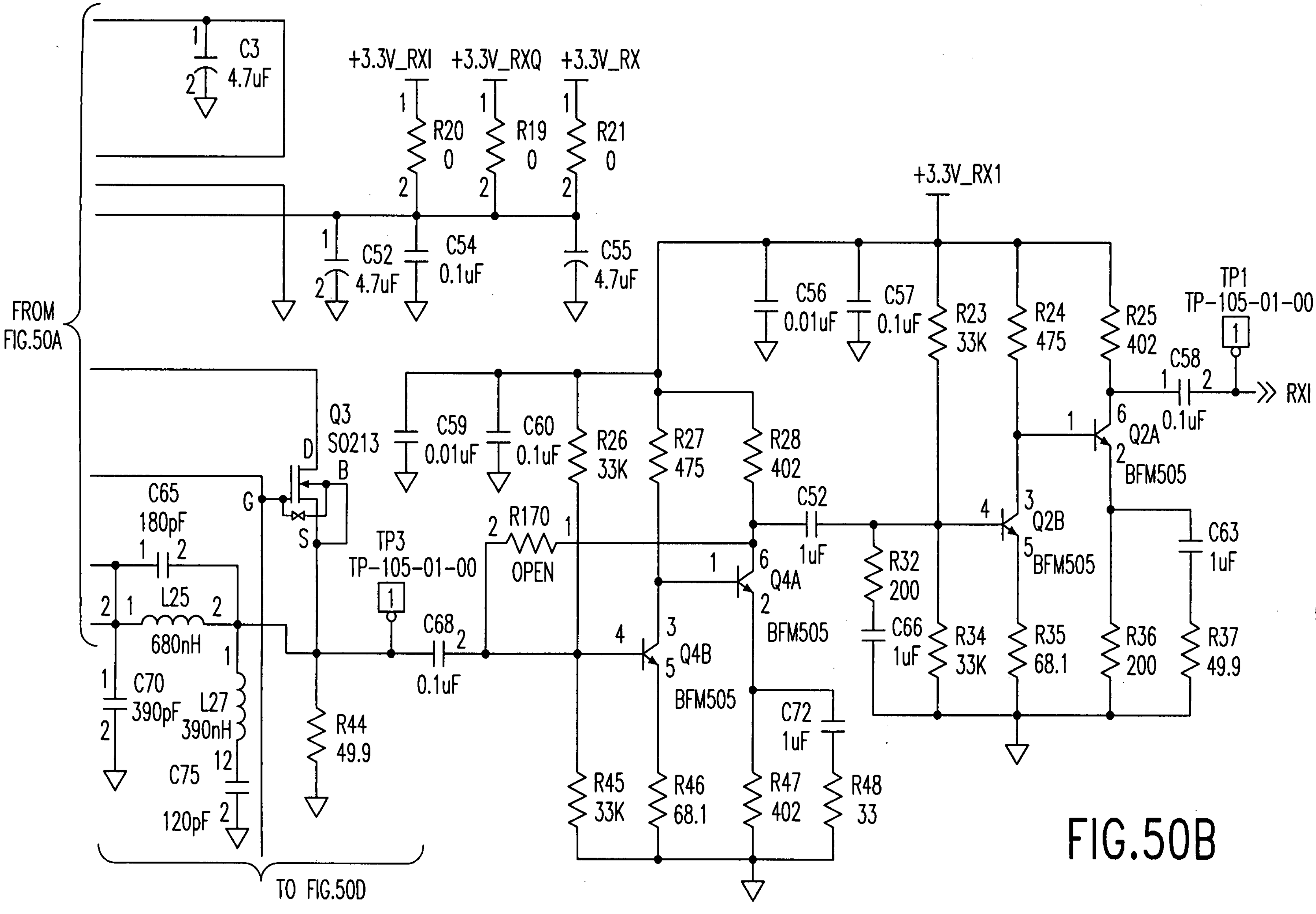


FIG.50B

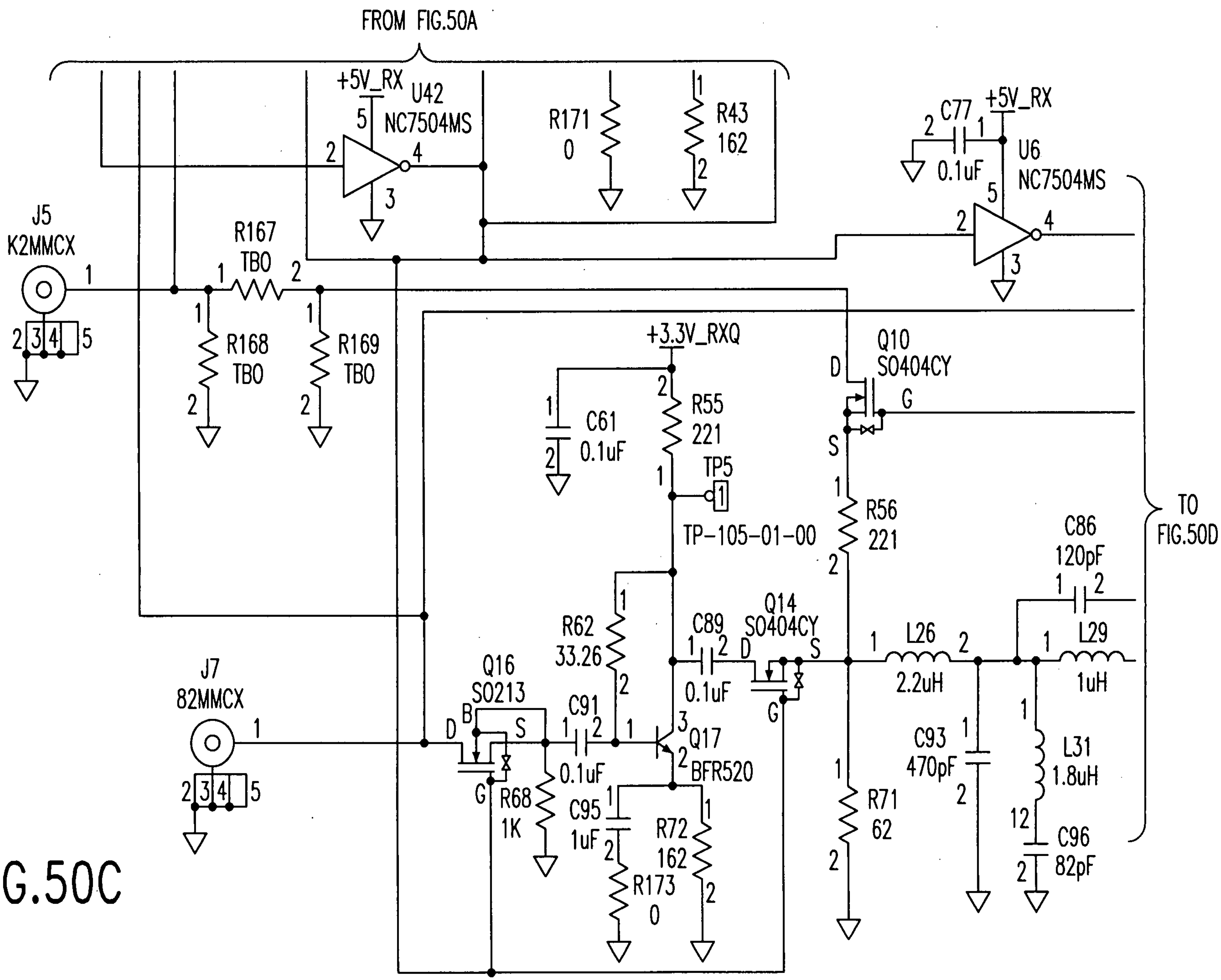

FROM FIG.50A
+5V_RX
U42
NC7504MS
R171
0
R43
162
C77
0.1uF
U6
NC7504MS
J5
K2MMCX
R167
TB0
R168
TB0
R169
TB0
+3.3V_RXQ
Q10
S0404CY
C61
0.1uF
R55
221
TP5
TP-105-01-00
R56
221
TO
FIG.50D
C86
120pF
R62
33.26
C89
0.1uF
Q14
S0404CY
L26
2.2uH
L29
1uH
J7
82MMCX
Q16
S0213
C91
0.1uF
Q17
BFR520
C93
470pF
L31
1.8uH
R68
1K
C95
1uF
R72
162
R71
62
C96
82pF
R173
0

FIG.50C

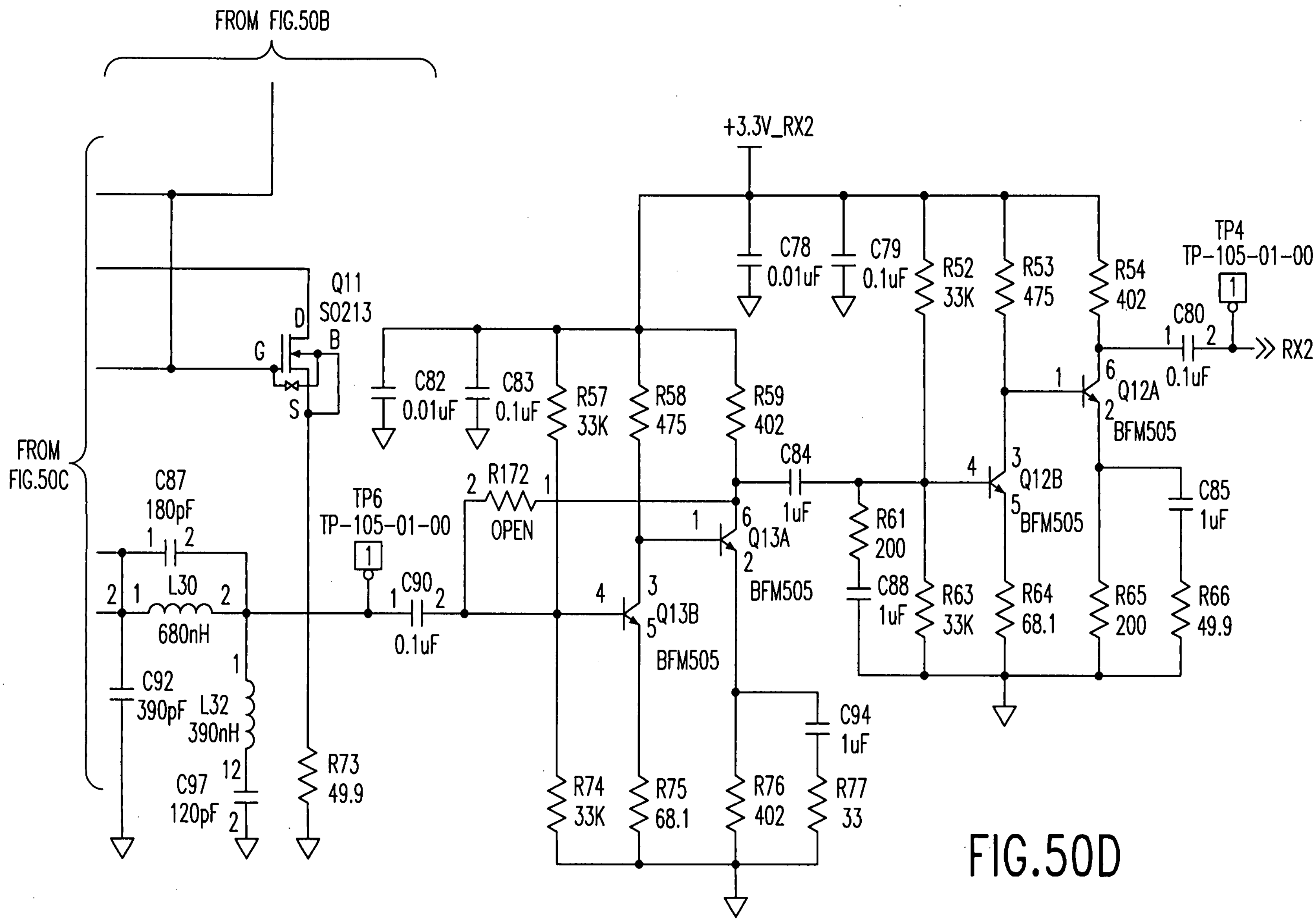


FIG.50D

New Sheet
Sheet 70 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

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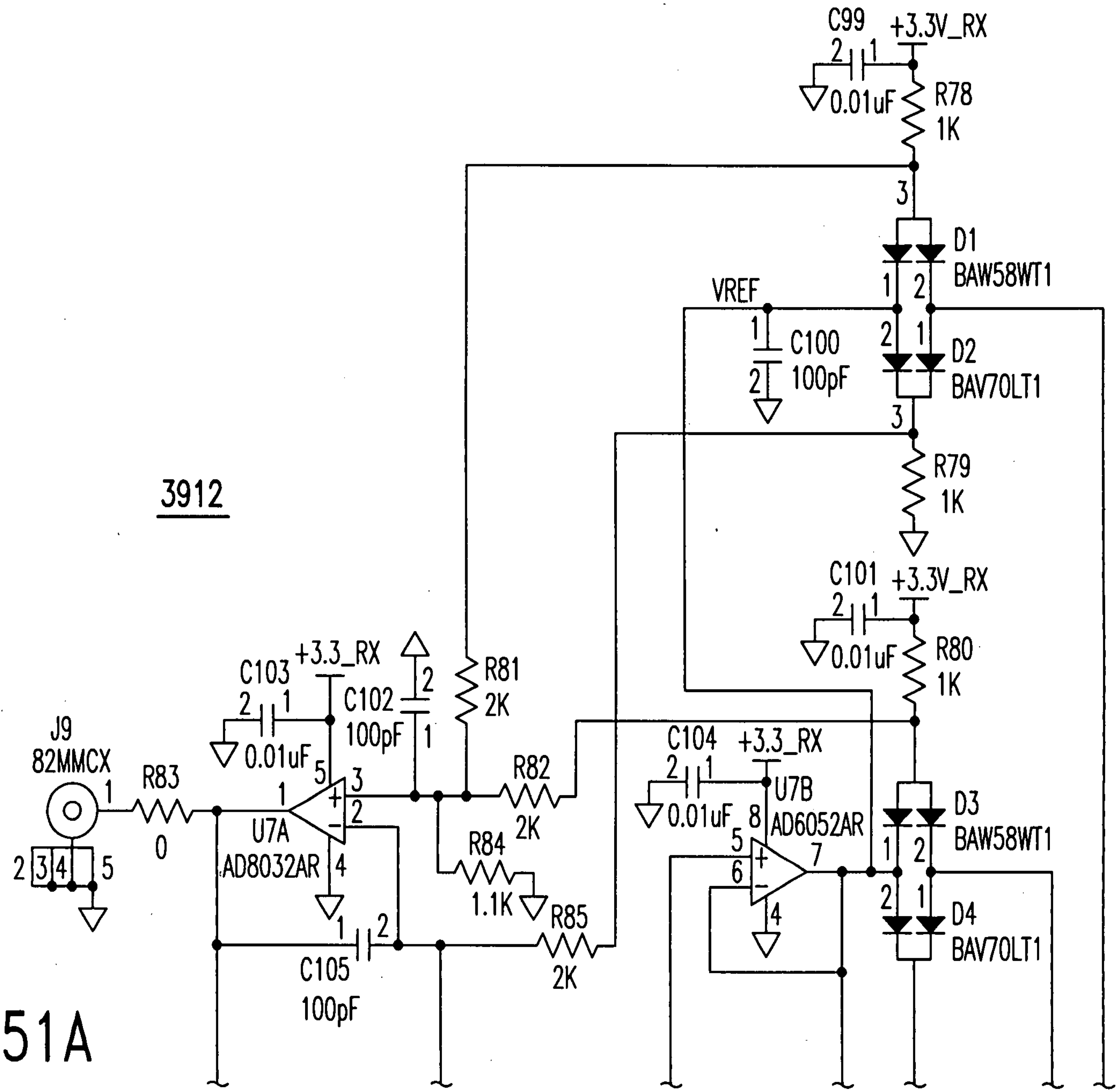
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit



TO FIG.51B

FIG. 51A

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

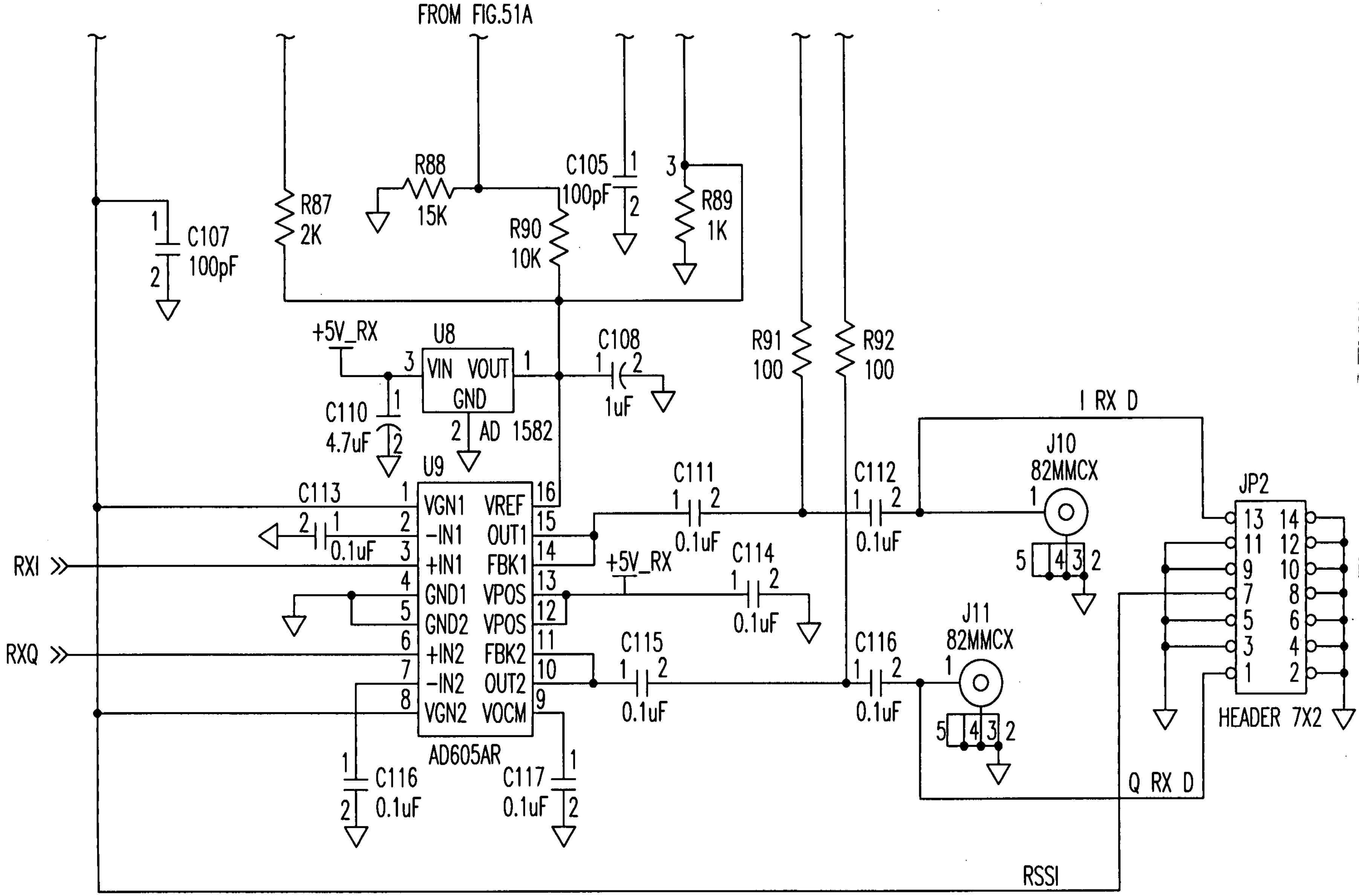


FIG. 51B

ITEM	QTY	REFERENCE	PART	PART NUMBER	MANUFACTURER
1	3	C3,C52,C55	4.7uF	T491A475K006AS	KEMET
2	26	C51,C54,C57,C58,C60,C61,	0.1uF	GRM39Y5V104Z016	MURATA
		C67,C68,C69,C77,C79,C80,			
		C81,C83,C89,C90,C91,C111,			
		C112,C113,C114,C115,C116,			
		C117,C118,C119			
3	8	C56,C59,C78,C82,C99,C101,	0.01uF	GRM39X7R103K050	MURATA
		C103,C104			
4	10	C62,C63,C66,C72,C73,C84,	1uf	GRM40Y5V105Z016	MURATA
		C85,C88,C94,C95			
5	4	C64,C75,C86,C97	120pF	GRM39COG121J050	MURATA
6	2	C87,C65	180pF	GRM39COG181J050	MURATA
7	2	C70,C92	390pF	GRM39COG391J050	MURATA
8	2	C71,C93	470pF	GRM39COG471J050	MURATA
9	2	C96,C74	82pF	GRM39COG820J050	MURATA
10	5	C100,C102,C105,C106,C107	100pF	GRM39COG101K050	MURATA
11	1	C108	1uF		
12	1	C110	4.7uF		
13	2	D3,D1	BAW56WT1	BAW56WT1	MOTOROLA
14	2	D4,D2	BAV70LT1	BAV70LT1	MOTOROLA
15	2	JP2,JP1	HEADER 7X2		
16	6	J1,J3,J5,J7,J10,J11	82MMCX	142-0701-231	JOHNSON
17	1	J9	82MMCX	82MMCX-50-0-1	SUHNER
18	1	L1	BLM11A121S	BLM11A121S	MURATA
19	2	L28,L23	2.2uH	LQG21N2R2K10	MURATA
20	2	L24,L29	1uH	LQG21N1R0K10	MURATA
21	2	L30,L25	680nH	LQG21NR68K10	MURATA
22	2	L26,L31	1.8uH	LQG21N1R8K10	MURATA

FIG.52A

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Sheet 73 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

23	2	L27,L32	390nH	LQG21NR39K10	MURATA
24	4	Q1,Q5,Q10,Q14	SD404CY	SD404CY	CALOGIC
25	4	Q2,Q4,Q12,Q13	BFM505	BFM505	PHILIPS
26	4	Q3,Q7,Q11,Q16	SD213	SD213	CALOGIC
27	2	Q17,Q8	BFR520	BFR505	PHILIPS
28	5	R19,R20,R21,R171,R173	0		
29	8	R23,R26,R34,R45,R52,R57,	33K	ERJ3GSY333	PANASONIC
		R63,R74			
30	4	R24,R27,R53,R58	475	ERJ3EKF4750	PANASONIC
31	6	R25,R28,R47,R54,R59,R76	402	ERJ3EKF4020	PANASONIC
32	4	R29,R30,R55,R56	221	ERF3EKF2210	PANASONIC
33	2	R32,R61	200	ERJ3GSYJ201	PANASONIC
34	2	R33,R62	33.2K	ERJ3GSYJ333	PANASONIC
35	4	R35,R46,R64,R75	68.1	ERJ3EKF68R1	PANASONIC
36	2	R36,R65	200	ERJ3EKF2000	PANASONIC
37	2	R66,R37	49.9	ERJ3EKF49R9	PANASONIC
38	6	R40,R68,R78,R79,R80,R89	1K	ERJ3EKF1001	PANASONIC
39	2	R42,R71	62	ERJ3GSYJ620	PANASONIC
40	2	R43,R72	162	ERJ3EKF6810	PANASONIC
41	2	R44,R73	49.9	ERJ3EKF1001	PANASONIC
42	2	R77,R48	33	ERJ3GSYJ330	PANASONIC
43	4	R81,R82,R85,R87	2K	ERJ3EKF2001	PANASONIC
44	1	R83	0	ERJGSY0R00	PANASONIC
45	1	R84	1.1K	ERJ3EKF2001	PANASONIC
46	1	R88	15K	ERJ3EKF1502	PANASONIC
47	1	R90	10K	ERJ3EKF1002	PANASONIC
48	2	R91,R92	100	ERJ3EKF1000	PANASONIC
49	6	R164,R165,R166,R167,R168,	TBD		
		R169			
50	2	R170,R172	OPEN		

FIG.52B

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Sheet 74 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

51	0	TP1,TP2,TP3,TP4,TP5,TP6	TP-105-01-00		
52	2	U42,U6	NC7S04M5		NATIONAL SEMICONDUCTOR
53	1	U7	AD8032AR	AD8032AR	ANALOG DEVICES
54	1	U8	AD1582	AD1582	ANALOG DEVICES
55	1	U9	AD605AR	AD605AR	ANALOG DEVICES
56	1	U43	TK11235AMTL	TK11235AMTL	TOKO

FIG.52B-1

New Sheet
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Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

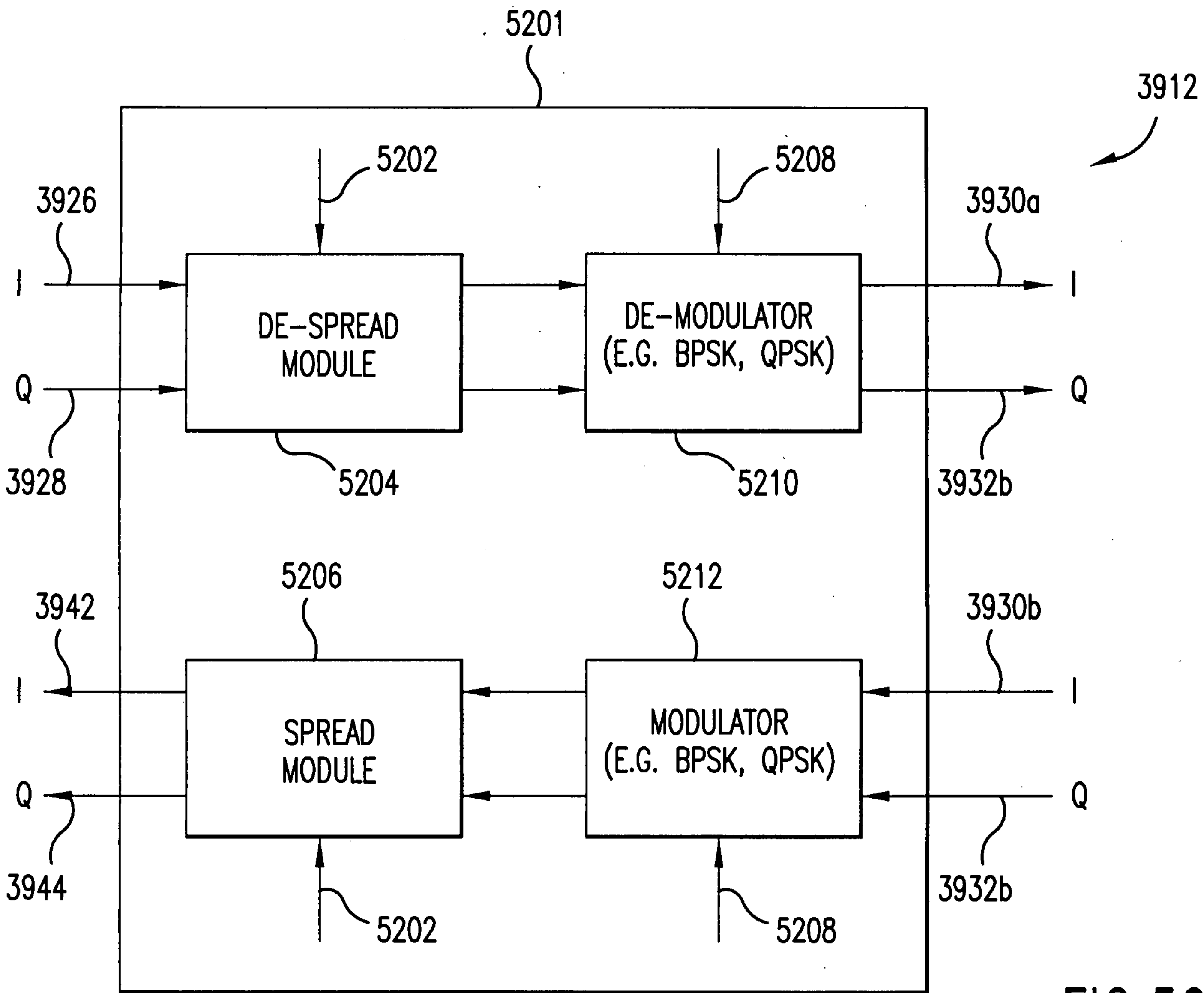

FIG.52C

Replacement Sheet
Sheet 76 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

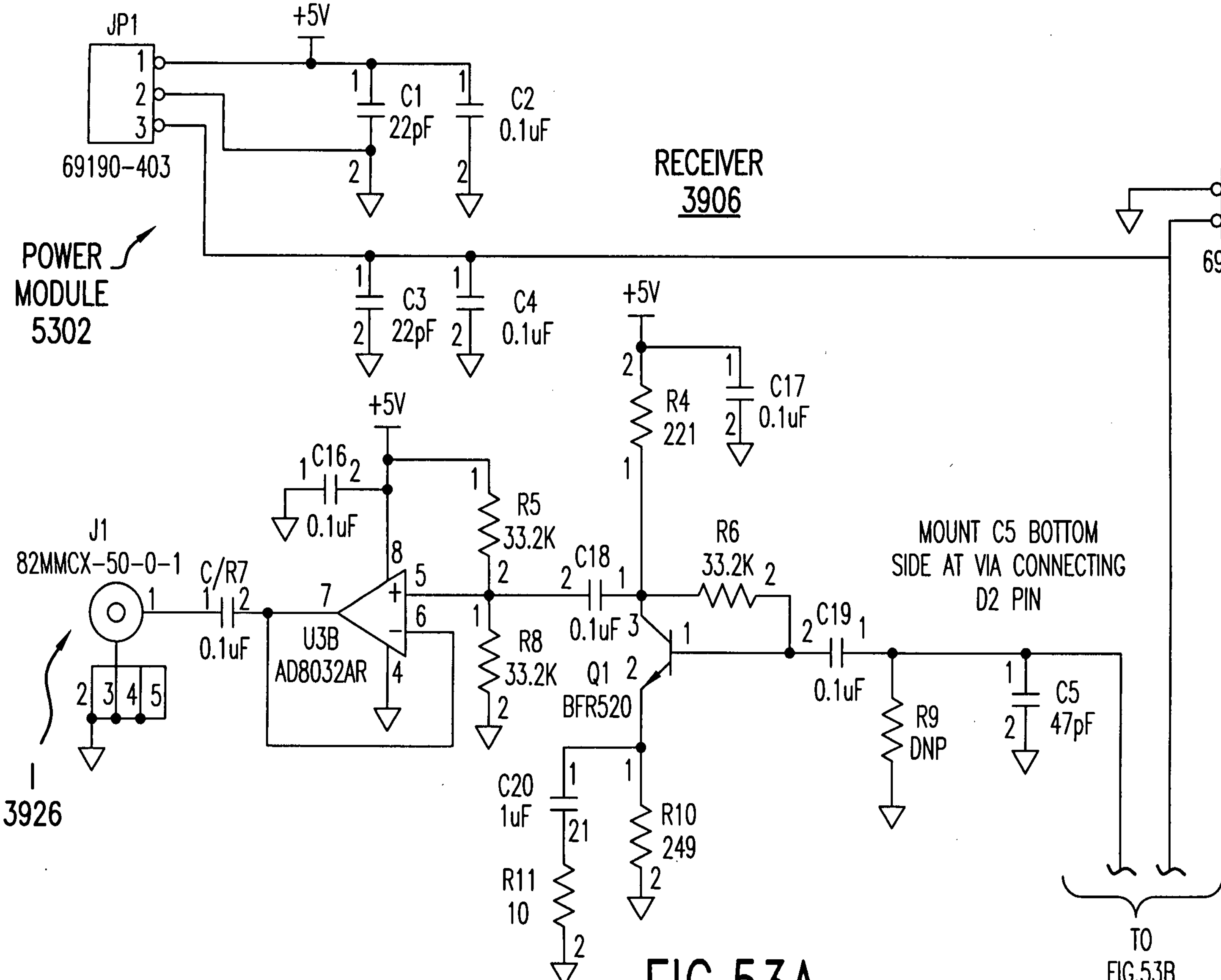

FIG.53A

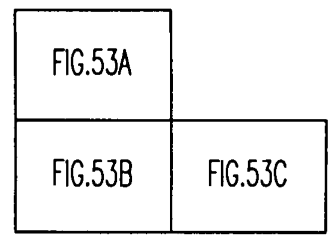

FIG.53

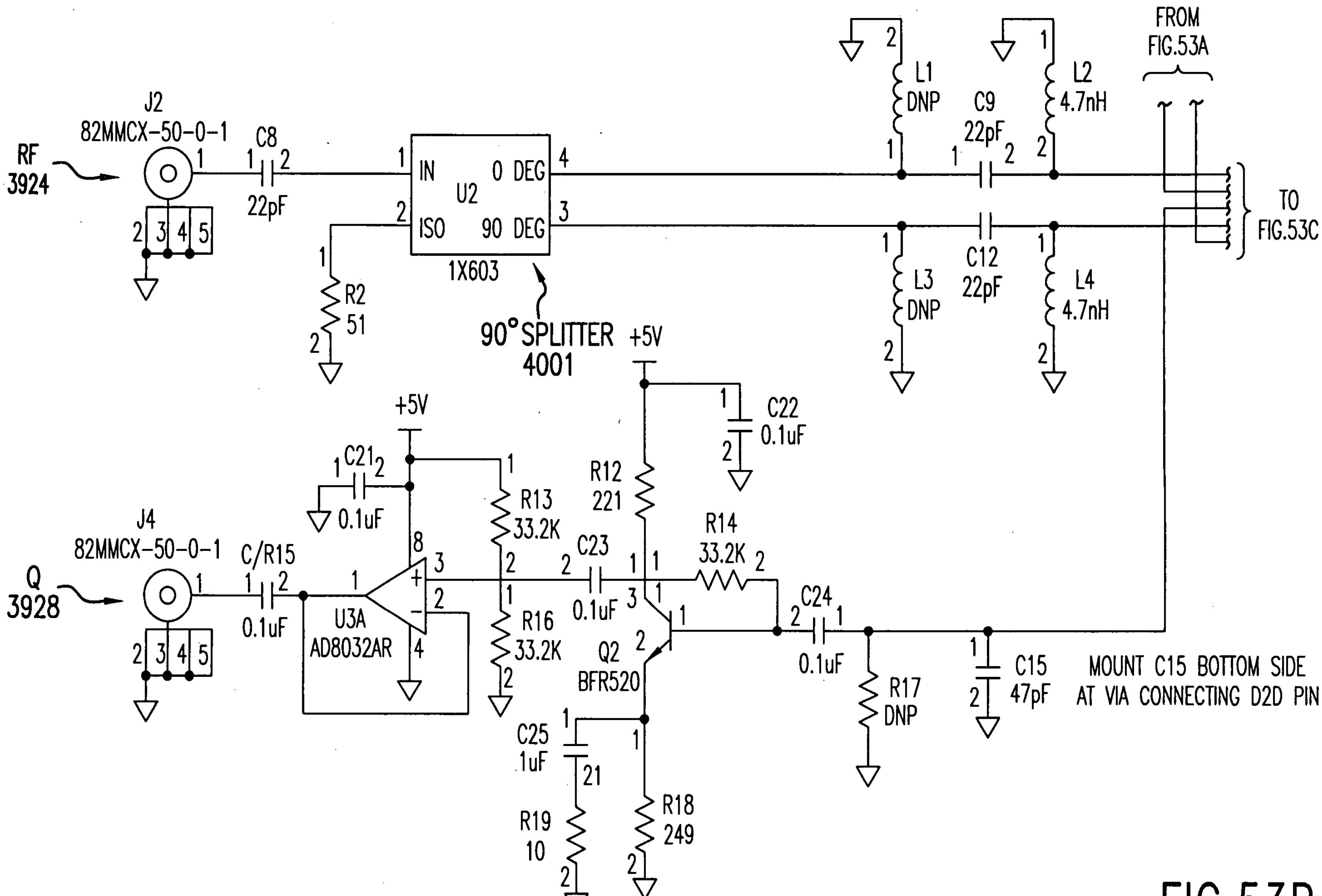
RF 3924
J2
82MMCX-50-0-1
C8
22pF
U2
IN
ISO
0 DEG
90 DEG
1X603
R2
51
90° SPLITTER 4001
L1 DNP
C9 22pF
L2 4.7nH
L3 DNP
C12 22pF
L4 4.7nH
FROM FIG.53A
TO FIG.53C
+5V
C22 0.1uF
R12 221
C21 0.1uF
R13 33.2K
J4
82MMCX-50-0-1
Q 3928
C/R15
0.1uF
U3A
AD8032AR
C23 0.1uF
R14 33.2K
C24 0.1uF
R16 33.2K
Q2
BFR520
R17 DNP
C15 47pF
MOUNT C15 BOTTOM SIDE AT VIA CONNECTING D2D PIN
C25 1uF
R19 10
R18 249

FIG.53B

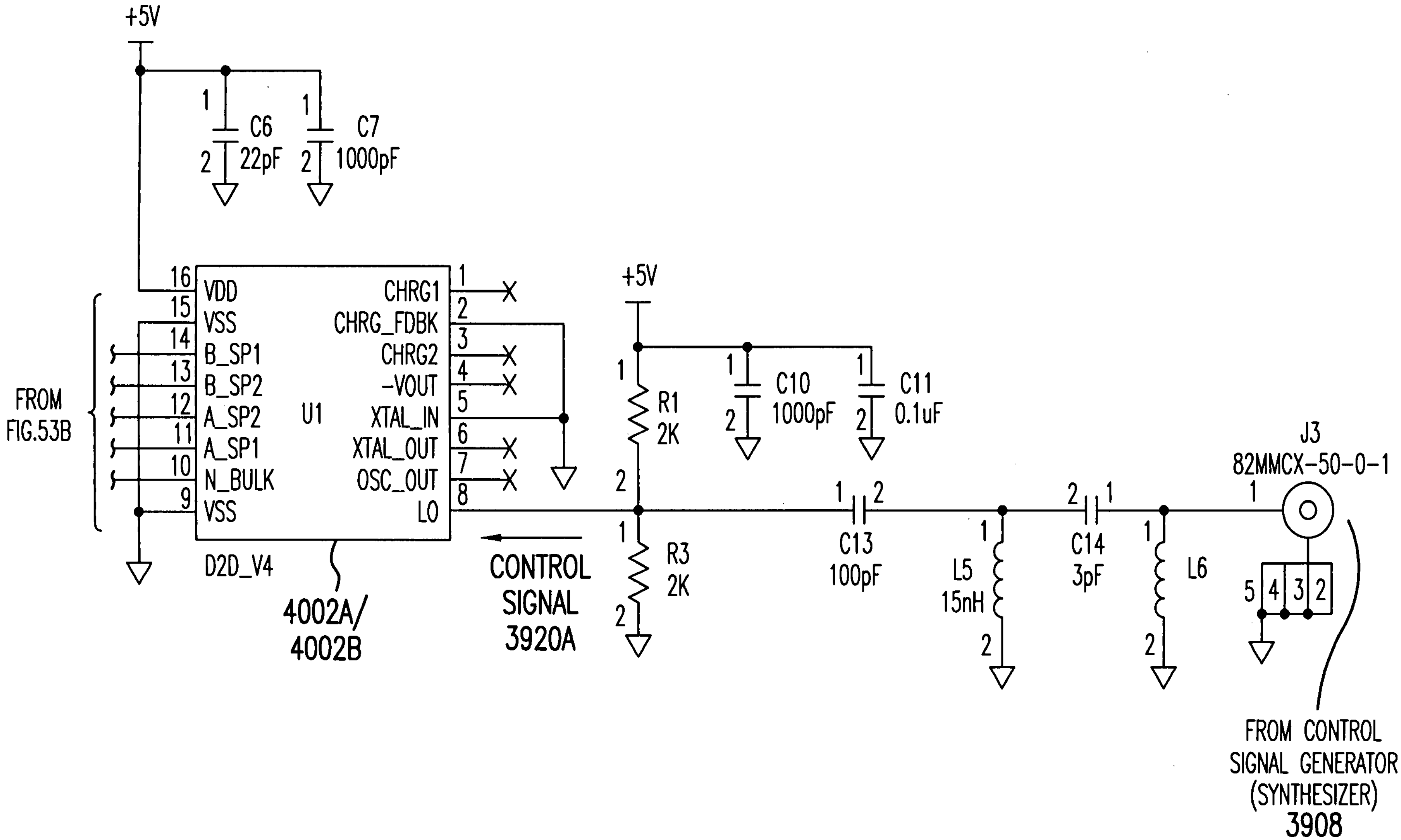
+5V
C6
22pF
C7
1000pF
VDD
VSS
B_SP1
B_SP2
A_SP2
A_SP1
N_BULK
VSS
CHRG1
CHRG_FDBK
CHRG2
-VOUT
XTAL_IN
XTAL_OUT
OSC_OUT
LO
U1
D2D_V4
FROM FIG.53B
4002A/ 4002B
CONTROL SIGNAL 3920A
+5V
R1
2K
R3
2K
C10
1000pF
C11
0.1uF
C13
100pF
L5
15nH
C14
3pF
L6
J3
82MMCX-50-0-1
FROM CONTROL SIGNAL GENERATOR (SYNTHESIZER)
3908

FIG.53C

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Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

ITEM	QTY	REFERENCE	PART	PART NIMBER	MANUFACTURER
1	10	C/R7,C/R15,C16,C17,C18	0.1uF	GRM39Y5V104Z016	MURATA
		C19,C21,C22,C23,C24			
2	6	C1,C3,C6,C8,C9,C12	22pF	GRM39COG220J050	MURATA
3	3	C2,C4,C11	0.1uF	GRM39X7R104K016	MURATA
4	2	C5,C15	47pF	GRM39COG470J050	MURATA
5	2	C10,C7	1000pF	GRM39X7R102K050	MURATA
6	1	C13	100pF	GRM39X7R101J050	MURATA
7	1	C14	3pF	GRM40COG030B50V	MURATA
8	2	C20,C25	1uF	GRM40Y5V105Z016	MURATA
9	1	JP1	69190-403	69190-403	BERG
10	1	JP2	69190-402	69190-402	BERG
11	4	J1,J2,J3,J4	82MMCX-50-0-1	82MMCX-50-0-1	SUHNER
12	2	L3,L1	DNP	L	TOKO
13	2	L4,L2	4.7nH	LL1608-F4N7K	TOKO
14	1	L5	15nH	LL2012FH15NJ	TOKO
15	1	L6	DNP	DNP	TOKO
16	2	Q1,Q2	BFR520	BFR520	PHILIPS
17	2	R1,R3	2K	ERJ3GSYJ202	PANASONIC
18	1	R2	51	ERJ3GSYJ510	PANASONIC
19	2	R4,R12	221	ERJ3EKF2210	PANASONIC
20	6	R5,R6,R8,R13,R14,R16	33.2K	ERJ3EKF3322	PANASONIC
21	2	R9,R17	DNP	ERJ3EKF1001	PANASONIC
22	2	R10,R18	249	ERJ3EKF2490	PANASONIC
23	2	R11,R19	10	ERJ3GSYJ100	PANASONIC
24	1	U1	D2D_V4	D2D_V4	PARKER VISION
25	1	U2	1X603	1X603	ANAREN
26	1	U3	AD8032AR	AD8032AR	ANALOG DEVICES
27	1		BOARD	STB500.641.001 V03.00	

FIG.54

Replacement Sheet
Sheet 81 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

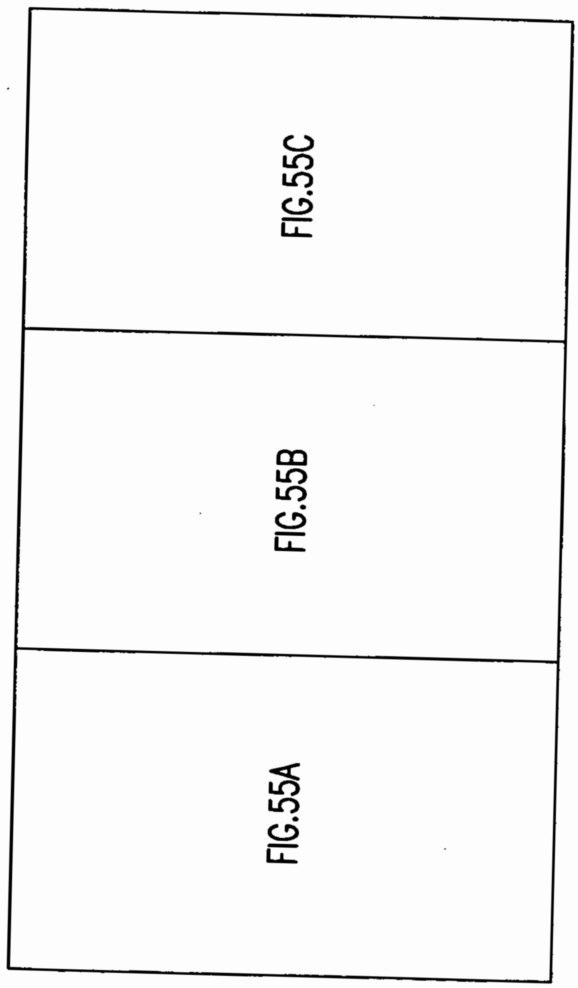

FIG.55

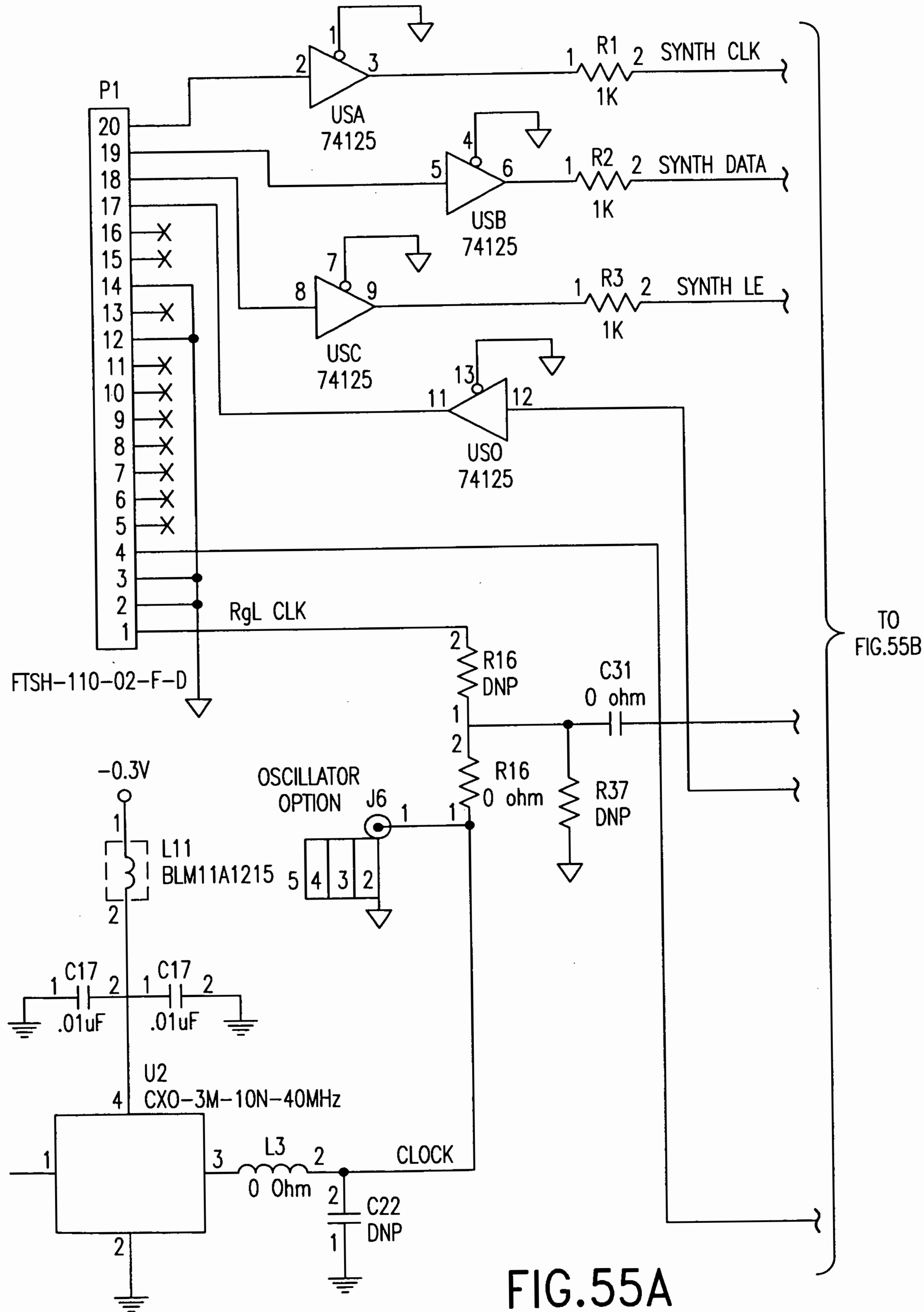
P1
FTSH-110-02-F-D
USA
74125
USB
74125
USC
74125
USO
74125
R1
1K
SYNTH CLK
R2
1K
SYNTH DATA
R3
1K
SYNTH LE
RgL CLK
R16
DNP
C31
0 ohm
R16
0 ohm
R37
DNP
OSCILLATOR
OPTION
J6
-0.3V
L11
BLM11A1215
C17
.01uF
C17
.01uF
U2
CXO-3M-10N-40MHz
L3
0 Ohm
CLOCK
C22
DNP
TO
FIG.55B

FIG.55A

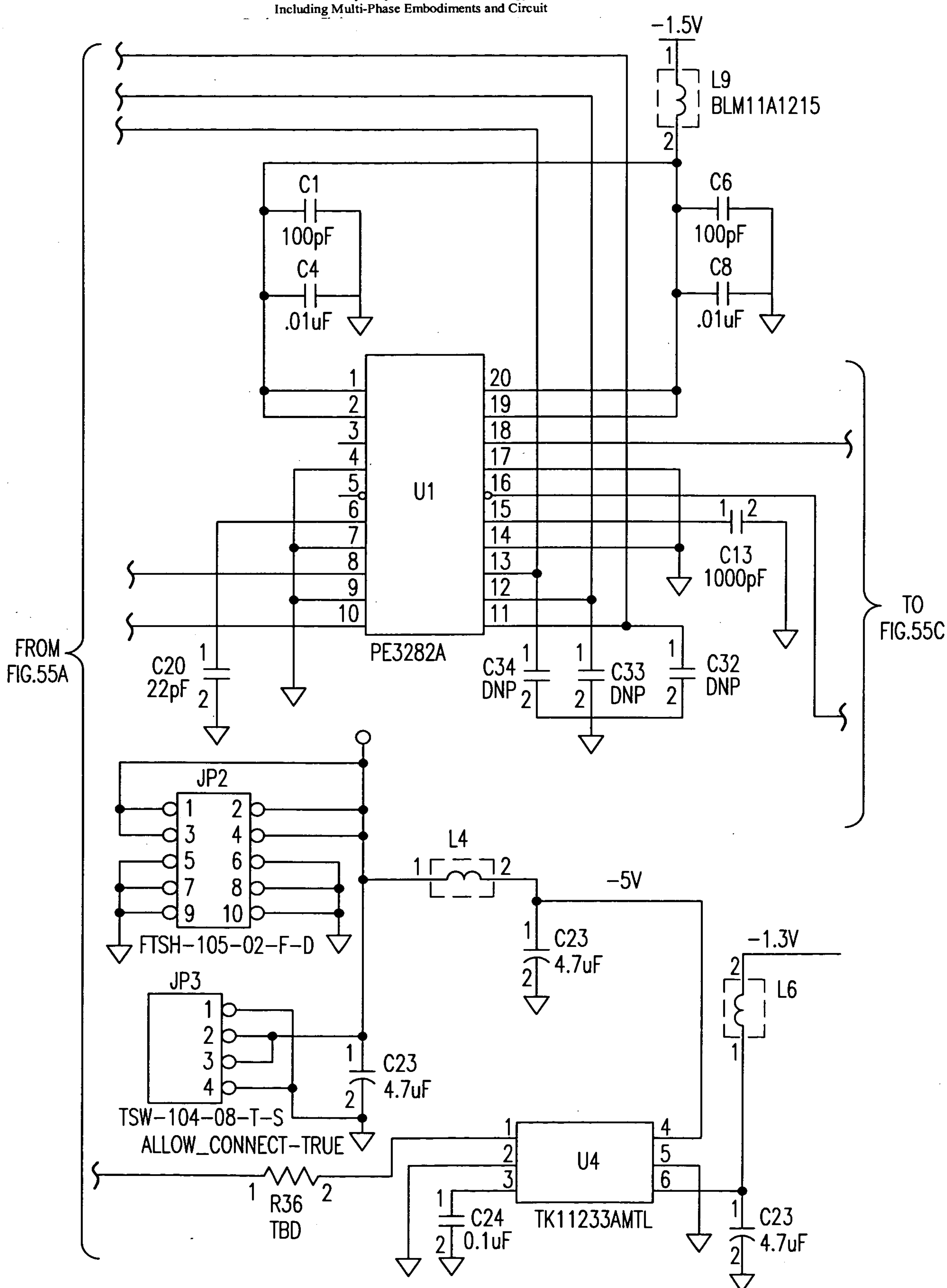
-1.5V
L9
BLM11A1215
C1
100pF
C4
.01uF
C6
100pF
C8
.01uF
U1
PE3282A
C13
1000pF
C20
22pF
C34
DNP
C33
DNP
C32
DNP
FROM
FIG.55A
TO
FIG.55C
JP2
FTSH-105-02-F-D
L4
-5V
C23
4.7uF
-1.3V
L6
JP3
TSW-104-08-T-S
ALLOW_CONNECT-TRUE
C23
4.7uF
U4
TK11233AMTL
R36
TBD
C24
0.1uF
C23
4.7uF

FIG.55B

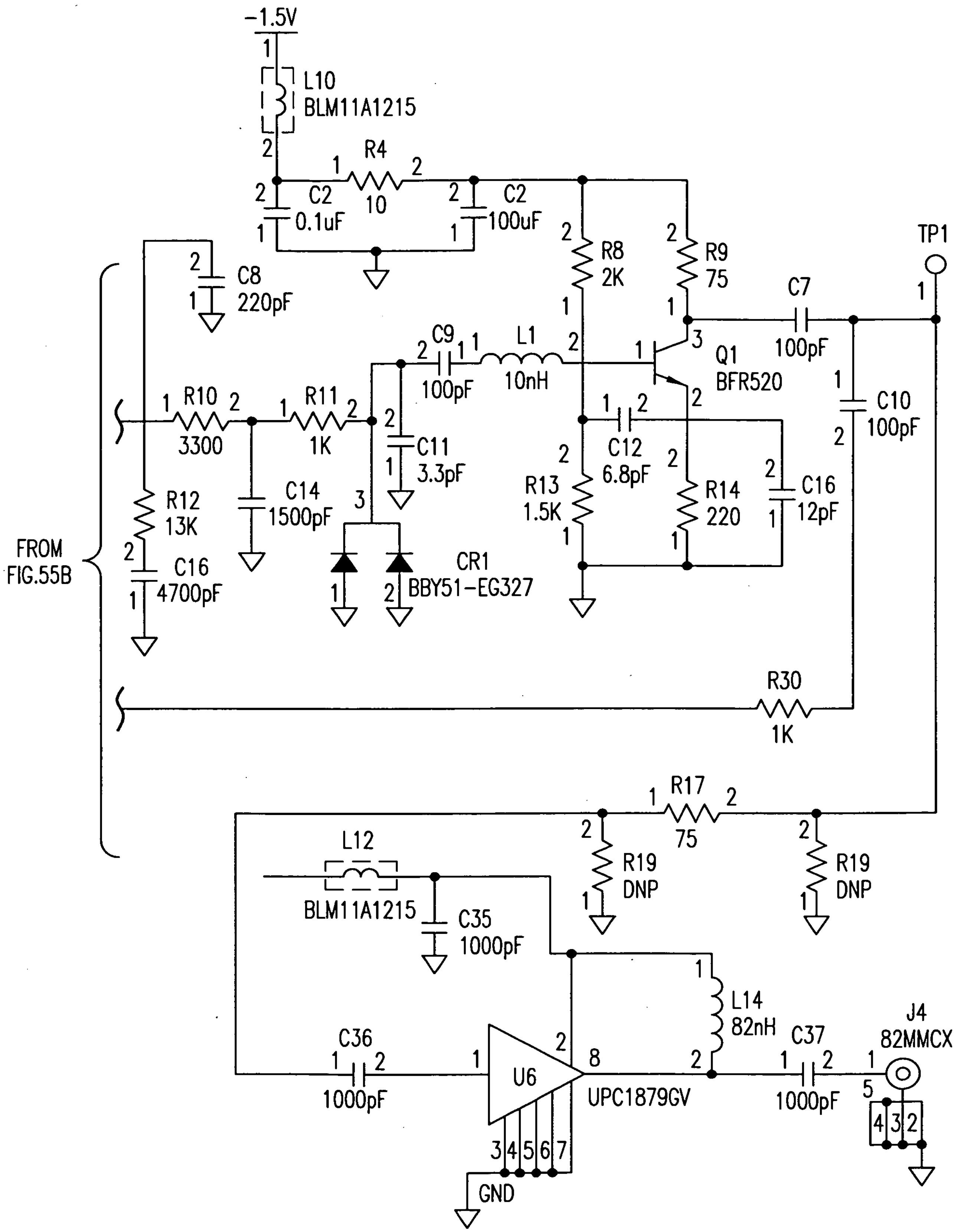
-1.5V
L10
BLM11A1215
R4
10
C2
0.1uF
C2
100uF
R8
2K
R9
75
TP1
C8
220pF
C7
100pF
C9
100pF
L1
10nH
Q1
BFR520
R10
3300
R11
1K
C11
3.3pF
C12
6.8pF
C10
100pF
R12
13K
C14
1500pF
R13
1.5K
R14
220
C16
12pF
FROM
FIG.55B
C16
4700pF
CR1
BBY51-EG327
R30
1K
R17
75
R19
DNP
R19
DNP
L12
BLM11A1215
C35
1000pF
L14
82nH
J4
82MMCX
C36
1000pF
U6
UPC1879GV
C37
1000pF
GND

FIG.55C

ITEM	QTY	REFERENCE	PART	DESCRIPTION	PART NUMBER	MANUFACT.
1	1	CR1	BBY51-E6327	DIODE,VARACTOR	BBY51-E6327	SIEMENS
2	6	C1,C3,C5,C7,C9,C10	100pF	CAPACITOR,CERAMIC,100pF,10%,C0G,0603	GRM39C0G101K050	MURATA
3	2	C29,C2	0.1uF	CAPACITOR,CERAMIC,.1uF,10%,X7R,0603	GRM39X7R104K016AD	MURATA
4	3	C4,C8,C17	.01uF	CAPACITOR,CERAMIC,.01uF,10%,X7R,0603	GRM39X7R103K050	MURATA
5	1	C6	220pF	CAPACITOR,CERAMIC,220pF,5%,C0G,0603	GRM39C0G221J025	MURATA
6	1	C11	3.3pF	CAPACITOR,CERAMIC,3.3pF,5%,C0G,0603	GRM39C0G3R3B100V	MURATA
7	1	C12	6.8pF	CAPACITOR,CERAMIC,6.8pF,+/-.25pF,C0G,0603	GRM39C0G6R8C100V	MURATA
8	4	C13,C35,C36,C37	1000pF	CAPACITOR,CERAMIC,1000pF,10%,X7R,0603	GRM39X7R102K016	MURATA
9	1	C14	1500pF	CAPACITOR,CERAMIC,1500Pf,10%,X7R,0603	GRM39X7R152K016	MURATA
10	1	C15	12pF	CAPACITOR,CERAMIC,12pF,5%,C0G,0603	GRM39C0G120J050	MURATA
11	1	C16	4700pF	CAPACITOR,CERAMIC,4700pF,10%,0603	GRM39X7R472K016	MURATA
12	2	C20,C18	22pF	CAPACITOR,CERAMIC,22pF,10%,C0G,0603	GRM36C0G220K050	MURATA
13	4	C22,C32,C33,C34	DNP	CAPACITOR,CERAMIC,,,,0603		MURATA
14	3	C23,C24,C27	4.7uF	CAPACITOR,TANTALUM,4.7uF,10%,3216	T491A475K006AS	KEMET
15	3	R16,C31,R17	0 OHM	RESISTOR,ZERO OHM,0603	ERJ3GSY0R00	PANASONIC
16	1	JP1	FTSH-110-02-F-D	HEADER,DUAL ROW 10X2,.050X.050	FTSH-110-02-F-D	SAMTEC
17	1	JP2	FTSH-105-02-F-D	HEADER,DUAL ROW 5X2,.050X.050	FTSH-105-02-F-D	SAMTEC
18	1	JP3	TSW-104-08-T-S	HEADER, SINGLE ROW 4 PIN, .100"	TSW-104-08-T-S	BERG
19	2	J5,J6	82MMCX	RF CONNECTOR	82MMCX-50-0-1	SUHNER
20	1	L1	18nH	INDUCTOR,18nH,10%, 0805	0805CS-180XJBC	COILCRAFT
21	1	L3	0 OHM	ZERO OHM JUMPER	RM73ZIJT	KOA
22	6	L4,L6,L9,L10,L11,L12	BLM11A121S	FERRITE BEAD, 0603	BLM11A121S	MURATA
23	1	L14	82nH	INDUCTOR, 82nH,10%,0805	LL2012-F82NK	TOKO
24	1	Q1	BFR520	TRANSISTOR, NPN	BFR520	PHILIPS
25	5	R1,R2,R3,R11,R30	1K	RESISTOR, 1K,5%,0603	ERF3GSYJ102	PANASONIC
26	1	R4	10	RESISTOR, 10 OHM,5%,0603	ERJ3GSYJ1R0	PANASONIC

FIG.56A

Replacement Sheet
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Dkt No. 1744.0630003; Group Unit: 2634
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For: Wireless Local Area Network (WLAN) Using
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Including Multi-Phase Embodiments and Circuit

27	1	R8	2K	RESISTOR, 2K,5%,0603	ERJ3GSYJ202	PANASONIC
28	1	R9	75	RESISTOR, 75 OHM,5%,0603	ERJ3GSYJ750	PANASONIC
29	1	R10	3300	RESISTOR, 3.3K,5%,0603	ERJ3GSYJ332	PANASONIC
30	1	R12	13K	RESISTOR, 13K,5%,0603	ERJ3GSYJ133	PANASONIC
31	1	R13	1.5K	RESISTOR, 1.5K,5%,0603	ERJ3GSYJ152	PANASONIC
32	1	R14	220	RESISTOR, 220 OHM,5%,0603	ERJ3GSYJ221	PANASONIC
33	1	R15	DNP	RESISTOR, ZERO OHM,0603	ERJ3GSY0R00	PANASONIC
34	2	R18,R19	DNP	RESISTOR, 91 OHM,5%,0603	ERJ3GSYJ910	PANASONIC
35	1	R36	TBD	RESISTOR, ZERO OHM,0603	ERJ3GSY0R00	PANASONIC
36	1	R37	DNP	RESISTOR,,,0603		PANASONIC
37	1	TP1	TEST POINT			
38	1	U1	PE3282A	IC,SYNTHESIZER	PE3282A	PEREGRINE
39	1	U2	CXO-3M-10N-40MHz	XTAL OSC,40MHz	CXO-3M-10N-40MHZ A/I	STATEK
40	1	U4	TK11233AMTL	VOLTAGE REGULATOR,3.5V	TK11235BM	TOKO
41	1	U5	74125	IC,BUFFER	MC74LCX125DT	MOTOROLA
42	1	U6	UPC1678GV	IC,RF AMPLIFIER	UPC1678GV	NEC
43	1		STB500.641.008 V03.00	BOARD		

FIG.56B

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Sheet 86 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

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Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

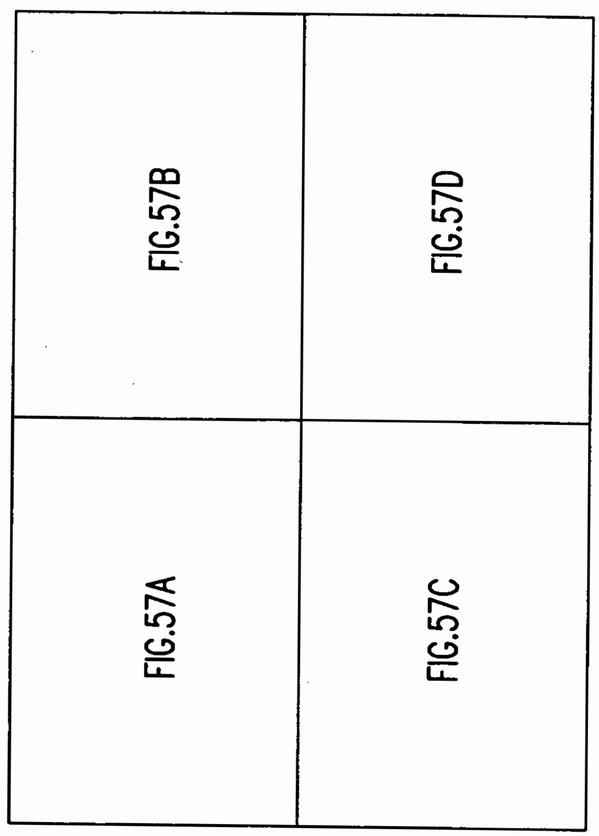

FIG.57

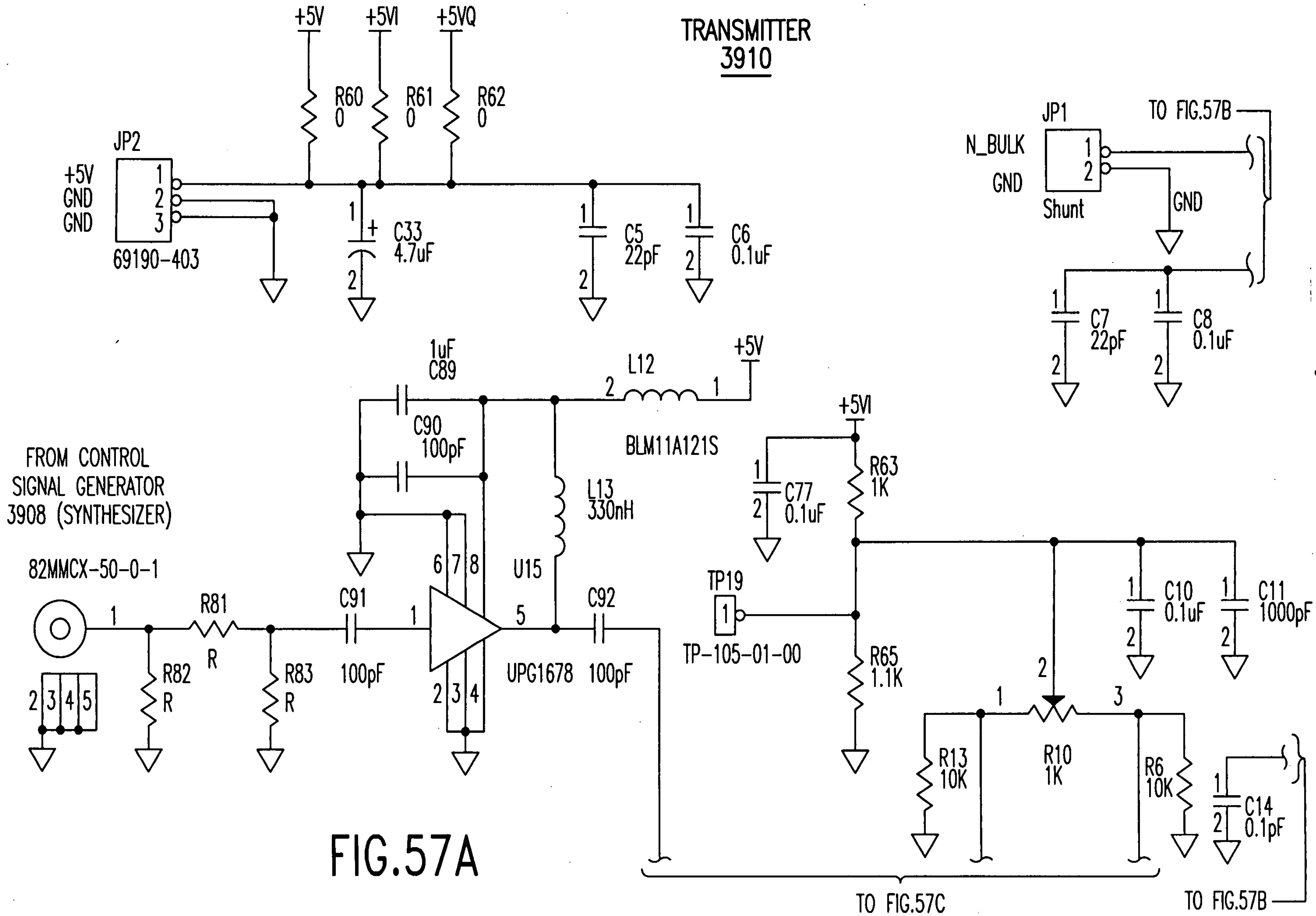

FIG.57A

New Sheet
Sheet 88 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

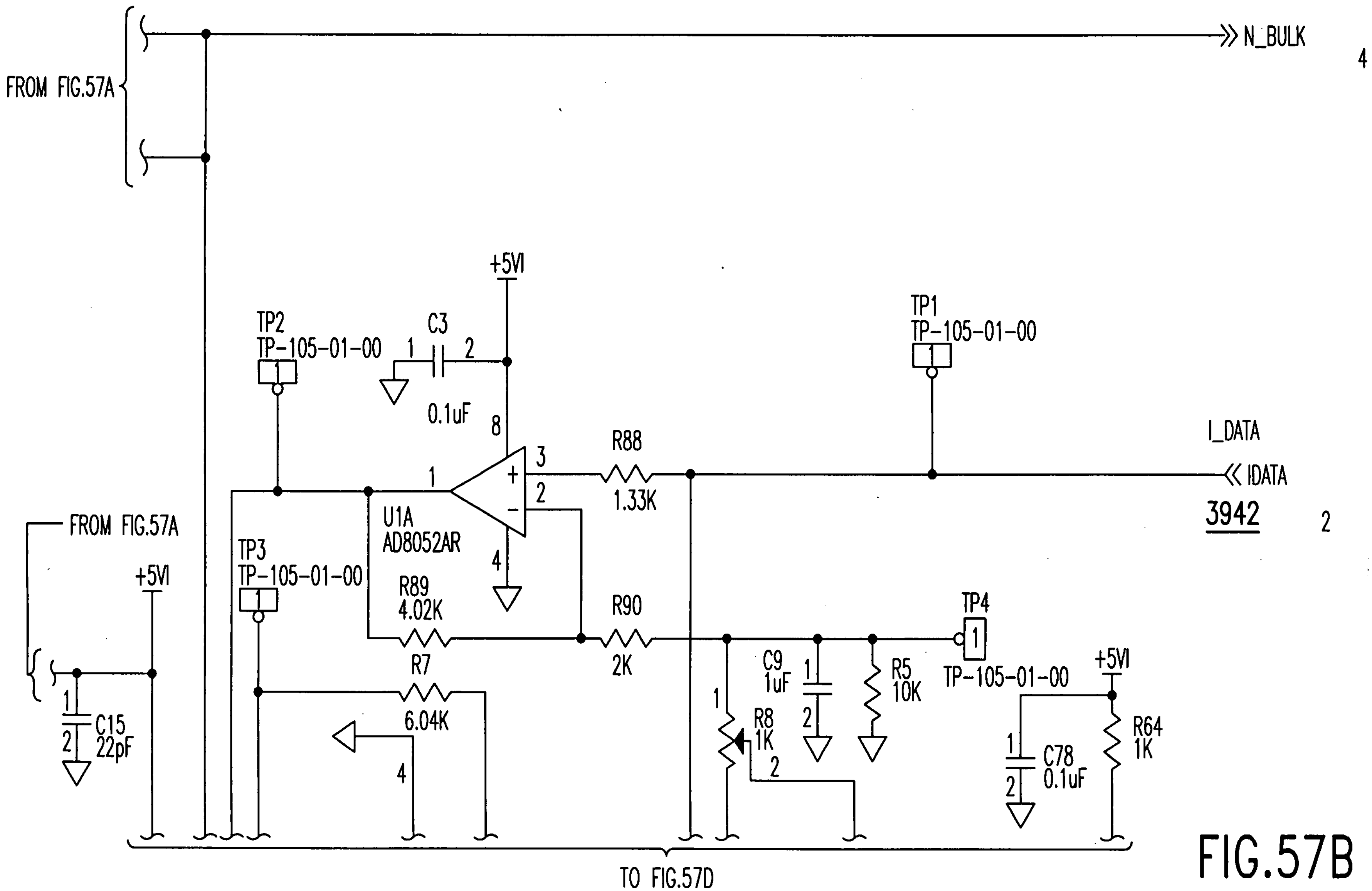

FIG.57B

New Sheet
Sheet 89 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

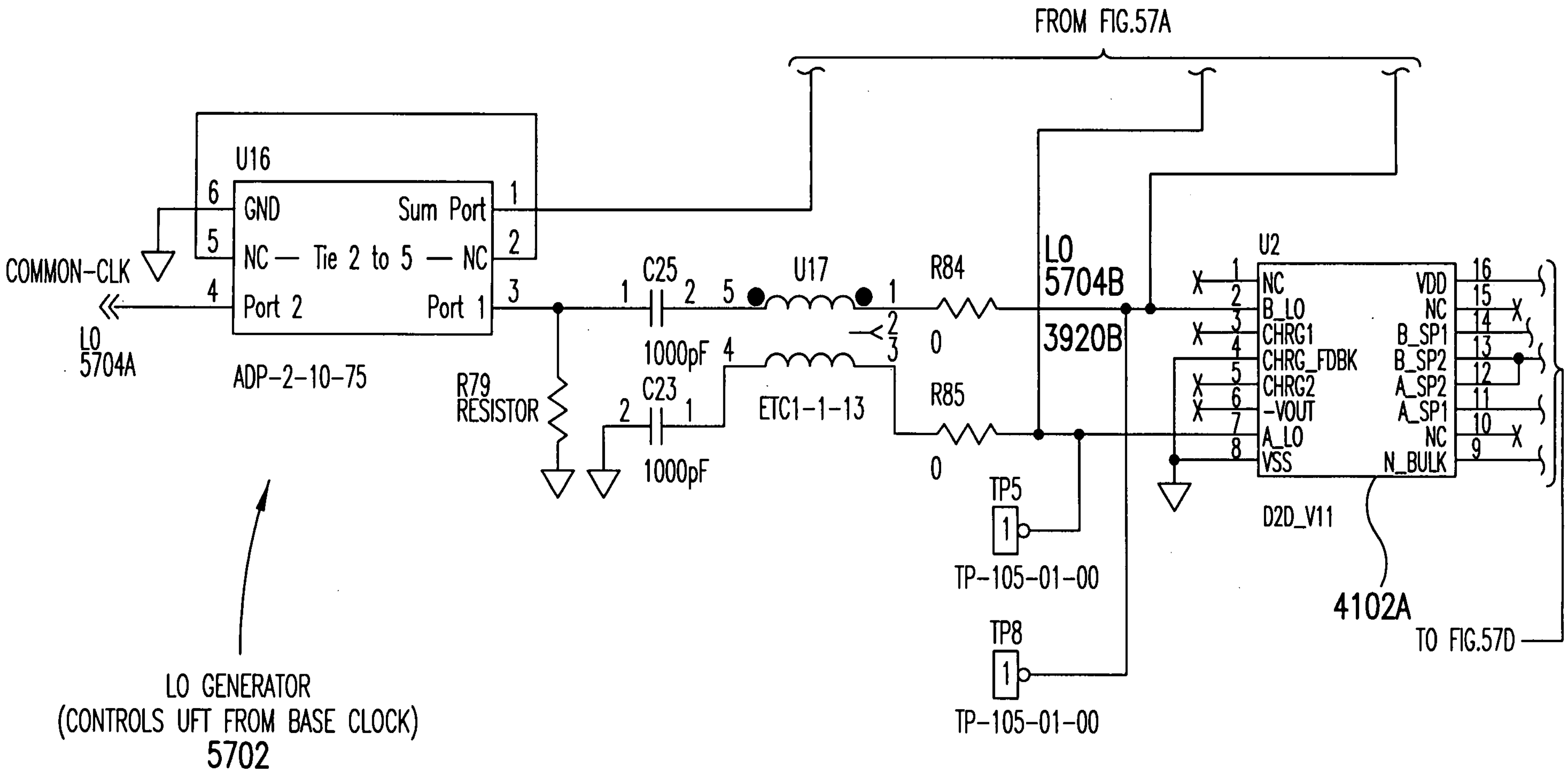

FIG.57C

New Sheet
Sheet 90 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.063003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

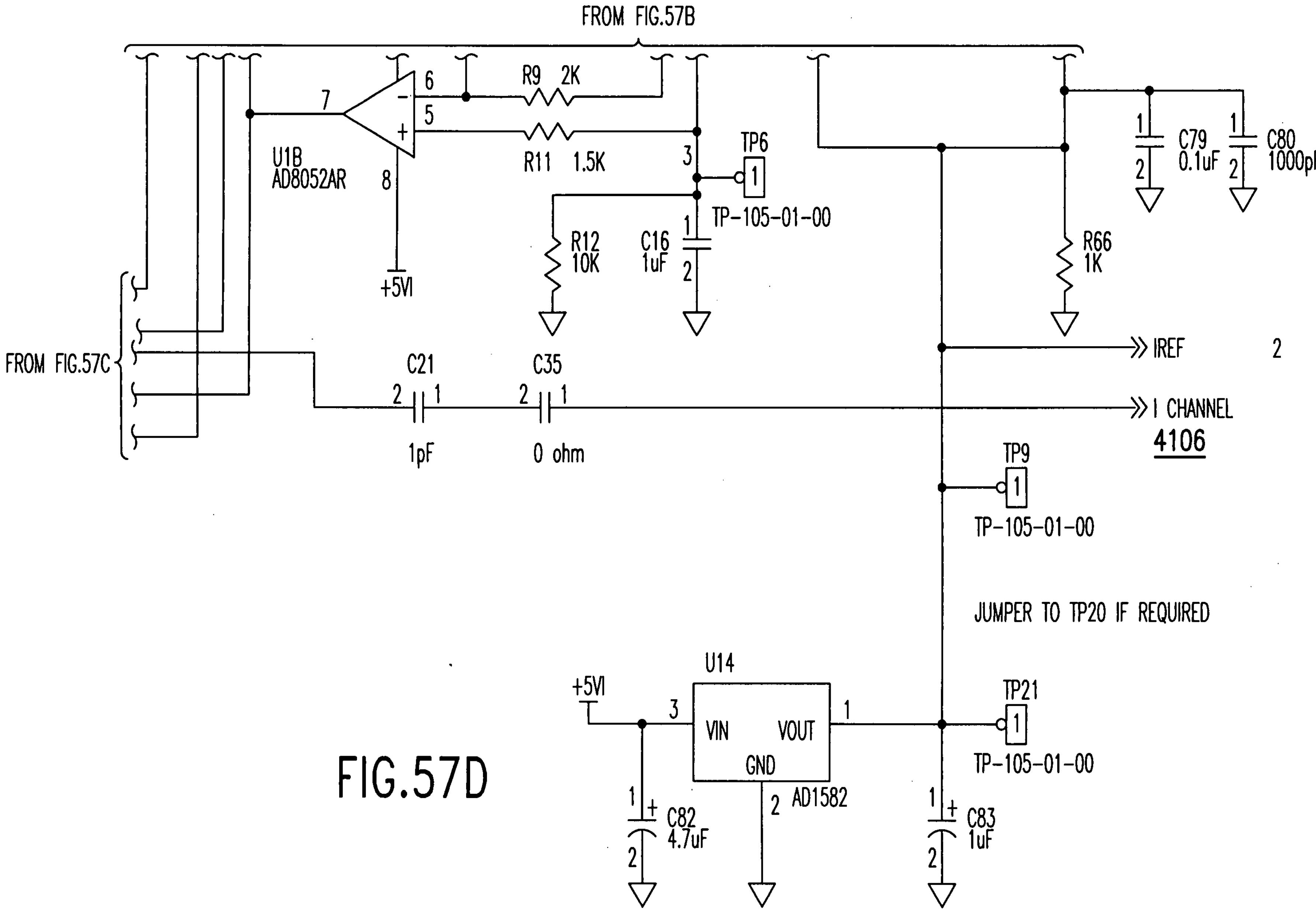

FIG.57D

New Sheet
Sheet 91 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.063003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

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Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

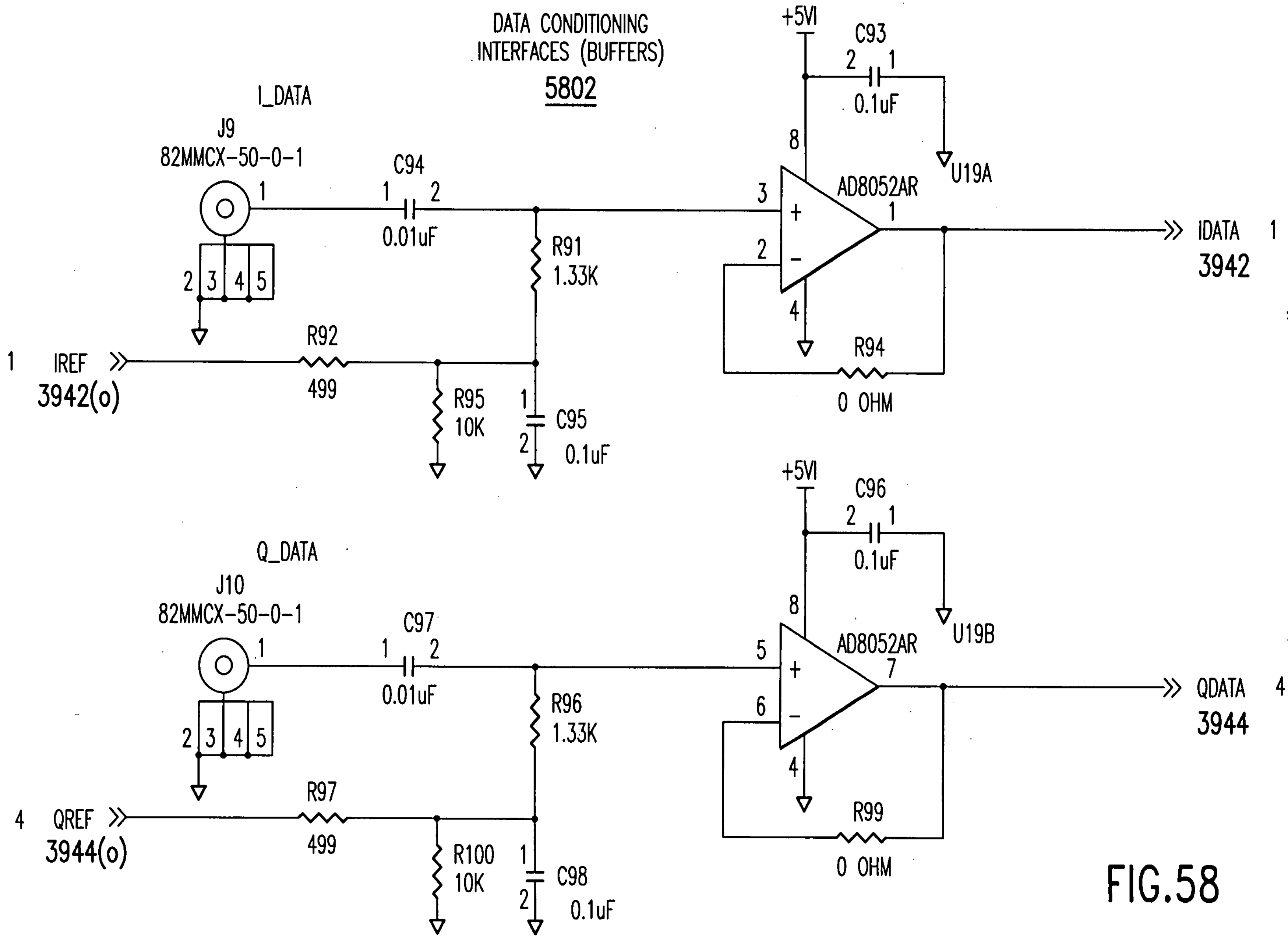

FIG.58

Replacement Sheet
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Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

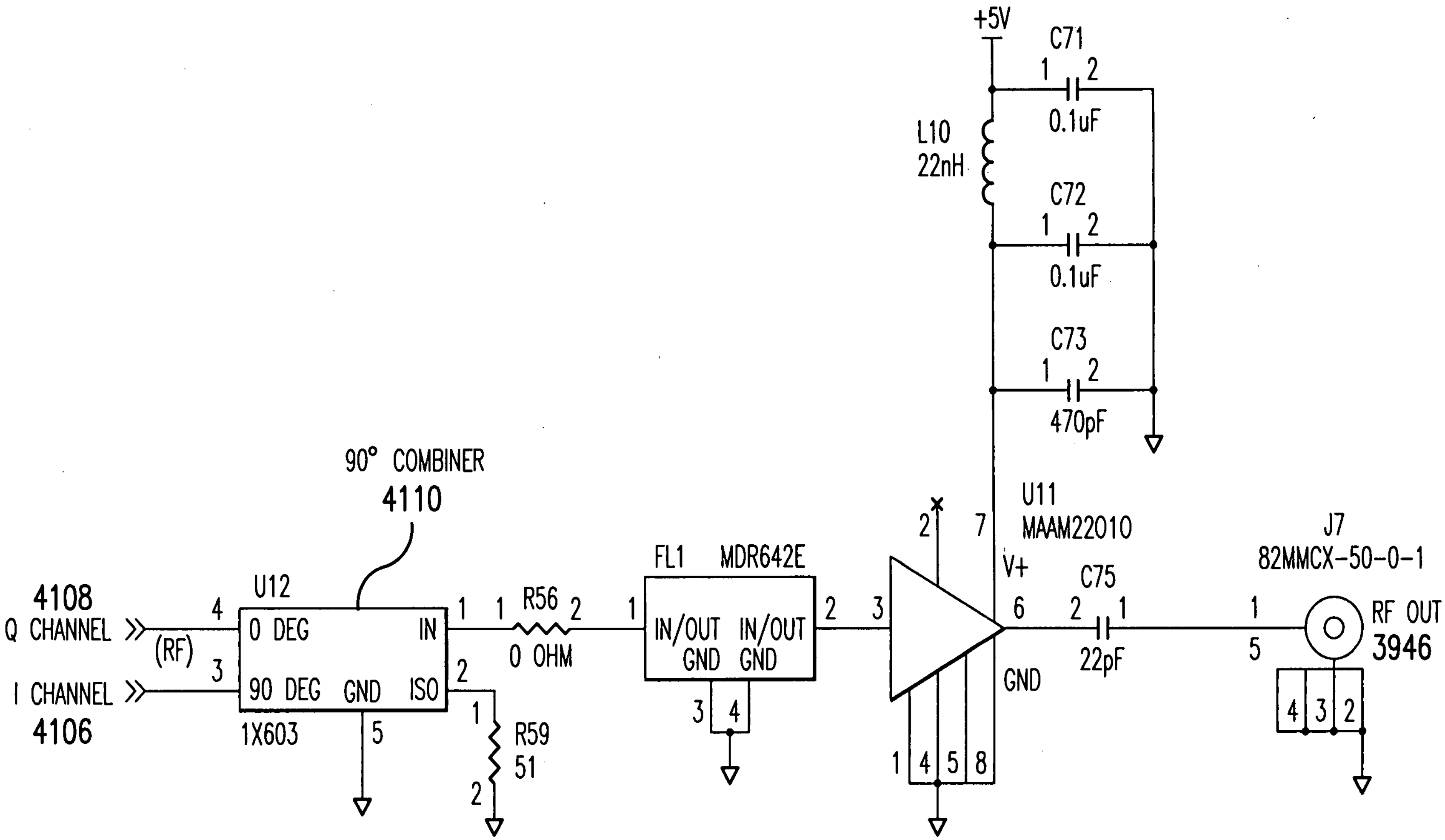

FIG.59

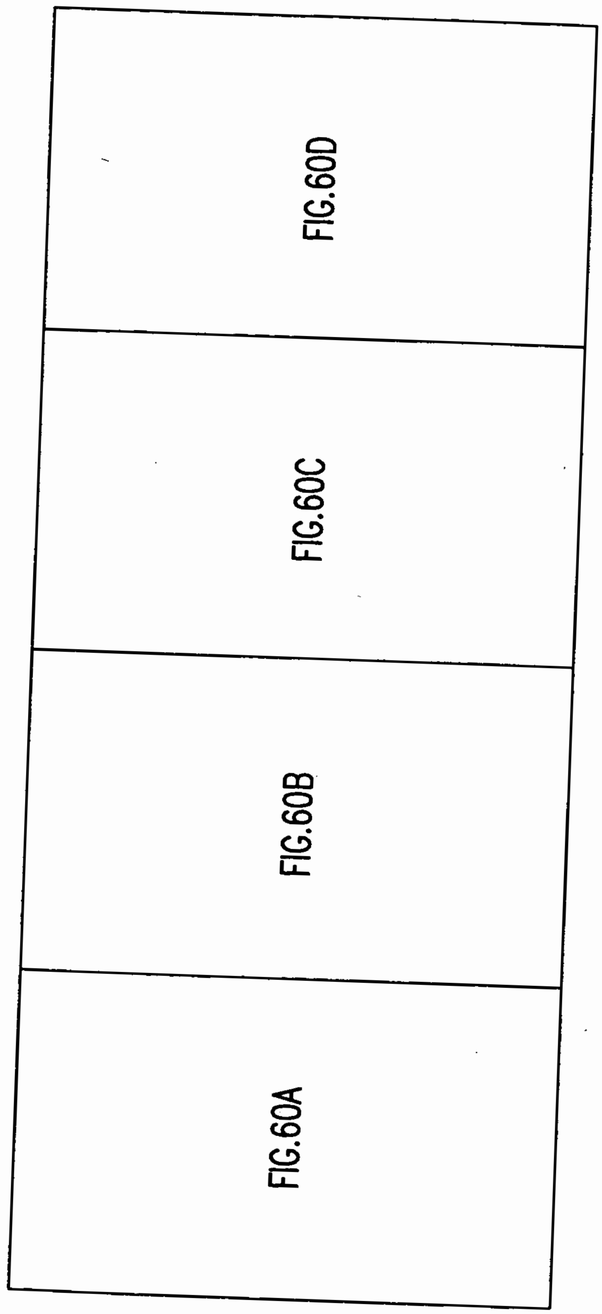

FIG.60

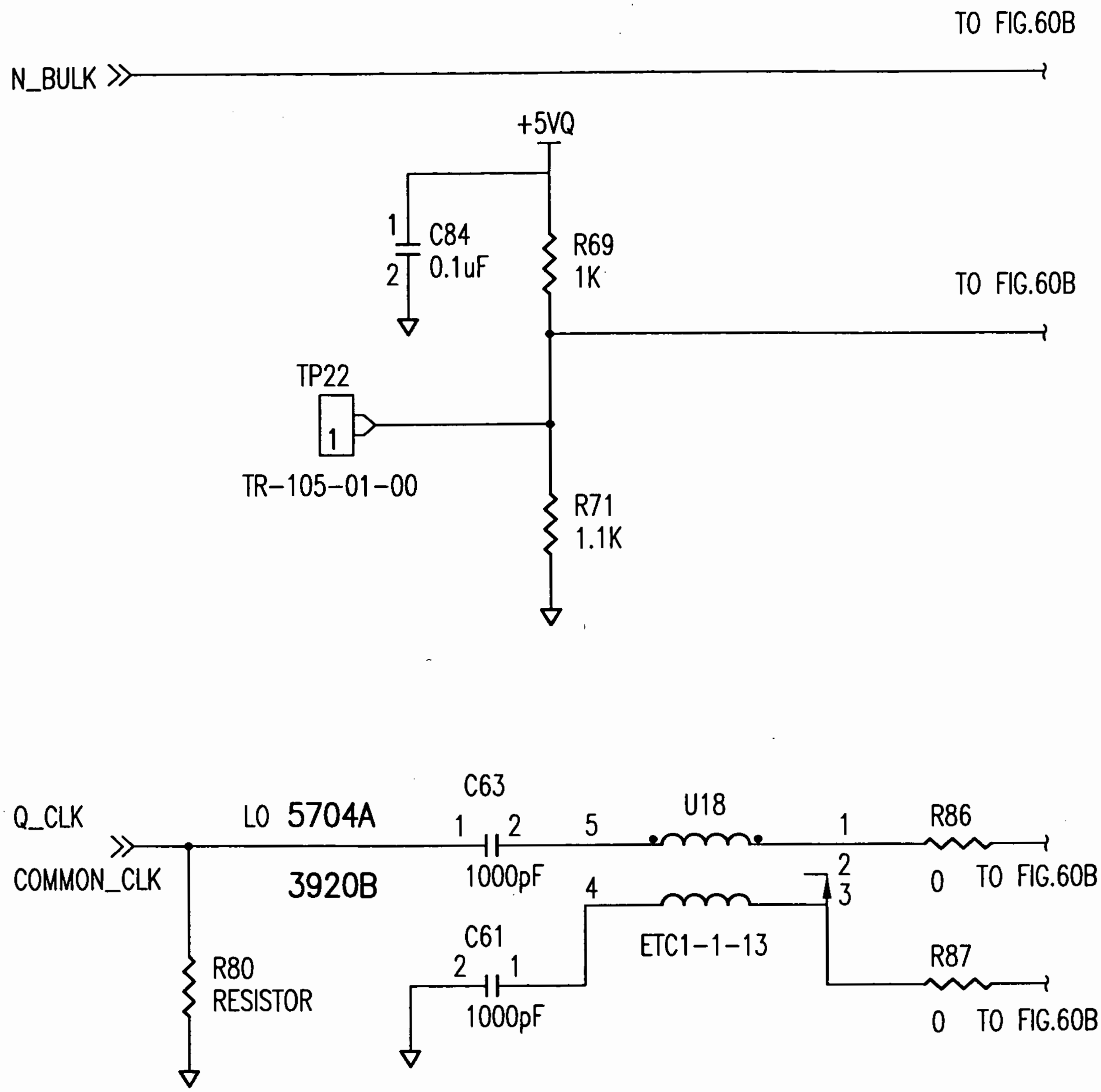
TO FIG.60B
N_BULK
+5VQ
C84
0.1uF
R69
1K
TO FIG.60B
TP22
TR-105-01-00
R71
1.1K
Q_CLK
COMMON_CLK
LO 5704A
3920B
C63
1000pF
U18
ETC1-1-13
R86
0 TO FIG.60B
C61
1000pF
R87
0 TO FIG.60B
R80
RESISTOR

FIG.60A

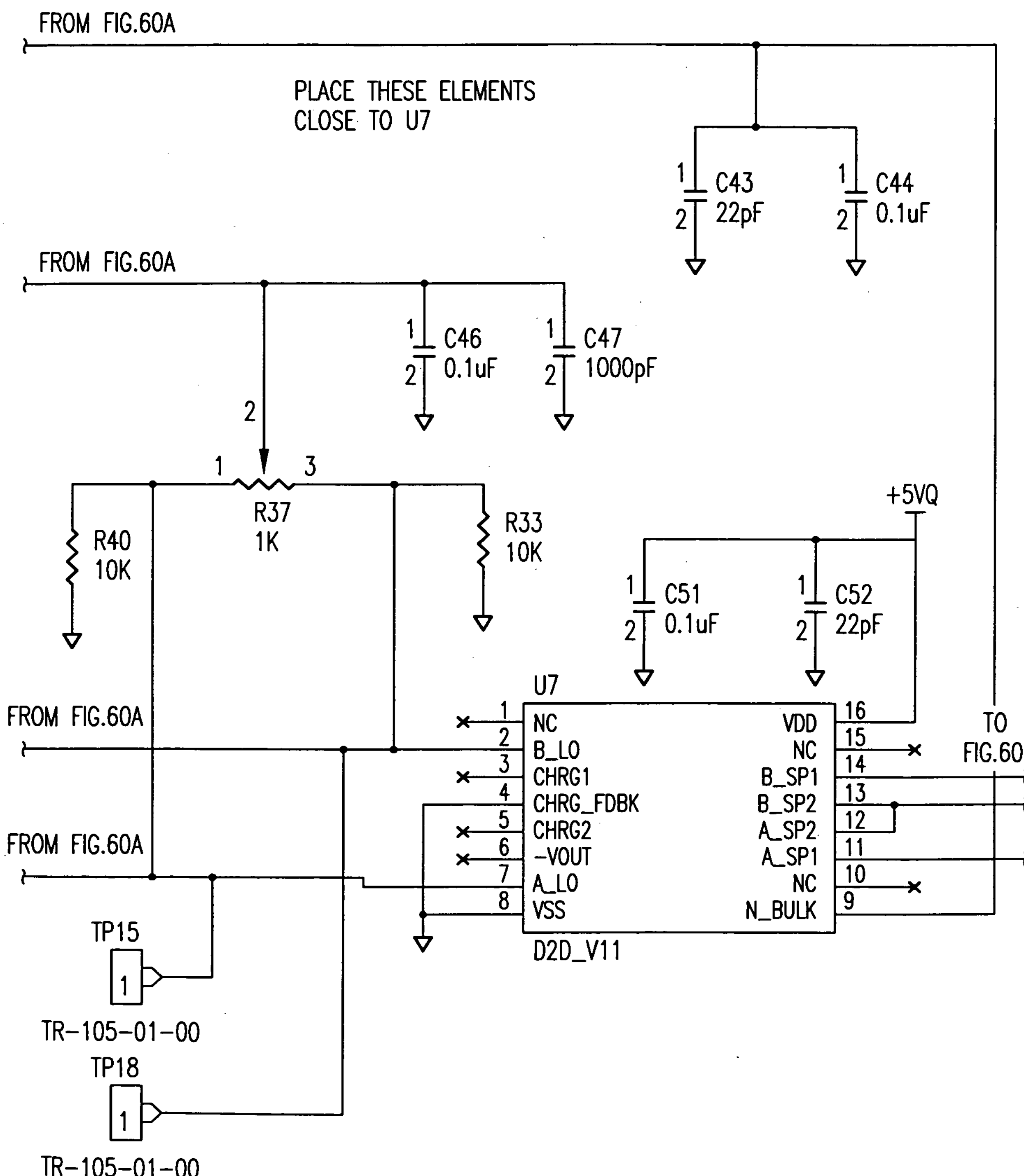
FROM FIG.60A
PLACE THESE ELEMENTS
CLOSE TO U7
C43
22pF
C44
0.1uF
FROM FIG.60A
C46
0.1uF
C47
1000pF
R37
1K
R40
10K
R33
10K
+5VQ
C51
0.1uF
C52
22pF
U7
FROM FIG.60A
FROM FIG.60A
NC
B_LO
CHRG1
CHRG_FDBK
CHRG2
-VOUT
A_LO
VSS
VDD
NC
B_SP1
B_SP2
A_SP2
A_SP1
NC
N_BULK
TO
FIG.60C
D2D_V11
TP15
TR-105-01-00
TP18
TR-105-01-00

FIG.60B

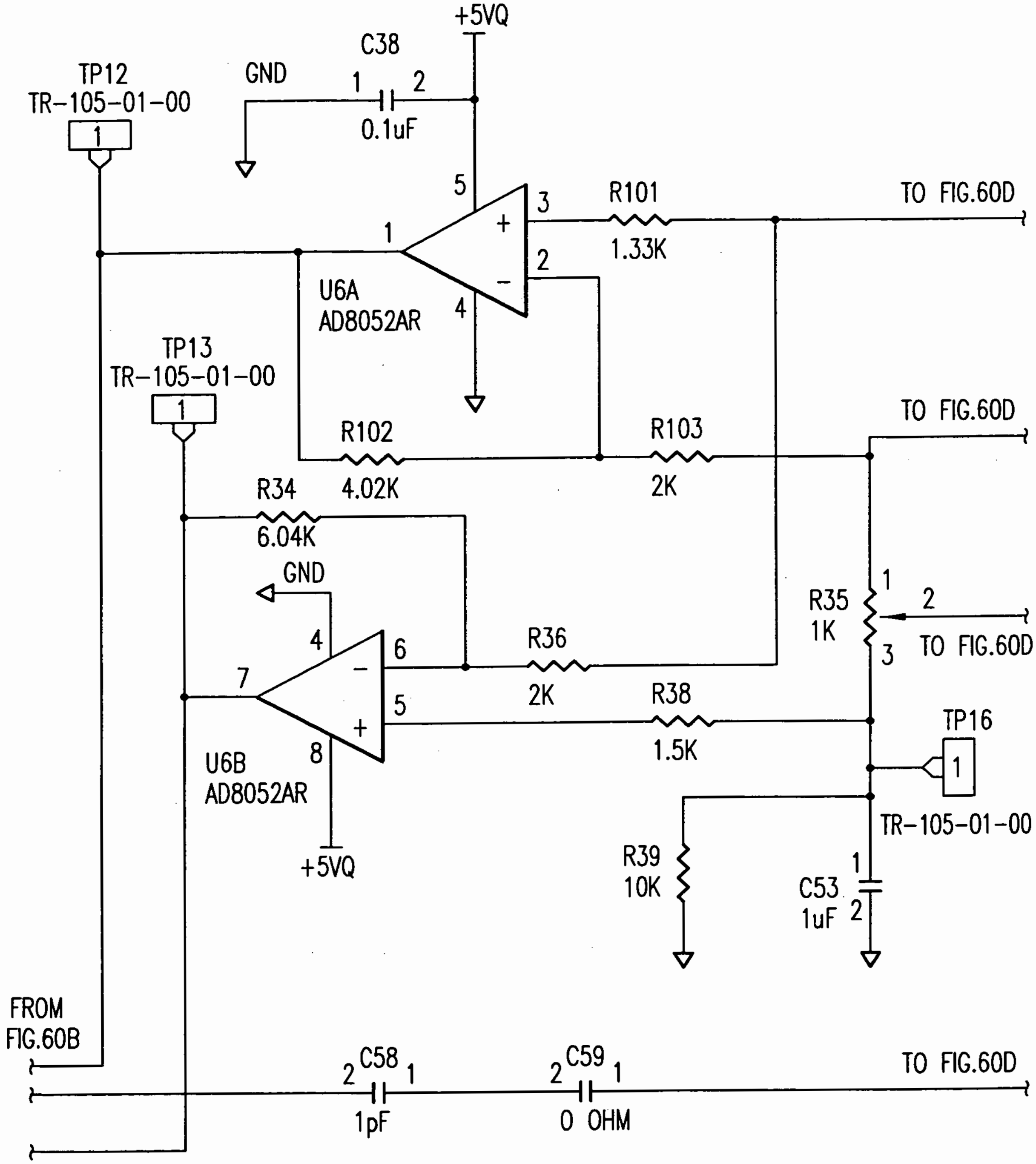
+5VQ
C38
GND
1
2
0.1uF
TP12
TR-105-01-00
1
5
3
R101
TO FIG.60D
1.33K
1
2
U6A
AD8052AR
4
TP13
TR-105-01-00
1
R102
4.02K
R103
2K
TO FIG.60D
R34
6.04K
GND
1
R35
1K
2
3
TO FIG.60D
4
6
R36
2K
7
5
R38
1.5K
TP16
1
U6B
AD8052AR
8
TR-105-01-00
+5VQ
R39
10K
C53
1uF
FROM
FIG.60B
C58
1pF
C59
0 OHM
TO FIG.60D

FIG.60C

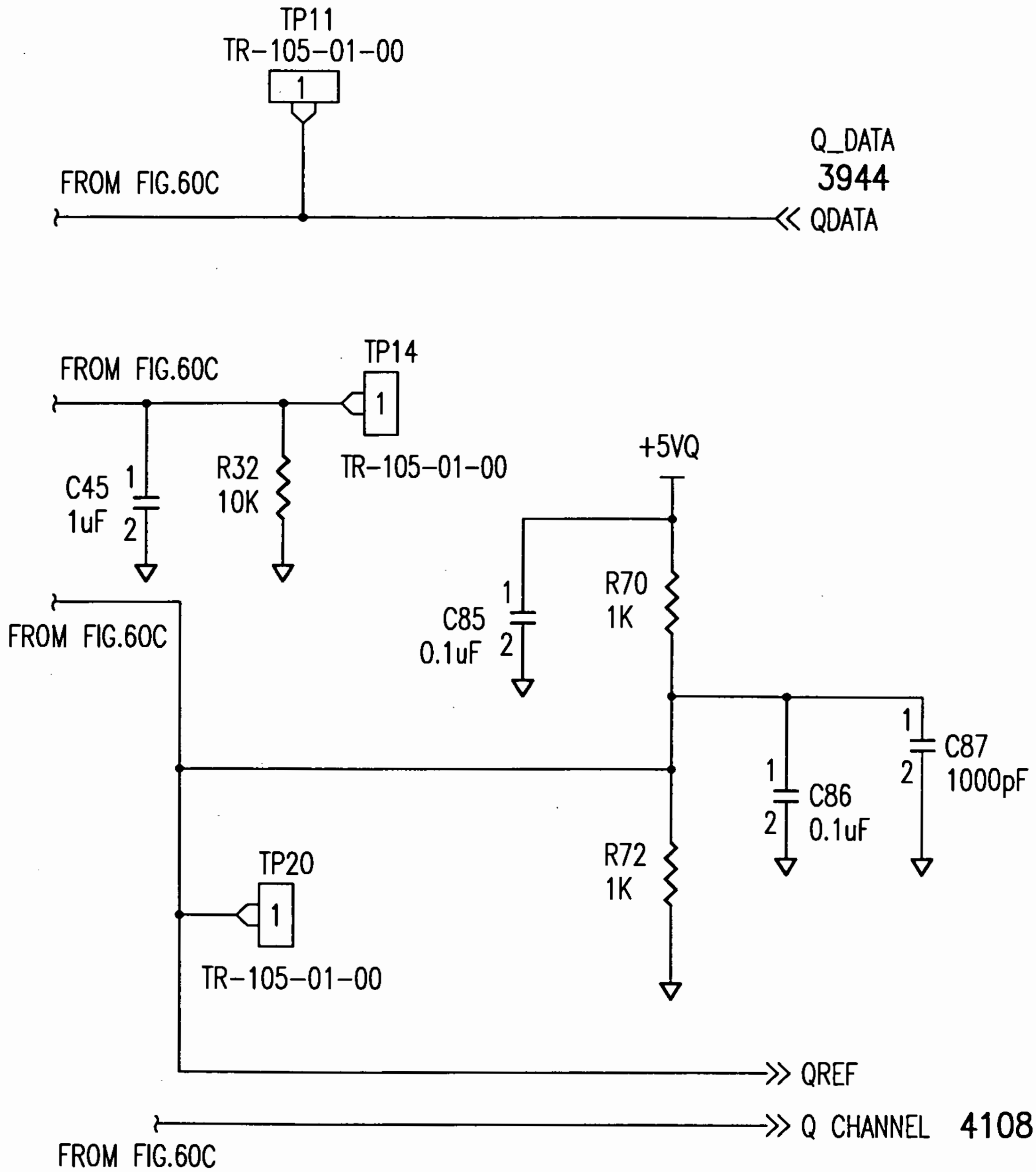
TP11
TR-105-01-00
1
FROM FIG.60C
Q_DATA
3944
QDATA
FROM FIG.60C
TP14
1
TR-105-01-00
C45
1uF
1
2
R32
10K
+5VQ
FROM FIG.60C
C85
0.1uF
1
2
R70
1K
C87
1000pF
1
2
C86
0.1uF
1
2
R72
1K
TP20
1
TR-105-01-00
QREF
Q CHANNEL
4108
FROM FIG.60C

FIG.60D

ITEM	QTY	REFERENCE	PART	PART NUMBER	MANUFACTURER
1	21	C3,C6,C8,C10,C14,C38,C44,	0.1uF	GRM39X7R104K016	MURATA
		C46,C51,C71,C72,C77,C78,			
		C79,C84,C85,C86,C93,C95,			
		C96,C98			
2	6	C5,C7,C15,C43,C52,C75	22pF	GRM39COG220J050	MURATA
3	5	C9,C16,C45,C53,C89	1uF	GRM40Y5V105Z016	MURATA
4	8	C11,C23,C25,C47,C61,C63	1000pF	GRM39X7R102K050	MURATA
		C80,C87			
5	2	C58,C21	1pF	GRM39COG010B50V	MURATA
6	2	C82,C33	4.7uF	T491A475K006AS	KEMET
7	2	C59,C35	0 ohm	GRM39COGxxxx50V	MURATA
8	1	C73	470pF	GRM39COG471J050	MURATA
9	1	C83	1uF	T491A105M016AS	KEMET
10	3	C90,C91,C92	100pF	ECU-V1H101JCV	
11	2	C94,C97	0.01uF	GRM39X7R103K016	MURATA
12	1	FL1	MDR642E	MDR642E	SOSHIN
13	1	JP1	Shunt	69190-402	BERG
14	1	JP2	69190-403	69190-403	BERG
15	4	J7,J8,J9,J10	82MMCX-50-0-1	82MMCX-50-0-1	SUHNER
16	1	L10	22nH	LL1608-F22NK	COILCRAFT
17	1	L12	BLM11A121S	BLM11A121S	MURATA
18	1	L13	330nH	LL2012-FR33K	
19	10	R5,R6,R12,R13,R32,R33,	10K	ERJ3EKF1002	PANASONIC
		R39,R40,R95,R100			
20	2	R34,R7	6.04K	ERJ3EKF6041	PANASONIC
21	4	R8,R10,R35,R37	1K	3224W-1-102	BOUMS
22	4	R9,R36,R90,R103	2K	ERJ3EKF2001	PANASONIC
23	2	R38,R11	1.5K	ERJ3EKF1501	PANASONIC
24	3	R56,R94,R99	0 ohm	ERJ3GSY0R00	PANASONIC

FIG.61A

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Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

25	1	R59	51	ERJ3GSYJ510	PANASONIC
26	7	R60,R61,R62,R84,R85,R86,	0	ERJ3GSY0R00	PANASONIC
		R87			
27	6	R63,R64,R66,R69,R70,R72	1K	ERJ3EKF1001	PANASONIC
28	2	R71,R65	1.1K	ERJ3EKF1101	PANASONIC
29	2	R80,R79	RESISTOR		
30	3	R81,R82,R83	R		
31	4	R88,R91,R96,R101	1.33K	ERJ3EKF1331	PANASONIC
32	2	R102,R89	4.02K	ERJ3EKF4021	PANASONIC
33	2	R92,R97	499	ERJ3EKF4990	PANASONIC
34	19	TP1,TP2,TP3,TP4,TP5,TP6,	TP-105-01-00		
		TP8,TP9,TP11,TP12,TP13,			
		TP14,TP15,TP16,TP18,TP19,			
		TP20,TP21,TP22			
35	3	U1,U6,U19	AD8052AR	AD8052AR	ANALOG DEVICES
36	2	U7,U2	D2D_V11	D2D_V11	PARKER VISION
37	1	U11	MAAM22010	MAAM22010	MACOM
38	1	U12	1X603	1X603	ANAREN
39	1	U14	AD1582	AD1582	ANALOG DEVICES
40	1	U15	UPG1678	UPG1678GV	NEC
41	1	U16	ADP-2-10-75	ADP-2-10-75	MINI-CIRCUITS
42	1		BOARD	8500.641.021	V05.10

FIG.61B

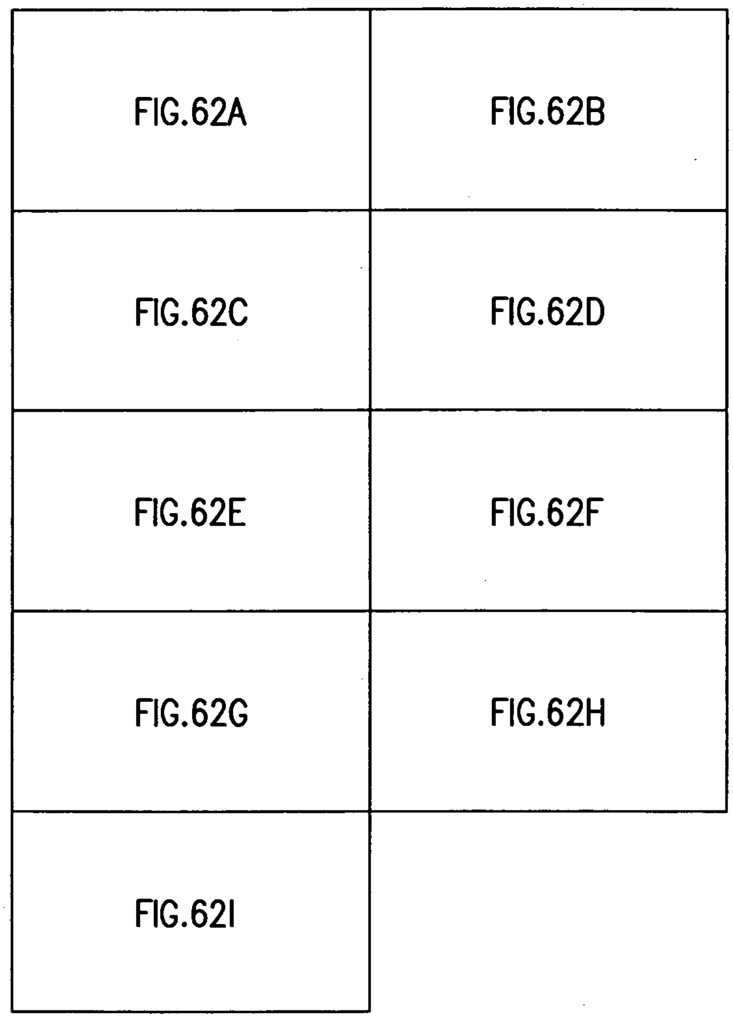
FIG.62A
FIG.62B
FIG.62C
FIG.62D
FIG.62E
FIG.62F
FIG.62G
FIG.62H
FIG.62I

FIG. 62

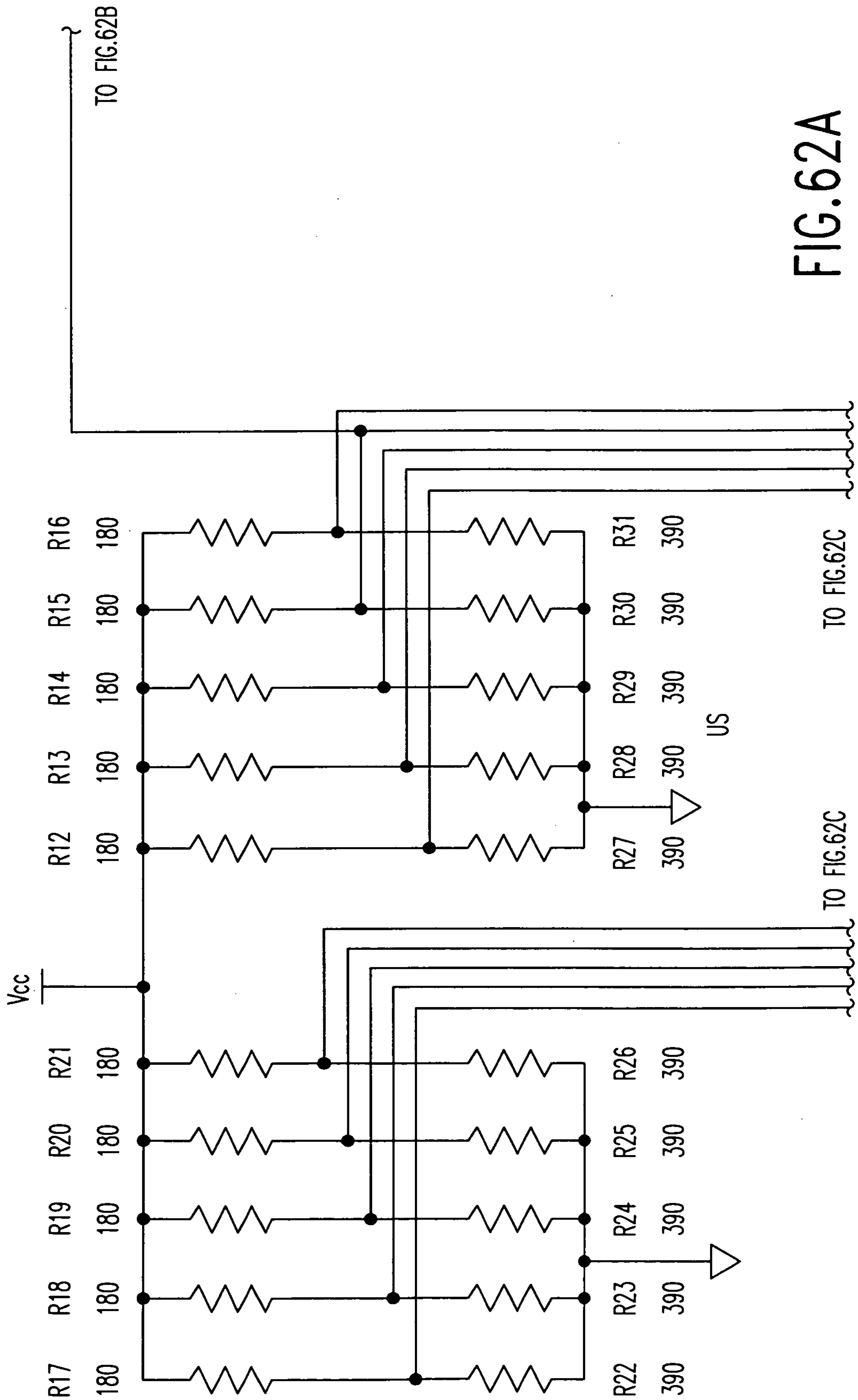
TO FIG.62B
R16 180
R15 180
R14 180
R13 180
R12 180
R31 390
R30 390
R29 390
R28 390
R27 390
US
TO FIG.62C
TO FIG.62C
Vcc
R21 180
R20 180
R19 180
R18 180
R17 180
R26 390
R25 390
R24 390
R23 390
R22 390

FIG.62A

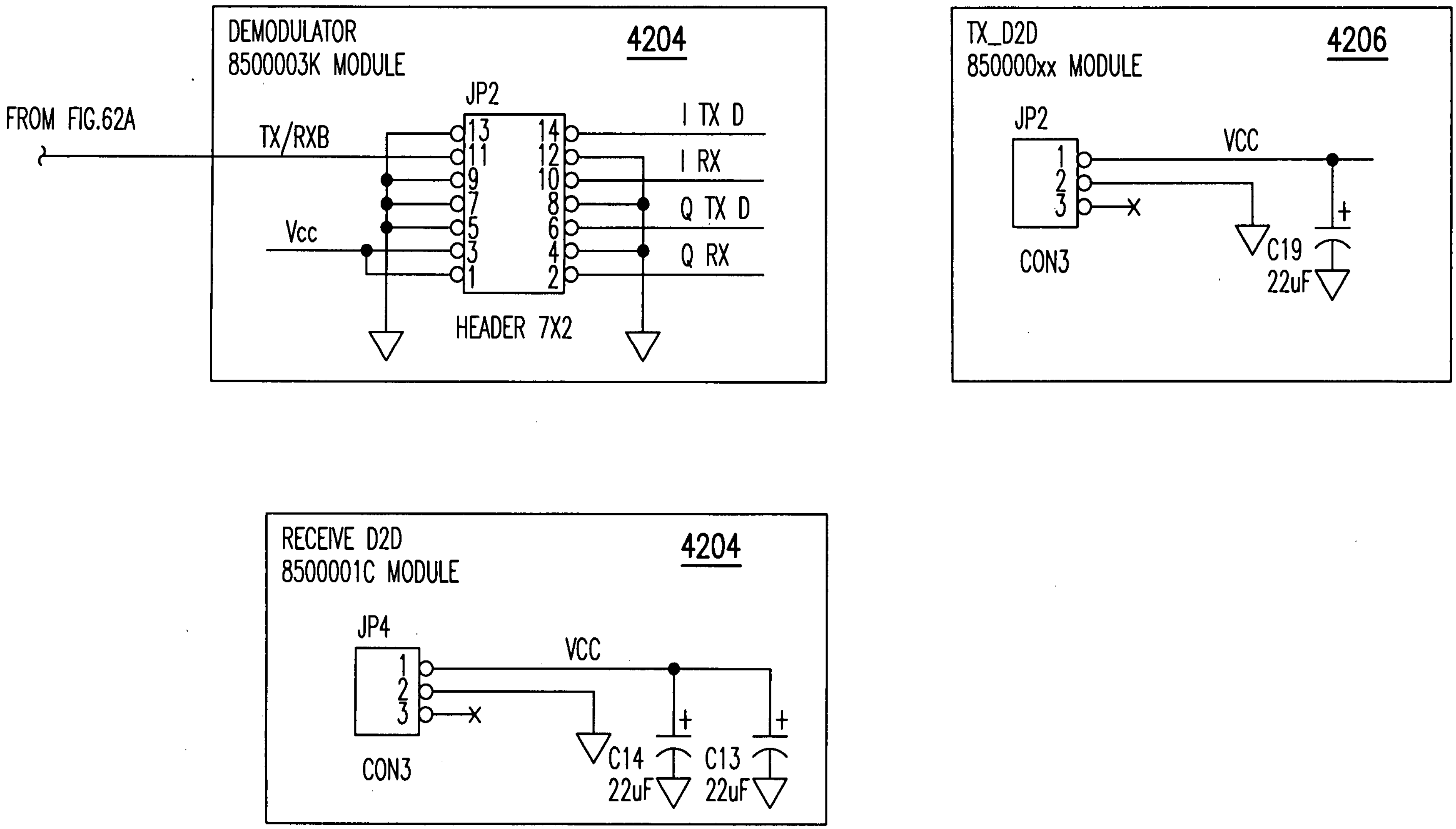

FIG.62B

New Sheet
Sheet 103 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

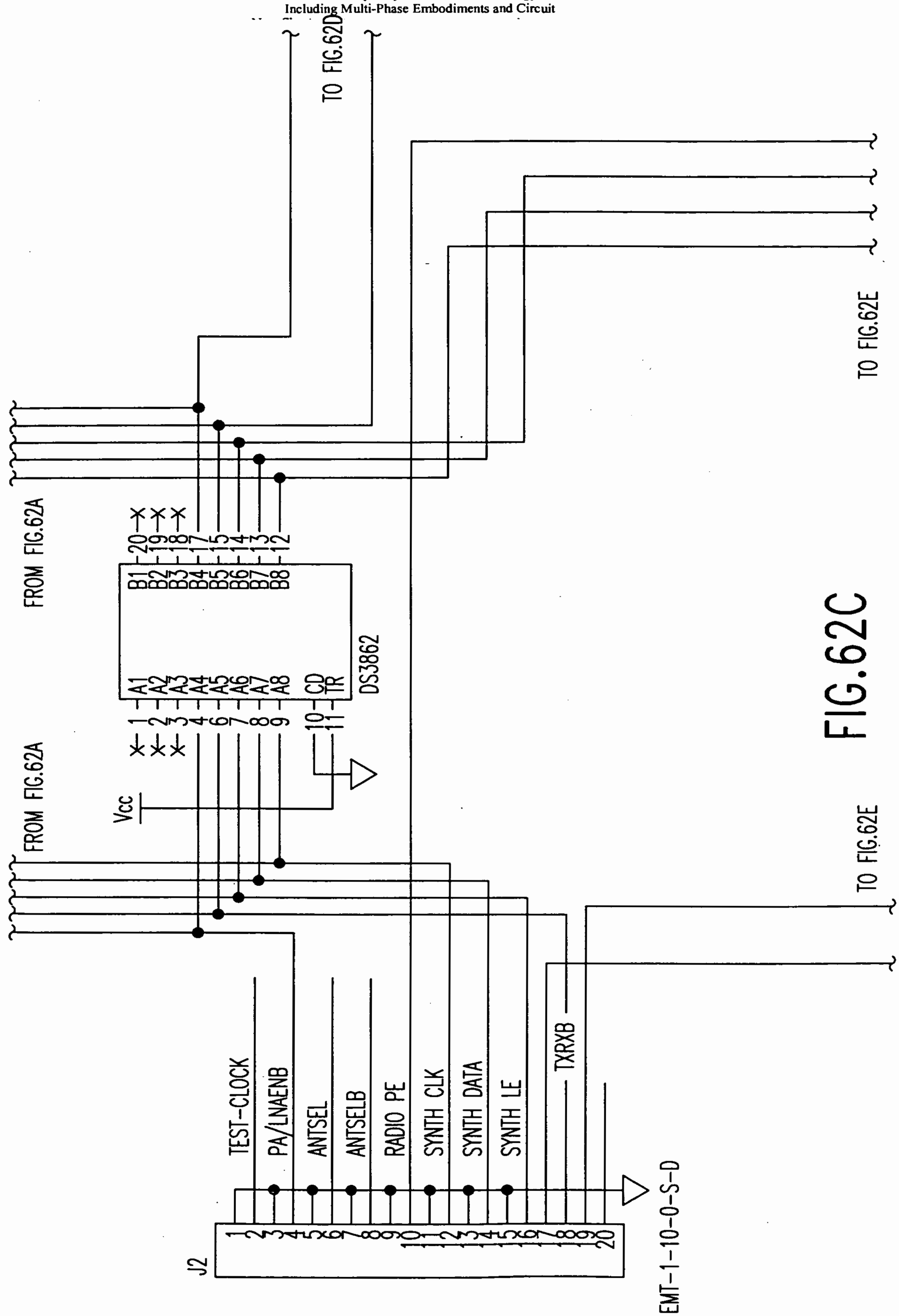

FIG.62C

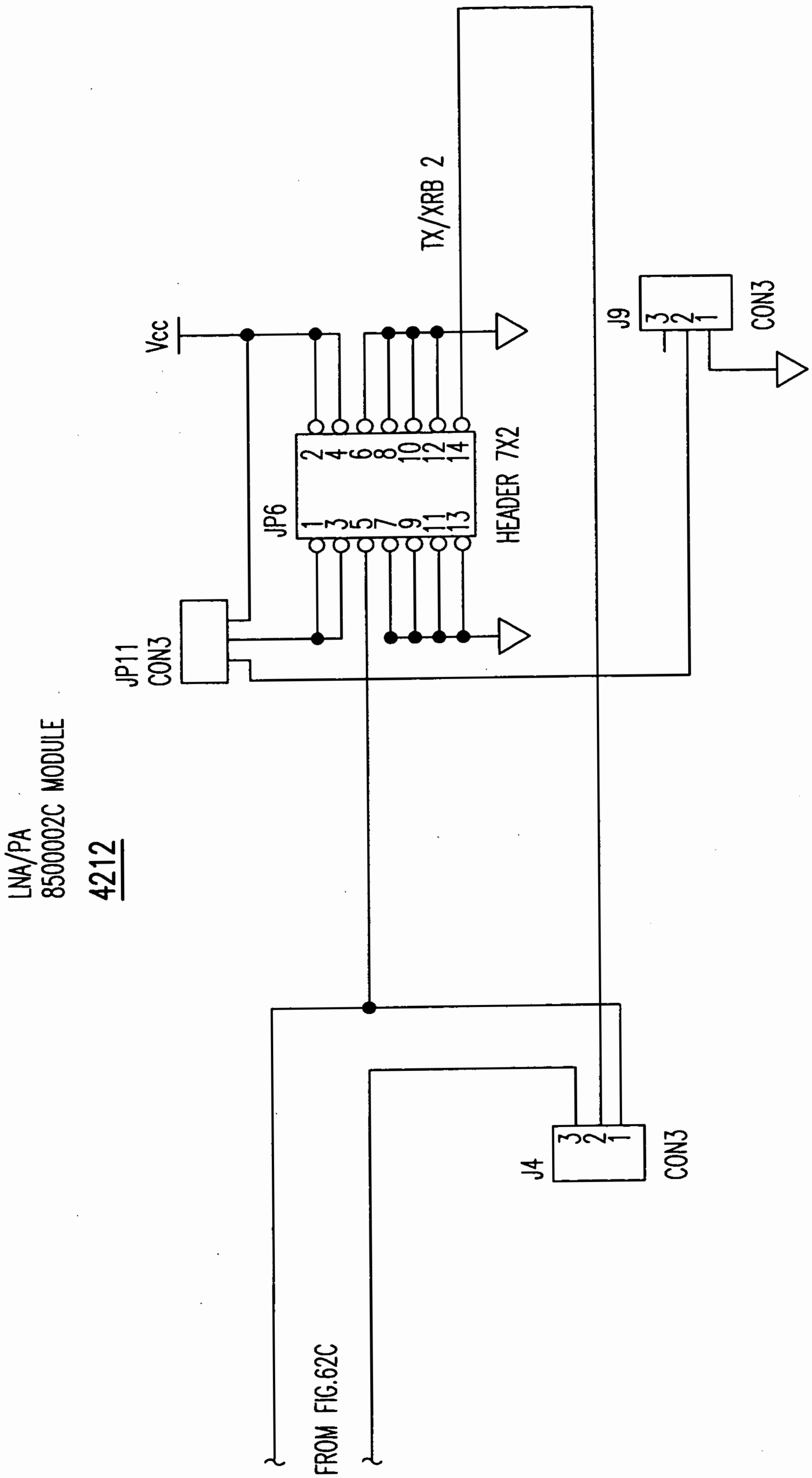
LNA/PA
8500002C MODULE
4212
Vcc
TX/XRB 2
JP6
HEADER 7X2
JP11
CON3
J9
CON3
J4
CON3
FROM FIG.62C

FIG.62D

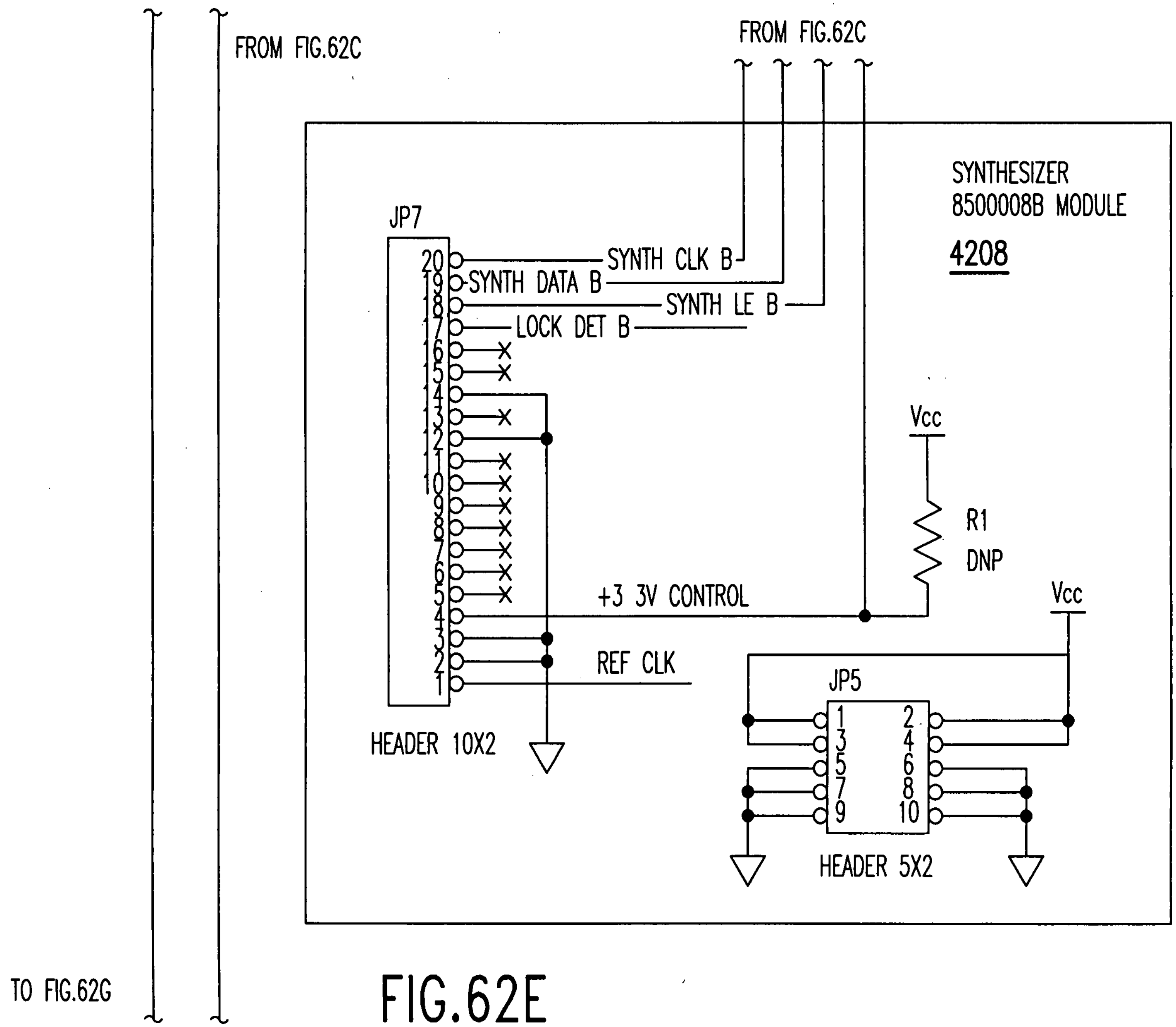

FIG.62E

New Sheet
Sheet 106 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

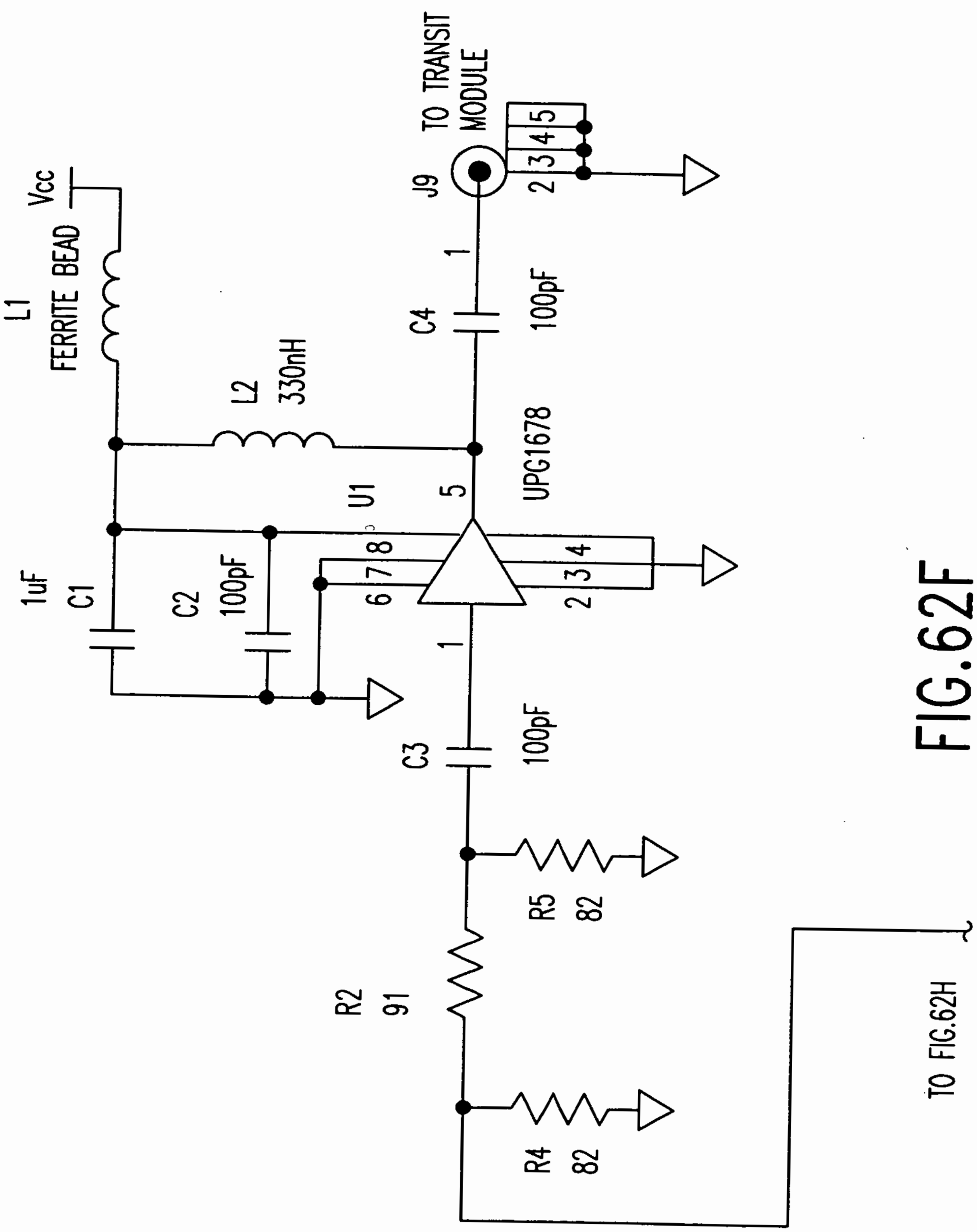

FIG.62F

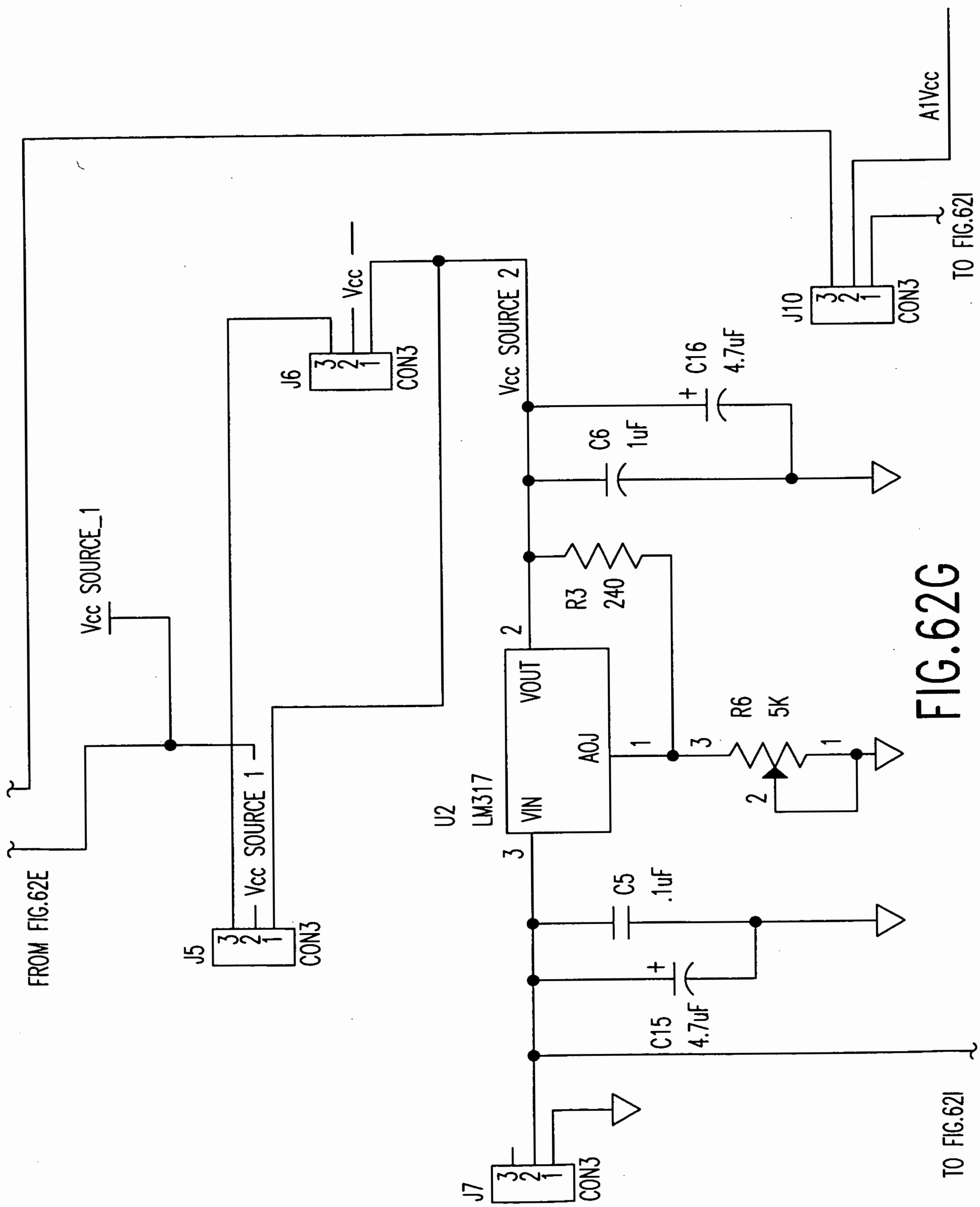
A1Vcc
TO FIG.62I
J10
CON3
Vcc
J6
CON3
Vcc SOURCE 2
C16
4.7uF
C6
1uF
Vcc SOURCE_1
R3
240
VOUT
AOJ
VIN
U2
LM317
R6
5K
Vcc SOURCE 1
FROM FIG.62E
J5
CON3
C5
.1uF
C15
4.7uF
J7
CON3
TO FIG.62I

FIG.62G

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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

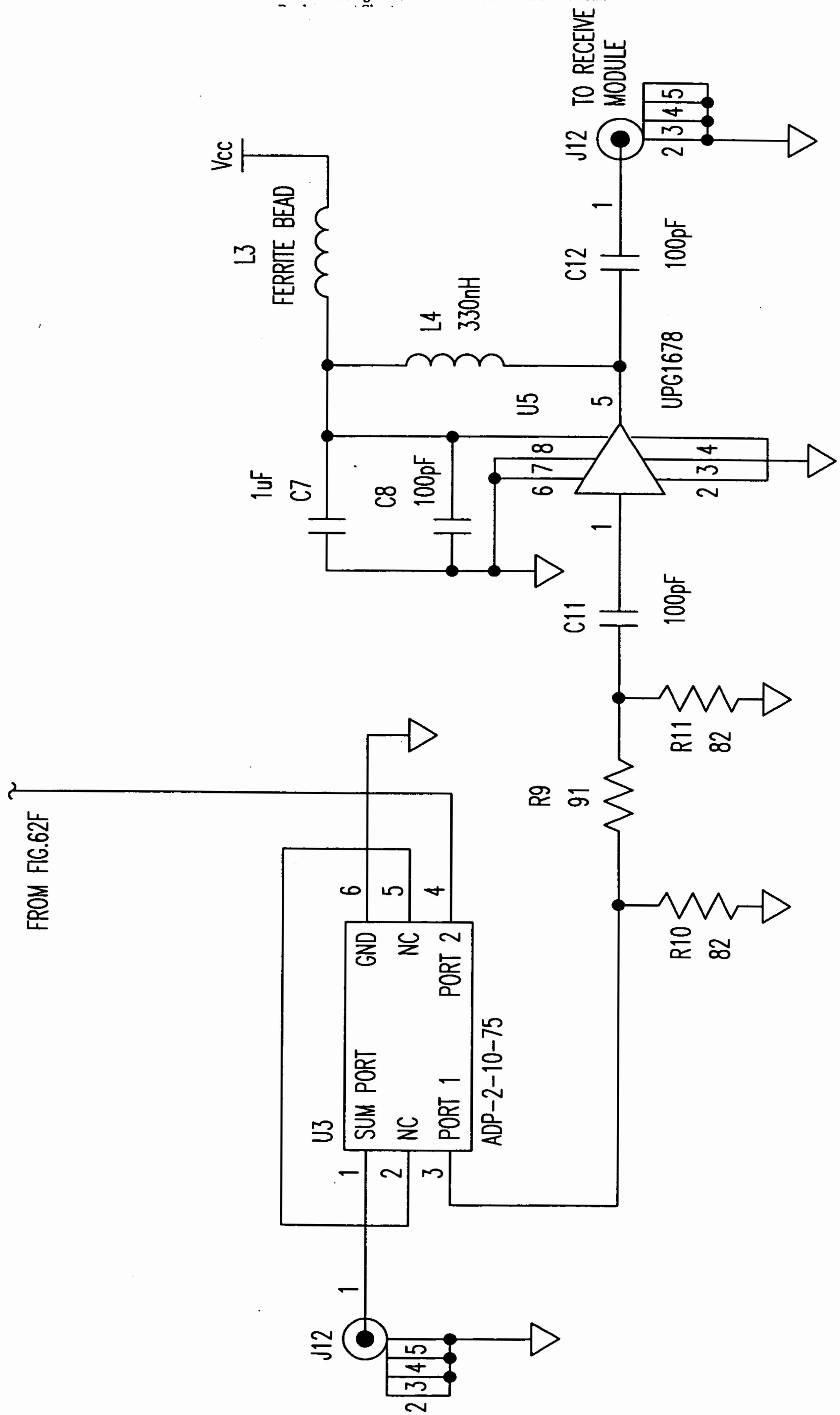

FIG.62H

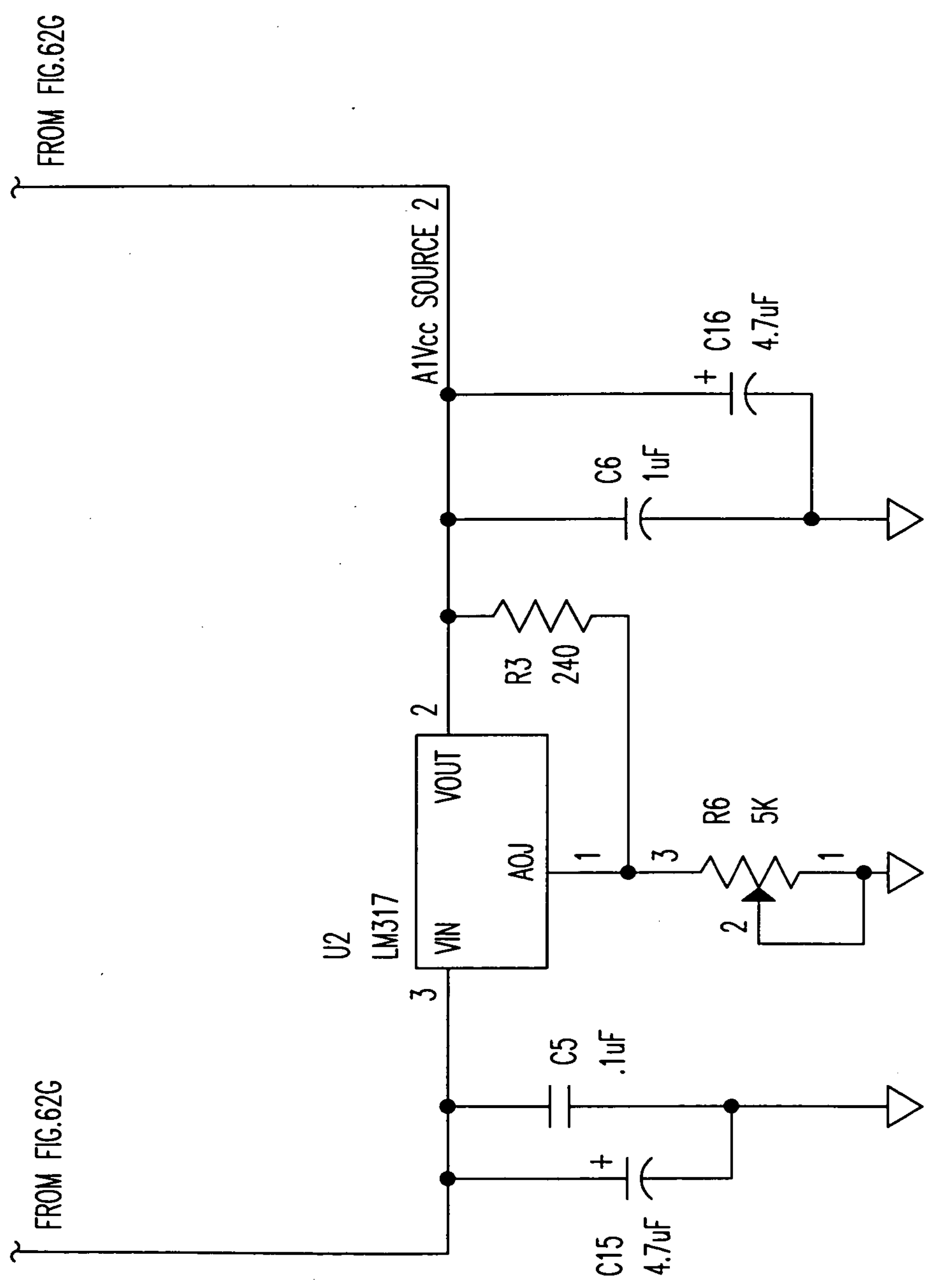
FROM FIG.62G
A1Vcc SOURCE 2
C16
4.7uF
C6
1uF
R3
240
U2
LM317
VOUT
VIN
AOJ
R6
5K
C5
.1uF
C15
4.7uF
FROM FIG.62G

FIG.62I

ITEM	QTY	REFERENCE	PART	DESCRIPTION	PART NUMBER	VENDOR
1	4	C1,C6,C7,C10	1uF	Cap, 1uF, +80-20%,0805	GRM40Y5V105Z016AD	MURATA
2	6	C2,C3,C4,C8,C11,C12	100pF	Cap, 100pF, 5%, COG, 0603	ECU-V1H101JCV	PANASONIC
3	2	C5,C9	.1uF	Cap, .1uF, +80-20%, Y5V, 0603		MURATA
4	3	C13,C14,C19	22uF	Cap, Tant, 22uF, 20%, 20V	T491D226M020AS	KEMET
5	4	C15,C16,C17,C18	4.7uF	Cap, Tant, 4.7uF, 20%, 20V	T491C475M020AS	KEMET
6	2	JP2,JP6	HEADER 7X2	Receptacle, 7x2pin, .050	SFMC-107-L1-S-D	SAMTEK
7	9	JP4, J4, J5, J6, J7, JP9, J9,	CON3	Header, 3pin, .100''	69190-403	BERG
		J10, JP11				
8	1	JP7	HEADER 10X2	Receptacle, 10X2pin, .050	SFMC-110-L1-S-D	SAMTEK
9	1	JP8	HEADER 5X2	Receptacle, 5X2pin, .050	SFMC-105-L1-S-D	SAMTEK
10	1	J2	EHT-1-10-01-S-D	Header, ribbon, 10X2pin, 2mm	EHT-1-10-01-S-D	SAMTEK
11	3	J8,J11,J12	82MMCX-50-0-1	Connector,RF	82MMCX-50-0-1	SUHNER
12	2	L3,L1	Ferrite Bead	Ferrite Bead, 0805	BLM21A121S	MURATA
13	2	L4,L2	330nH	Ind, 330nH, 10%, 0805	LL2012-FR33K	TOKO
14	1	R1	DNP	Res, 0603		PANASONIC
15	2	R9,R2	91	Res, 91 Ohn, 5%, 0603	ERJ-3GSYJ910	PANASONIC
16	2	R7,R3	240	Res, 240 Ohm, 5%, 0603	ERJ-3GSYJ241	PANASONIC
17	4	R4,R5,R10,R11	82	Res, 82 Ohm, 5%, 0603	ERJ-3GSYJ820	PANASONIC
18	2	R8,R6	5K	Var Res, 5K, 10%	3296W001502	BOUMS
19	10	R12, R13, R14, R15, R16,	180	Res, 180 Ohm, 5%, 0603	ERJ-3GSYJ181	PANASONIC
		R17, R18, R19, R20, R21				
20	10	R22, R23, R24, R25, R26,	390	Res, 390 Ohm, 5%, 0603	ERJ-3GSYJ391	PANASONIC
		R27, R28, R29, R30, R31				
21	2	U5,U1	UPG1678	IC, RF Buffer	UPG1678GV	NEC
22	2	U4,U2	LM317	IC, Voltage Regulator	LM317T	NATIONAL
23	1	U3	ADP-2-10-75	RF Splitter	ADP-2-10-75	MINICIRCUITS
24	1	U6	DS3862	IC, Buffer	DS3862WM	NATIONAL
25	1			BOARD	ST8500.641.023V0L01	

FIG.63

Replacement Sheet
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Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

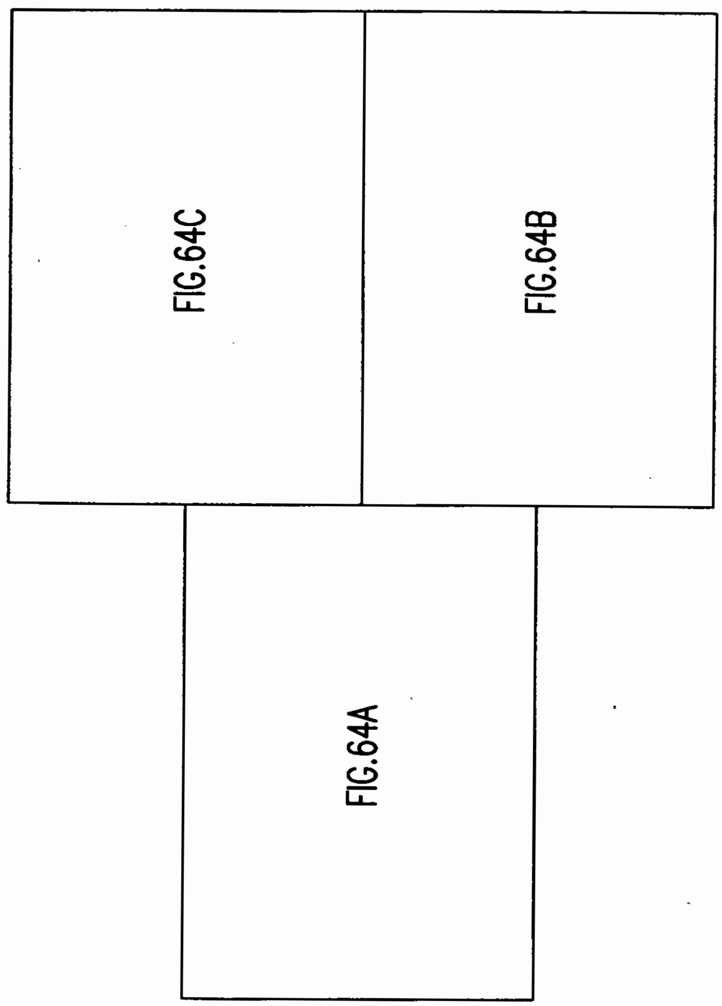
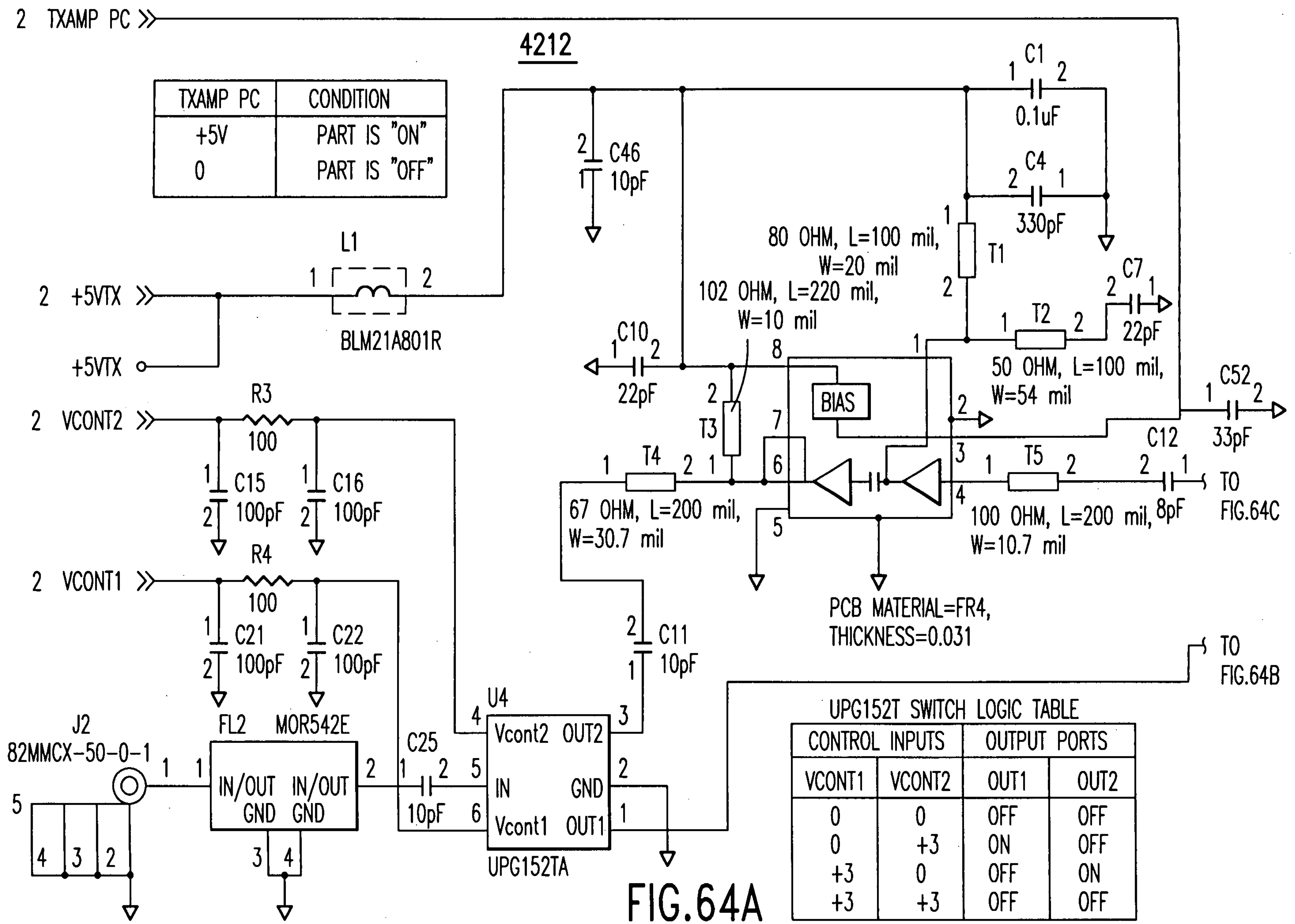


FIG.64



TXAMP PC	CONDITION
+5V	PART IS "ON"
0	PART IS "OFF"

UPG152T SWITCH LOGIC TABLE

CONTROL INPUTS		OUTPUT PORTS	
VCONT1	VCONT2	OUT1	OUT2
0	0	OFF	OFF
0	+3	ON	OFF
+3	0	OFF	ON
+3	+3	OFF	OFF

FIG.64A

New Sheet
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New Sheet
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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

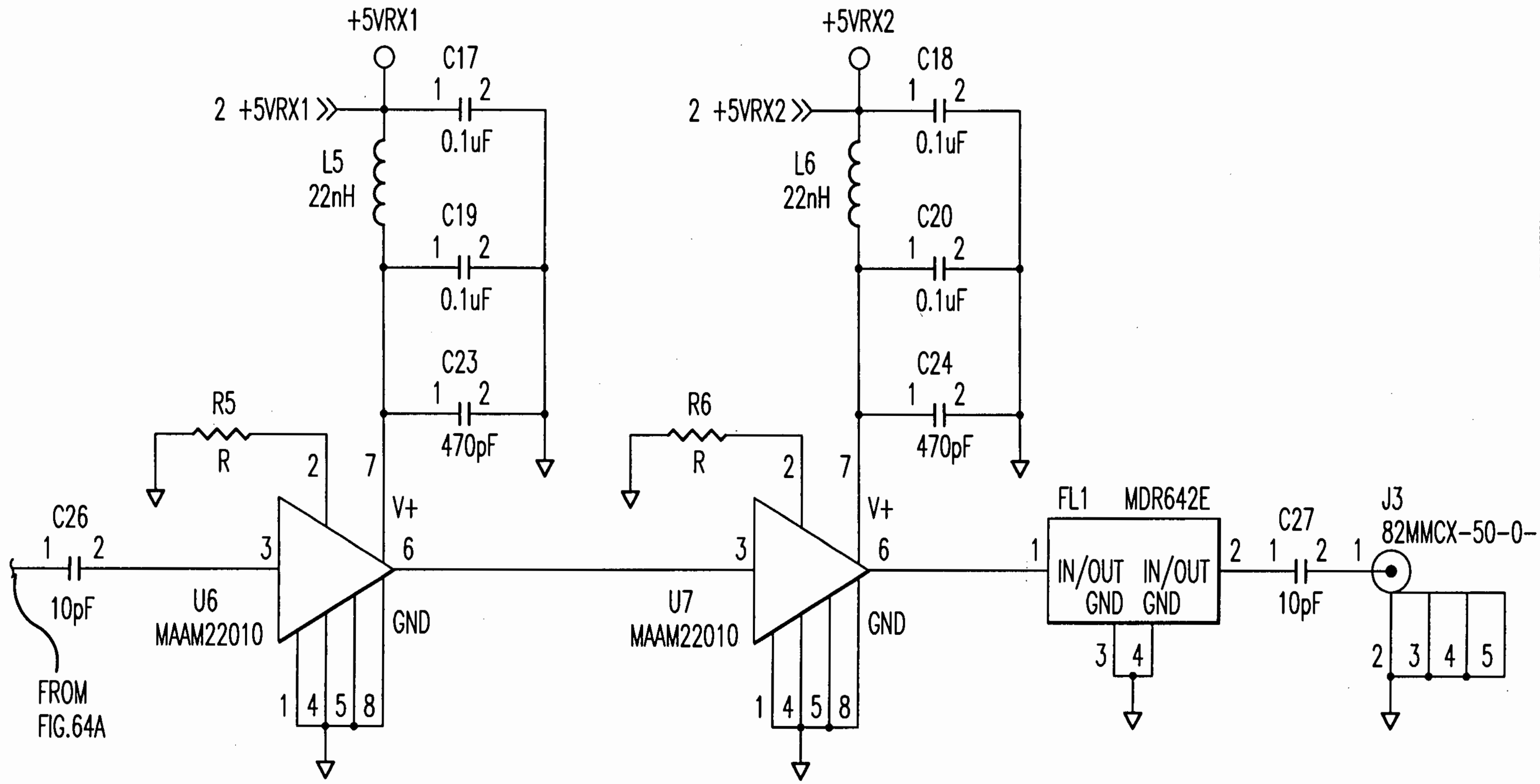

FIG.64B

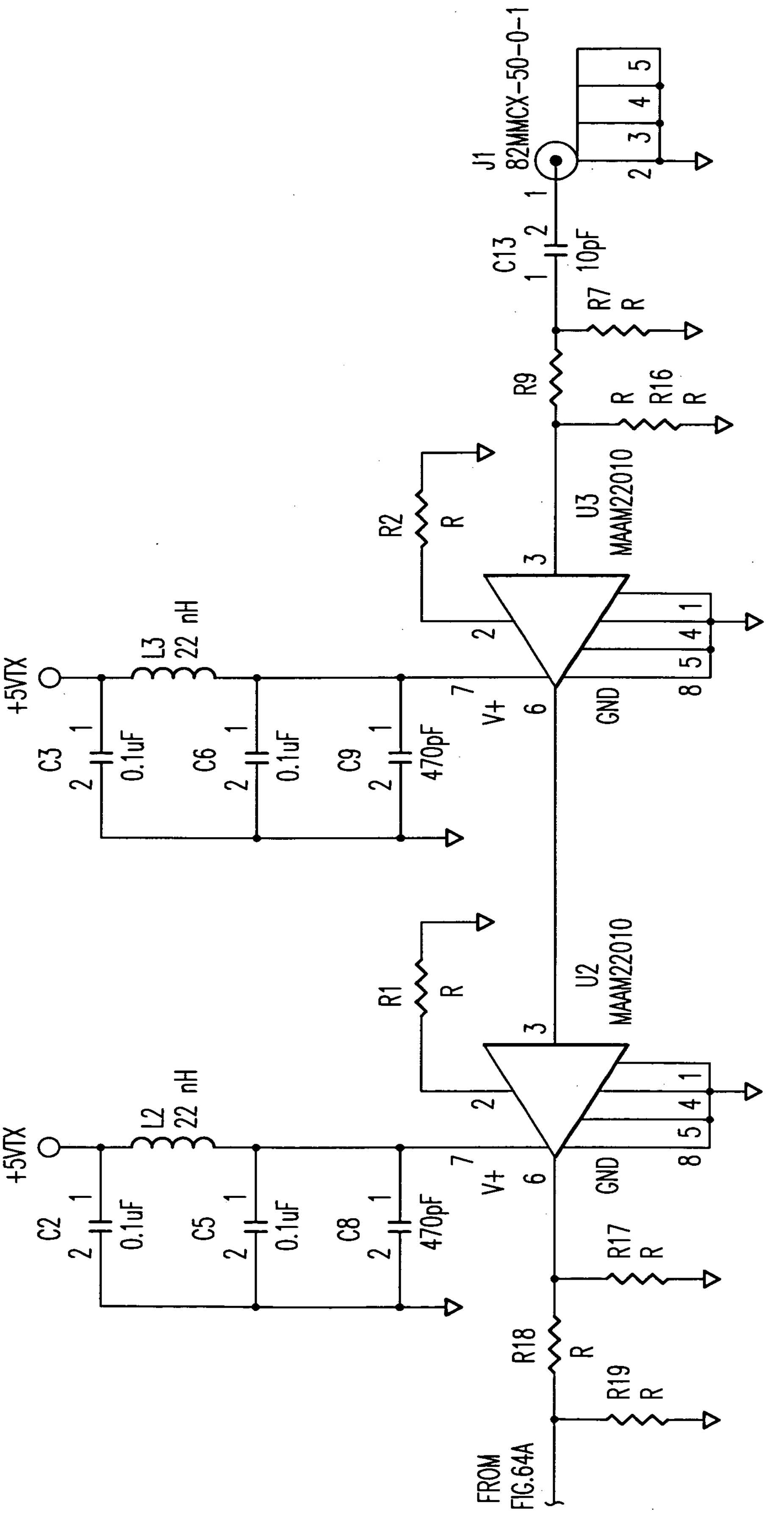
J1
82MMCX-50-0-1
C13
10pF
R7
R
R9
R16
R
R2
U3
MAAM22010
+5VTX
L3
22 nH
C3
0.1uF
C6
0.1uF
C9
470pF
V+
GND
R1
U2
MAAM22010
+5VTX
L2
22 nH
C2
0.1uF
C5
0.1uF
C8
470pF
R17
R18
R19
FROM
FIG.64A

FIG.64C

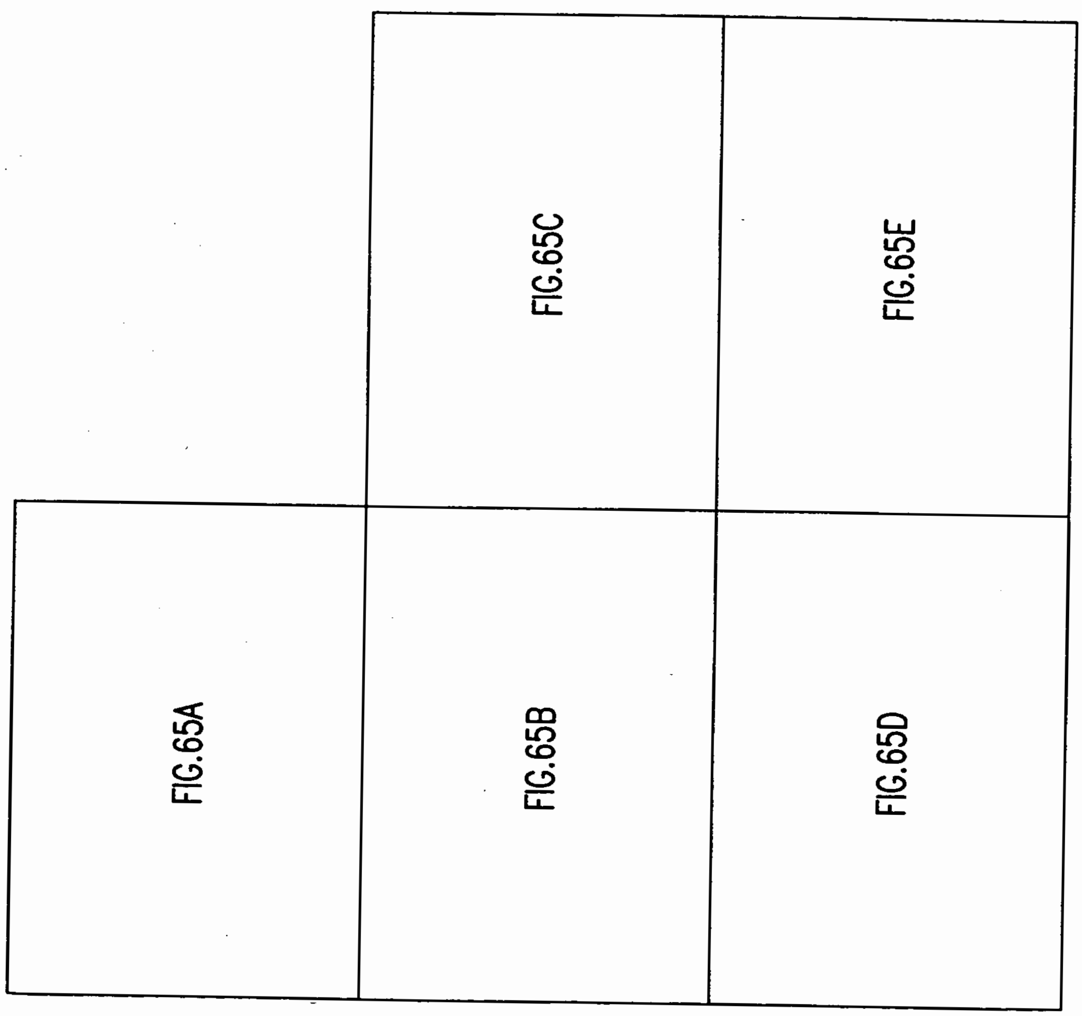

FIG.65

4212

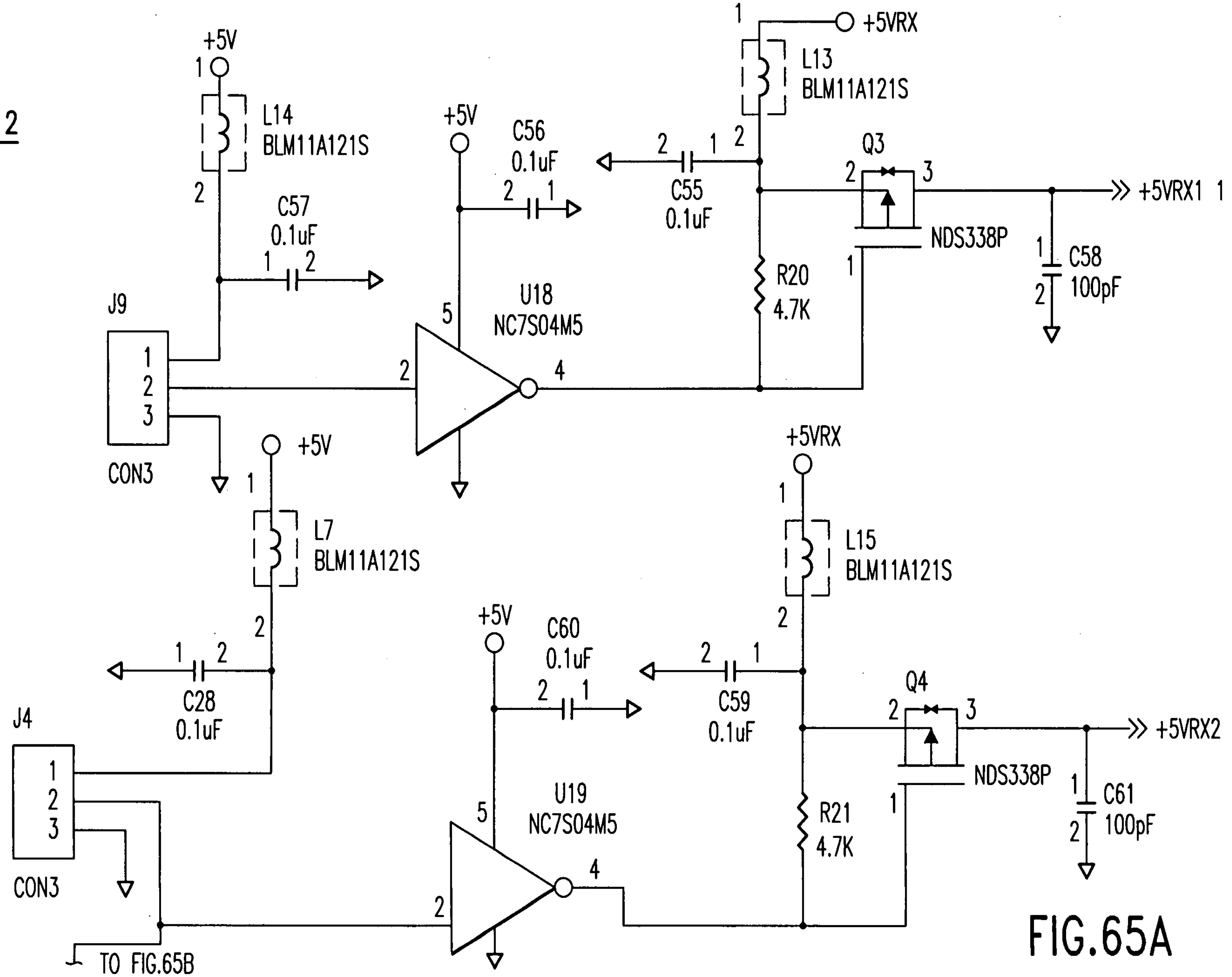

FIG.65A

New Sheet
Sheet 117 of 349
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Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

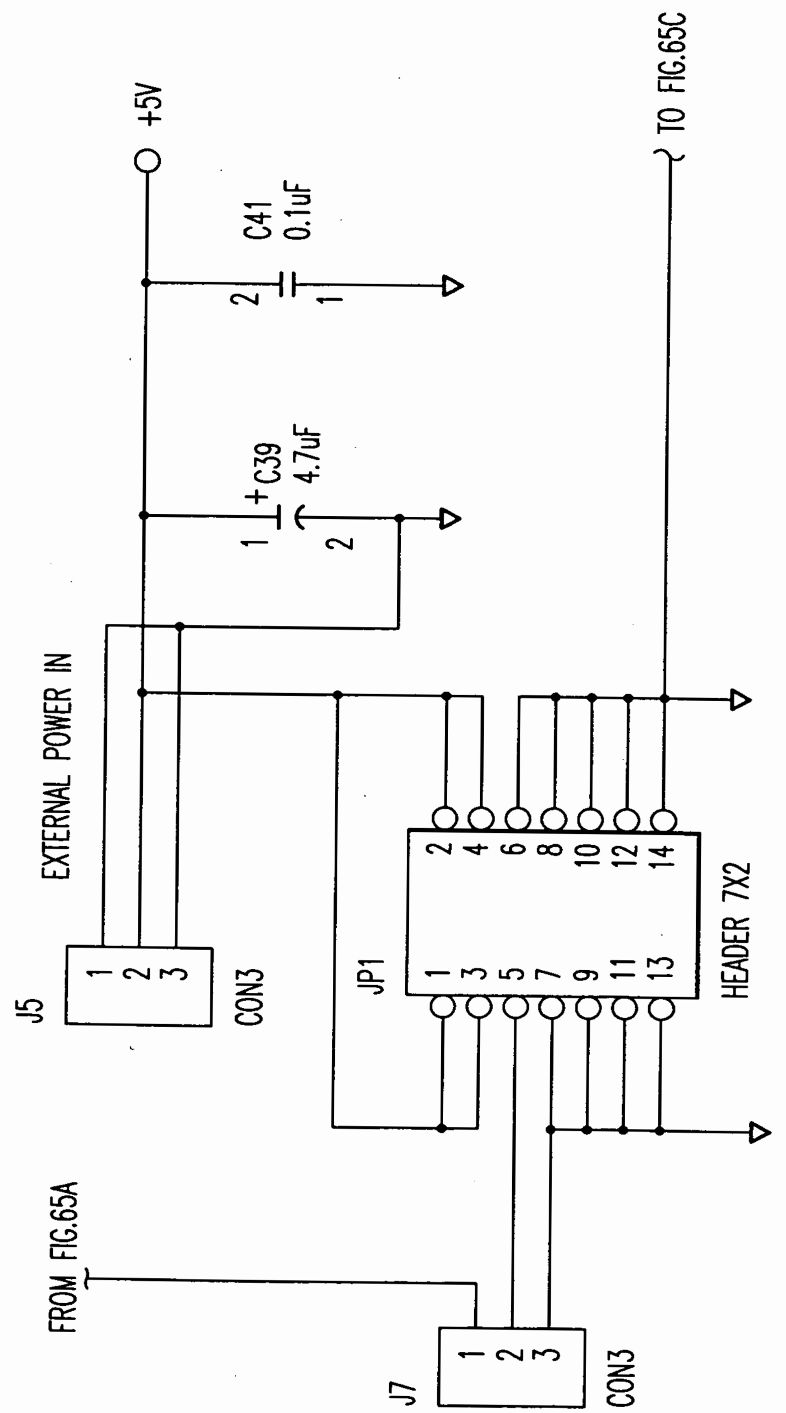
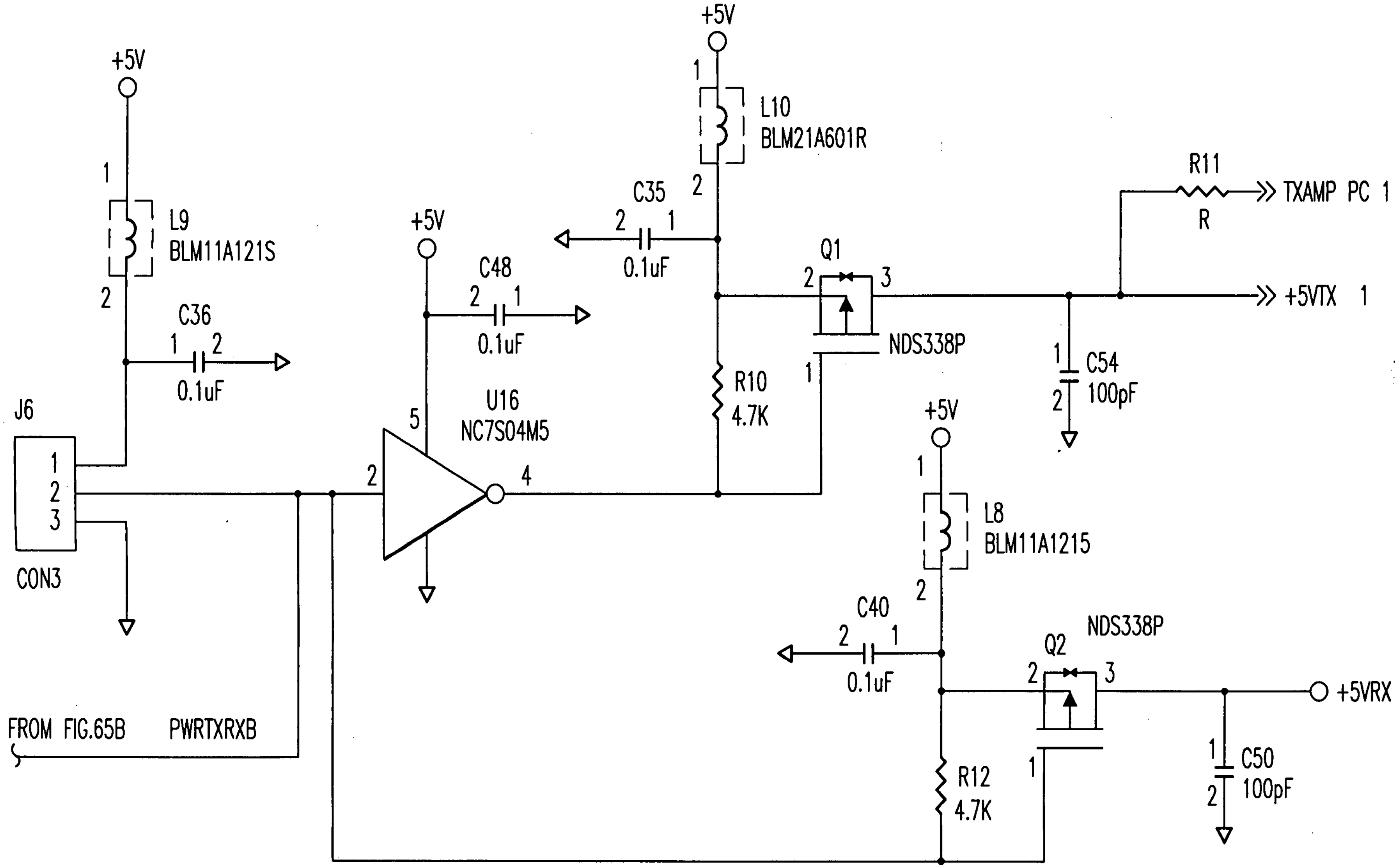

+5V
TO FIG.65C
C41
0.1uF
C39
4.7uF
EXTERNAL POWER IN
J5
CON3
JP1
HEADER 7X2
FROM FIG.65A
J7
CON3

FIG.65B



New Sheet
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FIG.65C

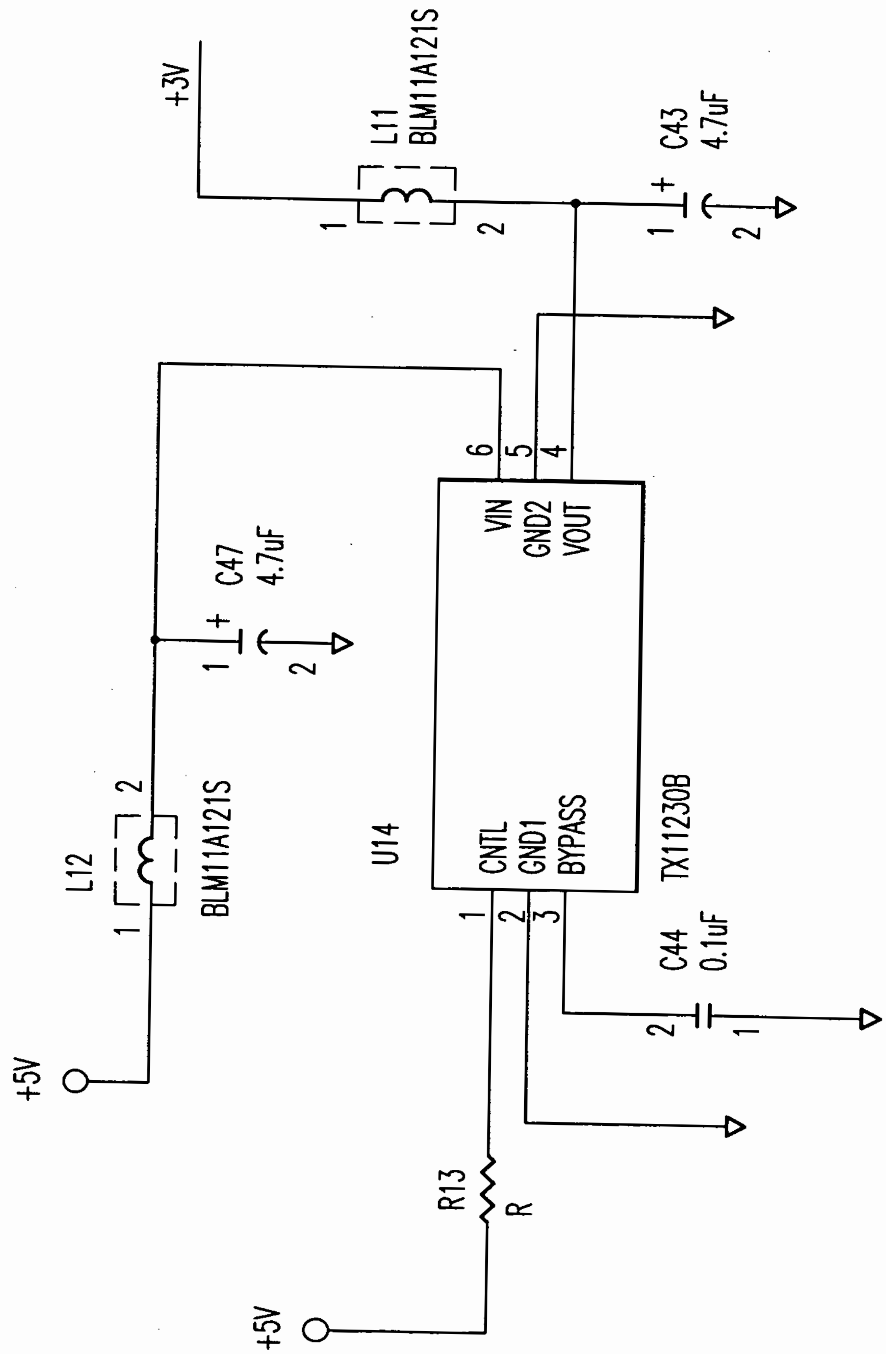
+3V
L11
BLM11A121S
C43
4.7uF
C47
4.7uF
L12
BLM11A121S
U14
VIN
GND2
VOUT
CNTL
GND1
BYPASS
TX11230B
C44
0.1uF
R13
R
+5V
+5V

FIG.65D

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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

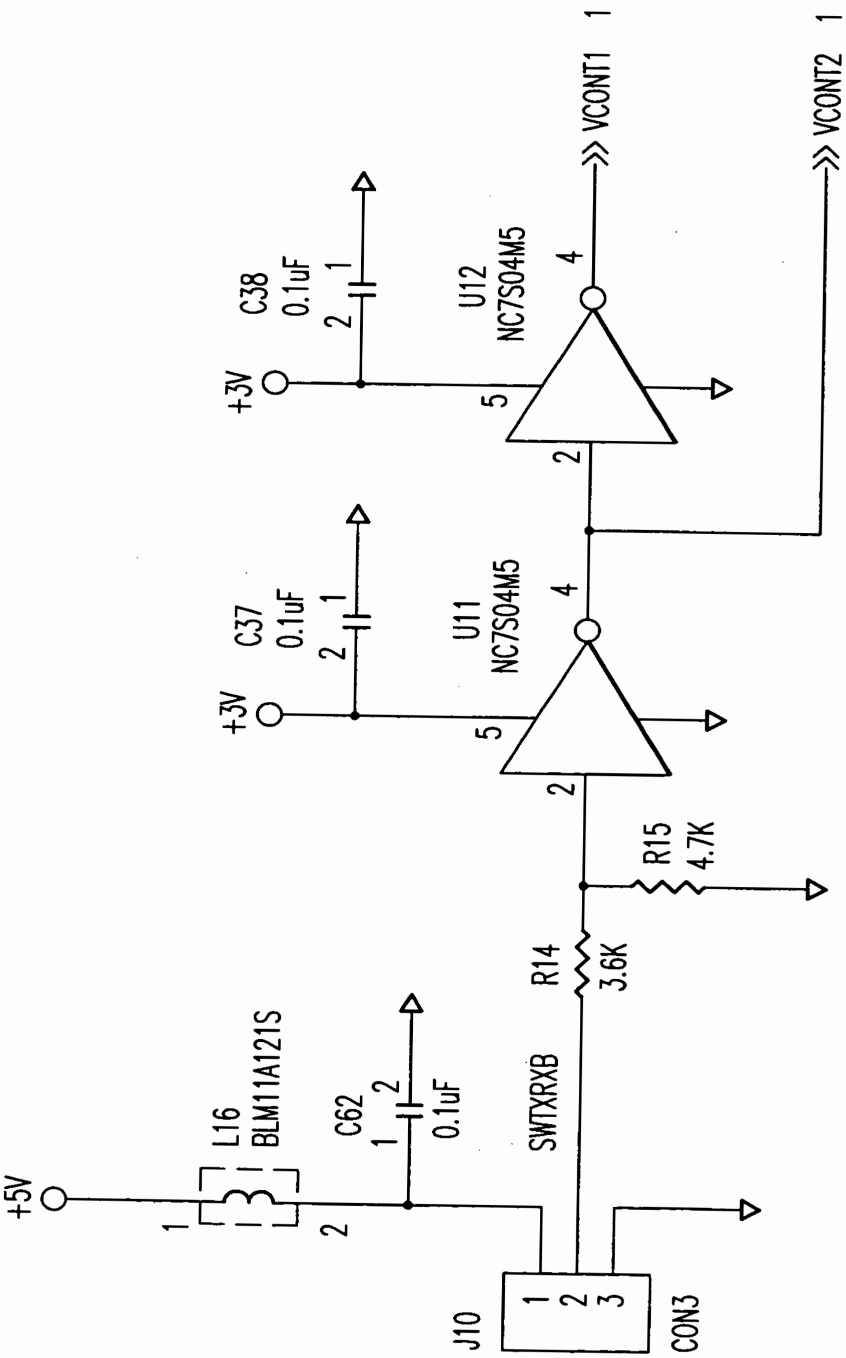

FIG.65E

ITEM	QTY	REFERENCE	PART	MANUFACT.	PART DESCRIPTION	PART NUMBER
1	24	C1,C2,C3,C5,C6,C17,C18,	0.1uF	MURATA	.1uF,0603,X7R,20%,16V	GRM39X7R104M016
		C19,C20,C28,C35,C36,C37,				
		C38,C40,C41,C44,C48,C55,				
		C56,C57,C59,C60,C62				
2	1	C4	330pF	MURATA	330pF,0603,COG,10%,50	GRM39COG331K050
3	2	C10,C7	22pF	MURATA	22pF,0603,COG,10%,50	GRM30COG220K050
4	4	C8,C9,C23,C24	470pF	MURATA	470pF,0603,COG,10%,50	GRM39COG471K050
5	6	C11,C13,C25,C26,C27,C46	10pF	MURATA	10pF,0603,COG,10%,50	GRM39COG100K050
6	1	C12	8pF	MURATA	8pF,0603,COG,10%,50	GRM39COG080K050
7	8	C15,C16,C21,C22,C50,C54	100pF	MURATA	100pF,0603,COG,10%,50	GRM39COG101K050
		C58,C61				
8	3	C39,C43,C47	4.7uF	PANASONIC	4.7uF TANTALUM,16V	ECS-T1CY475R
9	1	C52	33pF	MURATA	330pF,0603,COG,10%,50	GRM3COG330K050
10	2	FL1,FL2	MDR642E	SOSHIN	2.4-2.5GHz BPF	MDR642E
11	1	JP1	HEADER 7X2	SAMTEC	DUAL ROW, 7 PINS PER ROW	FTSH-107-01-F-D
12	3	J1,J2,J3	82MMCX-50-0-1	SUHNER	RF CONNECTOR	82MMCX-50-0-1
13	6	J4,J5,J6,J7,J9,J10	CON3	BERG	3 PIN HEADER W RETENTIVE LEG	69190-403H
14	2	L10,L1	BLM21A601R	MURATA	600 OHMS@100MHz,500mA FERRITE BEAD	BLM21A601R
15	4	L2,L3,L5,L6	22nH	COILCRAFT	22nH,0805CS (2012),5%	0805CS-220X-BC
16	9	L7,L8,L9,L11,L12,L13,L14,	BLM11A121S	MURATA	RF BEAD	BLM11A121S
		L15,L16				
17	4	Q1,Q2,Q3,Q4	NDS336P	NATIONAL	P-CHANNEL FET	NDS336P
18	12	R1,R2,R5,R6,R7,R9,R11,	R	PANASONIC		
		R13,R16,R17,R18,R19				
19	2	R3,R4	100	PANASONIC	0603,100,5%,1/16W	ERJ-3GSY-J-101
20	5	R10,R12,R15,R20,R21	4.7K	PANASONIC	0603,4.7K,5%,1/16W	ERJ-3GSY-J-472

FIG.66A

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21	1	R14	3.6K	PANASONIC	0603,3.6K,5%,1/16W	ERJ-3GSY-J-362
22	1	T1	80 OHM,L=100 MIL,W=20 MIL		80 OHM,L=100 MIL,W=20 MIL	
23	1	T2	50 OHM,L=100 MIL,W=54 MIL		50 OHM,L=100 MIL,W=54 MIL	
24	1	T3	102 OHM,L=220 MIL,W=10 MIL		102 OHM,L=220 MIL,W=10 MIL	
25	1	T4	67 OHM,L=200 MIL,W=30.7 MIL		67 OHM,L=200 MIL,W=30.7 MIL	
26	1	T5	100 OHM,L=200 MIL,W=10.7MIL		100 OHM,L=200 MIL,W=10.7 MIL	
27	4	U2,U3,U6,U7	MAAM22010	MACOM	2.4-2.5 GHz LNA	MAAM22010
28	1	U4	UPG152TA	NEC	RF SWITCH	UPG152TA
29	5	U11,U12,U16,U18,U19	NC7S04M5	NATIONAL	INVERTER	NC7S04M5
30	1	U14	TKN11230B	TOKO	VOLTAGE REGULATOR	TK11230B
31	1	U17	RF2128P	RFMD	MEDIUM POWER LINEAR AMPLIFIER	RF2128P
32	1				BOARD	B500.641.024 VOL.

FIG.66B

New Sheet
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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

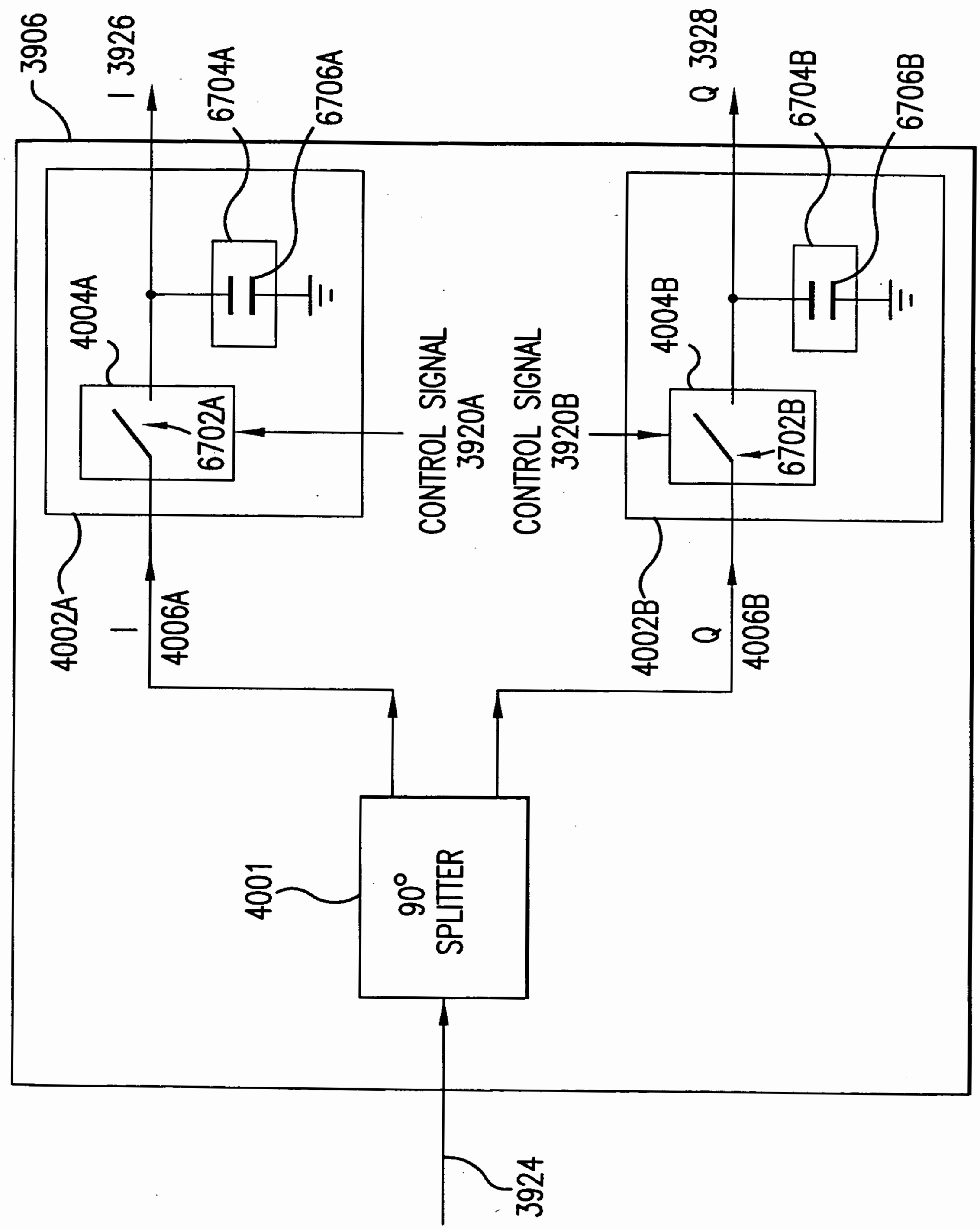

FIG.67A

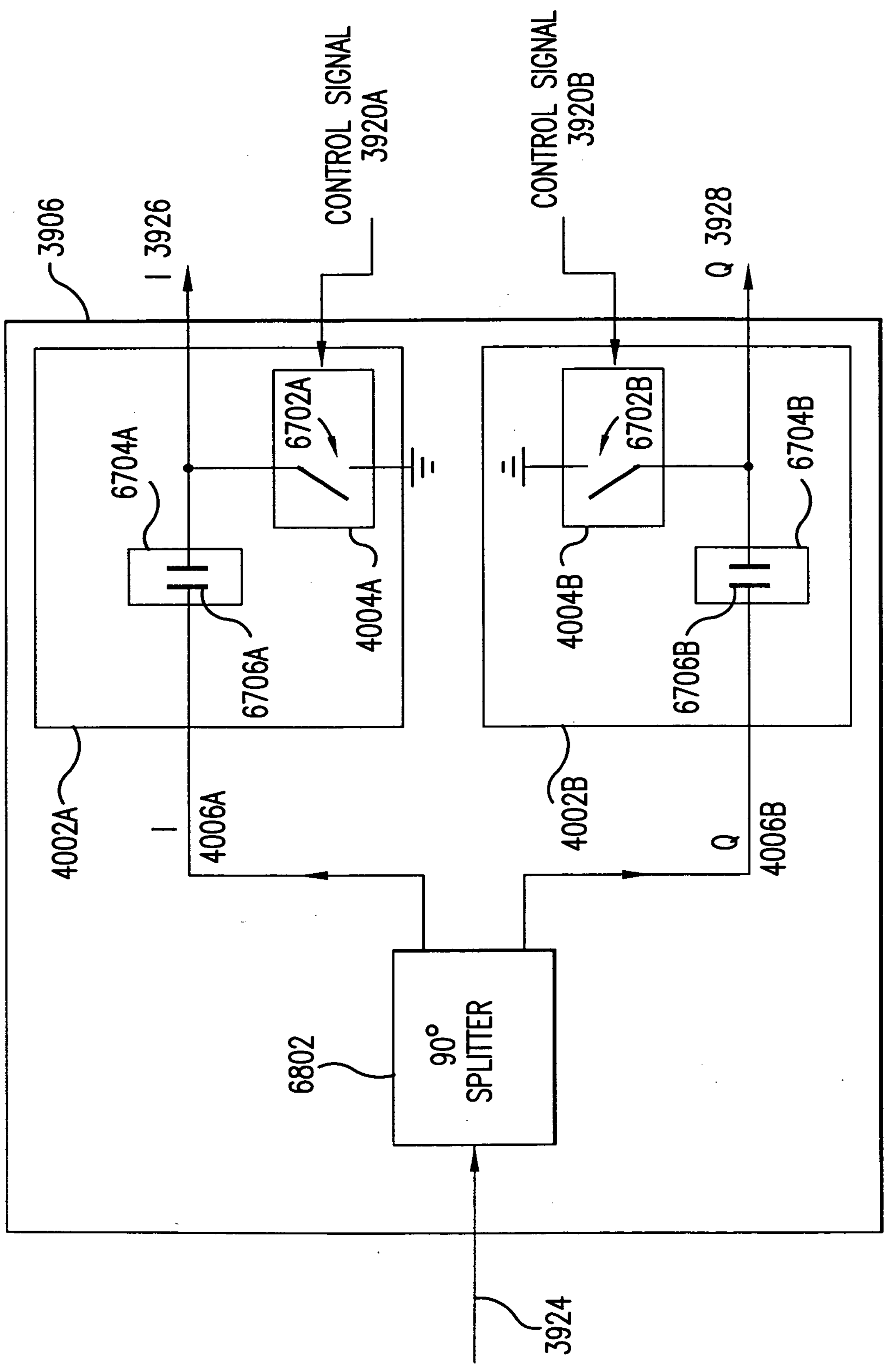
CONTROL SIGNAL 3920A
CONTROL SIGNAL 3920B
3906
I 3926
Q 3928
6702A
6702B
6704A
6704B
4004A
4004B
6706A
6706B
4002A
4002B
I
Q
4006A
4006B
90° SPLITTER
6802
3924

FIG.67B

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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
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Universal Frequency Translation Technology
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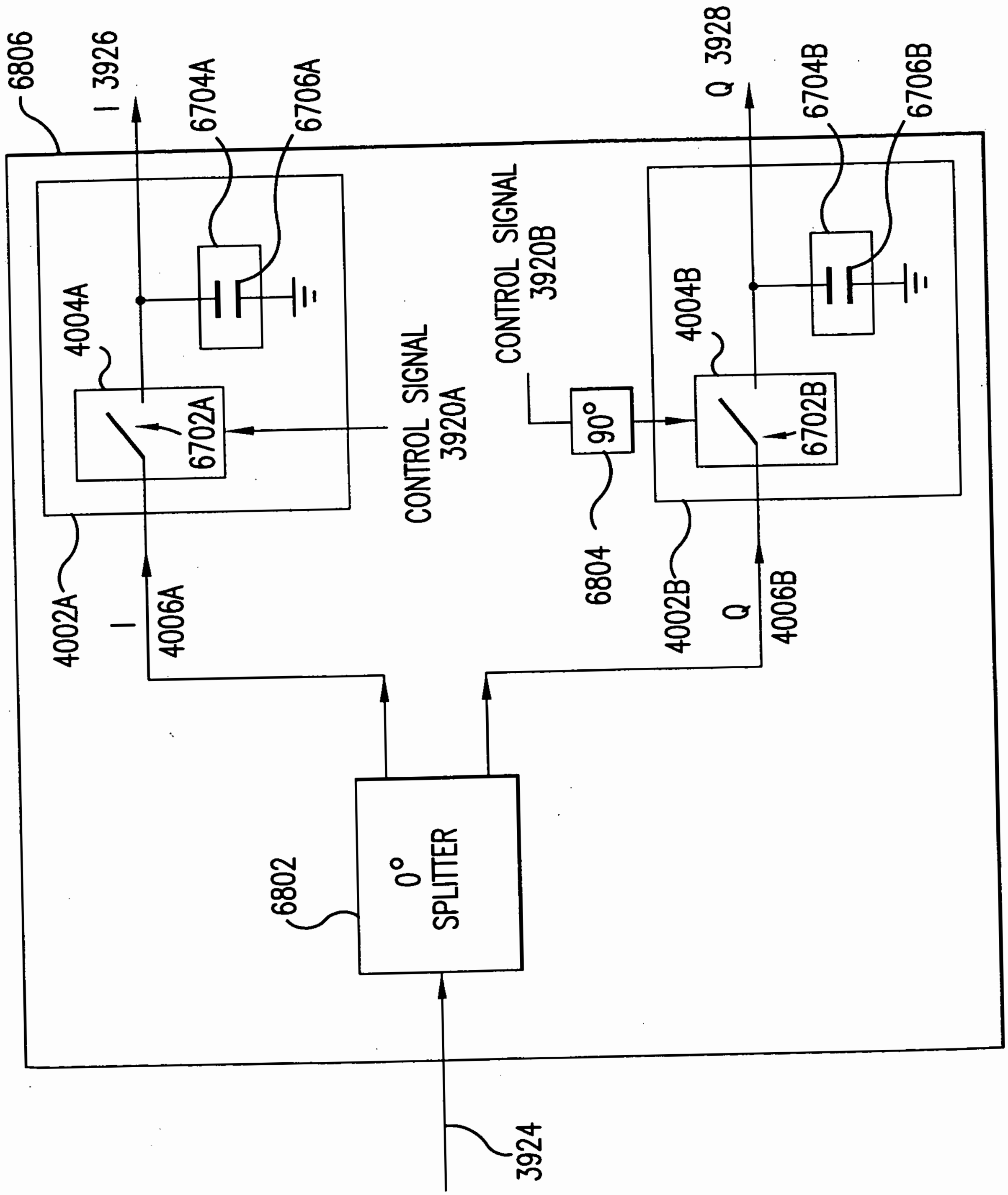
FIG.68A



Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

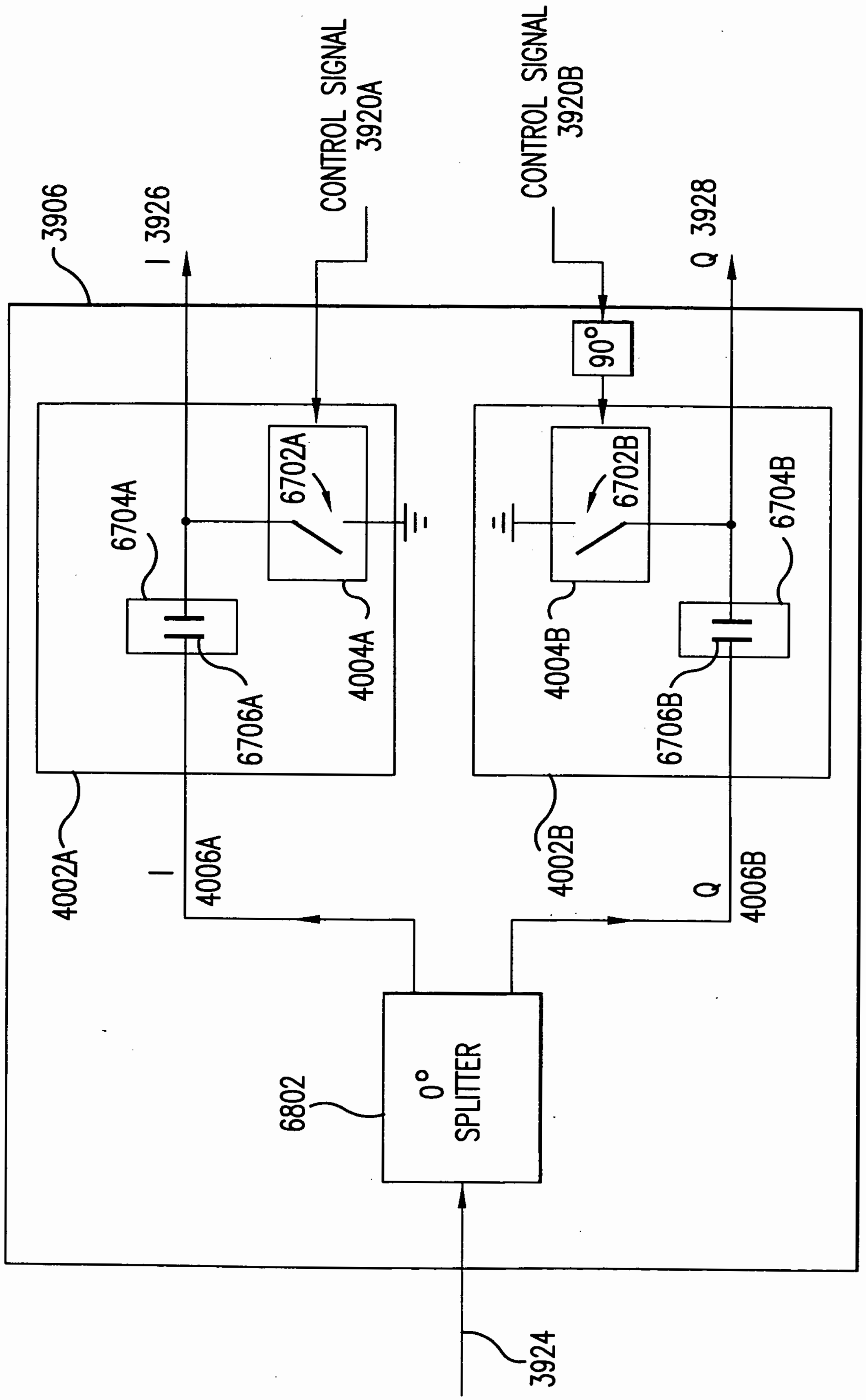


FIG.68B

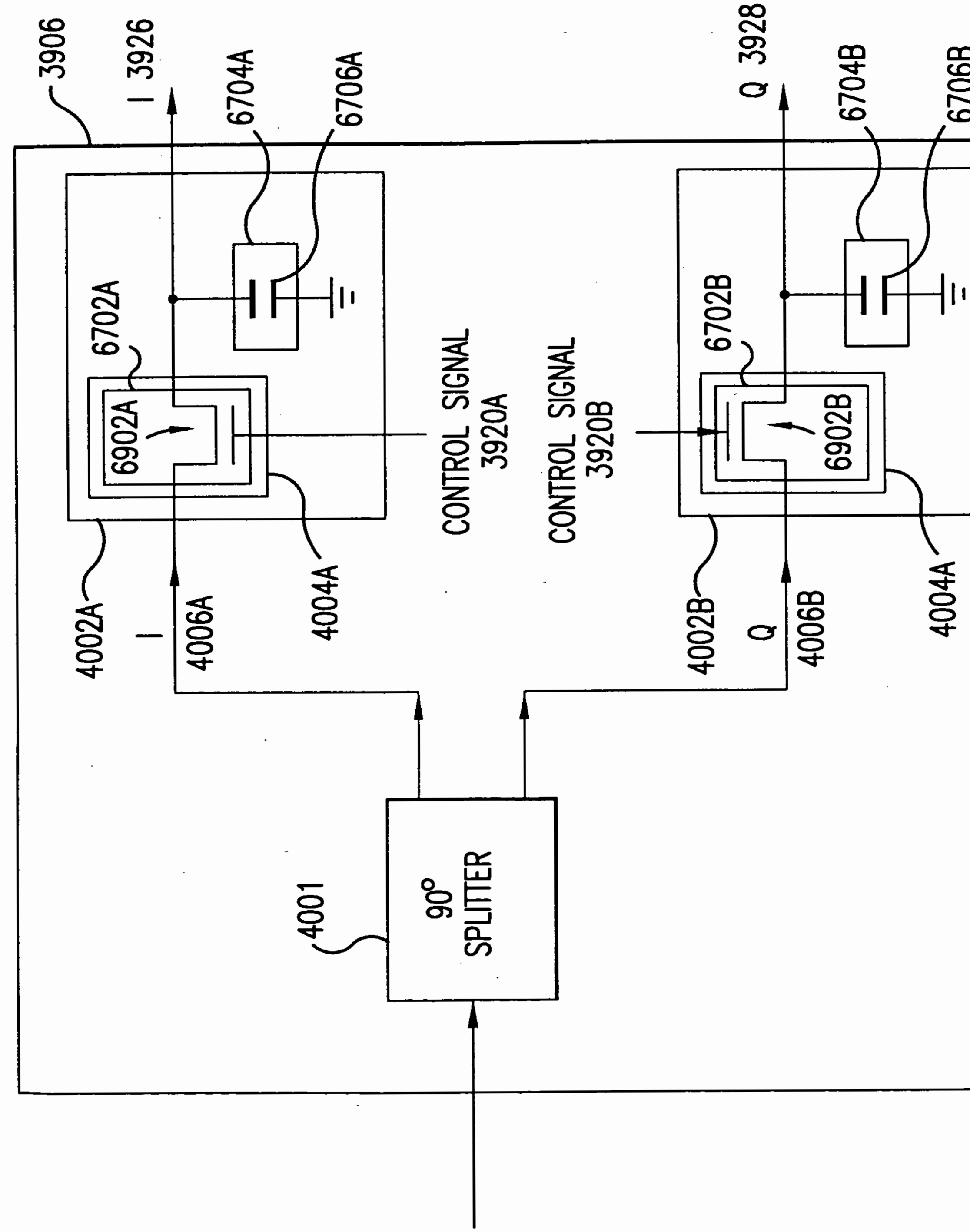

3906
I 3926
6704A
6706A
6702A
6902A
CONTROL SIGNAL
3920A
CONTROL SIGNAL
3920B
Q 3928
6704B
6706B
6702B
6902B
4002A
I
4006A
4004A
4002B
Q
4006B
4004A
4001
90°
SPLITTER

FIG.69A

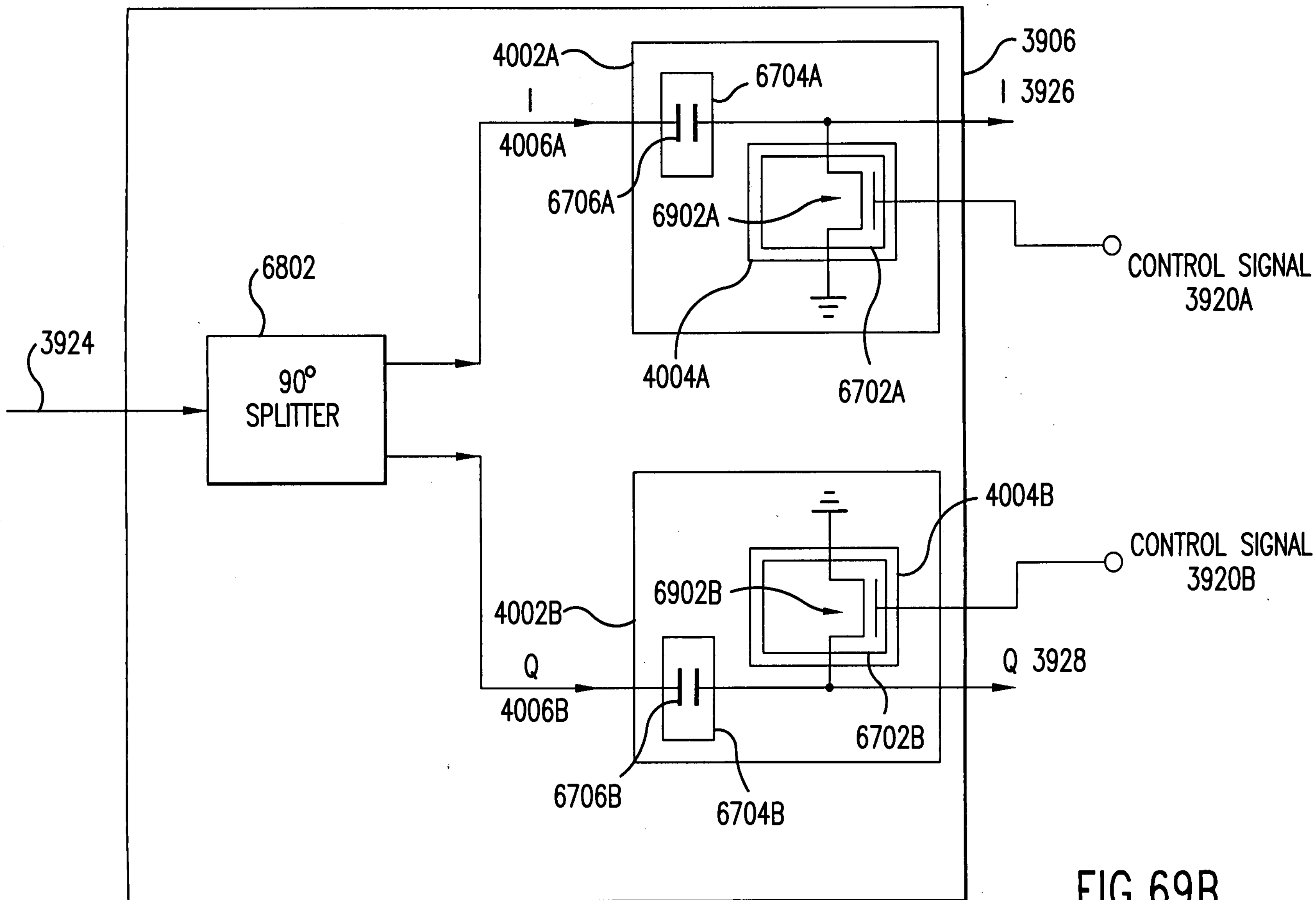


FIG.69B

Replacement Sheet
Sheet 129 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
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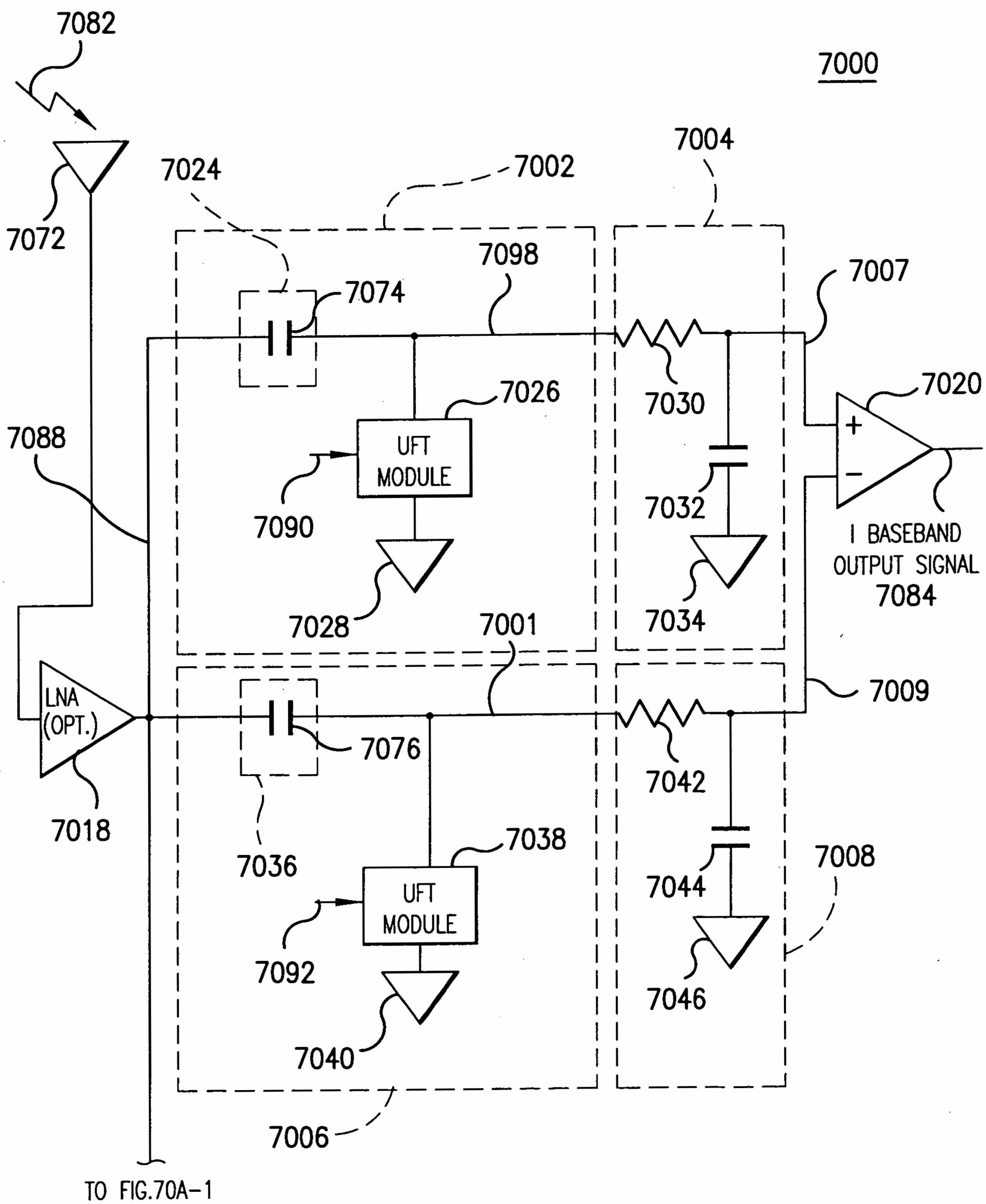
7000
7082
7072
7024
7002
7004
7098
7074
7007
7026
7030
7020
UFT MODULE
7088
7090
7032
7028
7034
I BASEBAND OUTPUT SIGNAL 7084
7001
7009
LNA (OPT.)
7076
7042
7018
7036
7038
7008
7044
UFT MODULE
7092
7046
7040
7006
TO FIG.70A-1

FIG.70A

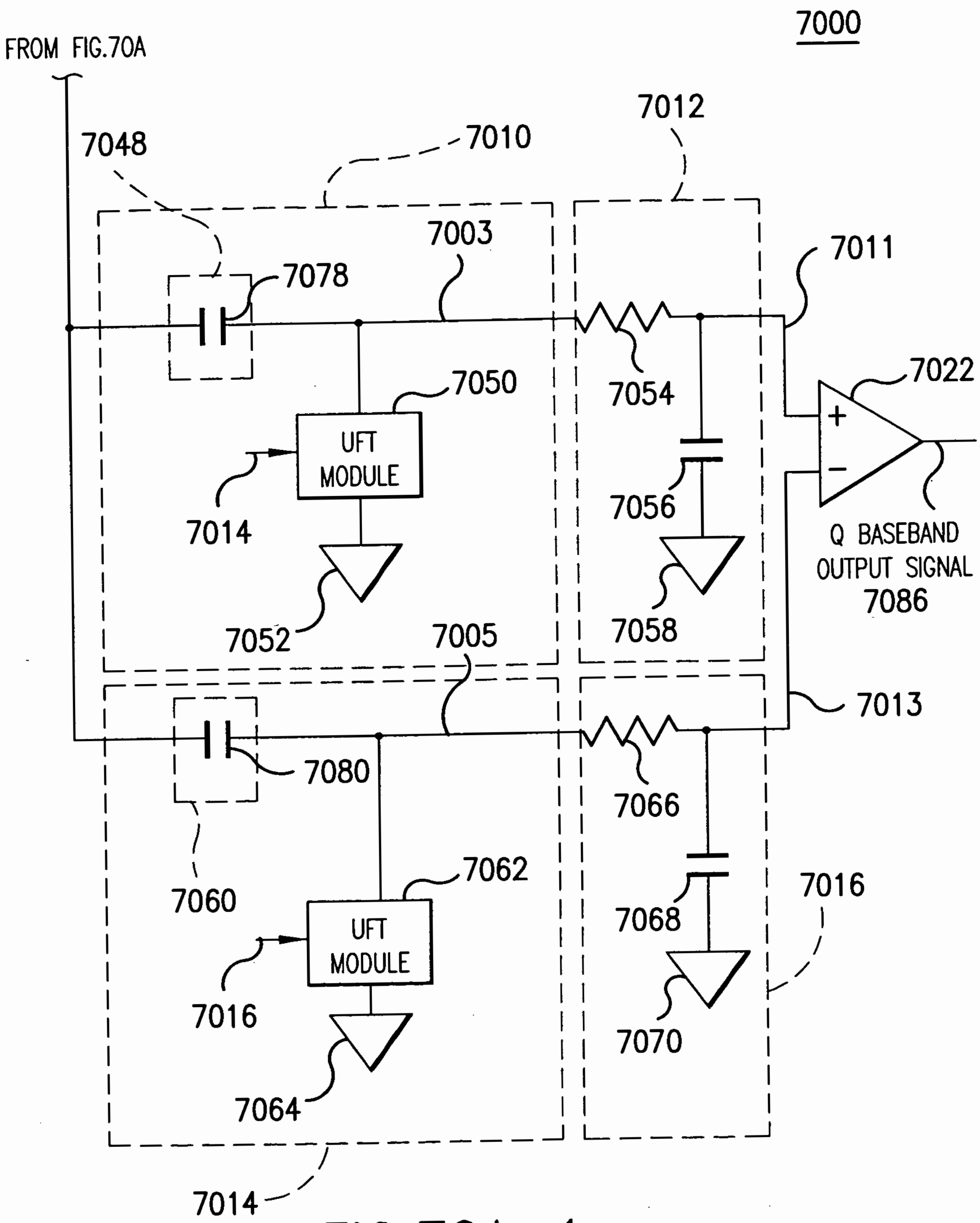
7000
FROM FIG.70A
7048
7010
7012
7003
7078
7011
7050
7054
7022
UFT MODULE
7014
7056
Q BASEBAND OUTPUT SIGNAL 7086
7052
7058
7005
7013
7080
7066
7062
7060
7016
7068
UFT MODULE
7016
7070
7064
7014

FIG.70A-1

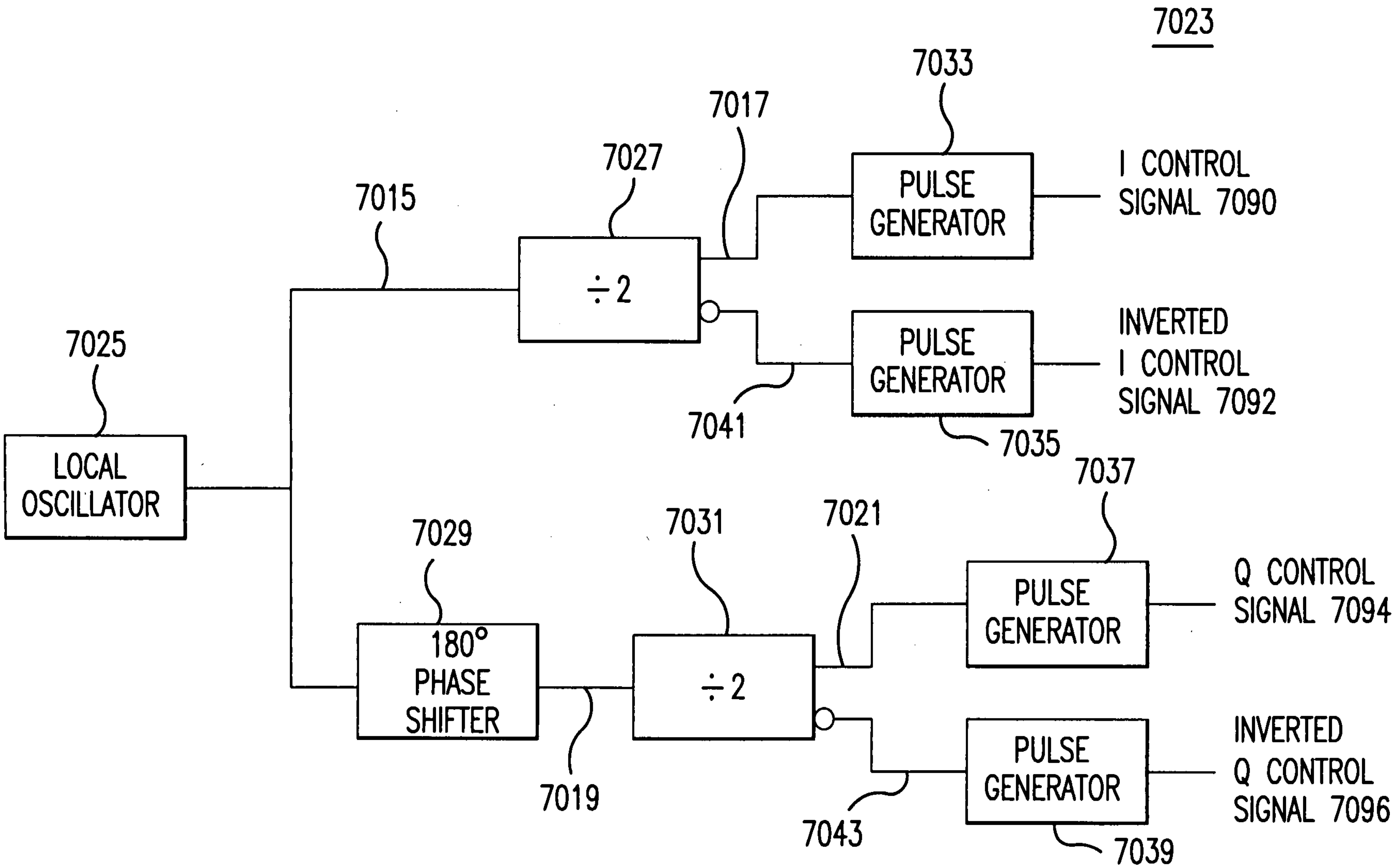

FIG.70B

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Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

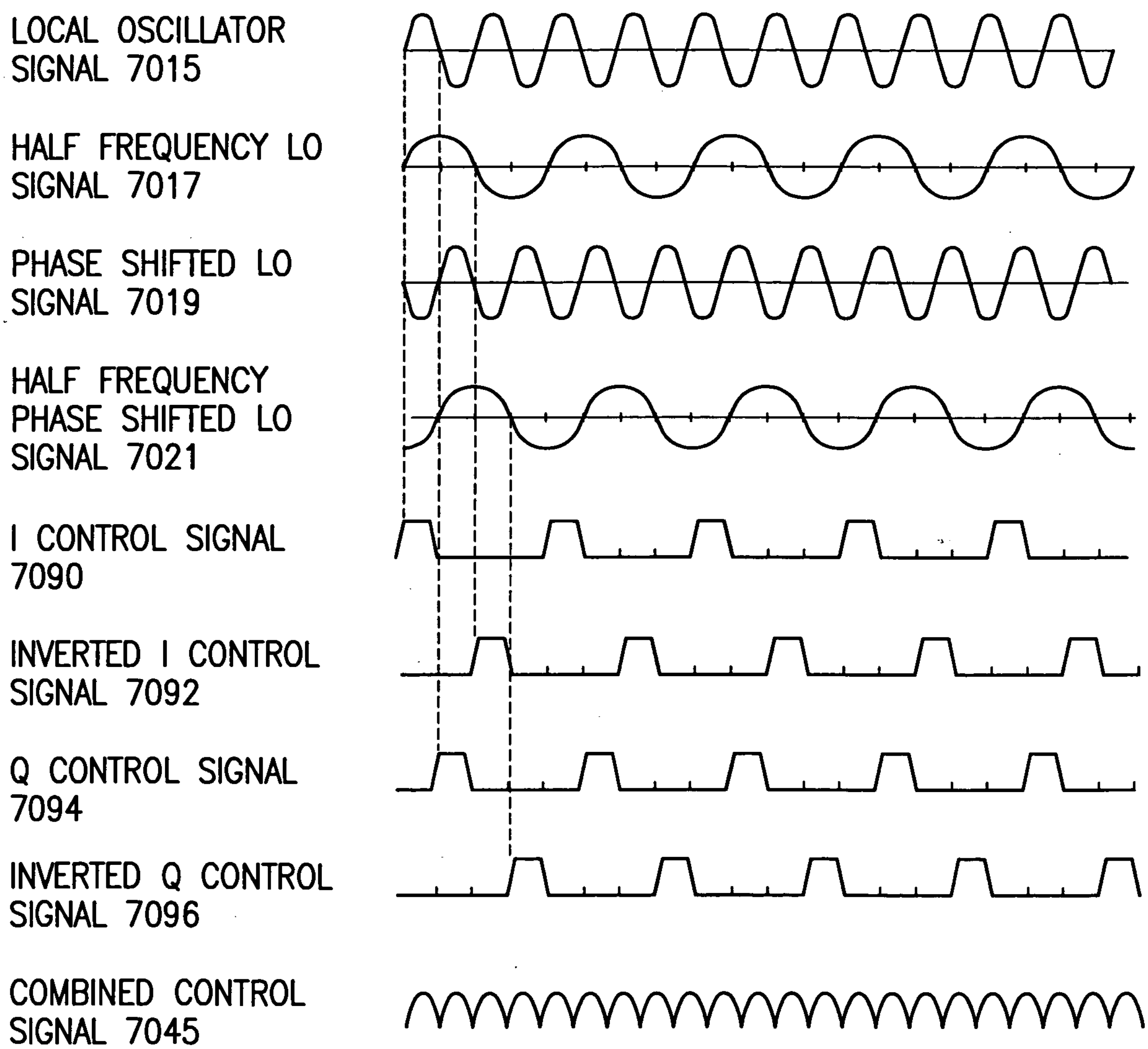
LOCAL OSCILLATOR SIGNAL 7015
HALF FREQUENCY LO SIGNAL 7017
PHASE SHIFTED LO SIGNAL 7019
HALF FREQUENCY PHASE SHIFTED LO SIGNAL 7021
I CONTROL SIGNAL 7090
INVERTED I CONTROL SIGNAL 7092
Q CONTROL SIGNAL 7094
INVERTED Q CONTROL SIGNAL 7096
COMBINED CONTROL SIGNAL 7045

FIG.70C

(A) IQDEMOD PULSE RELATIONSHIPS TO INPUT RF CARRIER

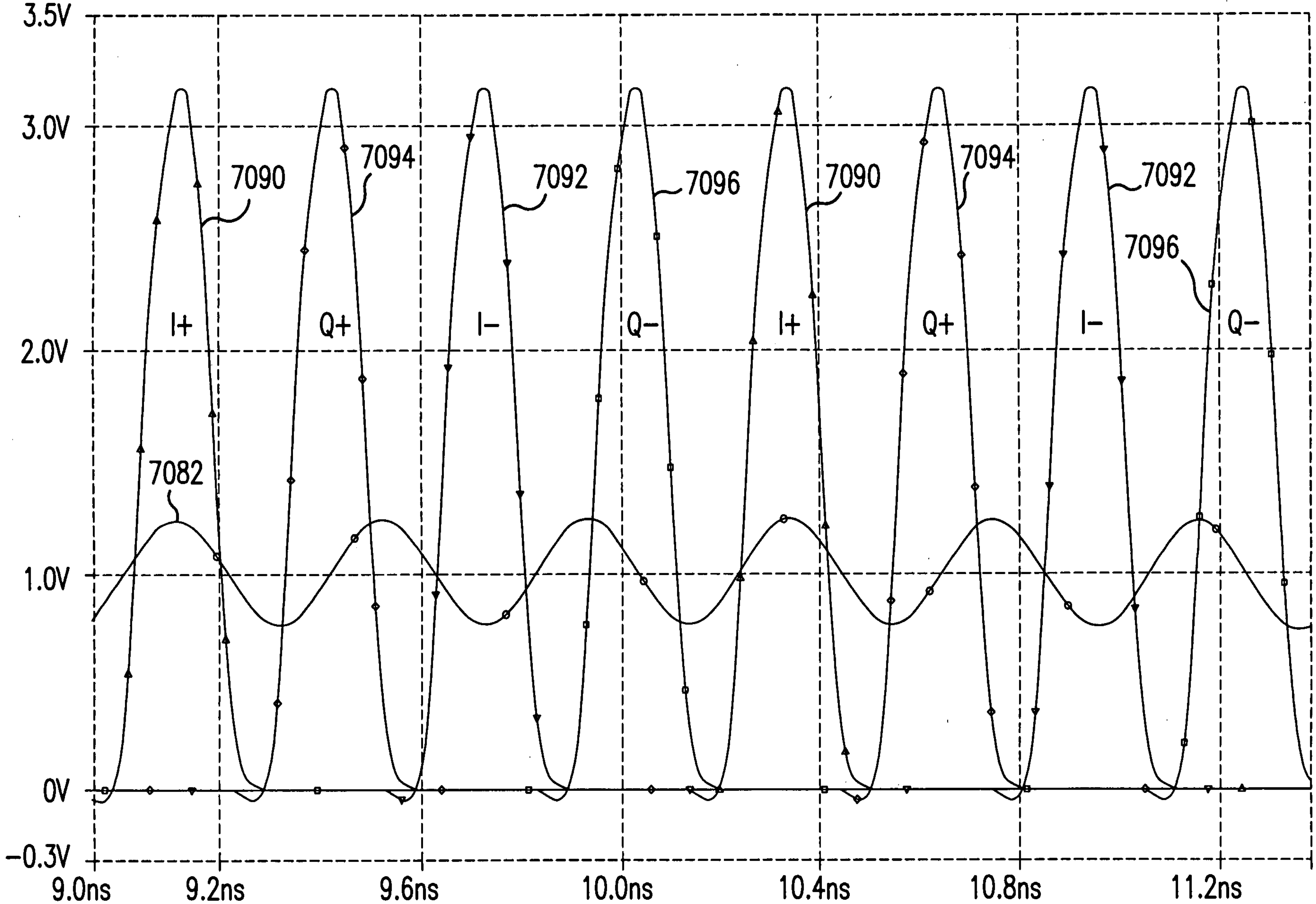

FIG.70D

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Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

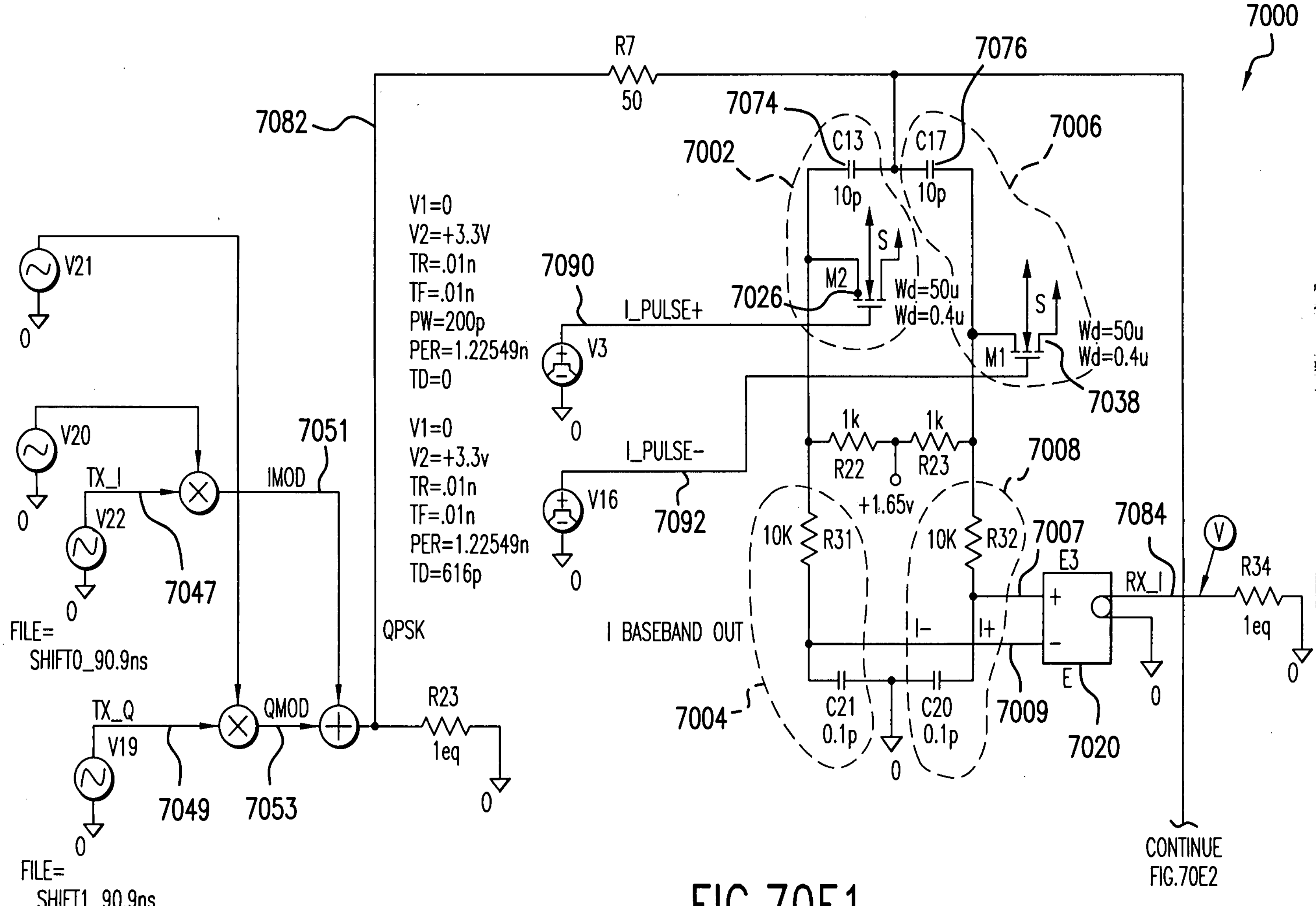

FIG.70E1

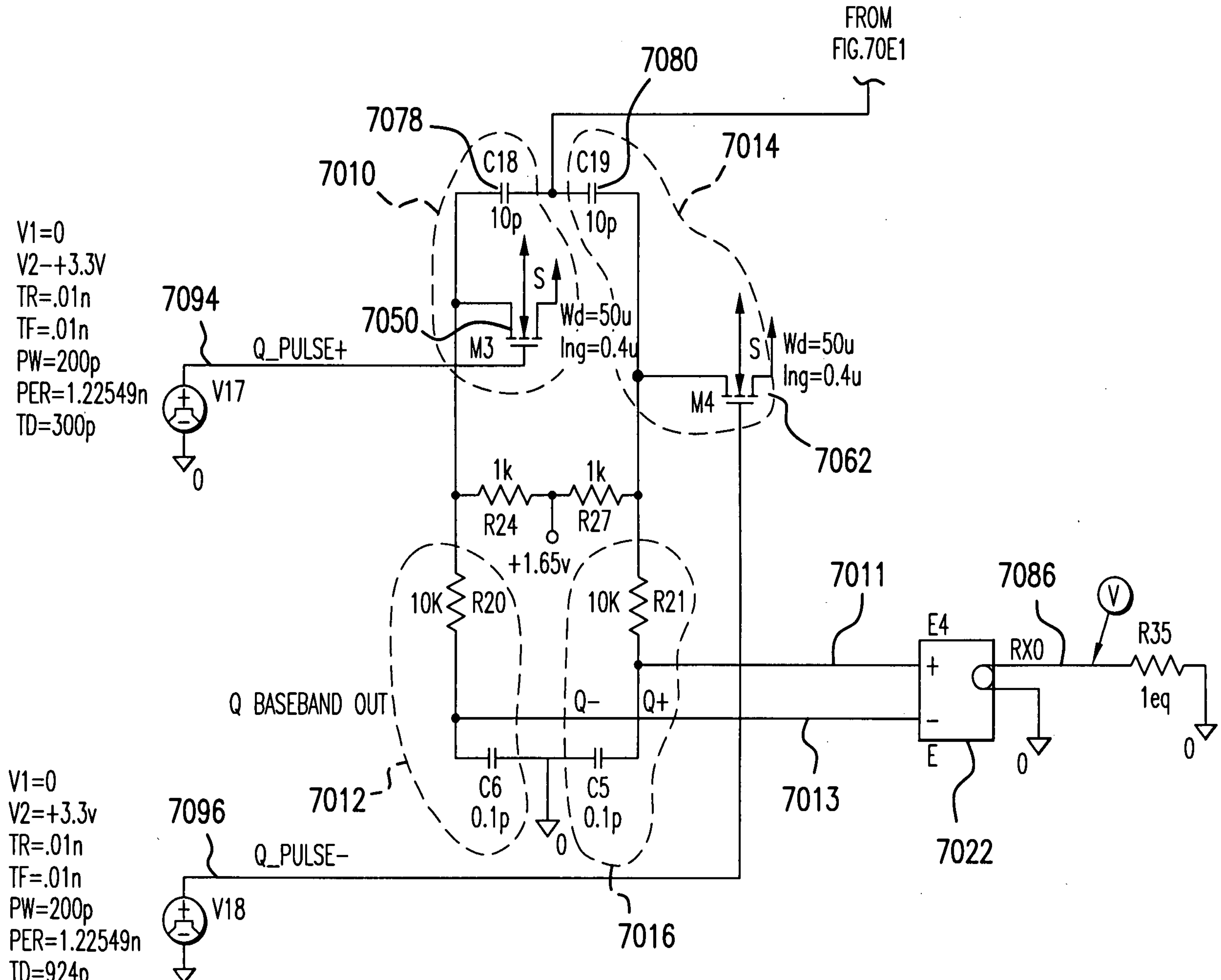

FIG.70E2

New Sheet
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Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

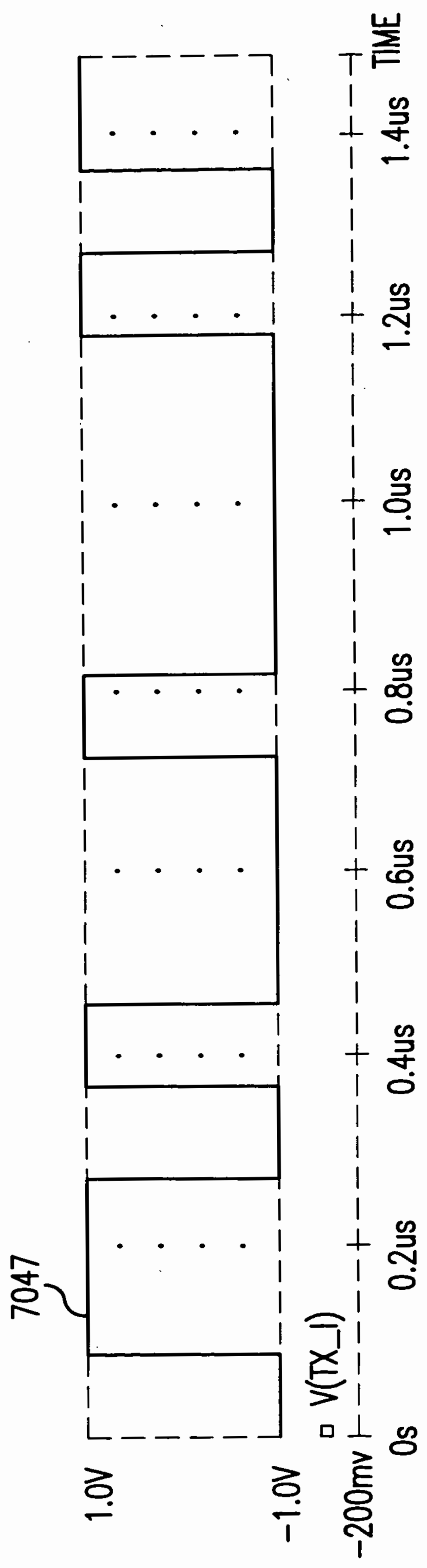

FIG.70F

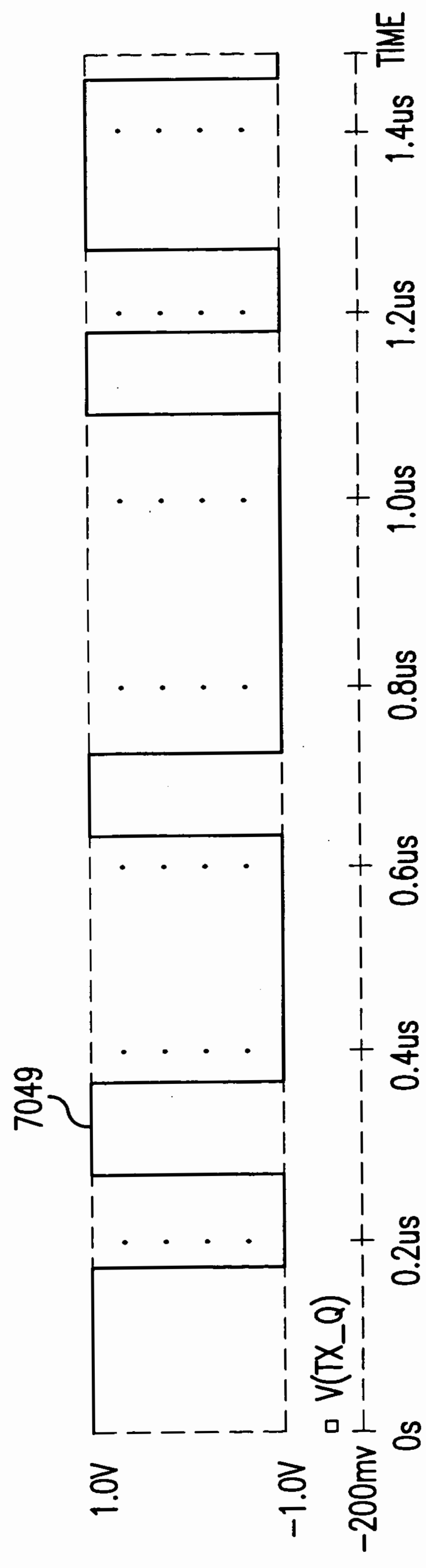

FIG.70G

FIG. 70H

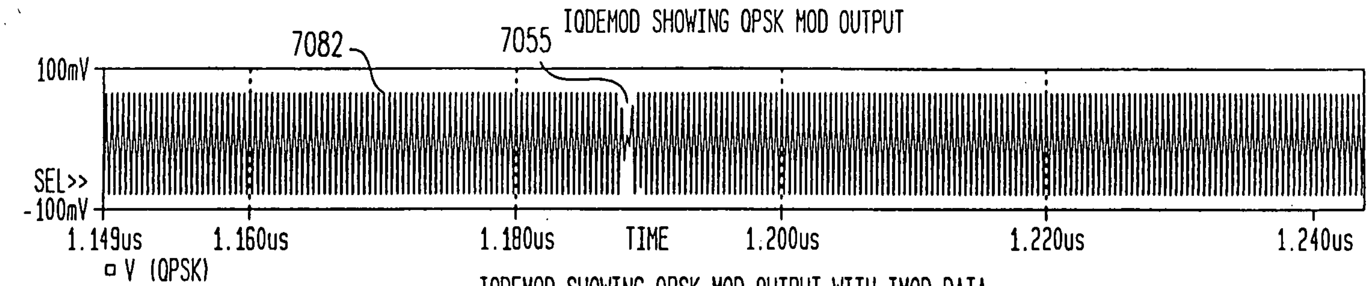

FIG. 70I

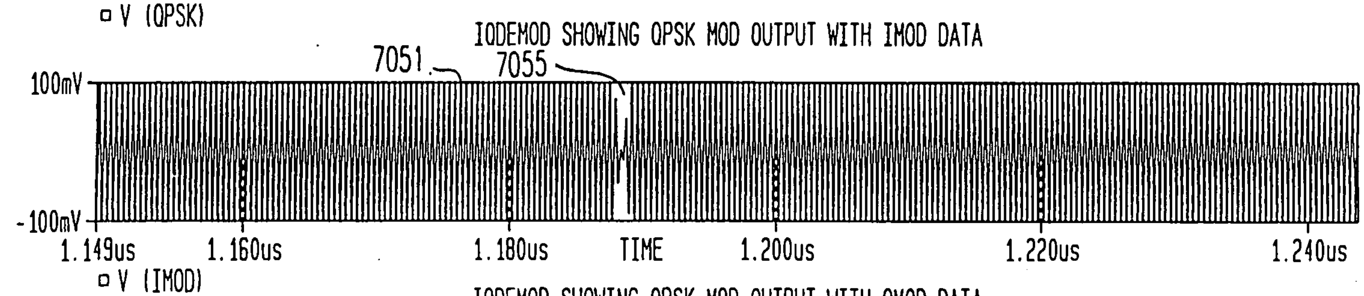

FIG. 70J

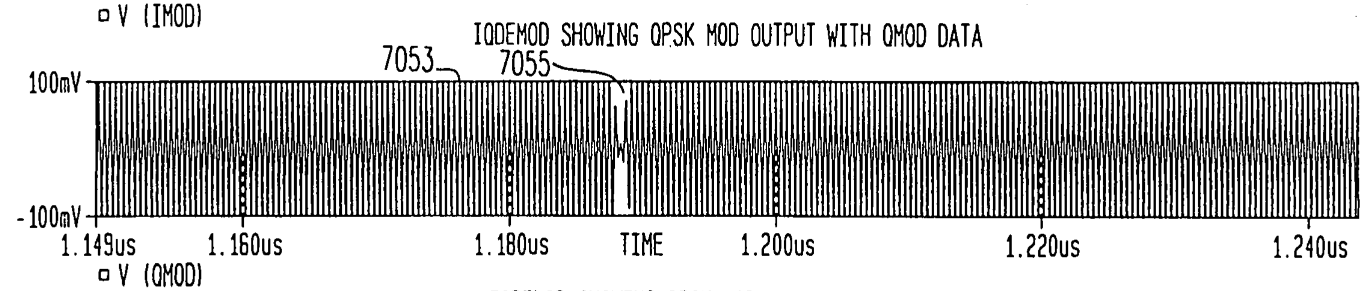

FIG. 70K

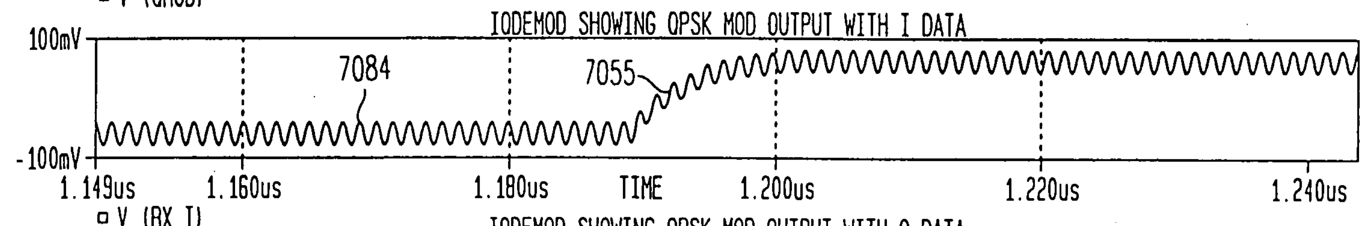

FIG. 70L

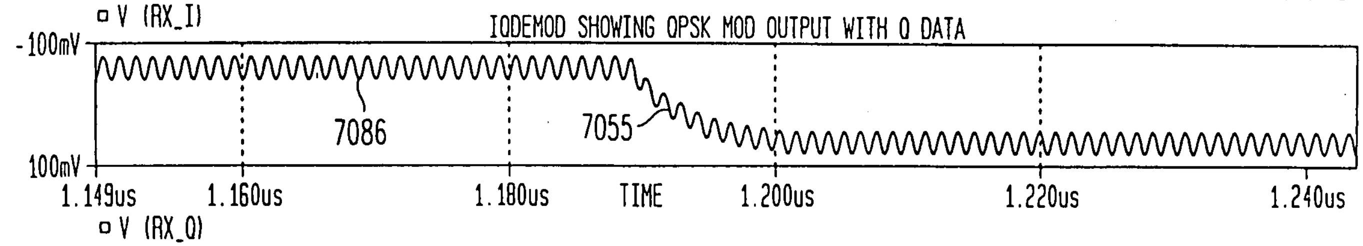

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FIG. 70M

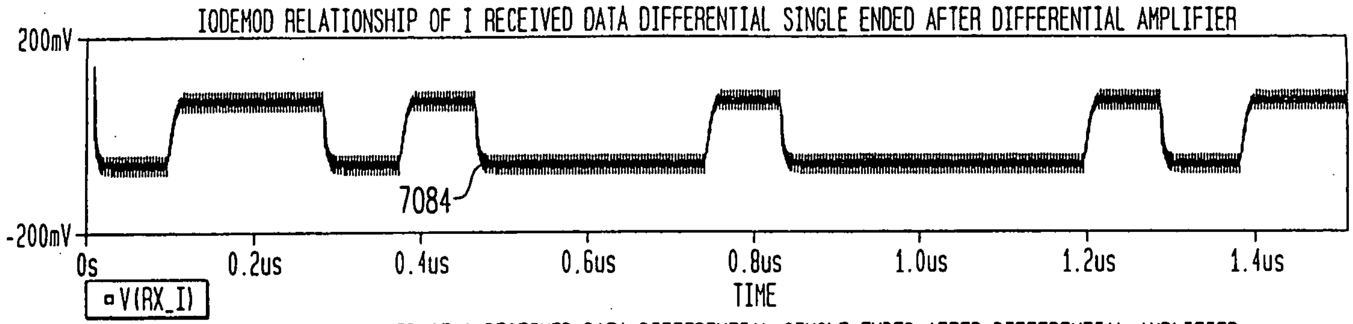


FIG. 70N

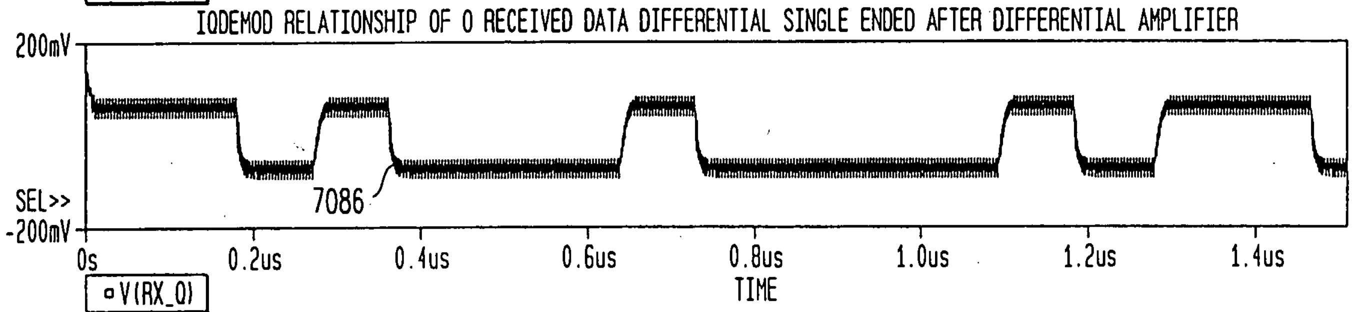


FIG. 70O

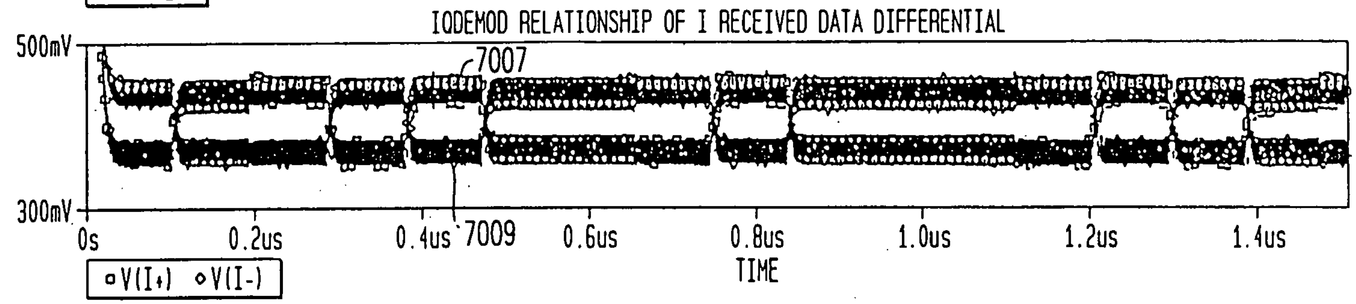
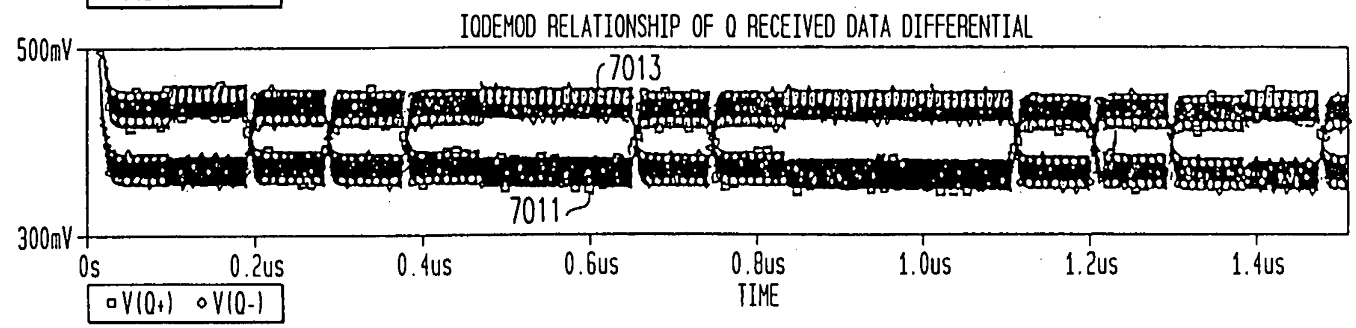


FIG. 70P



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Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

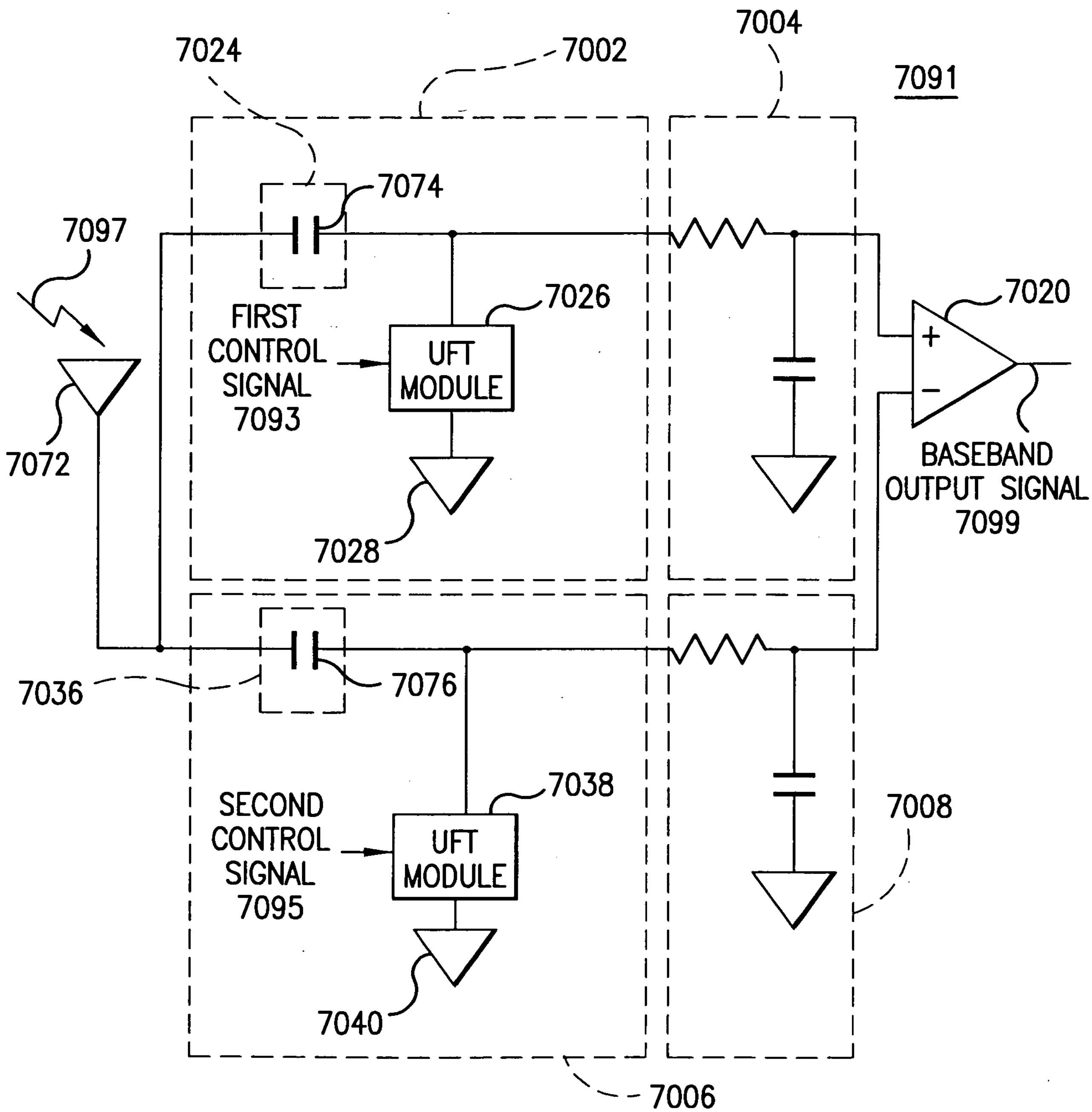
7024
7002
7004
7091
7074
7097
7026
7020
FIRST CONTROL SIGNAL 7093
UFT MODULE
+
−
7072
BASEBAND OUTPUT SIGNAL 7099
7028
7036
7076
7038
SECOND CONTROL SIGNAL 7095
UFT MODULE
7008
7040
7006

FIG.70Q

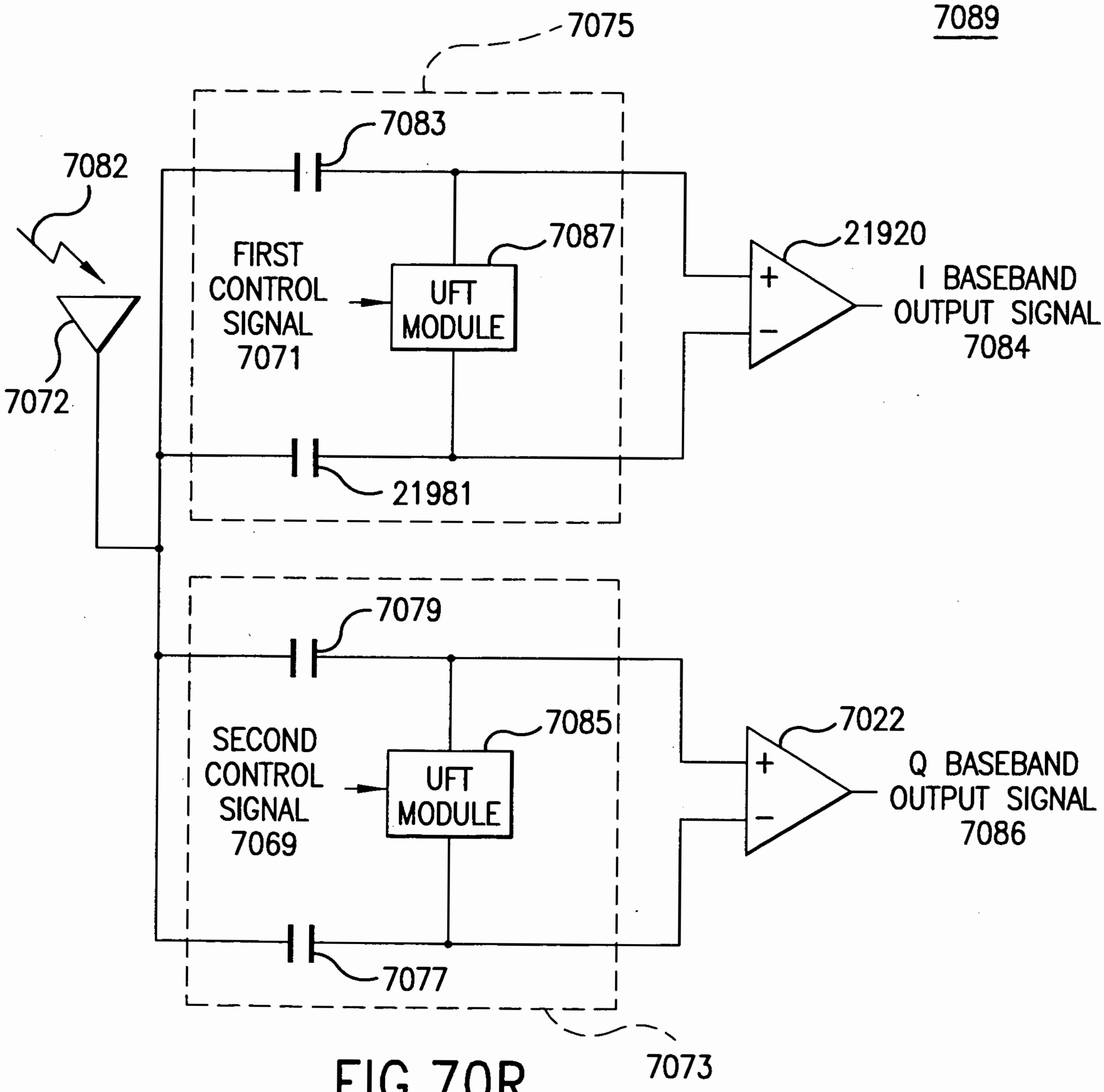
7089
7075
7083
7082
7087
21920
FIRST
CONTROL
SIGNAL
7071
UFT
MODULE
+
−
I BASEBAND
OUTPUT SIGNAL
7084
7072
21981
7079
7085
7022
SECOND
CONTROL
SIGNAL
7069
UFT
MODULE
+
−
Q BASEBAND
OUTPUT SIGNAL
7086
7077
7073

FIG.70R

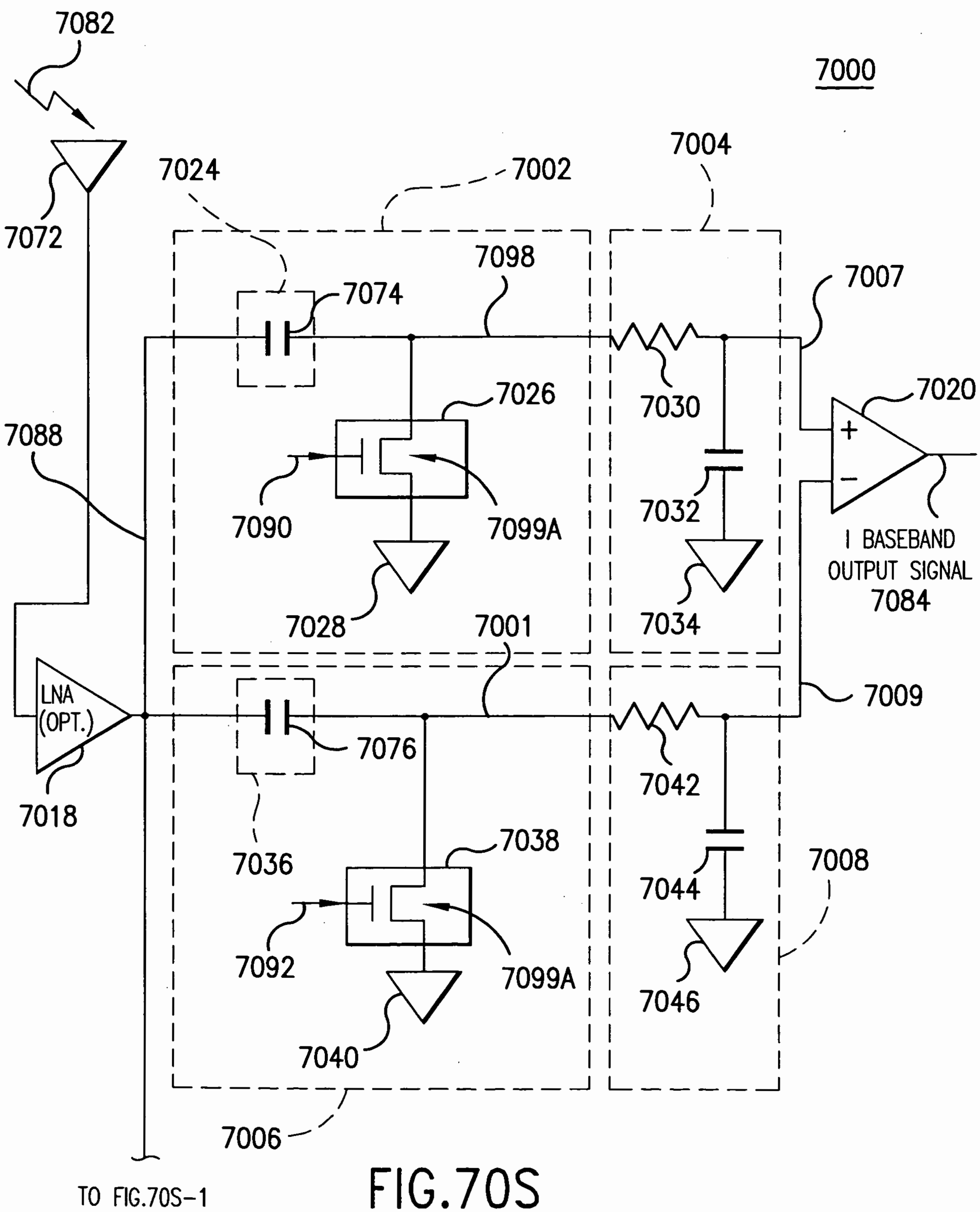
7082
7000
7072
7024
7002
7004
7098
7074
7007
7026
7020
7088
7030
7090
7099A
7032
I BASEBAND
OUTPUT SIGNAL
7084
7028
7001
7034
7009
LNA
(OPT.)
7076
7042
7018
7036
7038
7008
7044
7092
7099A
7046
7040
7006
TO FIG.70S-1

FIG.70S

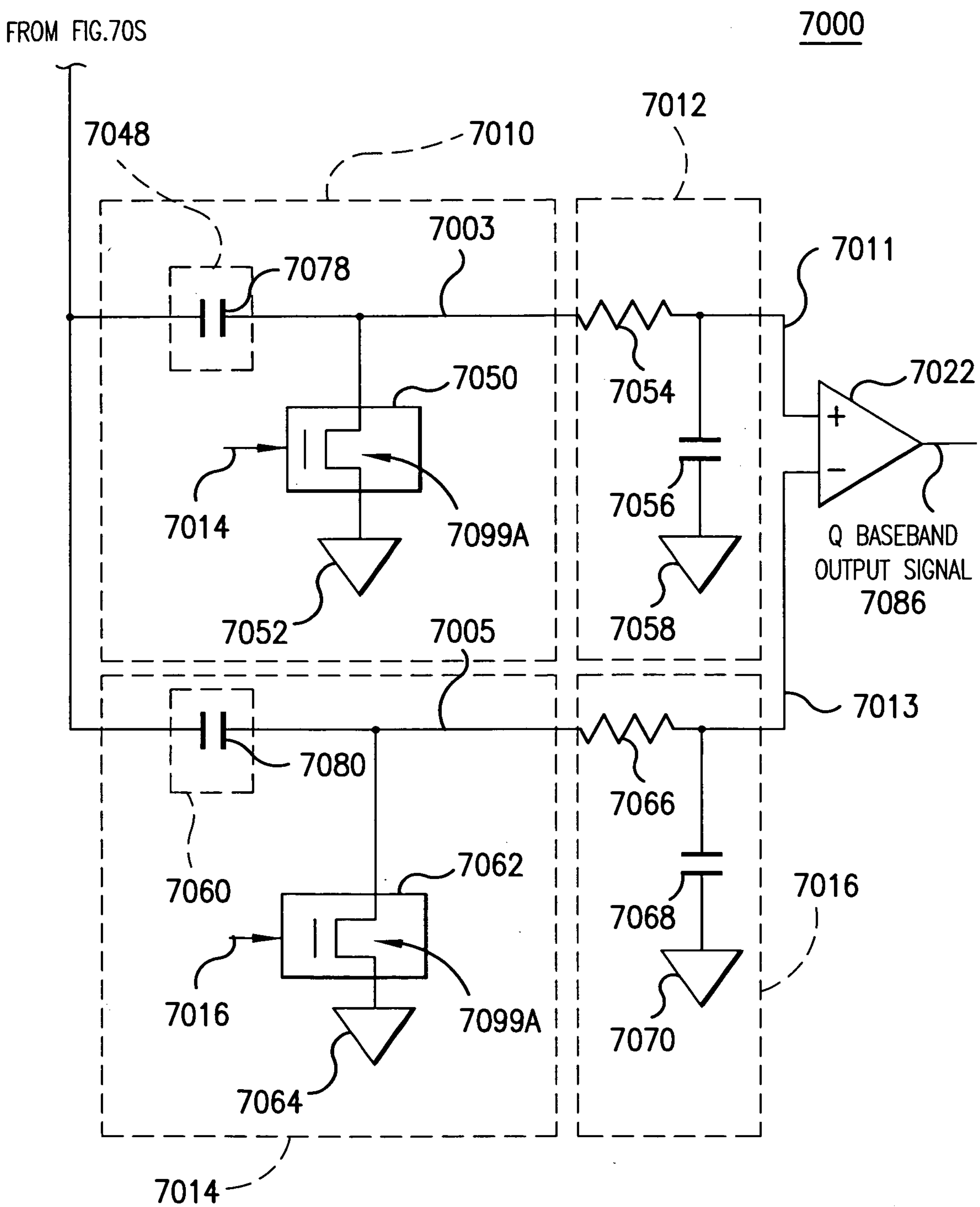
FROM FIG.70S
7000
7048
7010
7012
7003
7078
7011
7050
7054
7022
7014
7099A
7056
Q BASEBAND
OUTPUT SIGNAL
7086
7052
7005
7058
7013
7080
7066
7060
7062
7016
7068
7016
7099A
7070
7064
7014

FIG.70S-1

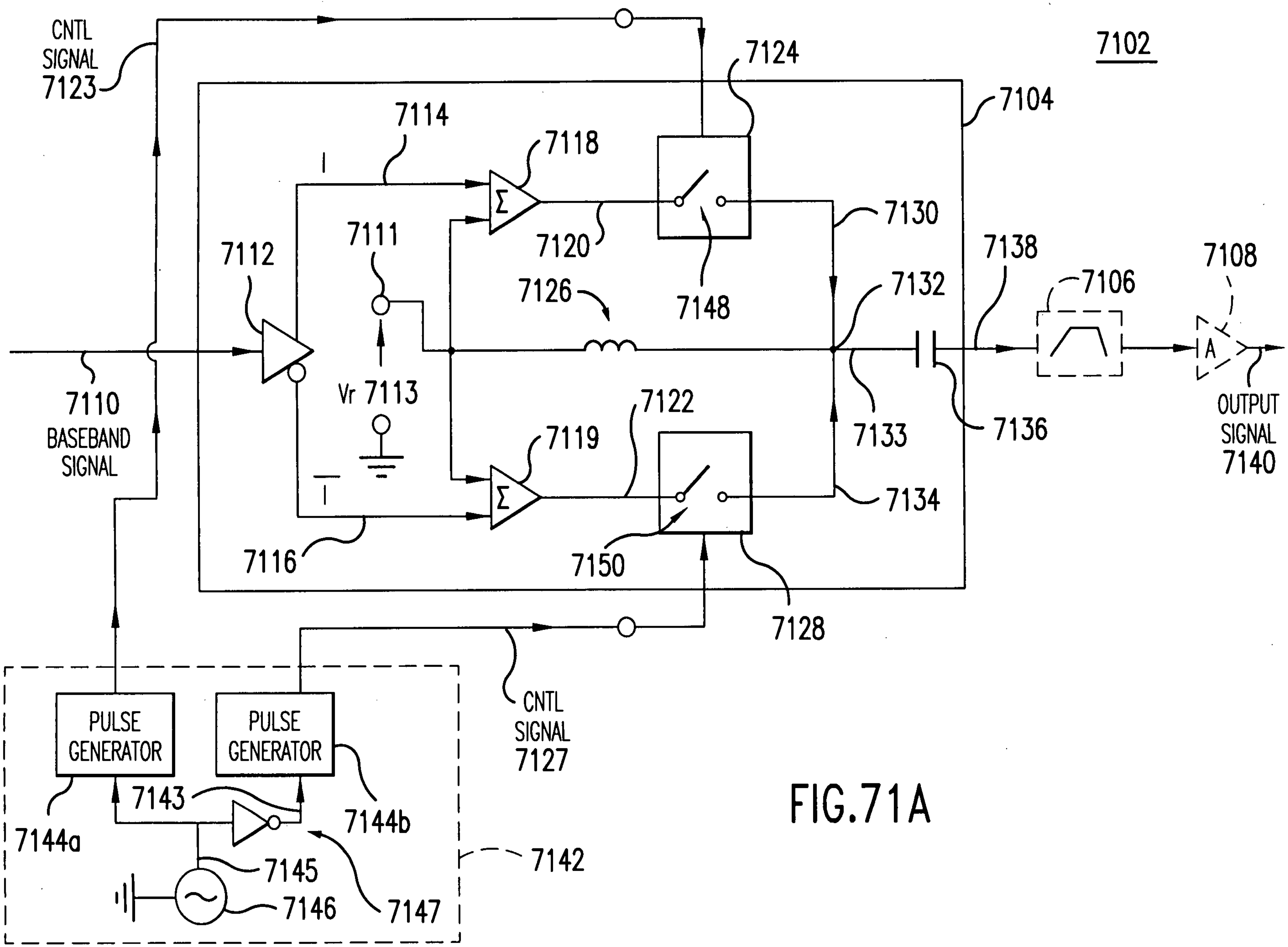

FIG.71A

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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

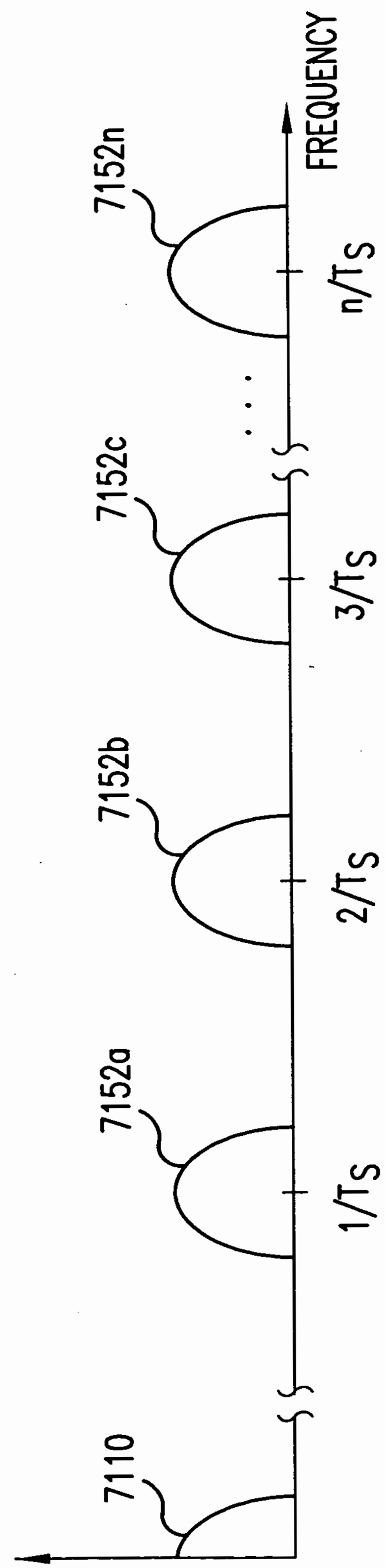

FIG.71B

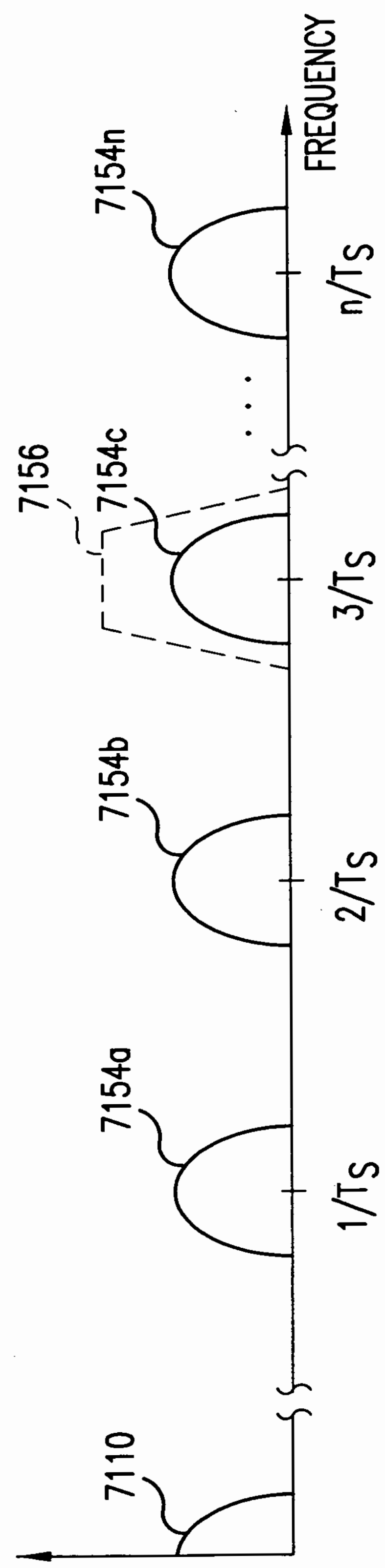

FIG.71C

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Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

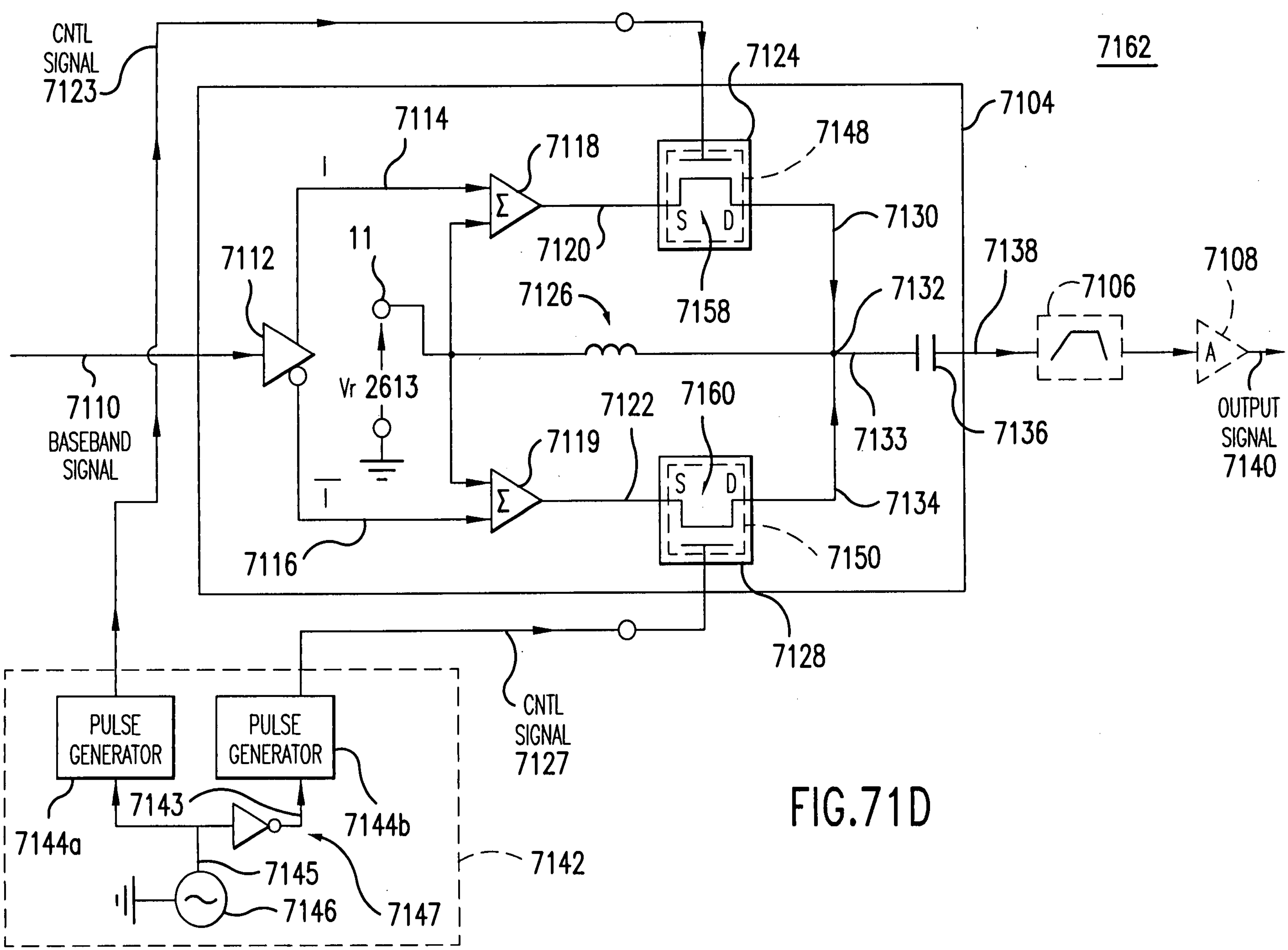

FIG.71D

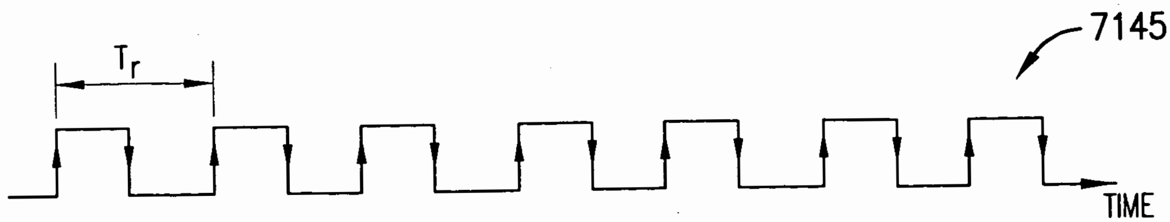

FIG.72A

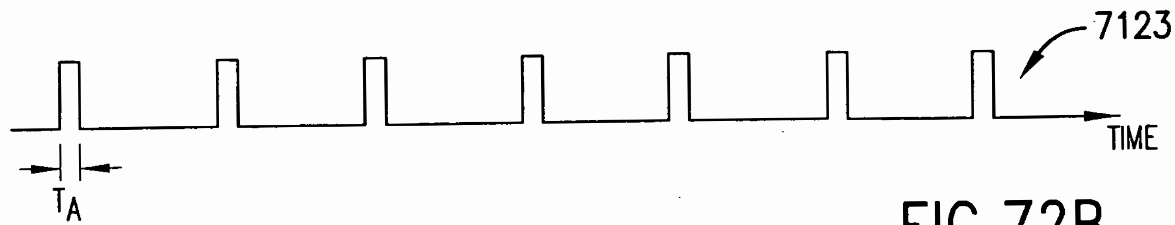

FIG.72B

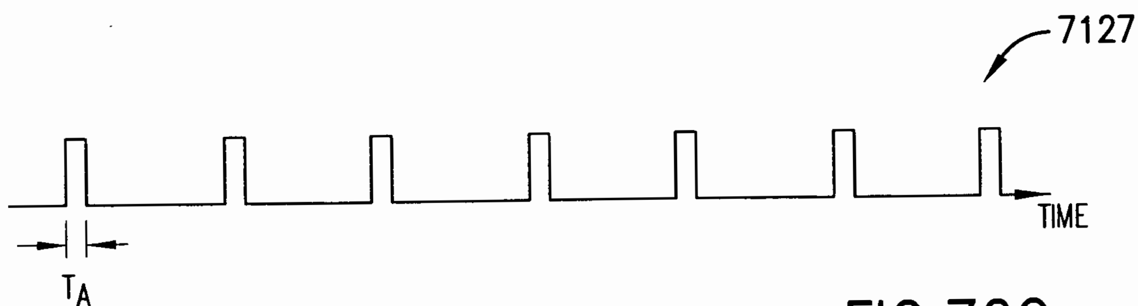

FIG.72C

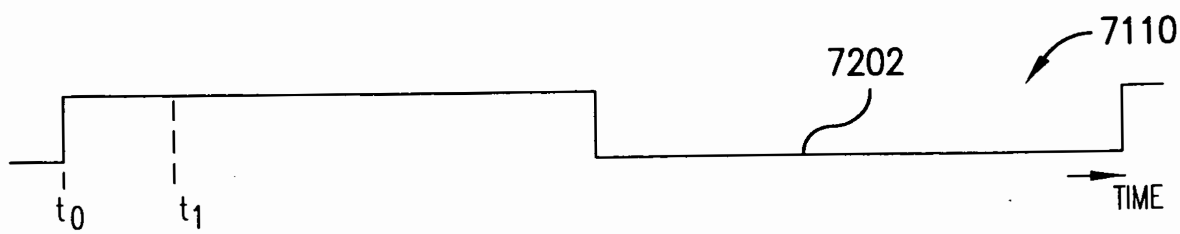

FIG.72D

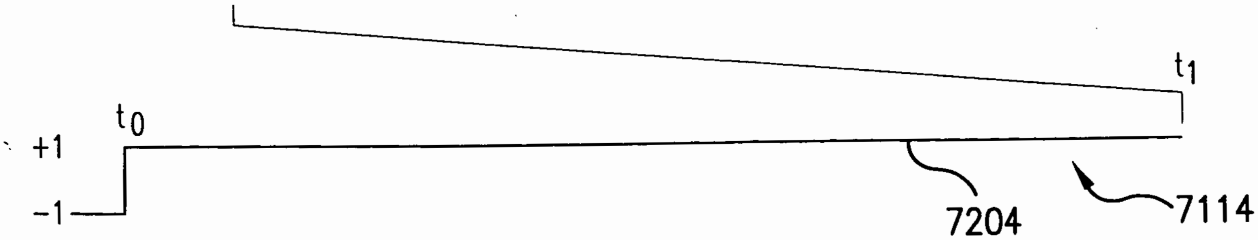

FIG.72E

FIG.72F

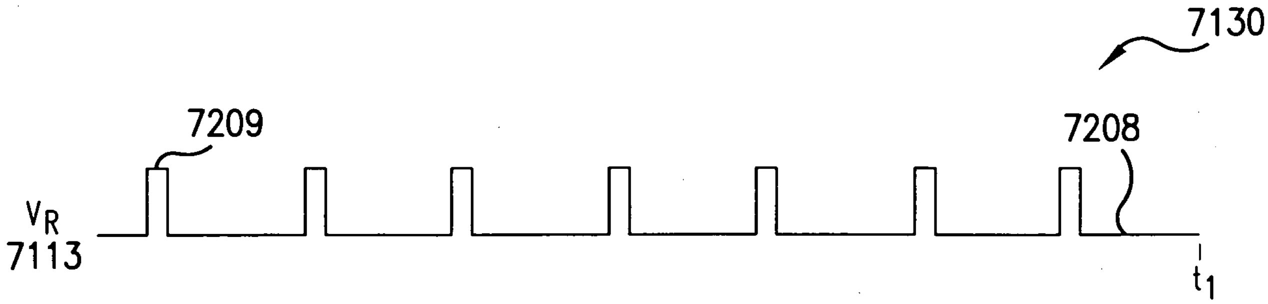

FIG.72G

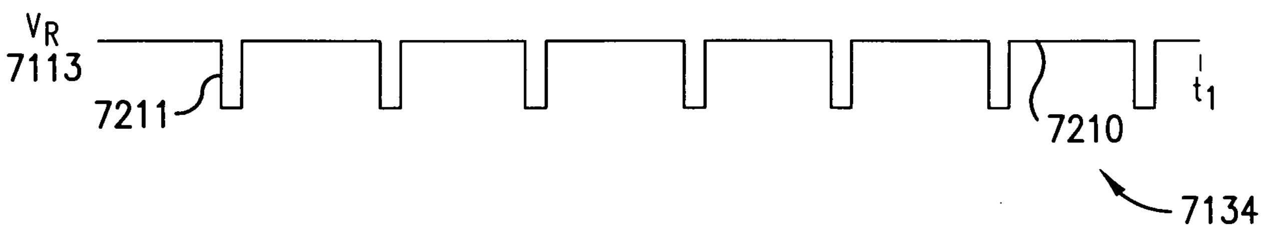

FIG.72H

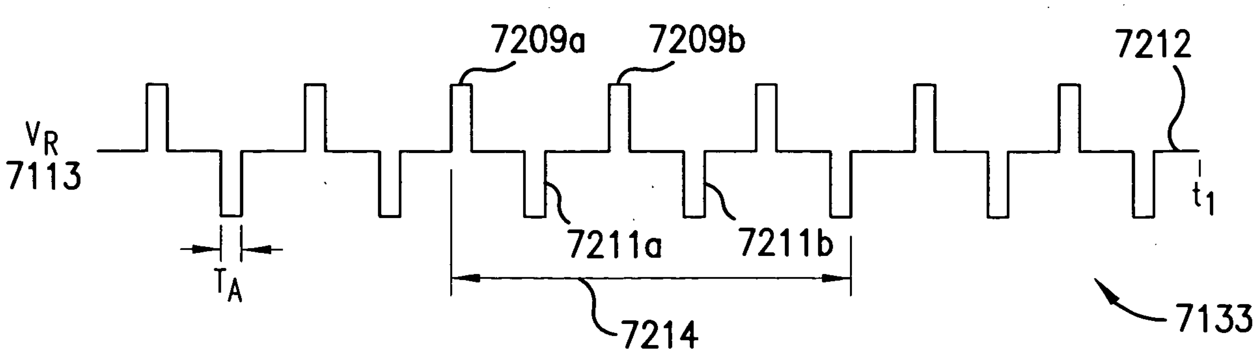

FIG.72I

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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

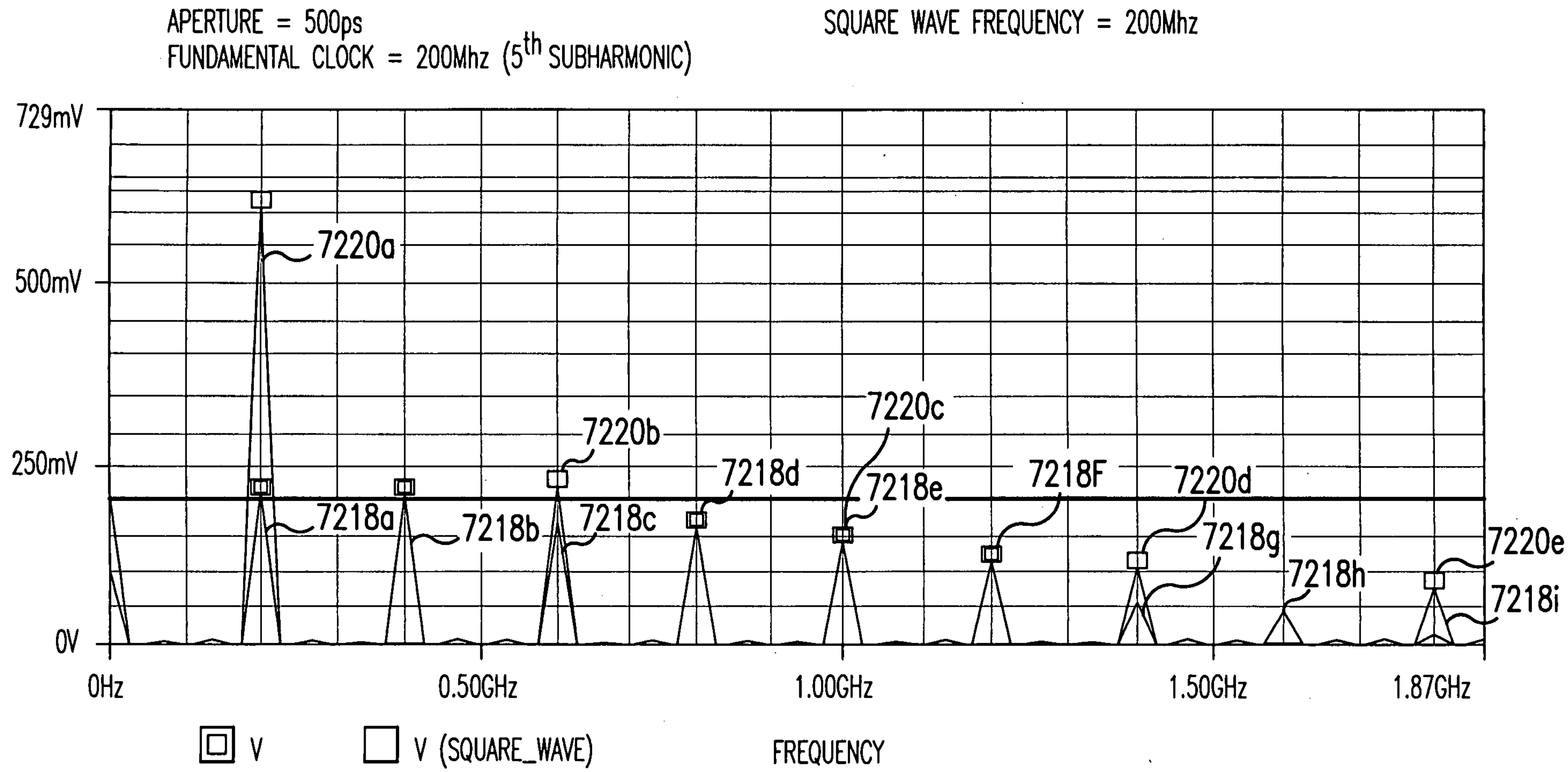

FIG.72J

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Inventors: Sorrells et al.
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Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

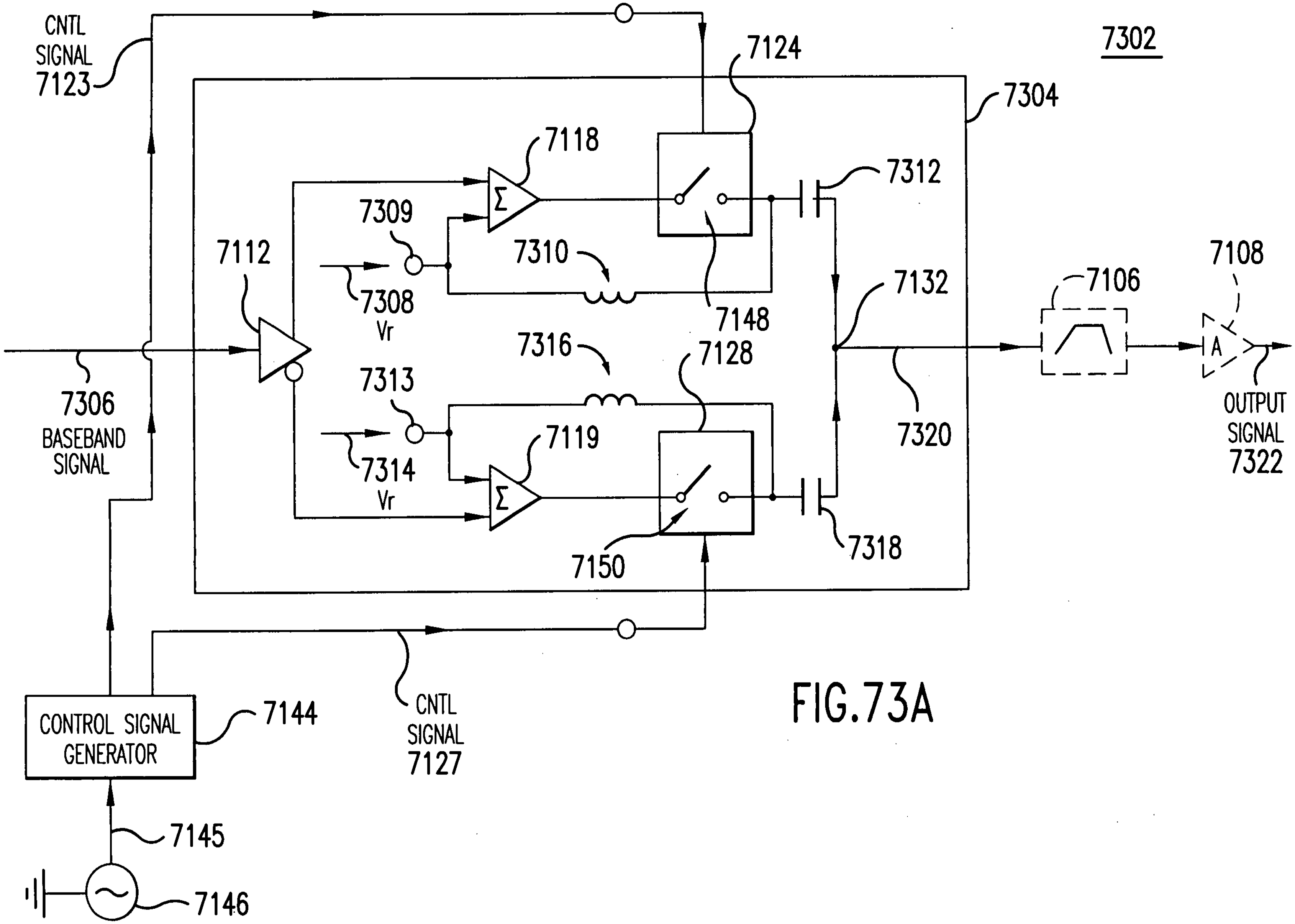

FIG.73A

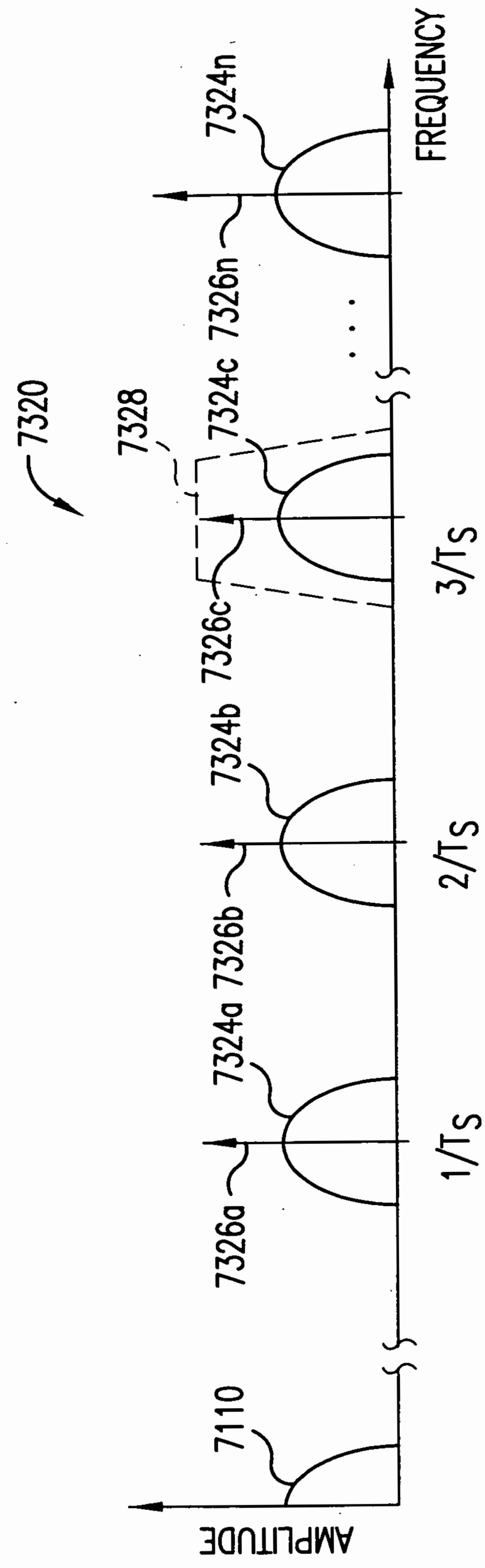
7320
7328
7110
7326a
7324a
7326b
7324b
7326c
7324c
7326n
7324n
1/Ts
2/Ts
3/Ts
AMPLITUDE
FREQUENCY

FIG.73B

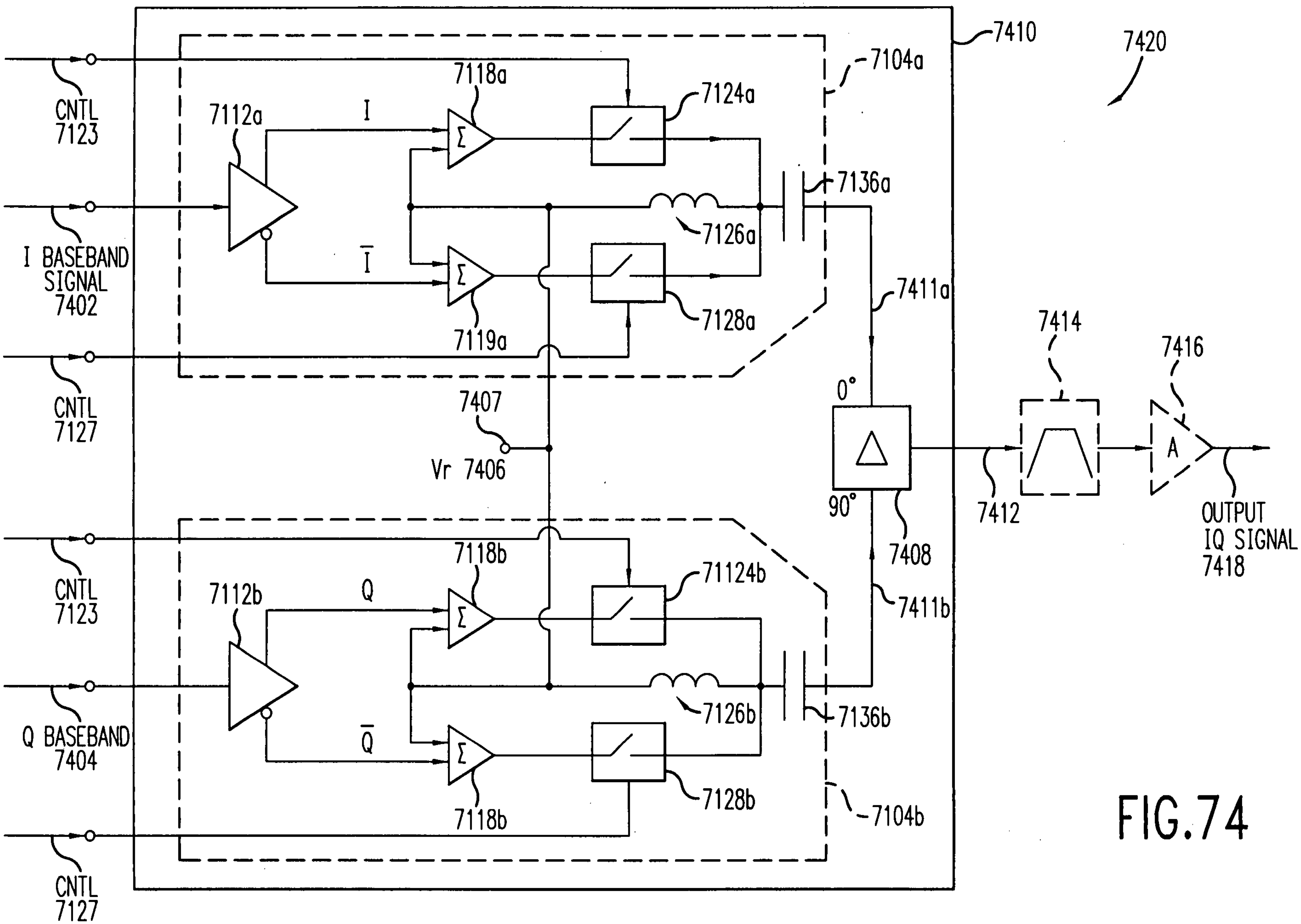

FIG.74

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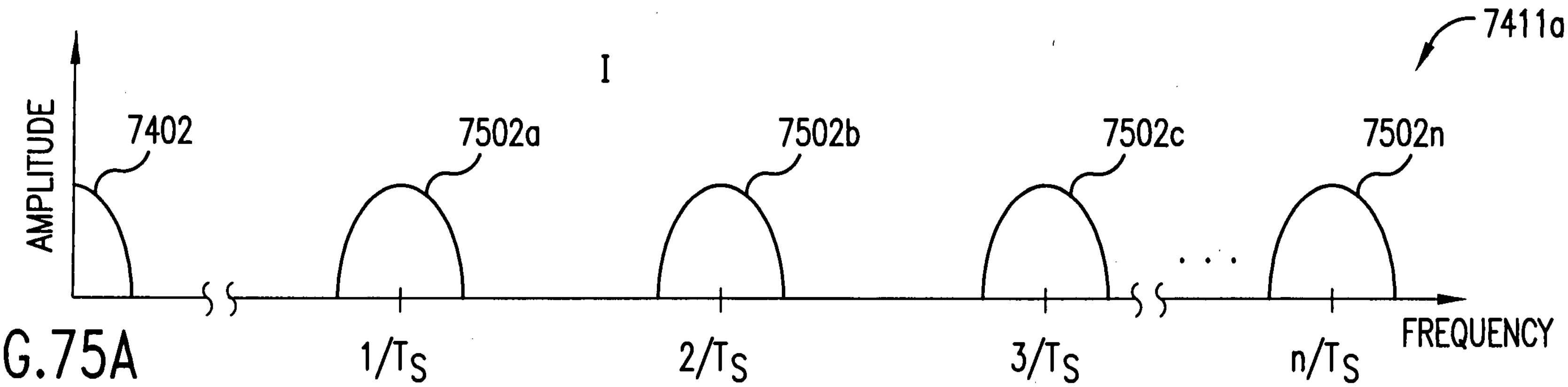

FIG.75A

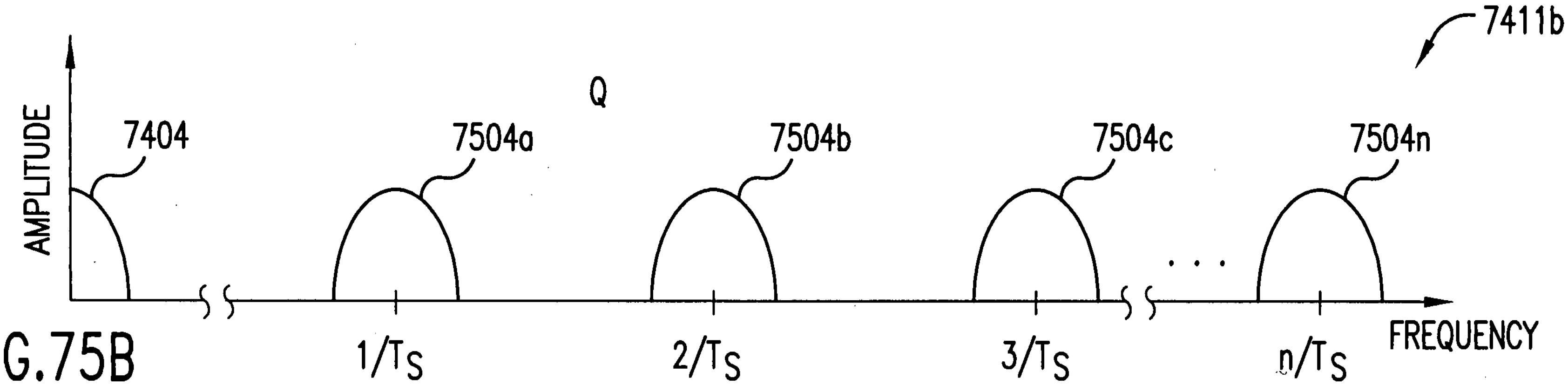

FIG.75B

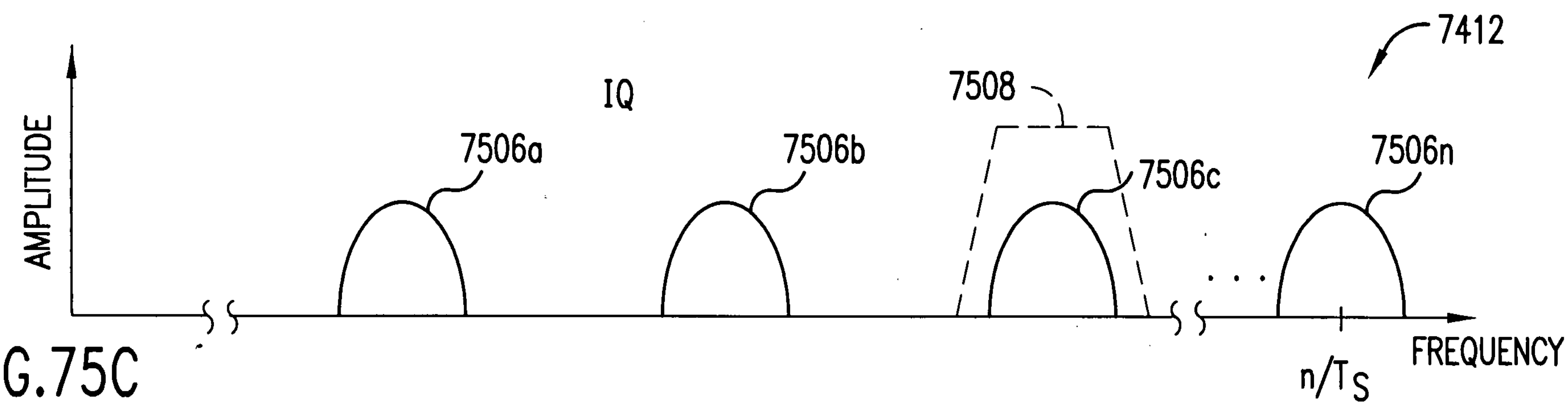

FIG.75C

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Inventors: Sorrells et al.
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Universal Frequency Translation Technology
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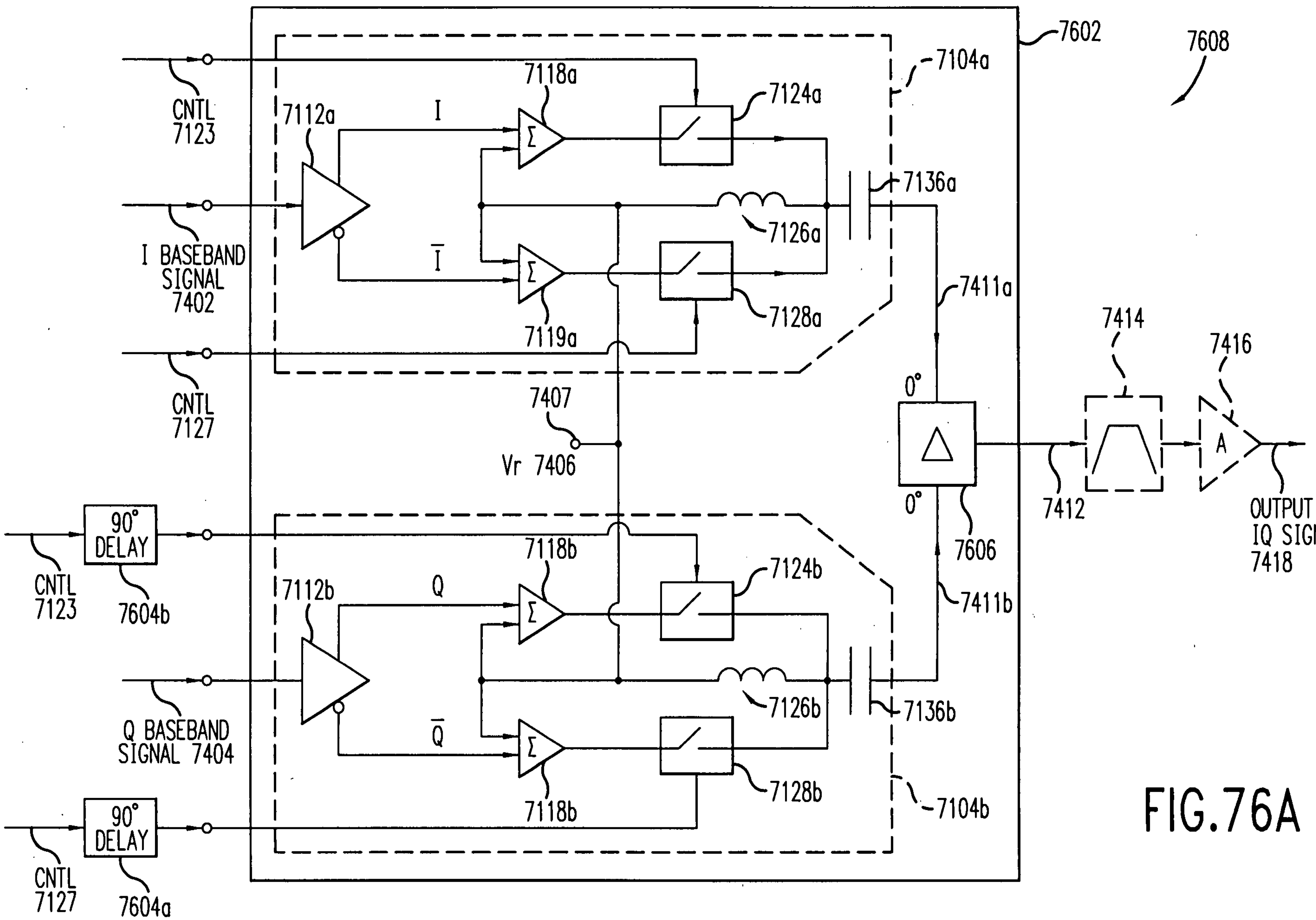

FIG.76A

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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
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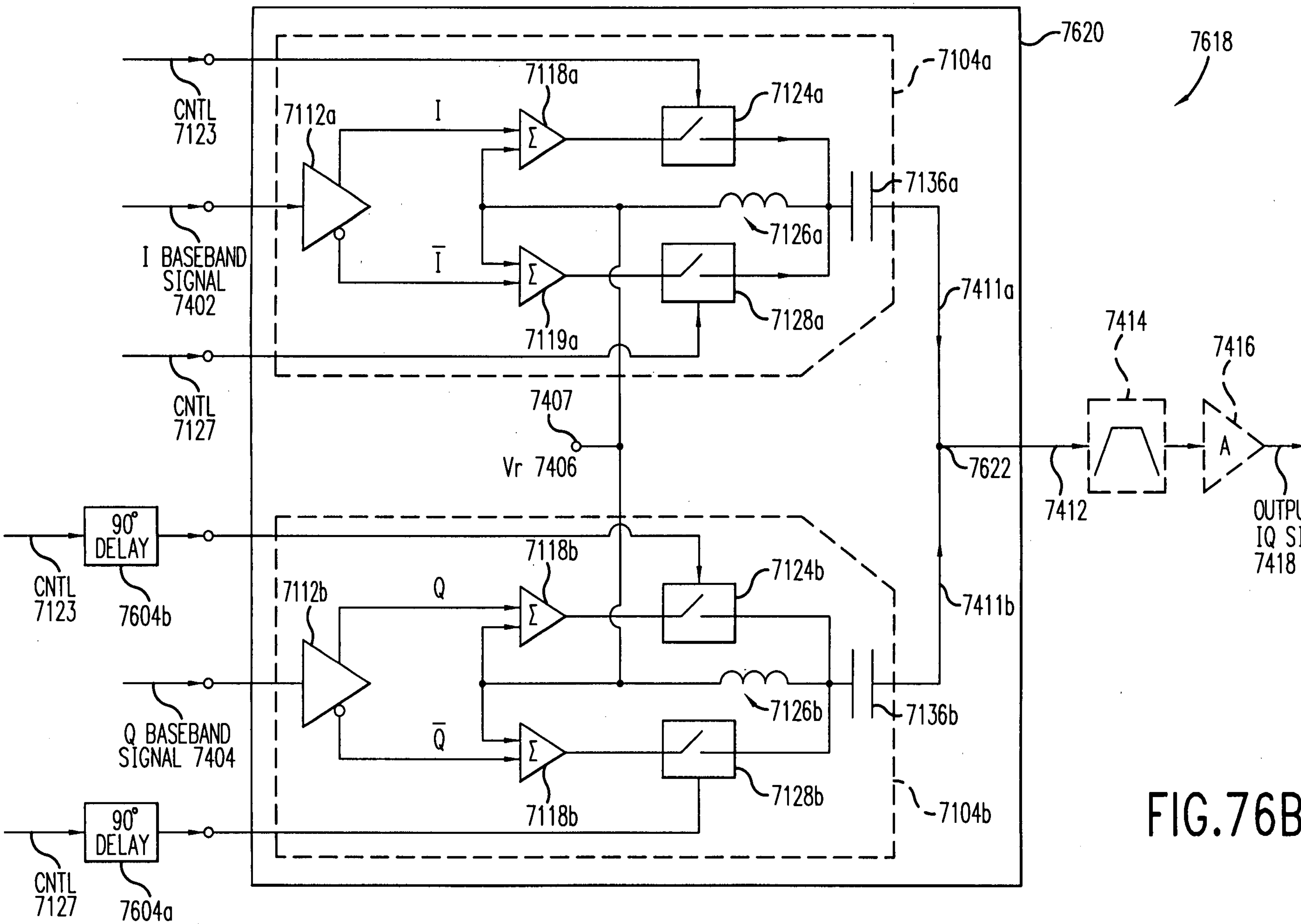

FIG.76B

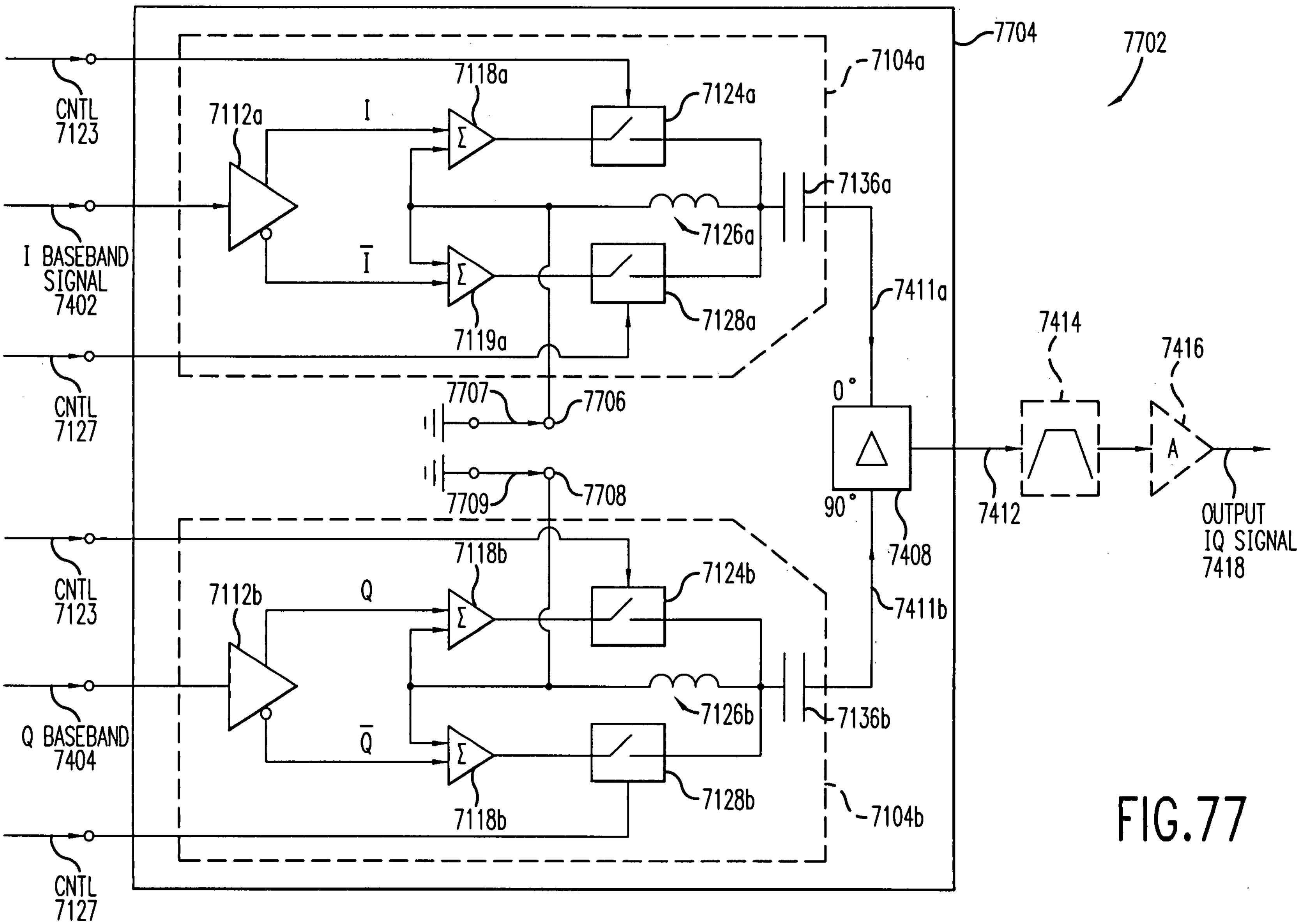

FIG.77

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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

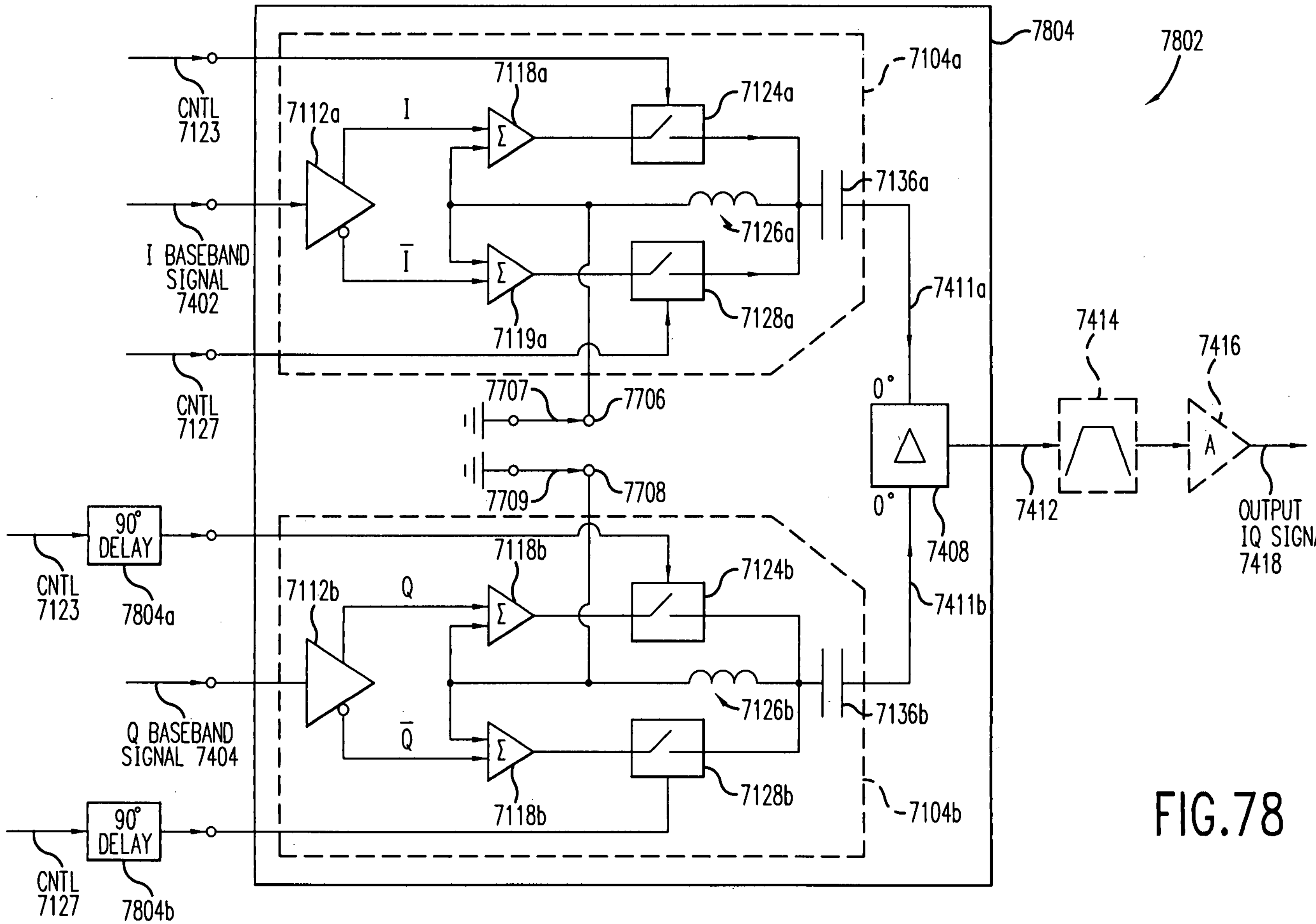

FIG.78

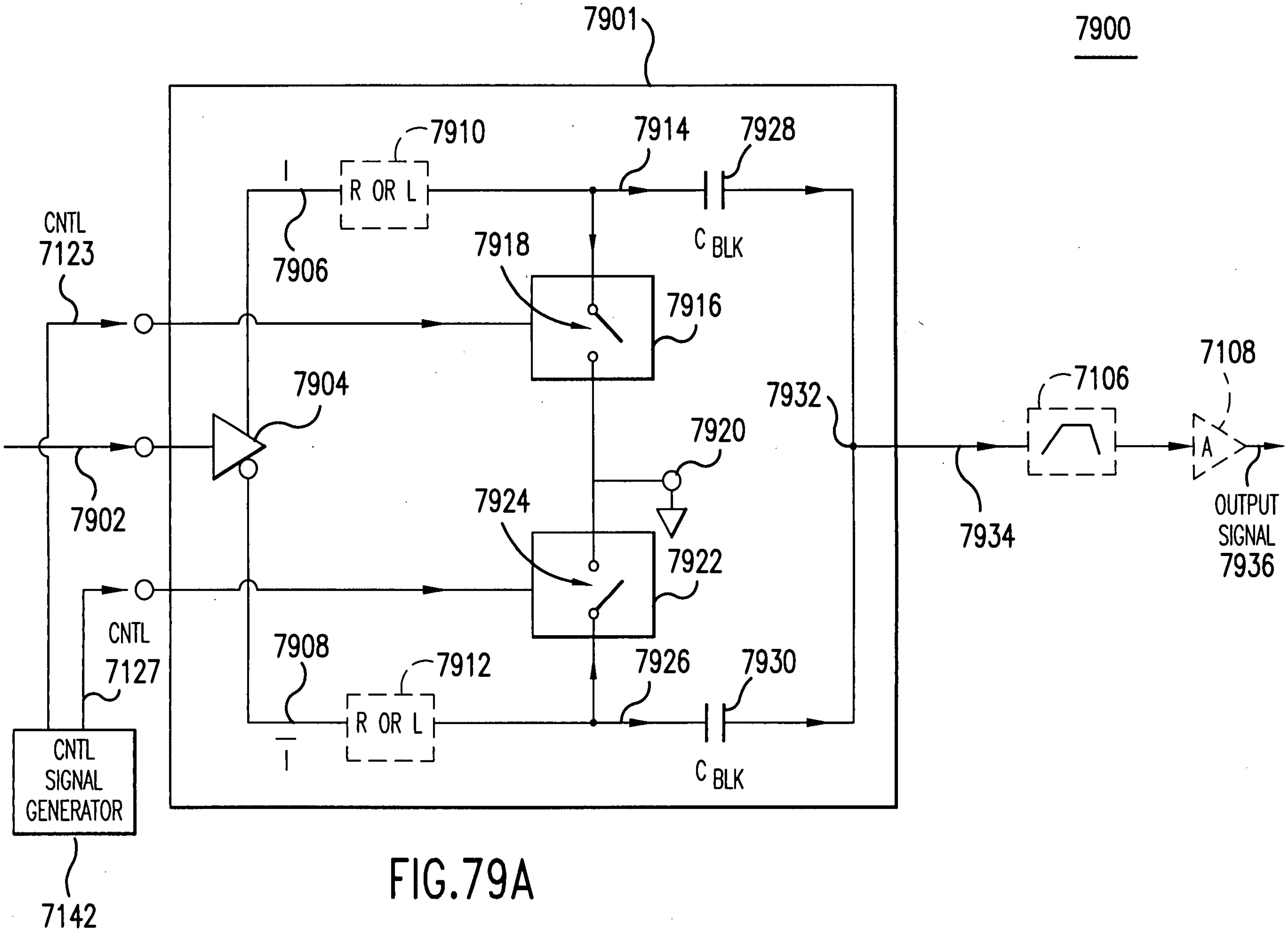

FIG.79A

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Inventors: Sorrells et al.
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For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

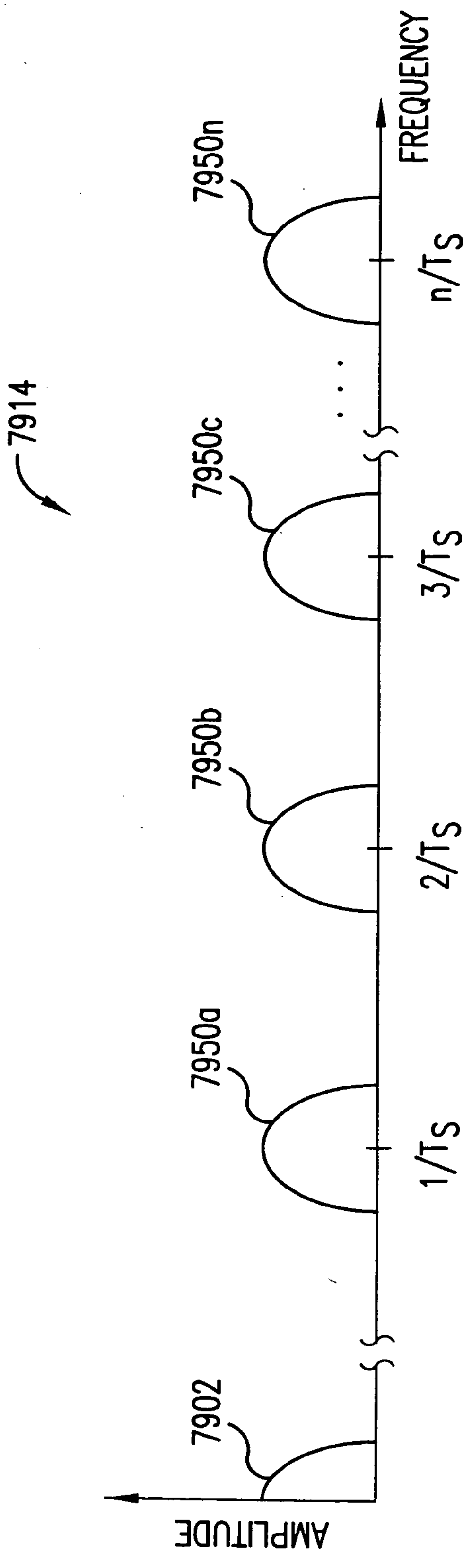

FIG.79B

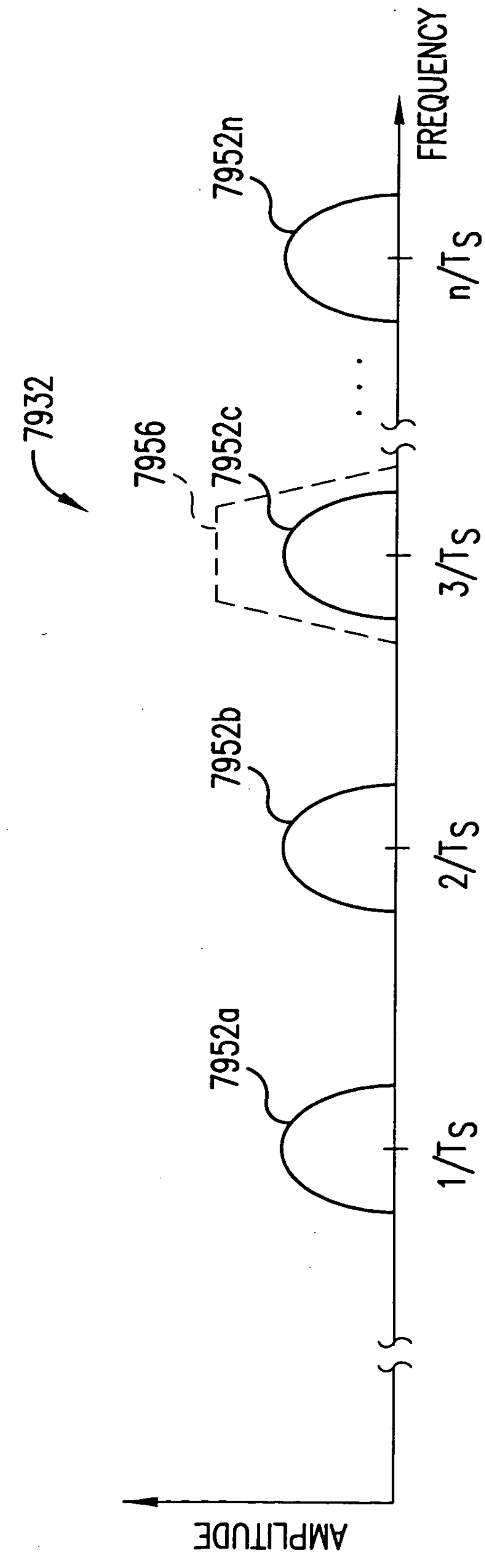

FIG.79C

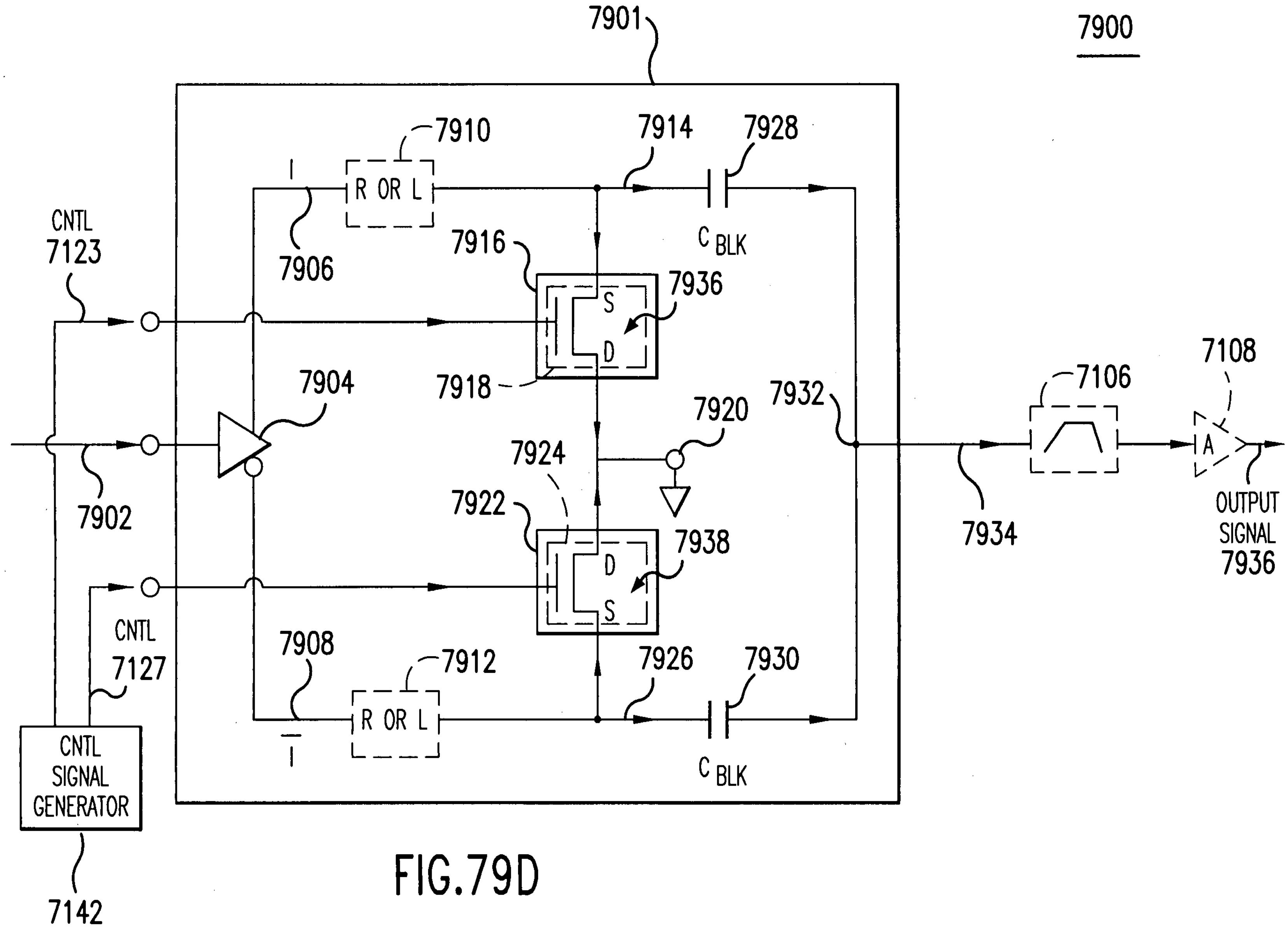

FIG.79D

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Inventors: Sorrells et al.
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Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

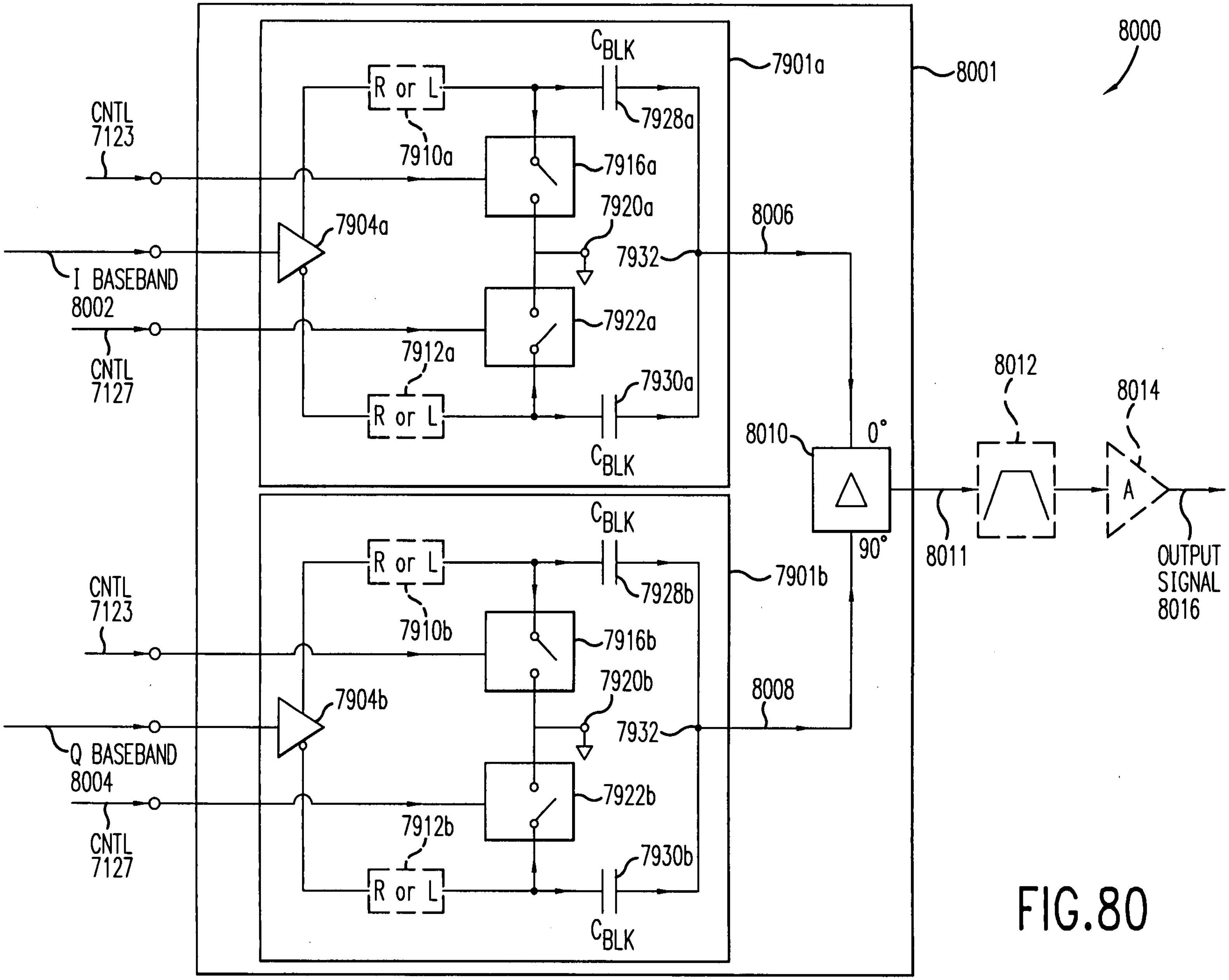

FIG.80

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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

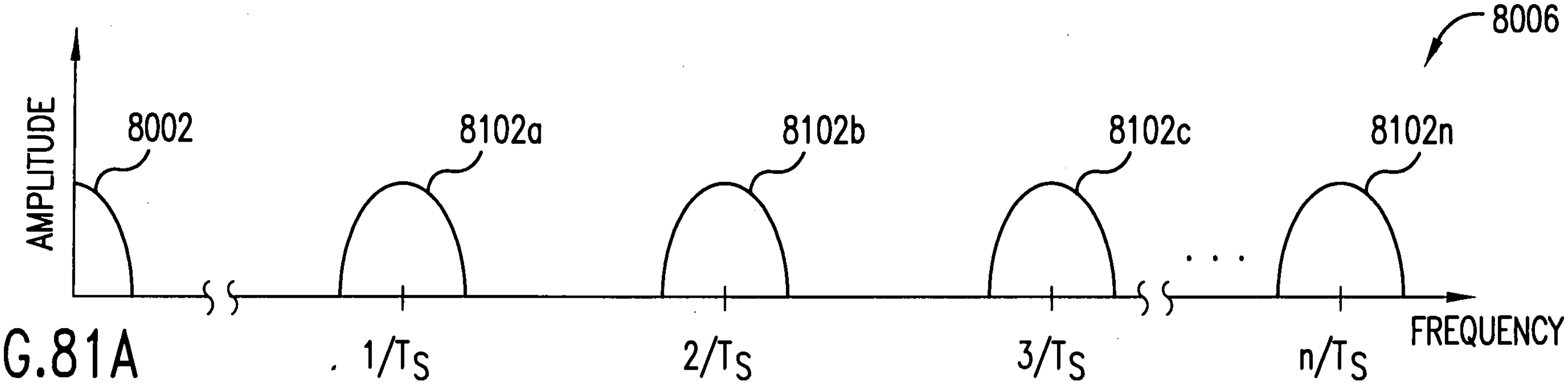

FIG.81A

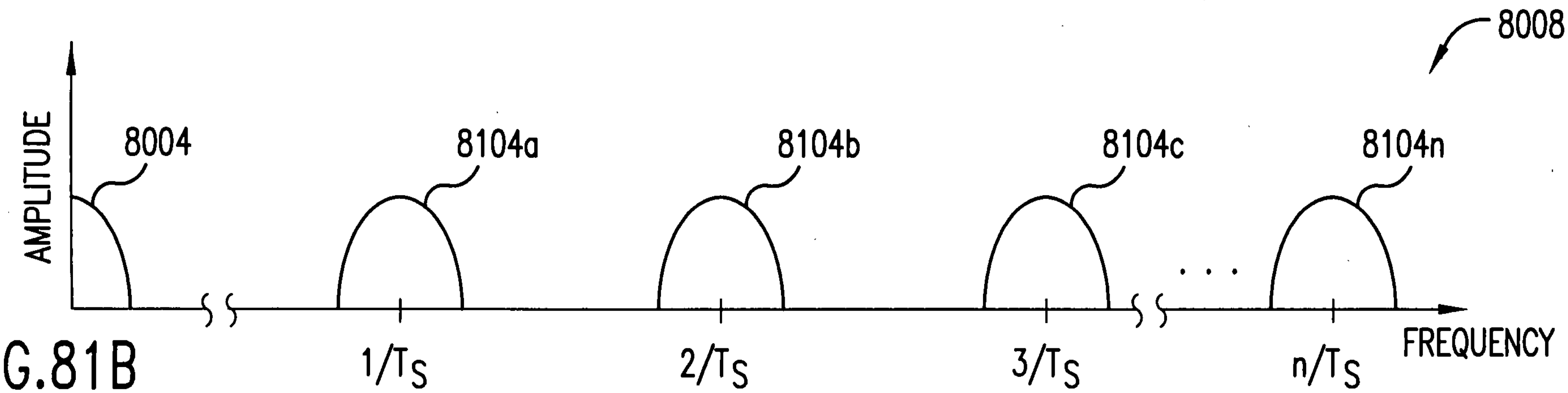

FIG.81B

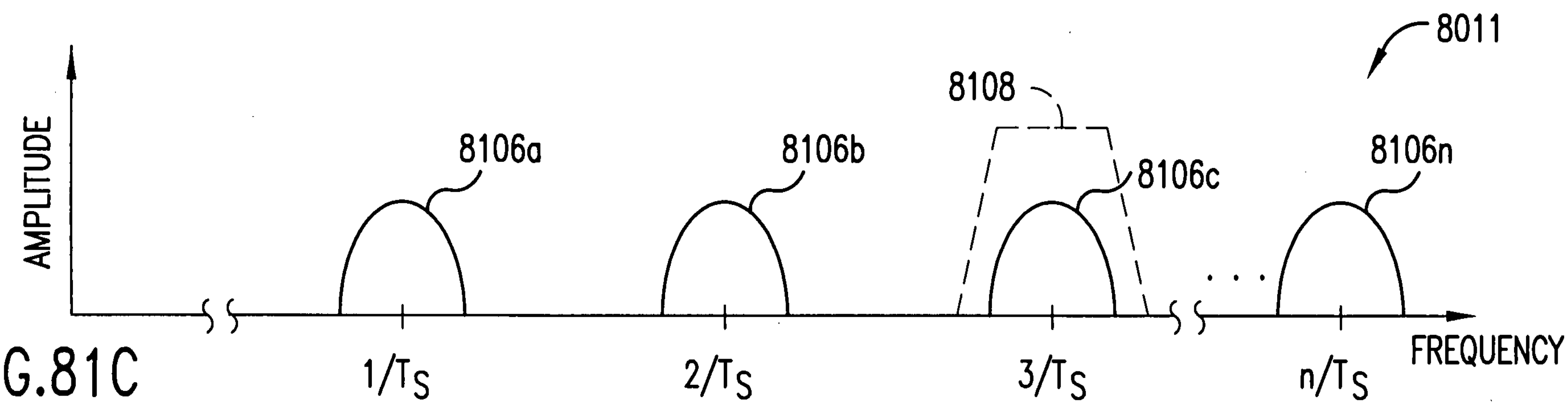

FIG.81C

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Inventors: Sorrells et al.
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For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

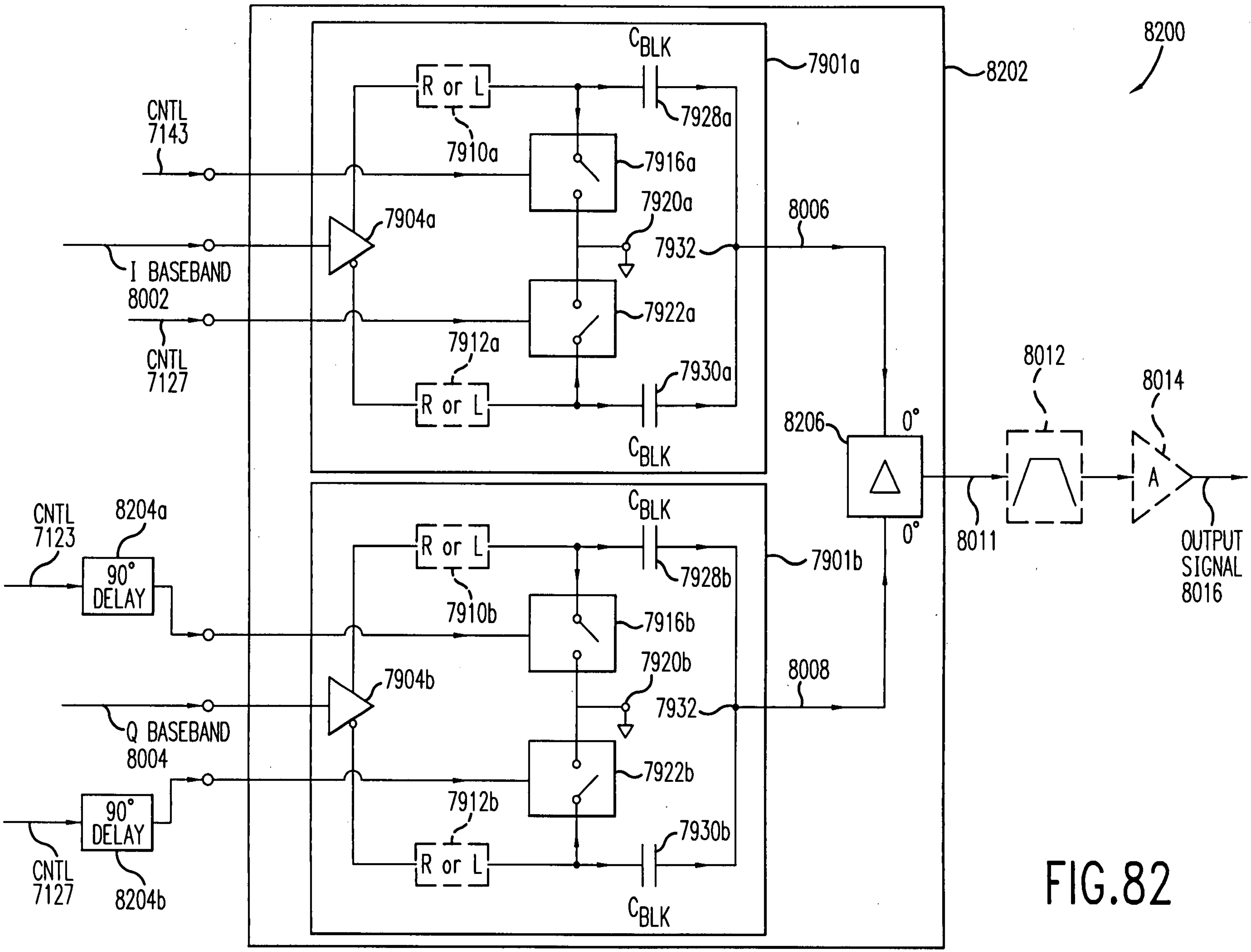

FIG.82

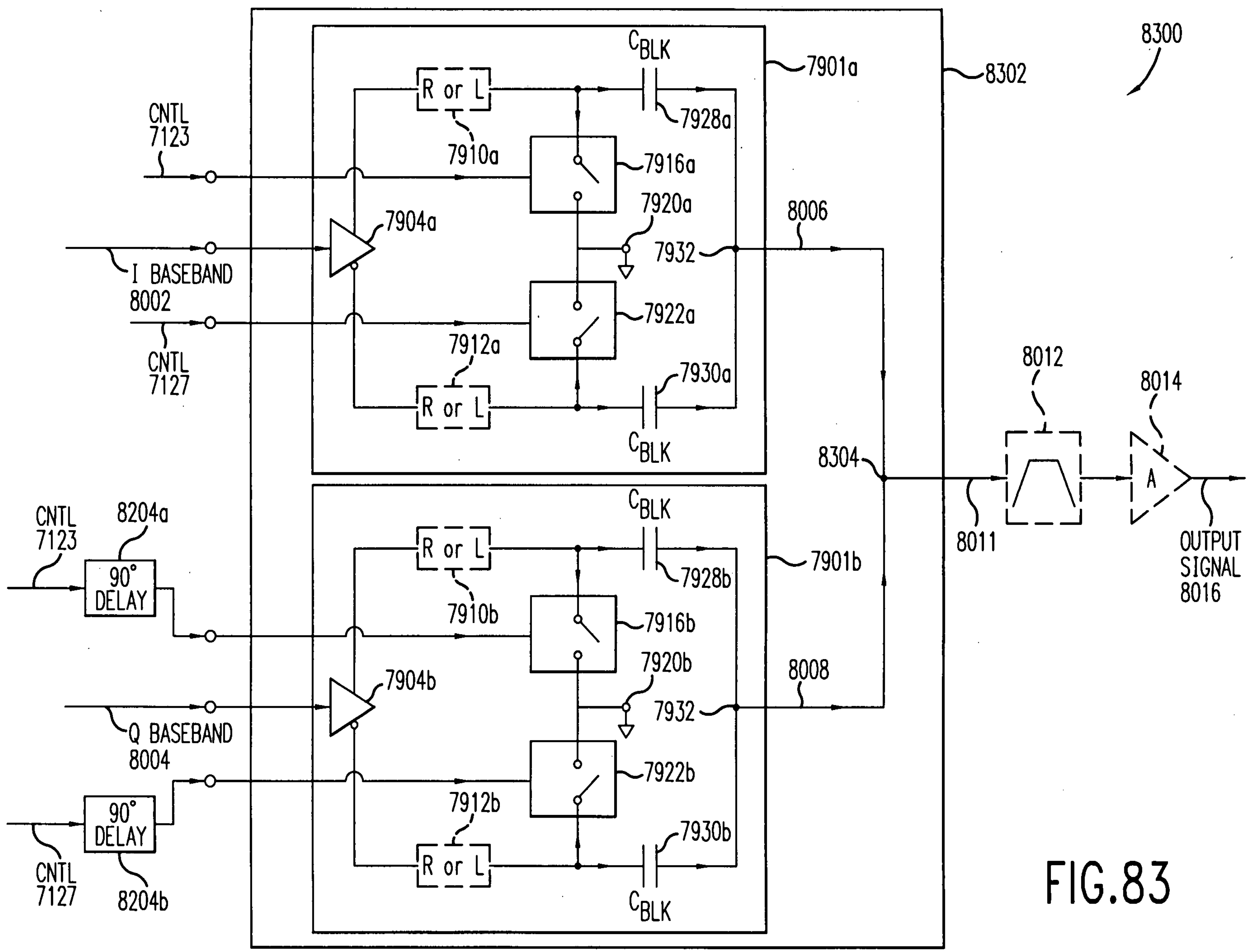

FIG.83

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Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

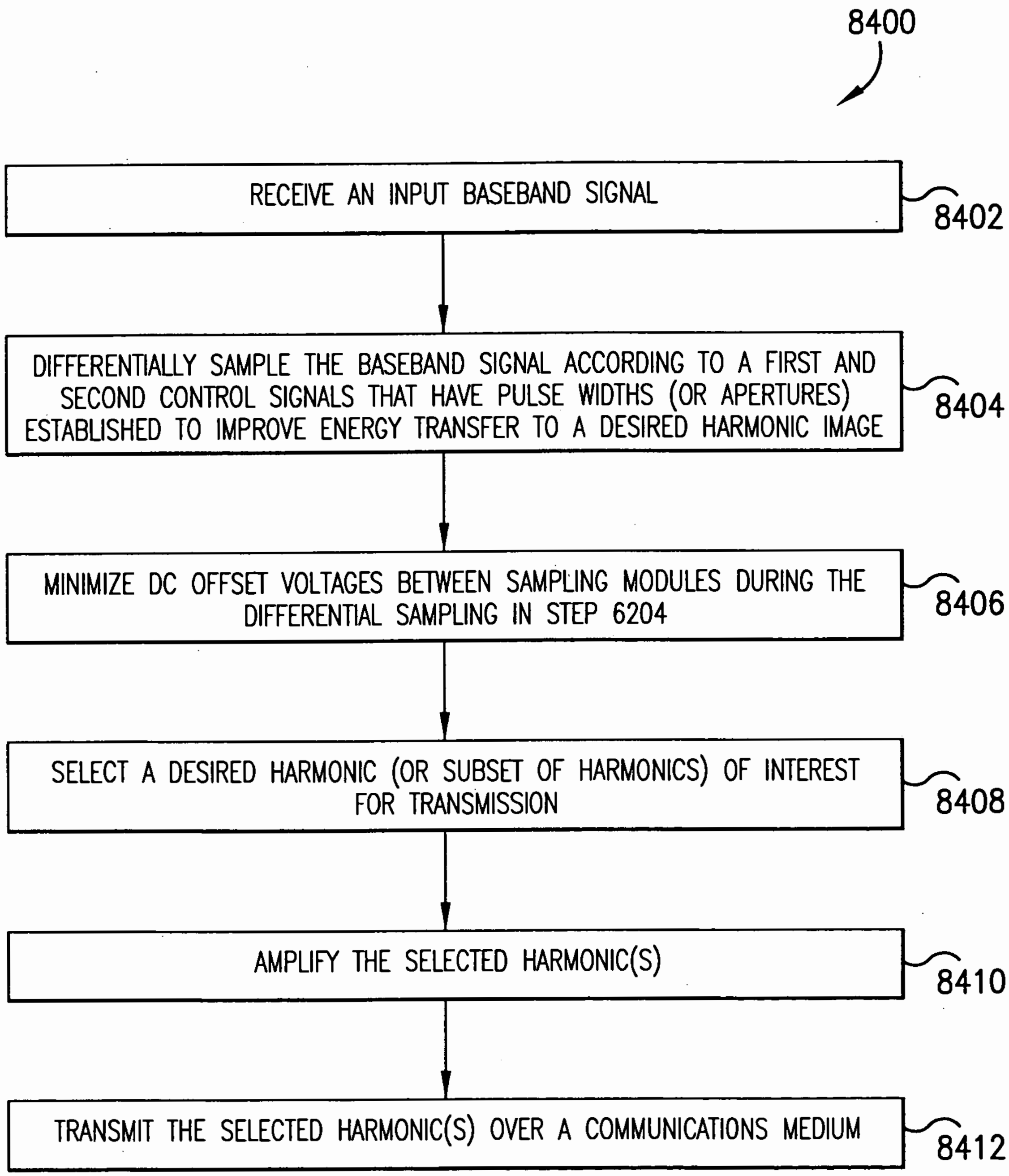
8400
RECEIVE AN INPUT BASEBAND SIGNAL
8402
DIFFERENTIALLY SAMPLE THE BASEBAND SIGNAL ACCORDING TO A FIRST AND SECOND CONTROL SIGNALS THAT HAVE PULSE WIDTHS (OR APERTURES) ESTABLISHED TO IMPROVE ENERGY TRANSFER TO A DESIRED HARMONIC IMAGE
8404
MINIMIZE DC OFFSET VOLTAGES BETWEEN SAMPLING MODULES DURING THE DIFFERENTIAL SAMPLING IN STEP 6204
8406
SELECT A DESIRED HARMONIC (OR SUBSET OF HARMONICS) OF INTEREST FOR TRANSMISSION
8408
AMPLIFY THE SELECTED HARMONIC(S)
8410
TRANSMIT THE SELECTED HARMONIC(S) OVER A COMMUNICATIONS MEDIUM
8412

FIG.84

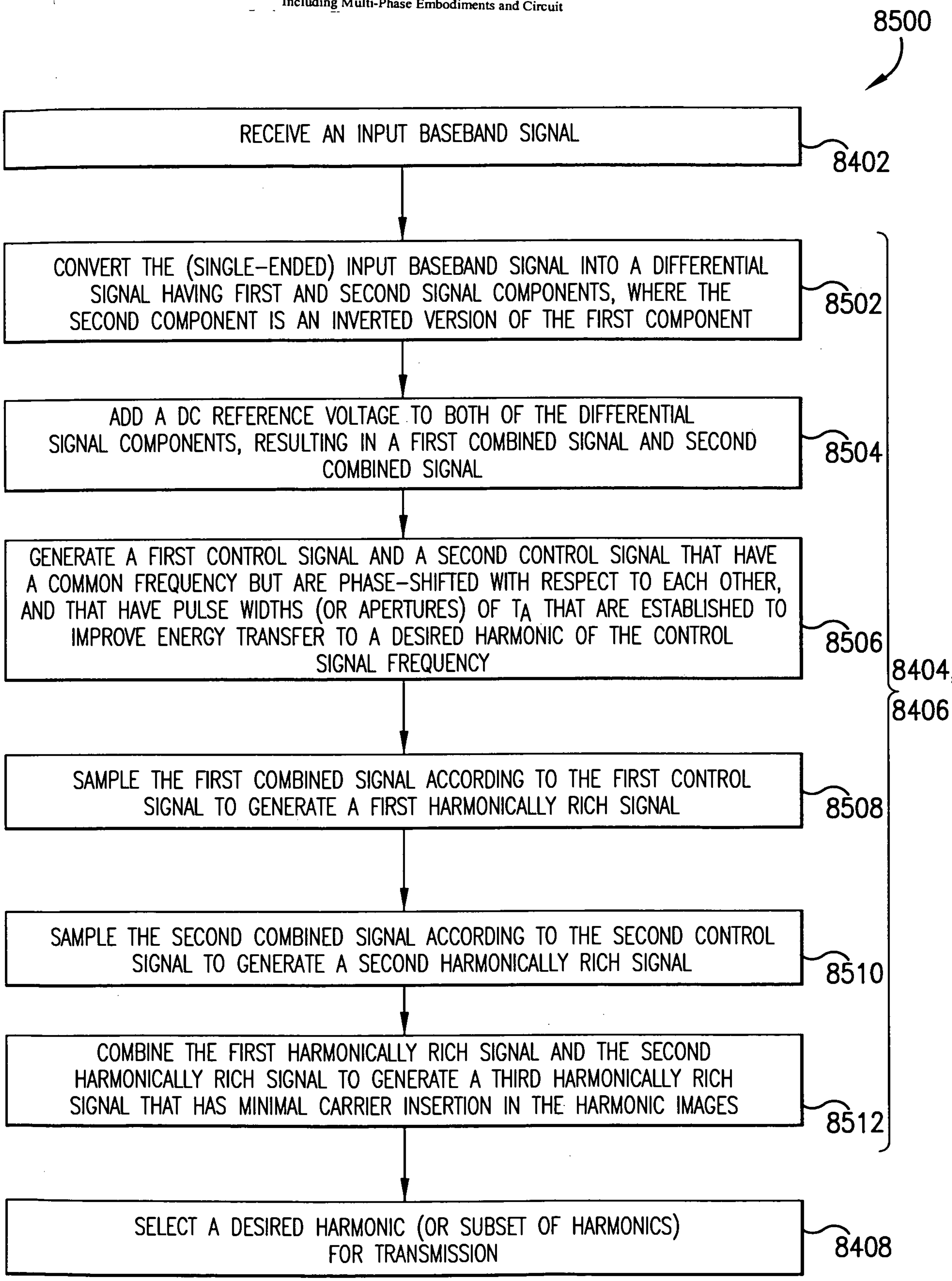
8500
RECEIVE AN INPUT BASEBAND SIGNAL
8402
CONVERT THE (SINGLE-ENDED) INPUT BASEBAND SIGNAL INTO A DIFFERENTIAL SIGNAL HAVING FIRST AND SECOND SIGNAL COMPONENTS, WHERE THE SECOND COMPONENT IS AN INVERTED VERSION OF THE FIRST COMPONENT
8502
ADD A DC REFERENCE VOLTAGE TO BOTH OF THE DIFFERENTIAL SIGNAL COMPONENTS, RESULTING IN A FIRST COMBINED SIGNAL AND SECOND COMBINED SIGNAL
8504
GENERATE A FIRST CONTROL SIGNAL AND A SECOND CONTROL SIGNAL THAT HAVE A COMMON FREQUENCY BUT ARE PHASE-SHIFTED WITH RESPECT TO EACH OTHER, AND THAT HAVE PULSE WIDTHS (OR APERTURES) OF T_A THAT ARE ESTABLISHED TO IMPROVE ENERGY TRANSFER TO A DESIRED HARMONIC OF THE CONTROL SIGNAL FREQUENCY
8506
8404, 8406
SAMPLE THE FIRST COMBINED SIGNAL ACCORDING TO THE FIRST CONTROL SIGNAL TO GENERATE A FIRST HARMONICALLY RICH SIGNAL
8508
SAMPLE THE SECOND COMBINED SIGNAL ACCORDING TO THE SECOND CONTROL SIGNAL TO GENERATE A SECOND HARMONICALLY RICH SIGNAL
8510
COMBINE THE FIRST HARMONICALLY RICH SIGNAL AND THE SECOND HARMONICALLY RICH SIGNAL TO GENERATE A THIRD HARMONICALLY RICH SIGNAL THAT HAS MINIMAL CARRIER INSERTION IN THE HARMONIC IMAGES
8512
SELECT A DESIRED HARMONIC (OR SUBSET OF HARMONICS) FOR TRANSMISSION
8408

FIG.85

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For: Wireless Local Area Network (WLAN) Using
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Including Multi-Phase Embodiments and Circuit

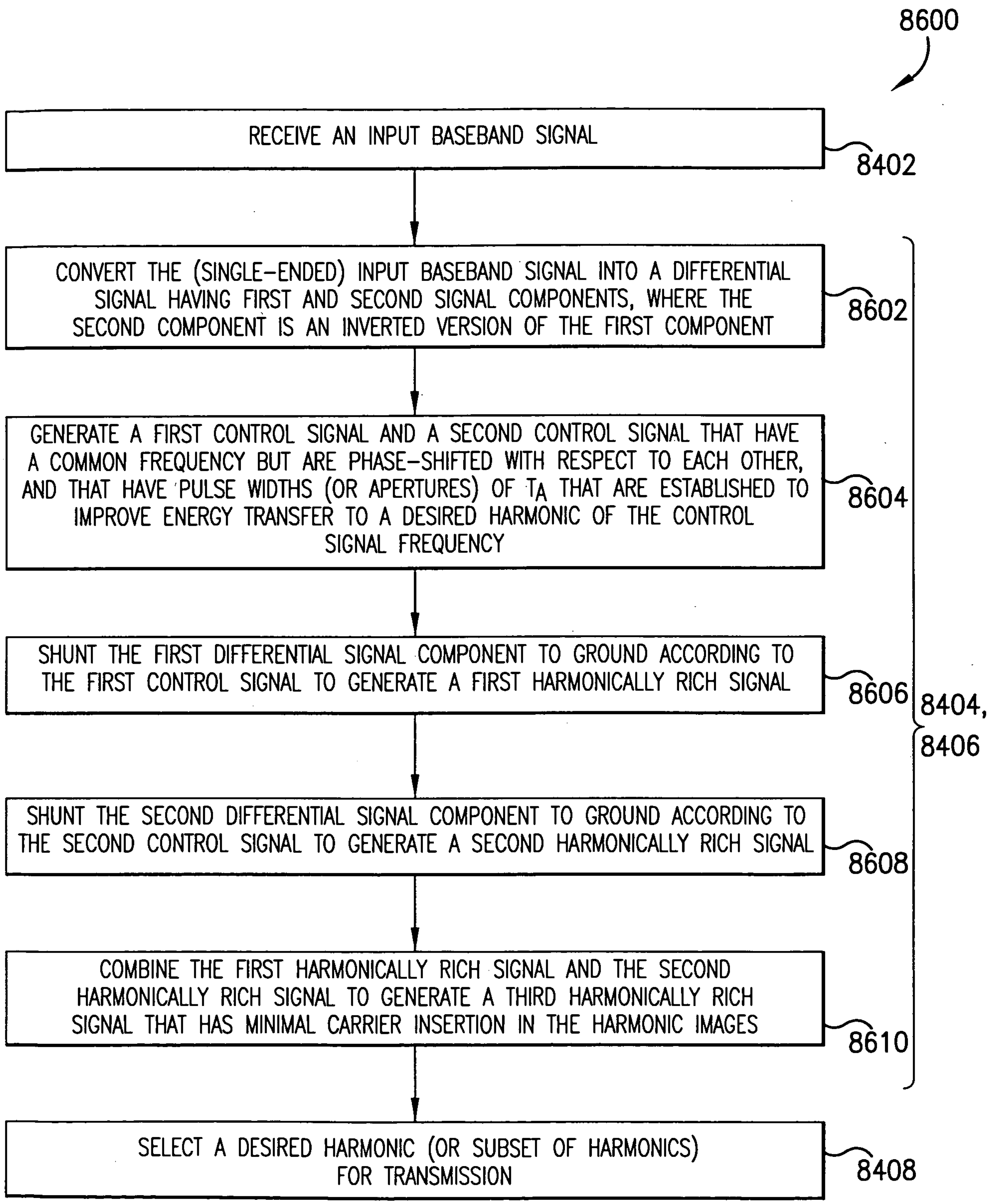


FIG.86

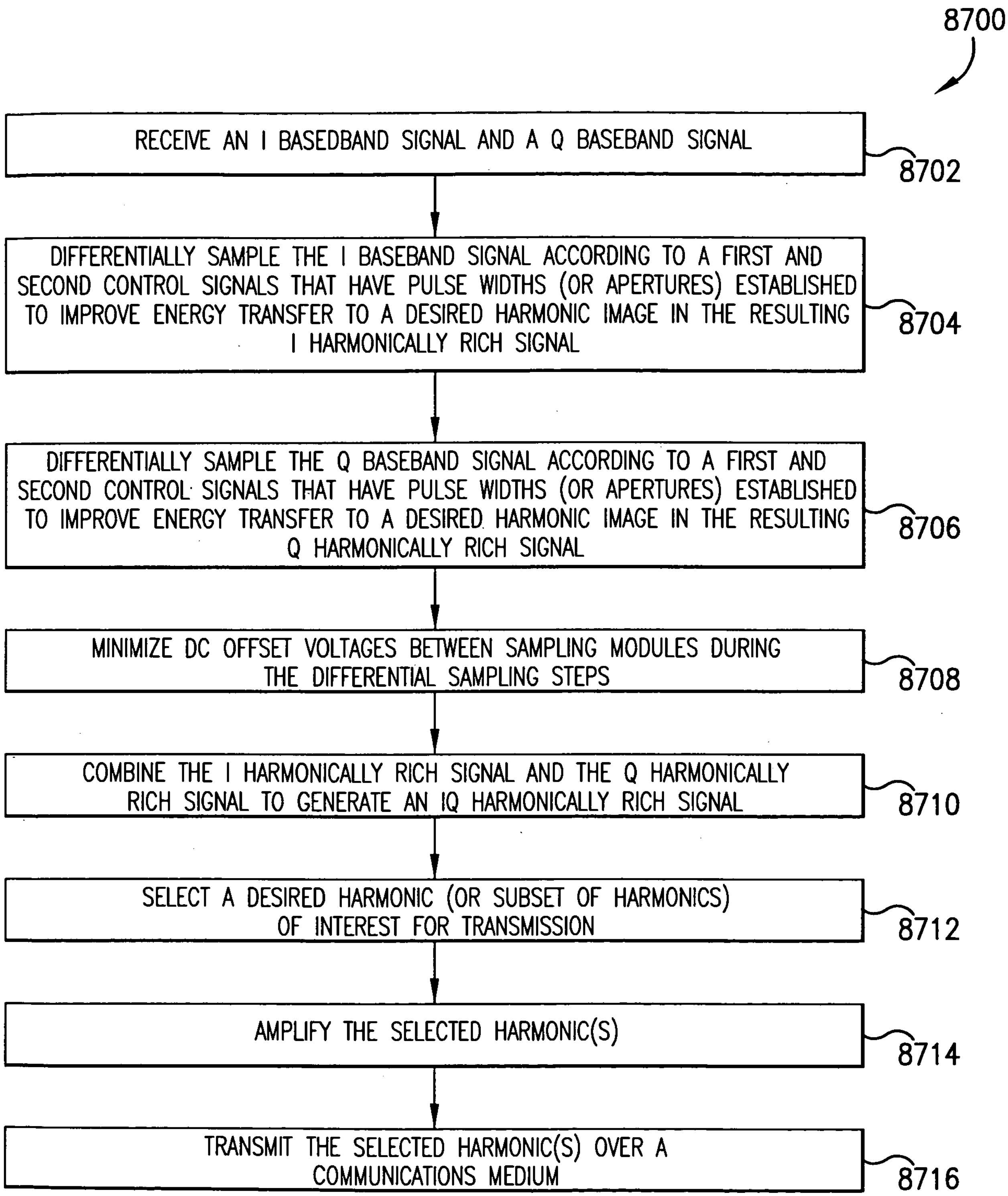

8700
RECEIVE AN I BASEDBAND SIGNAL AND A Q BASEBAND SIGNAL
8702
DIFFERENTIALLY SAMPLE THE I BASEBAND SIGNAL ACCORDING TO A FIRST AND SECOND CONTROL SIGNALS THAT HAVE PULSE WIDTHS (OR APERTURES) ESTABLISHED TO IMPROVE ENERGY TRANSFER TO A DESIRED HARMONIC IMAGE IN THE RESULTING I HARMONICALLY RICH SIGNAL
8704
DIFFERENTIALLY SAMPLE THE Q BASEBAND SIGNAL ACCORDING TO A FIRST AND SECOND CONTROL SIGNALS THAT HAVE PULSE WIDTHS (OR APERTURES) ESTABLISHED TO IMPROVE ENERGY TRANSFER TO A DESIRED HARMONIC IMAGE IN THE RESULTING Q HARMONICALLY RICH SIGNAL
8706
MINIMIZE DC OFFSET VOLTAGES BETWEEN SAMPLING MODULES DURING THE DIFFERENTIAL SAMPLING STEPS
8708
COMBINE THE I HARMONICALLY RICH SIGNAL AND THE Q HARMONICALLY RICH SIGNAL TO GENERATE AN IQ HARMONICALLY RICH SIGNAL
8710
SELECT A DESIRED HARMONIC (OR SUBSET OF HARMONICS) OF INTEREST FOR TRANSMISSION
8712
AMPLIFY THE SELECTED HARMONIC(S)
8714
TRANSMIT THE SELECTED HARMONIC(S) OVER A COMMUNICATIONS MEDIUM
8716

FIG.87

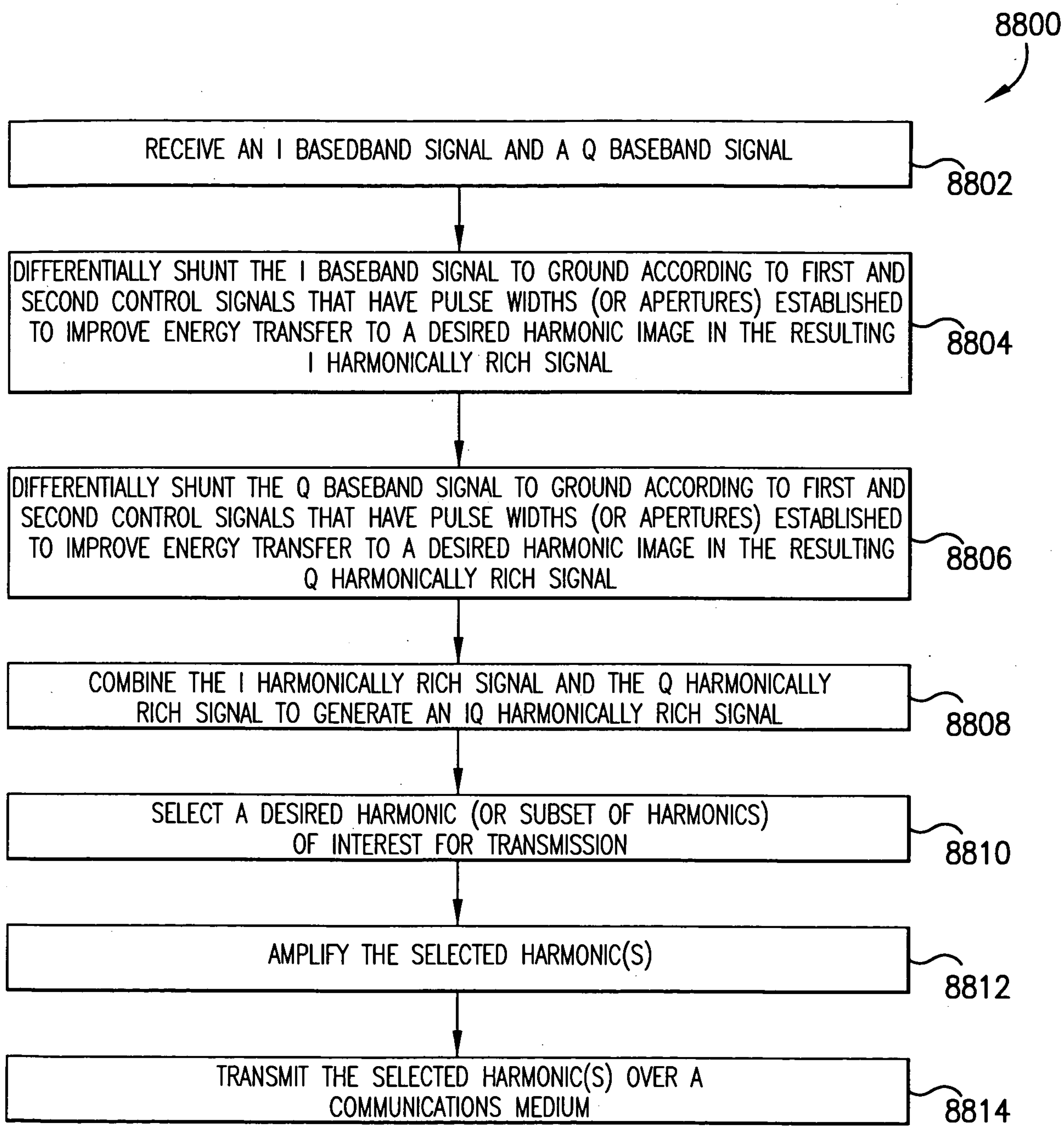

8800
RECEIVE AN I BASEDBAND SIGNAL AND A Q BASEBAND SIGNAL
8802
DIFFERENTIALLY SHUNT THE I BASEBAND SIGNAL TO GROUND ACCORDING TO FIRST AND SECOND CONTROL SIGNALS THAT HAVE PULSE WIDTHS (OR APERTURES) ESTABLISHED TO IMPROVE ENERGY TRANSFER TO A DESIRED HARMONIC IMAGE IN THE RESULTING I HARMONICALLY RICH SIGNAL
8804
DIFFERENTIALLY SHUNT THE Q BASEBAND SIGNAL TO GROUND ACCORDING TO FIRST AND SECOND CONTROL SIGNALS THAT HAVE PULSE WIDTHS (OR APERTURES) ESTABLISHED TO IMPROVE ENERGY TRANSFER TO A DESIRED HARMONIC IMAGE IN THE RESULTING Q HARMONICALLY RICH SIGNAL
8806
COMBINE THE I HARMONICALLY RICH SIGNAL AND THE Q HARMONICALLY RICH SIGNAL TO GENERATE AN IQ HARMONICALLY RICH SIGNAL
8808
SELECT A DESIRED HARMONIC (OR SUBSET OF HARMONICS) OF INTEREST FOR TRANSMISSION
8810
AMPLIFY THE SELECTED HARMONIC(S)
8812
TRANSMIT THE SELECTED HARMONIC(S) OVER A COMMUNICATIONS MEDIUM
8814

FIG.88

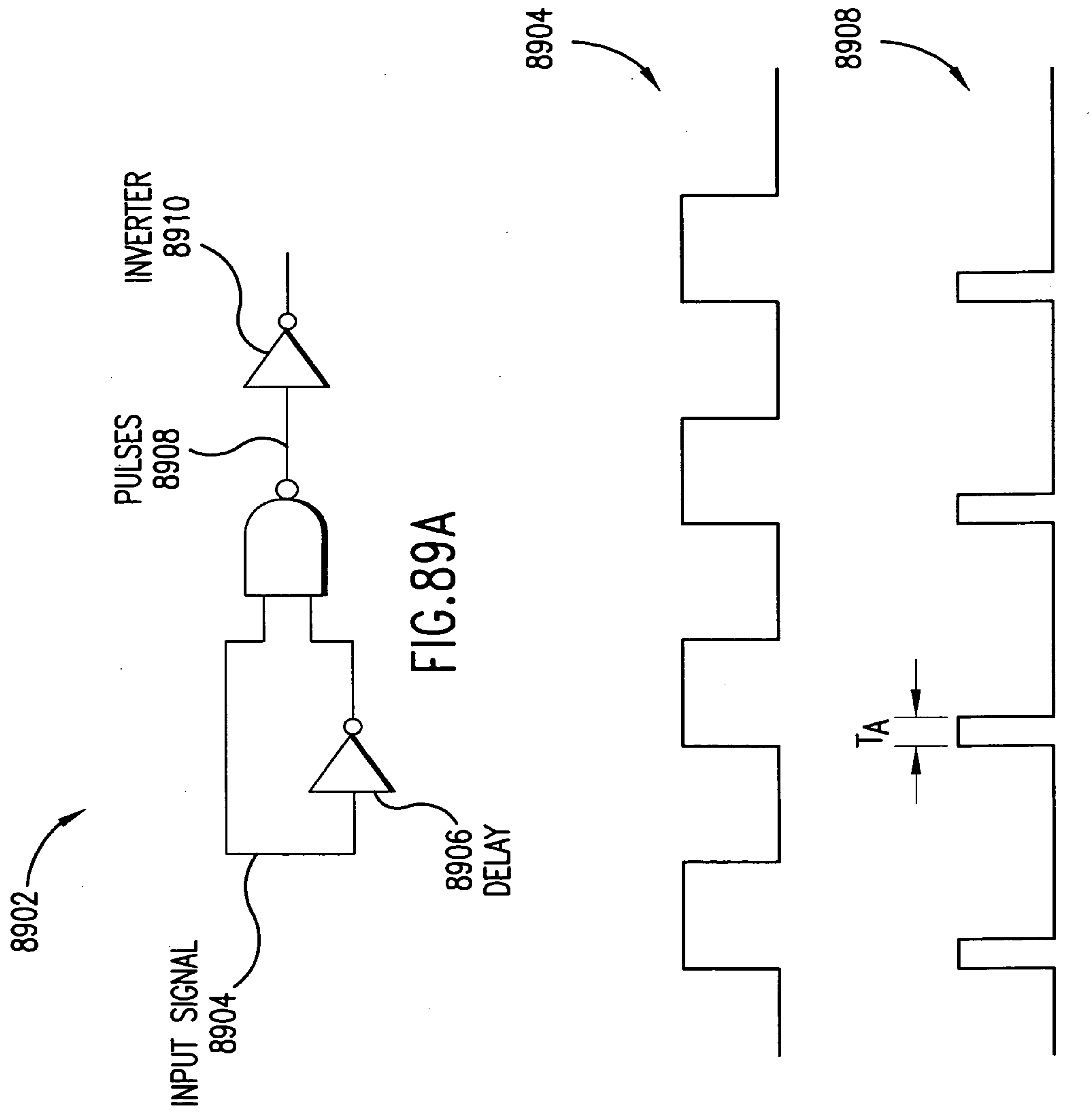
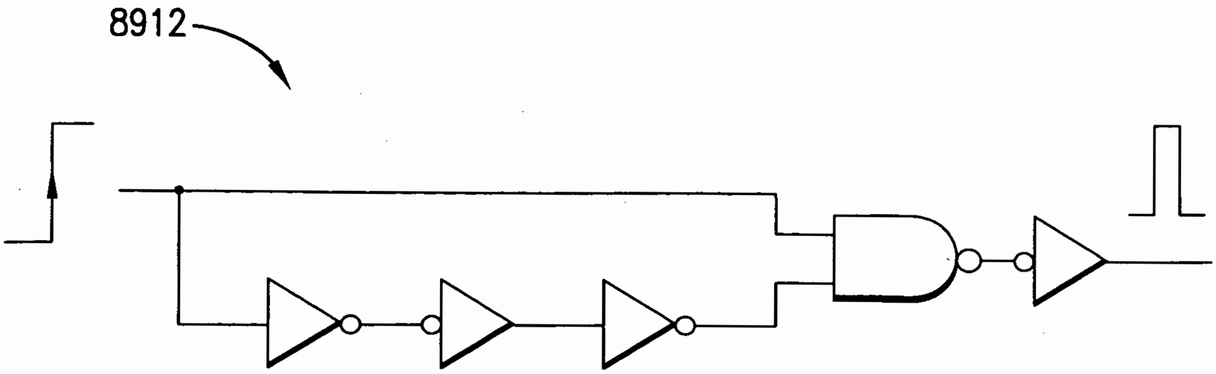


FIG.89A

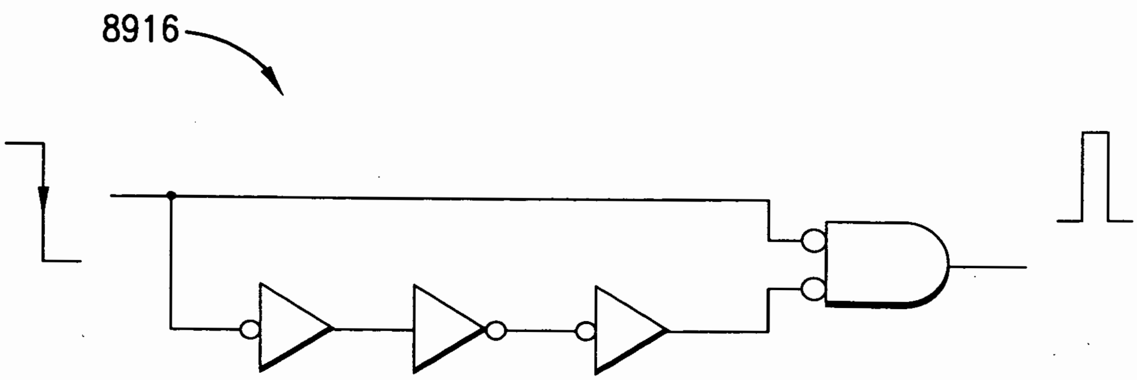
FIG.89B

FIG.89C



RISING EDGE PULSE GENERATOR

FIG.89D



FALLING EDGE PULSE GENERATOR

FIG.89E

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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

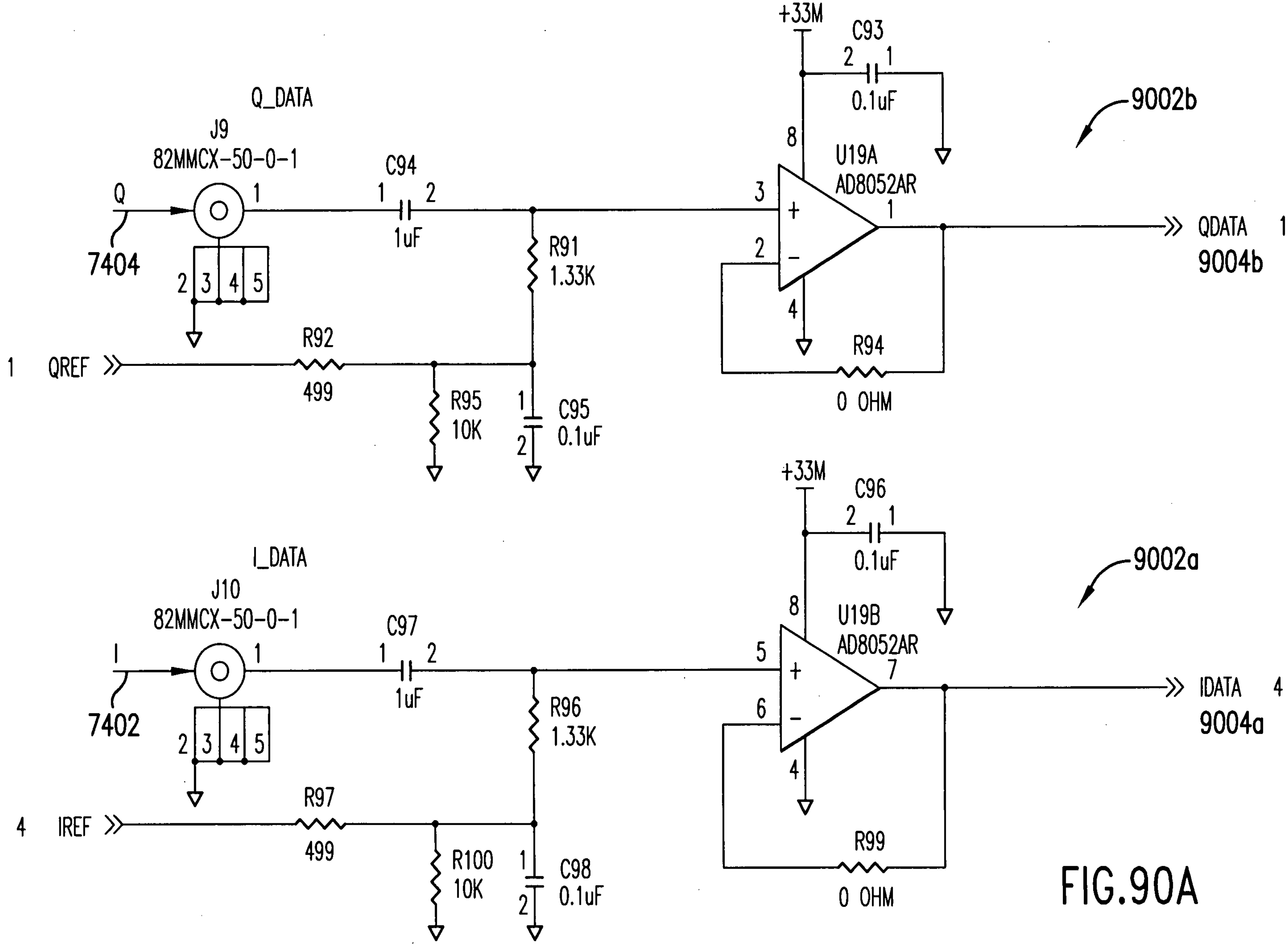

FIG.90A

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Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
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Including Multi-Phase Embodiments and Circuit

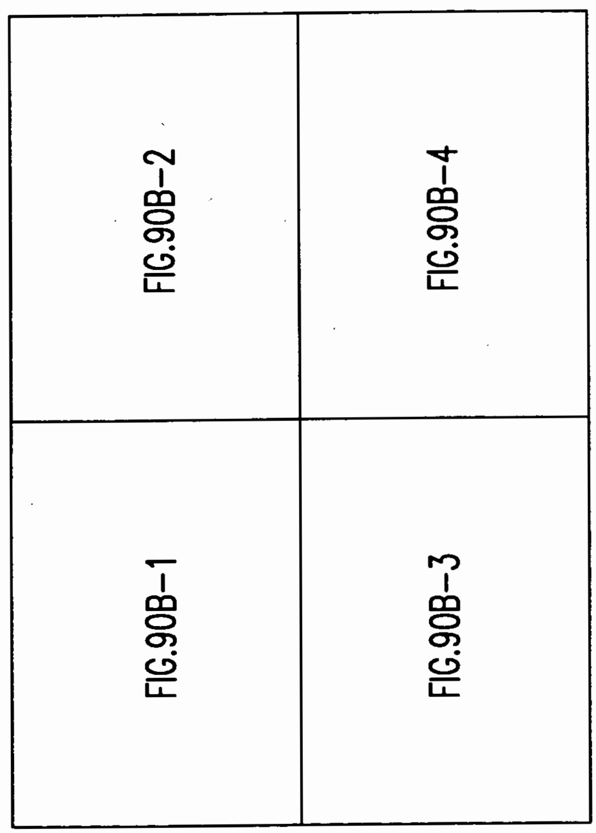

FIG.90B

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Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
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Including Multi-Phase Embodiments and Circuit

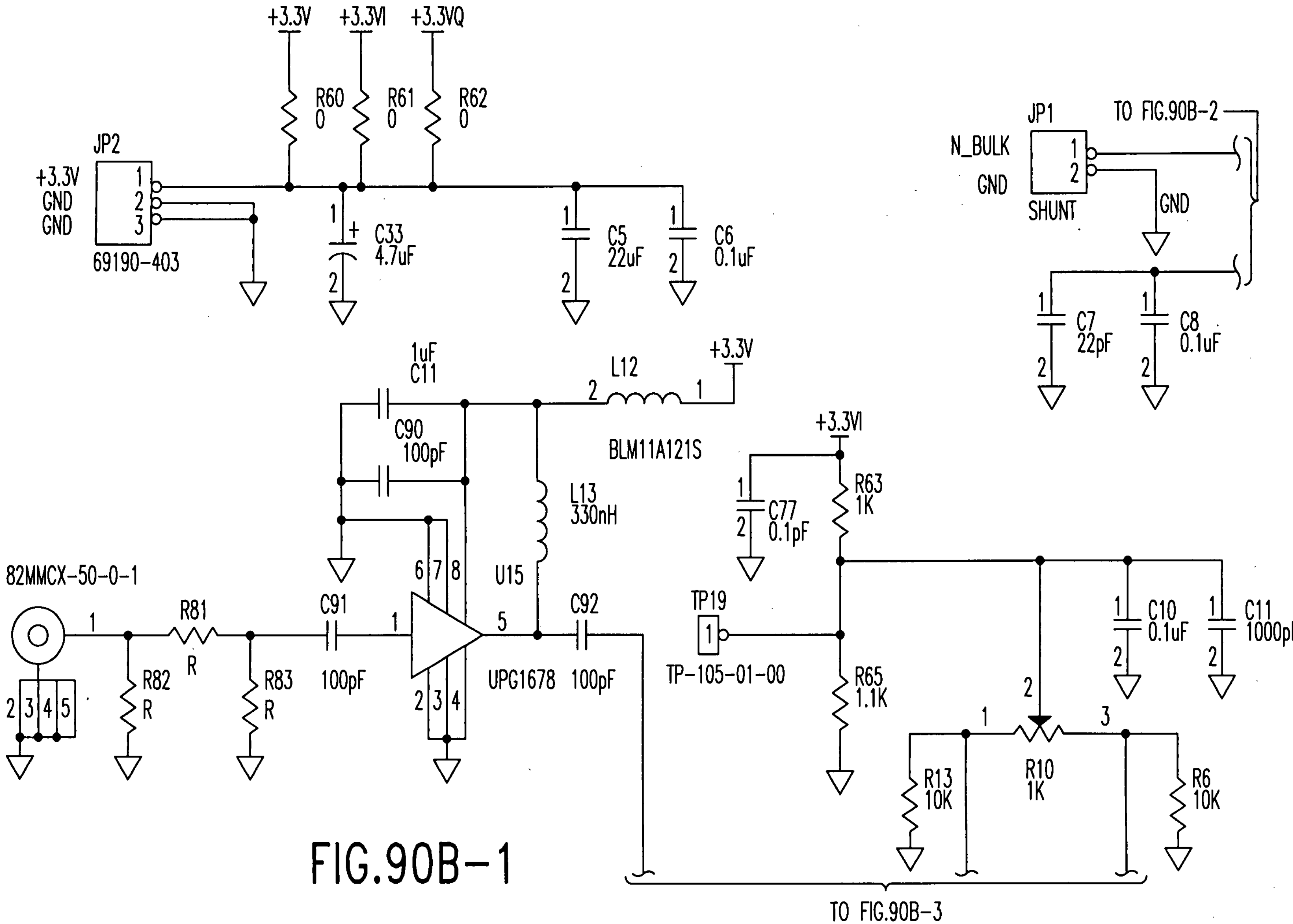

FIG.90B-1

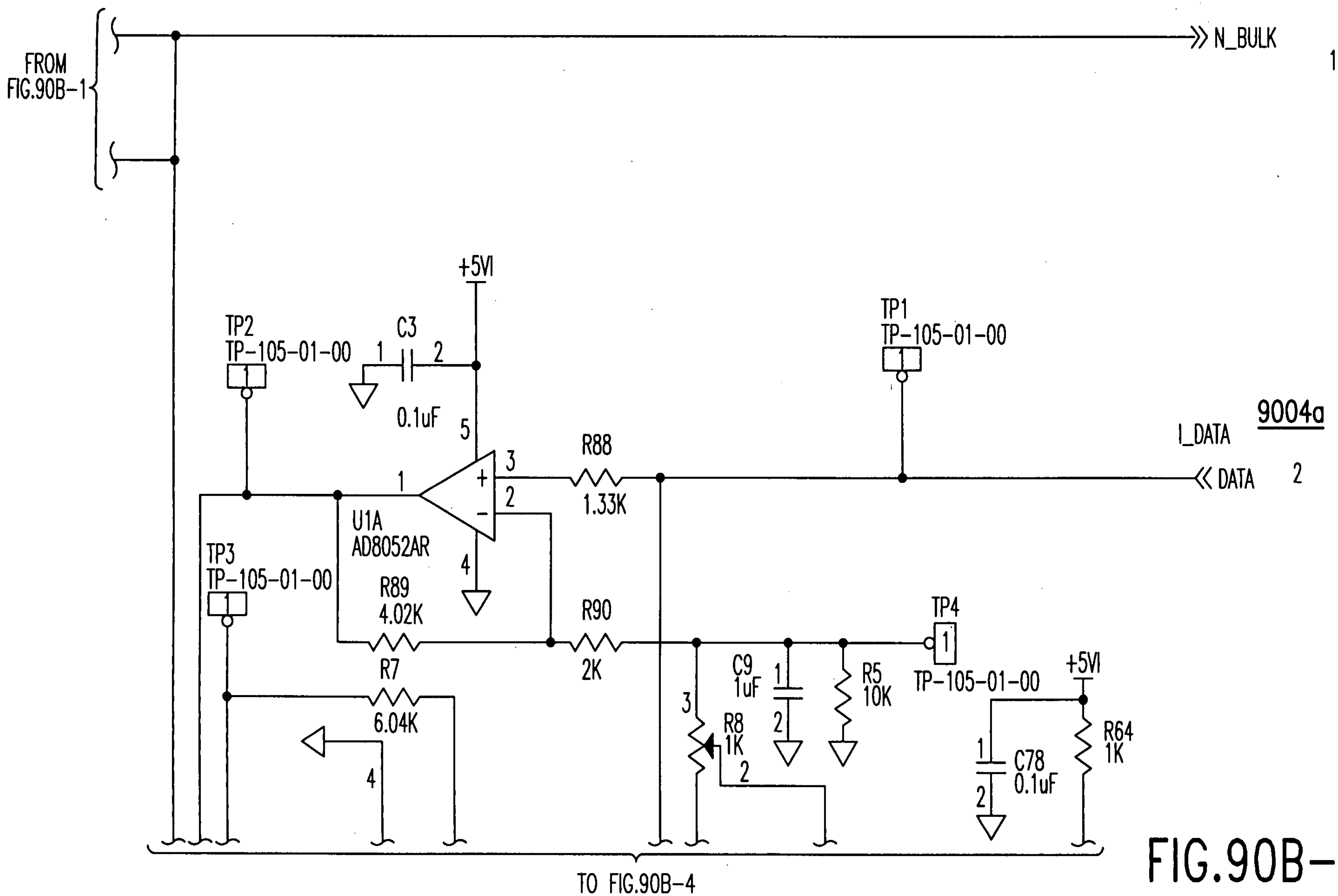

FIG.90B-2

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Inventors: Sorrells et al.
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For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

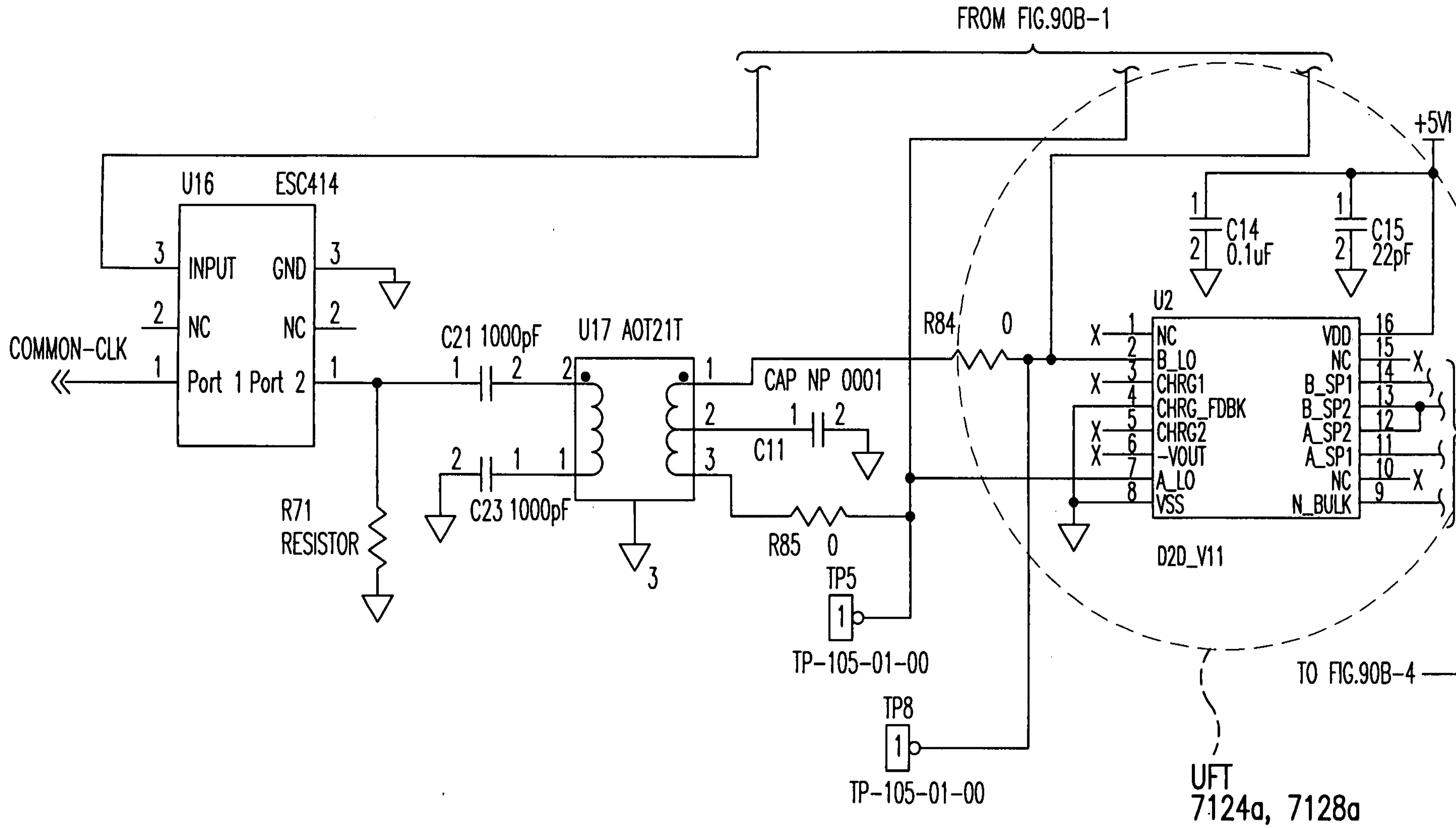
FROM FIG.90B-1
U16 ESC414
INPUT
GND
NC
NC
Port 1 Port 2
COMMON-CLK
R71
RESISTOR
C21 1000pF
C23 1000pF
U17 AOT21T
CAP NP 0001
C11
R84 0
R85 0
TP5
TP-105-01-00
TP8
TP-105-01-00
+5VI
C14
0.1uF
C15
22pF
U2
NC
B_LO
CHRG1
CHRG_FDBK
CHRG2
-VOUT
A_LO
VSS
VDD
NC
B_SP1
B_SP2
A_SP2
A_SP1
NC
N_BULK
D2D_V11
TO FIG.90B-4
UFT
7124a, 7128a

FIG.90B-3

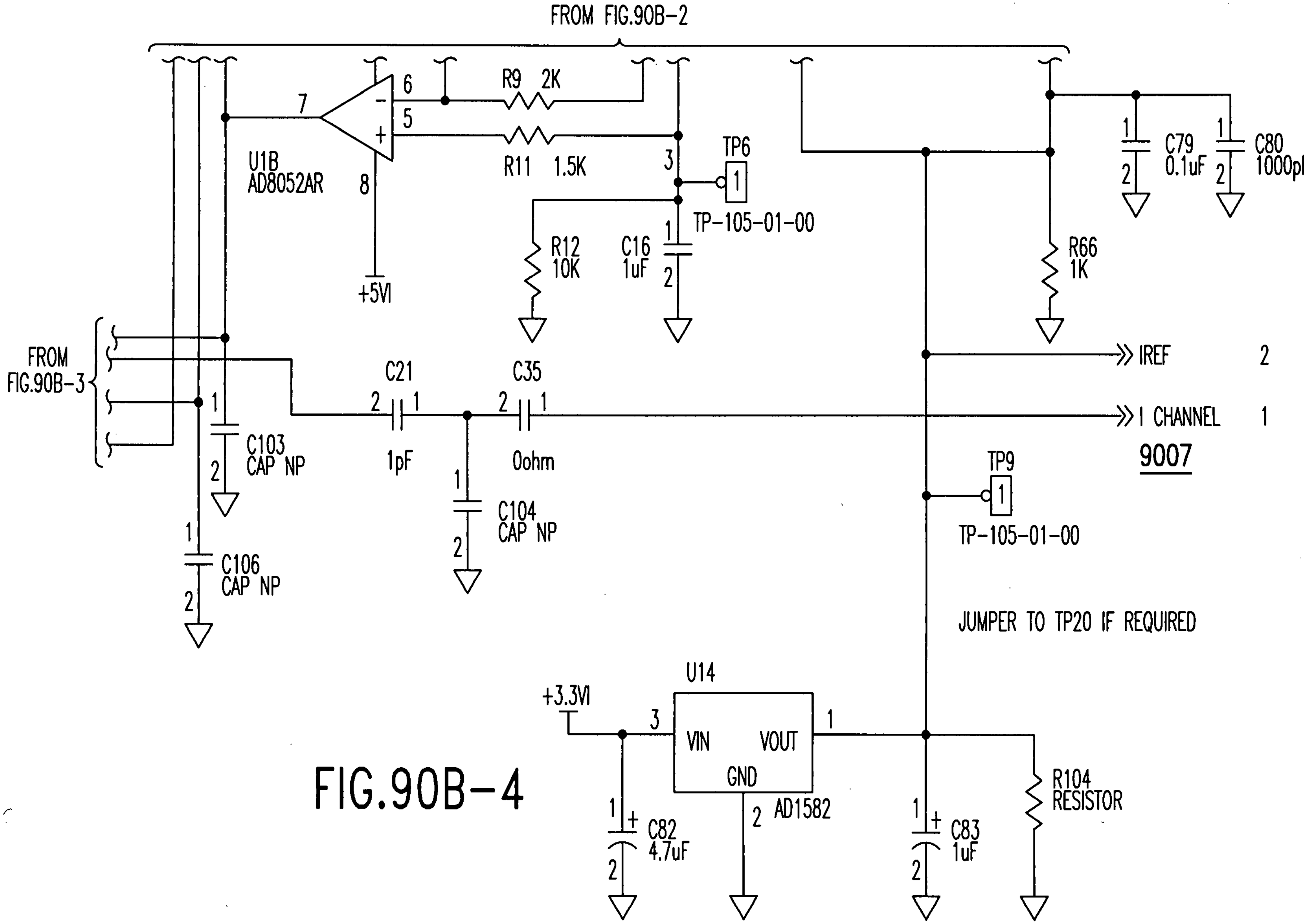

FIG.90B-4

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Sheet 177 of 349
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Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

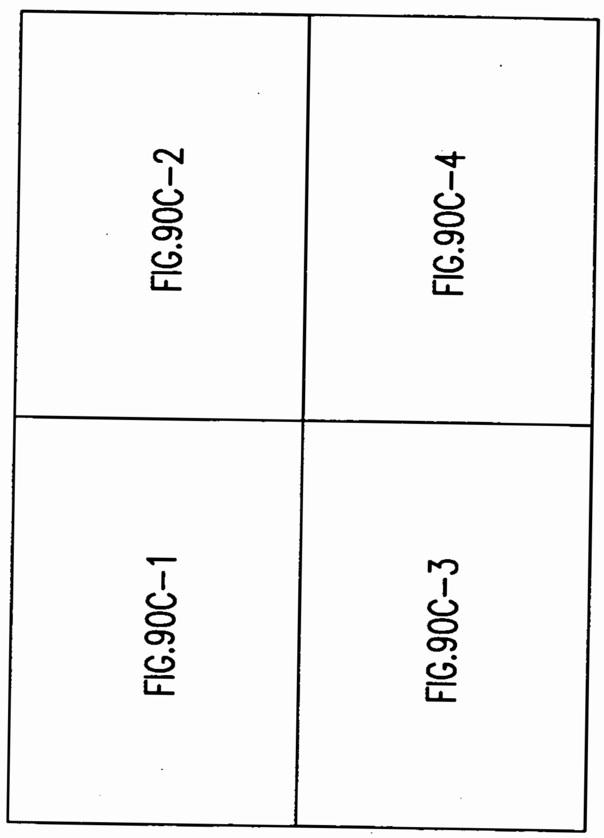

FIG.90C

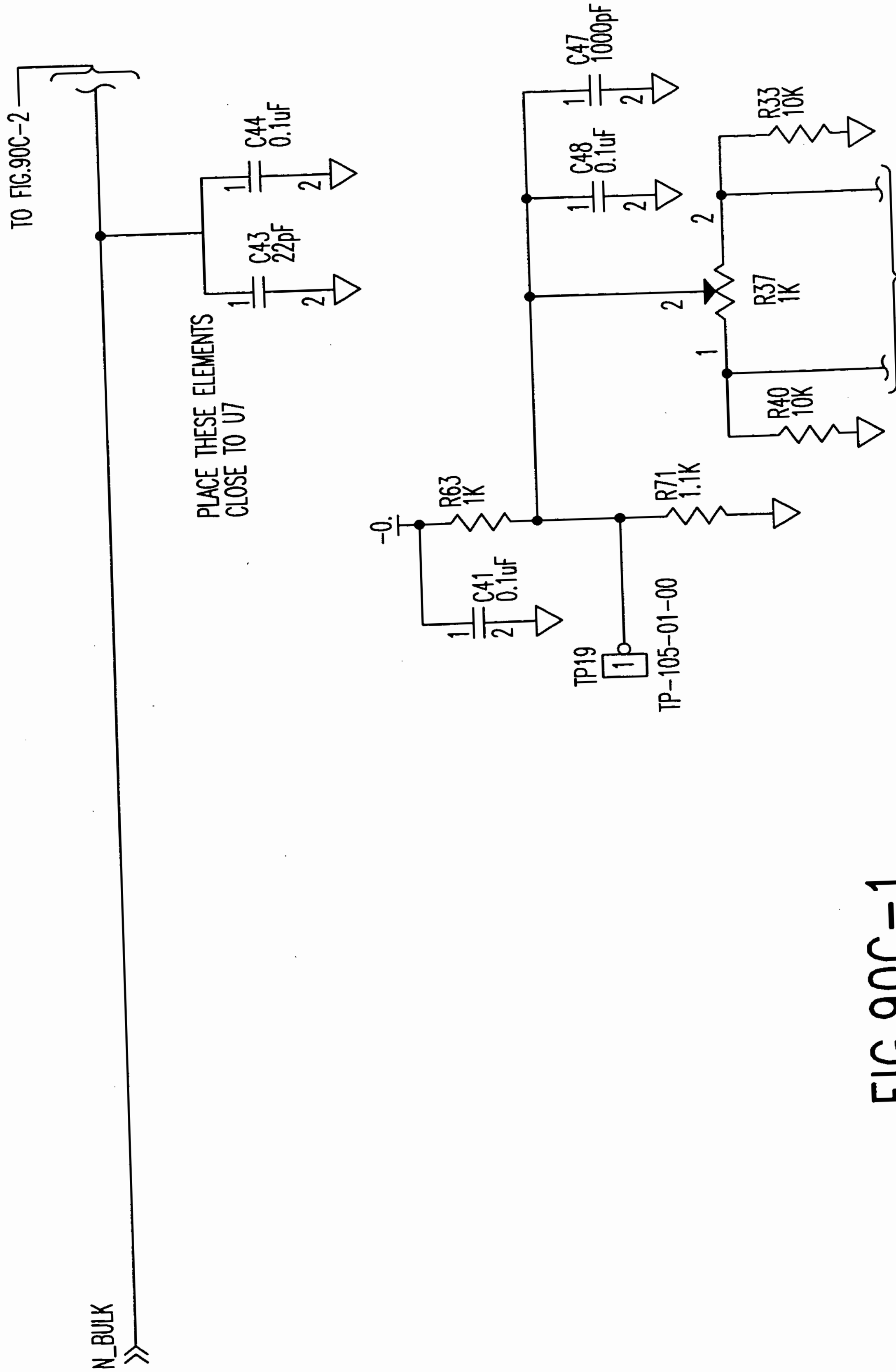
TO FIG.90C-2
C44
0.1uF
C43
22pF
PLACE THESE ELEMENTS
CLOSE TO U7
C47
1000pF
C48
0.1uF
R33
10K
R37
1K
R40
10K
TO FIG.90C-3
R63
1K
R71
1.1K
-0.
C41
0.1uF
TP19
TP-105-01-00
N_BULK

FIG.90C-1

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Including Multi-Phase Embodiments and Circuit

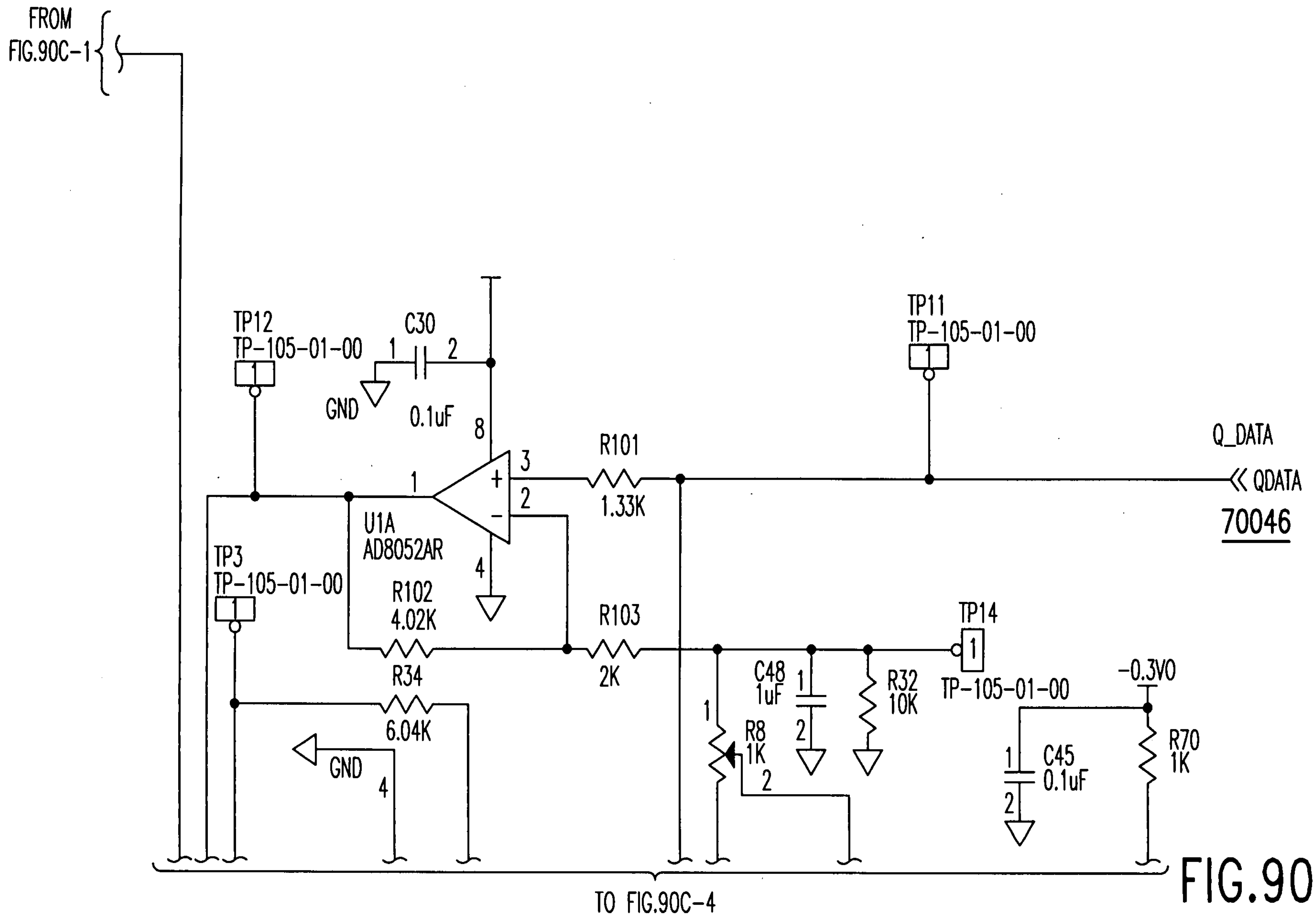

FIG.90C-2

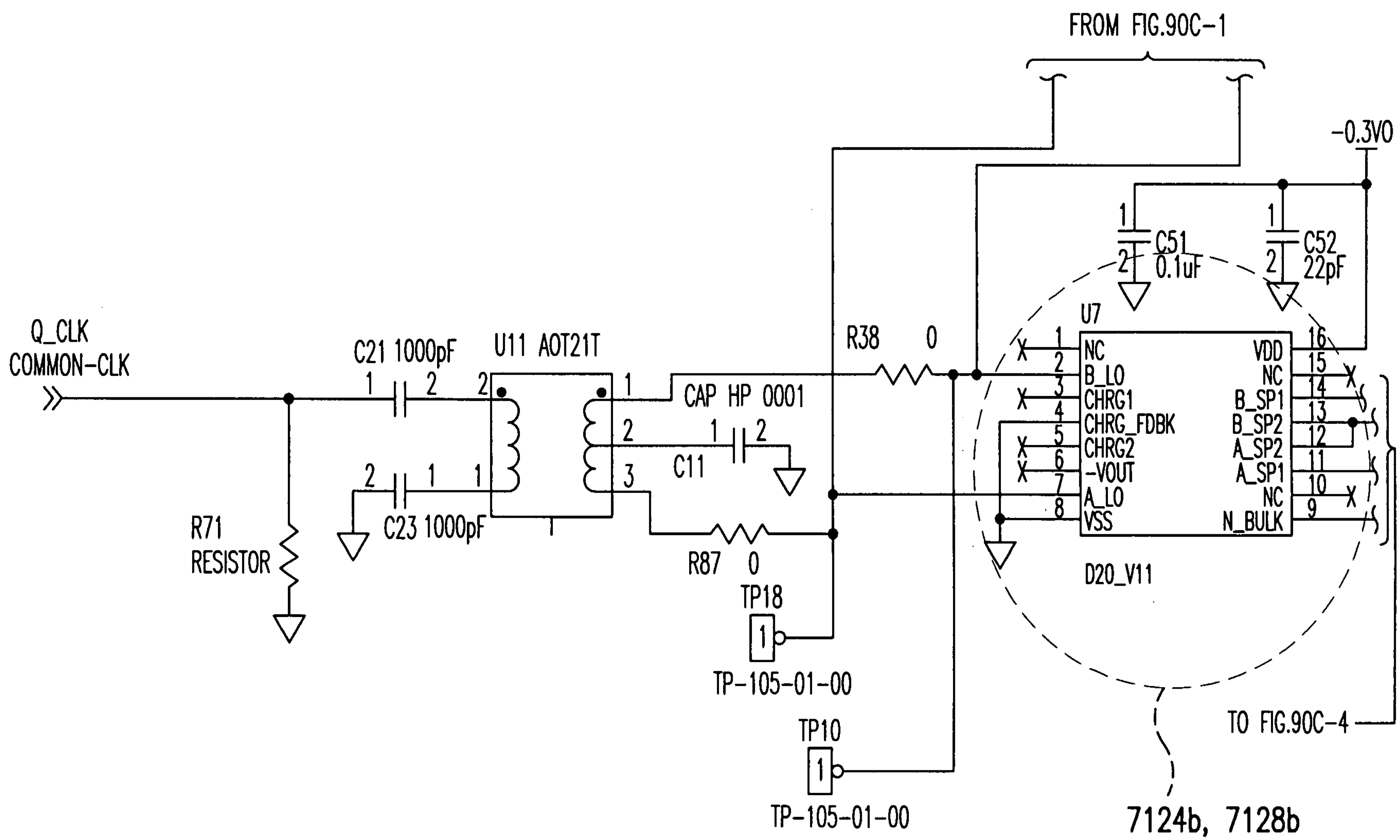
FROM FIG.90C-1
-0.3V0
C51
0.1uF
C52
22pF
U7
Q_CLK
COMMON-CLK
C21 1000pF
U11 AOT21T
R38 0
CAP HP 0001
C11
C23 1000pF
R71
RESISTOR
R87 0
TP18
TP-105-01-00
TP10
TP-105-01-00
NC
B_LO
CHRG1
CHRG_FDBK
CHRG2
-VOUT
A_LO
VSS
VDD
NC
B_SP1
B_SP2
A_SP2
A_SP1
NC
N_BULK
D20_V11
TO FIG.90C-4
7124b, 7128b

FIG.90C-3

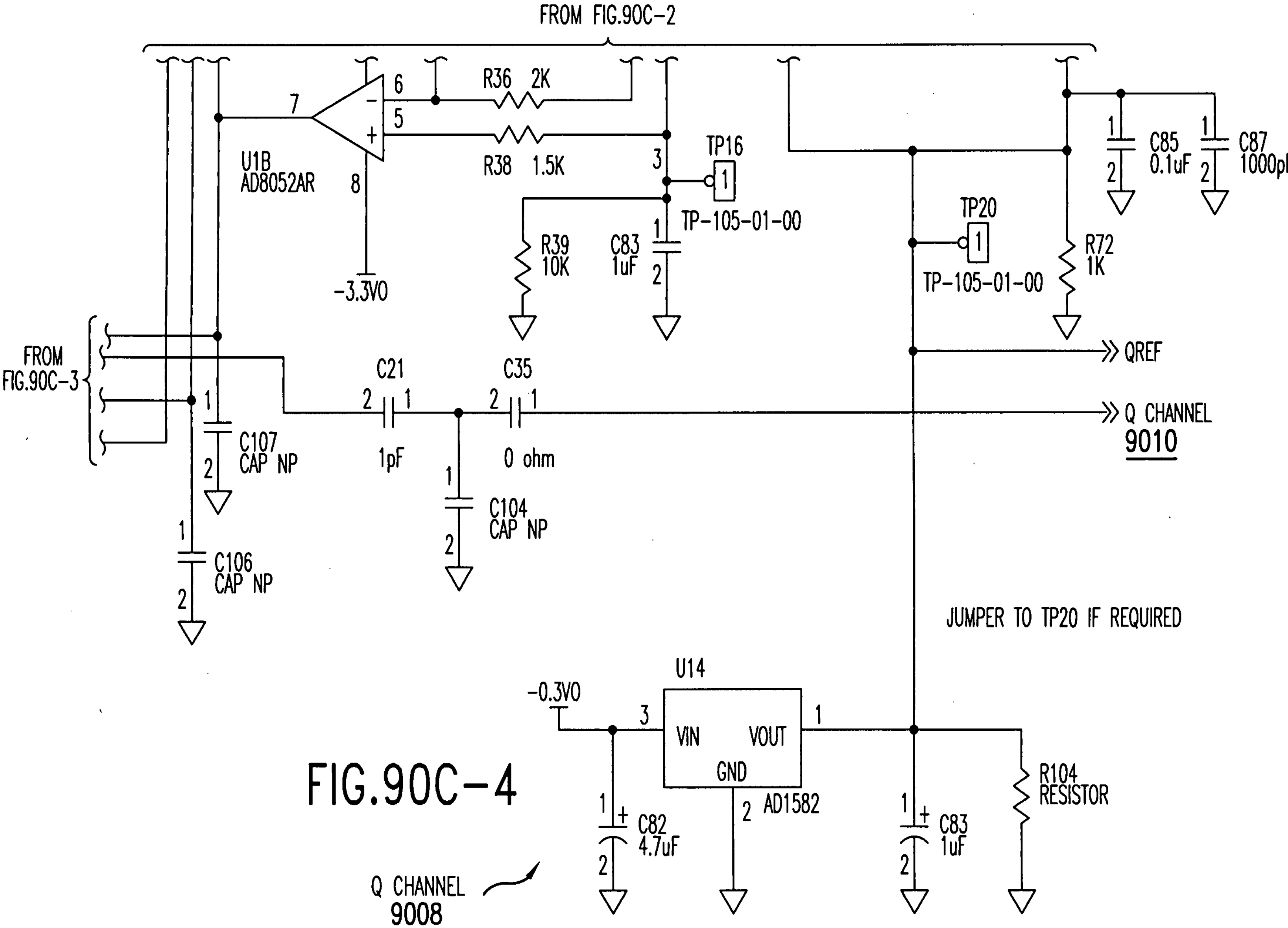

FIG.90C-4

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Inventors: Sorrells et al.
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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

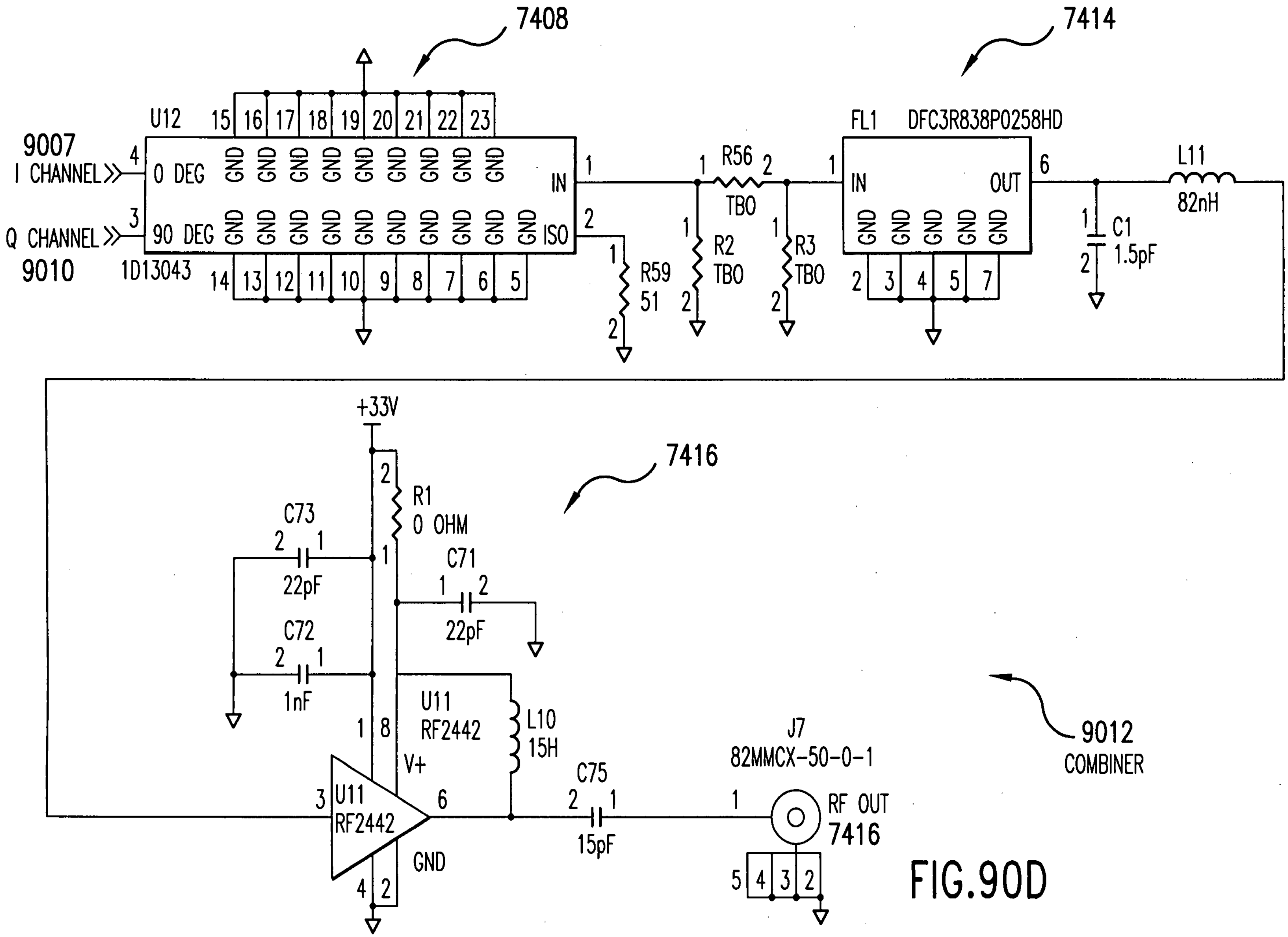

FIG.90D

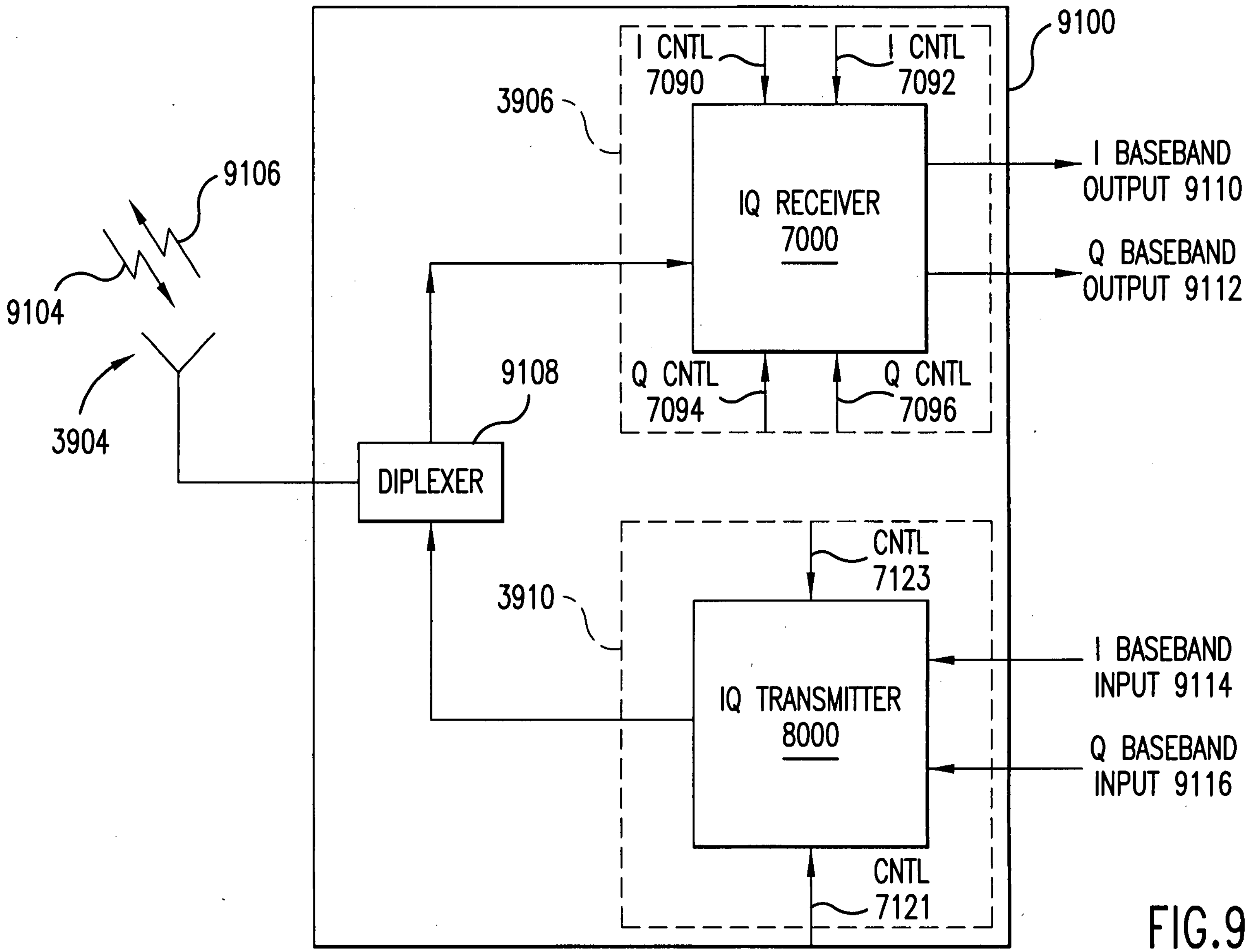

FIG.91

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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
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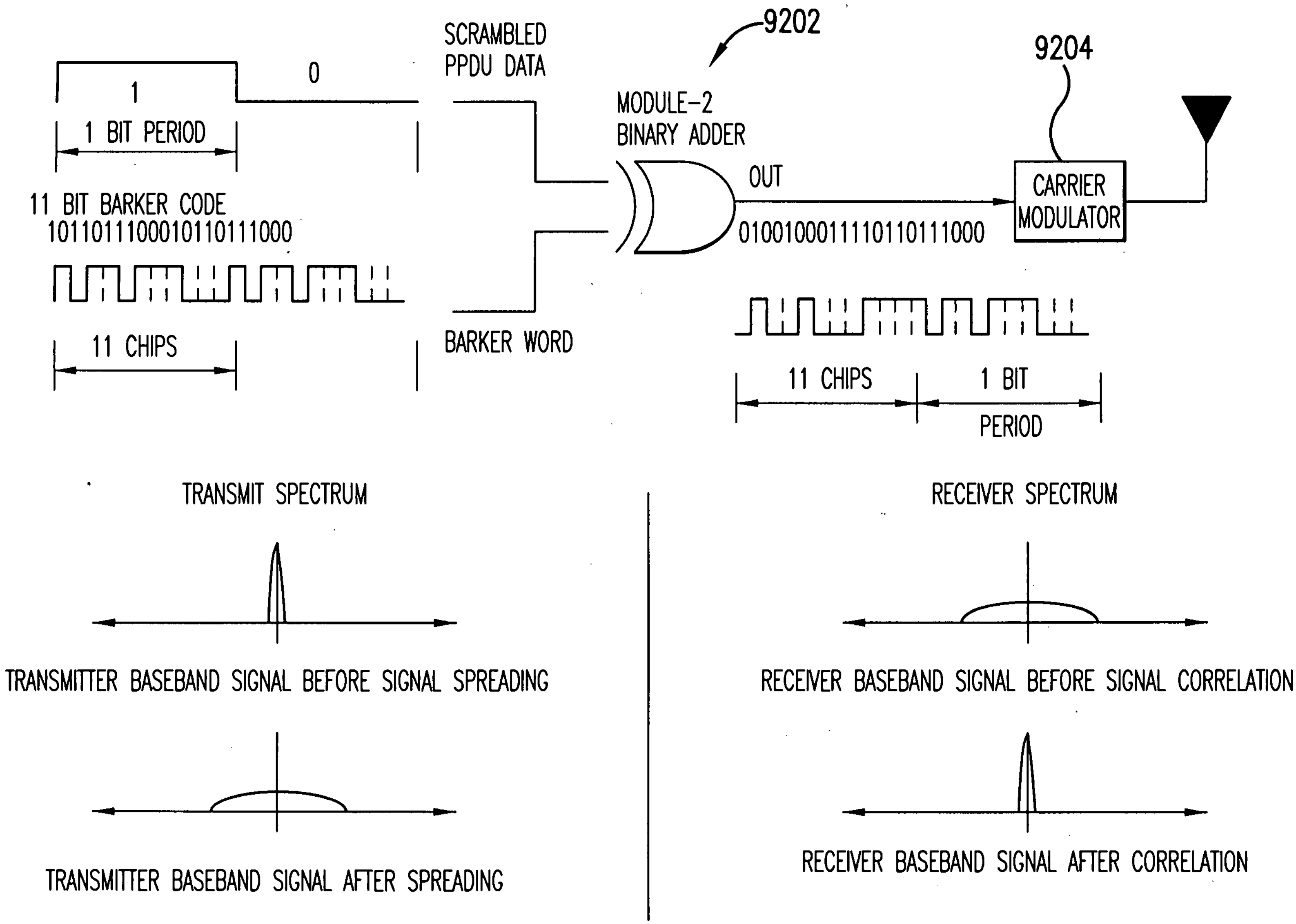

FIG.92

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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
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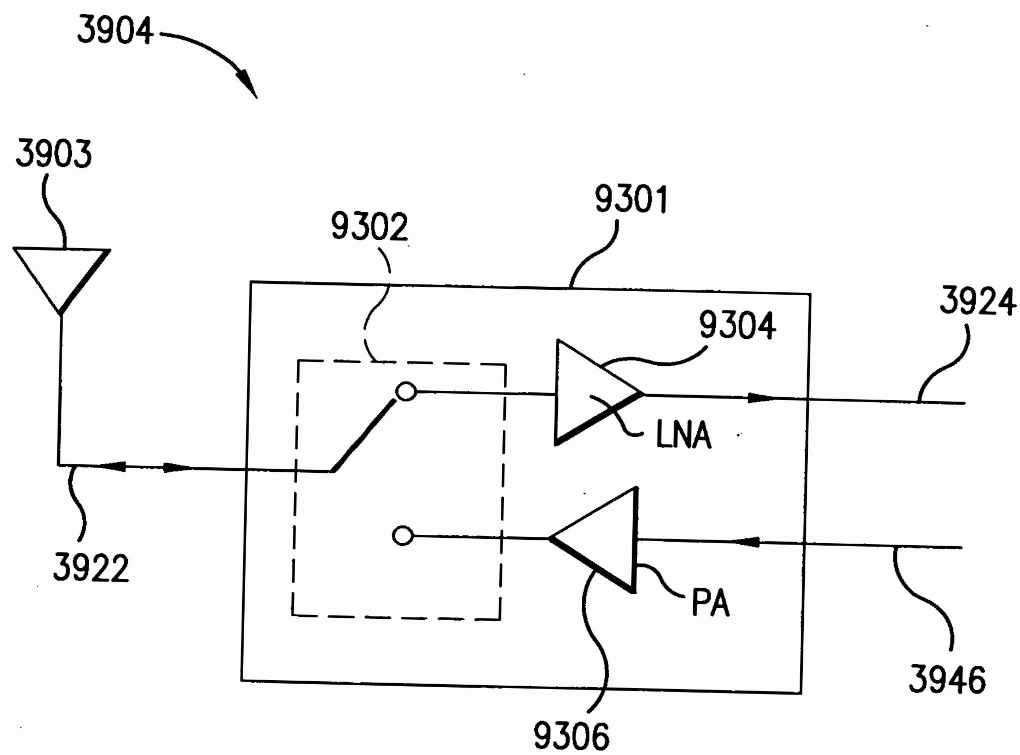

FIG.93

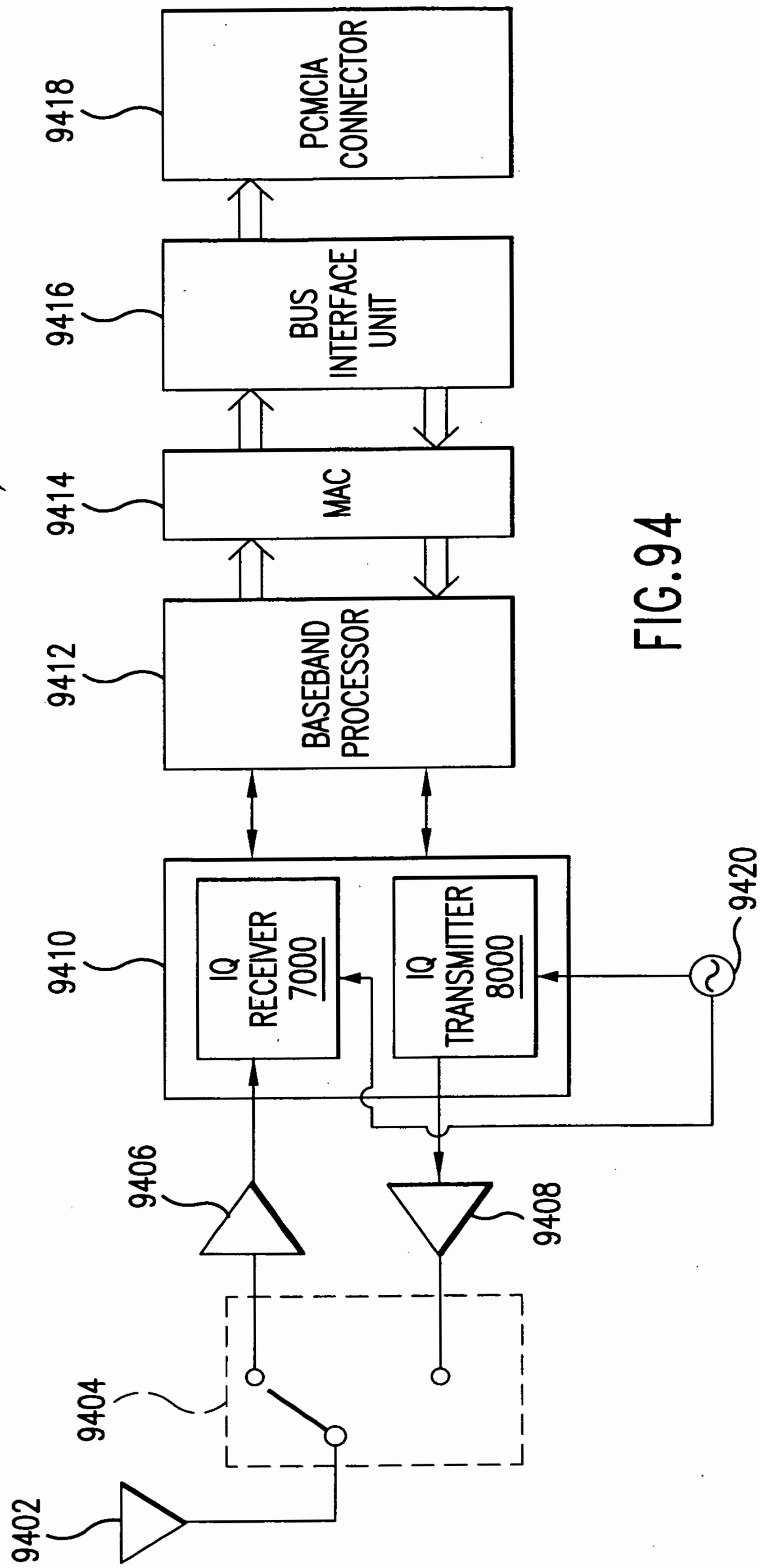
9400
9418
PCMCIA CONNECTOR
9416
BUS INTERFACE UNIT
9414
MAC
9412
BASEBAND PROCESSOR
9410
IQ RECEIVER 7000
IQ TRANSMITTER 8000
9420
9406
9408
9404
9402

FIG.94

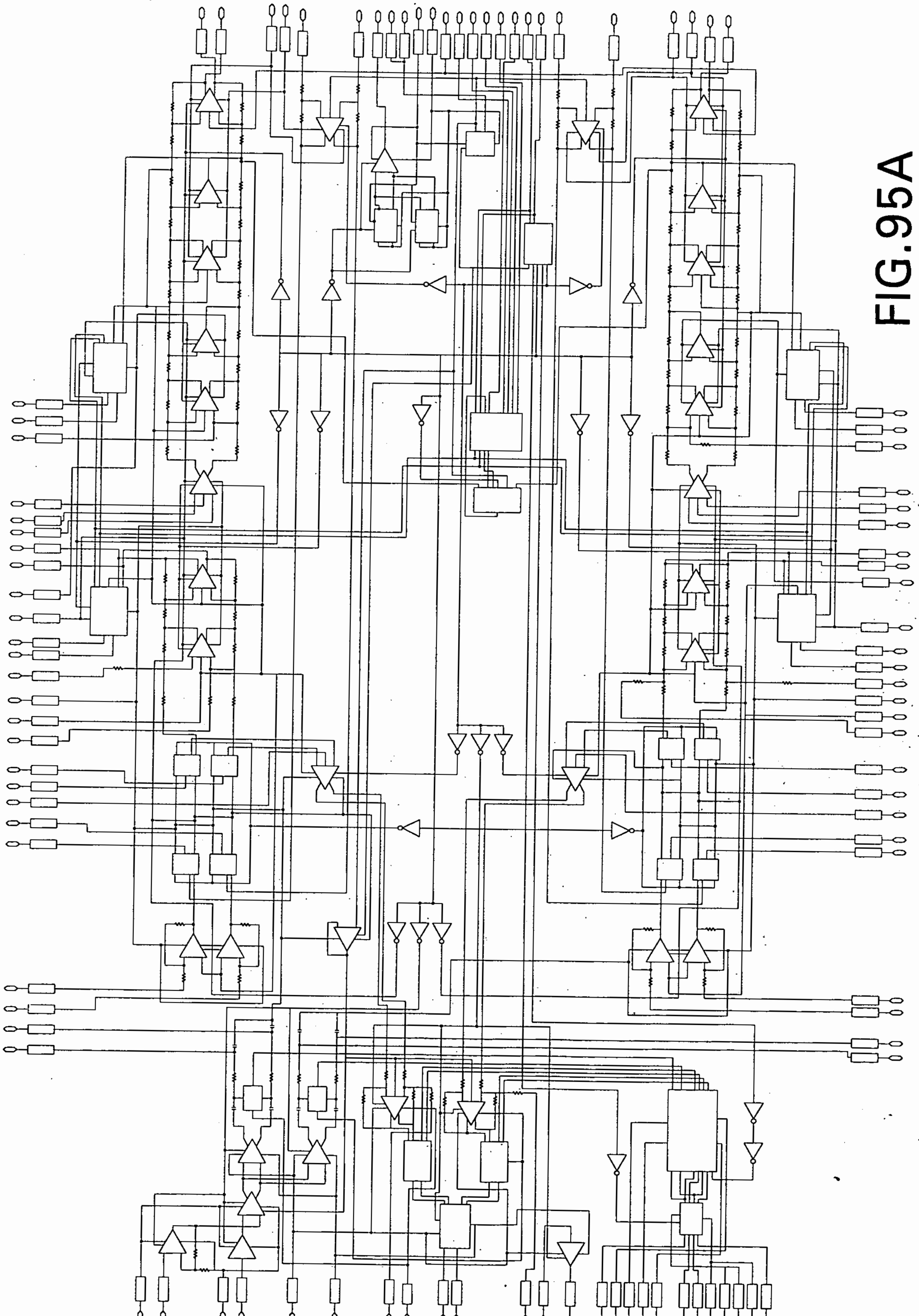

FIG.95A

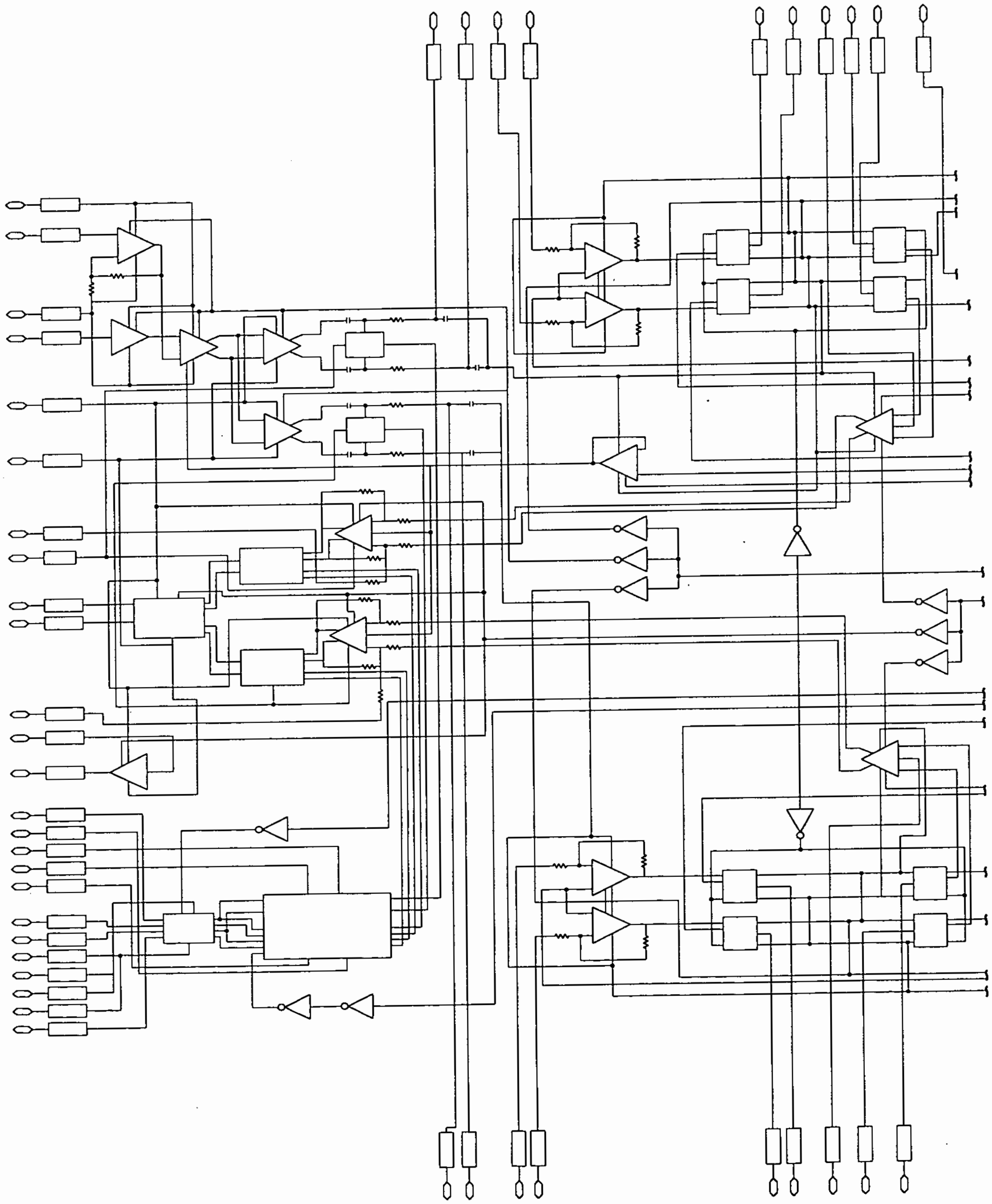

FIG.95B

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

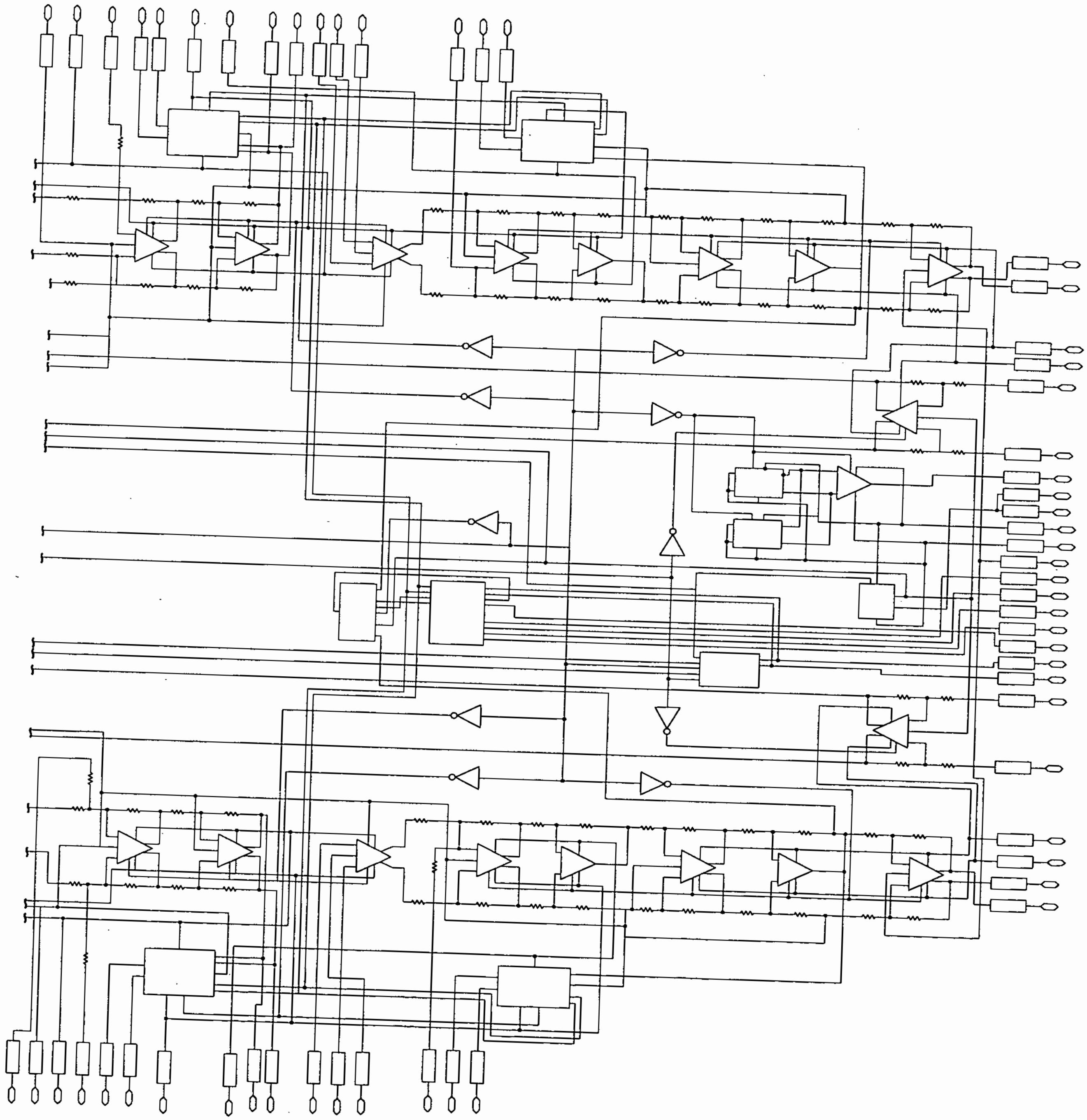

FIG.95C

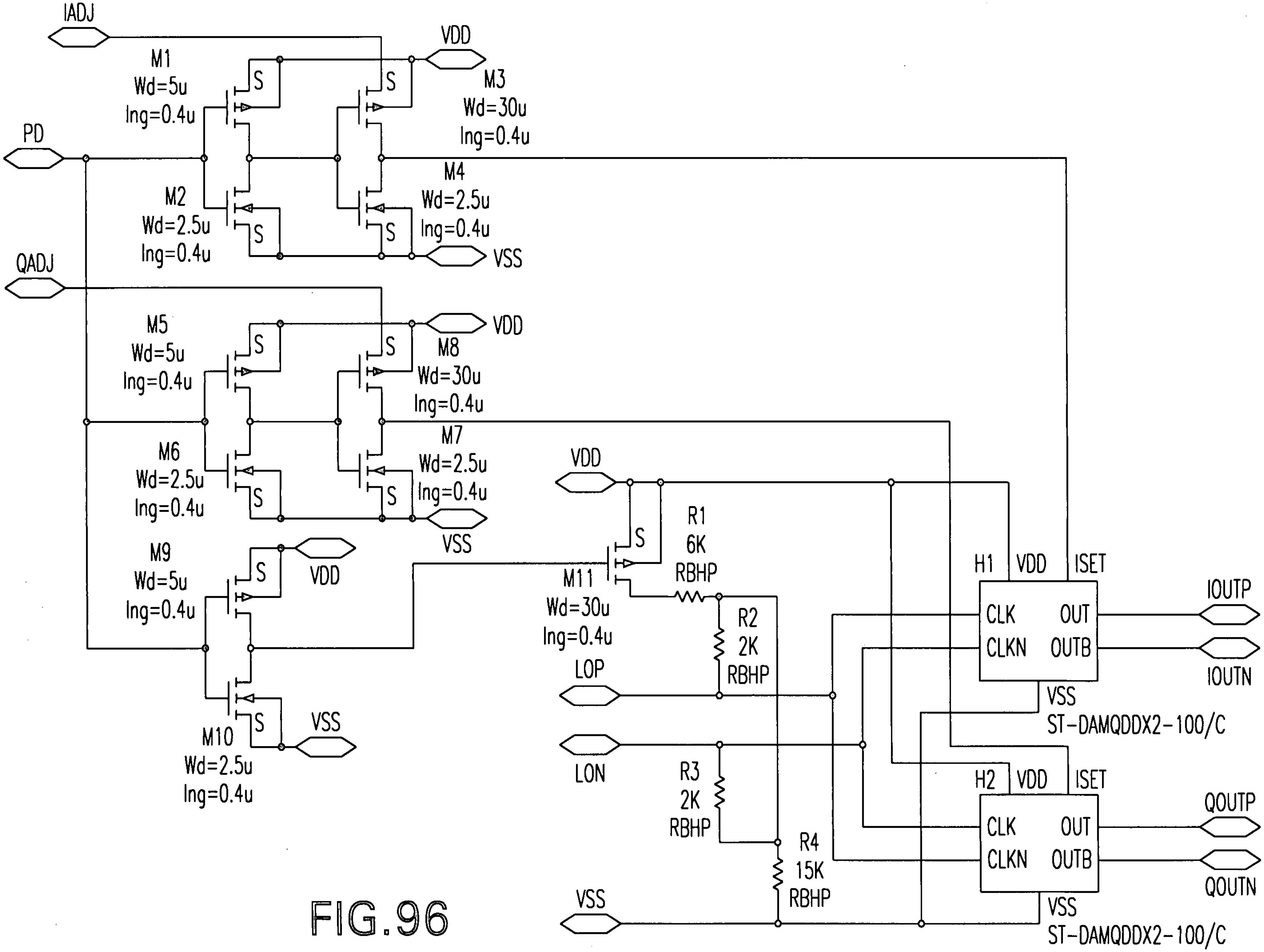

FIG.96

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Inventors: Sorrells et al.
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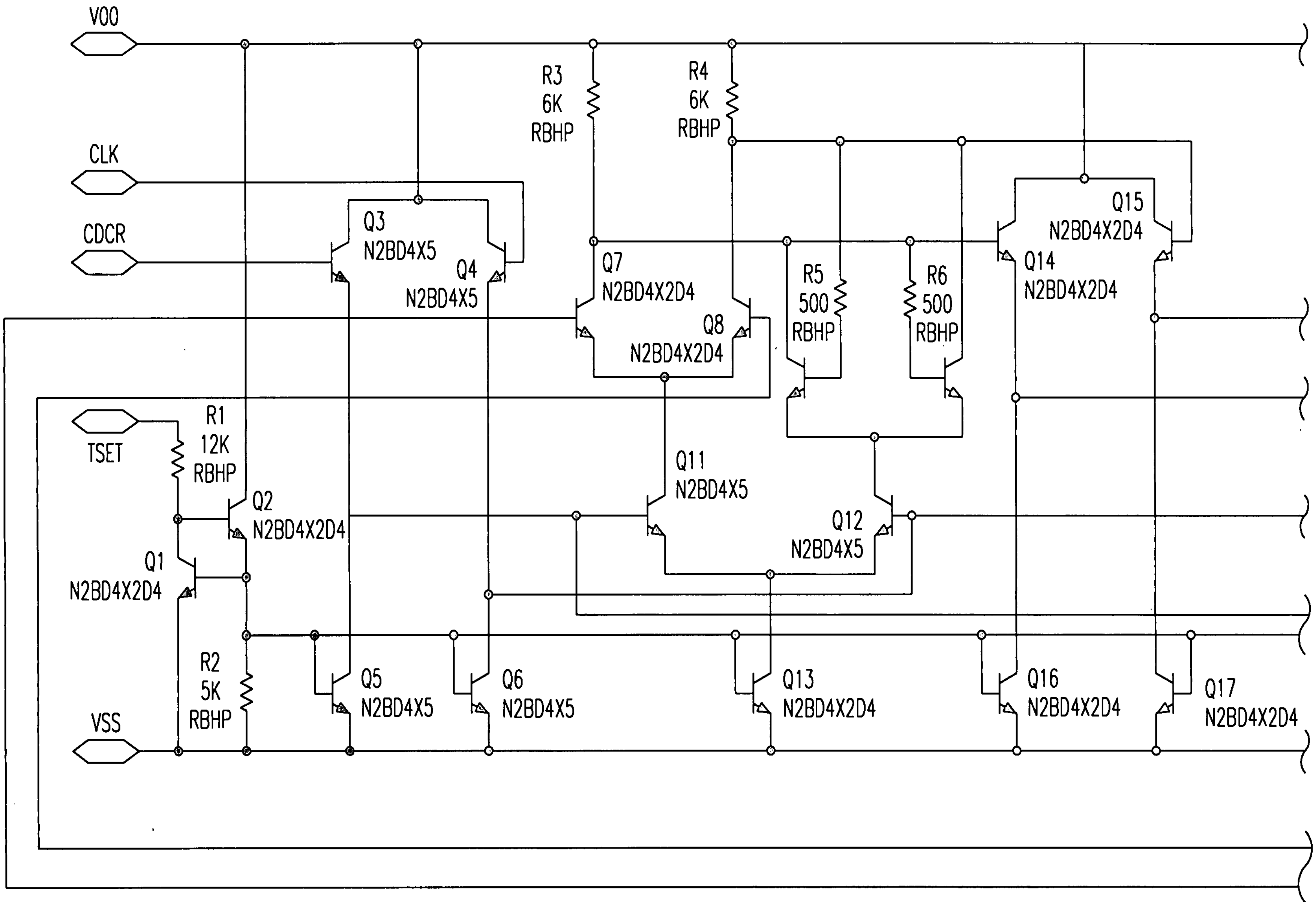
V00
CLK
CDCR
TSET
VSS
R1
12K
RBHP
R2
5K
RBHP
R3
6K
RBHP
R4
6K
RBHP
R5
500
RBHP
R6
500
RBHP
Q1
N2BD4X2D4
Q2
N2BD4X2D4
Q3
N2BD4X5
Q4
N2BD4X5
Q5
N2BD4X5
Q6
N2BD4X5
Q7
N2BD4X2D4
Q8
N2BD4X2D4
Q11
N2BD4X5
Q12
N2BD4X5
Q13
N2BD4X2D4
Q14
N2BD4X2D4
Q15
N2BD4X2D4
Q16
N2BD4X2D4
Q17
N2BD4X2D4

FIG.97A

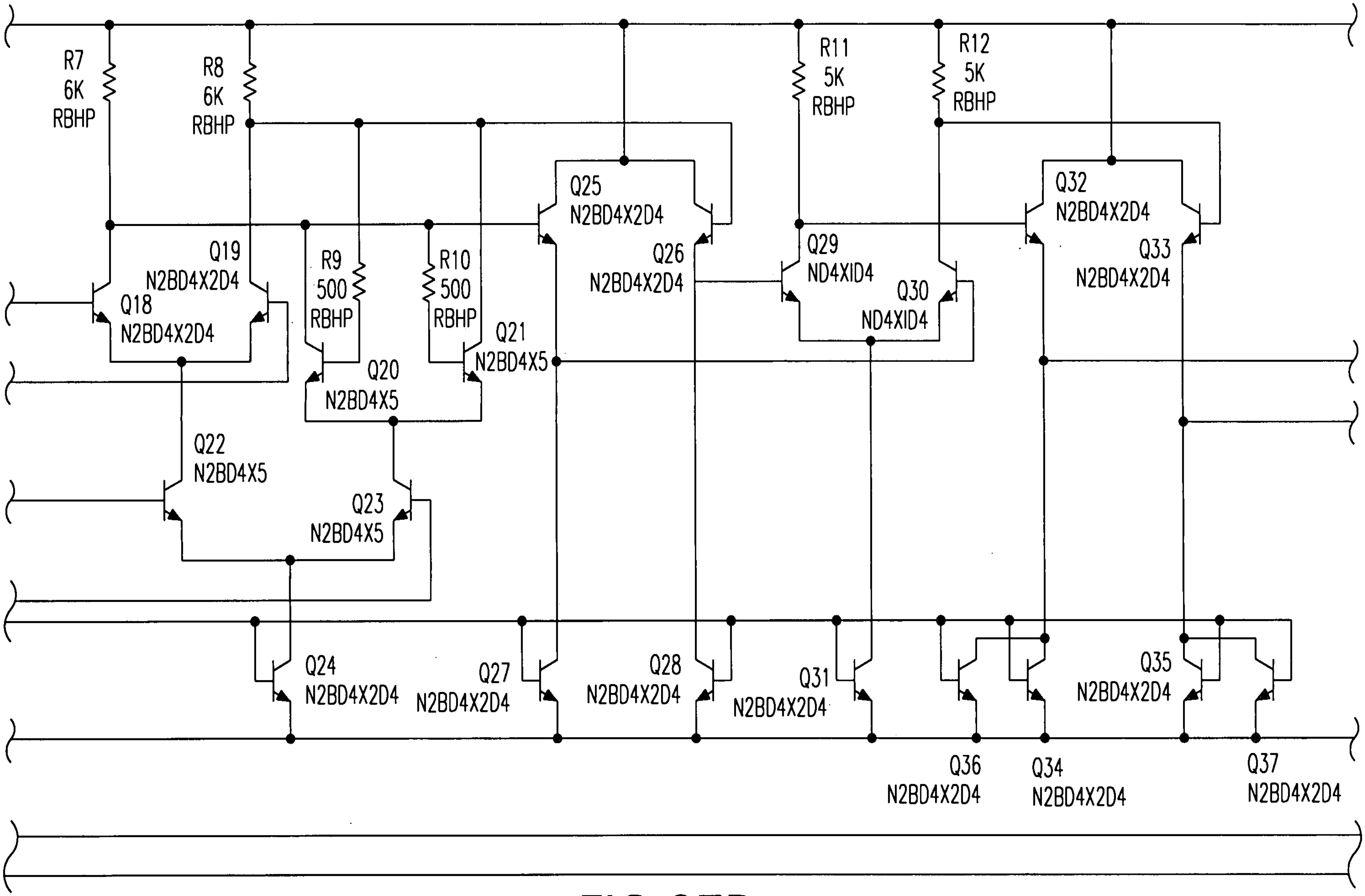

FIG.97B

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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

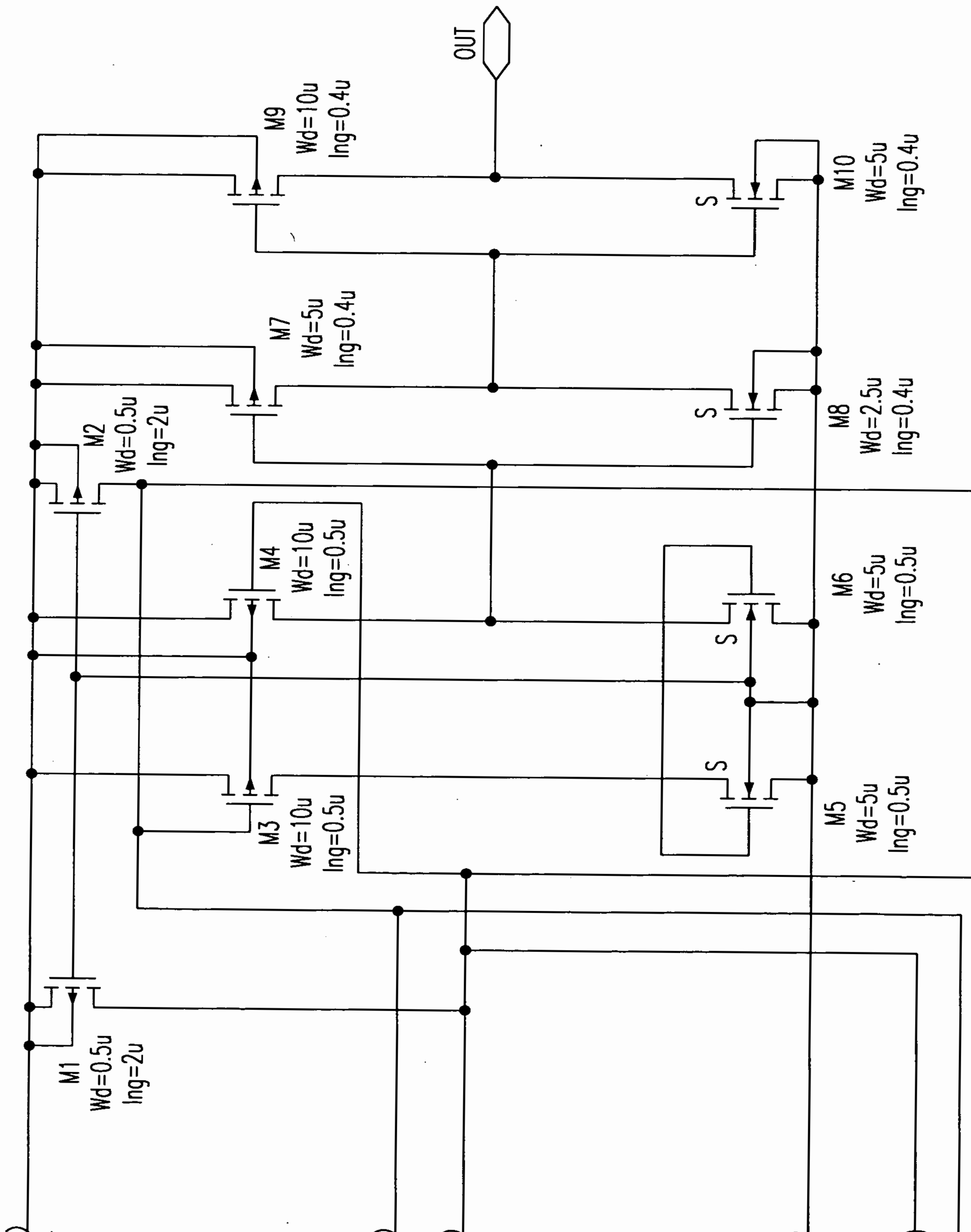
OUT
M9
Wd=10u
lng=0.4u
M10
Wd=5u
lng=0.4u
M7
Wd=5u
lng=0.4u
M8
Wd=2.5u
lng=0.4u
M2
Wd=0.5u
lng=2u
M4
Wd=10u
lng=0.5u
M6
Wd=5u
lng=0.5u
M3
Wd=10u
lng=0.5u
M5
Wd=5u
lng=0.5u
M1
Wd=0.5u
lng=2u
S
S
S
S

FIG.97C

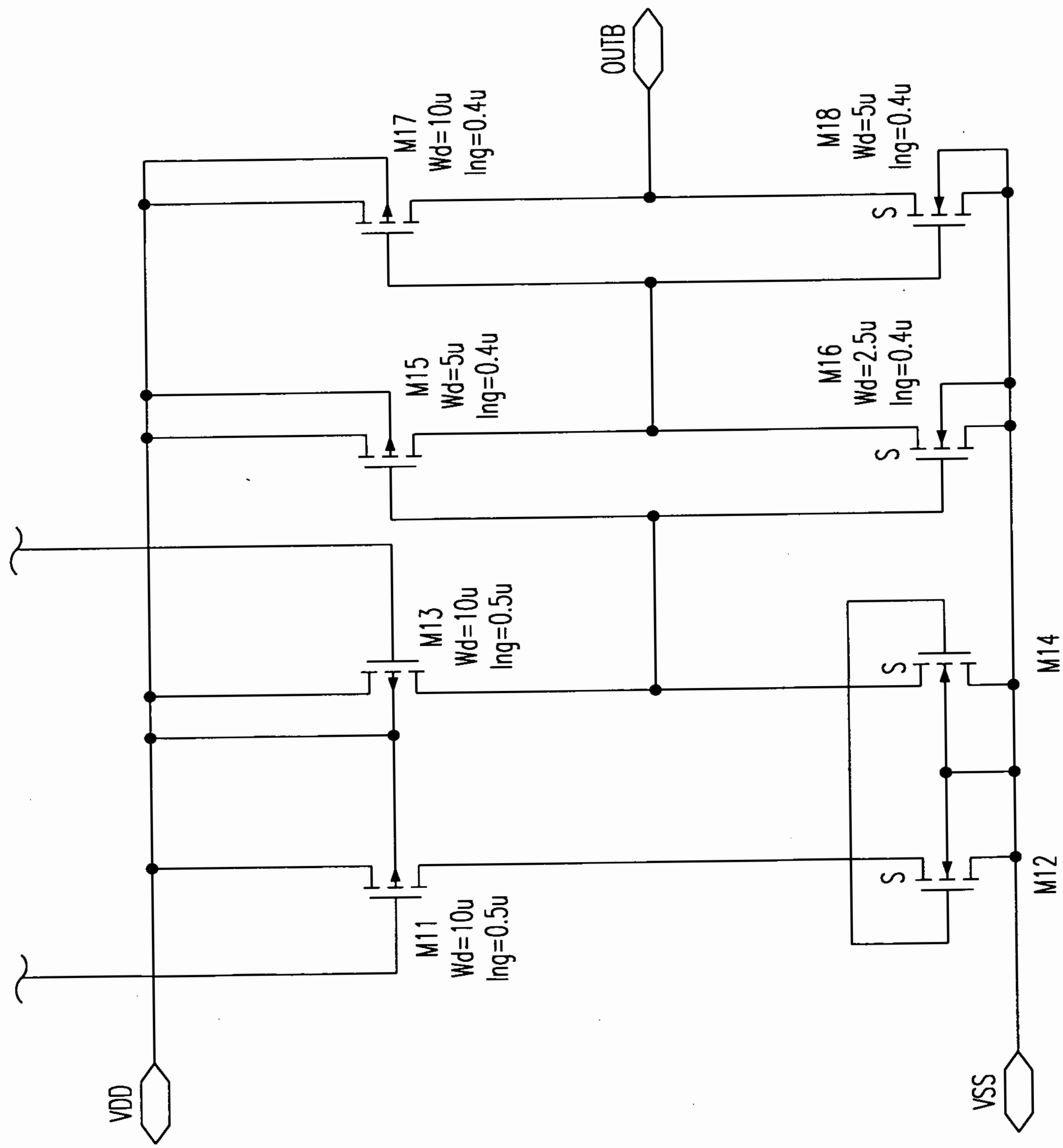
OUTB
M17
Wd=10u
lng=0.4u
M18
Wd=5u
lng=0.4u
M15
Wd=5u
lng=0.4u
M16
Wd=2.5u
lng=0.4u
M13
Wd=10u
lng=0.5u
M14
Wd=2.5u
lng=0.5u
M11
Wd=10u
lng=0.5u
M12
Wd=5u
lng=0.5u
S
S
S
S
VDD
VSS

FIG.97D

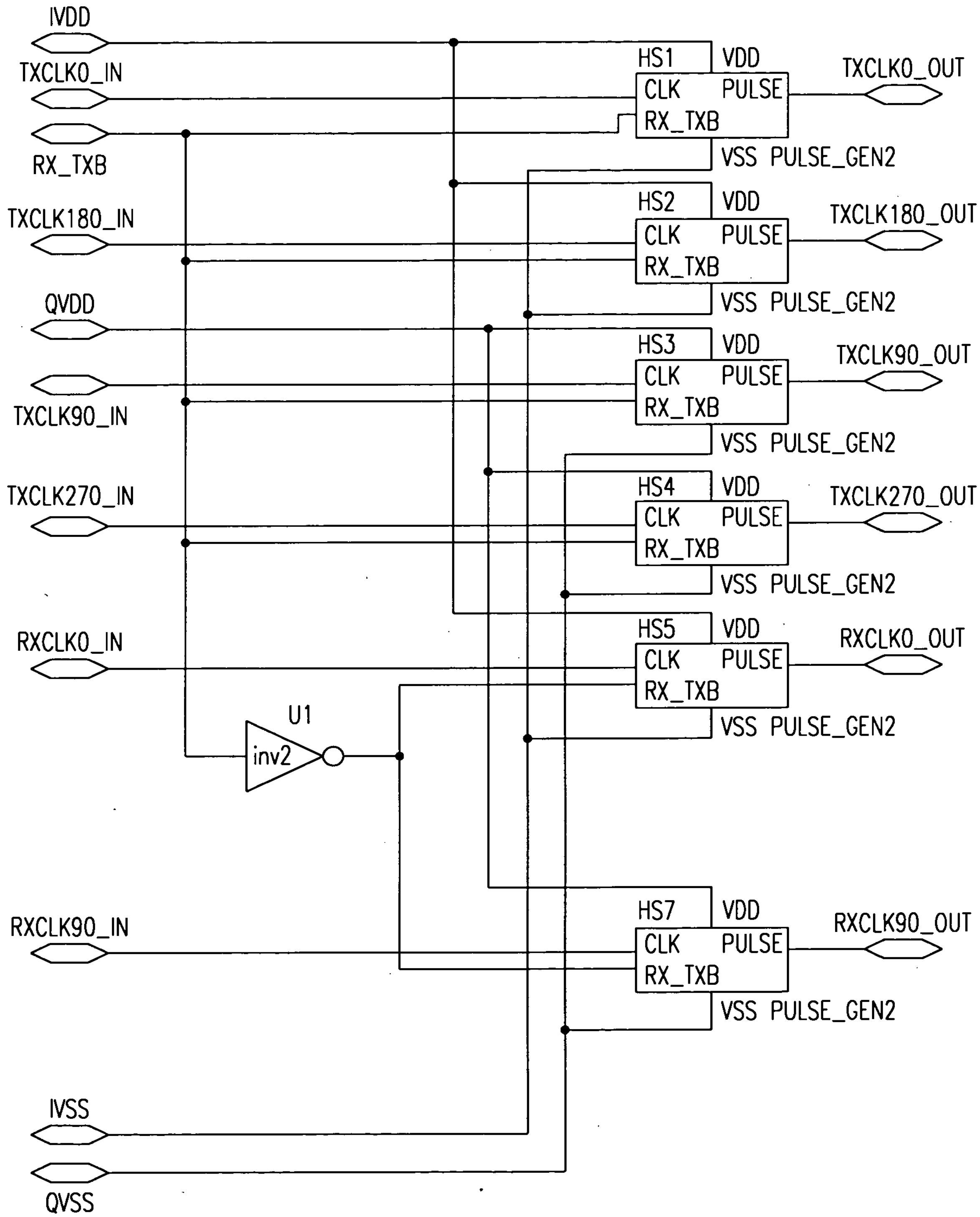
IVDD
TXCLK0_IN
RX_TXB
TXCLK180_IN
QVDD
TXCLK90_IN
TXCLK270_IN
RXCLK0_IN
RXCLK90_IN
IVSS
QVSS
HS1 VDD CLK PULSE RX_TXB VSS PULSE_GEN2
HS2 VDD CLK PULSE RX_TXB VSS PULSE_GEN2
HS3 VDD CLK PULSE RX_TXB VSS PULSE_GEN2
HS4 VDD CLK PULSE RX_TXB VSS PULSE_GEN2
HS5 VDD CLK PULSE RX_TXB VSS PULSE_GEN2
HS7 VDD CLK PULSE RX_TXB VSS PULSE_GEN2
U1
inv2
TXCLK0_OUT
TXCLK180_OUT
TXCLK90_OUT
TXCLK270_OUT
RXCLK0_OUT
RXCLK90_OUT

FIG.98

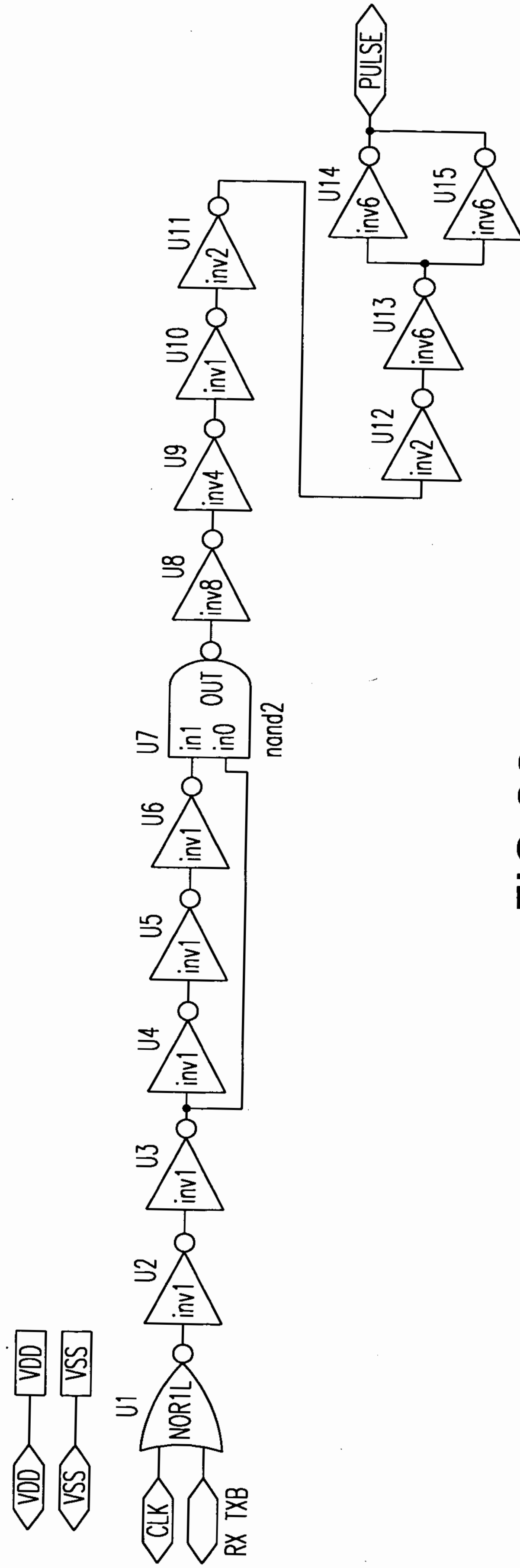
PULSE
U14
inv6
U15
inv6
U13
inv6
U12
inv2
U11
inv2
U10
inv1
U9
inv4
U8
inv8
U7
in1
in0
OUT
nand2
U6
inv1
U5
inv1
U4
inv1
U3
inv1
U2
inv1
U1
NOR1L
CLK
RX TXB
VDD
VDD
VSS
VSS

FIG.99

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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

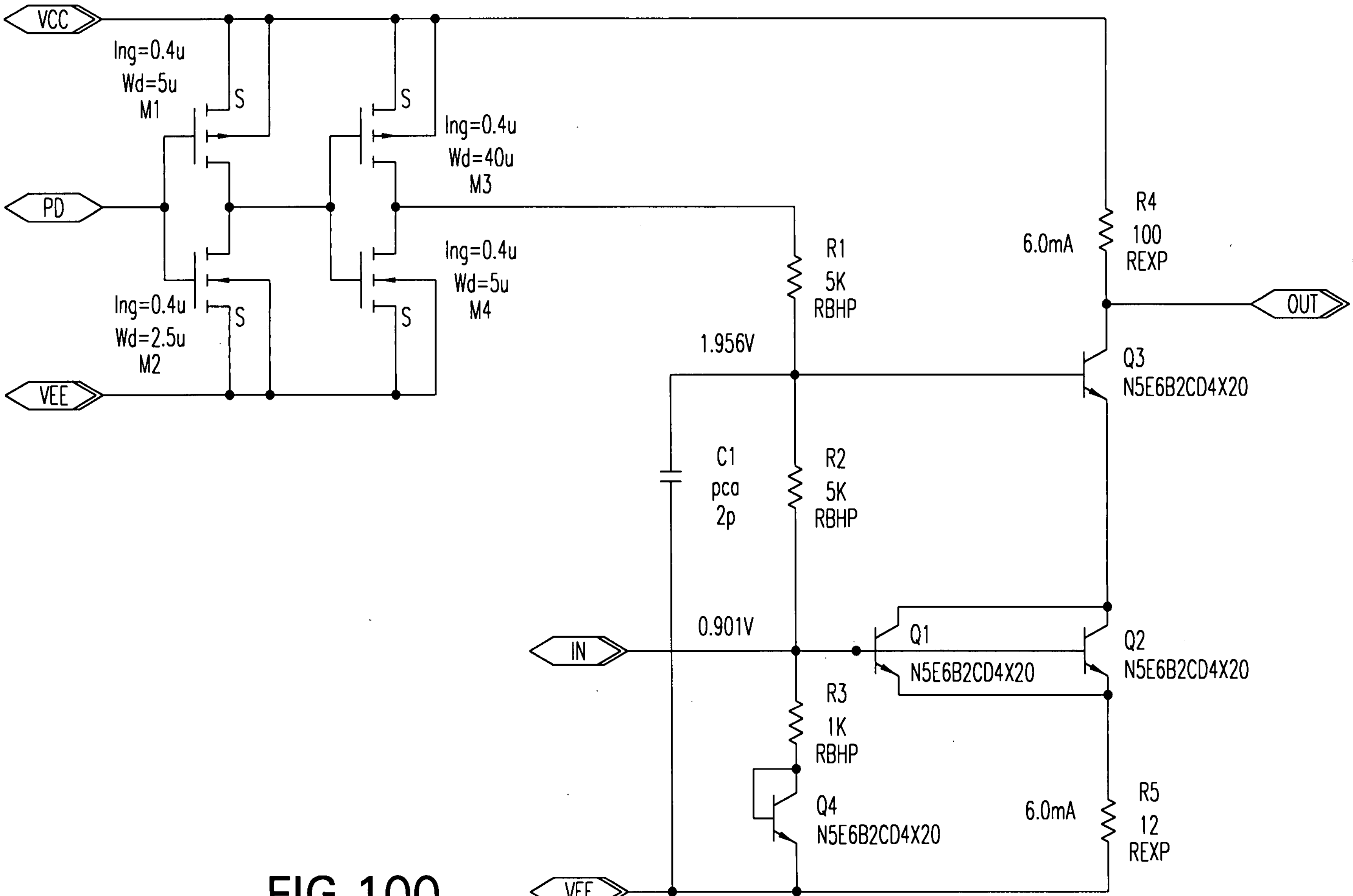

FIG.100

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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

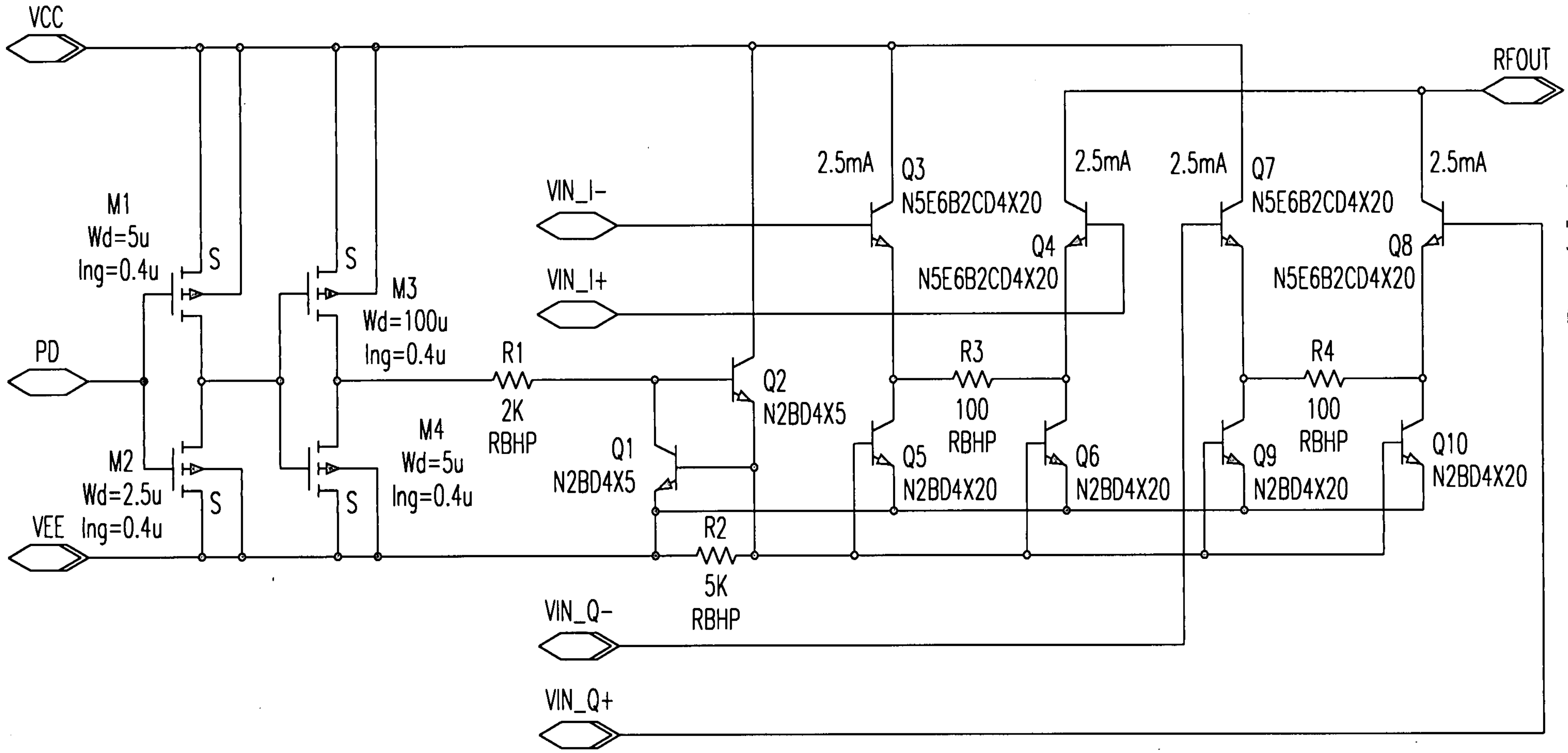

FIG.101

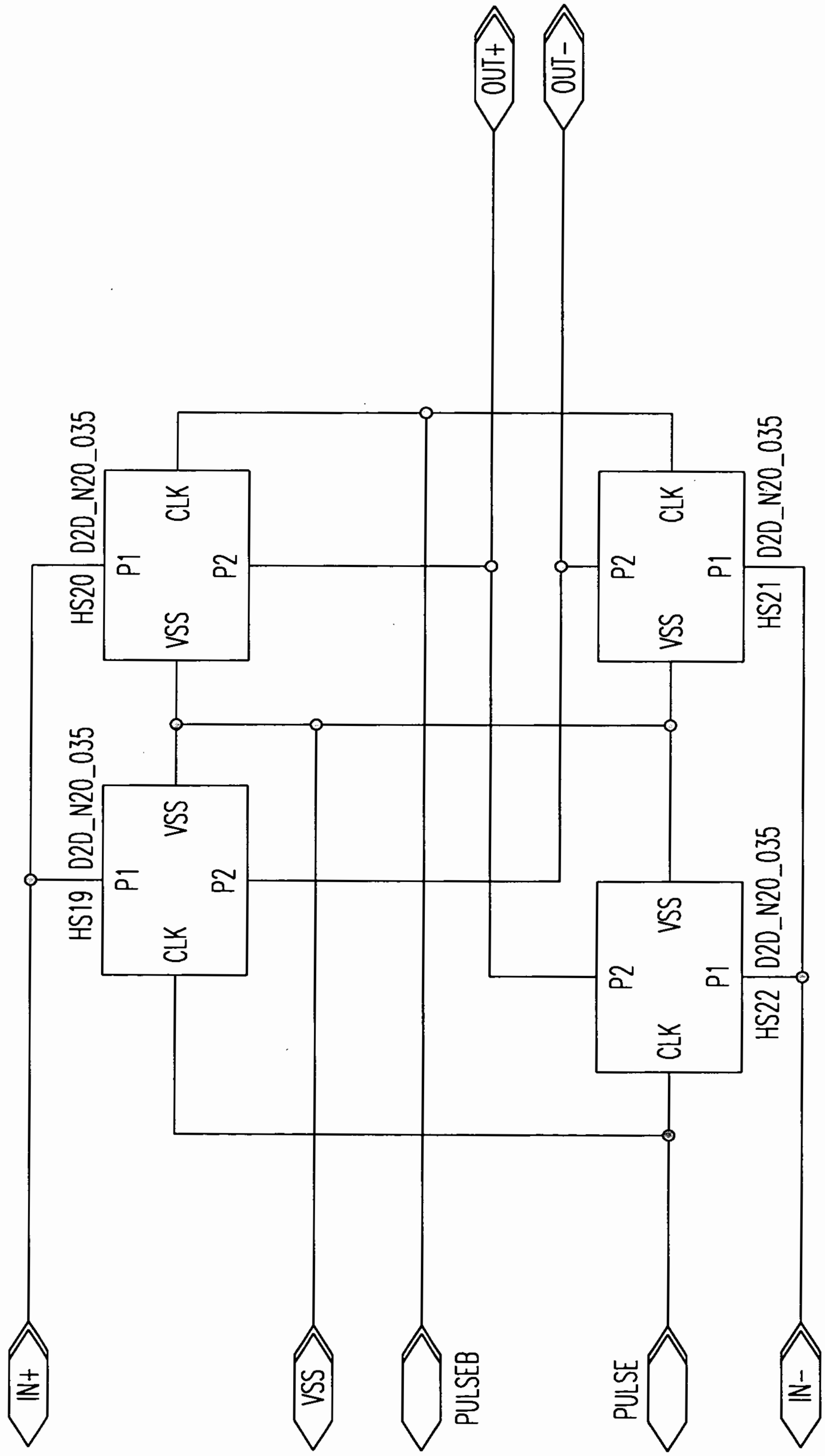
OUT+
OUT-
HS20
D2D_N20_035
P1
CLK
P2
VSS
HS21
D2D_N20_035
P2
CLK
P1
VSS
HS19
D2D_N20_035
P1
VSS
CLK
P2
HS22
D2D_N20_035
P2
VSS
CLK
P1
IN+
VSS
PULSEB
PULSE
IN-

FIG. 102

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Inventors: Sorrells et al.
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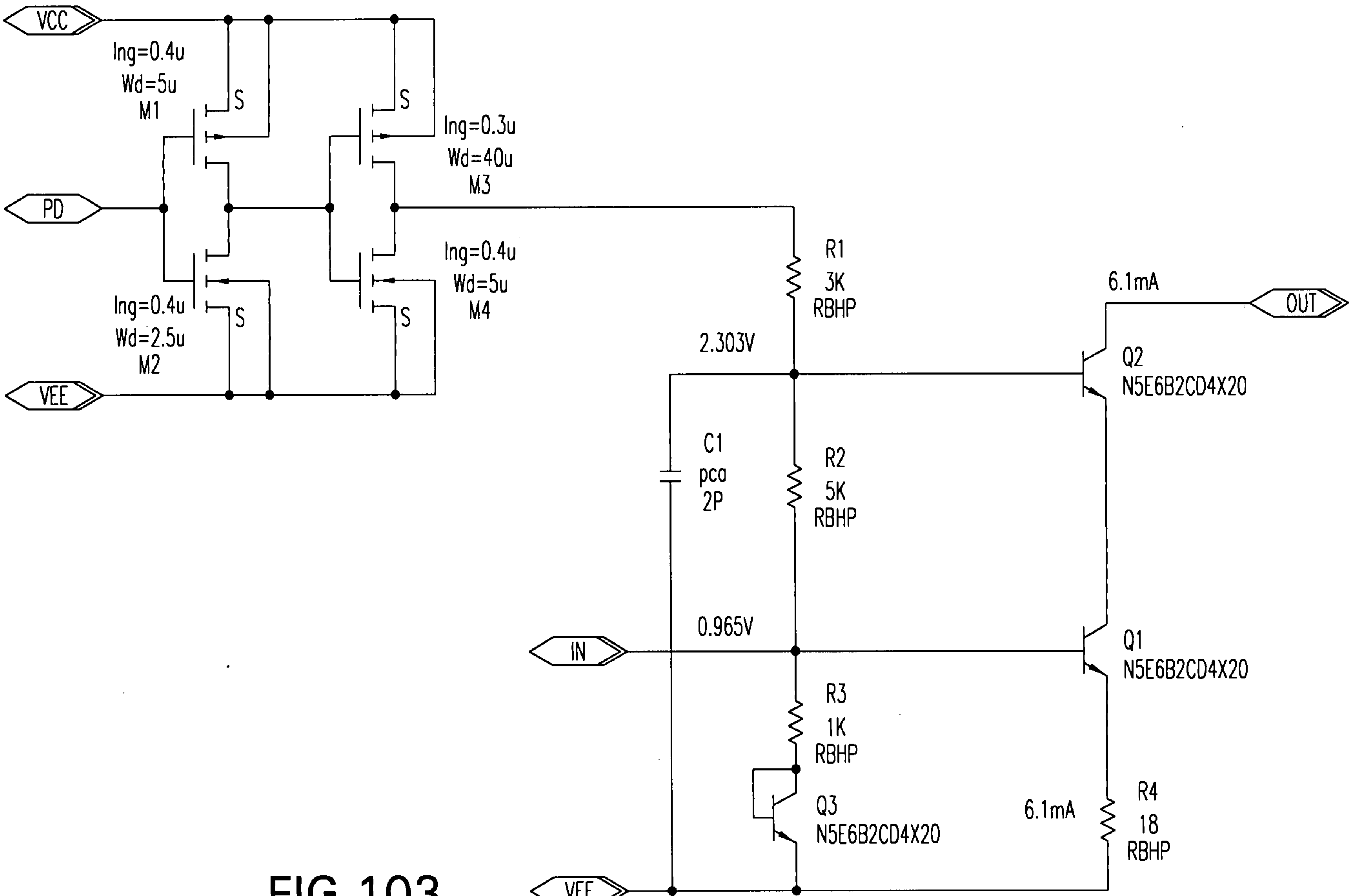

FIG.103

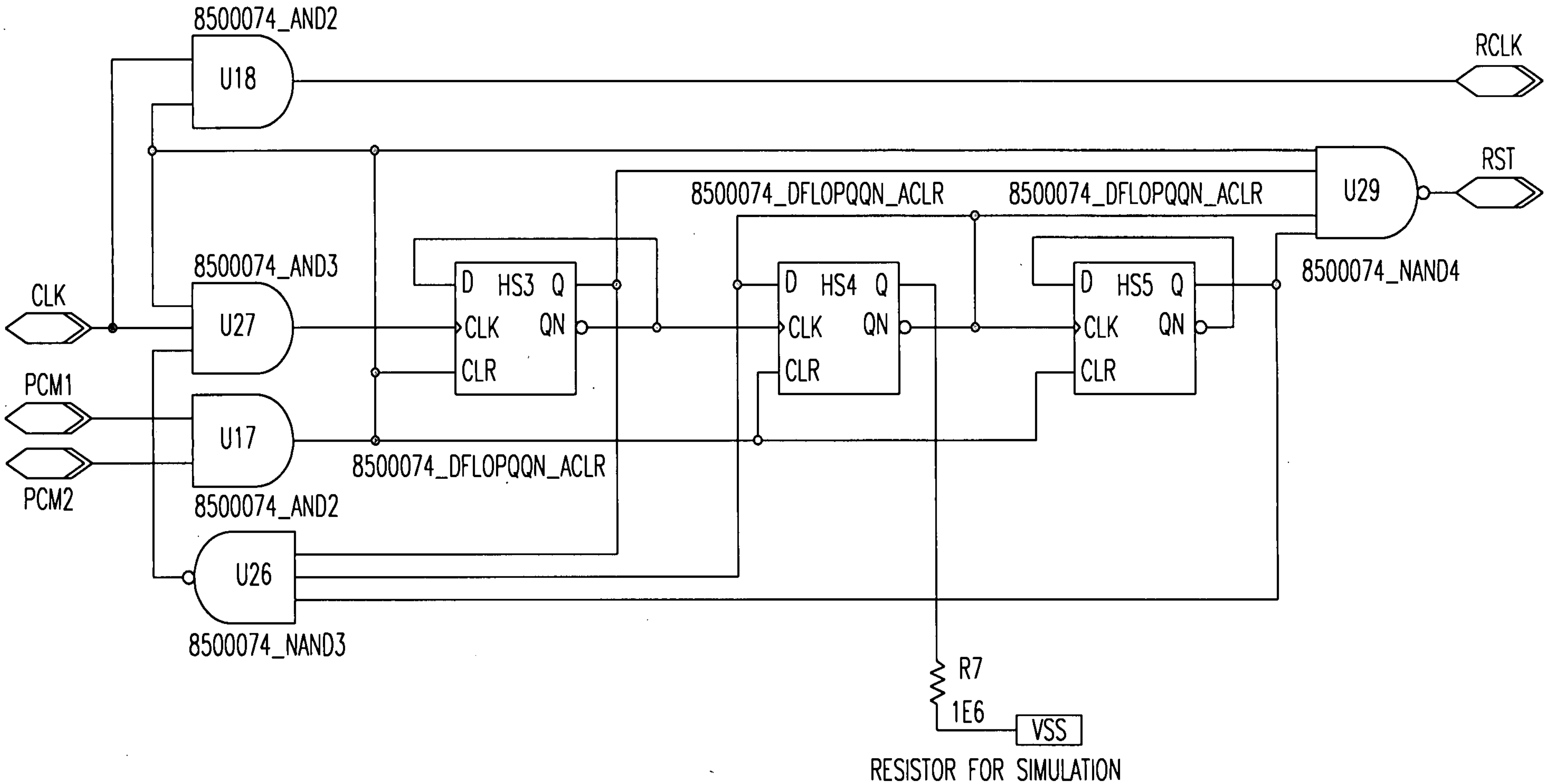

FIG.104

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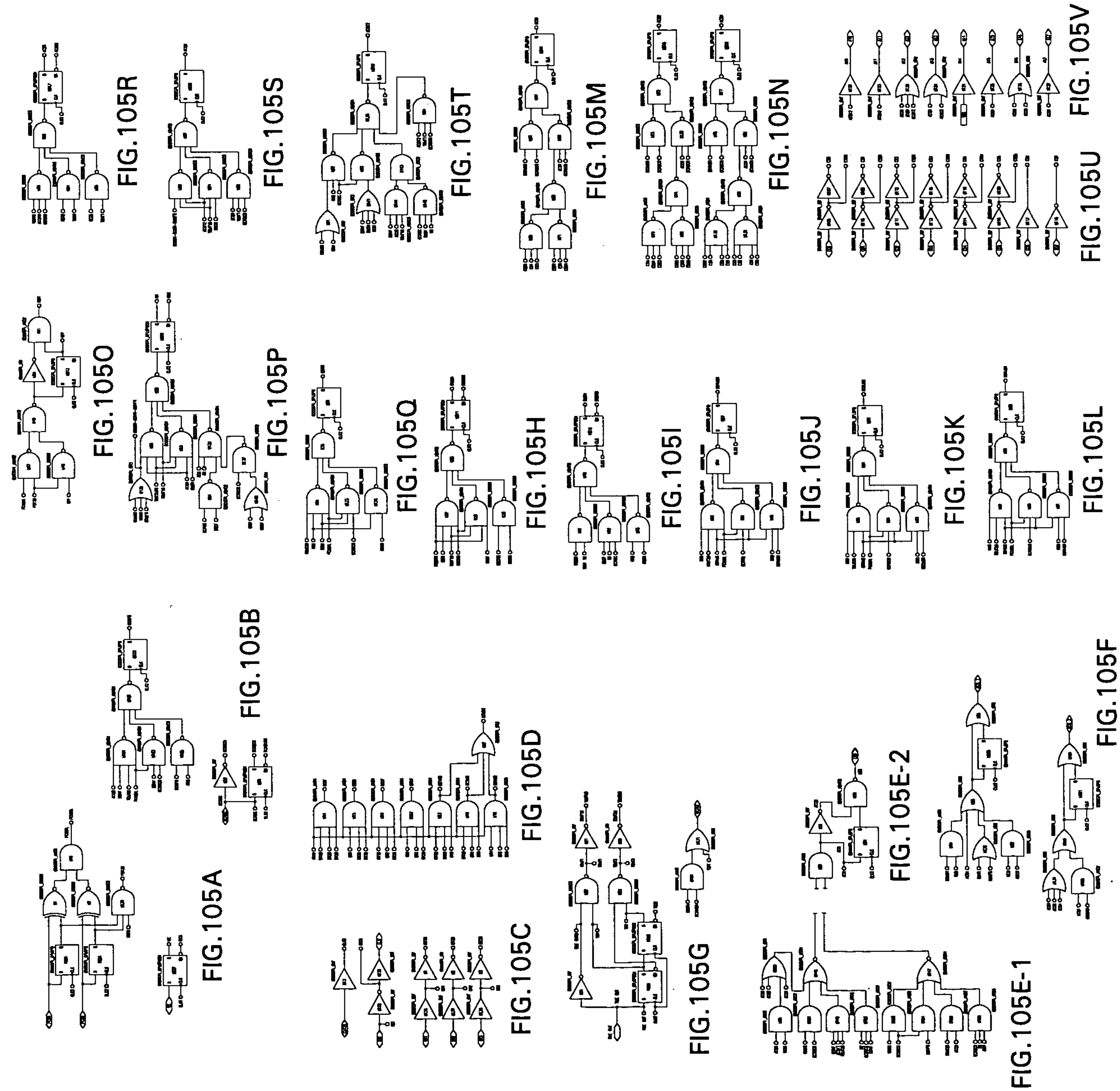

FIG.105

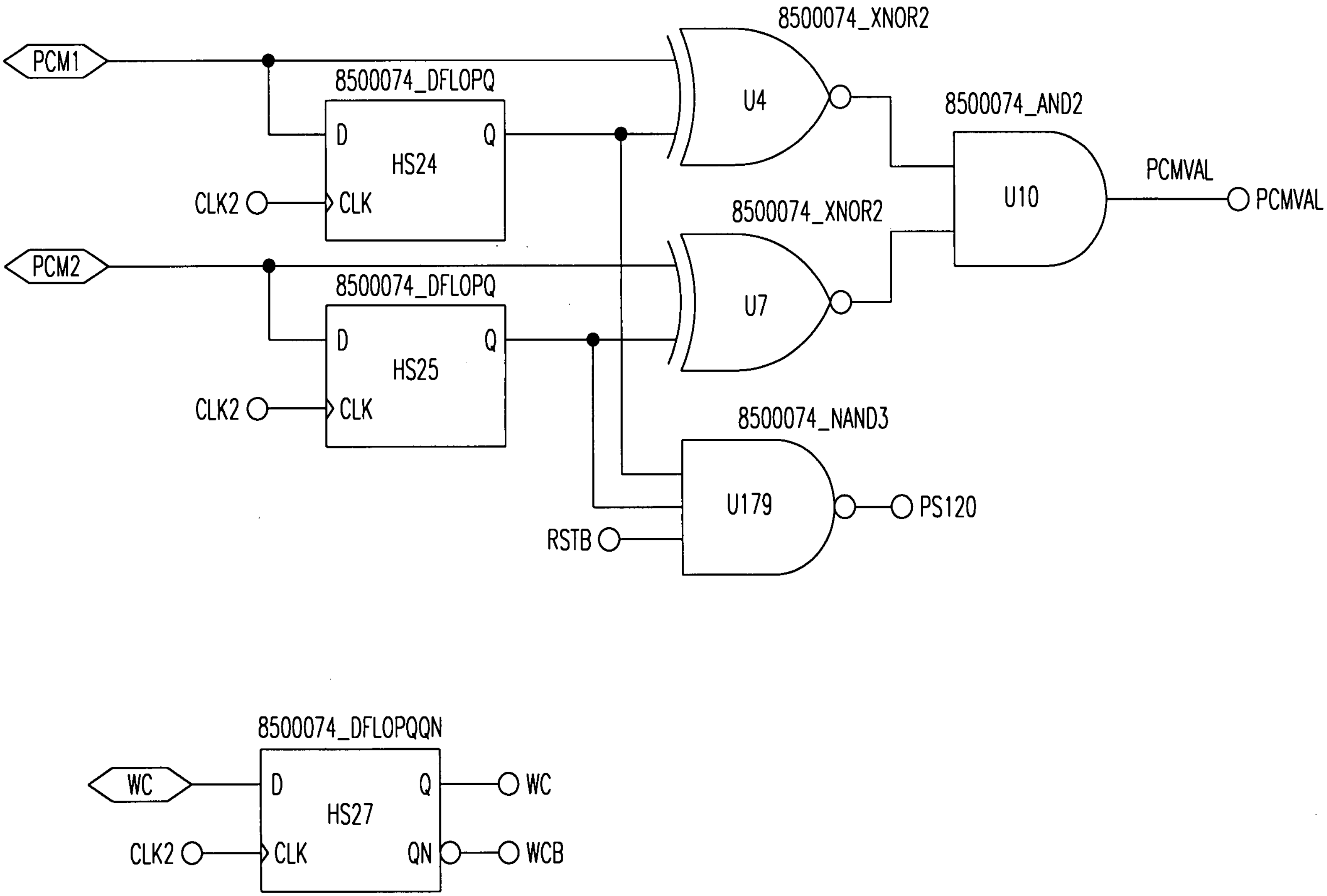

FIG.105A

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Inventors: Sorrells et al.
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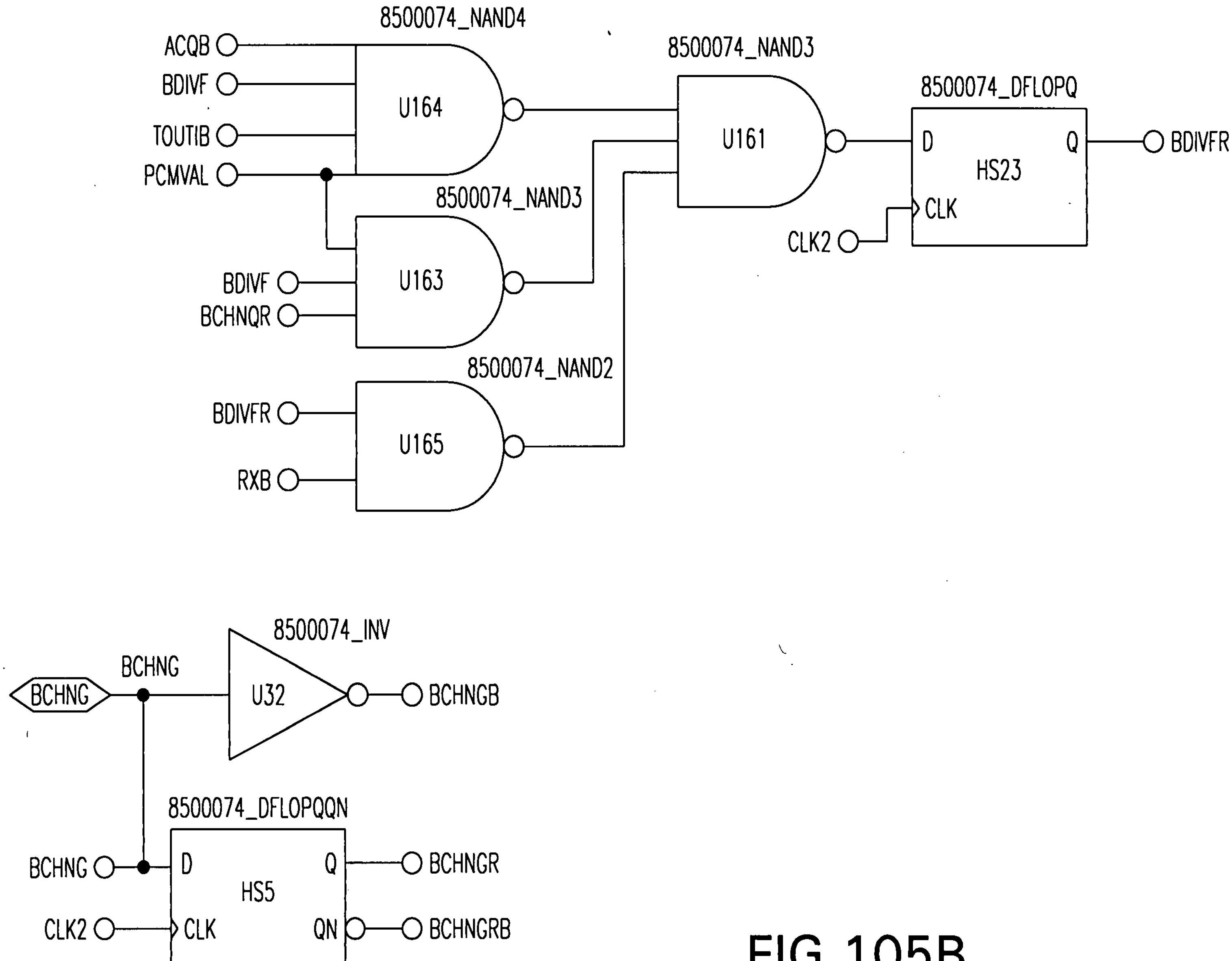

FIG. 105B

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Inventors: Sorrells et al.
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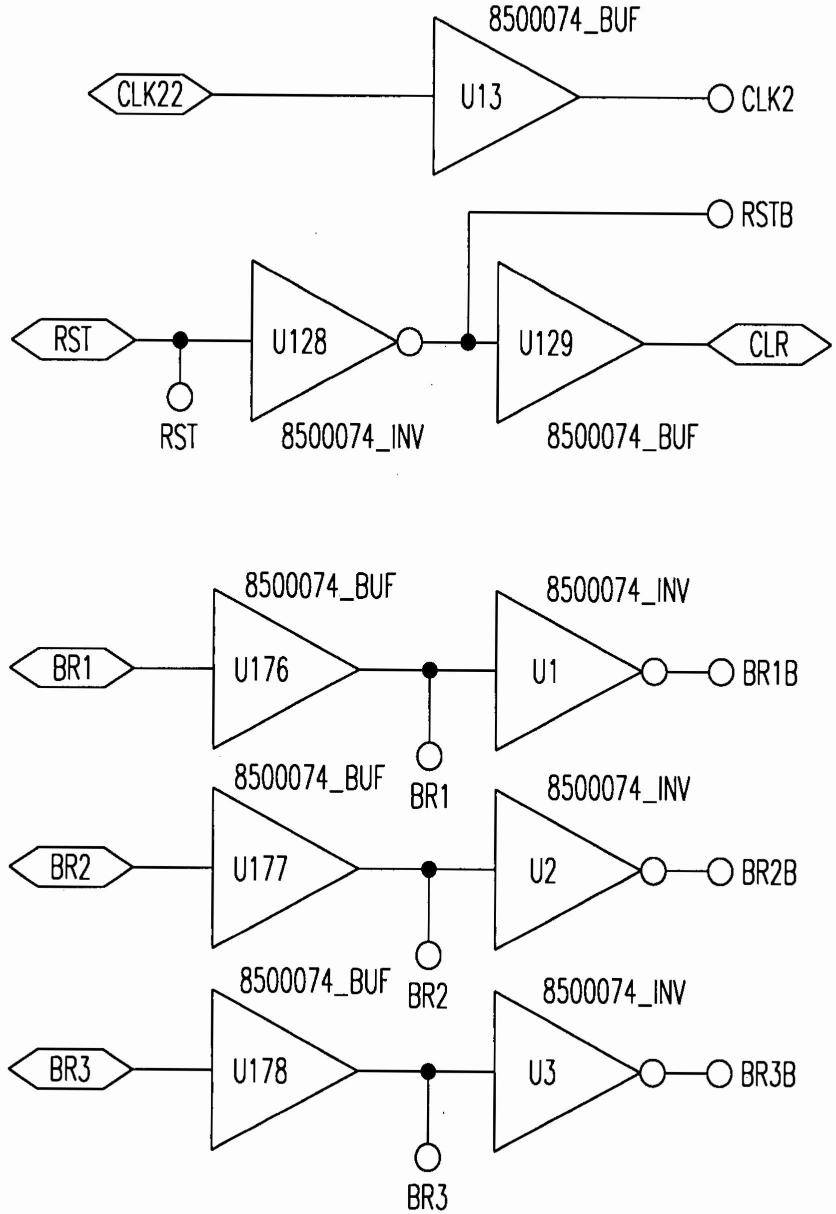

FIG. 105C

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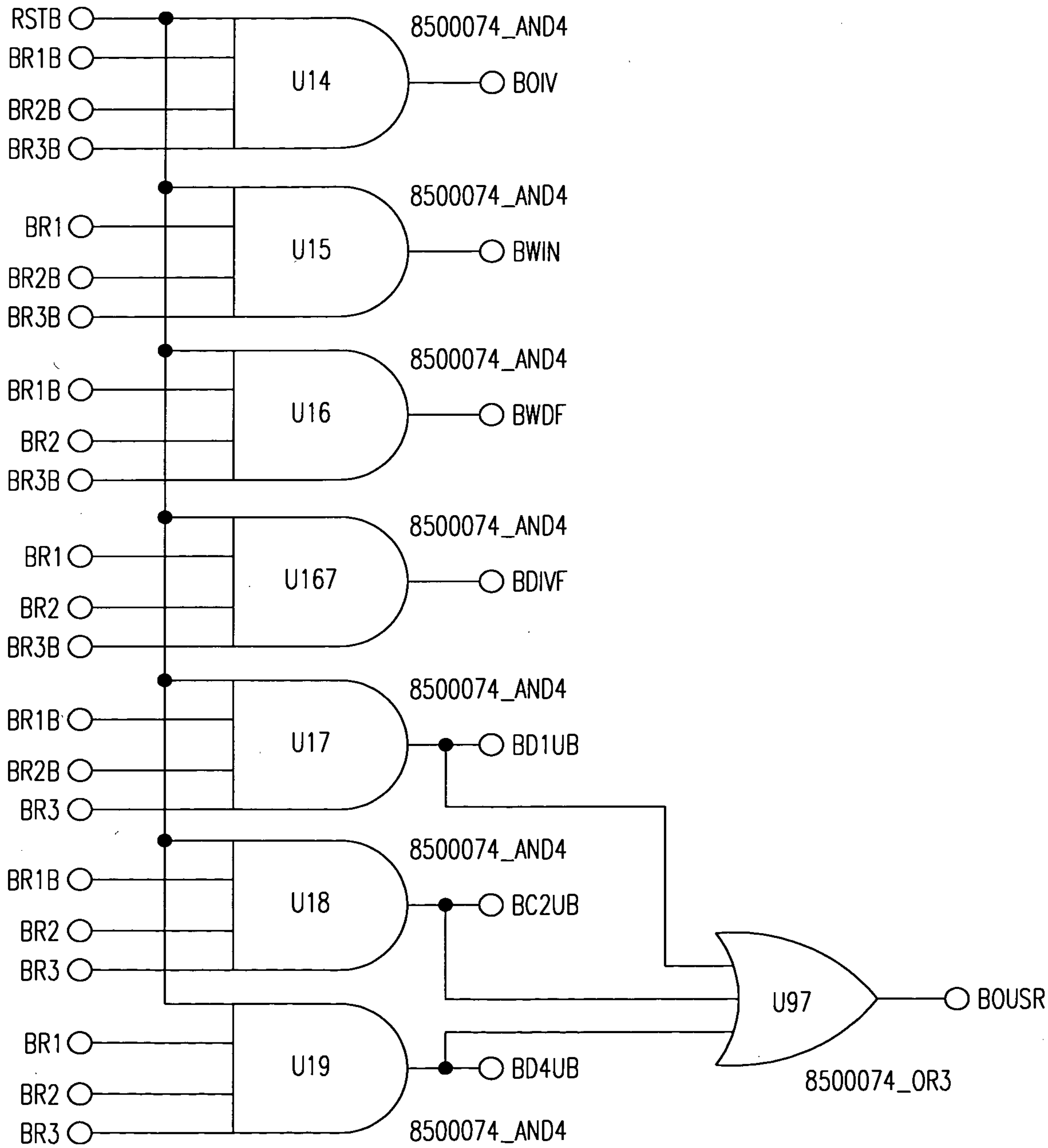
RSTB
BR1B
BR2B
BR3B
U14
8500074_AND4
BOIV
BR1
BR2B
BR3B
U15
8500074_AND4
BWIN
BR1B
BR2
BR3B
U16
8500074_AND4
BWDF
BR1
BR2
BR3B
U167
8500074_AND4
BDIVF
BR1B
BR2B
BR3
U17
8500074_AND4
BD1UB
BR1B
BR2
BR3
U18
8500074_AND4
BC2UB
BR1
BR2
BR3
U19
8500074_AND4
BD4UB
U97
8500074_OR3
BOUSR

FIG. 105D

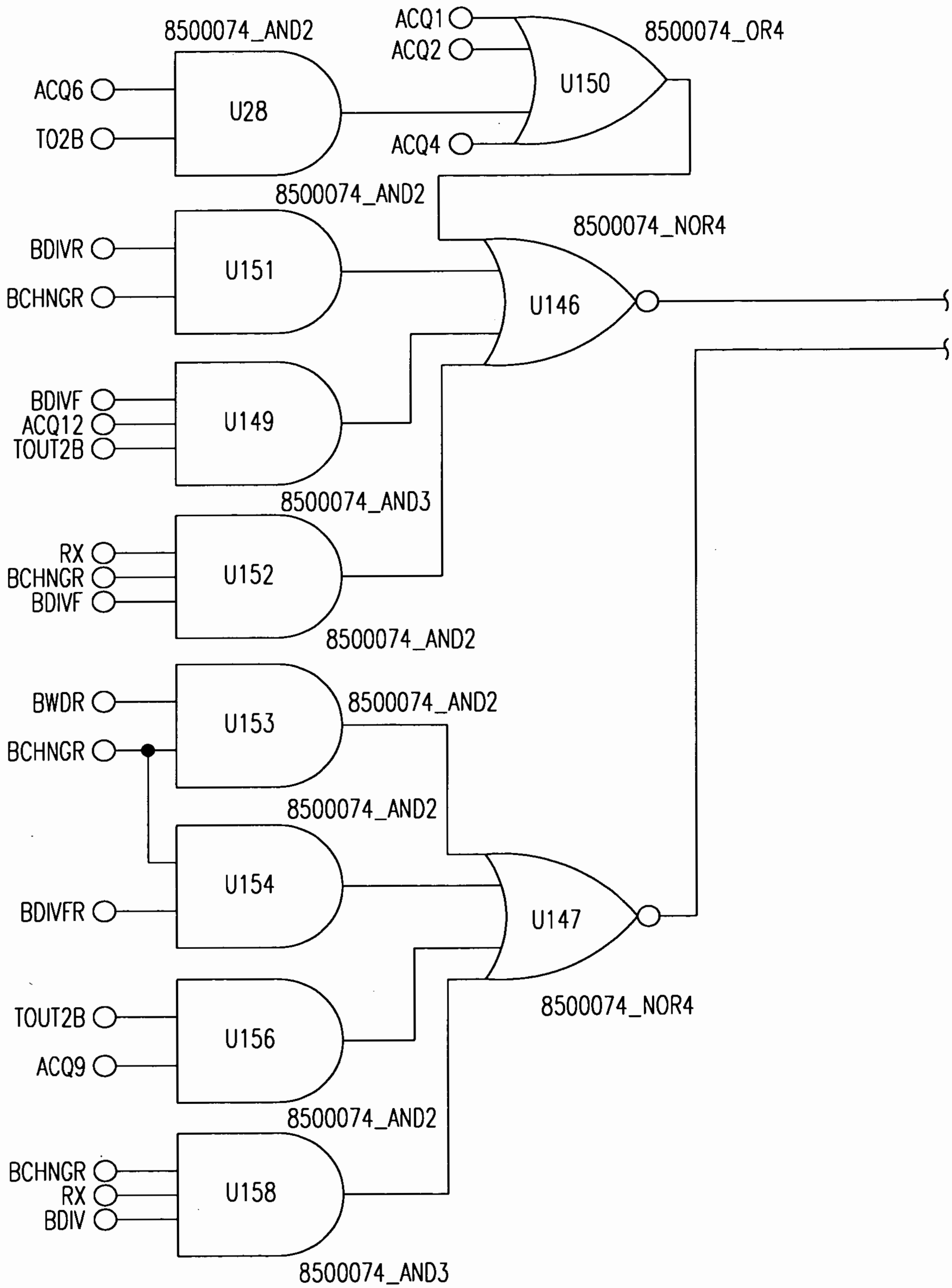
8500074_AND2
ACQ1
ACQ2
8500074_OR4
ACQ6
U28
T02B
U150
ACQ4
8500074_AND2
8500074_NOR4
BDIVR
U151
BCHNGR
U146
BDIVF
ACQ12
TOUT2B
U149
8500074_AND3
RX
BCHNGR
BDIVF
U152
8500074_AND2
BWDR
U153
8500074_AND2
BCHNGR
8500074_AND2
U154
BDIVFR
U147
TOUT2B
U156
8500074_NOR4
ACQ9
8500074_AND2
BCHNGR
RX
BDIV
U158
8500074_AND3

FIG. 105E-1

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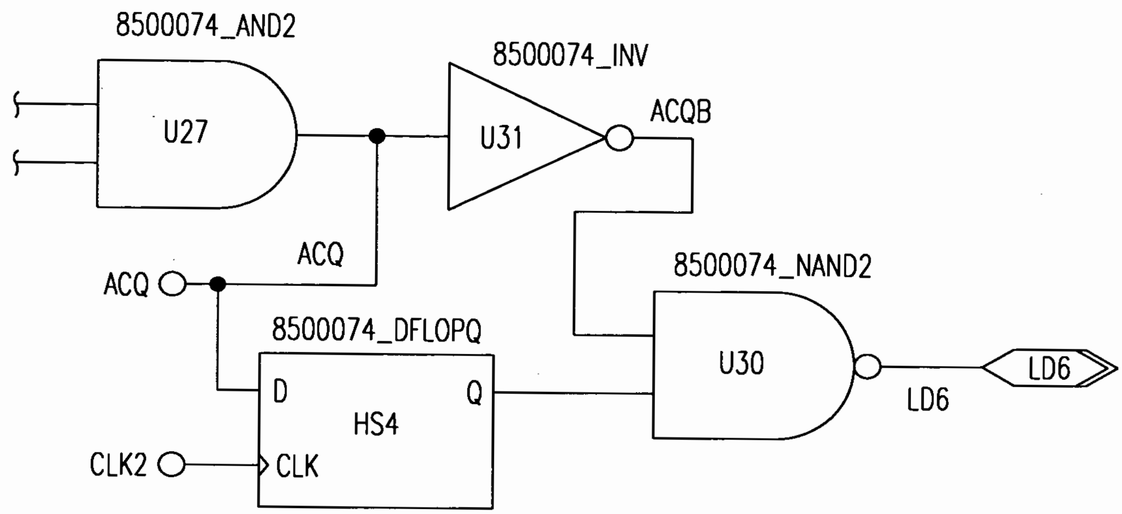

FIG.105E-2

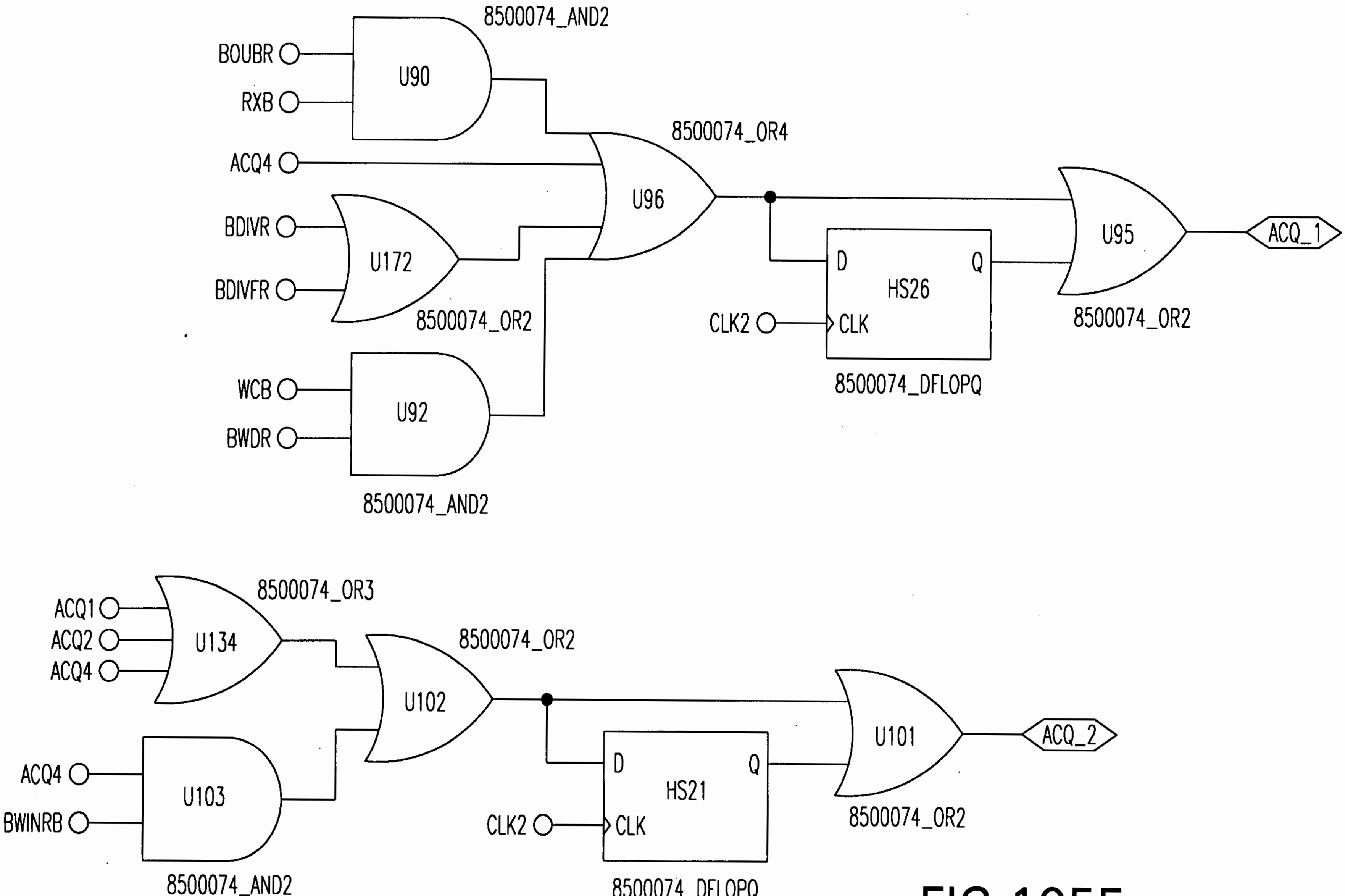

FIG.105F

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Inventors: Sorrells et al.
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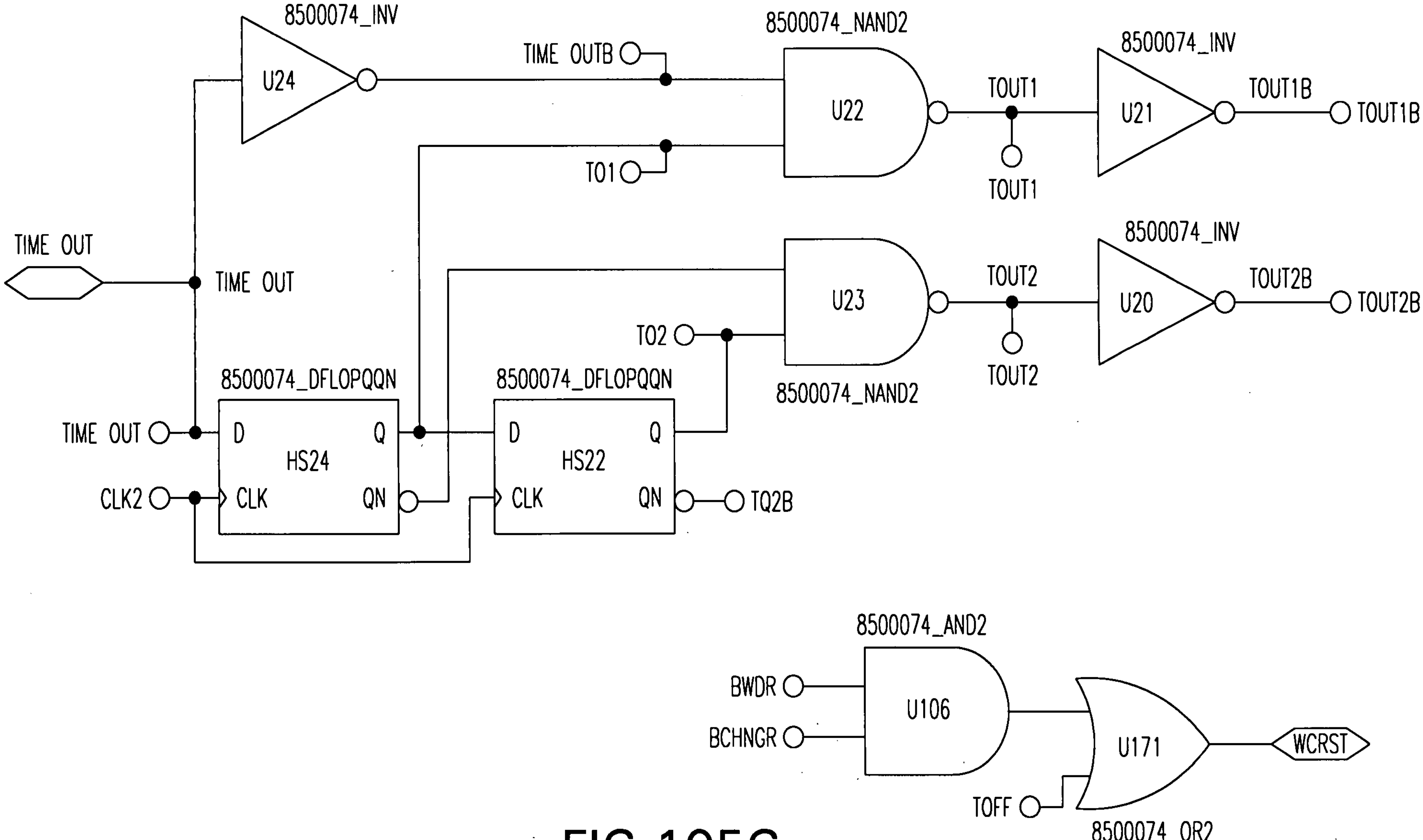

FIG.105G

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Inventors: Sorrells et al.
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Including Multi-Phase Embodiments and Circuit

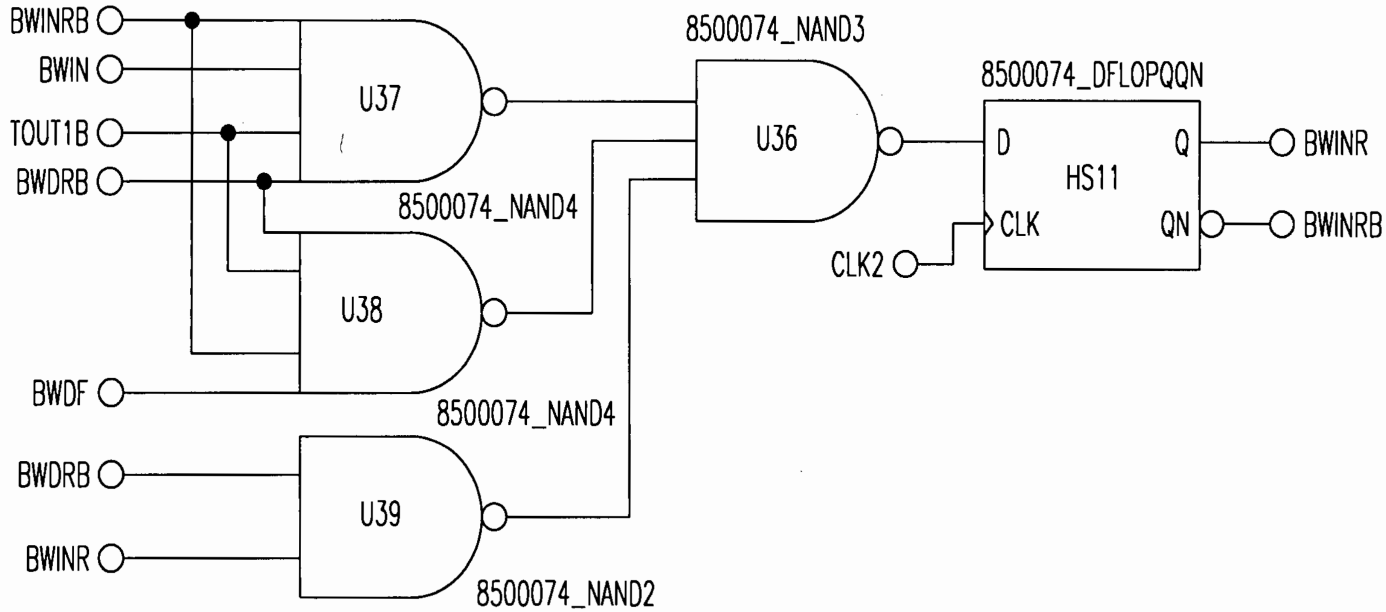

FIG.105H

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Inventors: Sorrells et al.
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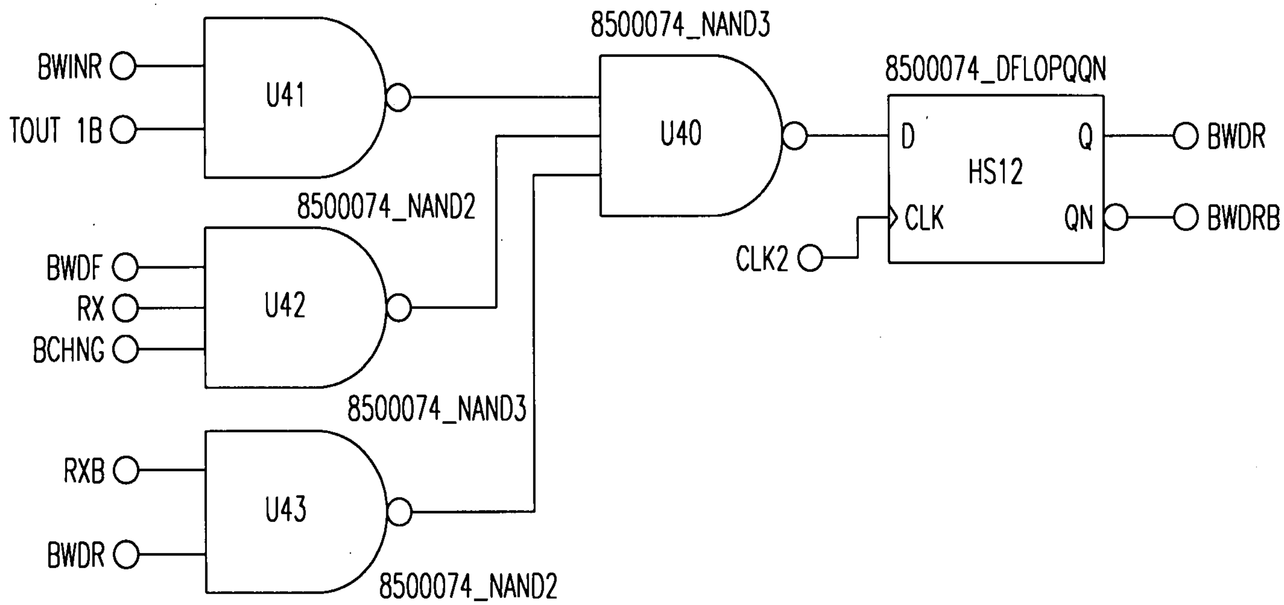

FIG.105I

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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

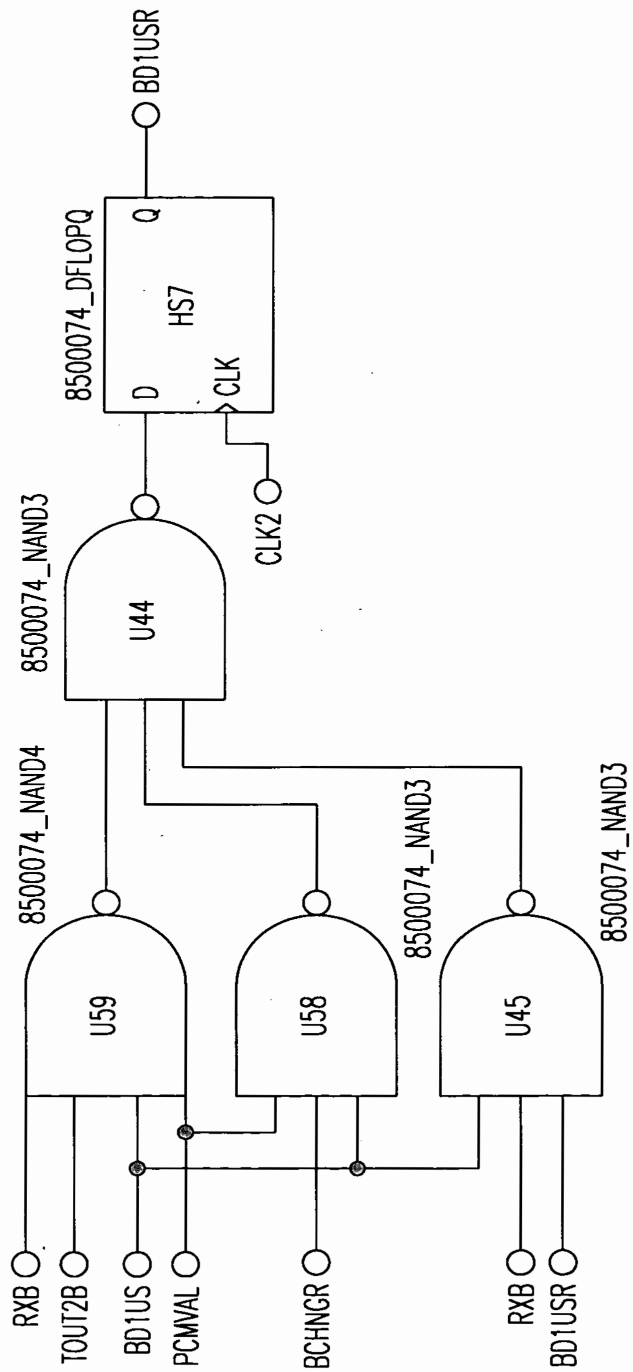

FIG. 105J

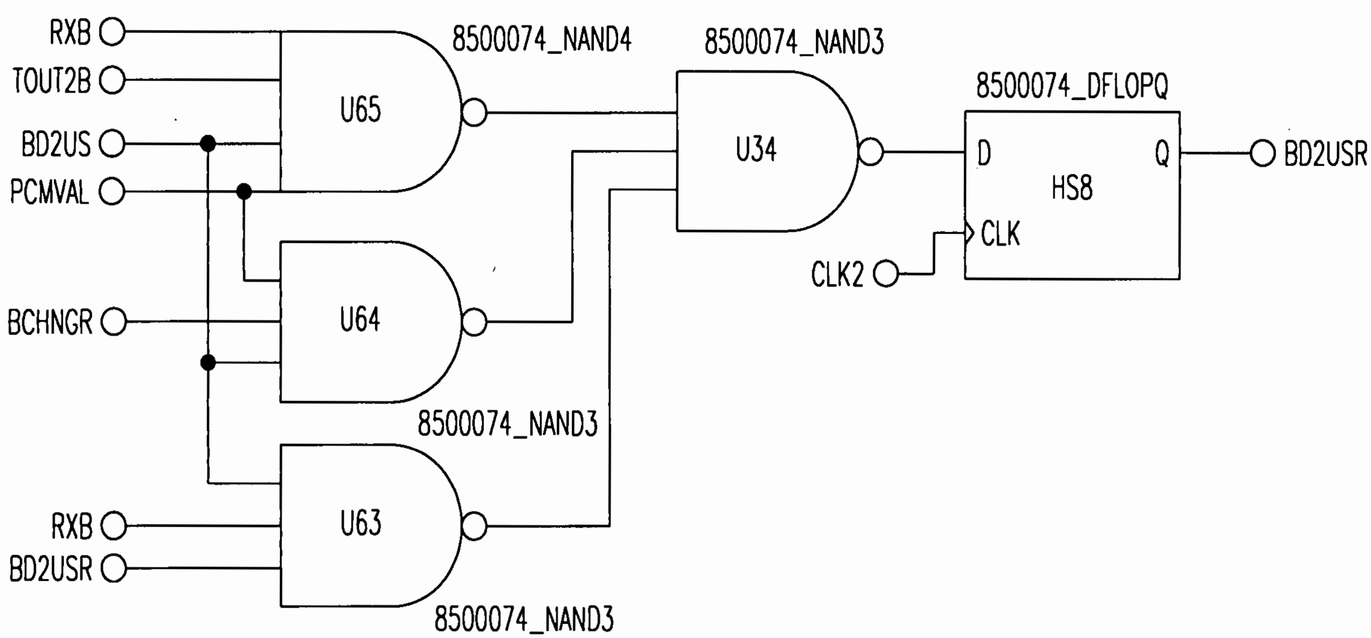

FIG. 105K

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Inventors: Sorrells et al.
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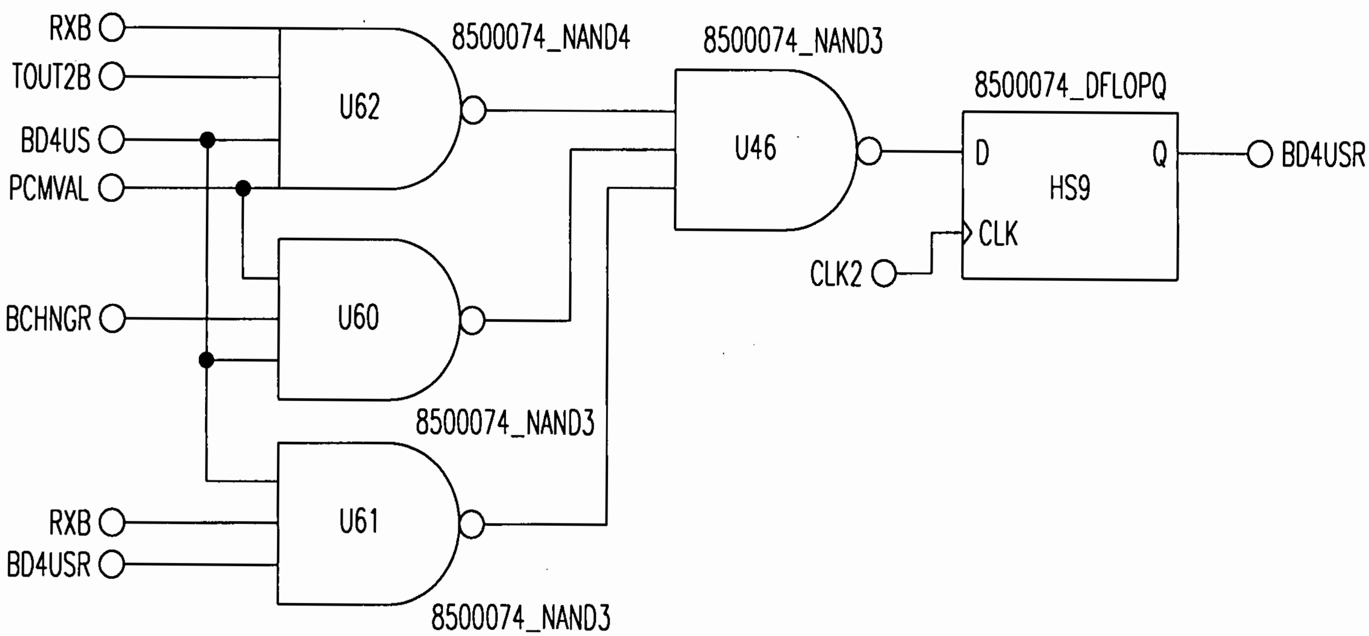

FIG.105L

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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

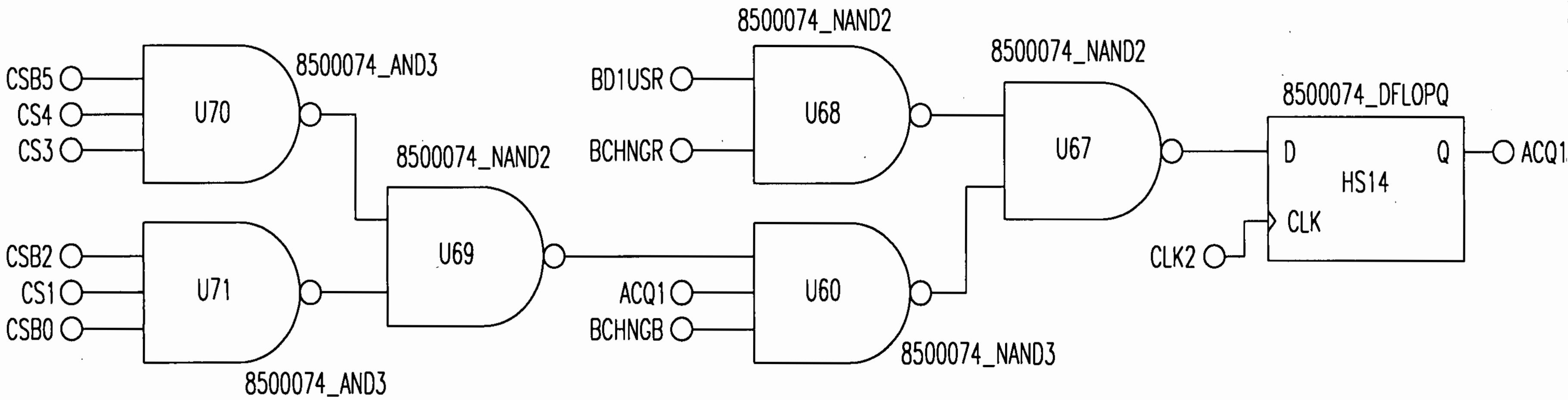

FIG.105M

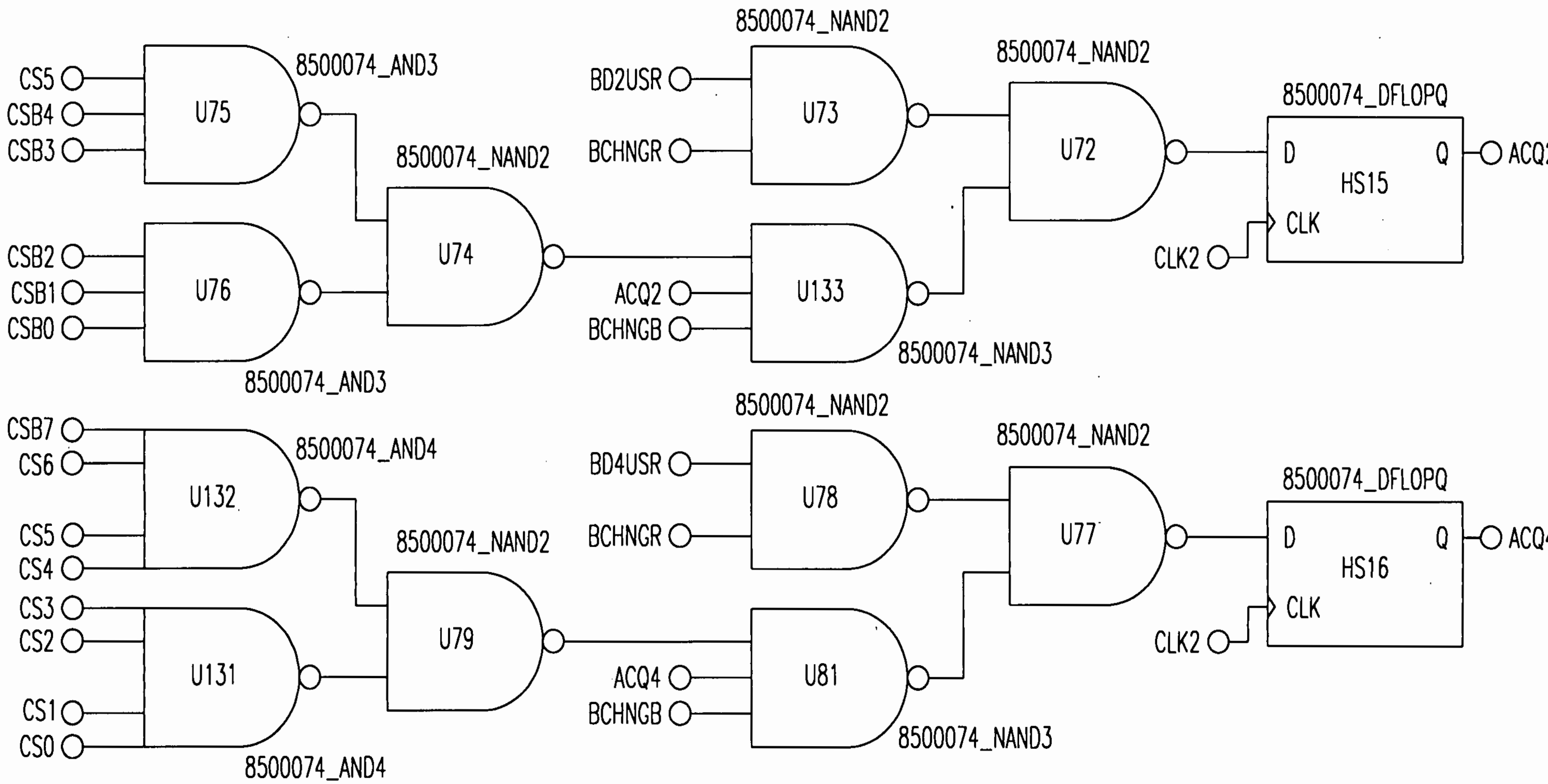

FIG.105N

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Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

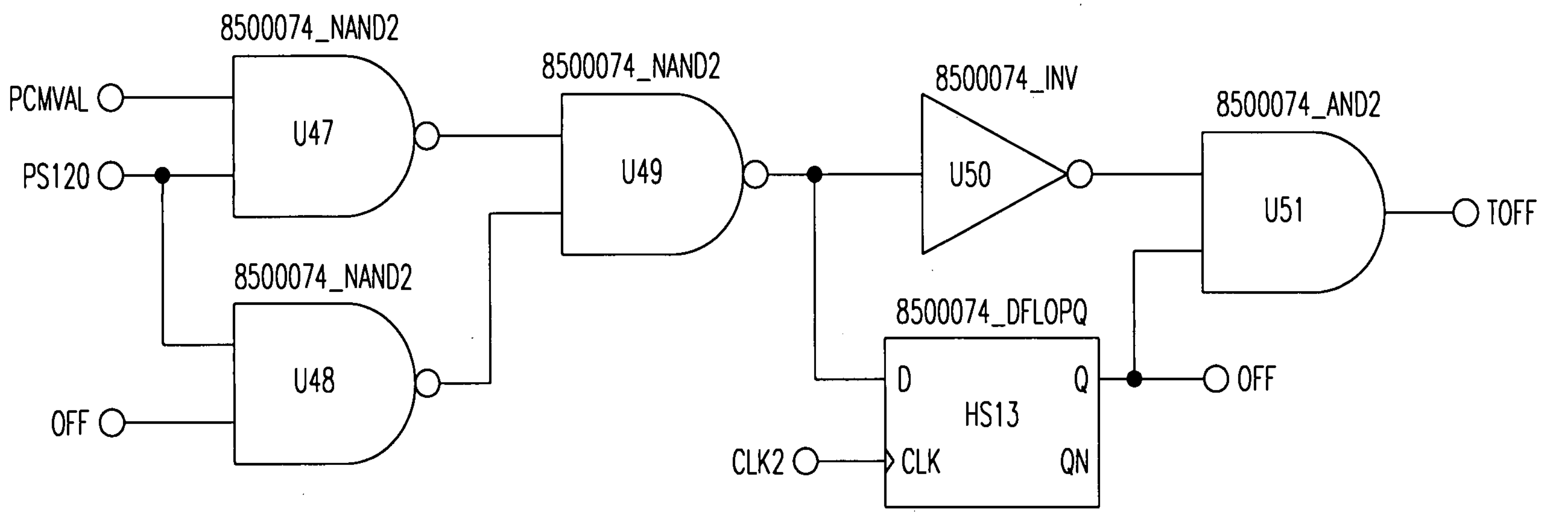

FIG.105O

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Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
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Including Multi-Phase Embodiments and Circuit

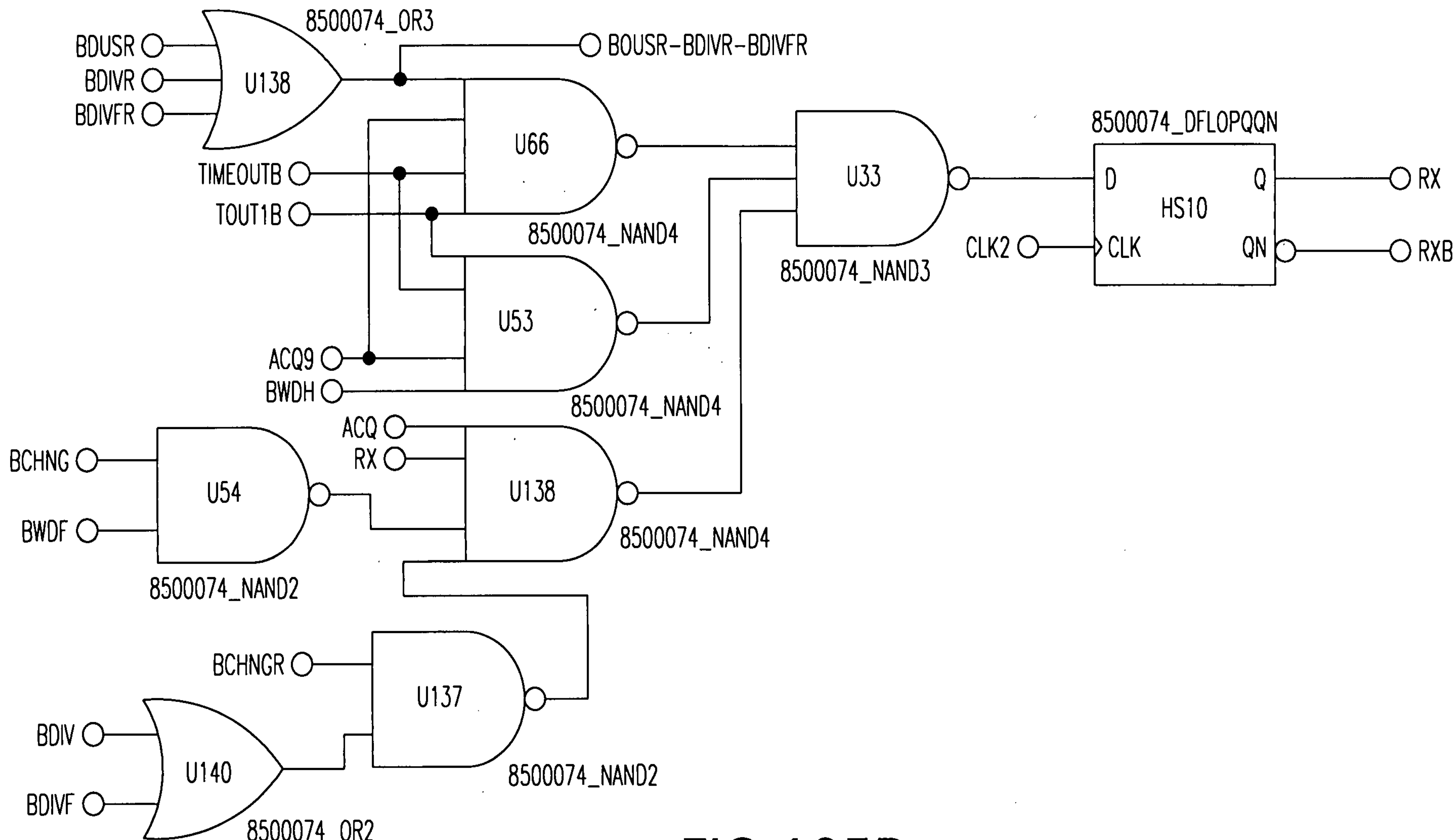

FIG.105P

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Inventors: Sorrells et al.
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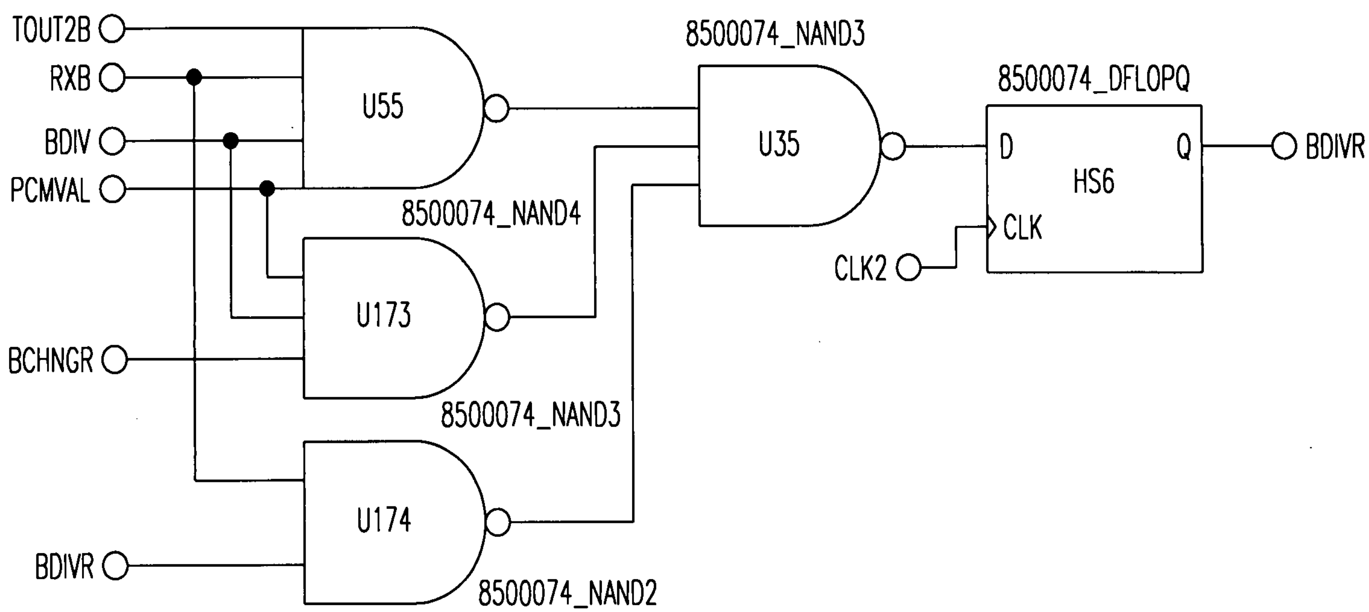

FIG.105Q

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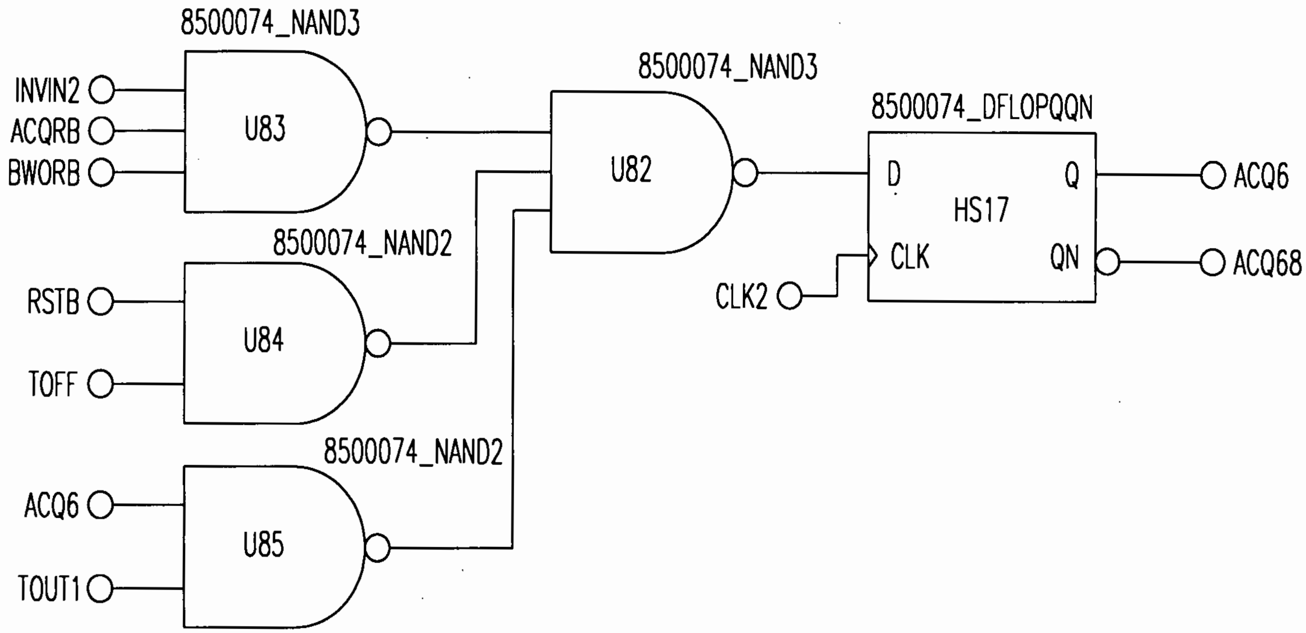

FIG.105R

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Inventors: Sorrells et al.
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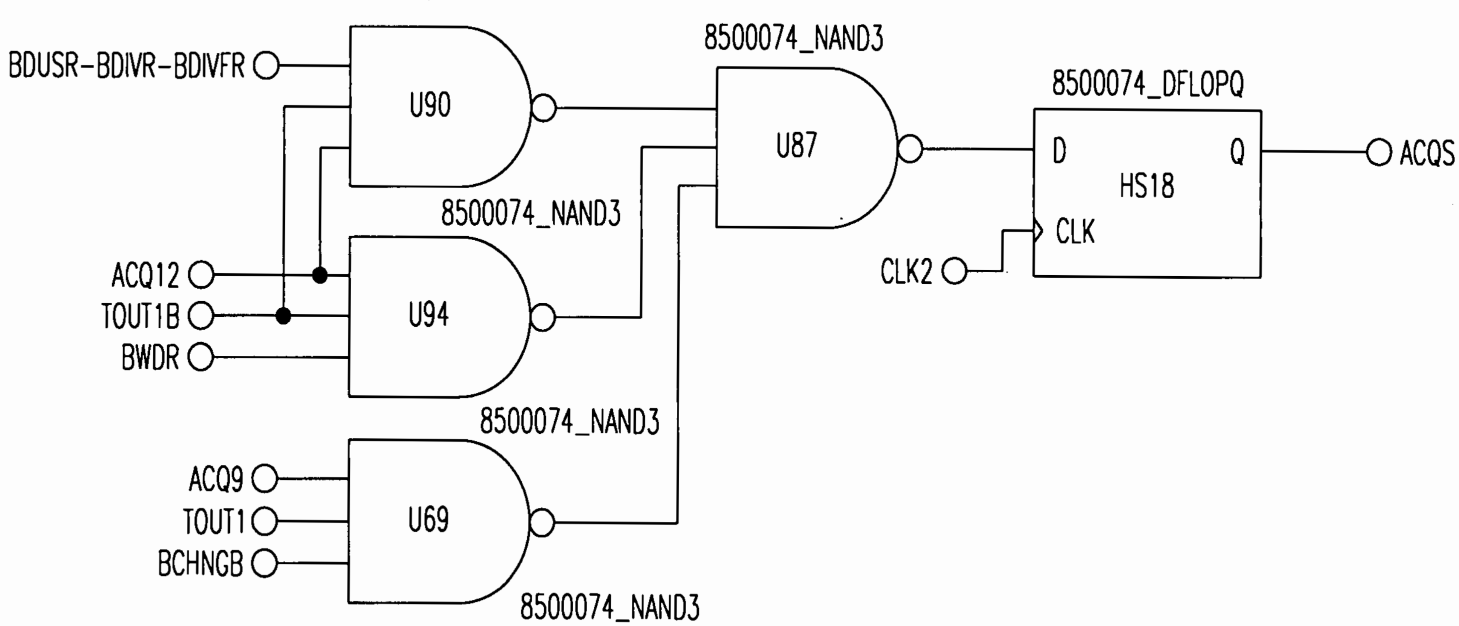

FIG.105S

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Inventors: Sorrells et al.
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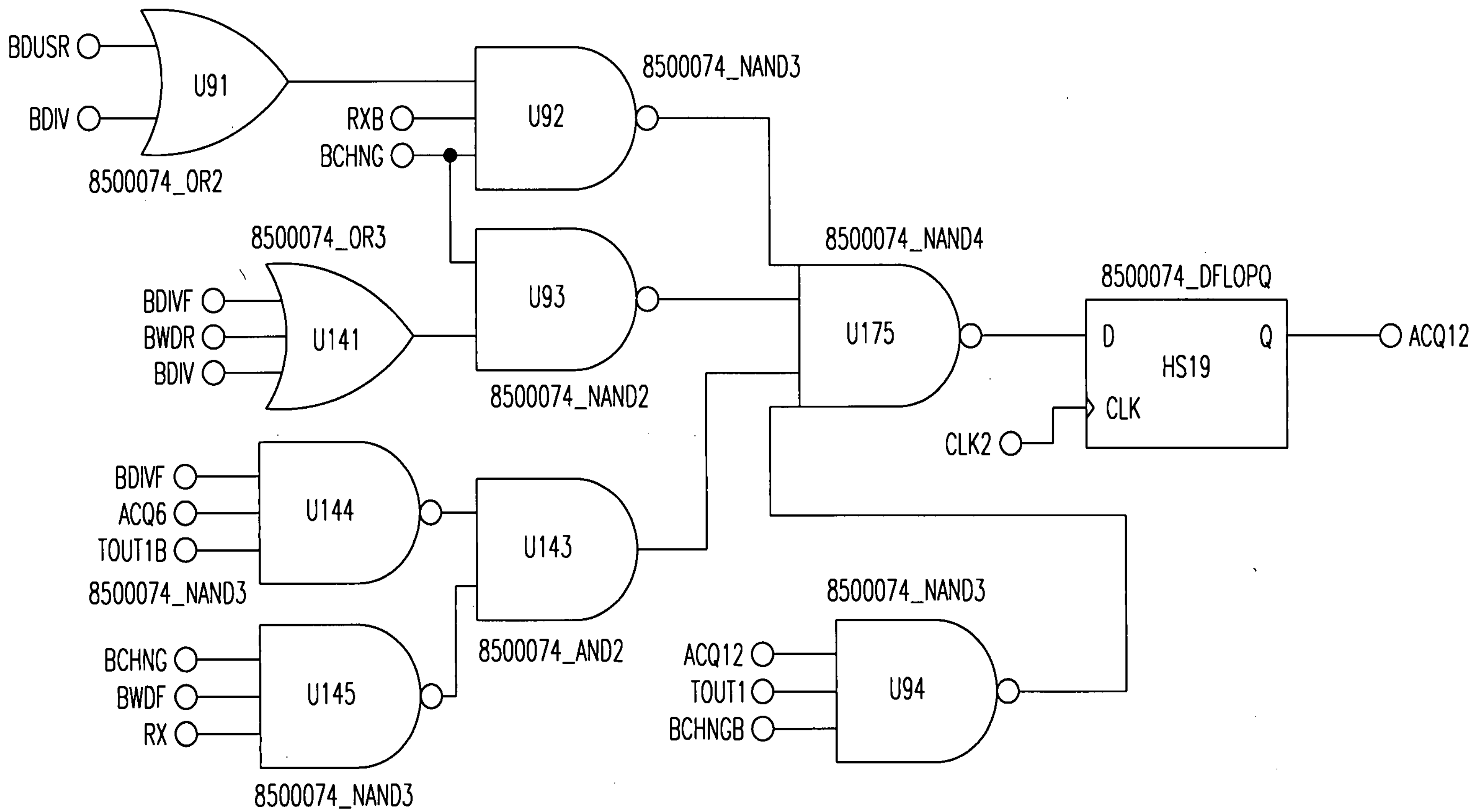

FIG.105T

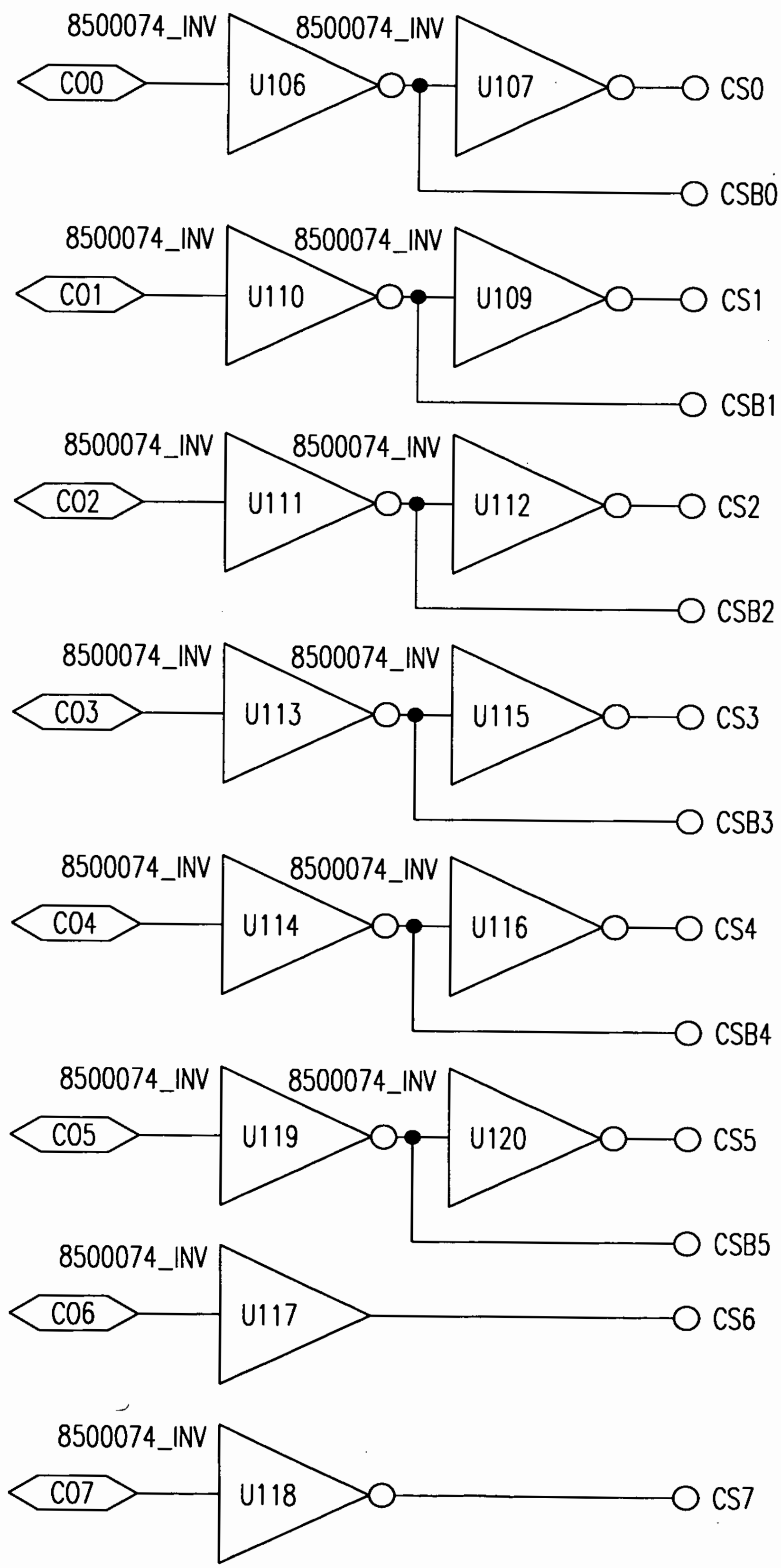
8500074_INV
8500074_INV
C00
U106
U107
CS0
CSB0
8500074_INV
8500074_INV
C01
U110
U109
CS1
CSB1
8500074_INV
8500074_INV
C02
U111
U112
CS2
CSB2
8500074_INV
8500074_INV
C03
U113
U115
CS3
CSB3
8500074_INV
8500074_INV
C04
U114
U116
CS4
CSB4
8500074_INV
8500074_INV
C05
U119
U120
CS5
CSB5
8500074_INV
C06
U117
CS6
8500074_INV
C07
U118
CS7

FIG.105U

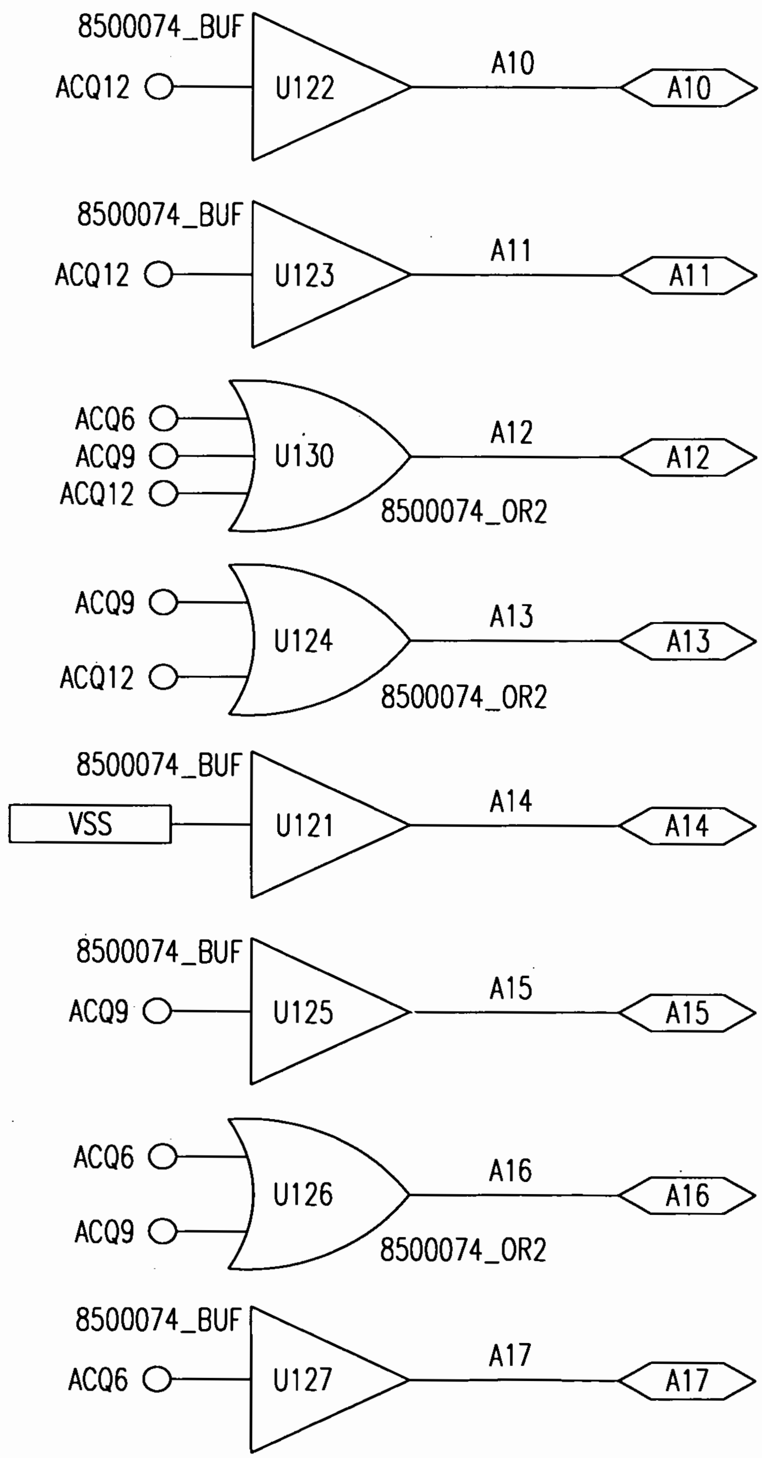
8500074_BUF
ACQ12
U122
A10
A10
8500074_BUF
ACQ12
U123
A11
A11
ACQ6
ACQ9
ACQ12
U130
A12
8500074_OR2
A12
ACQ9
ACQ12
U124
A13
8500074_OR2
A13
8500074_BUF
VSS
U121
A14
A14
8500074_BUF
ACQ9
U125
A15
A15
ACQ6
ACQ9
U126
A16
8500074_OR2
A16
8500074_BUF
ACQ6
U127
A17
A17

FIG.105V

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Inventors: Sorrells et al.
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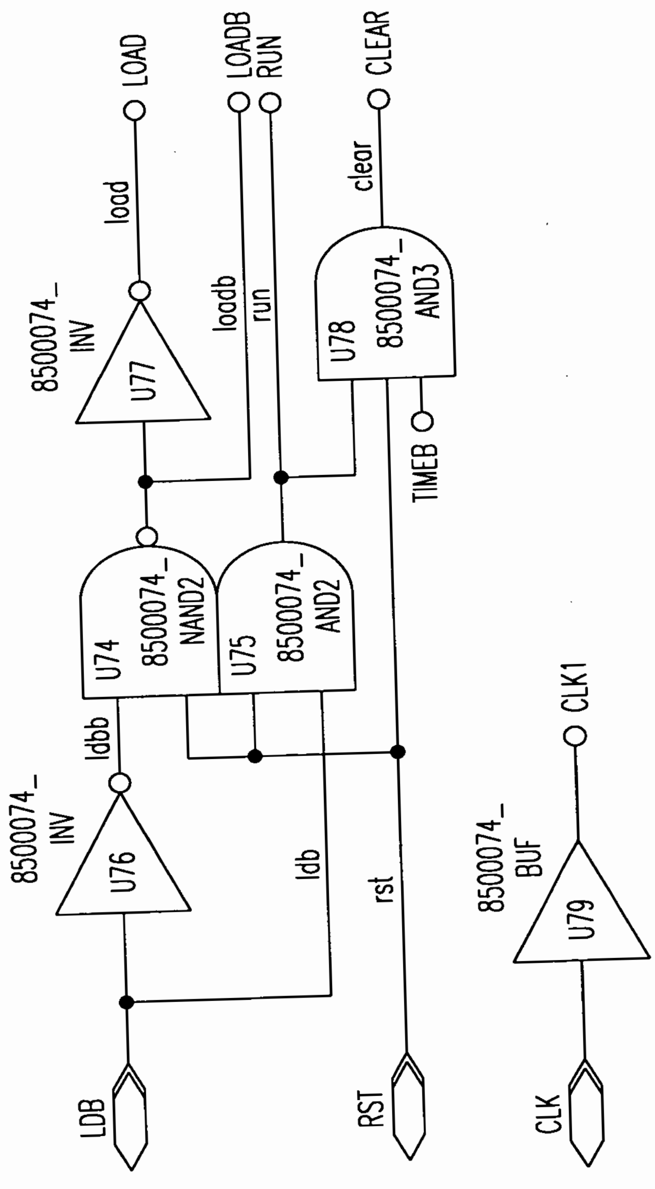

FIG.106A

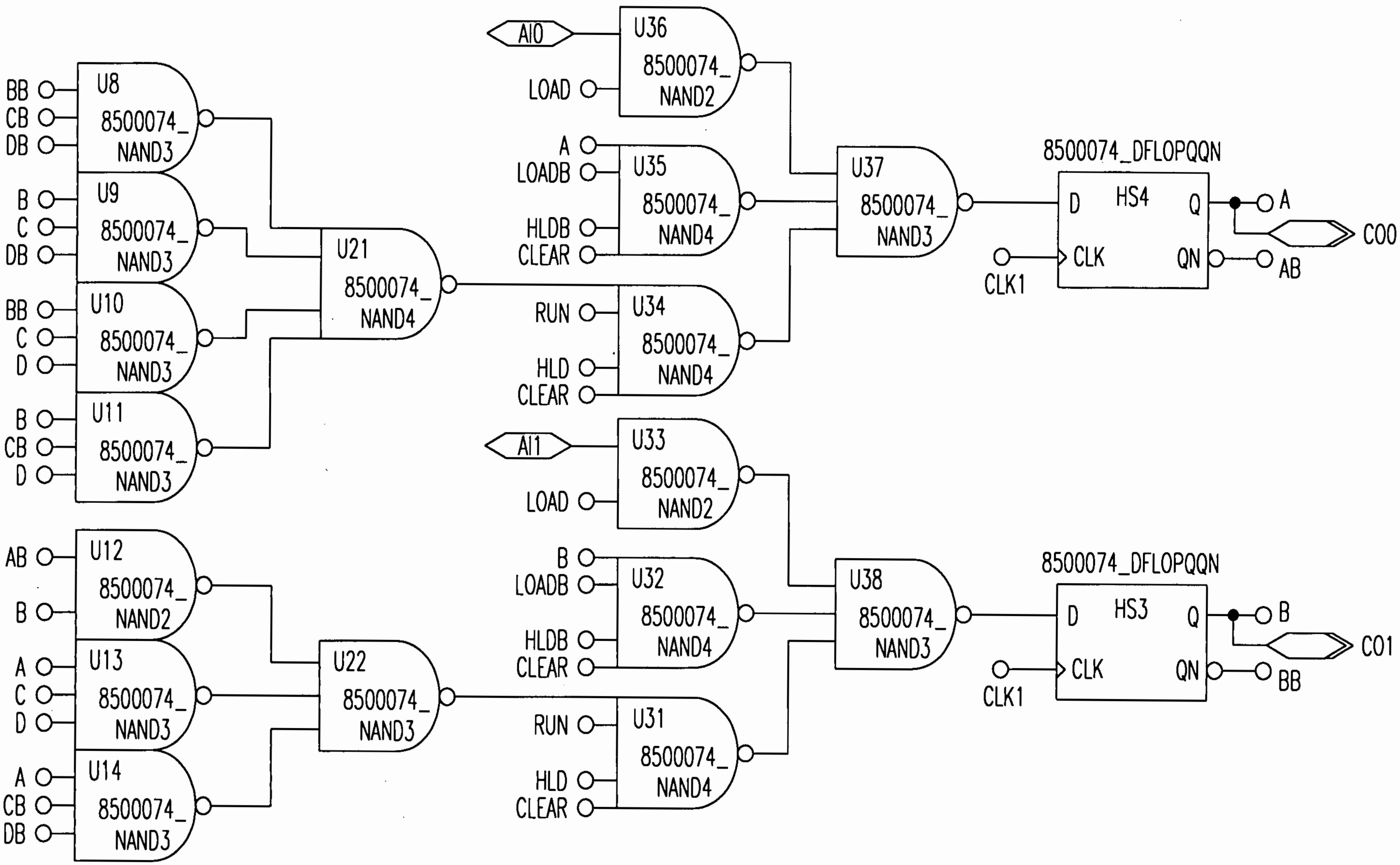

FIG.106B

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Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

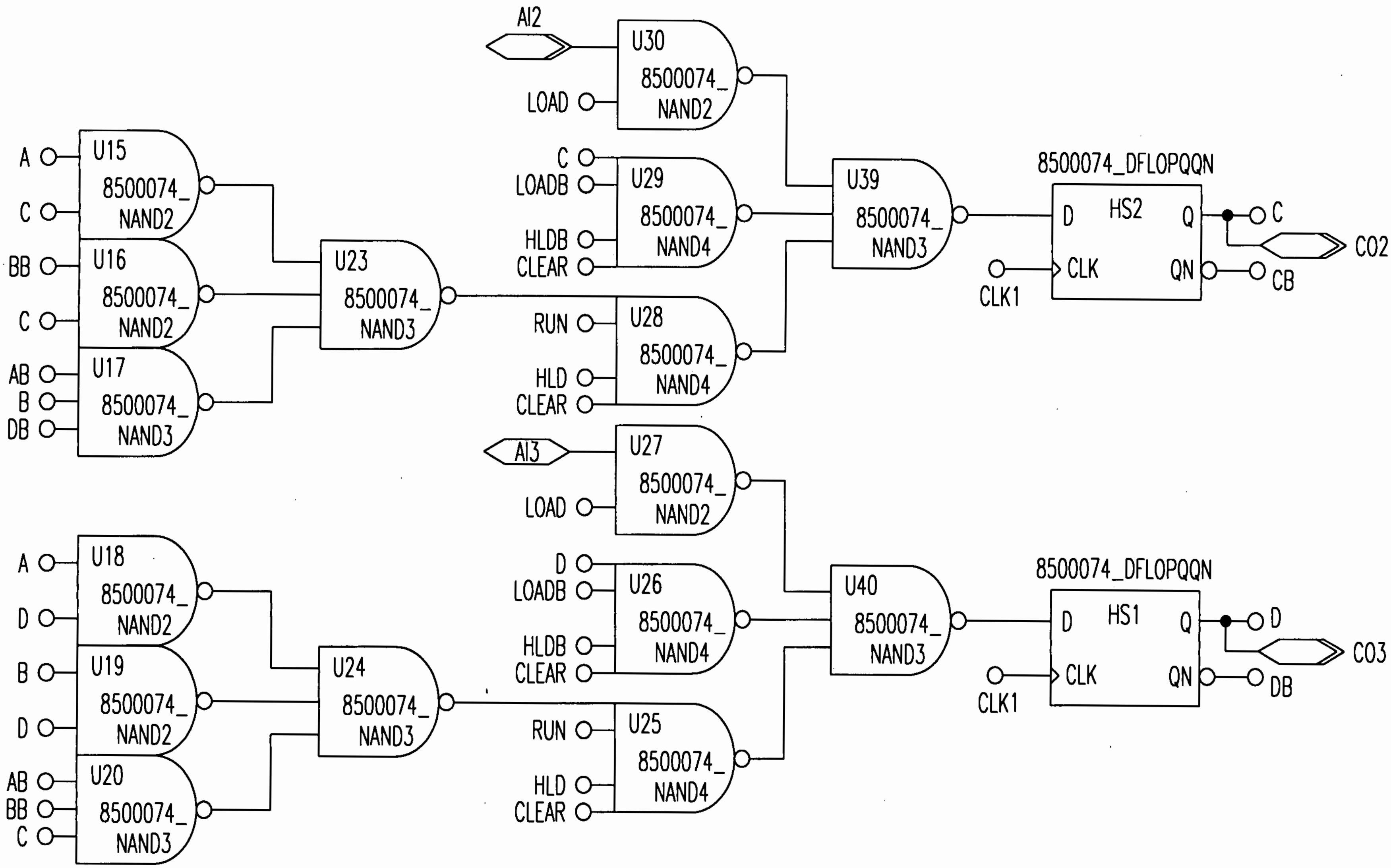

FIG.106C

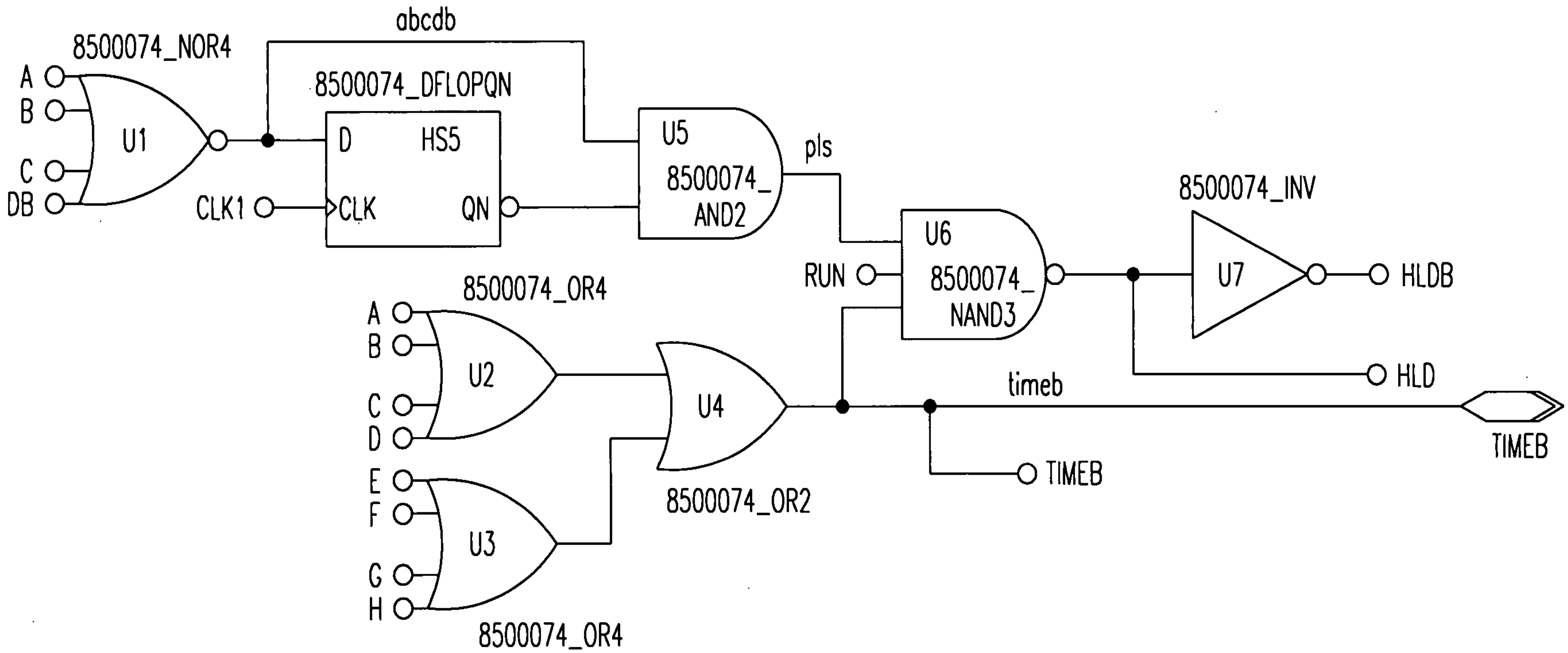

FIG.106D

New Sheet
Sheet 230 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

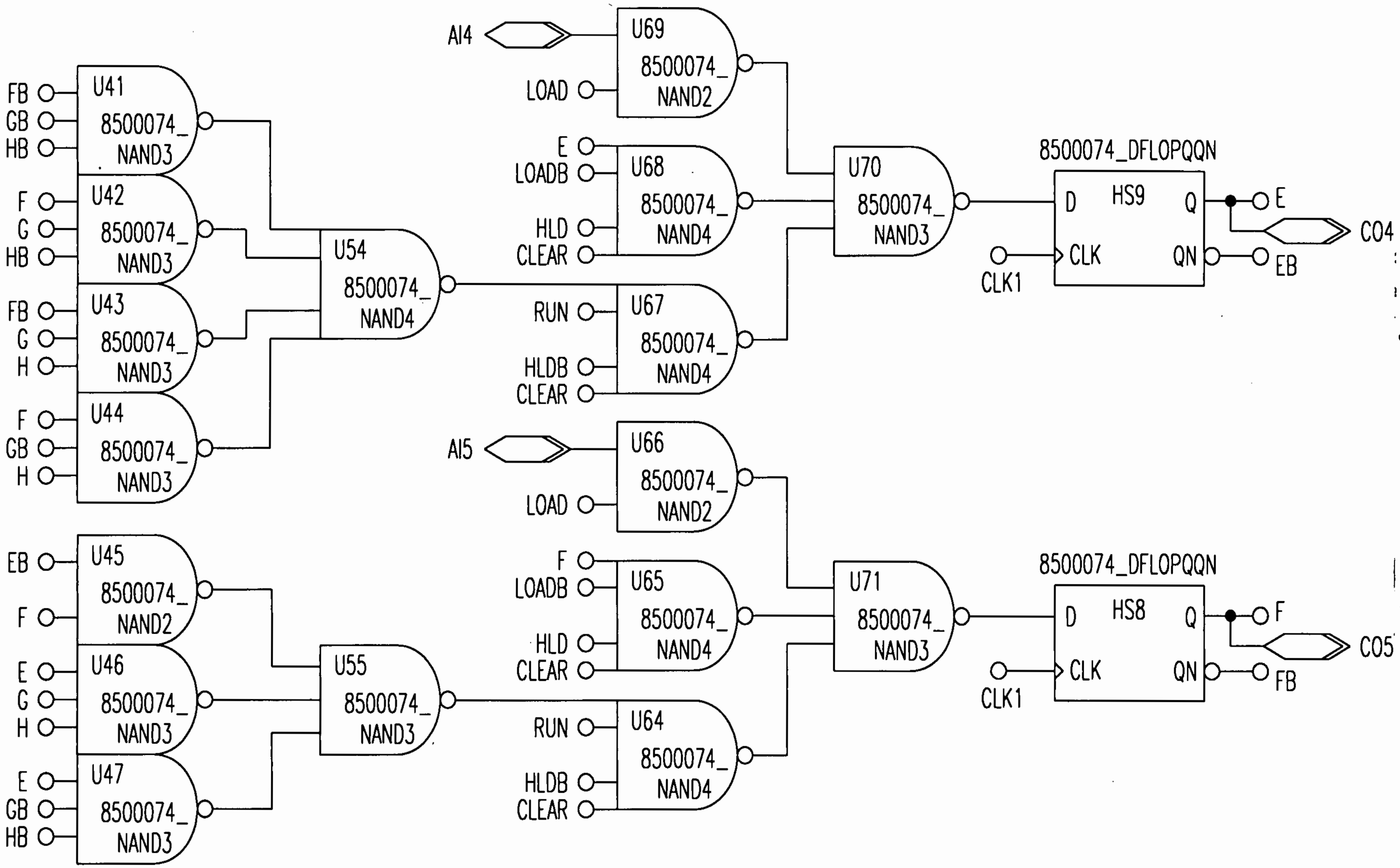

FIG. 106E

New Sheet
Sheet 231 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

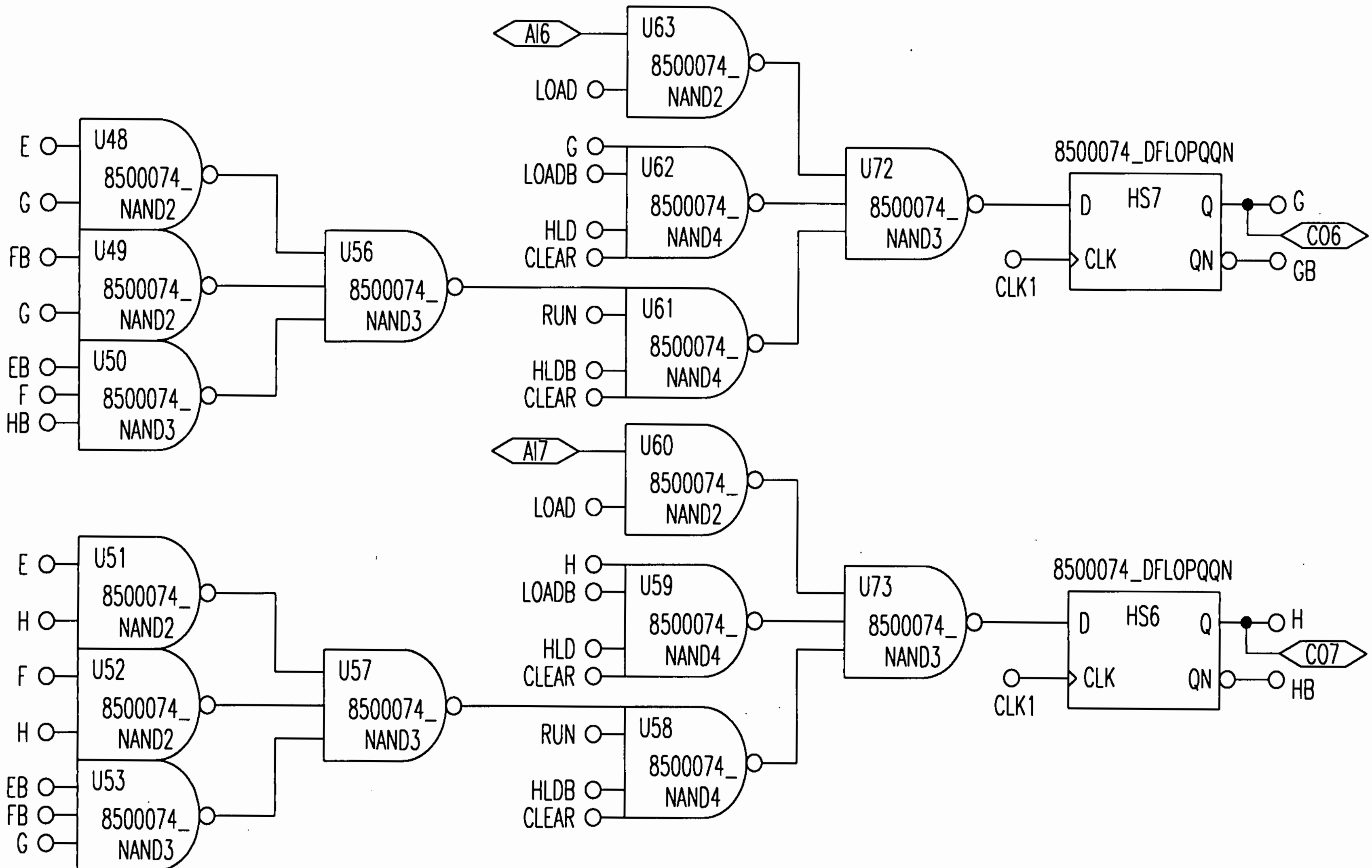

FIG.106F

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Sheet 232 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
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Replacement Sheet
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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

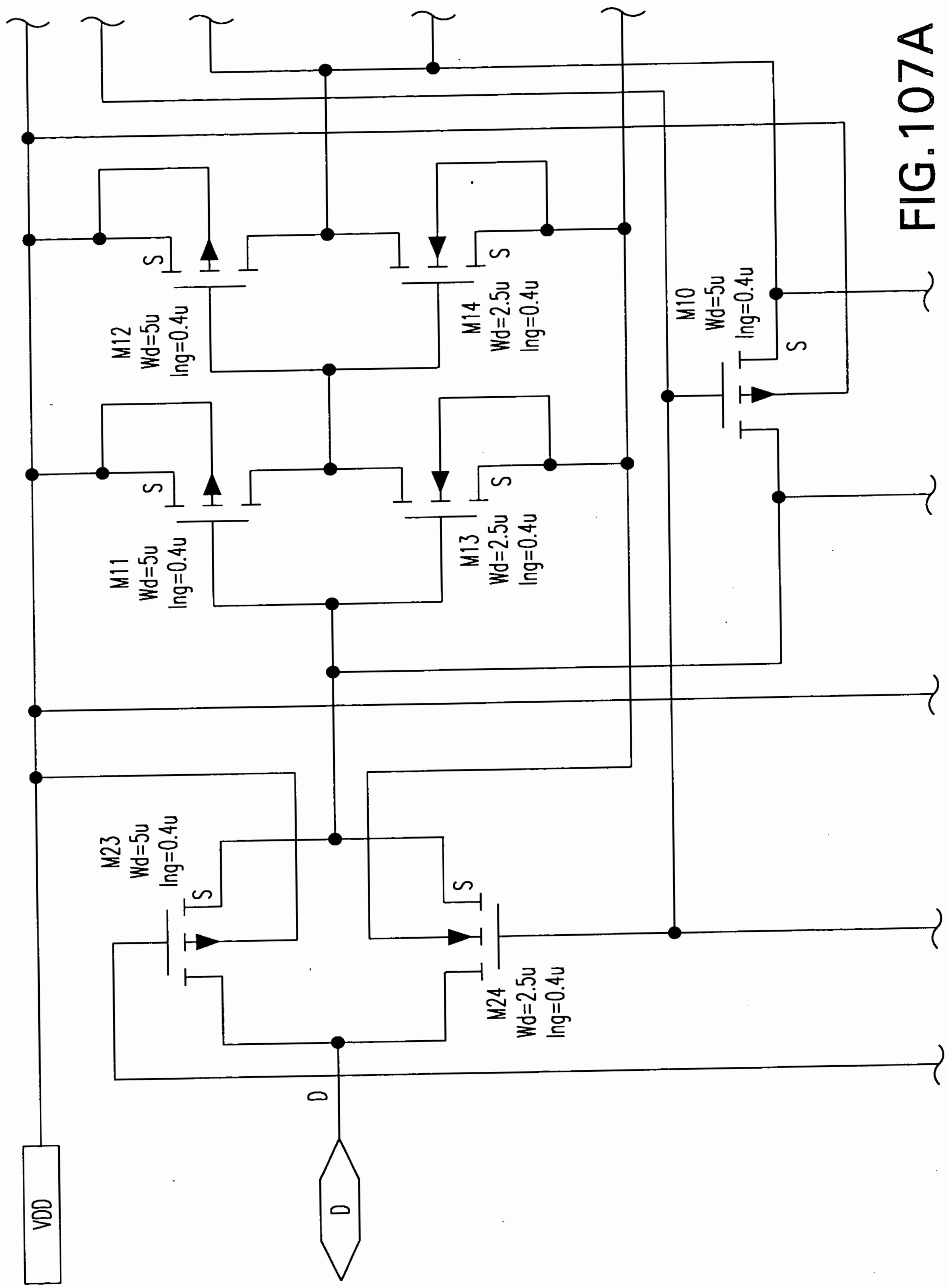

FIG.107A

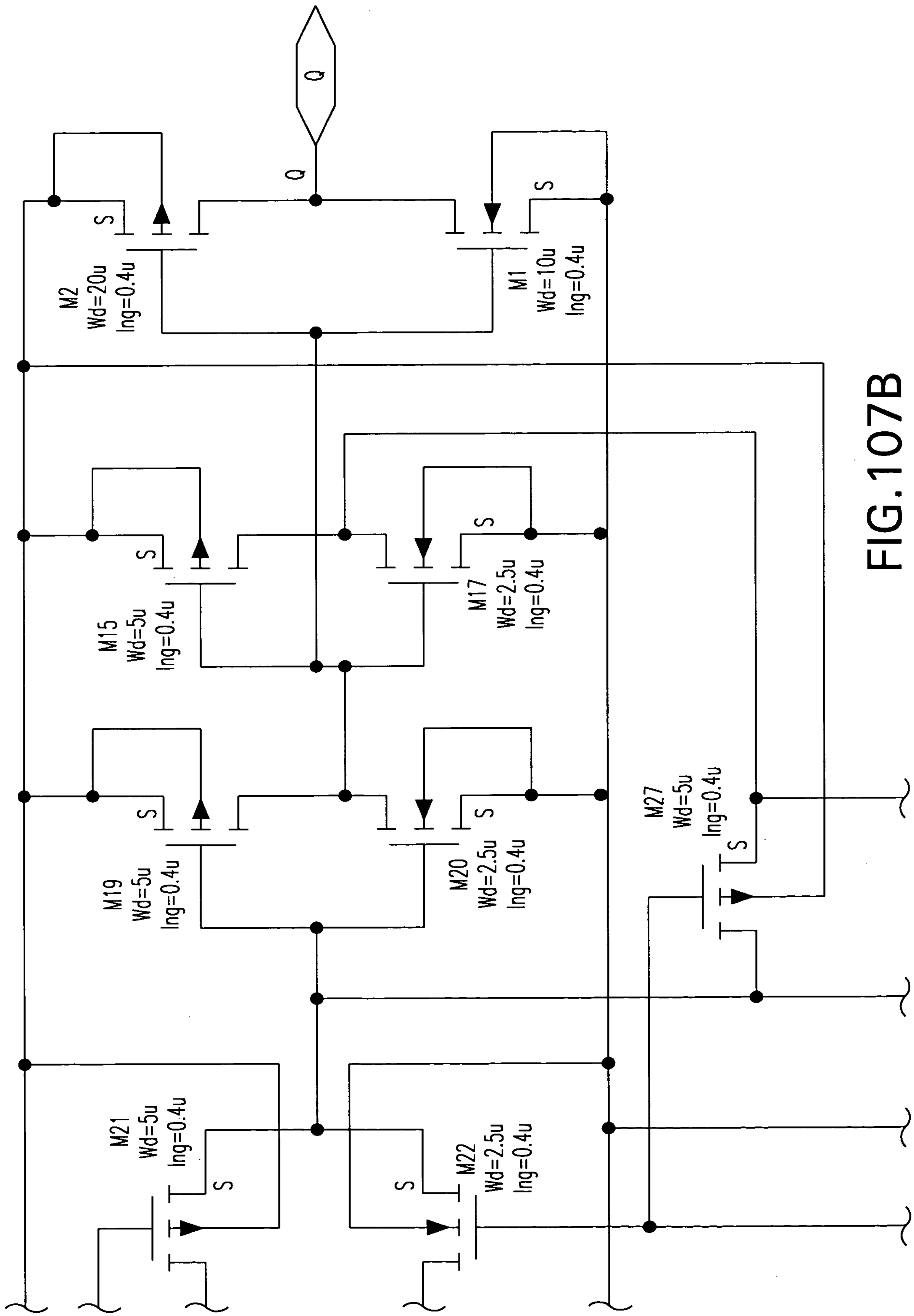
Q
Q
S
M2
Wd=20u
lng=0.4u
S
M1
Wd=10u
lng=0.4u
S
M15
Wd=5u
lng=0.4u
S
M17
Wd=2.5u
lng=0.4u
S
M19
Wd=5u
lng=0.4u
S
M20
Wd=2.5u
lng=0.4u
M27
Wd=5u
lng=0.4u
S
M21
Wd=5u
lng=0.4u
S
S
M22
Wd=2.5u
lng=0.4u

FIG.107B

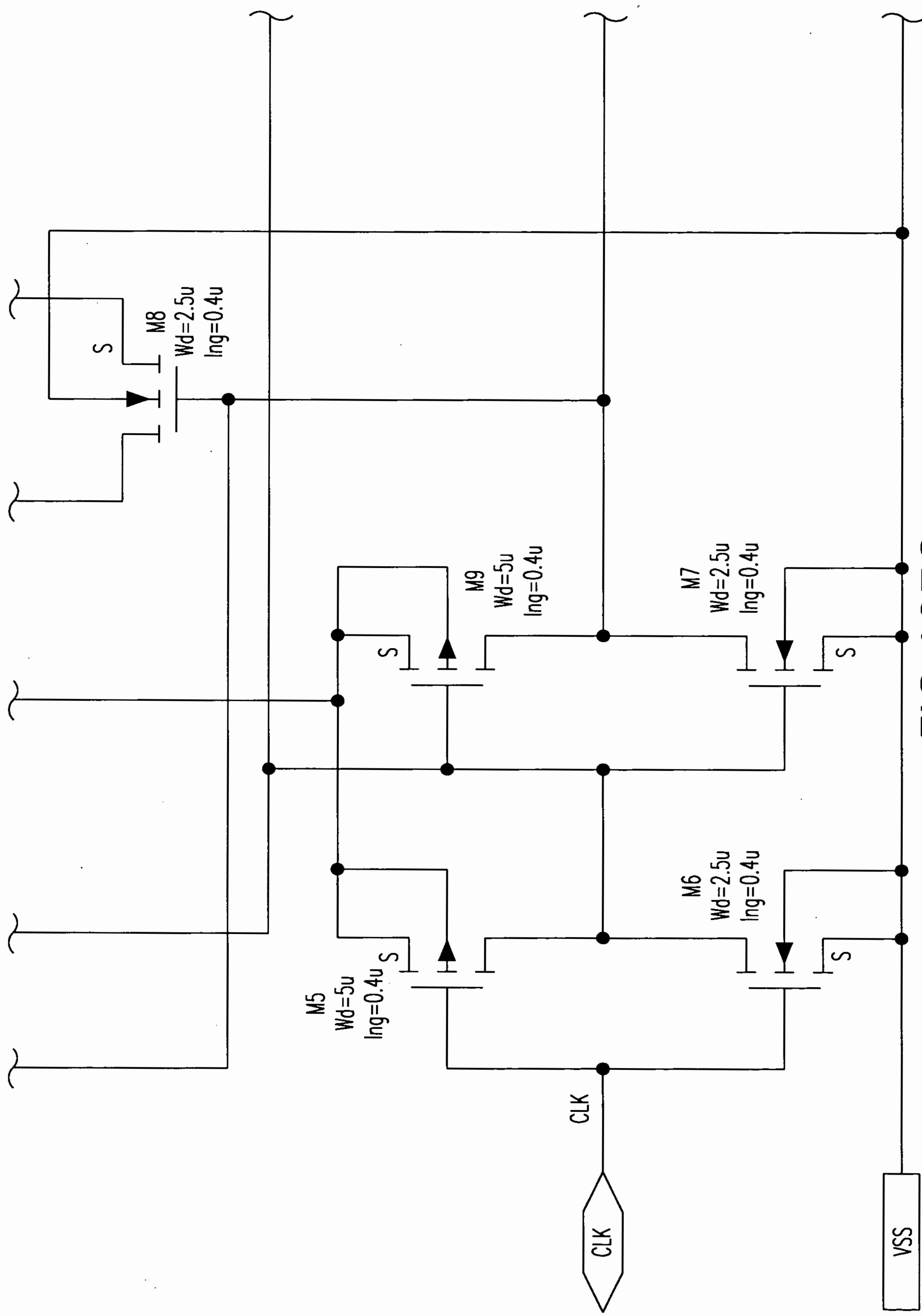
S
M8
Wd=2.5u
lng=0.4u
S
M9
Wd=5u
lng=0.4u
M7
Wd=2.5u
lng=0.4u
S
S
M5
Wd=5u
lng=0.4u
M6
Wd=2.5u
lng=0.4u
S
CLK
CLK
VSS

FIG.107C

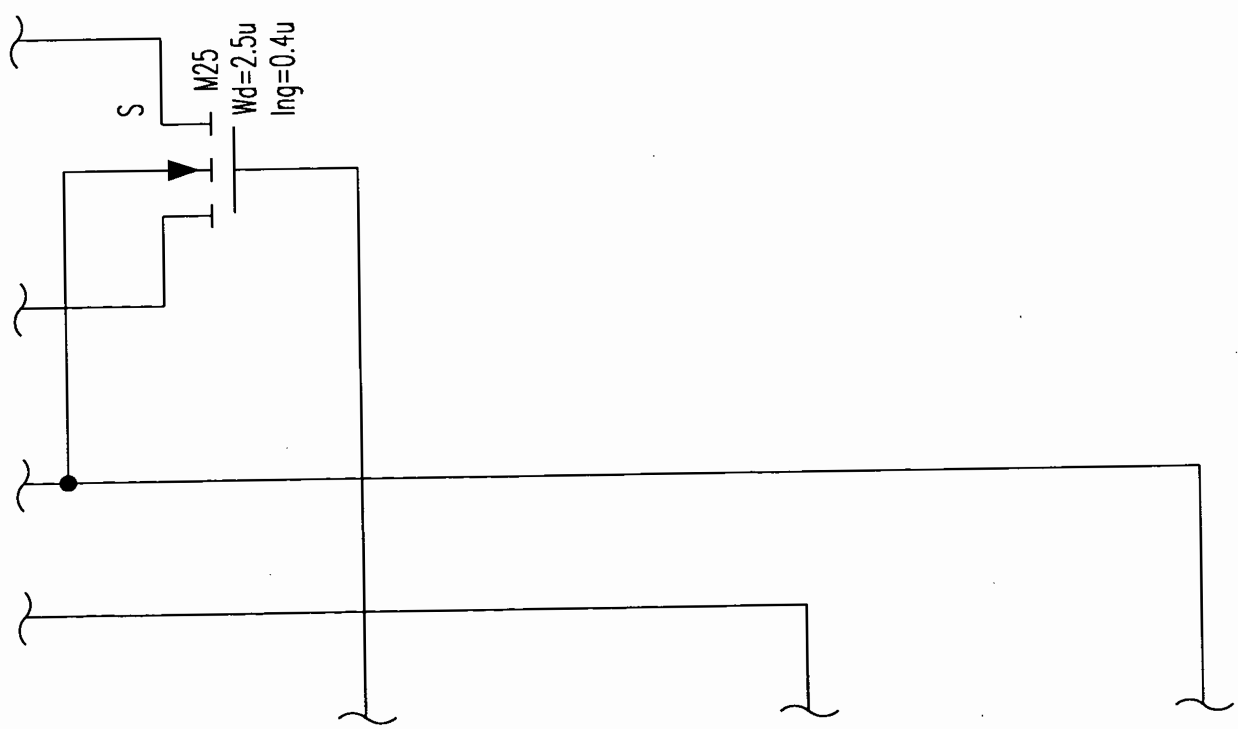

FIG.107D

Replacement Sheet
Sheet 237 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

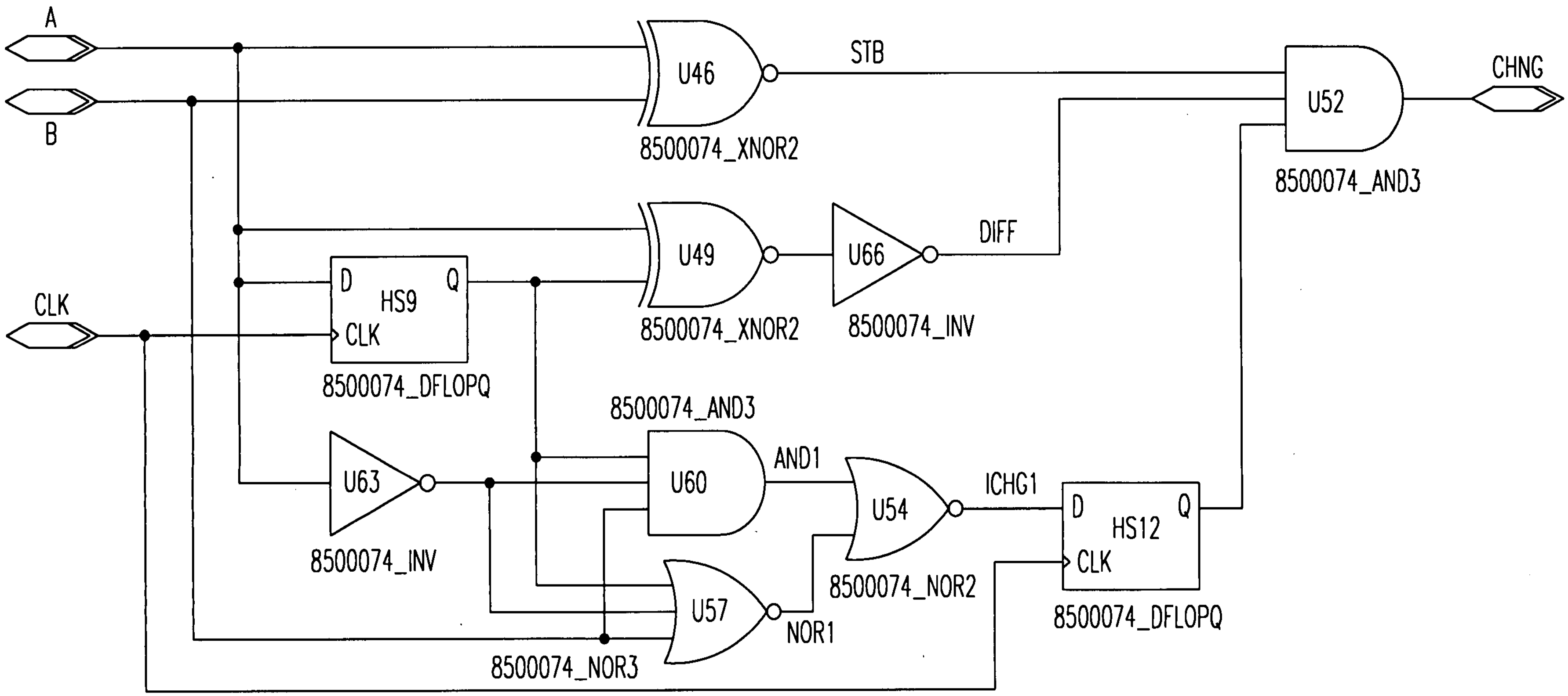

FIG.108

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Sheet 238 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

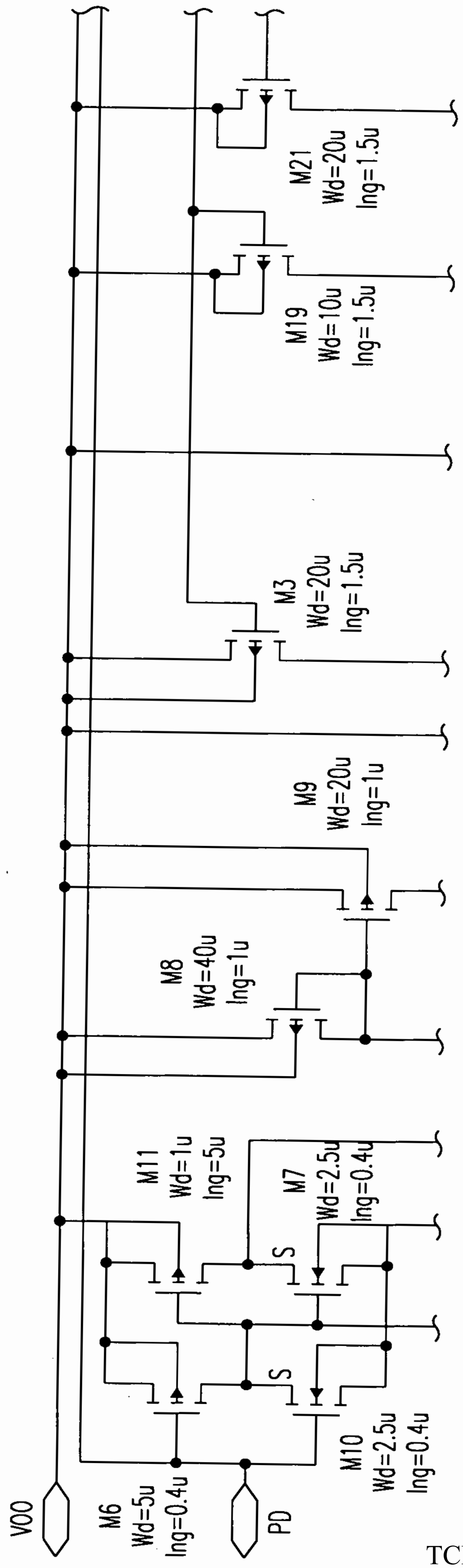

FIG.109A

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

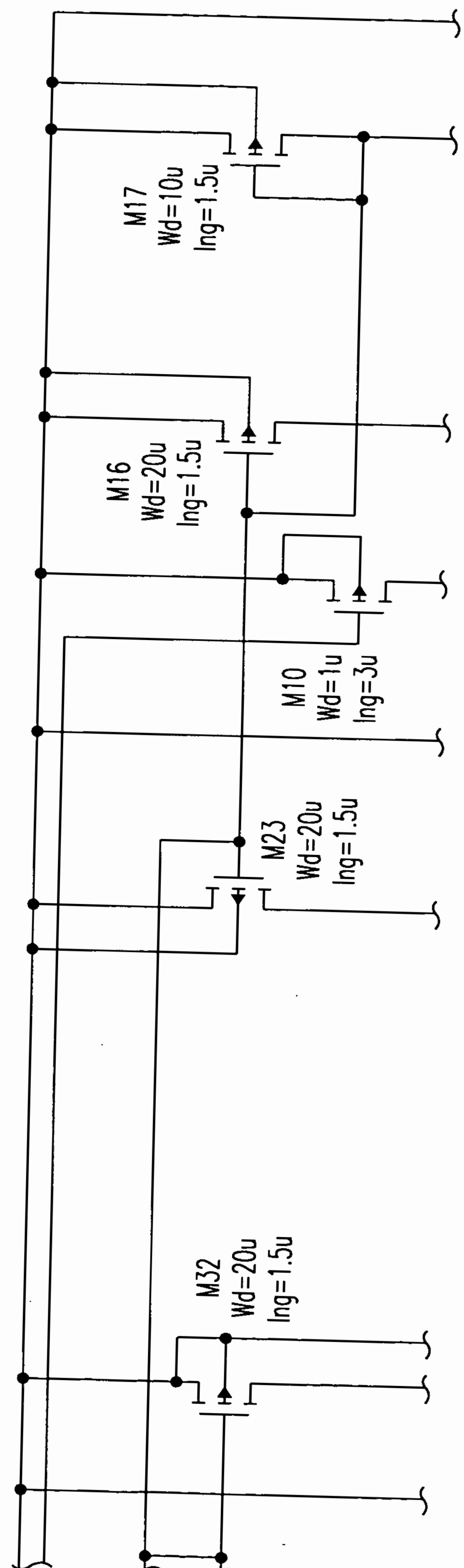

FIG.109B

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

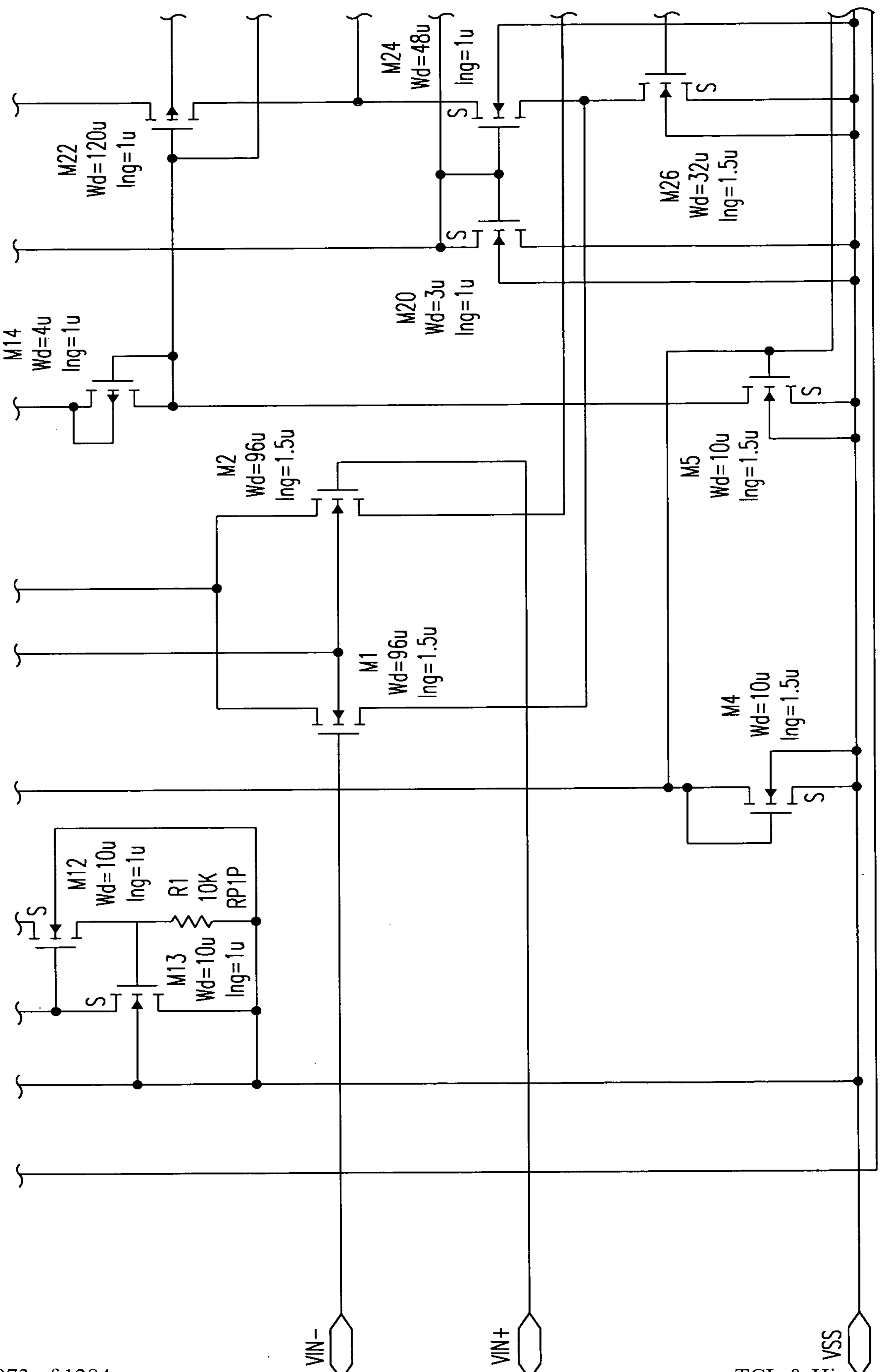

FIG. 109C

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Sheet 241 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

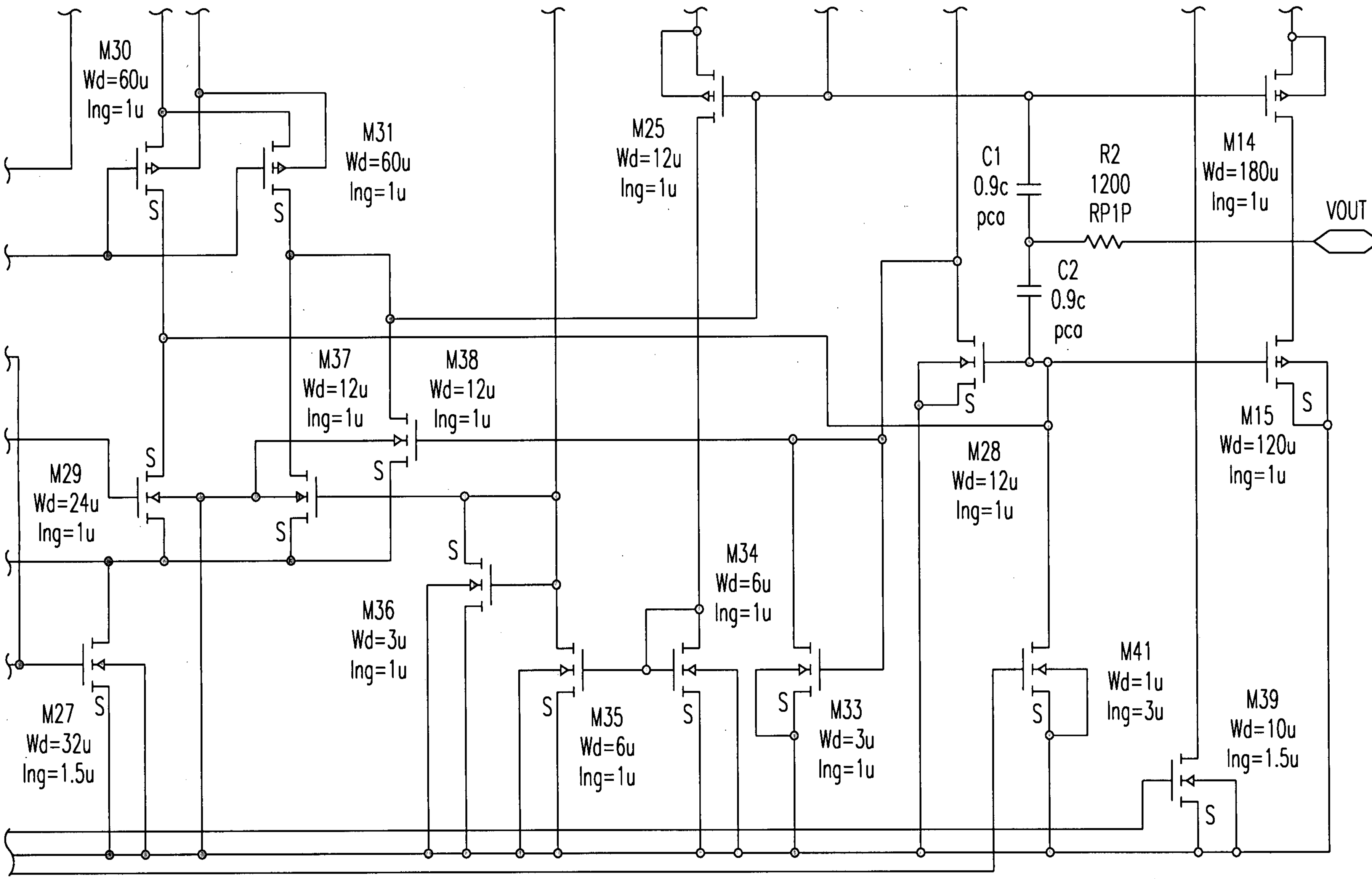

FIG. 109D

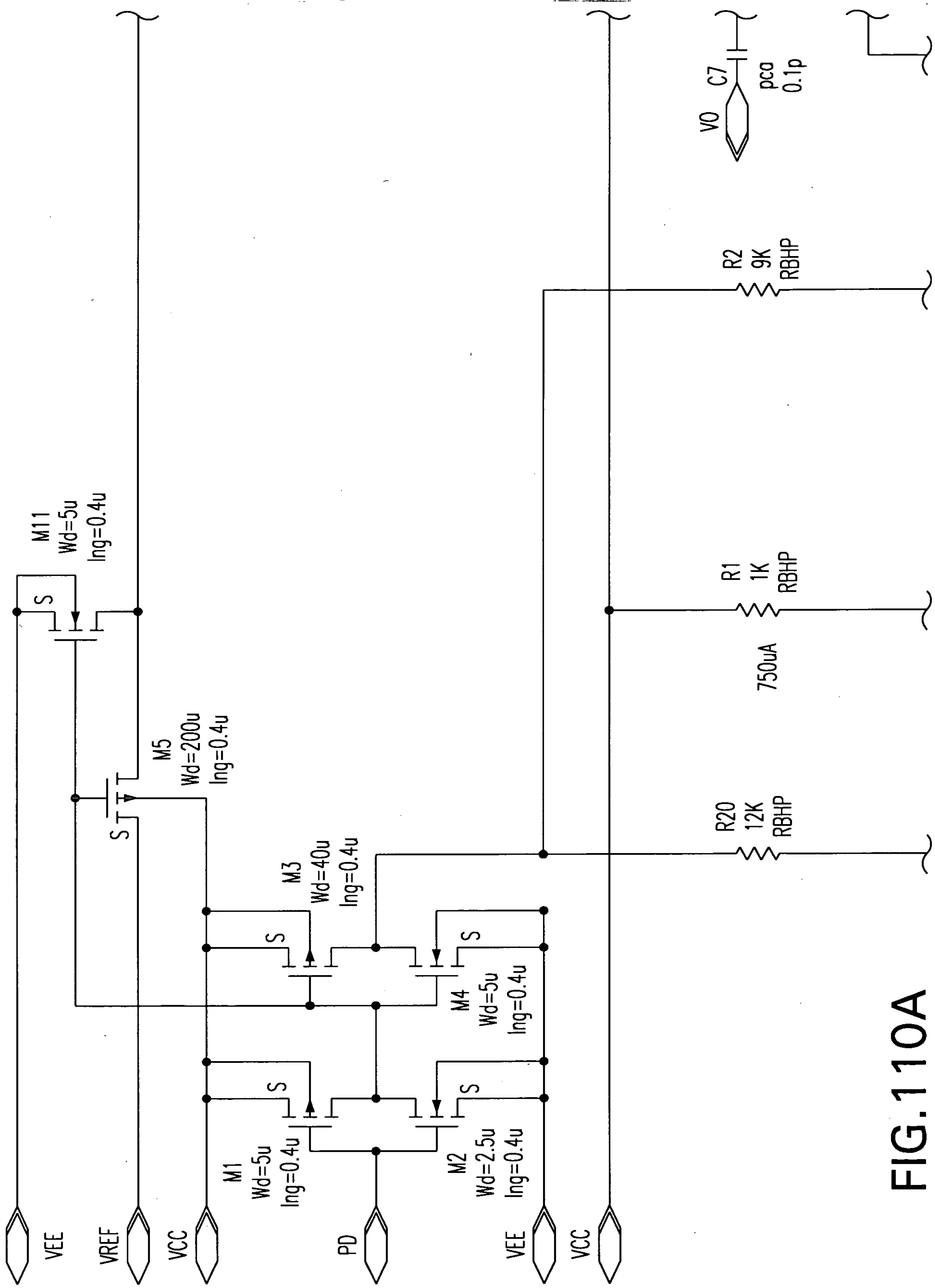
VO
C7
pca
0.1p
R2
9K
RBHP
R1
1K
RBHP
750uA
R20
12K
RBHP
M11
Wd=5u
lng=0.4u
M5
Wd=200u
lng=0.4u
M3
Wd=40u
lng=0.4u
M4
Wd=5u
lng=0.4u
M1
Wd=5u
lng=0.4u
M2
Wd=2.5u
lng=0.4u
S
VEE
VREF
VCC
PD
VEE
VCC

FIG.110A

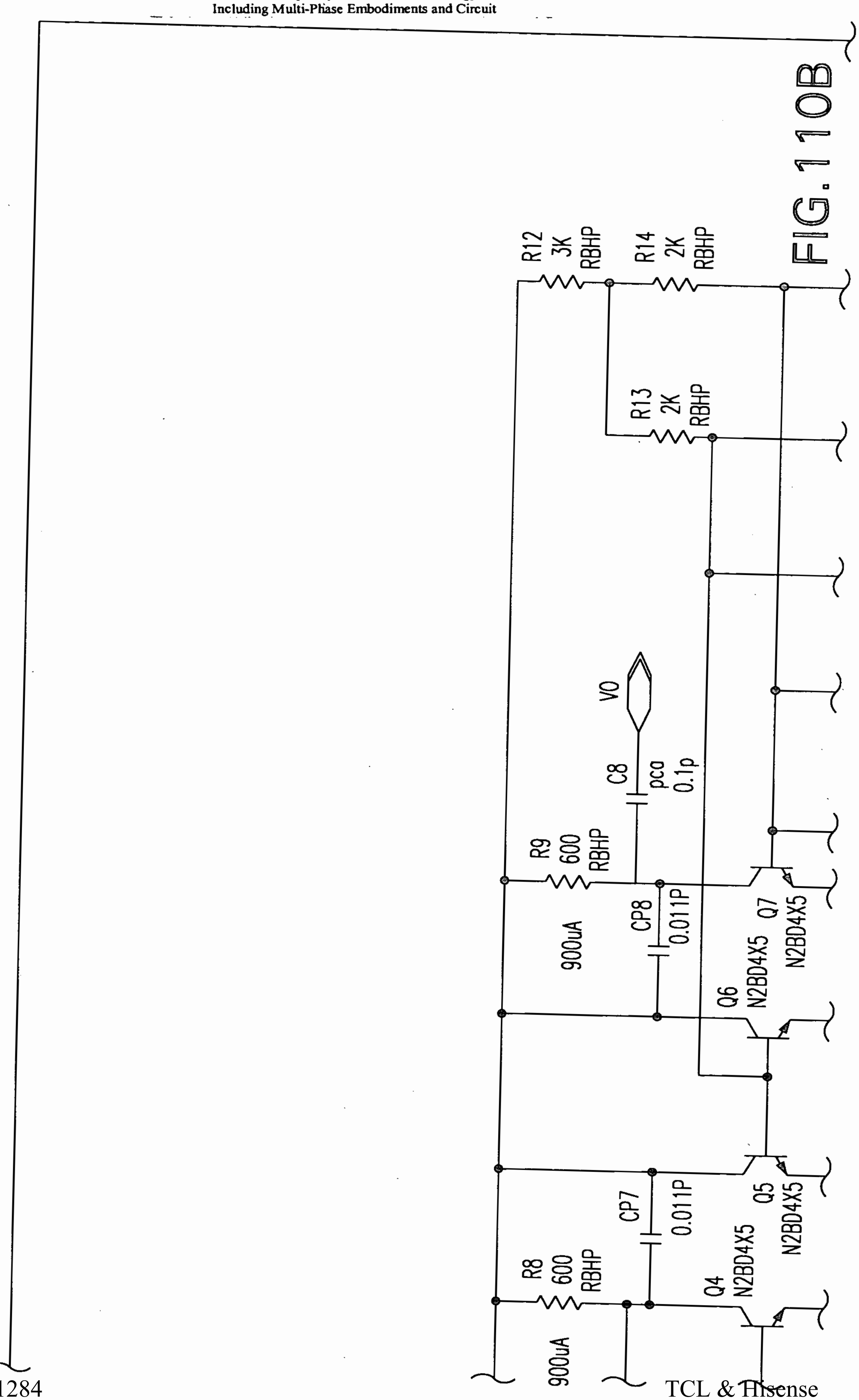
R12
3K
RBHP
R14
2K
RBHP
R13
2K
RBHP
VO
C8
pca
0.1p
R9
600
RBHP
900uA
CP8
0.011P
Q7
N2BD4X5
Q6
N2BD4X5
CP7
0.011P
Q5
N2BD4X5
Q4
N2BD4X5
R8
600
RBHP
900uA

FIG. 110B

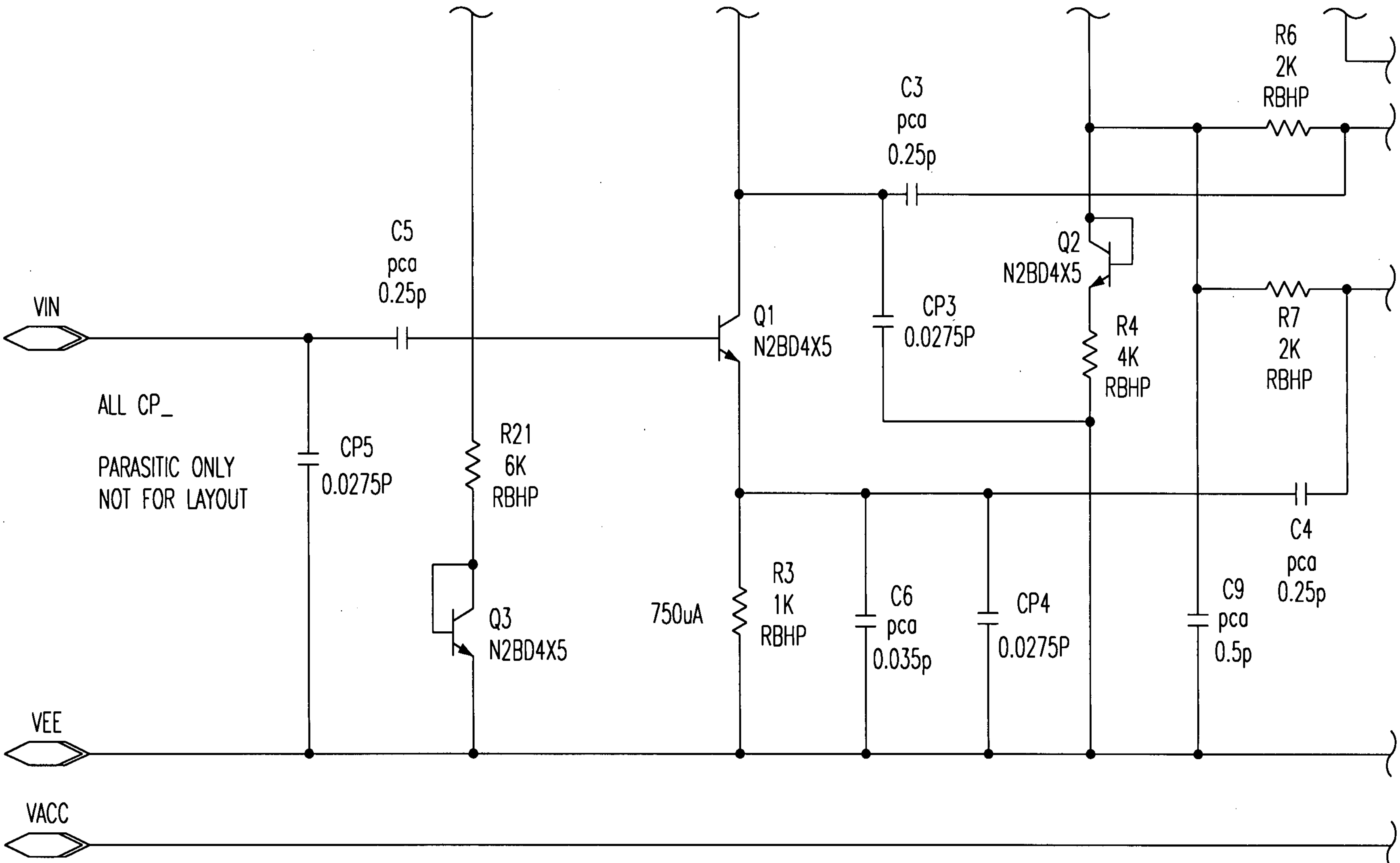

FIG.110C

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Sheet 244 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

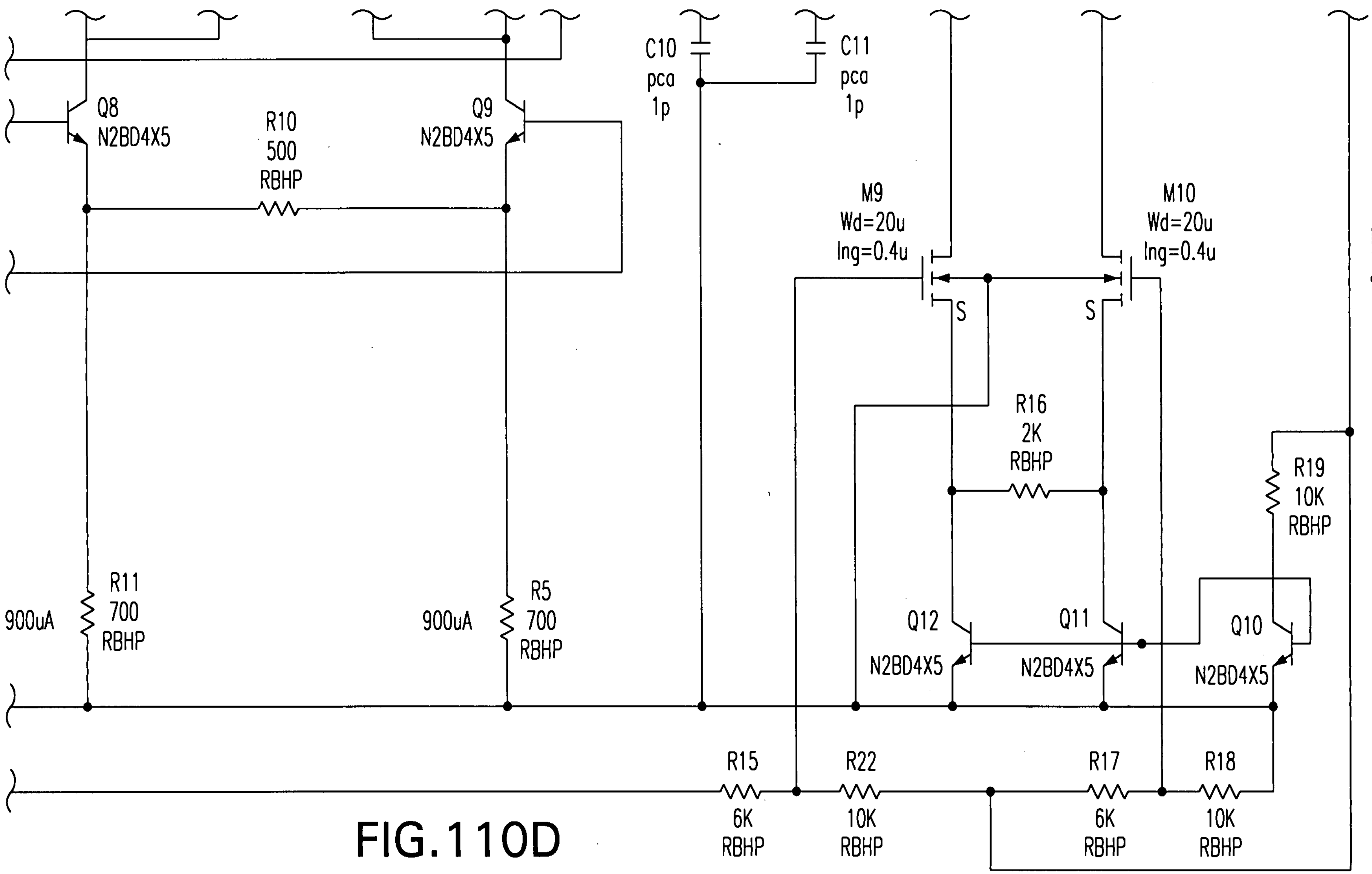

FIG.110D

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Sheet 245 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
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Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

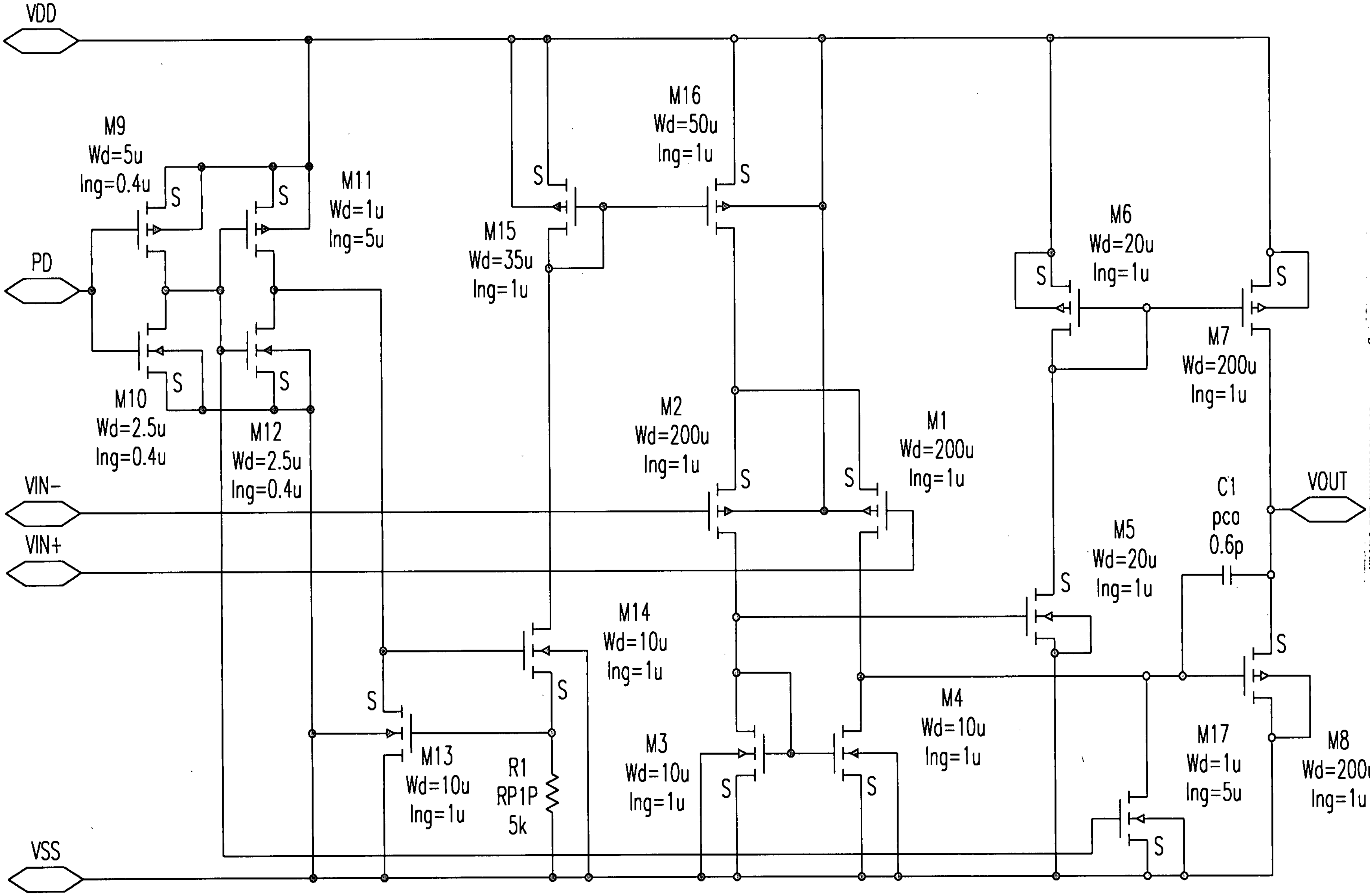


FIG.111

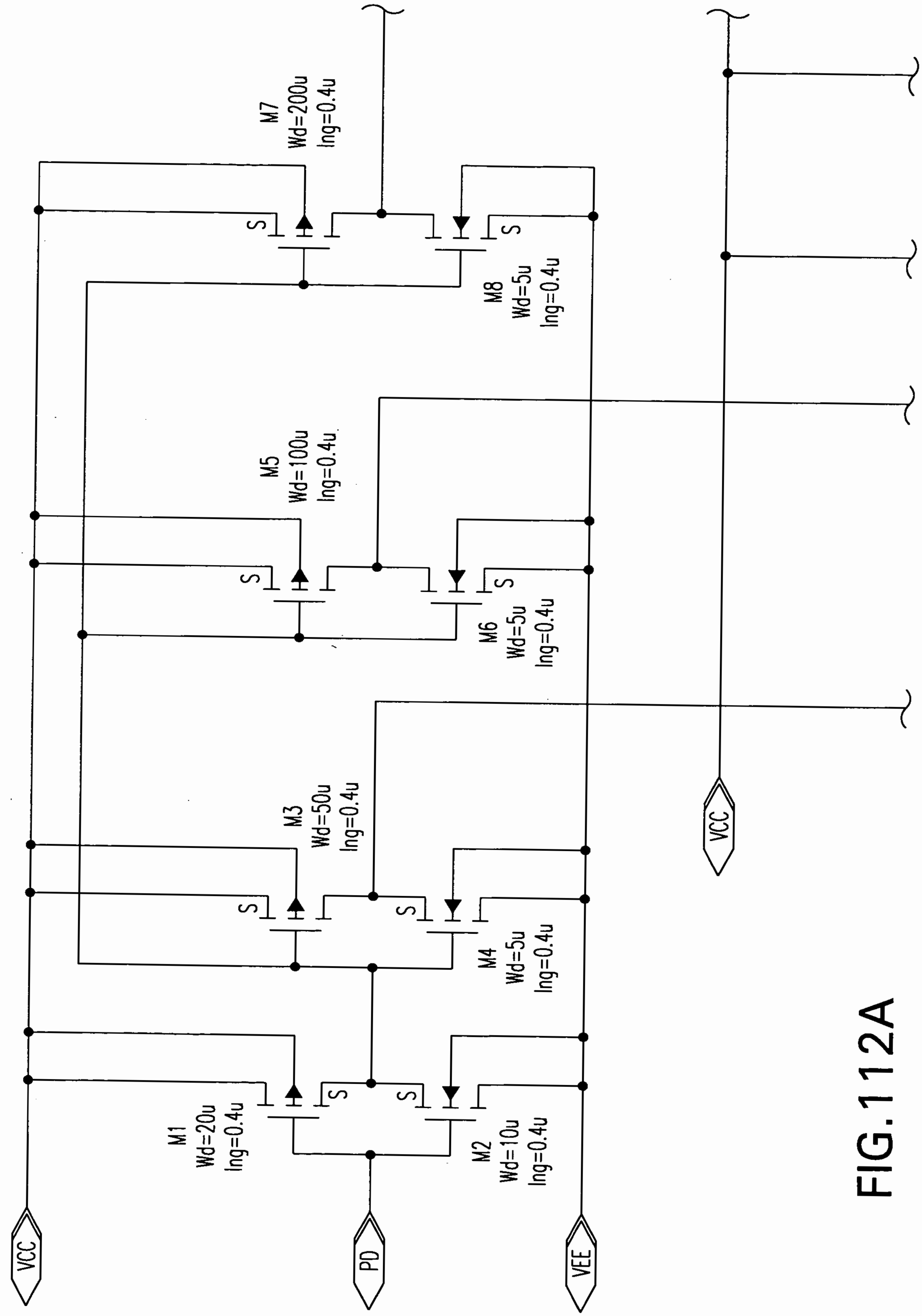
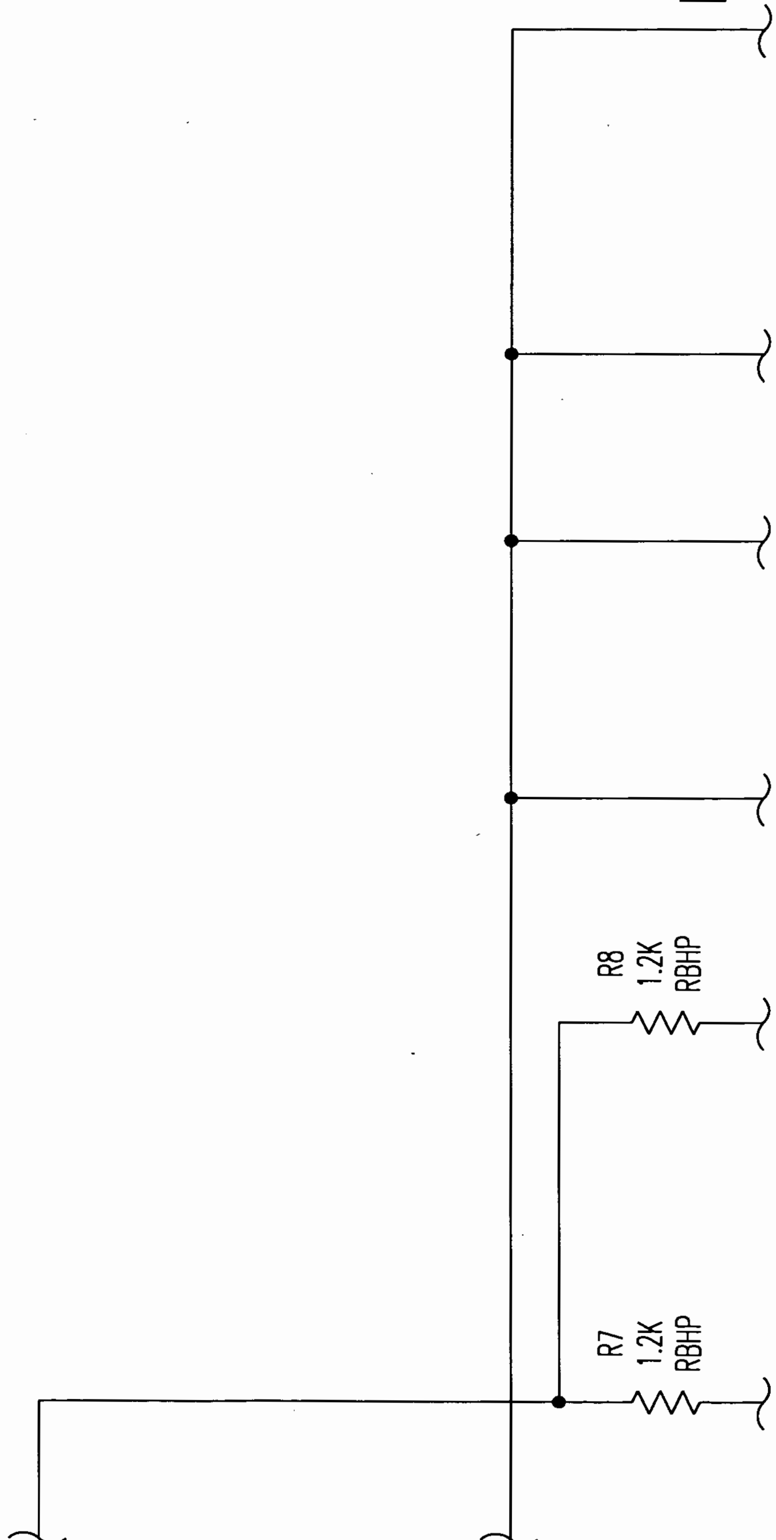

M7
Wd=200u
lng=0.4u
M8
Wd=5u
lng=0.4u
M5
Wd=100u
lng=0.4u
M6
Wd=5u
lng=0.4u
M3
Wd=50u
lng=0.4u
M4
Wd=5u
lng=0.4u
M1
Wd=20u
lng=0.4u
M2
Wd=10u
lng=0.4u
S
VCC
PD
VEE

FIG.112A

New Sheet
Sheet 248 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

FIG.112B



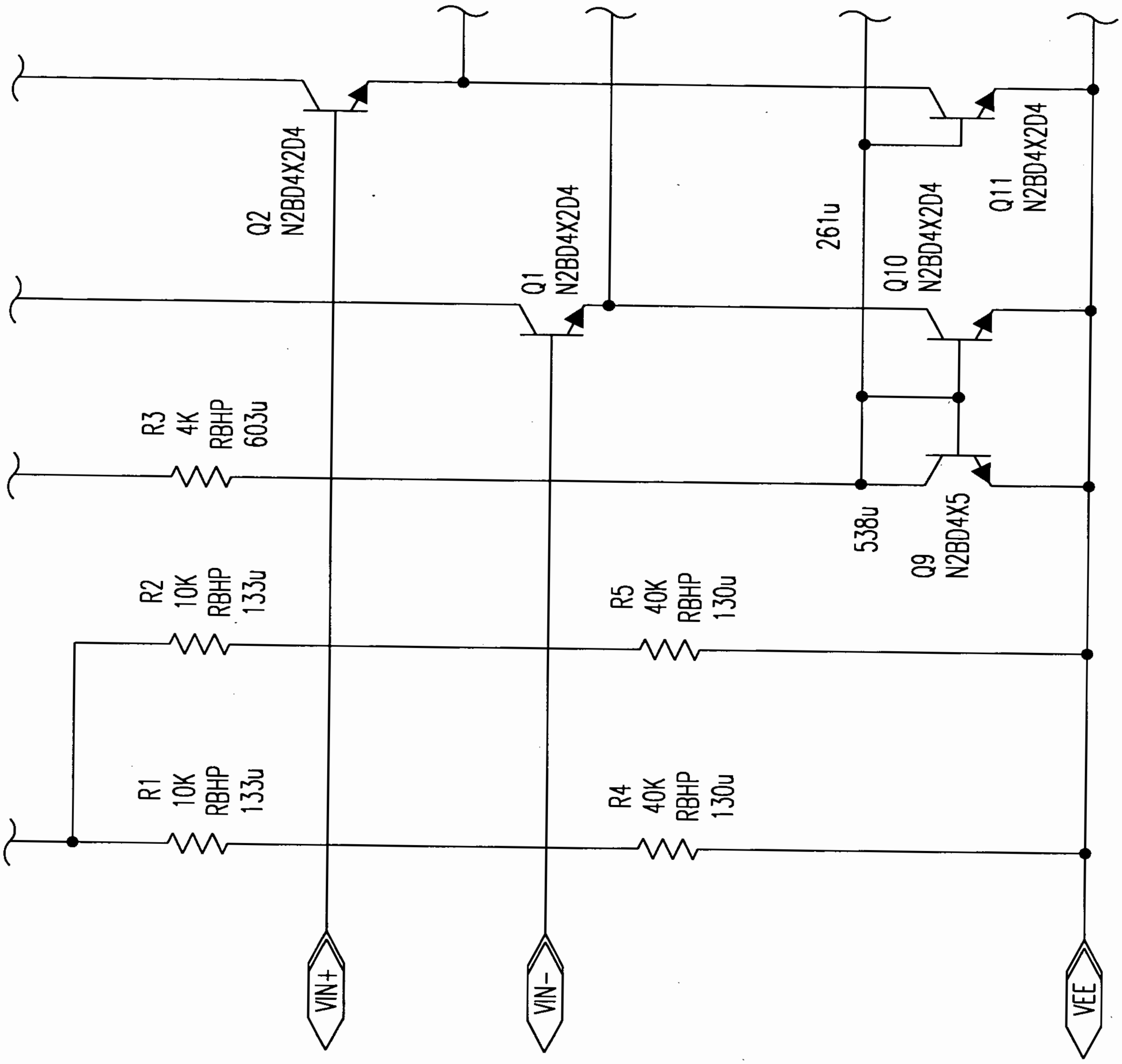

Q2
N2BD4X2D4
Q1
N2BD4X2D4
261u
Q10
N2BD4X2D4
Q11
N2BD4X2D4
R3
4K
RBHP
603u
538u
Q9
N2BD4X5
R2
10K
RBHP
133u
R5
40K
RBHP
130u
R1
10K
RBHP
133u
R4
40K
RBHP
130u
VIN+
VIN-
VEE

FIG.112C

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

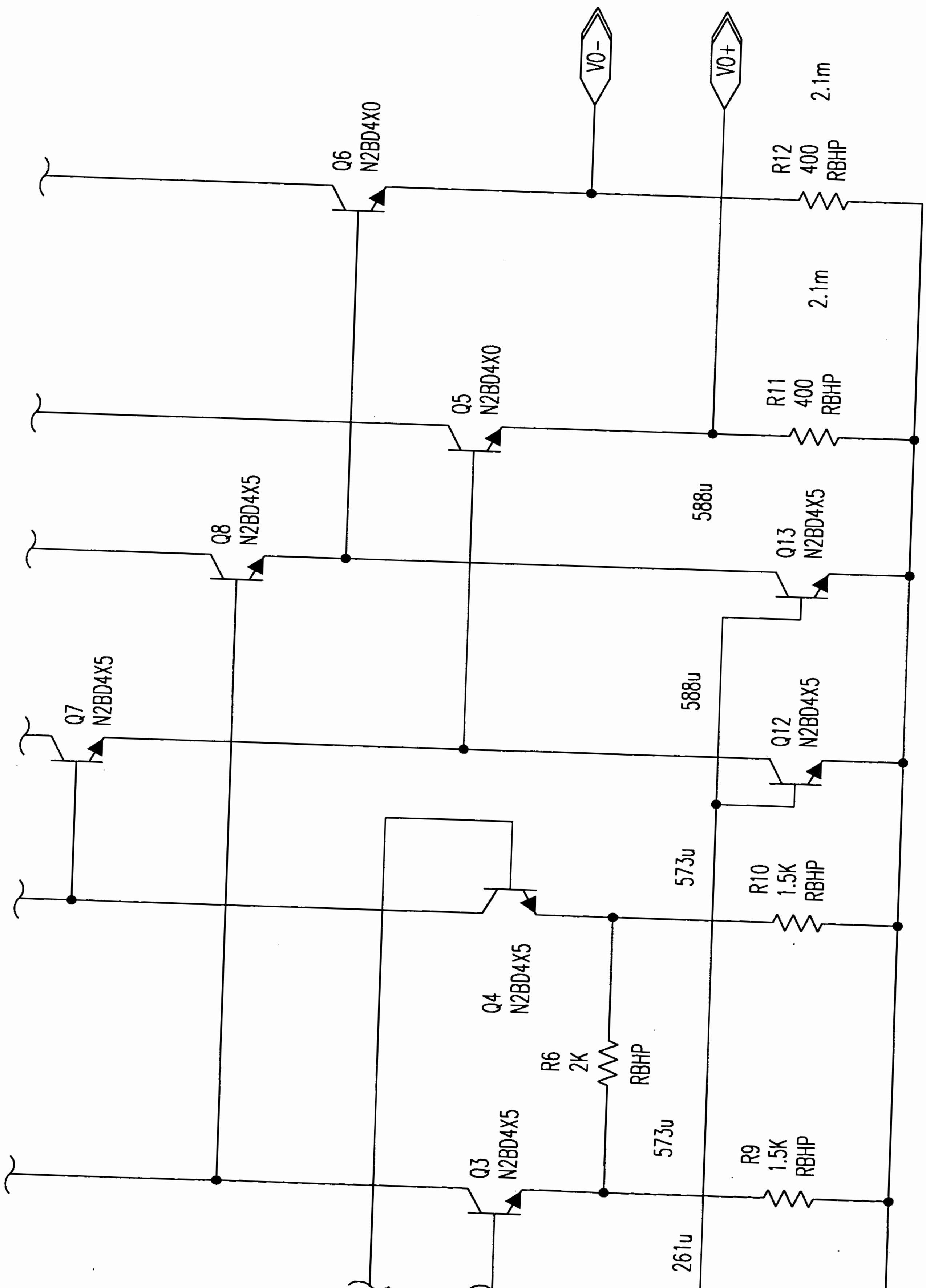


FIG.112D

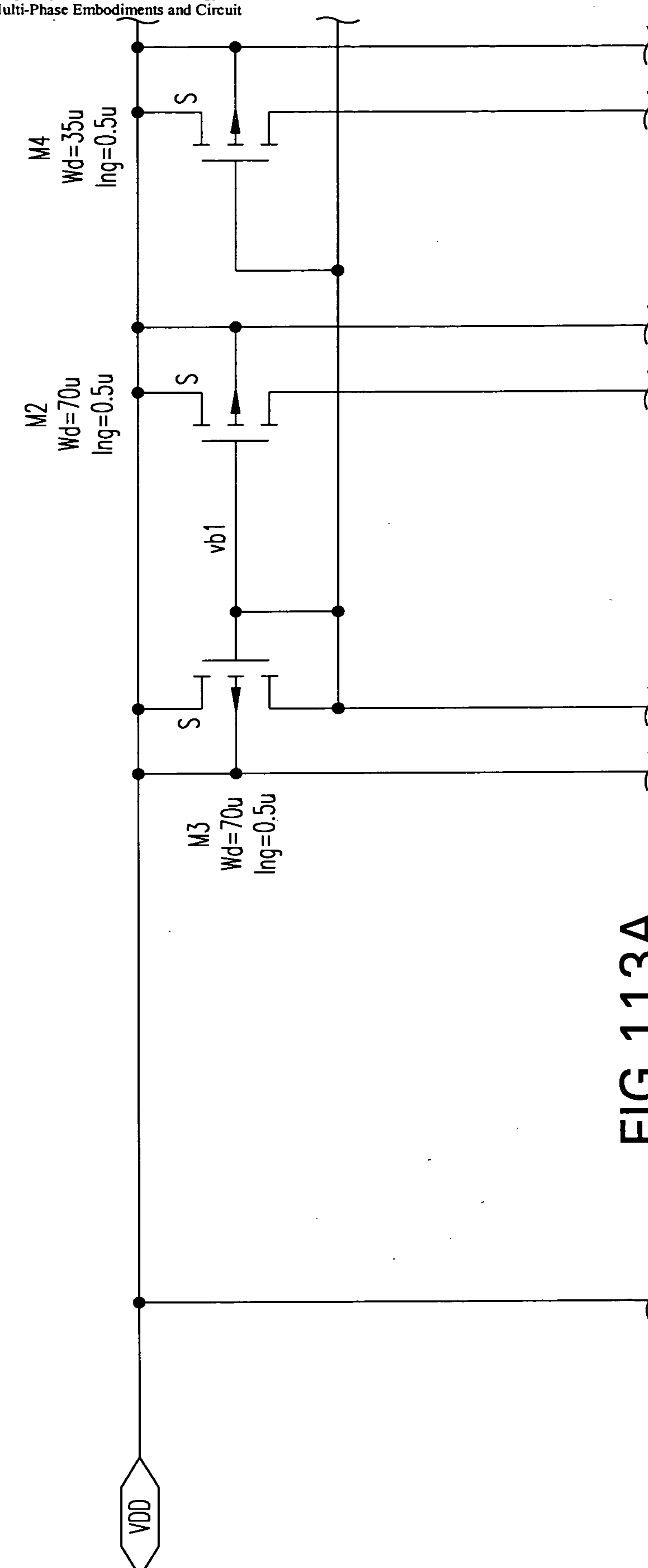


FIG.113A

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

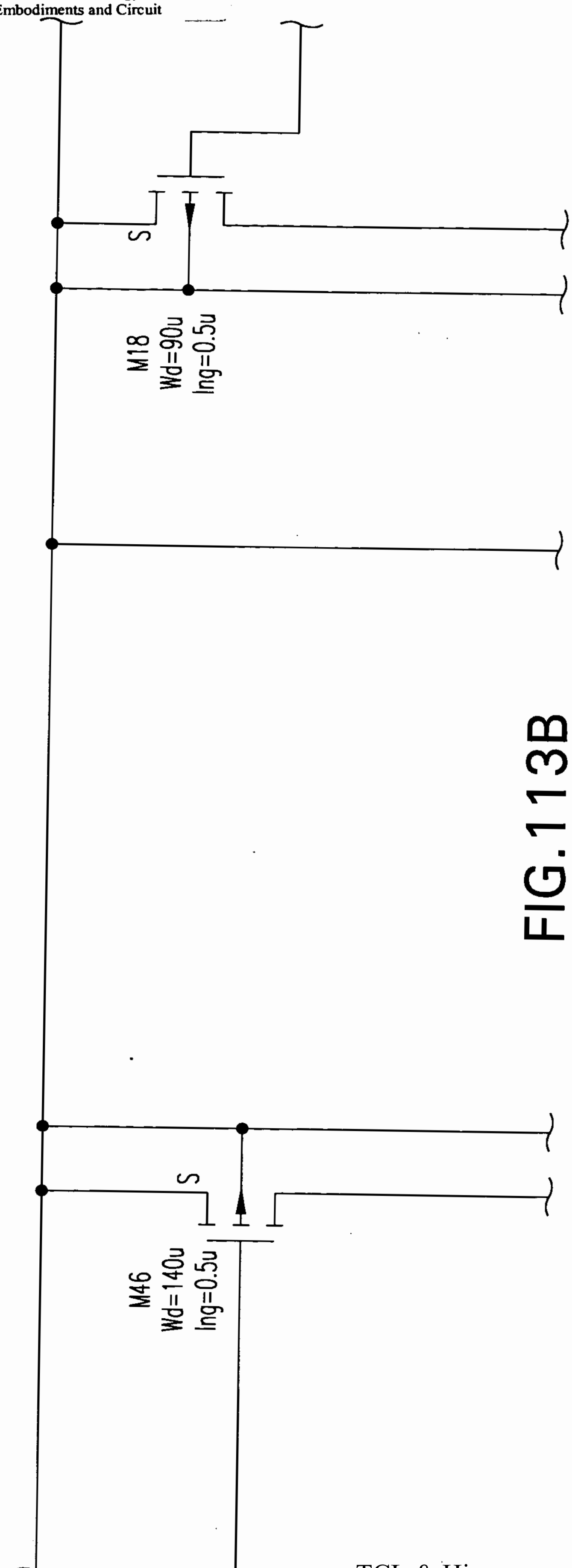


FIG.113B

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

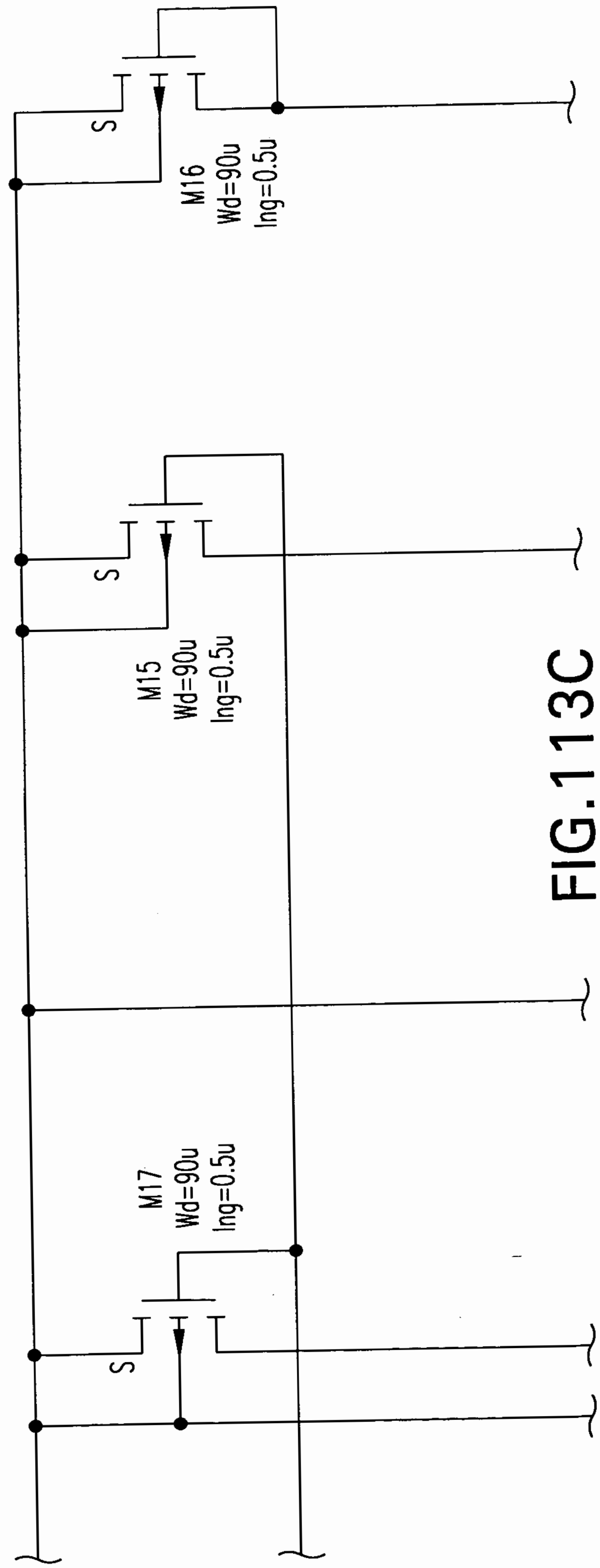


FIG.113C

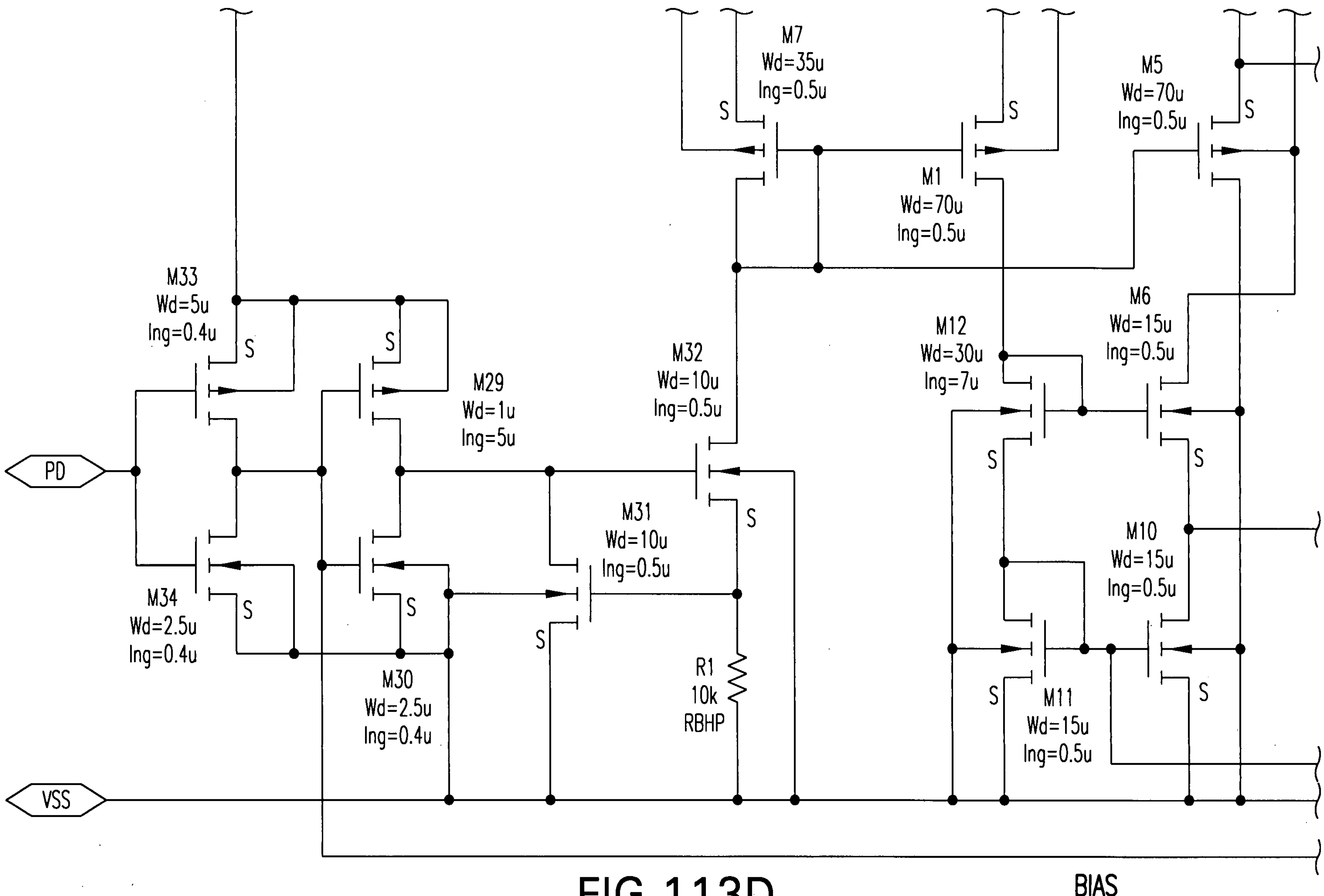


FIG.113D

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Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

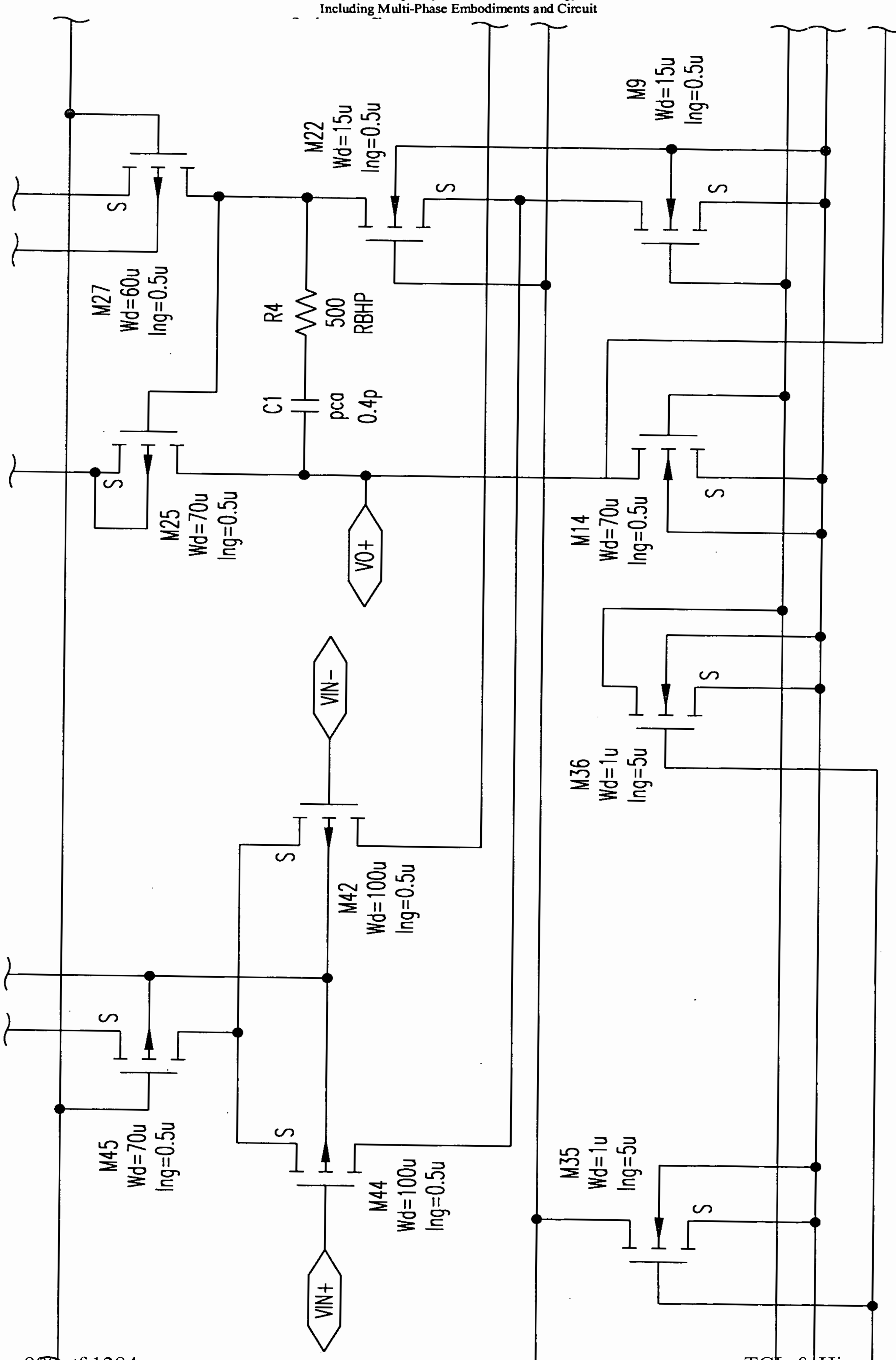
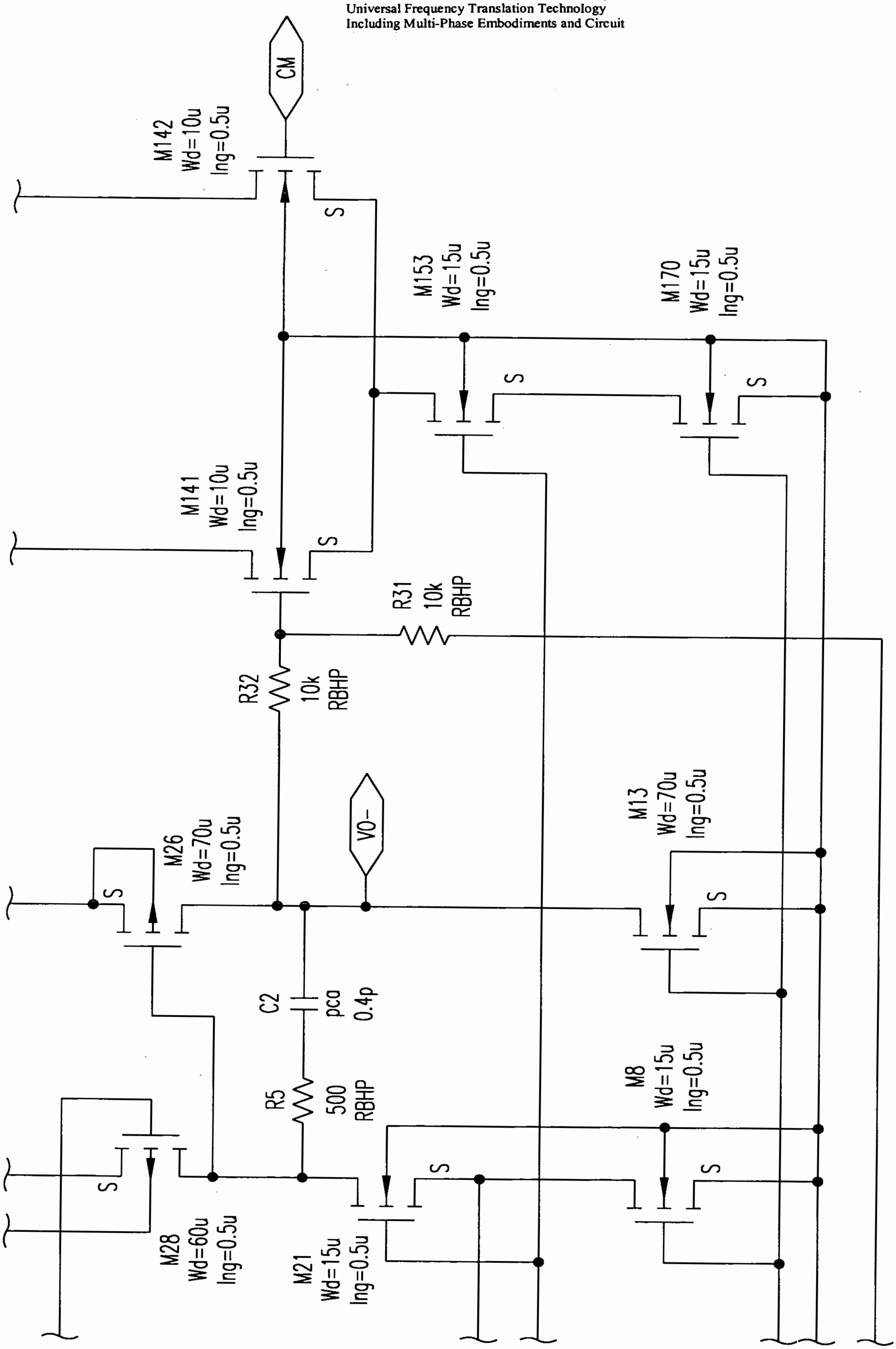

M27
Wd=60u
lng=0.5u
M25
Wd=70u
lng=0.5u
M22
Wd=15u
lng=0.5u
M9
Wd=15u
lng=0.5u
R4
500
RBHP
C1
pca
0.4p
VO+
VIN-
M14
Wd=70u
lng=0.5u
M36
Wd=1u
lng=5u
M42
Wd=100u
lng=0.5u
M45
Wd=70u
lng=0.5u
M44
Wd=100u
lng=0.5u
VIN+
M35
Wd=1u
lng=5u
S

FIG.113E



CMFB

FIG.113F

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Inventors: Sorrells et al.
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Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

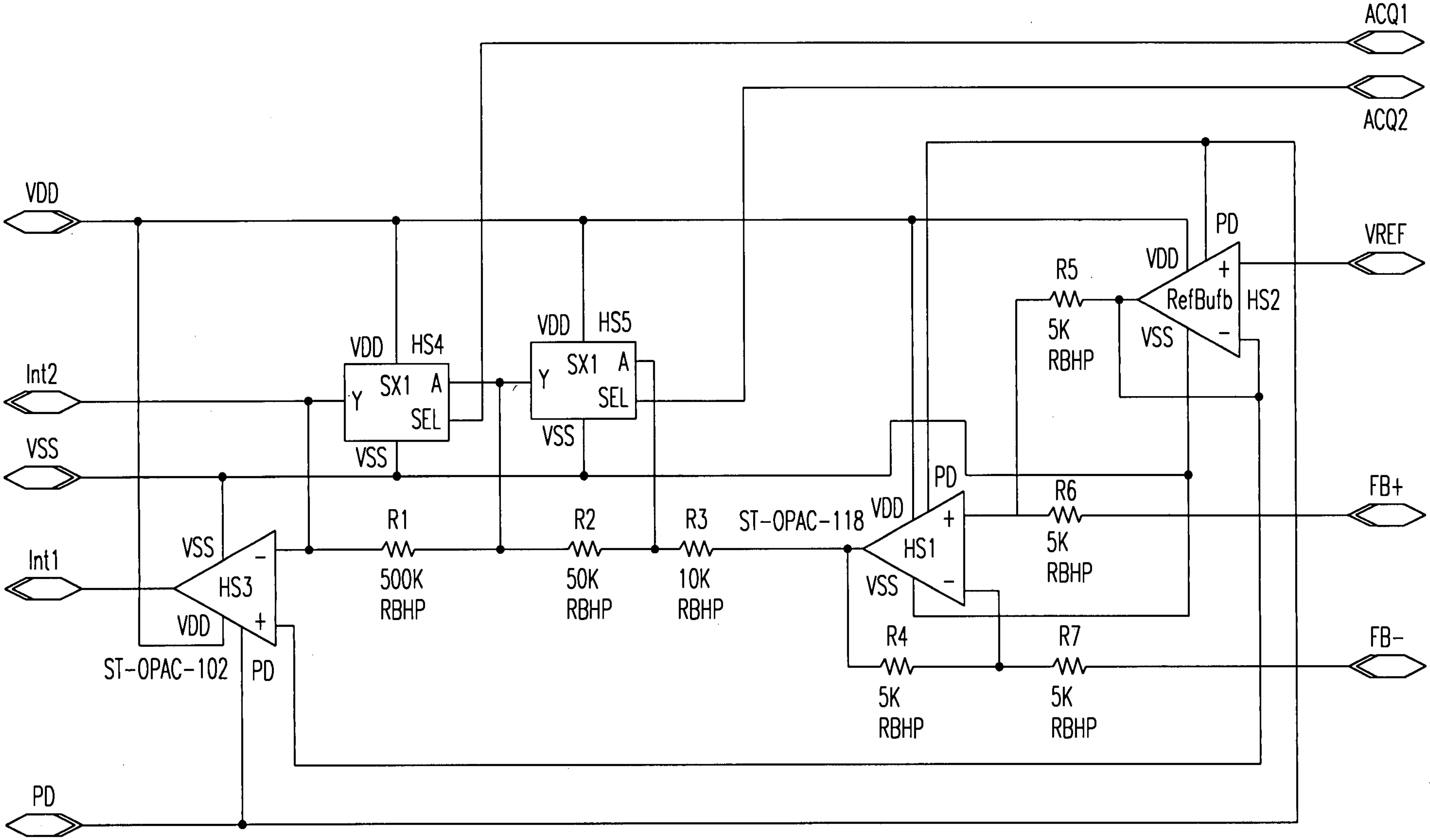

FIG.114

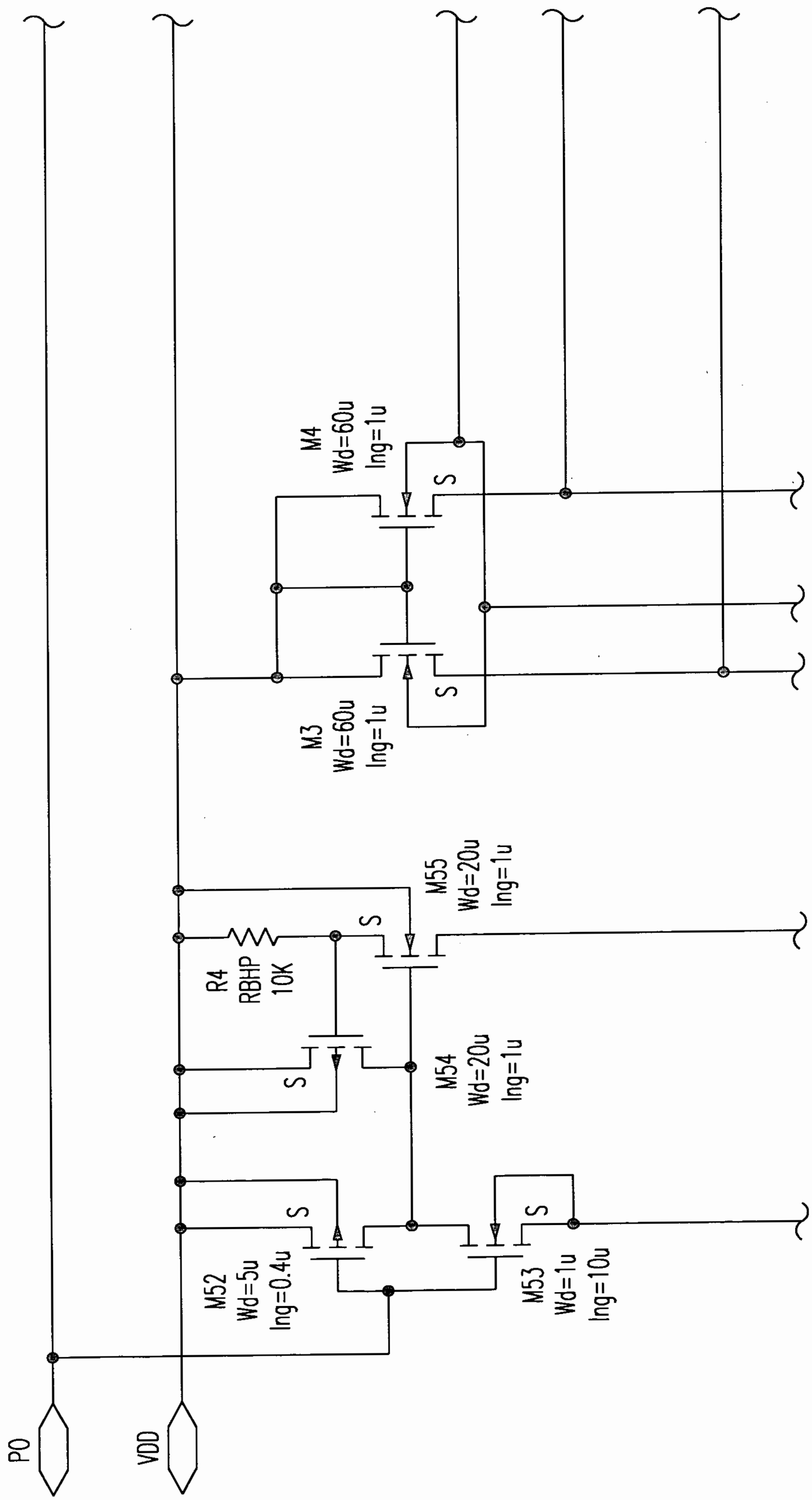
M4
Wd=60u
lng=1u
S
M3
Wd=60u
lng=1u
S
M55
Wd=20u
lng=1u
S
R4
RBHP
10K
M54
Wd=20u
lng=1u
S
M52
Wd=5u
lng=0.4u
S
M53
Wd=1u
lng=10u
S
PO
VDD

FIG. 115A

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Sheet 259 of 349
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Inventors: Sorrells et al.
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Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

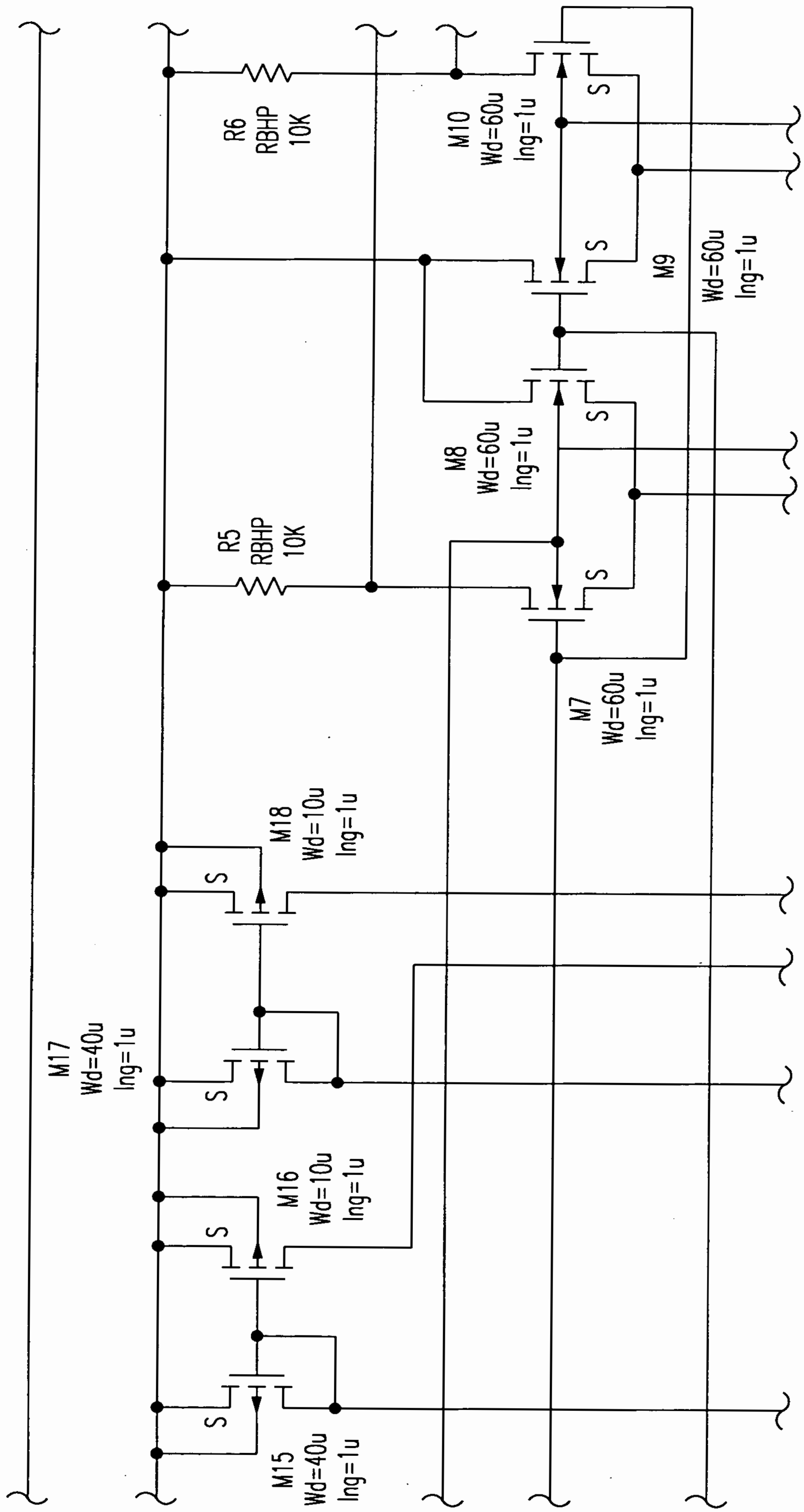

FIG.115B

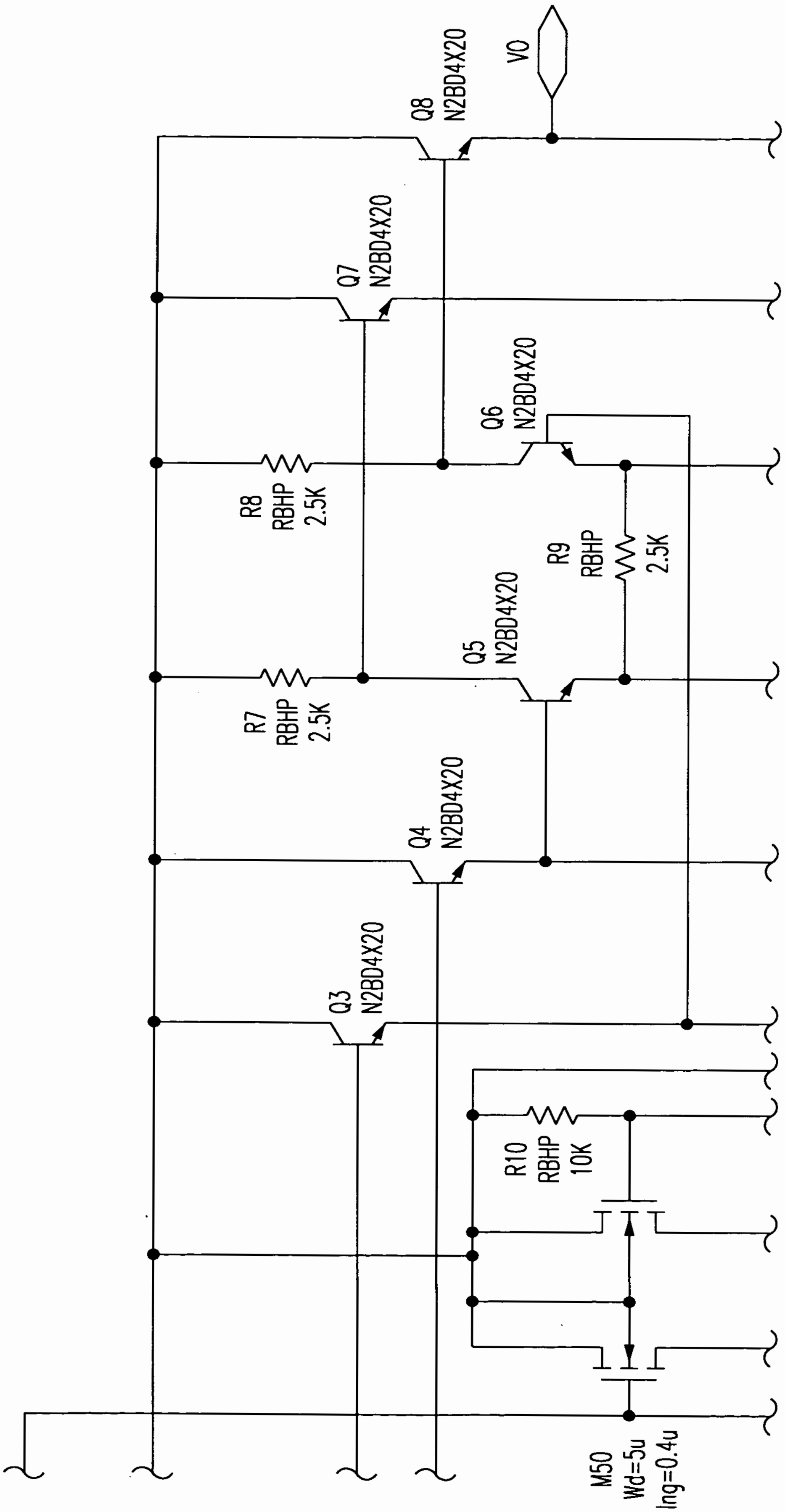
VO
Q8
N2BD4X20
Q7
N2BD4X20
Q6
N2BD4X20
R8
RBHP
2.5K
R9
RBHP
2.5K
Q5
N2BD4X20
R7
RBHP
2.5K
Q4
N2BD4X20
Q3
N2BD4X20
R10
RBHP
10K
M50
Wd=5u
lng=0.4u

FIG.115C

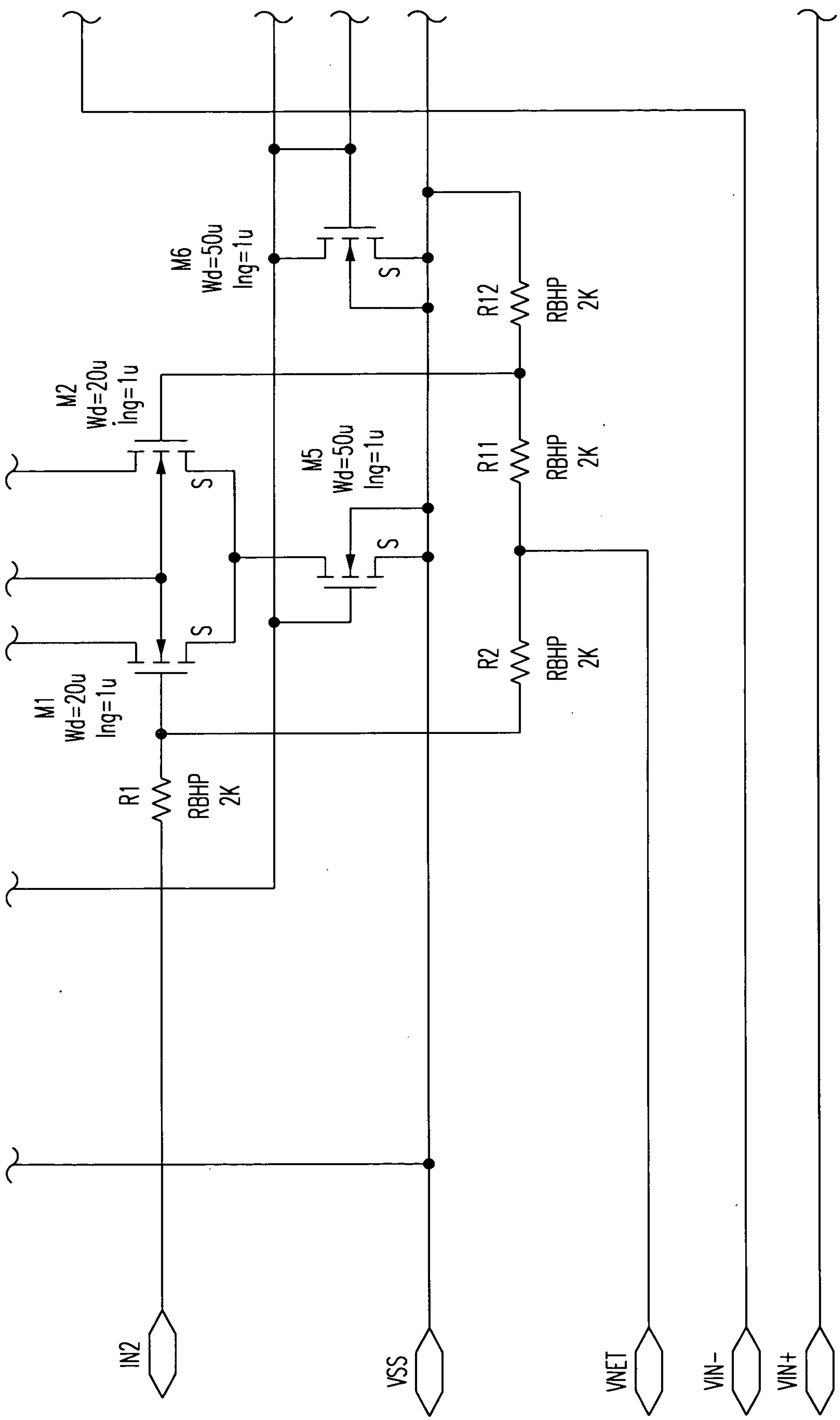
M6
Wd=50u
lng=1u
S
R12
RBHP
2K
M2
Wd=20u
lng=1u
S
M5
Wd=50u
lng=1u
S
R11
RBHP
2K
S
M1
Wd=20u
lng=1u
R2
RBHP
2K
R1
RBHP
2K
IN2
VSS
VNET
VIN-
VIN+

FIG.115D

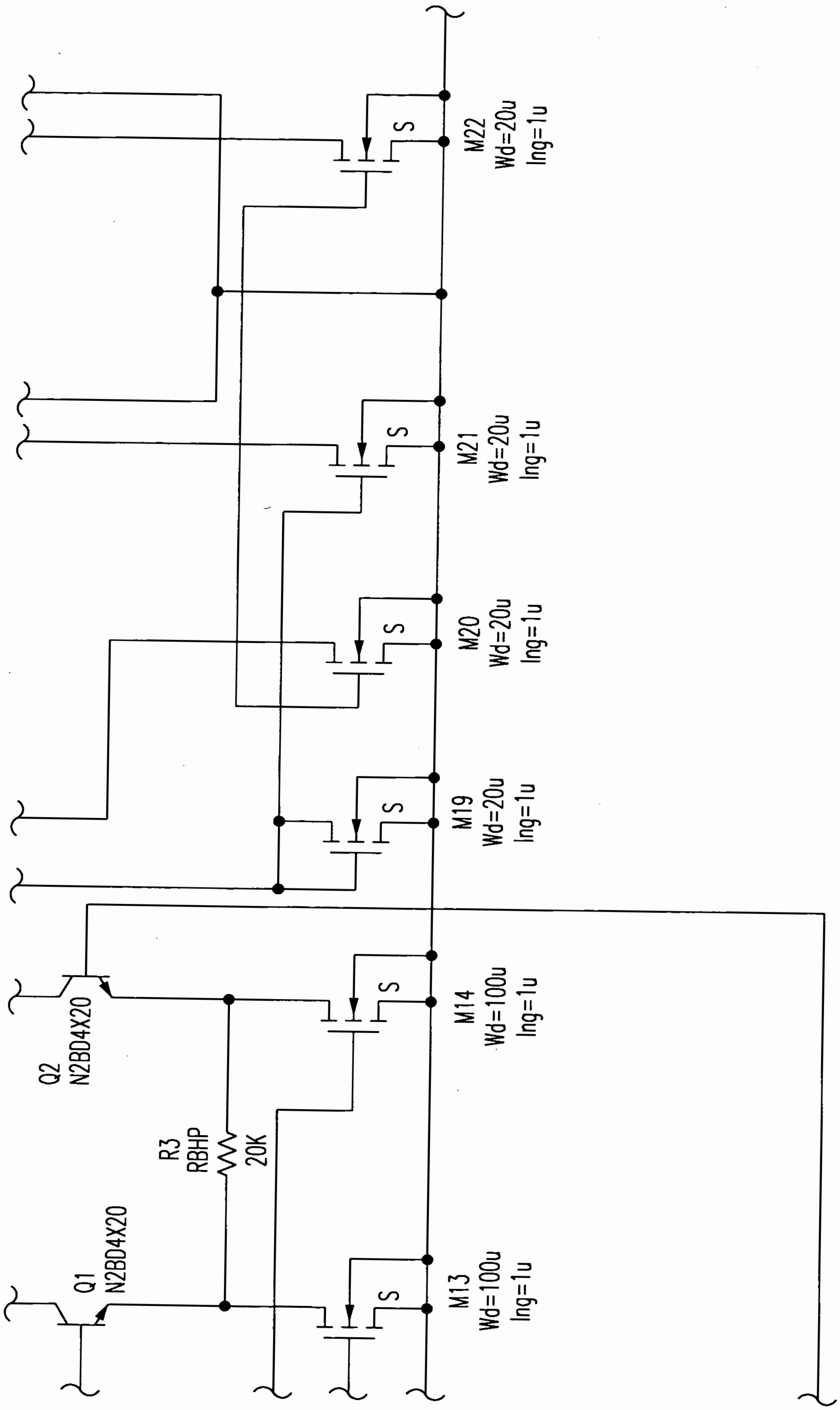
M22
Wd=20u
lng=1u
M21
Wd=20u
lng=1u
M20
Wd=20u
lng=1u
M19
Wd=20u
lng=1u
M14
Wd=100u
lng=1u
M13
Wd=100u
lng=1u
Q2
N2BD4X20
Q1
N2BD4X20
R3
RBHP
20K
S

FIG.115E

Appl. No. 09/632,856; Filed: Aug 4, 2000
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Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

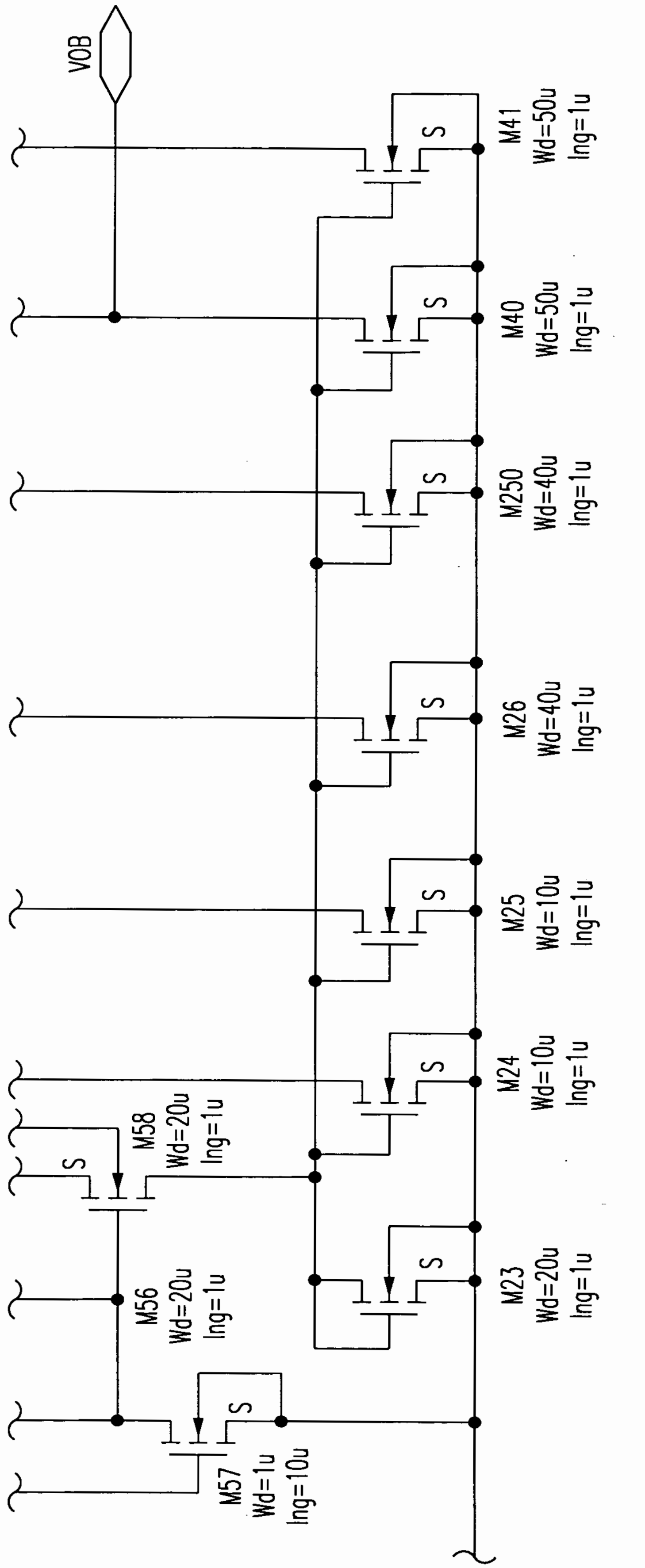


FIG.115F

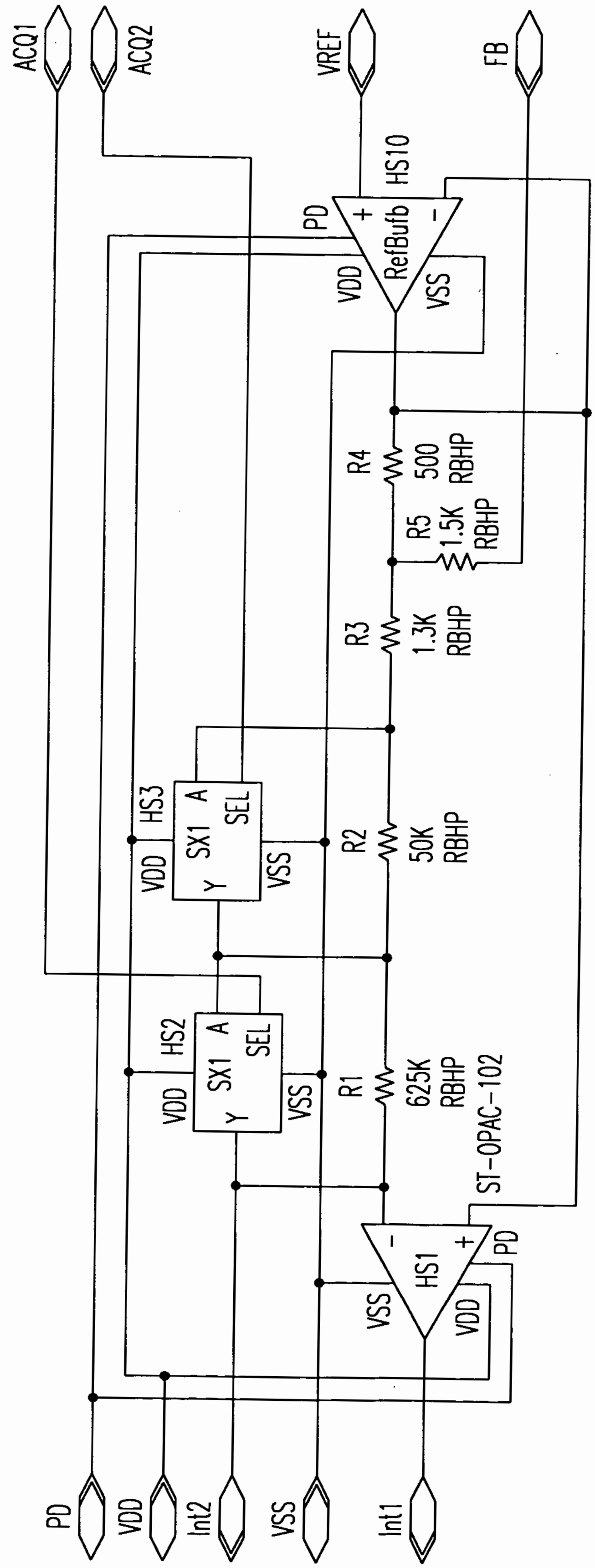

ACQ1
ACQ2
VREF
FB
PD
VDD
RefBufb
HS10
VSS
R4
500
RBHP
R5
1.5K
RBHP
R3
1.3K
RBHP
HS3
SX1
A
Y
SEL
VDD
VSS
R2
50K
RBHP
HS2
SX1
A
Y
SEL
VDD
VSS
R1
625K
RBHP
ST-OPAC-102
HS1
VSS
VDD
PD
PD
VDD
Int2
VSS
Int1

FIG.116

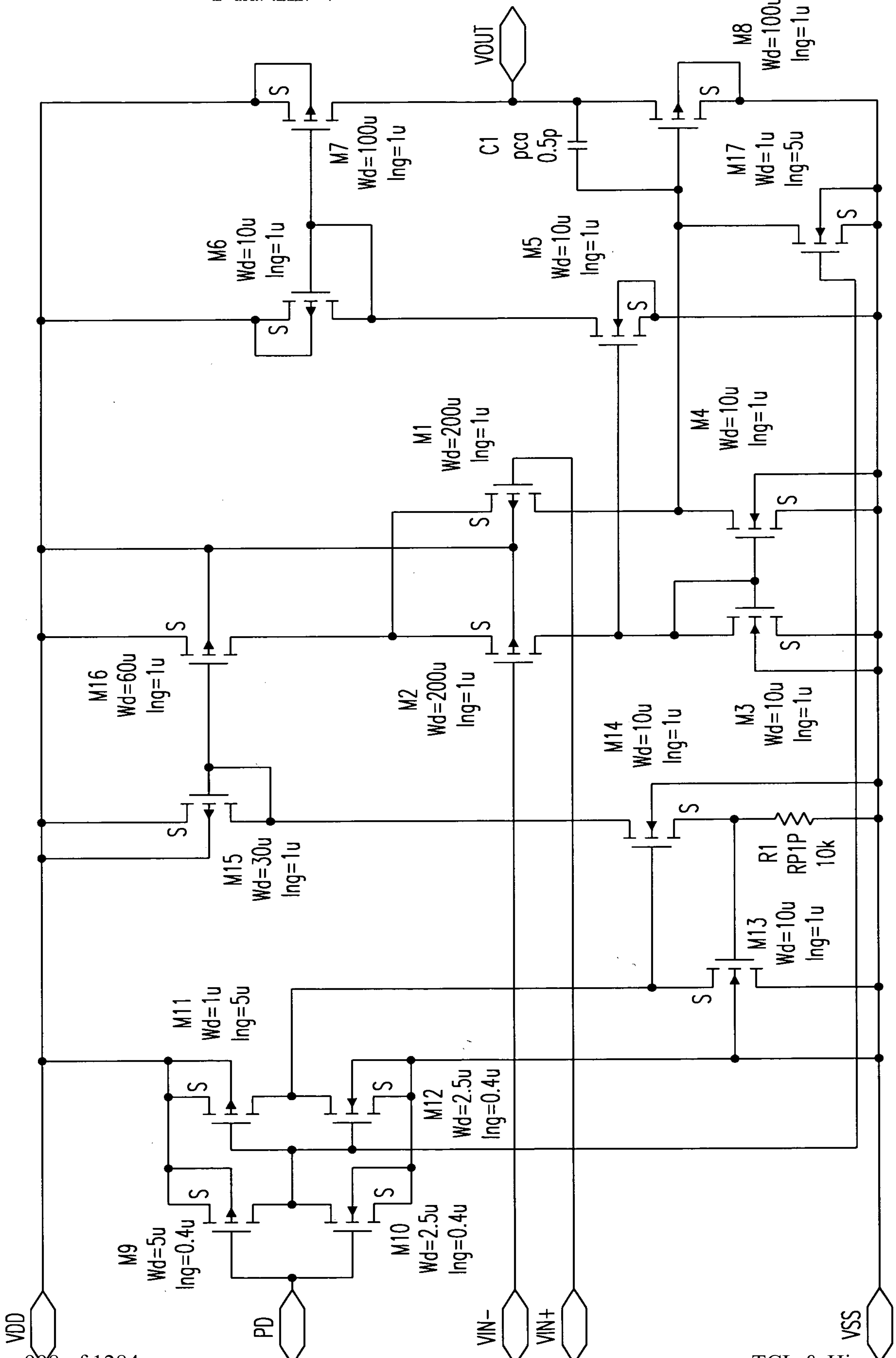

VOUT
M7 Wd=100u lng=1u
M8 Wd=100u lng=1u
C1 pca 0.5p
M17 Wd=1u lng=5u
M6 Wd=10u lng=1u
M5 Wd=10u lng=1u
M1 Wd=200u lng=1u
M4 Wd=10u lng=1u
M16 Wd=60u lng=1u
M2 Wd=200u lng=1u
M14 Wd=10u lng=1u
M3 Wd=10u lng=1u
M15 Wd=30u lng=1u
R1 RP1P 10k
M13 Wd=10u lng=1u
M11 Wd=1u lng=5u
M12 Wd=2.5u lng=0.4u
M9 Wd=5u lng=0.4u
M10 Wd=2.5u lng=0.4u
VDD
PD
VIN-
VIN+
VSS

FIG.117

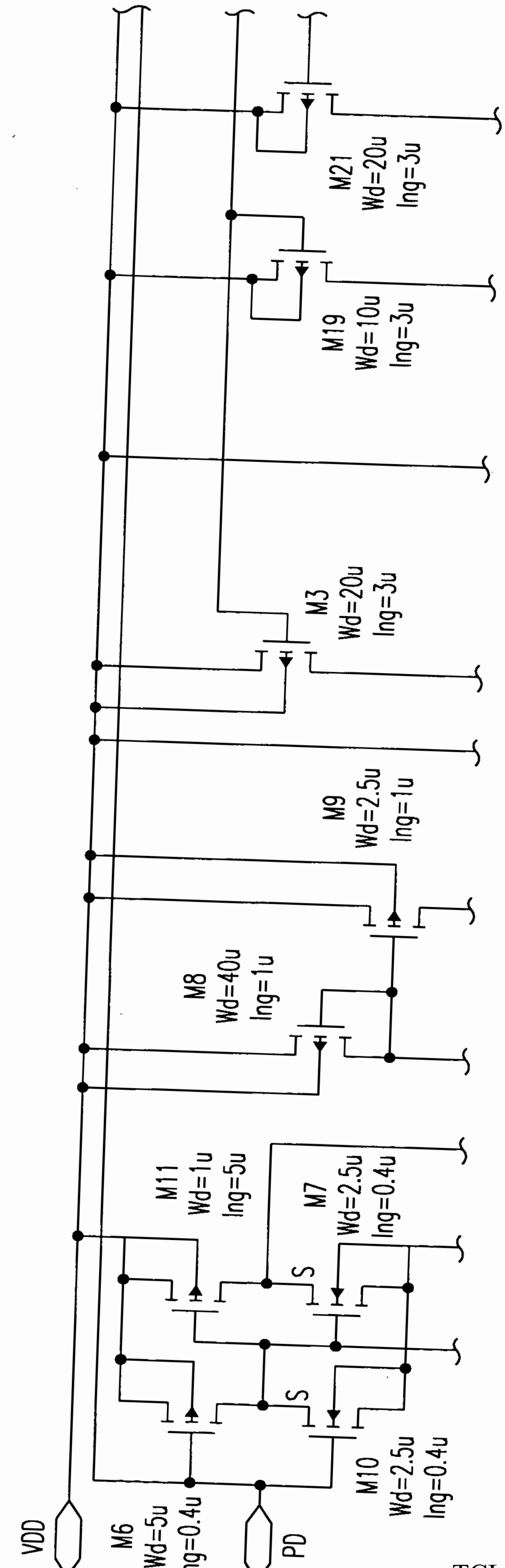

M21
Wd=20u
lng=3u
M19
Wd=10u
lng=3u
M3
Wd=20u
lng=3u
M9
Wd=2.5u
lng=1u
M8
Wd=40u
lng=1u
M11
Wd=1u
lng=5u
M7
Wd=2.5u
lng=0.4u
S
S
M10
Wd=2.5u
lng=0.4u
M6
Wd=5u
lng=0.4u
VDD
PD

FIG.118A

New Sheet
Sheet 267 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

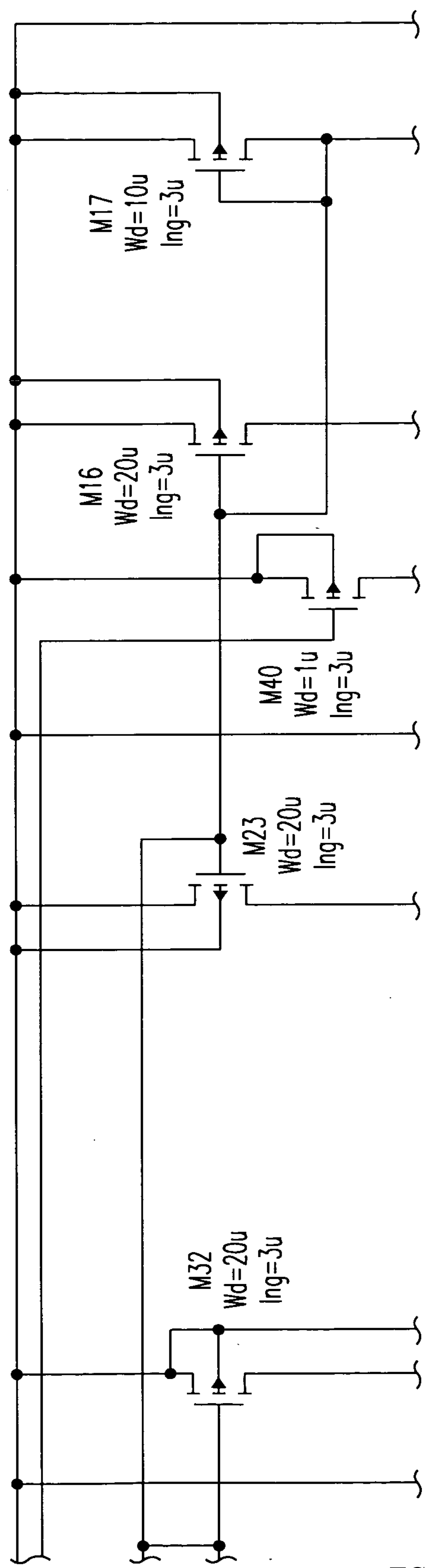


FIG.118B

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

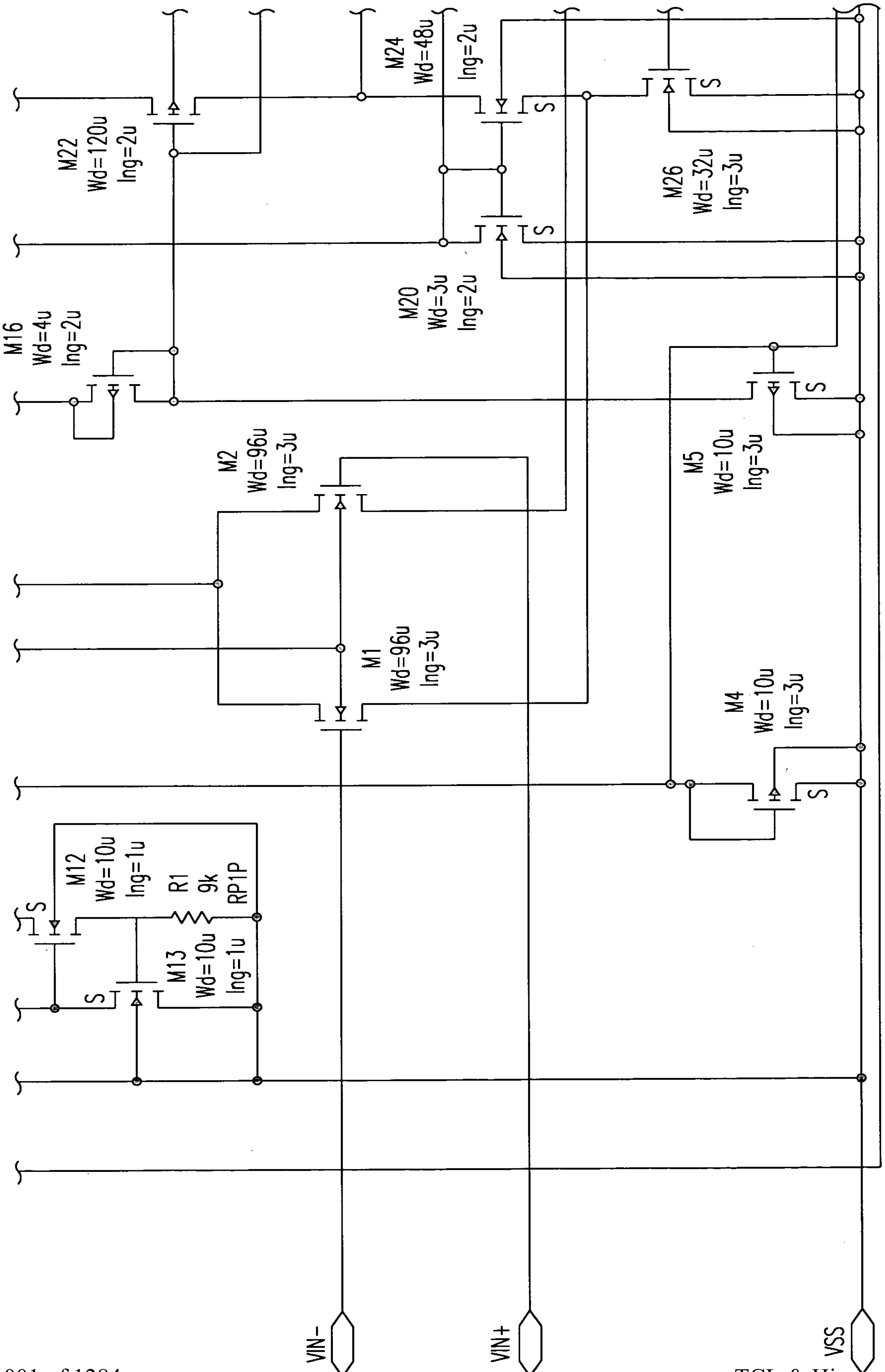


FIG. 118C

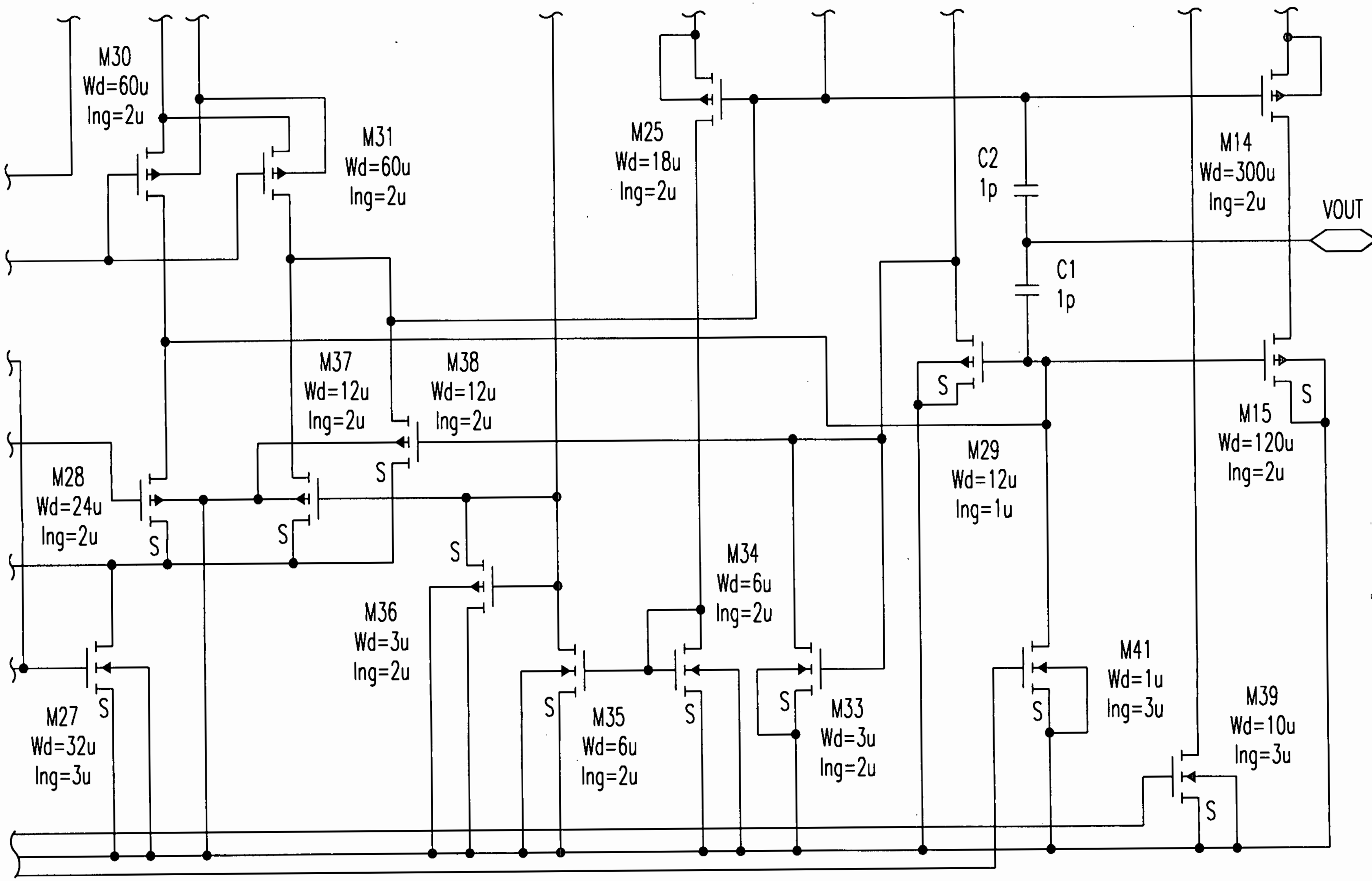


FIG.118D

New Sheet
Sheet 269 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

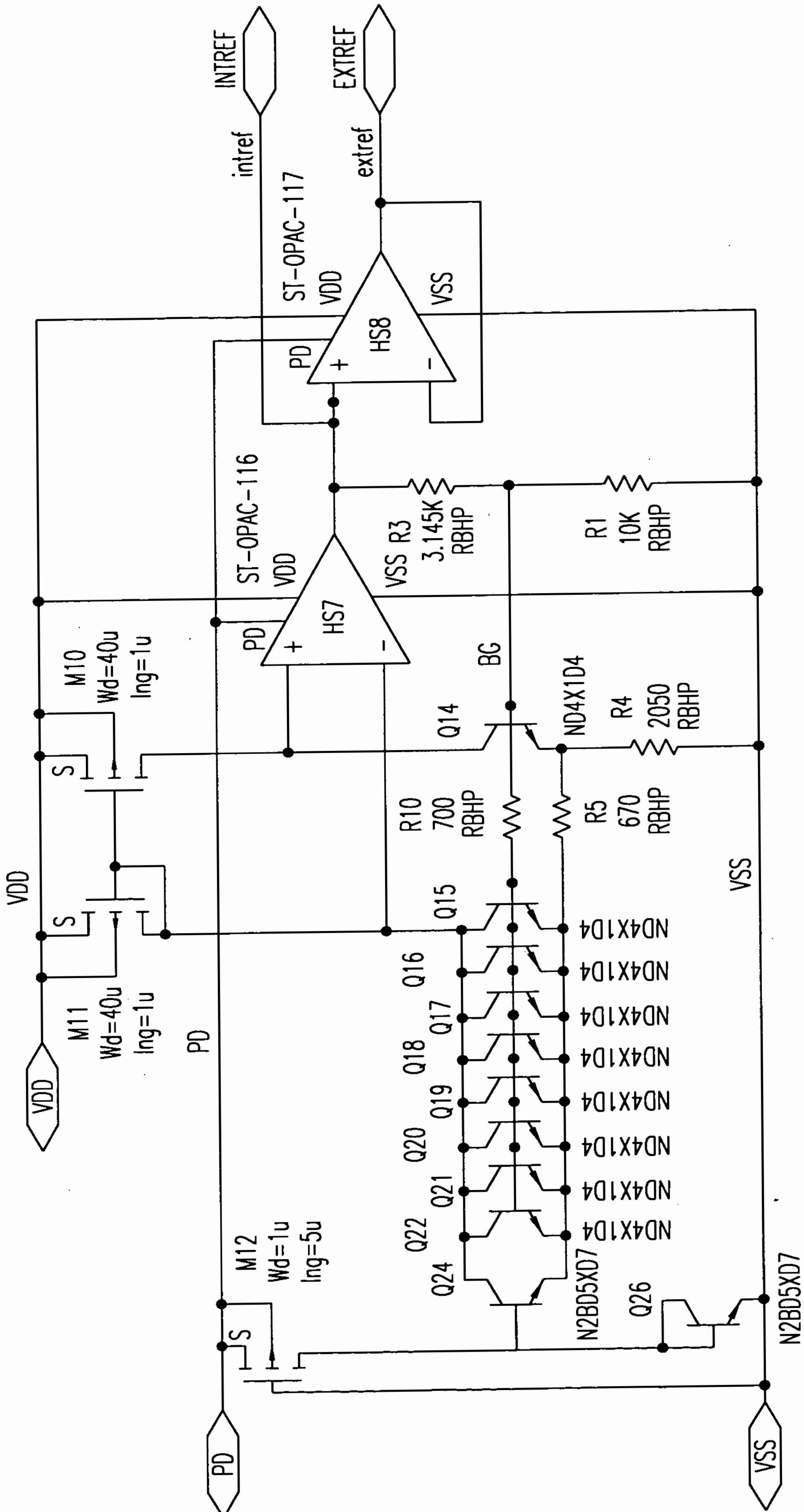


FIG.119

Replacement Sheet
Sheet 271 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

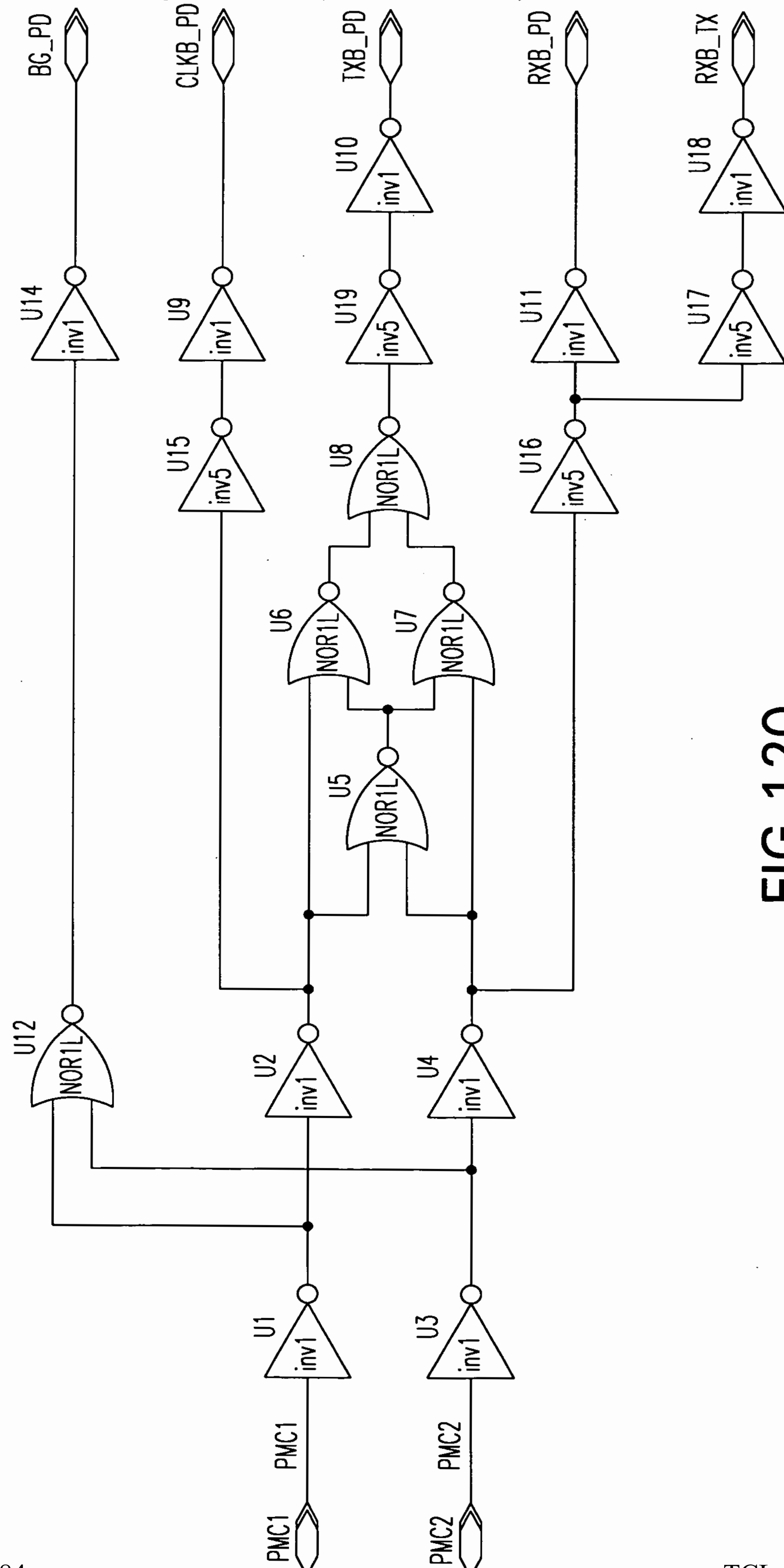


FIG.120

Replacement Sheet
Sheet 272 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

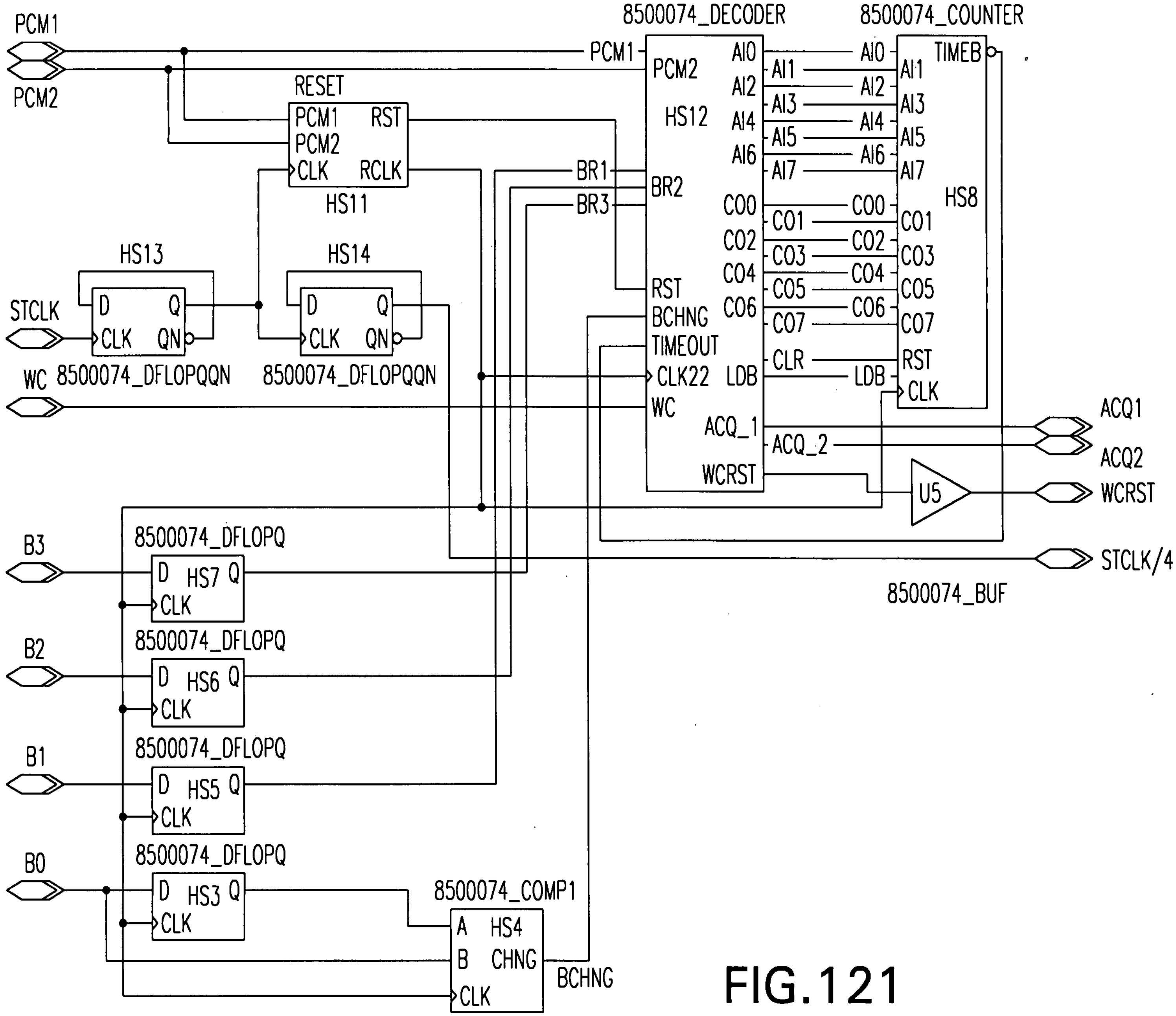
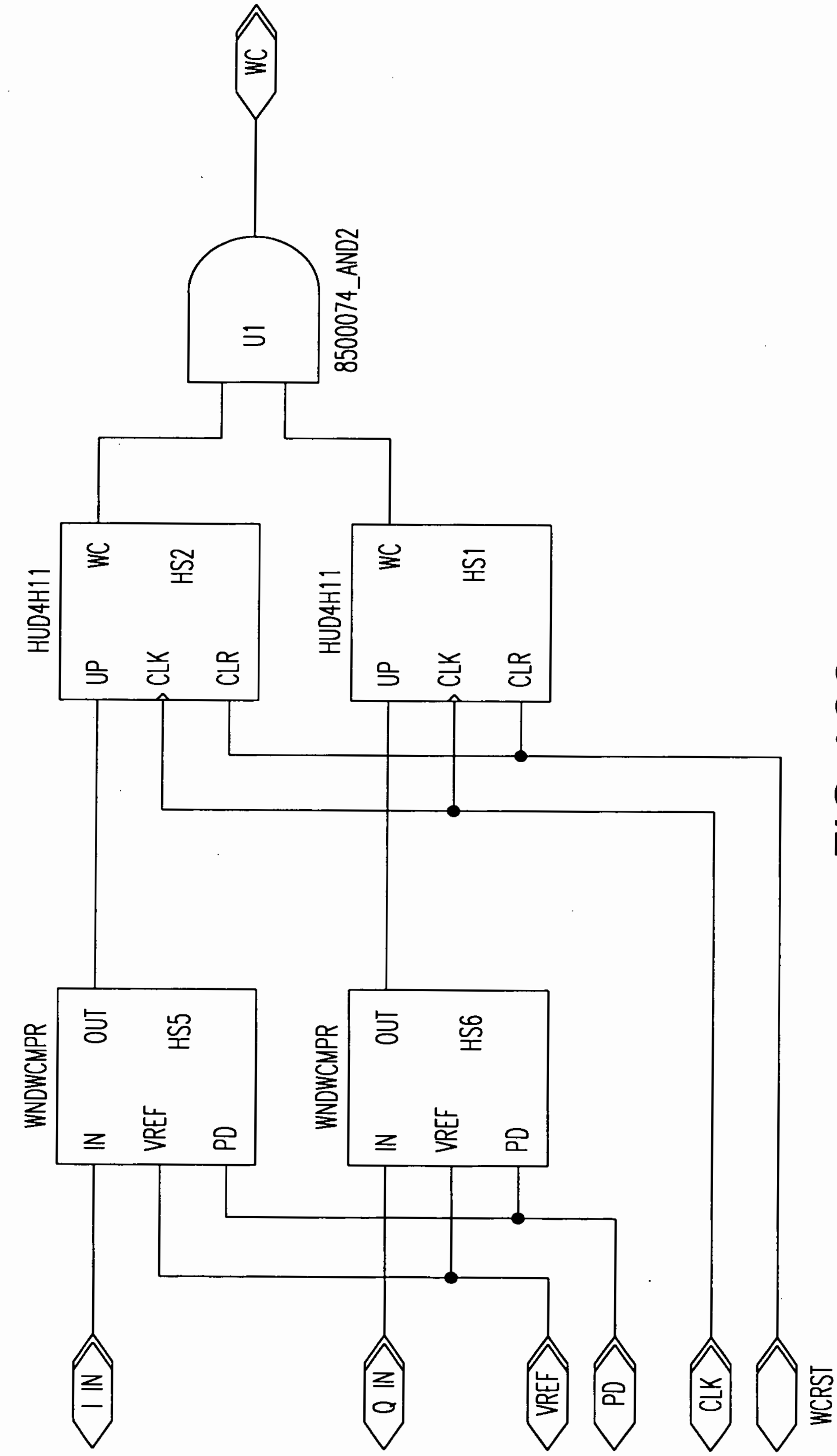


FIG.121



WC
U1
8500074_AND2
HUD4H11
WC
HS2
UP
CLK
CLR
HUD4H11
WC
HS1
UP
CLK
CLR
WNDWCMPR
OUT
HS5
IN
VREF
PD
WNDWCMPR
OUT
HS6
IN
VREF
PD
I IN
Q IN
VREF
PD
CLK
WCRST

FIG.122

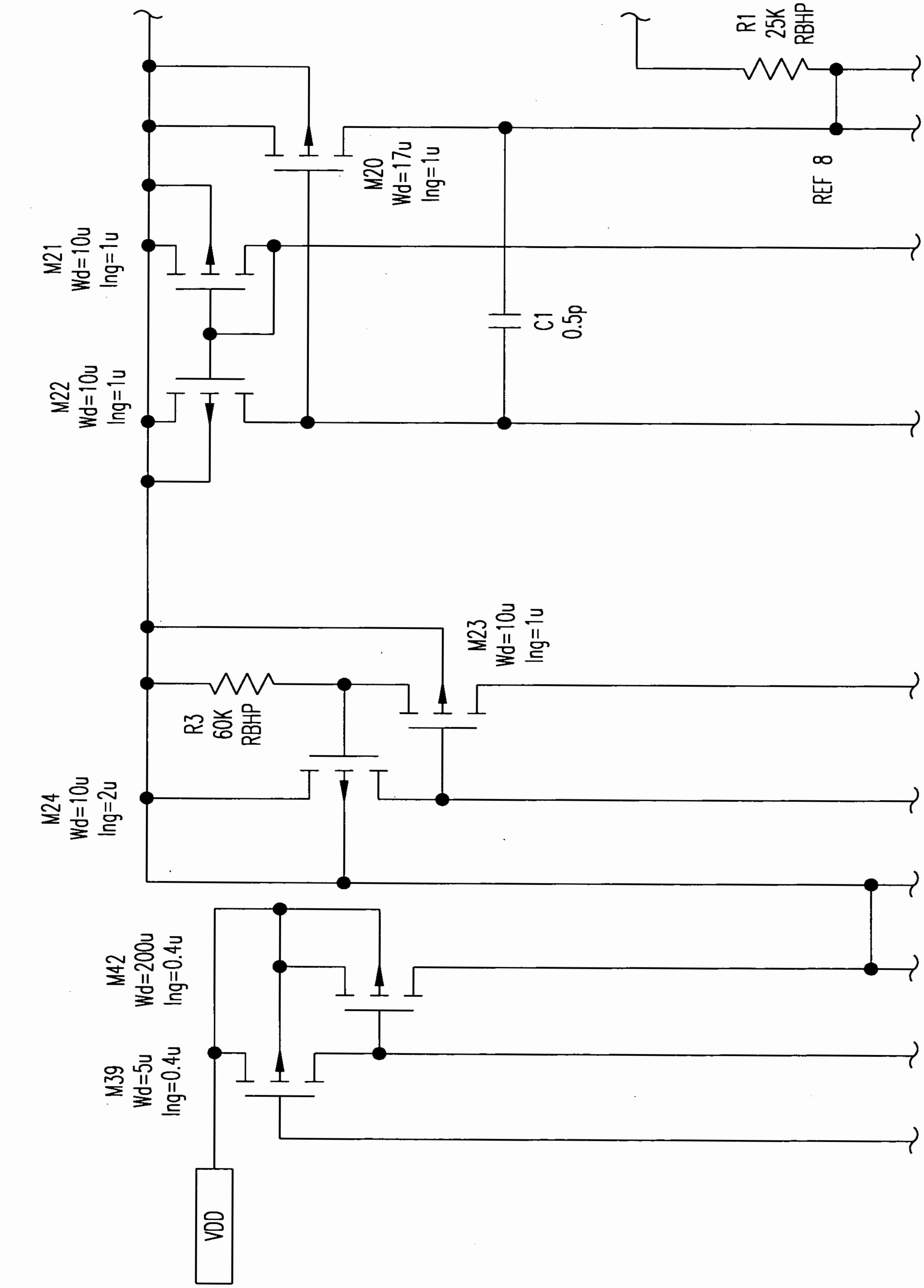

R1
25K
RBHP
M20
Wd=17u
lng=1u
REF 8
M21
Wd=10u
lng=1u
C1
0.5p
M22
Wd=10u
lng=1u
M23
Wd=10u
lng=1u
R3
60K
RBHP
M24
Wd=10u
lng=2u
M42
Wd=200u
lng=0.4u
M39
Wd=5u
lng=0.4u
VDD

FIG.123A

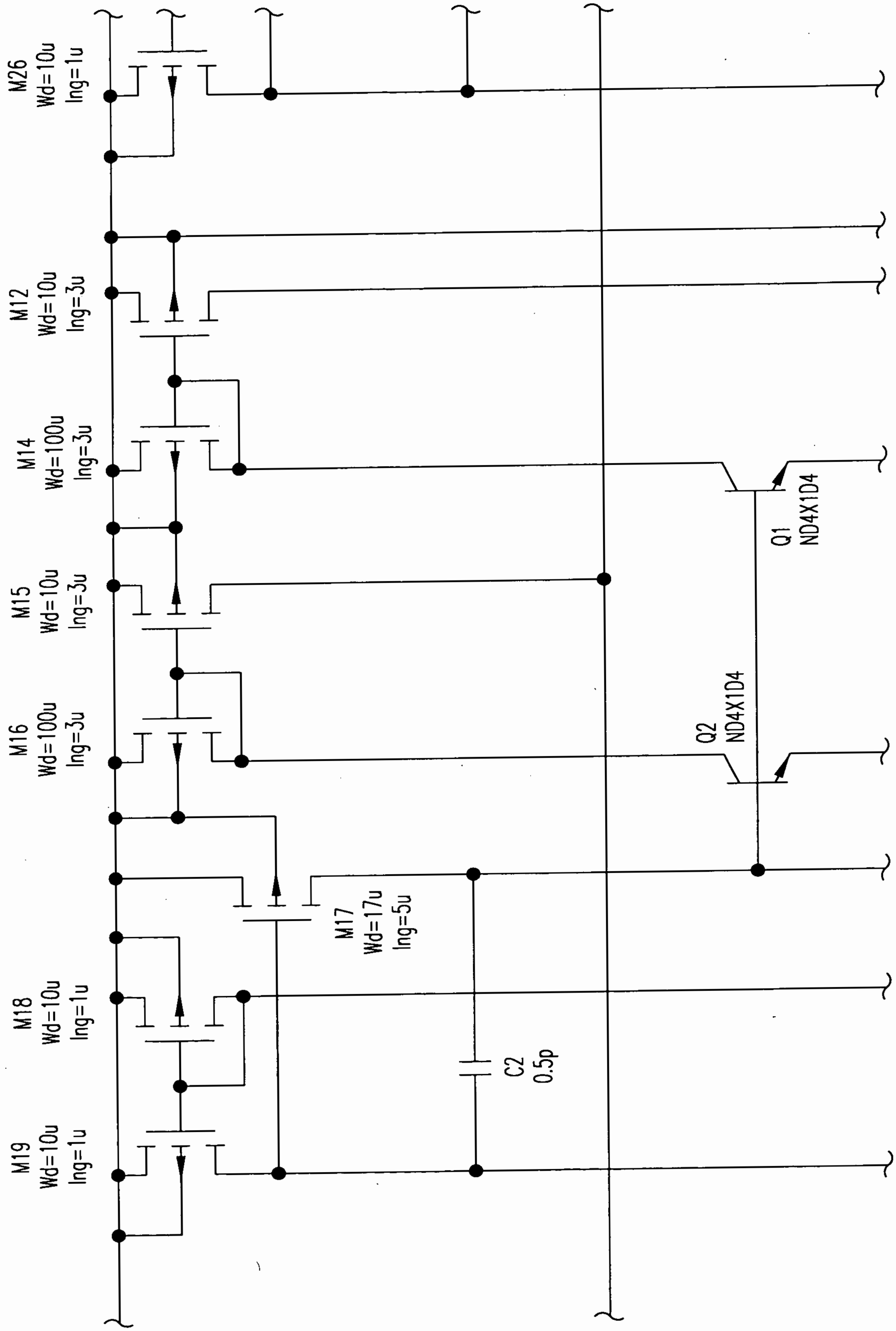

M26
Wd=10u
lng=1u
M12
Wd=10u
lng=3u
M14
Wd=100u
lng=3u
M15
Wd=10u
lng=3u
M16
Wd=100u
lng=3u
M17
Wd=17u
lng=5u
M18
Wd=10u
lng=1u
M19
Wd=10u
lng=1u
Q1
ND4X1D4
Q2
ND4X1D4
C2
0.5p

FIG.123B

New Sheet
Sheet 276 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

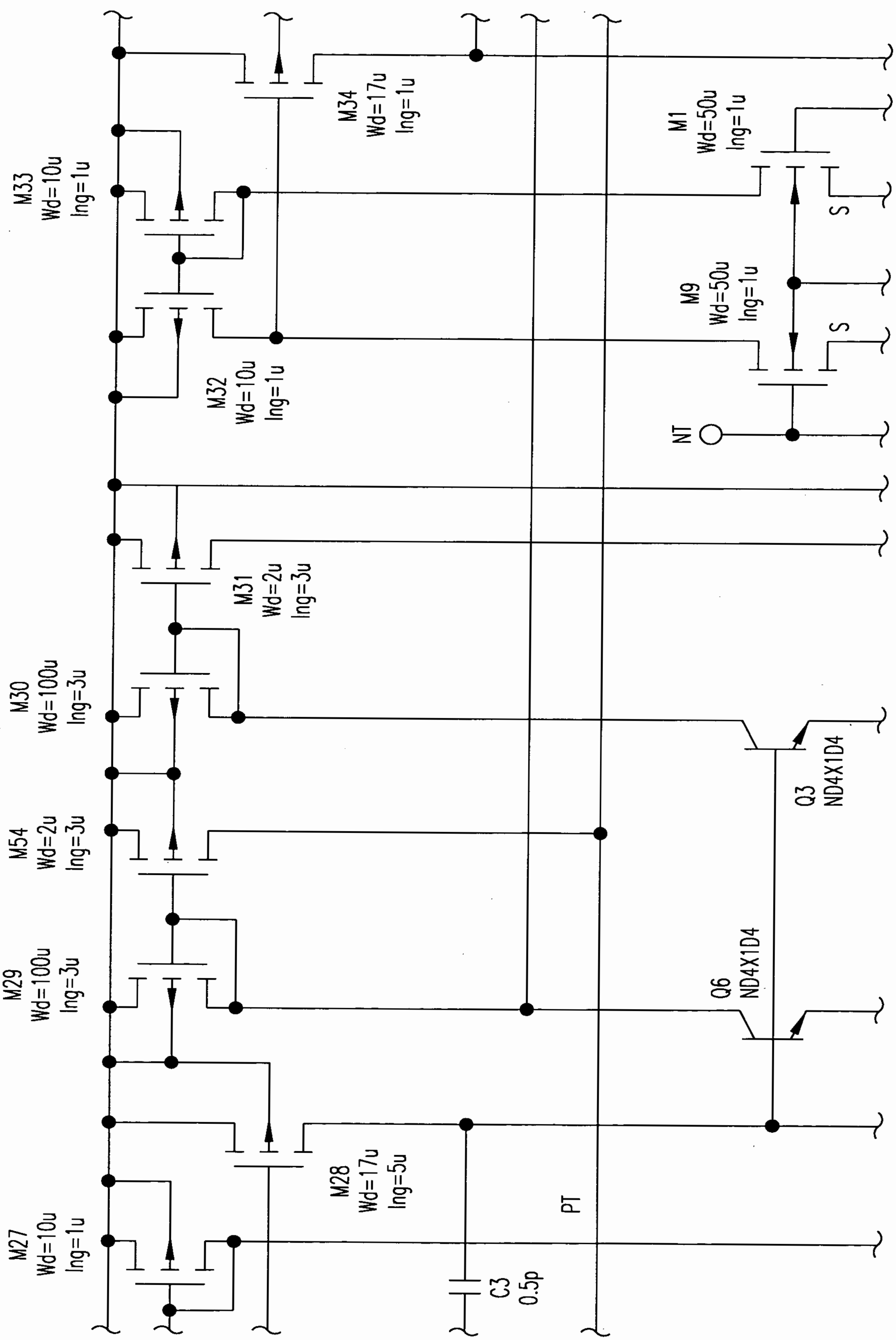


FIG.123C

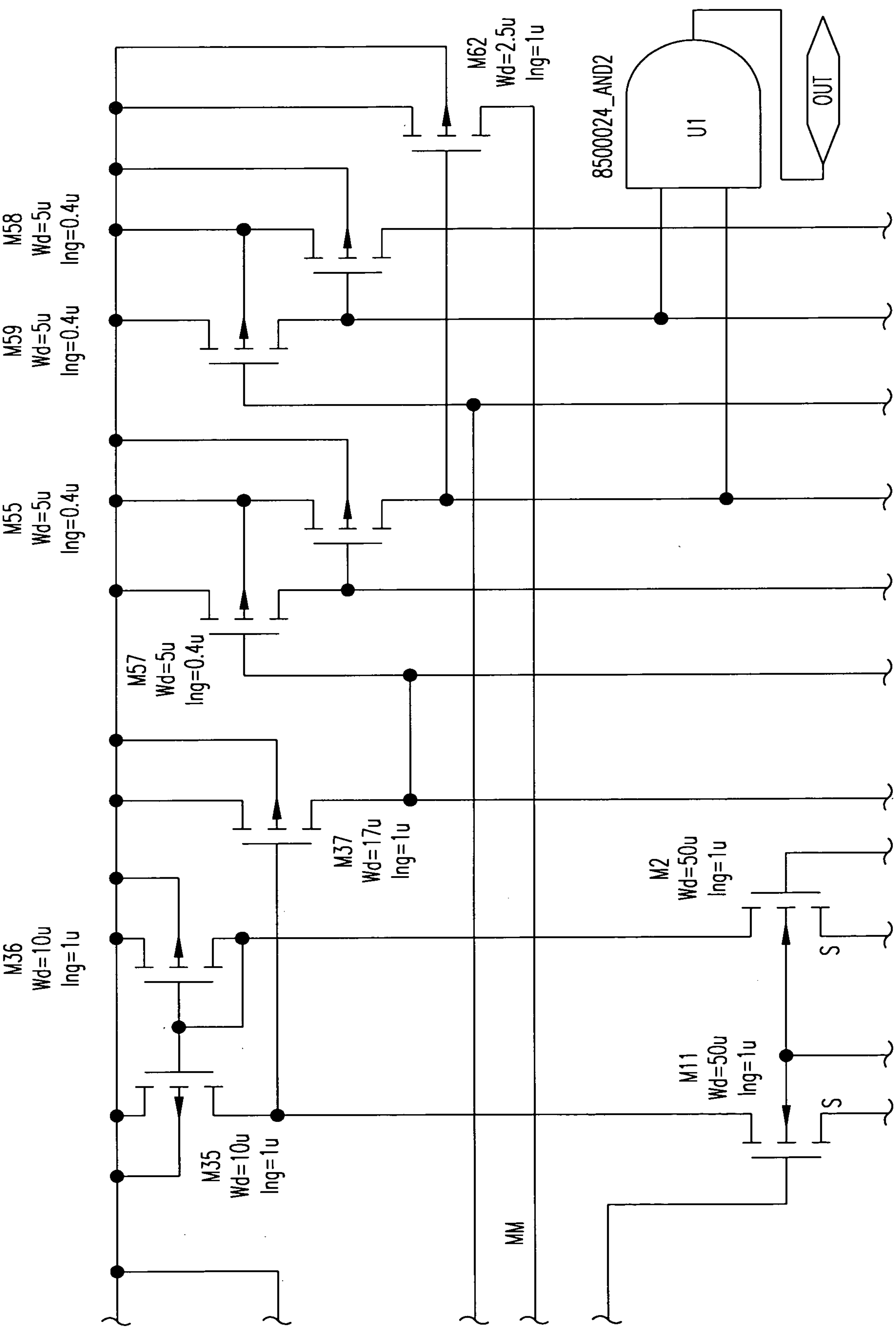

M62
Wd=2.5u
lng=1u
8500024_AND2
U1
OUT
M58
Wd=5u
lng=0.4u
M59
Wd=5u
lng=0.4u
M55
Wd=5u
lng=0.4u
M57
Wd=5u
lng=0.4u
M37
Wd=17u
lng=1u
M36
Wd=10u
lng=1u
M35
Wd=10u
lng=1u
M2
Wd=50u
lng=1u
M11
Wd=50u
lng=1u
S
S
MM

FIG.123D

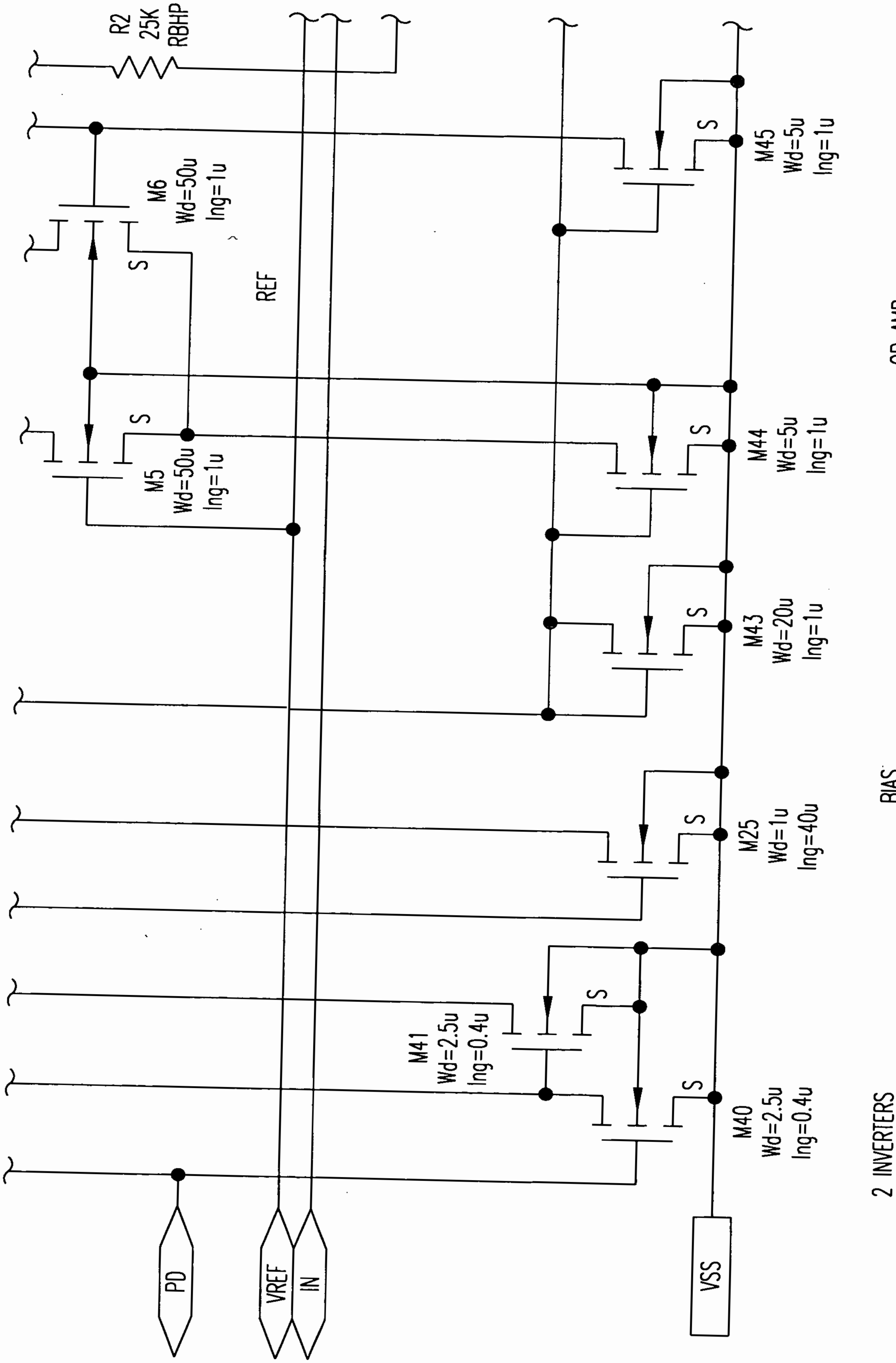

R2
25K
RBHP
M6
Wd=50u
lng=1u
S
REF
M5
Wd=50u
lng=1u
S
M45
Wd=5u
lng=1u
S
M44
Wd=5u
lng=1u
S
M43
Wd=20u
lng=1u
S
OP AMP
M25
Wd=1u
lng=40u
S
BIAS
M41
Wd=2.5u
lng=0.4u
S
M40
Wd=2.5u
lng=0.4u
S
2 INVERTERS
PD
VREF
IN
VSS

FIG.123E

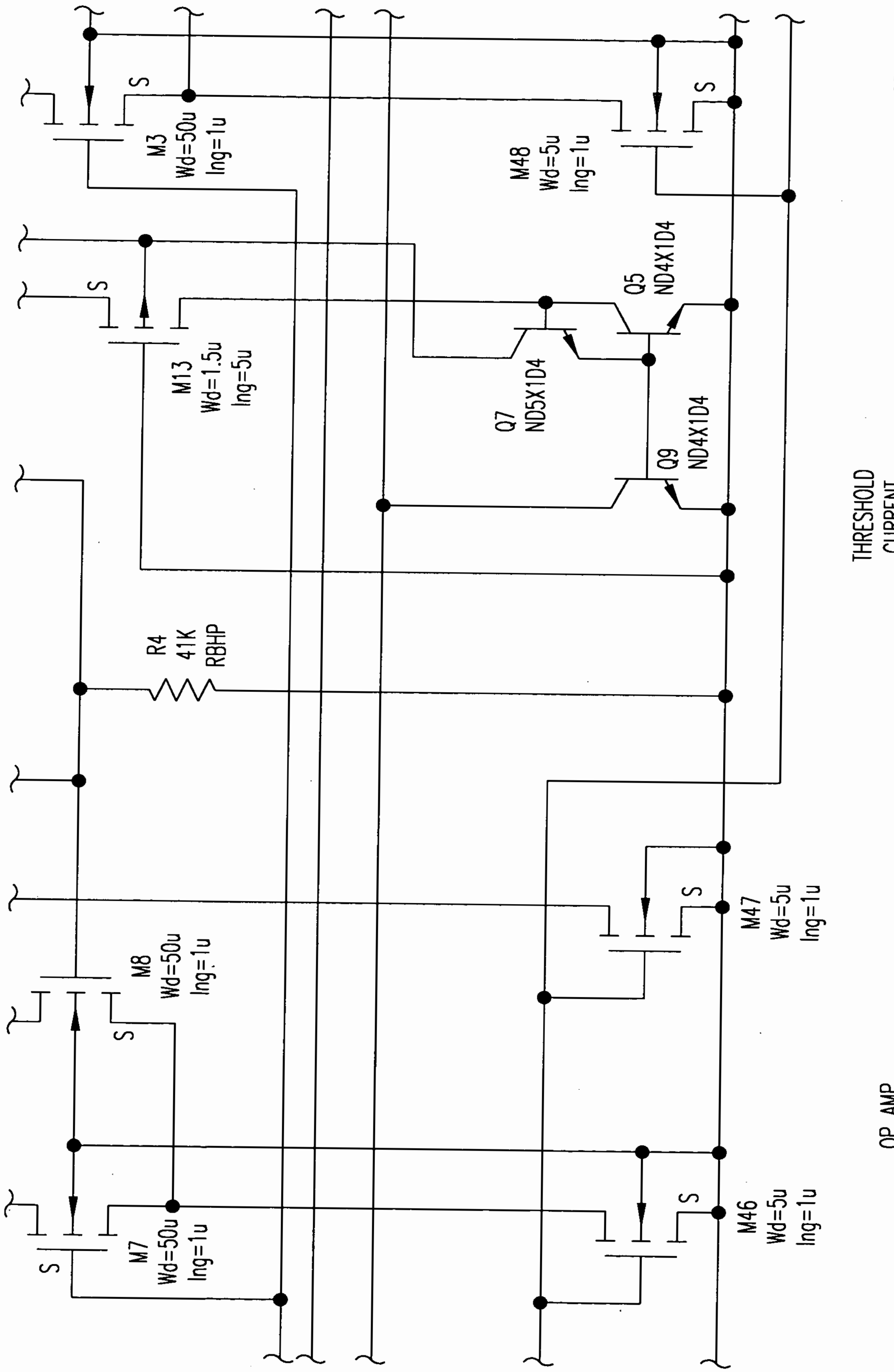

M3
Wd=50u
lng=1u
M48
Wd=5u
lng=1u
Q5
ND4X1D4
M13
Wd=1.5u
lng=5u
Q7
ND5X1D4
Q9
ND4X1D4
R4
41K
RBHP
M47
Wd=5u
lng=1u
M8
Wd=50u
lng=1u
M7
Wd=50u
lng=1u
M46
Wd=5u
lng=1u
S
OP AMP
THRESHOLD
CURRENT
SOURCE
OP AMP

FIG.123F

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

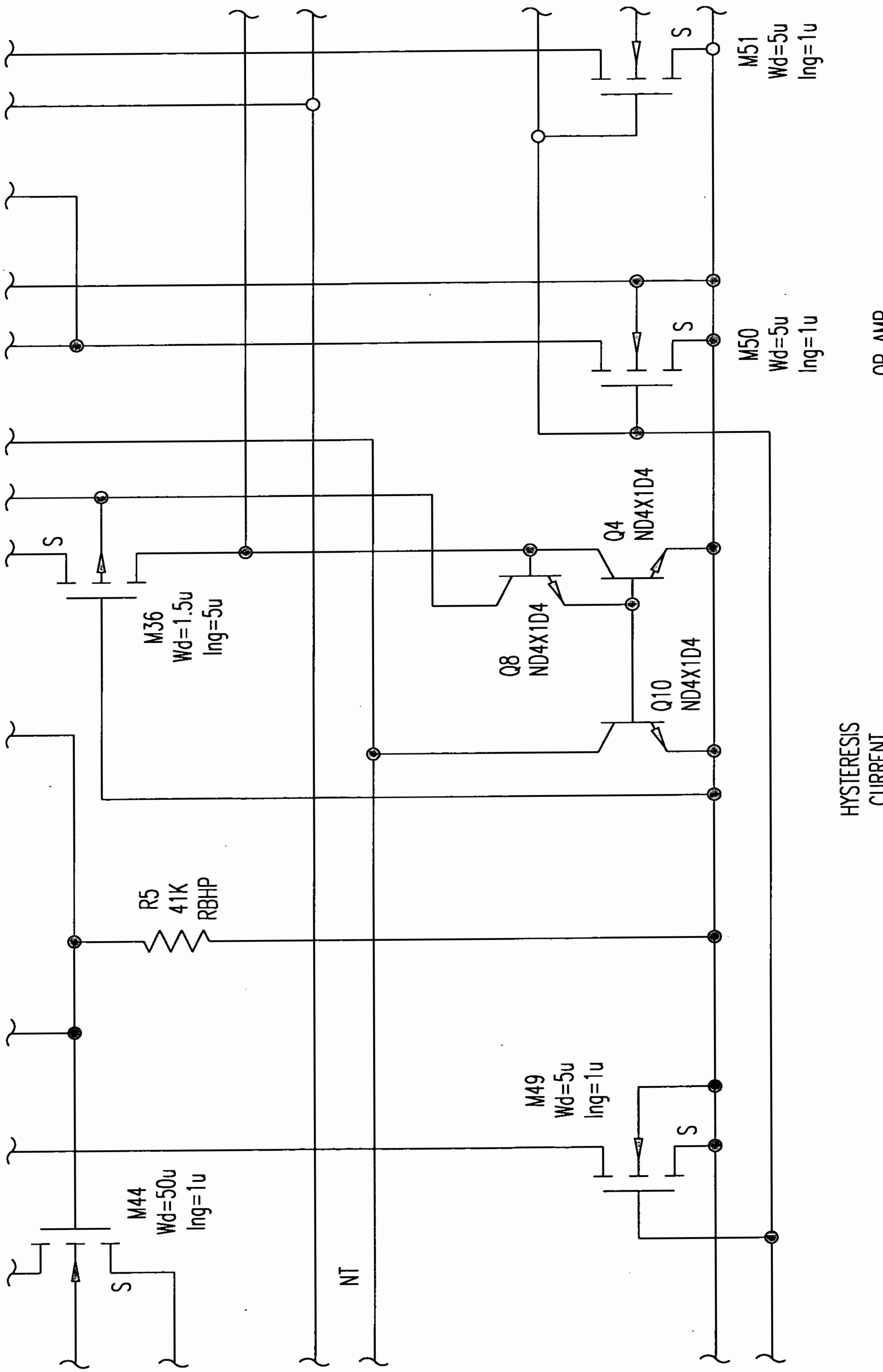


FIG. 123G

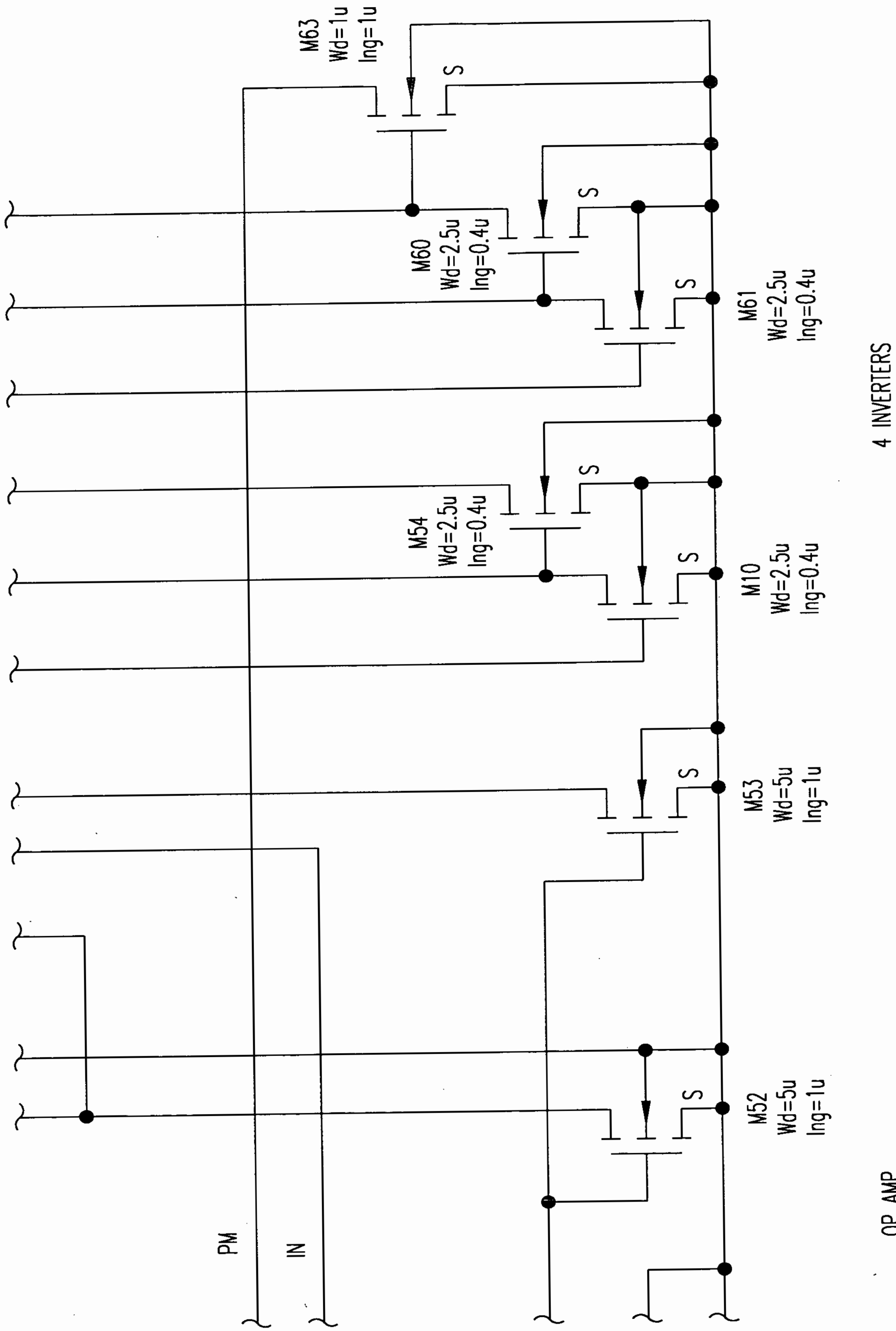

M63
Wd=1u
lng=1u
S
M60
Wd=2.5u
lng=0.4u
S
M61
Wd=2.5u
lng=0.4u
S
4 INVERTERS
M54
Wd=2.5u
lng=0.4u
S
M10
Wd=2.5u
lng=0.4u
S
M53
Wd=5u
lng=1u
S
M52
Wd=5u
lng=1u
S
OP AMP
PM
IN

FIG.123H

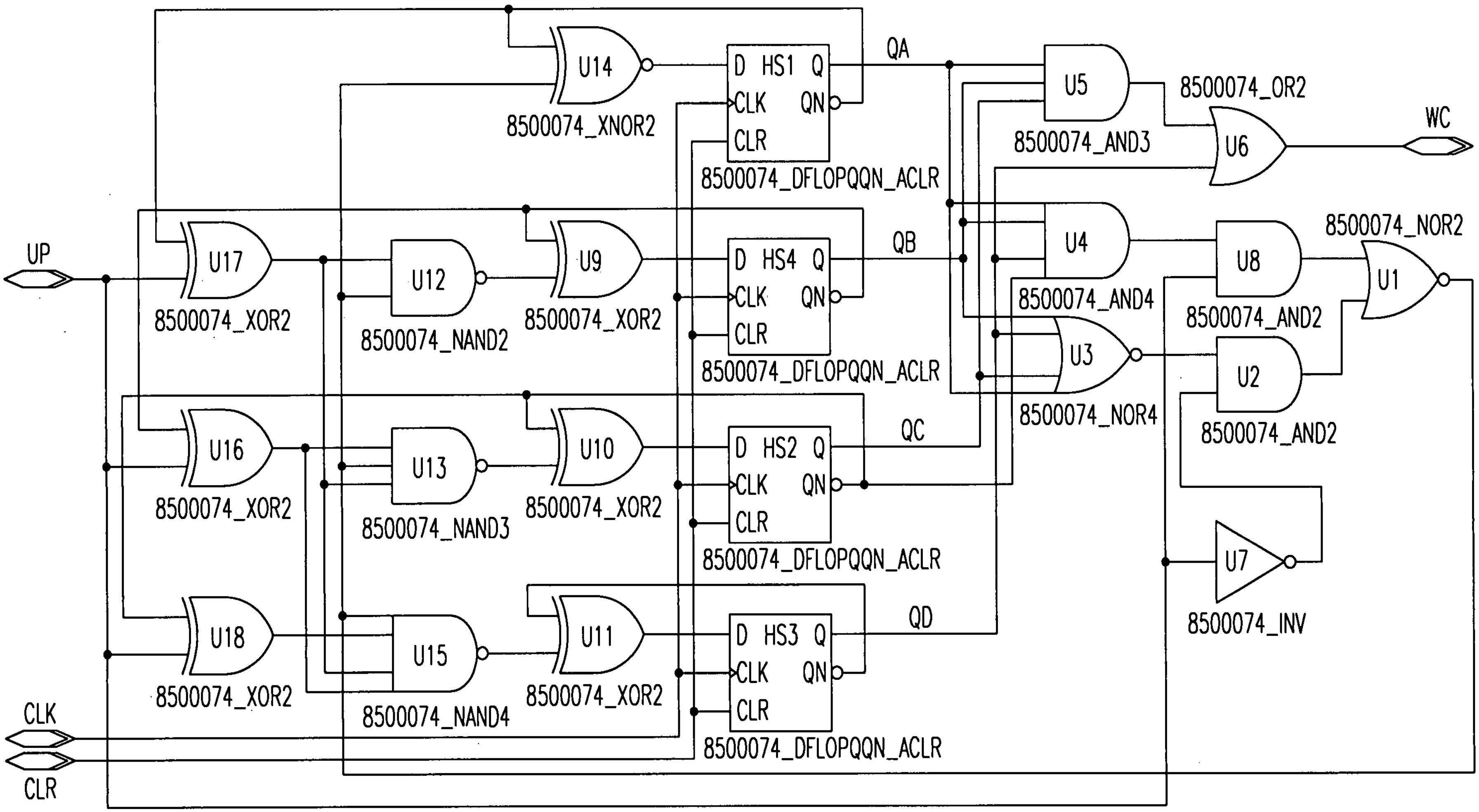

U14
8500074_XNOR2
D HS1 Q
CLK QN
CLR
8500074_DFLOPQQN_ACLR
QA
U5
8500074_AND3
8500074_OR2
U6
WC
UP
U17
8500074_XOR2
U12
8500074_NAND2
U9
8500074_XOR2
D HS4 Q
CLK QN
CLR
8500074_DFLOPQQN_ACLR
QB
U4
8500074_AND4
U8
8500074_AND2
8500074_NOR2
U1
U3
8500074_NOR4
U2
8500074_AND2
U16
8500074_XOR2
U13
8500074_NAND3
U10
8500074_XOR2
D HS2 Q
CLK QN
CLR
8500074_DFLOPQQN_ACLR
QC
U7
8500074_INV
U18
8500074_XOR2
U15
8500074_NAND4
U11
8500074_XOR2
D HS3 Q
CLK QN
CLR
8500074_DFLOPQQN_ACLR
QD
CLK
CLR

FIG. 124

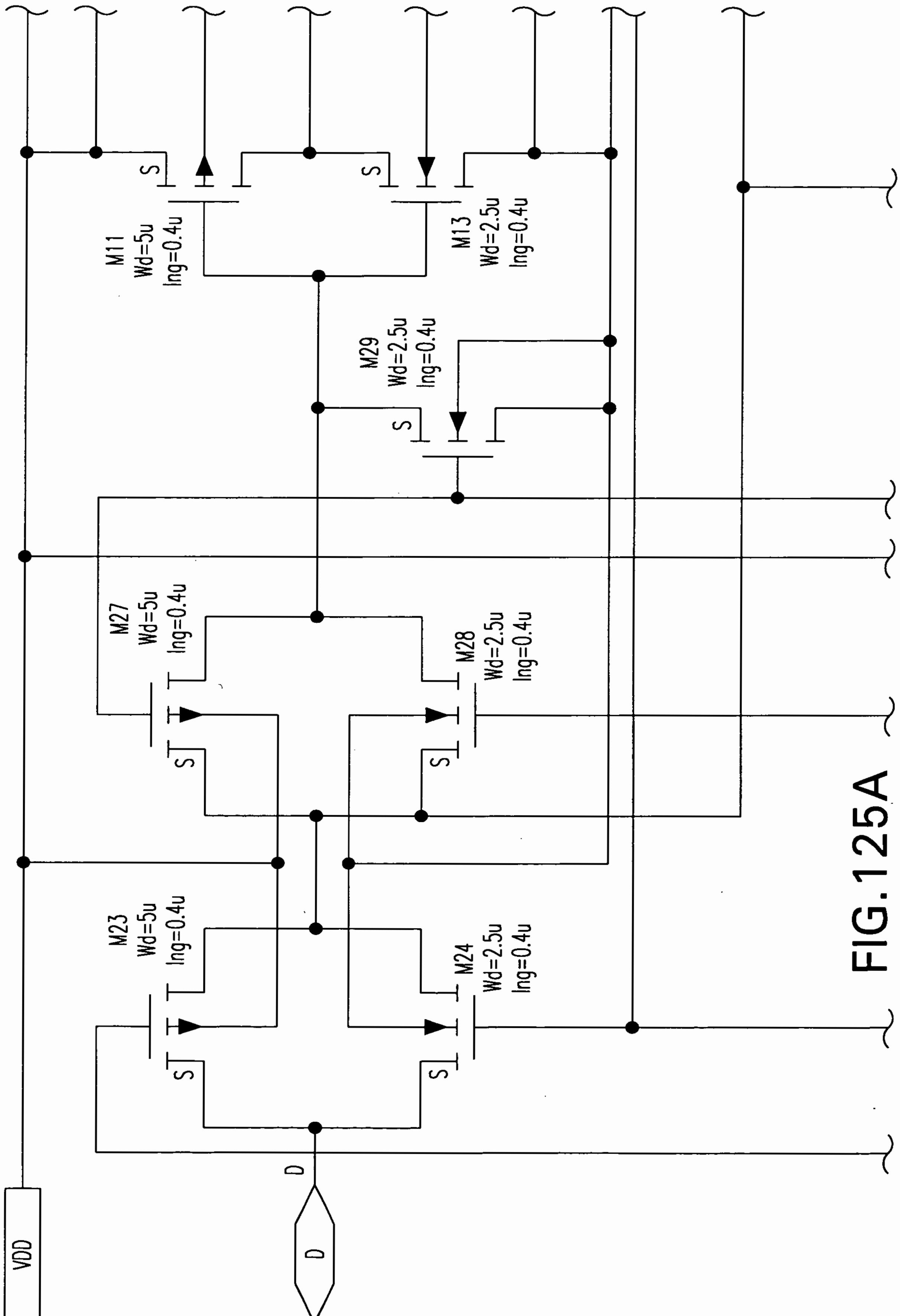

M11
Wd=5u
lng=0.4u
M13
Wd=2.5u
lng=0.4u
M29
Wd=2.5u
lng=0.4u
M27
Wd=5u
lng=0.4u
M28
Wd=2.5u
lng=0.4u
M23
Wd=5u
lng=0.4u
M24
Wd=2.5u
lng=0.4u
S
D
D
VDD

FIG.125A

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

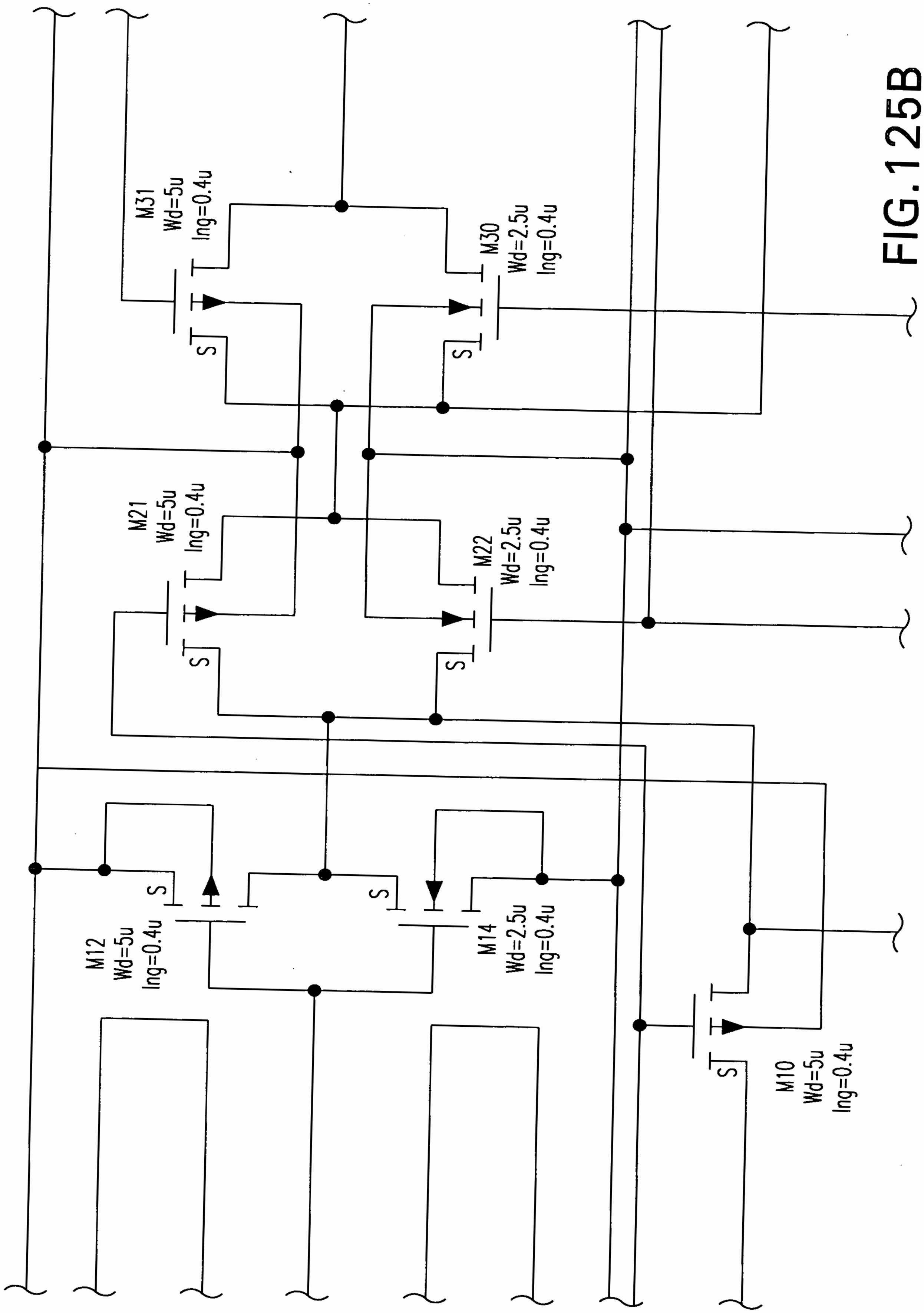


FIG.125B

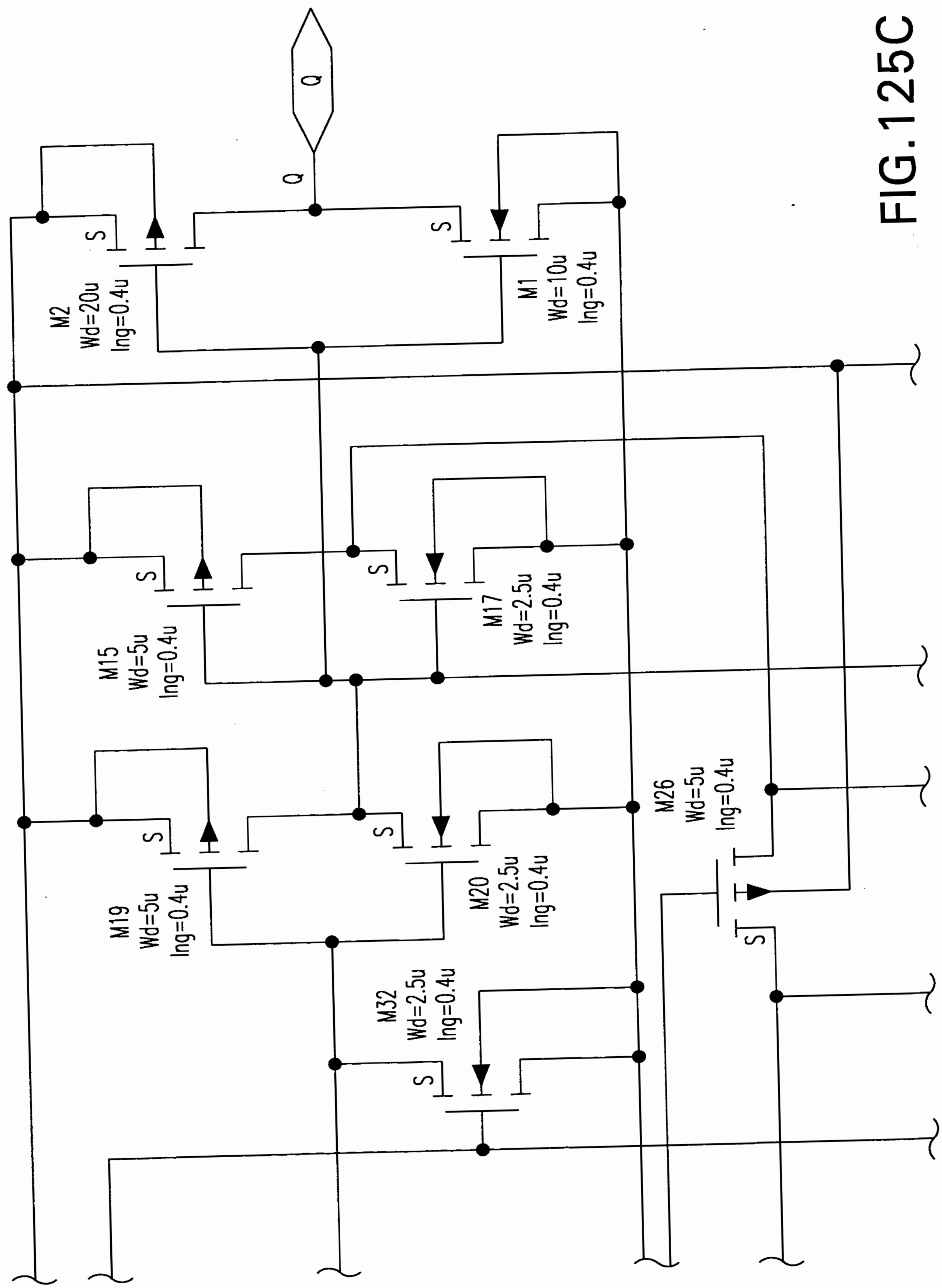

Q
Q
M2
Wd=20u
lng=0.4u
M1
Wd=10u
lng=0.4u
M15
Wd=5u
lng=0.4u
M17
Wd=2.5u
lng=0.4u
M19
Wd=5u
lng=0.4u
M20
Wd=2.5u
lng=0.4u
M26
Wd=5u
lng=0.4u
M32
Wd=2.5u
lng=0.4u
S

FIG.125C

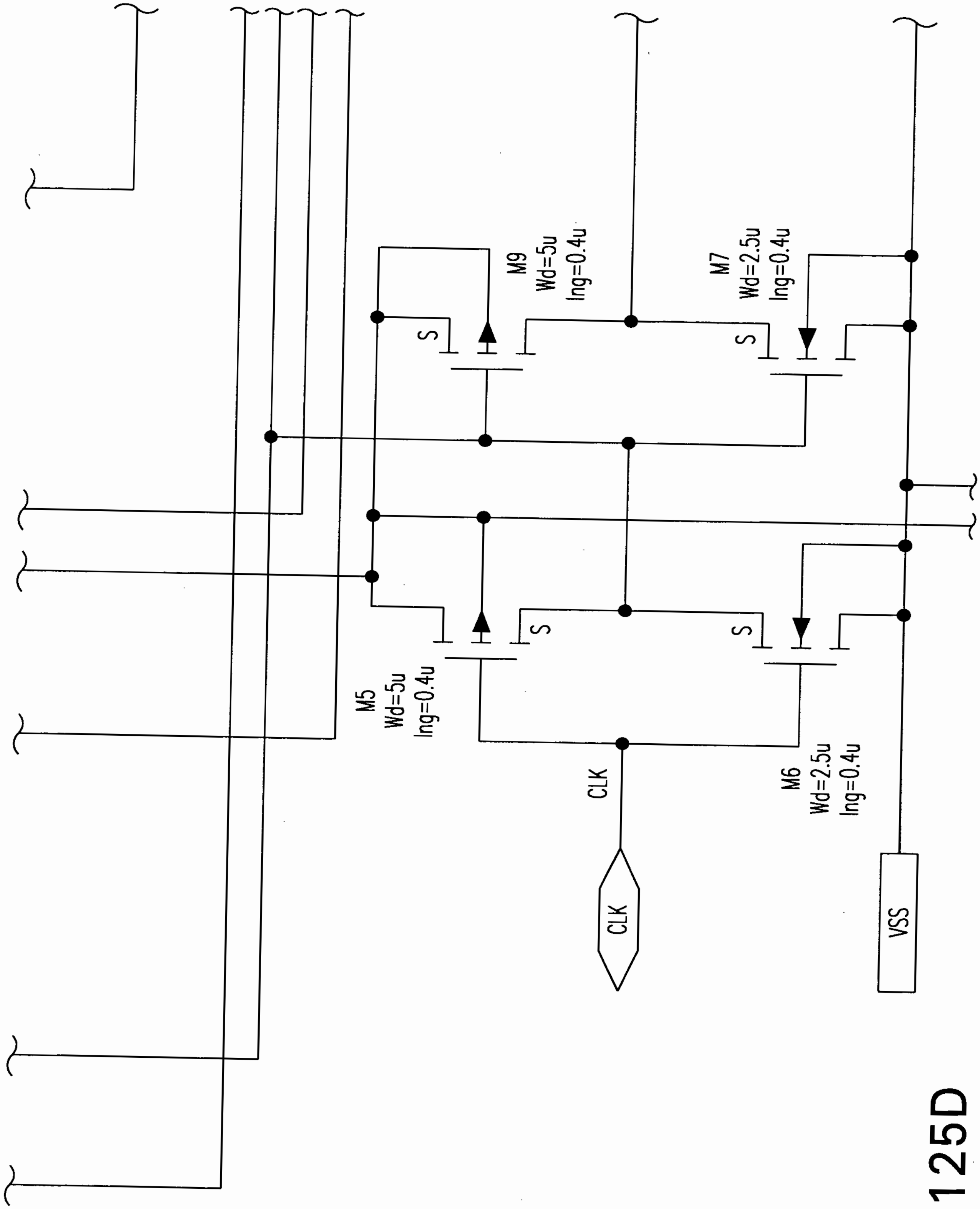

M9
Wd=5u
lng=0.4u
S
M7
Wd=2.5u
lng=0.4u
S
S
S
M5
Wd=5u
lng=0.4u
CLK
CLK
M6
Wd=2.5u
lng=0.4u
VSS

FIG.125D

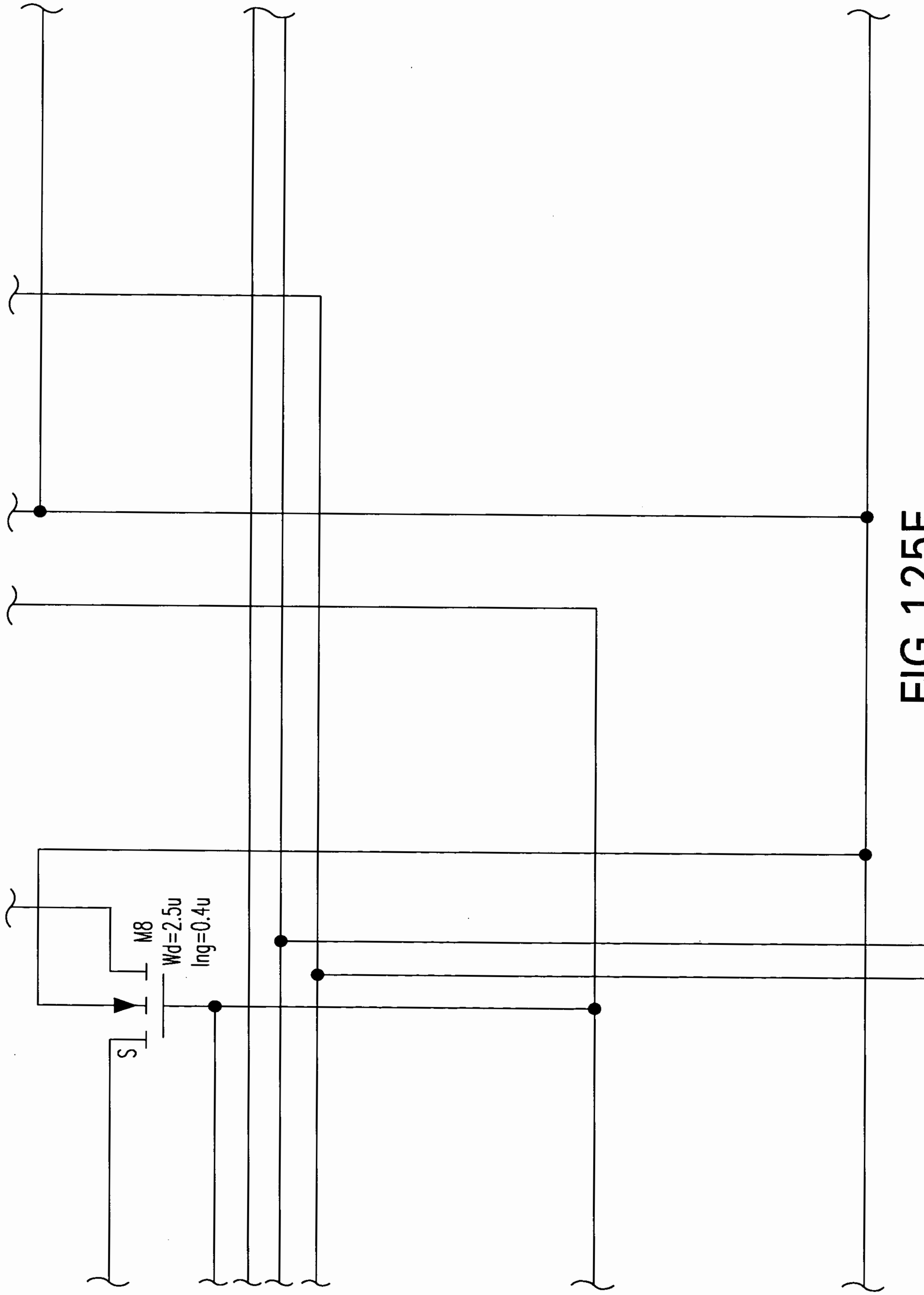


FIG.125E

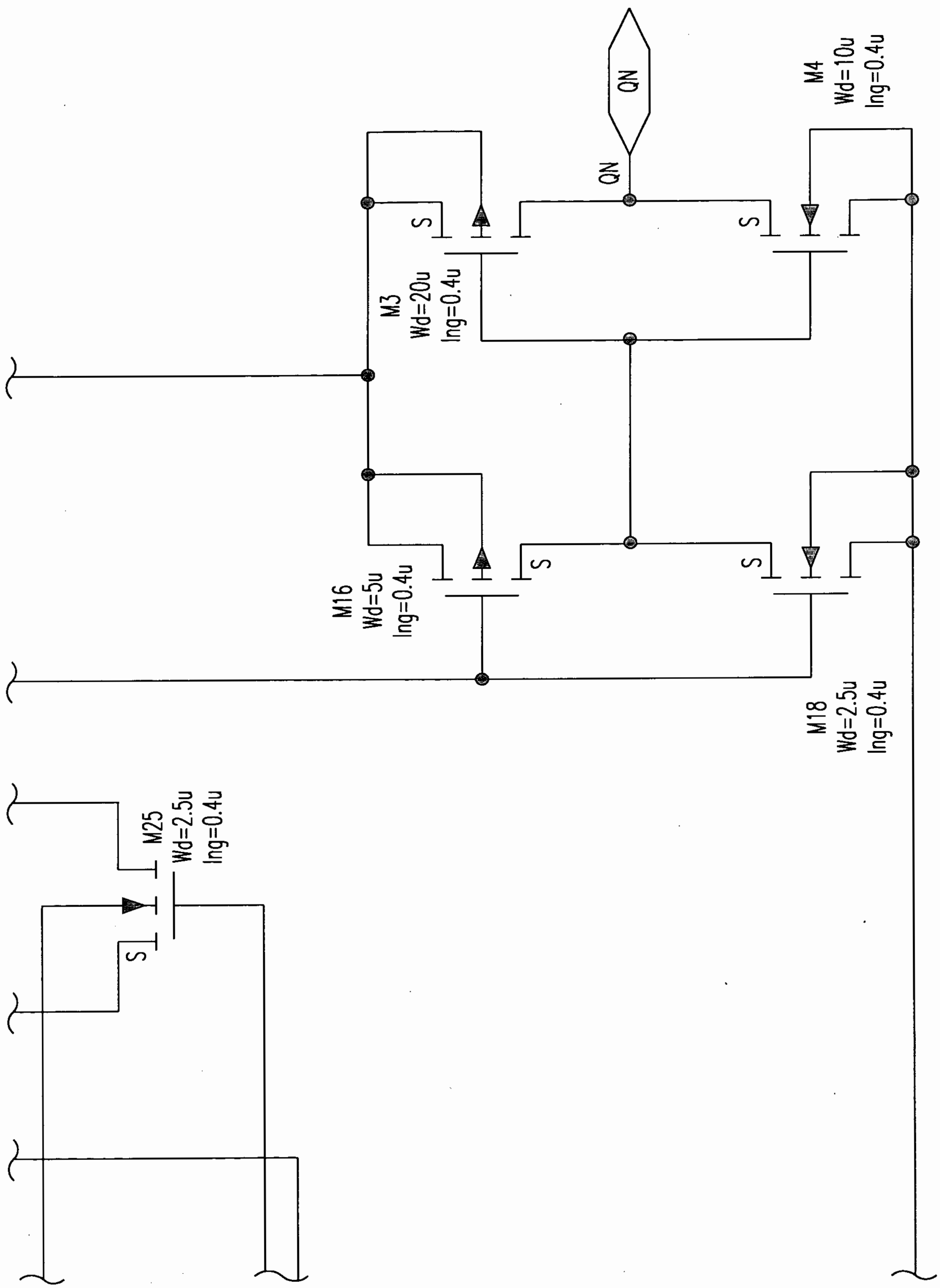

QN
QN
M4
Wd=10u
lng=0.4u
M3
Wd=20u
lng=0.4u
M16
Wd=5u
lng=0.4u
M18
Wd=2.5u
lng=0.4u
M25
Wd=2.5u
lng=0.4u
S
S
S
S
S
S

FIG.125F

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

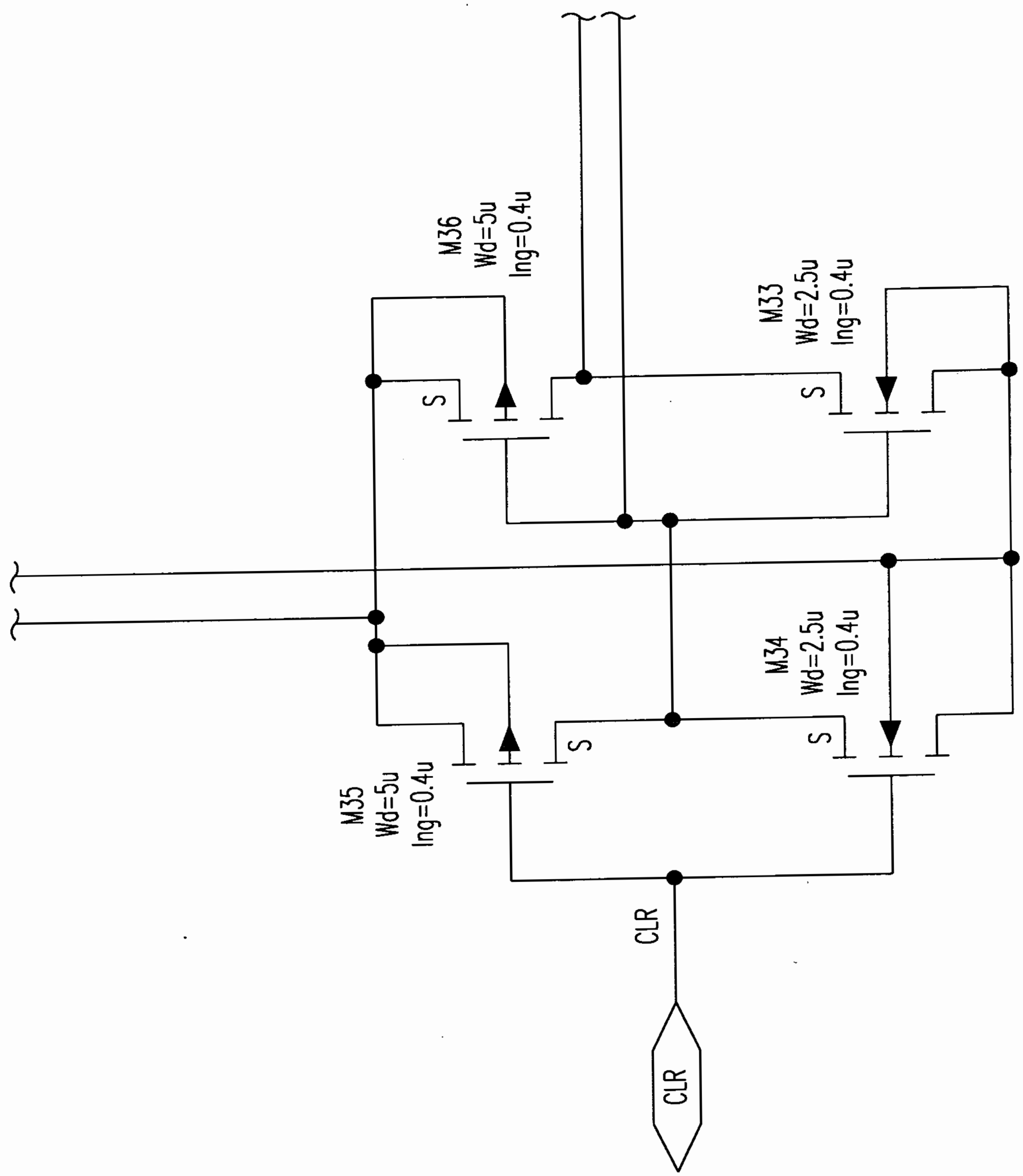
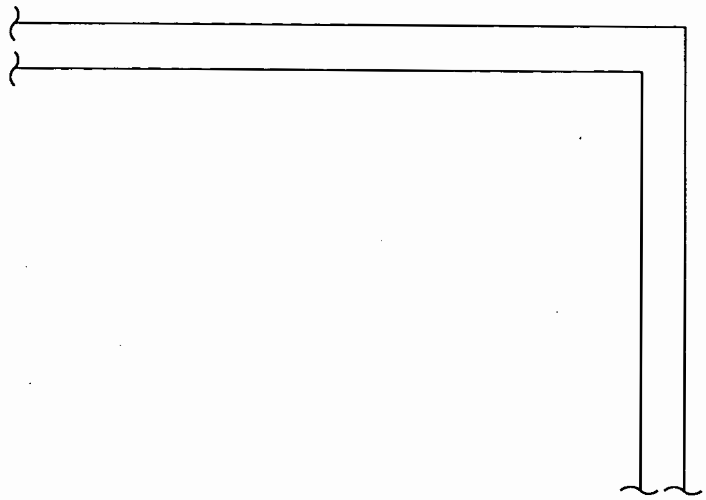


FIG.125G

FIG.125H



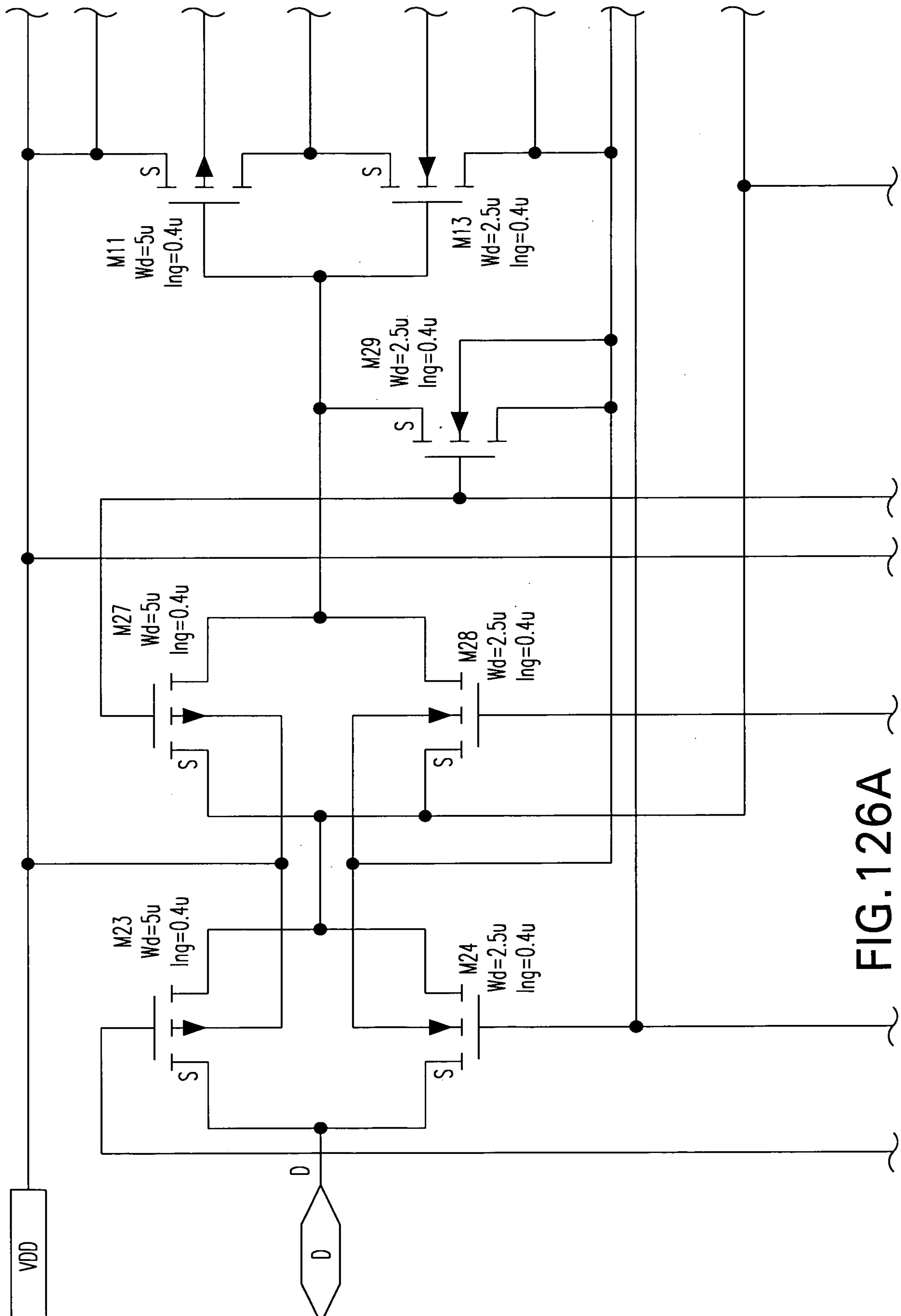

M11
Wd=5u
lng=0.4u
M13
Wd=2.5u
lng=0.4u
M29
Wd=2.5u
lng=0.4u
M27
Wd=5u
lng=0.4u
M28
Wd=2.5u
lng=0.4u
M23
Wd=5u
lng=0.4u
M24
Wd=2.5u
lng=0.4u
S
D
D
VDD

FIG.126A

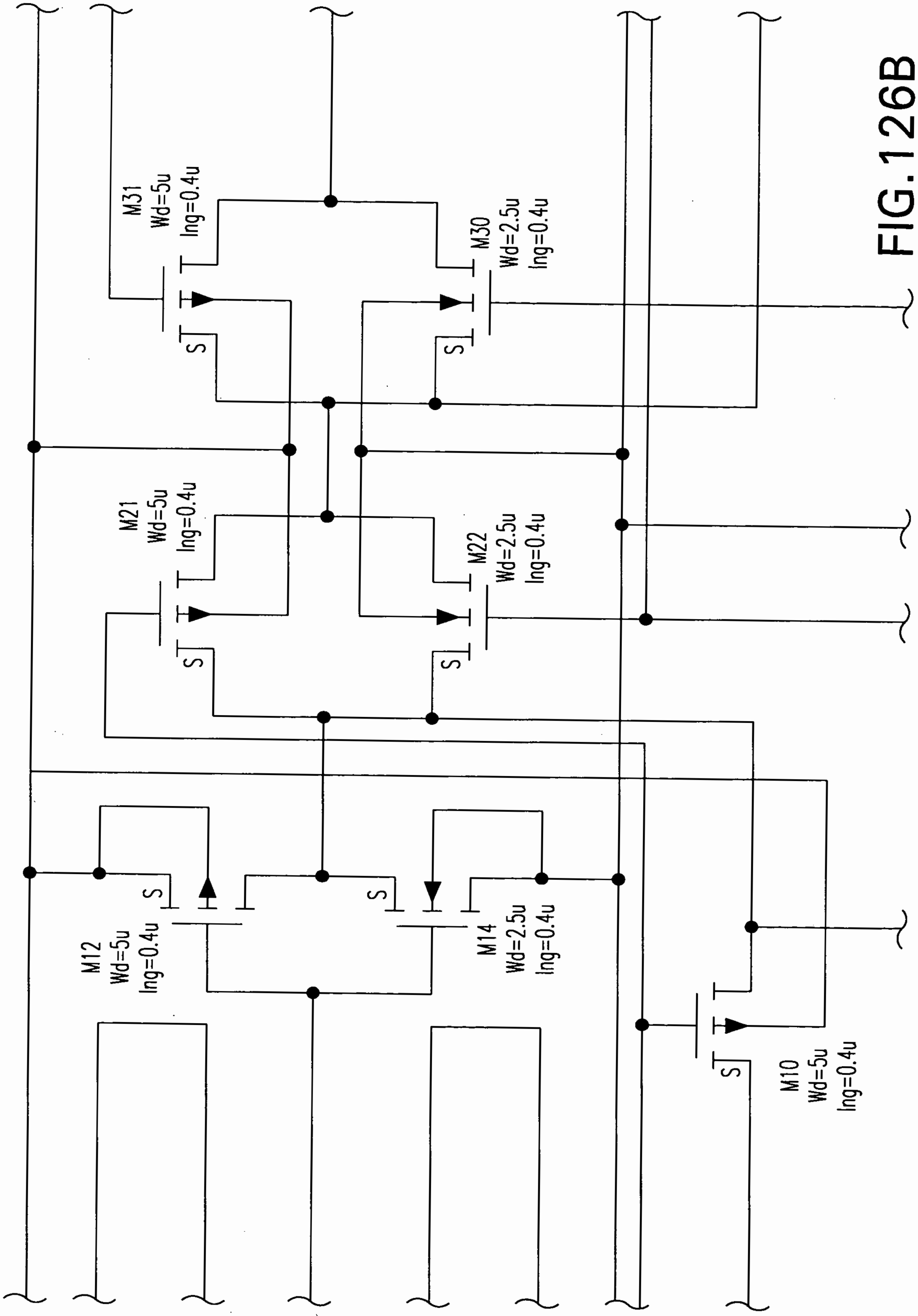

M31
Wd=5u
lng=0.4u
S
M30
Wd=2.5u
lng=0.4u
S
M21
Wd=5u
lng=0.4u
S
M22
Wd=2.5u
lng=0.4u
S
S
M12
Wd=5u
lng=0.4u
S
M14
Wd=2.5u
lng=0.4u
S
M10
Wd=5u
lng=0.4u

FIG.126B

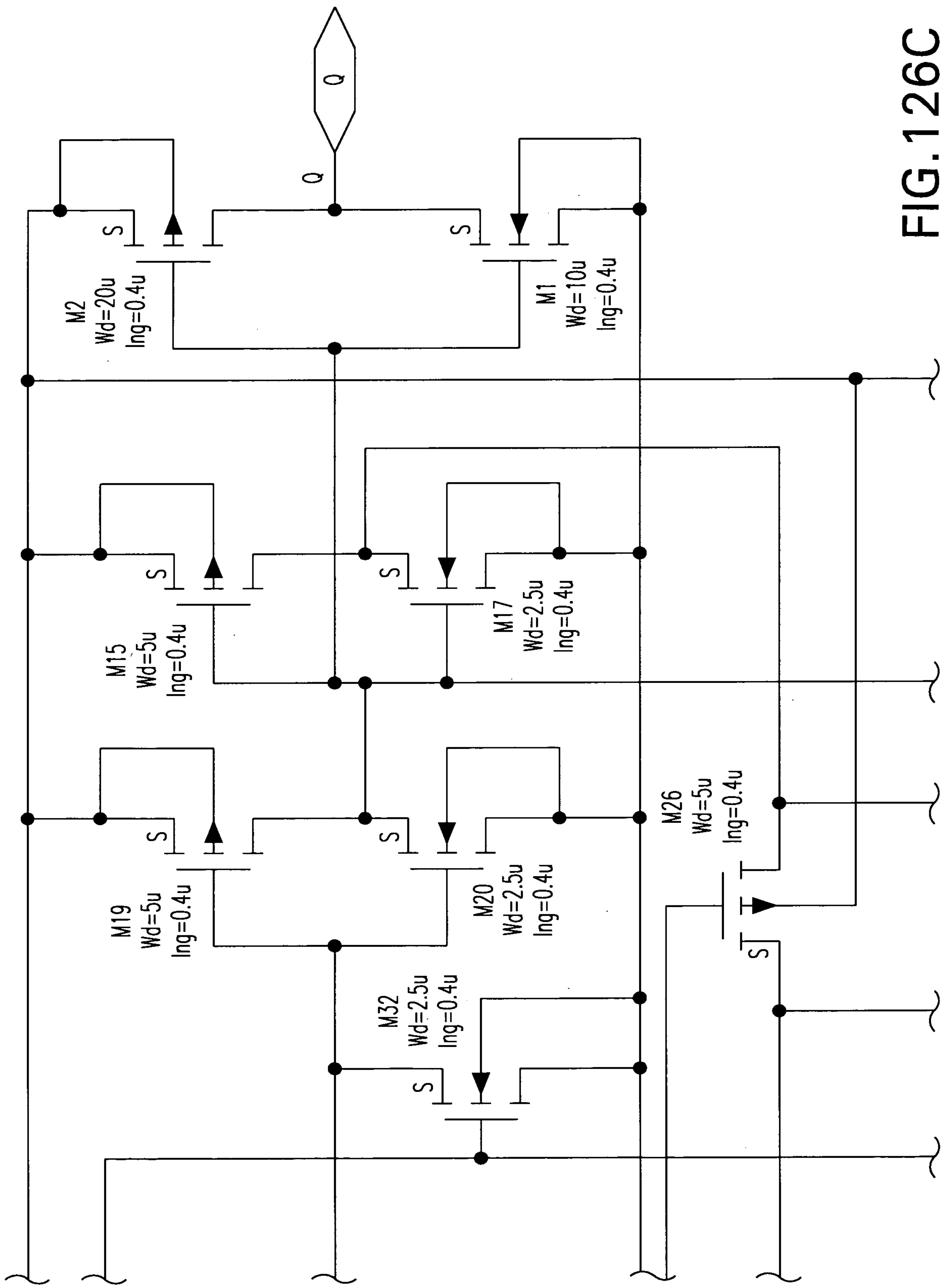

Q
Q
M2
Wd=20u
lng=0.4u
M1
Wd=10u
lng=0.4u
M15
Wd=5u
lng=0.4u
M17
Wd=2.5u
lng=0.4u
M19
Wd=5u
lng=0.4u
M20
Wd=2.5u
lng=0.4u
M26
Wd=5u
lng=0.4u
M32
Wd=2.5u
lng=0.4u
S

FIG.126C

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

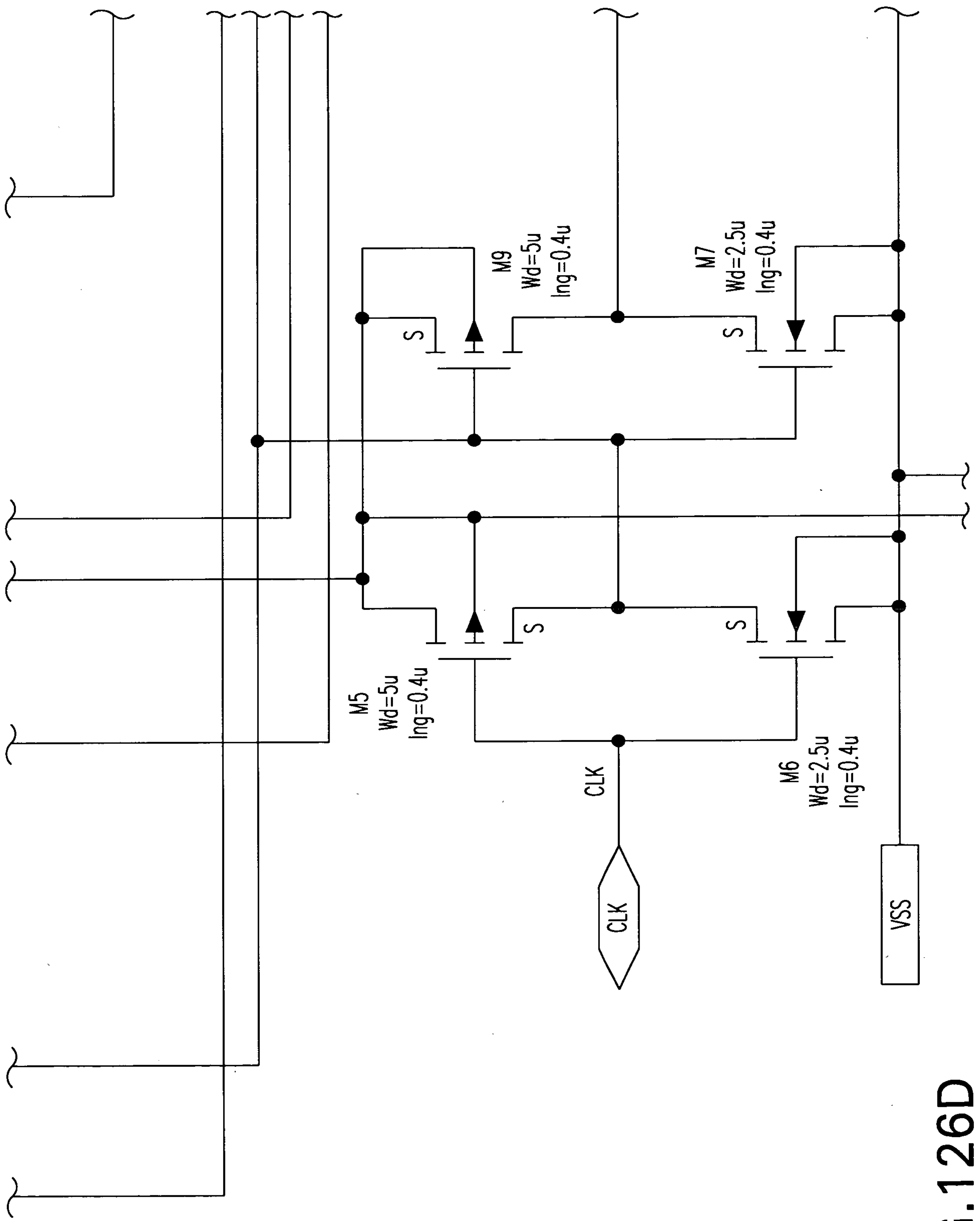


FIG.126D

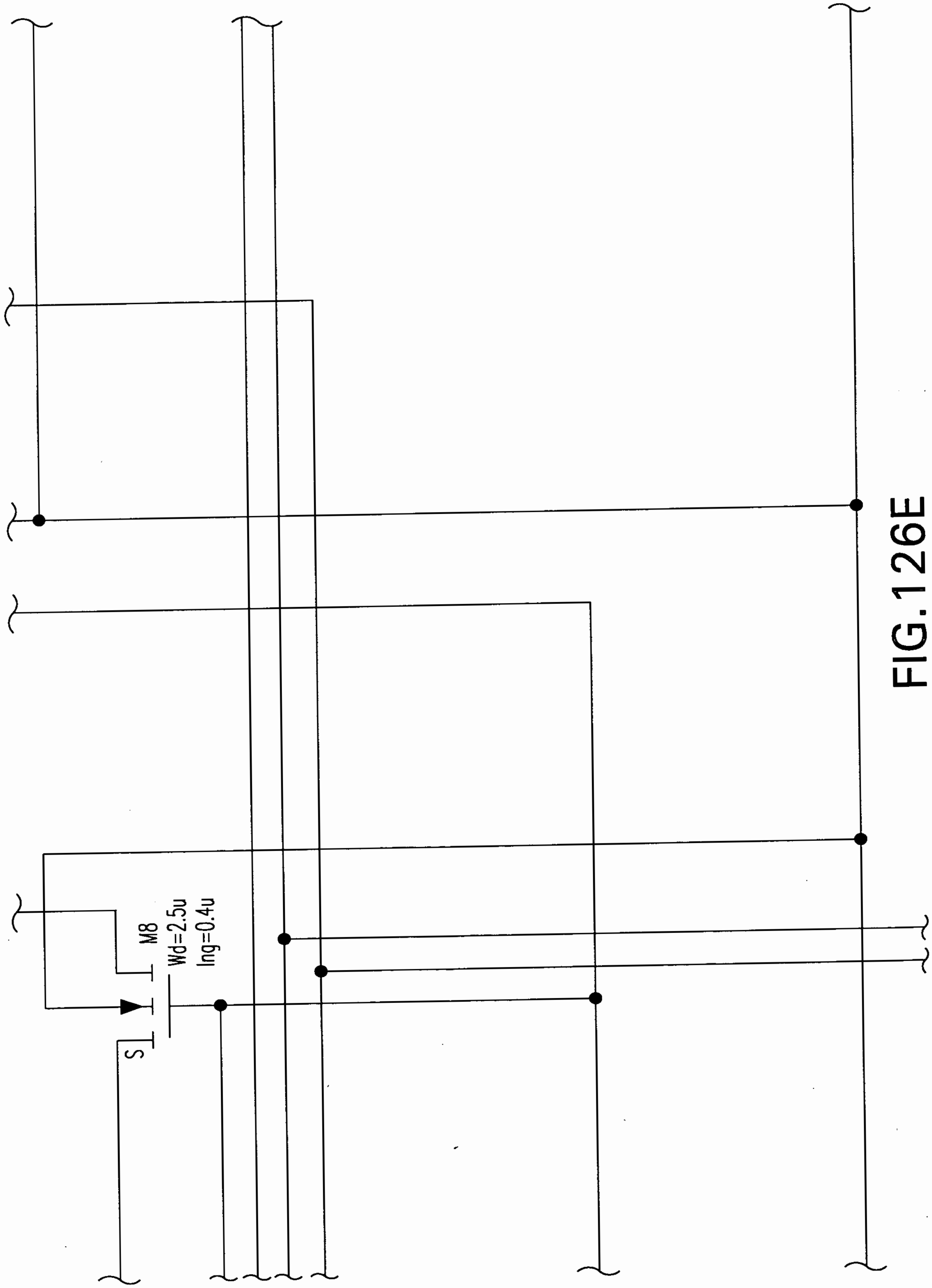


FIG.126E

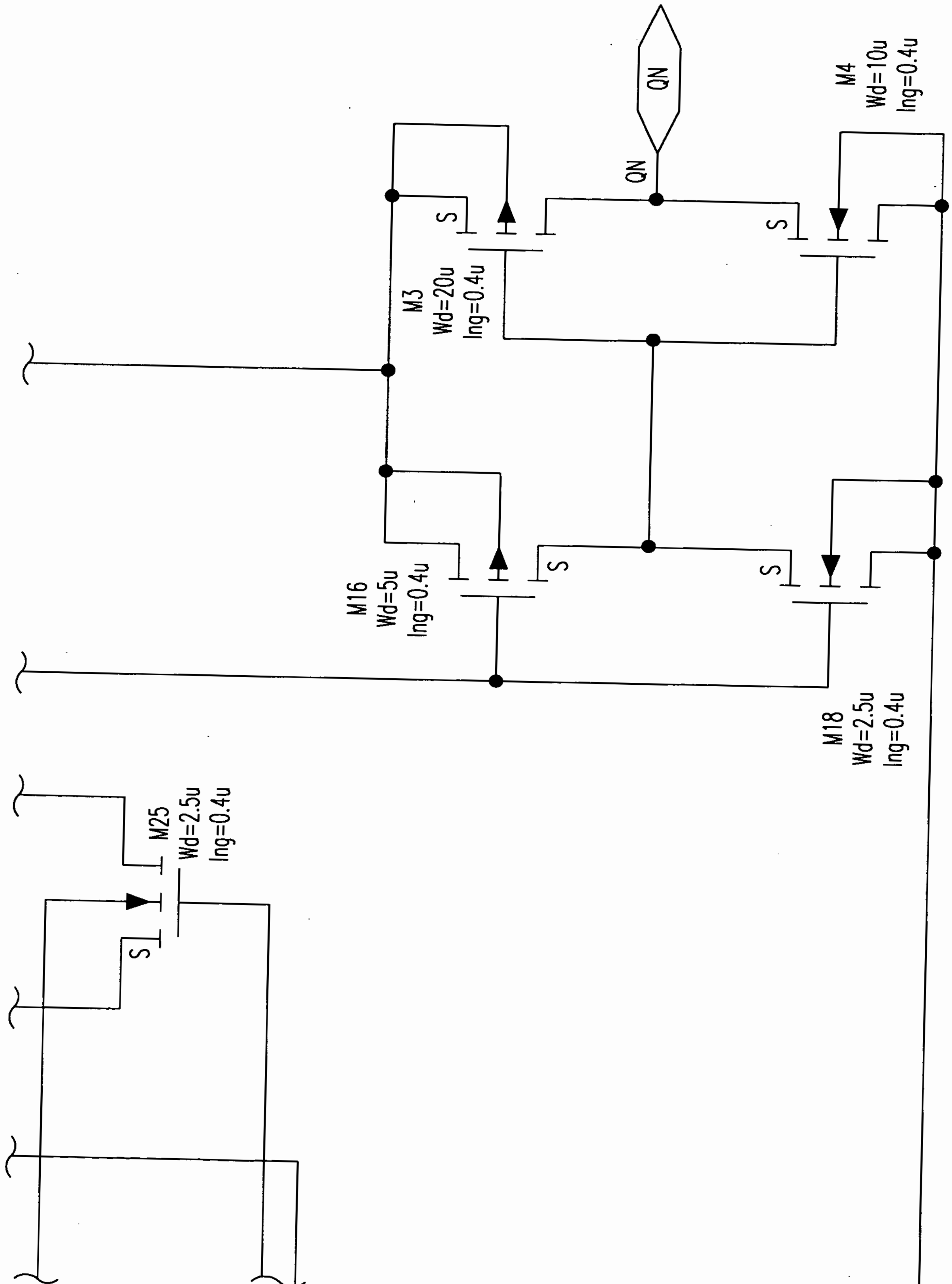

QN
QN
M4
Wd=10u
lng=0.4u
S
S
M3
Wd=20u
lng=0.4u
M16
Wd=5u
lng=0.4u
S
S
M18
Wd=2.5u
lng=0.4u
M25
Wd=2.5u
lng=0.4u
S

FIG.126F

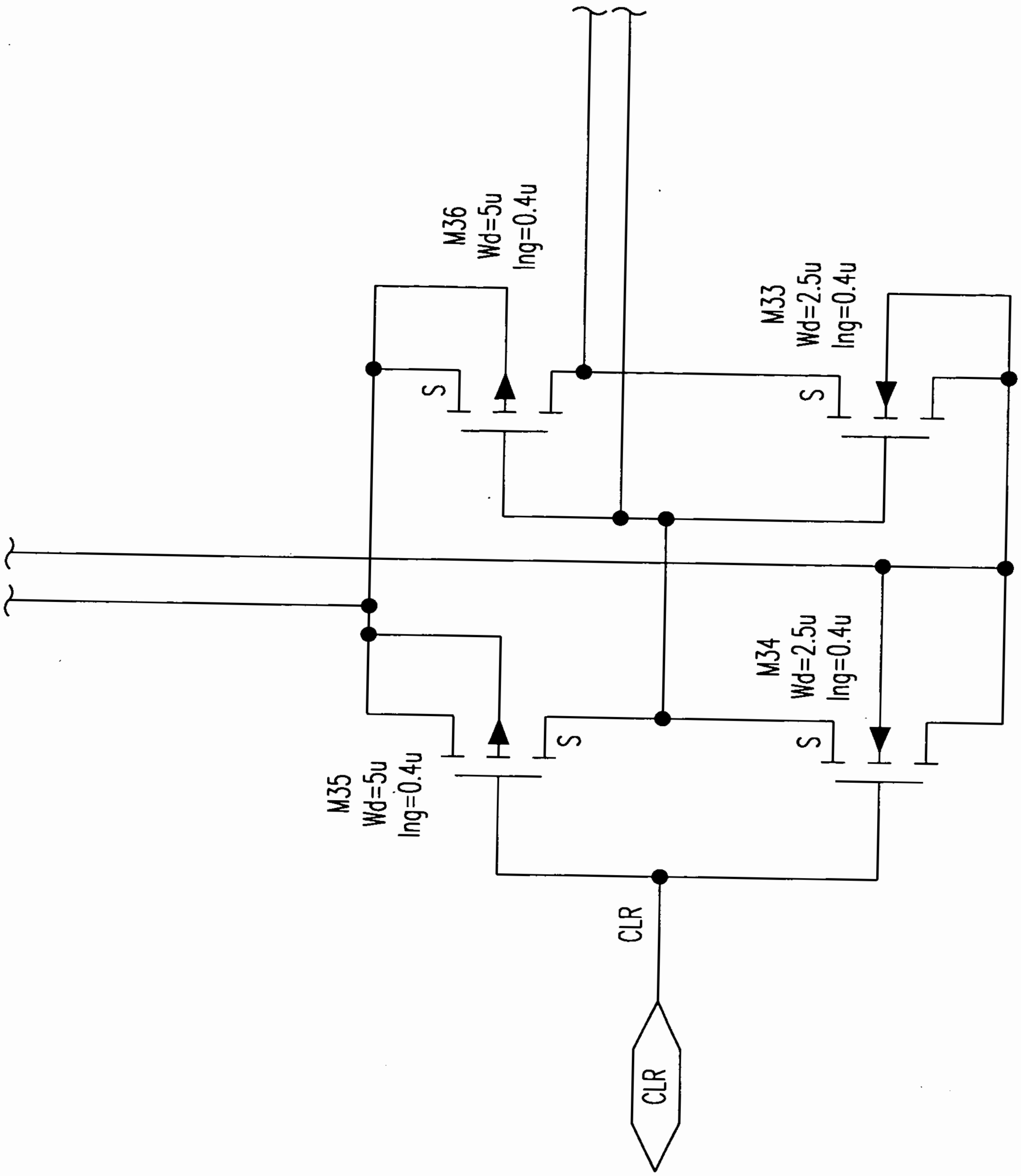
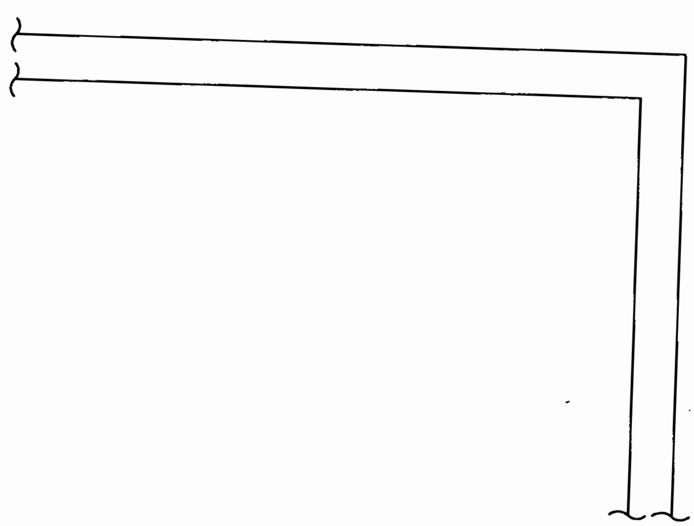

M36
Wd=5u
lng=0.4u
M33
Wd=2.5u
lng=0.4u
S
S
M34
Wd=2.5u
lng=0.4u
S
S
M35
Wd=5u
lng=0.4u
CLR
CLR

FIG.126G

FIG.126H



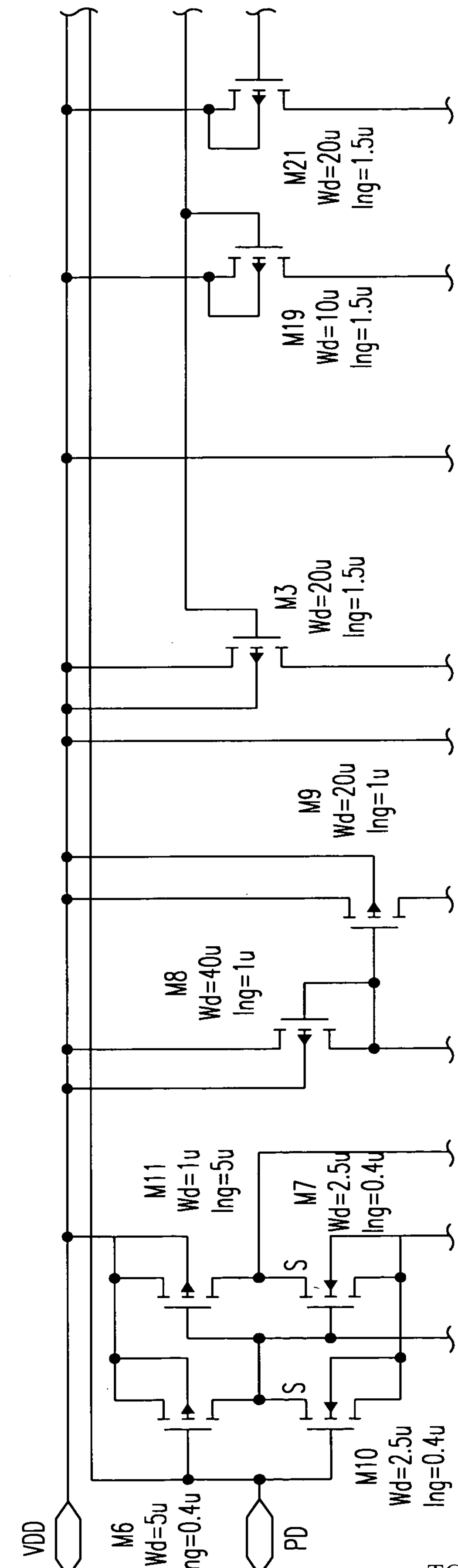

M21
Wd=20u
lng=1.5u
M19
Wd=10u
lng=1.5u
M3
Wd=20u
lng=1.5u
M9
Wd=20u
lng=1u
M8
Wd=40u
lng=1u
M11
Wd=1u
lng=5u
M7
Wd=2.5u
lng=0.4u
S
S
M10
Wd=2.5u
lng=0.4u
VDD
M6
Wd=5u
lng=0.4u
PD

FIG.127A

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

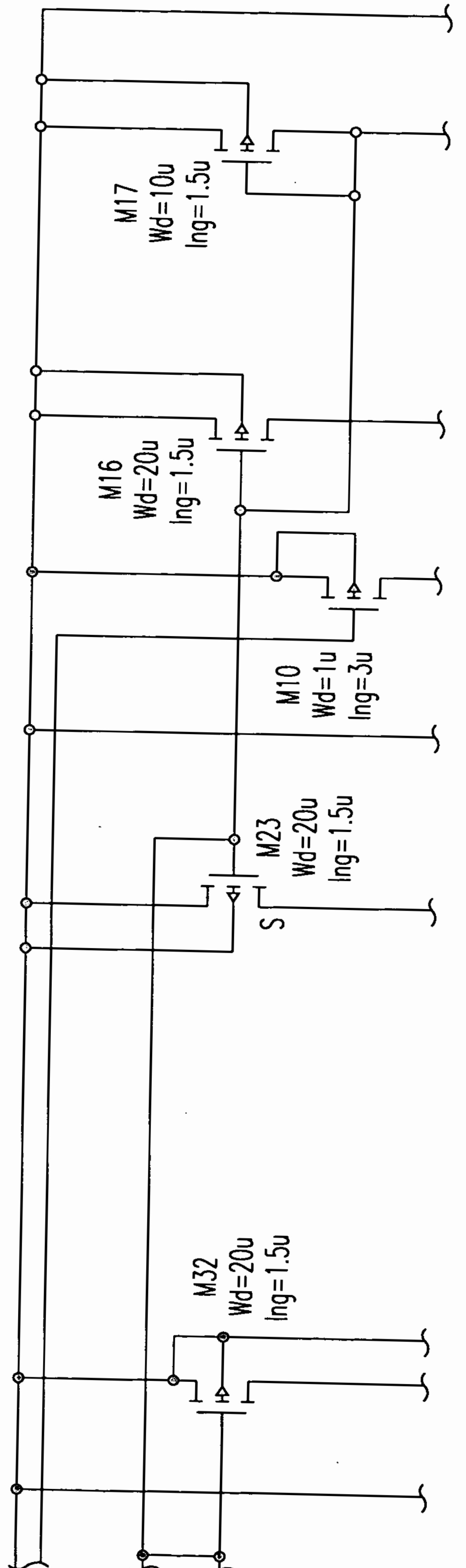


FIG. 127B

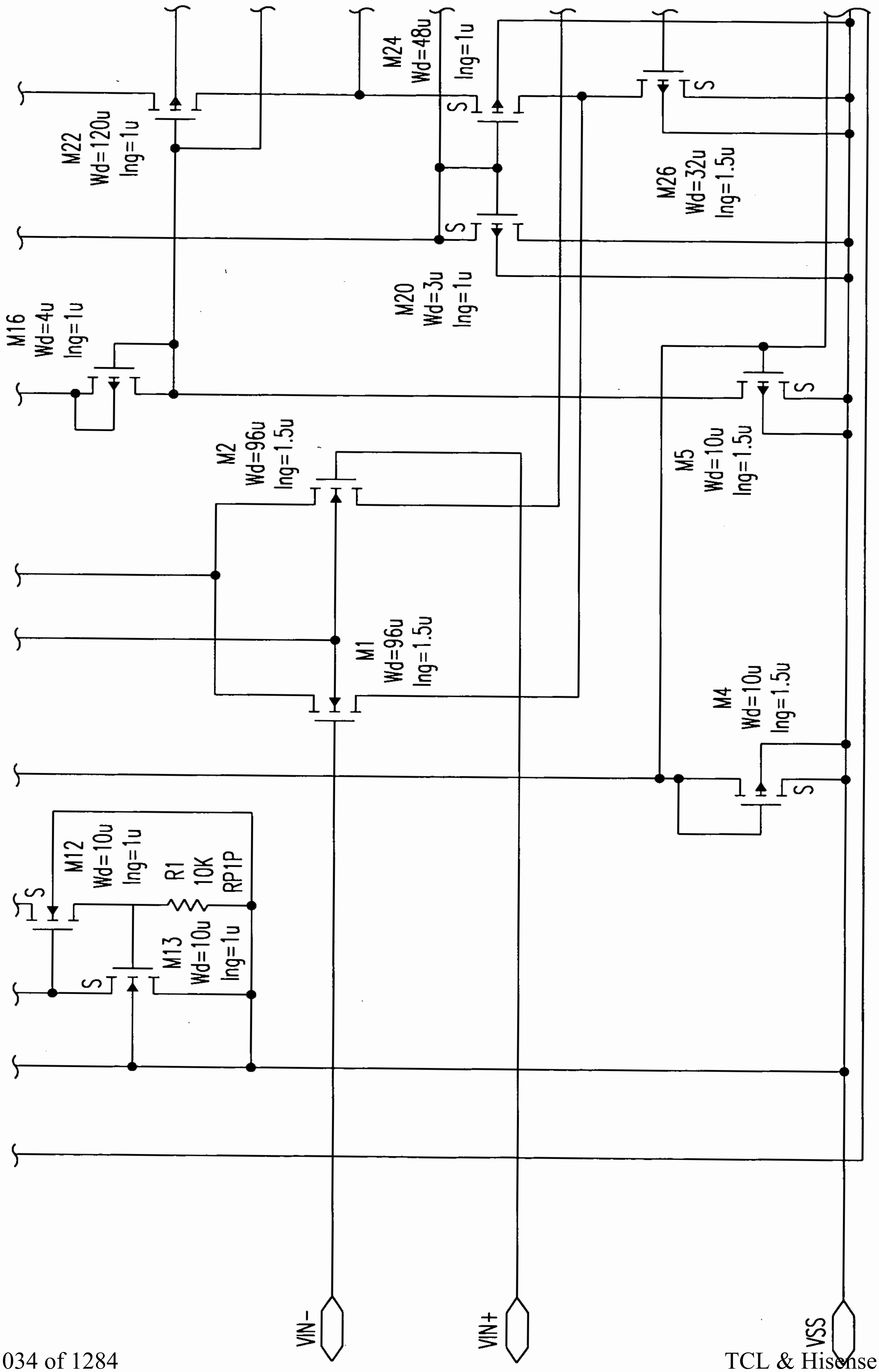

M22
Wd=120u
lng=1u
M16
Wd=4u
lng=1u
M24
Wd=48u
lng=1u
M20
Wd=3u
lng=1u
M26
Wd=32u
lng=1.5u
M2
Wd=96u
lng=1.5u
M1
Wd=96u
lng=1.5u
M5
Wd=10u
lng=1.5u
M4
Wd=10u
lng=1.5u
M12
Wd=10u
lng=1u
R1
10K
RP1P
M13
Wd=10u
lng=1u
S
VIN-
VIN+
VSS

FIG.127C

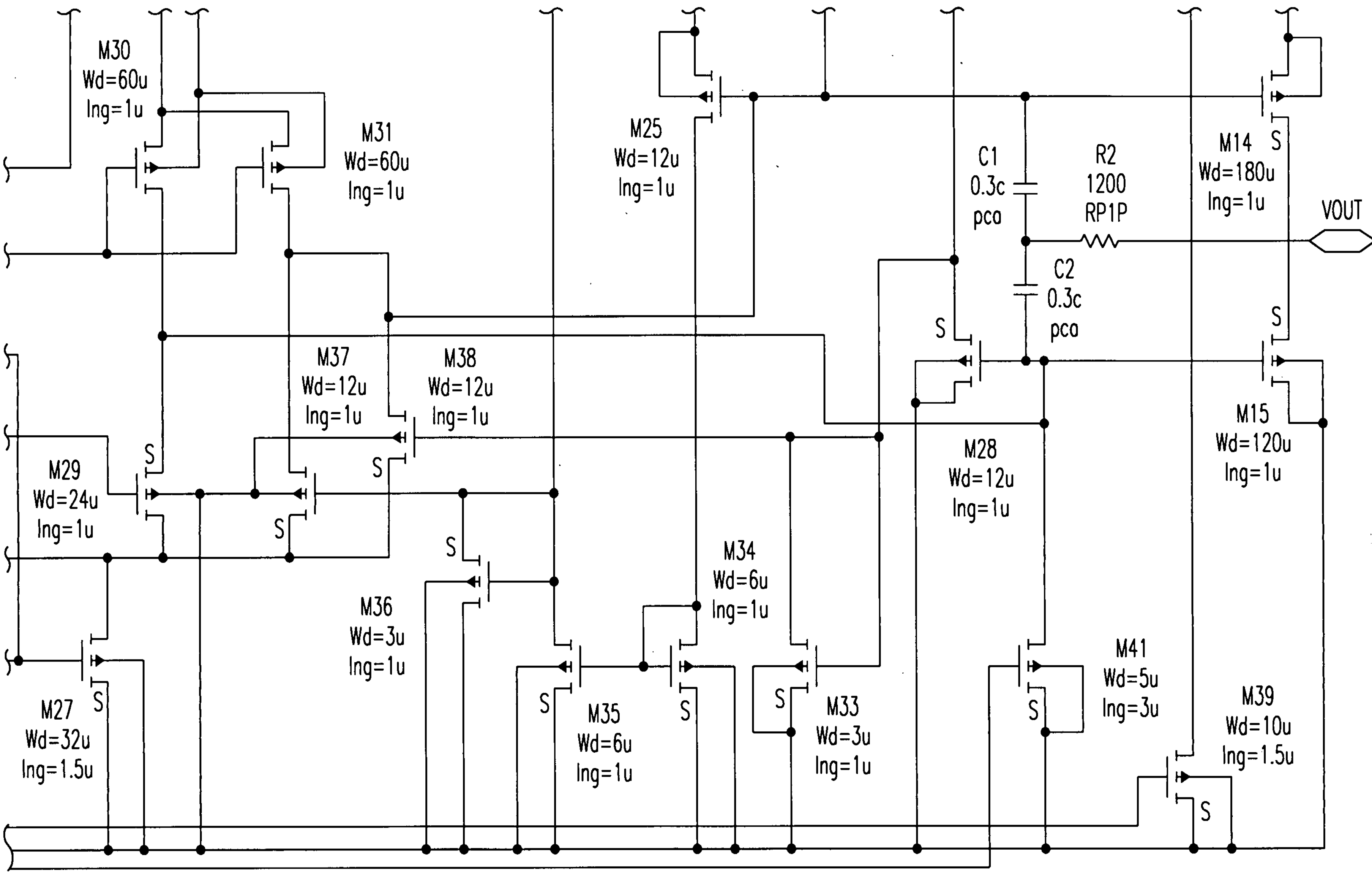

M30
Wd=60u
lng=1u
M31
Wd=60u
lng=1u
M25
Wd=12u
lng=1u
C1
0.3c
pca
R2
1200
RP1P
M14
Wd=180u
lng=1u
VOUT
C2
0.3c
pca
M37
Wd=12u
lng=1u
M38
Wd=12u
lng=1u
M28
Wd=12u
lng=1u
M15
Wd=120u
lng=1u
M29
Wd=24u
lng=1u
M36
Wd=3u
lng=1u
M34
Wd=6u
lng=1u
M35
Wd=6u
lng=1u
M33
Wd=3u
lng=1u
M41
Wd=5u
lng=3u
M39
Wd=10u
lng=1.5u
M27
Wd=32u
lng=1.5u
S

FIG.127D

Replacement Sheet
Sheet 303 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.063003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

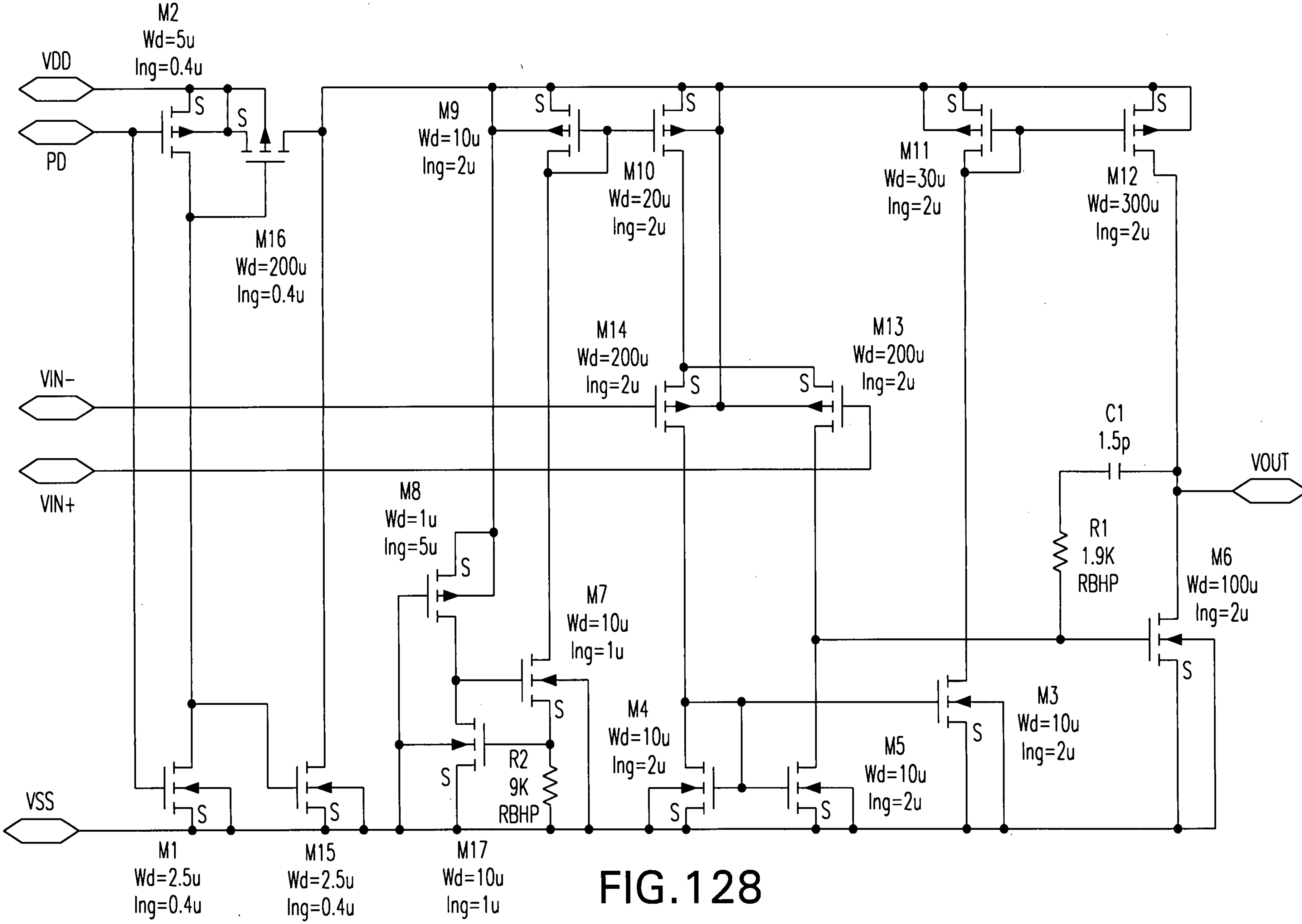


FIG.128

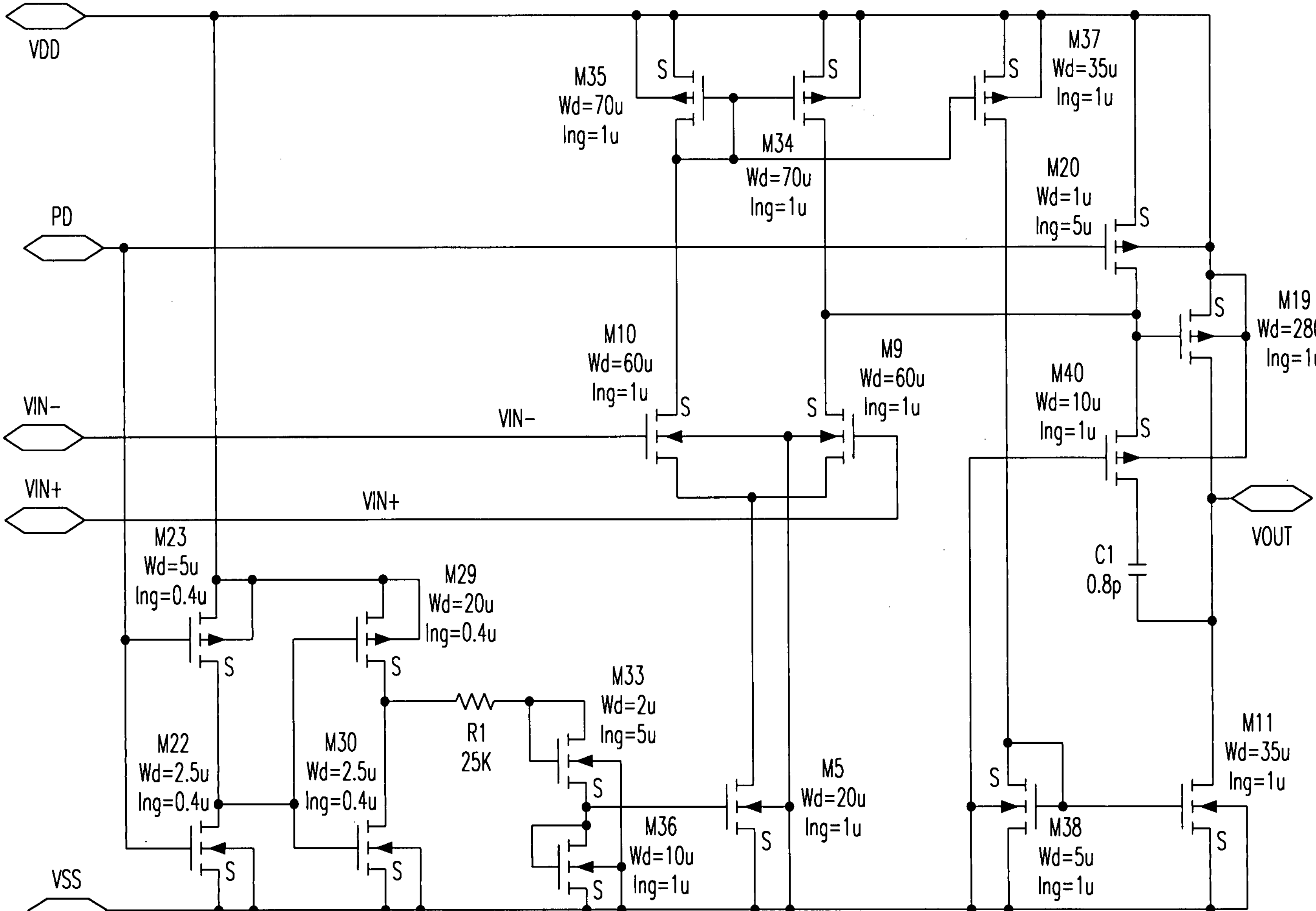


FIG.129

Replacement Sheet
Sheet 304 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

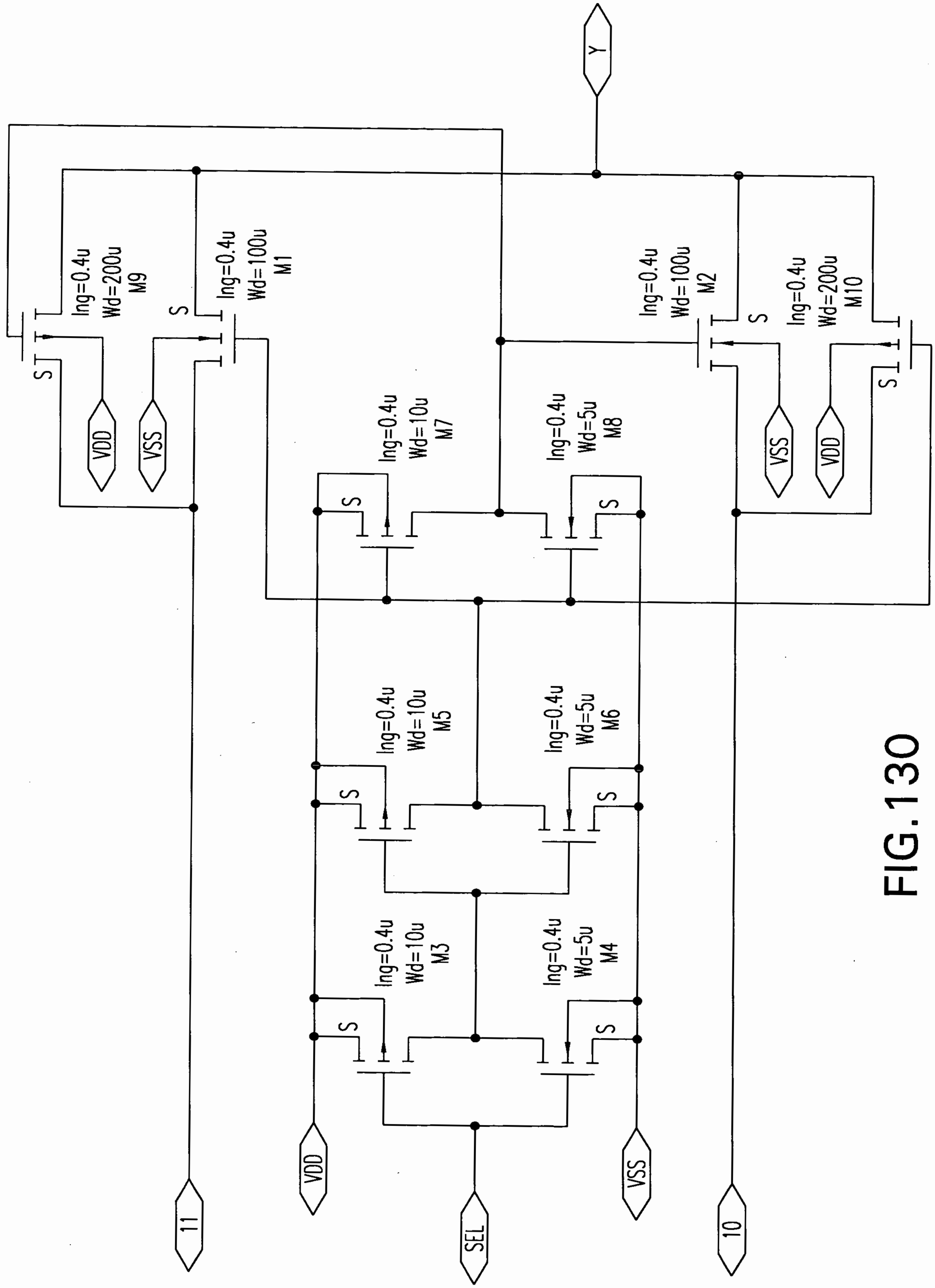

Y
lng=0.4u
Wd=200u
M9
lng=0.4u
Wd=100u
M1
lng=0.4u
Wd=100u
M2
lng=0.4u
Wd=200u
M10
S
VDD
VSS
lng=0.4u
Wd=10u
M7
lng=0.4u
Wd=5u
M8
lng=0.4u
Wd=10u
M5
lng=0.4u
Wd=5u
M6
lng=0.4u
Wd=10u
M3
lng=0.4u
Wd=5u
M4
11
SEL
10

FIG.130

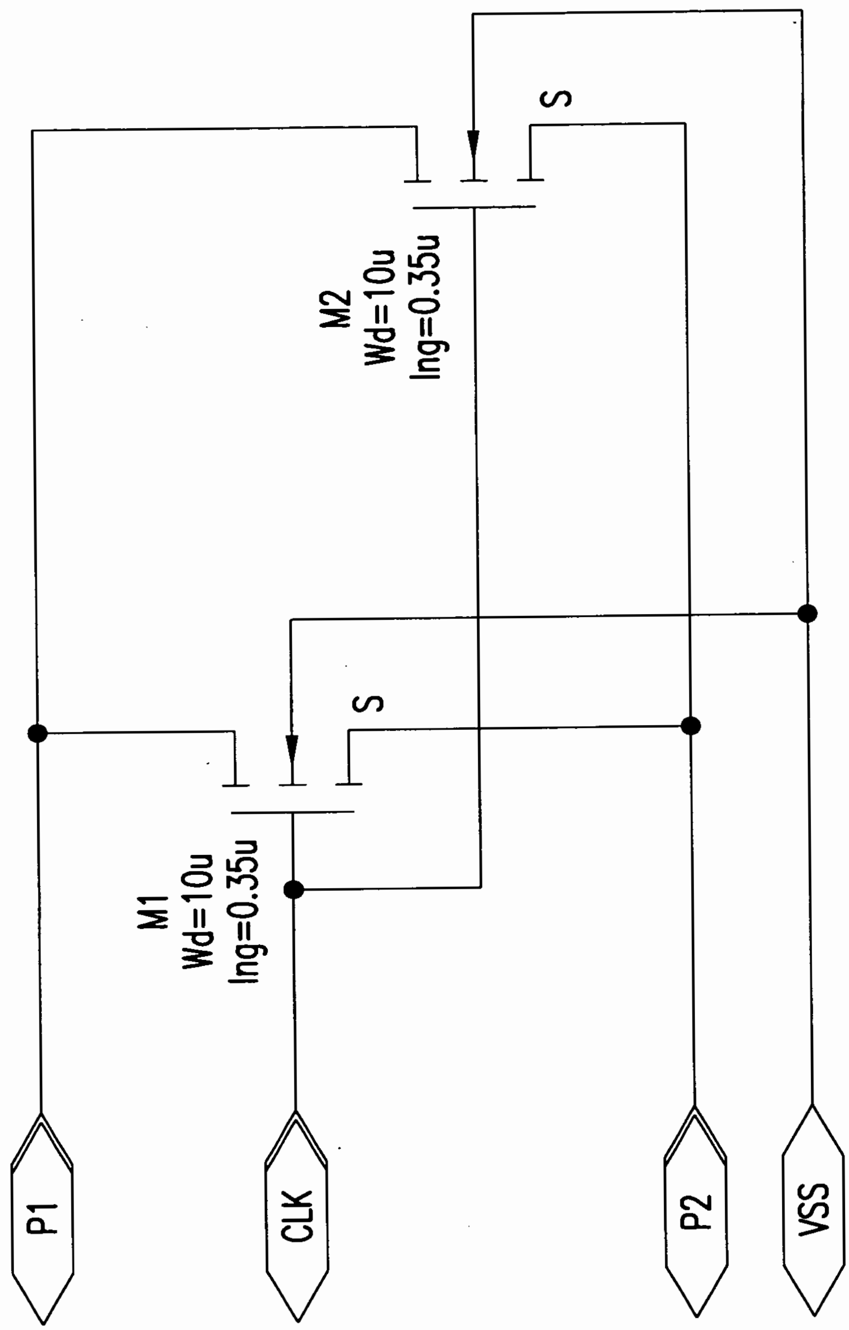


FIG.131

Replacement Sheet
Sheet 307 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

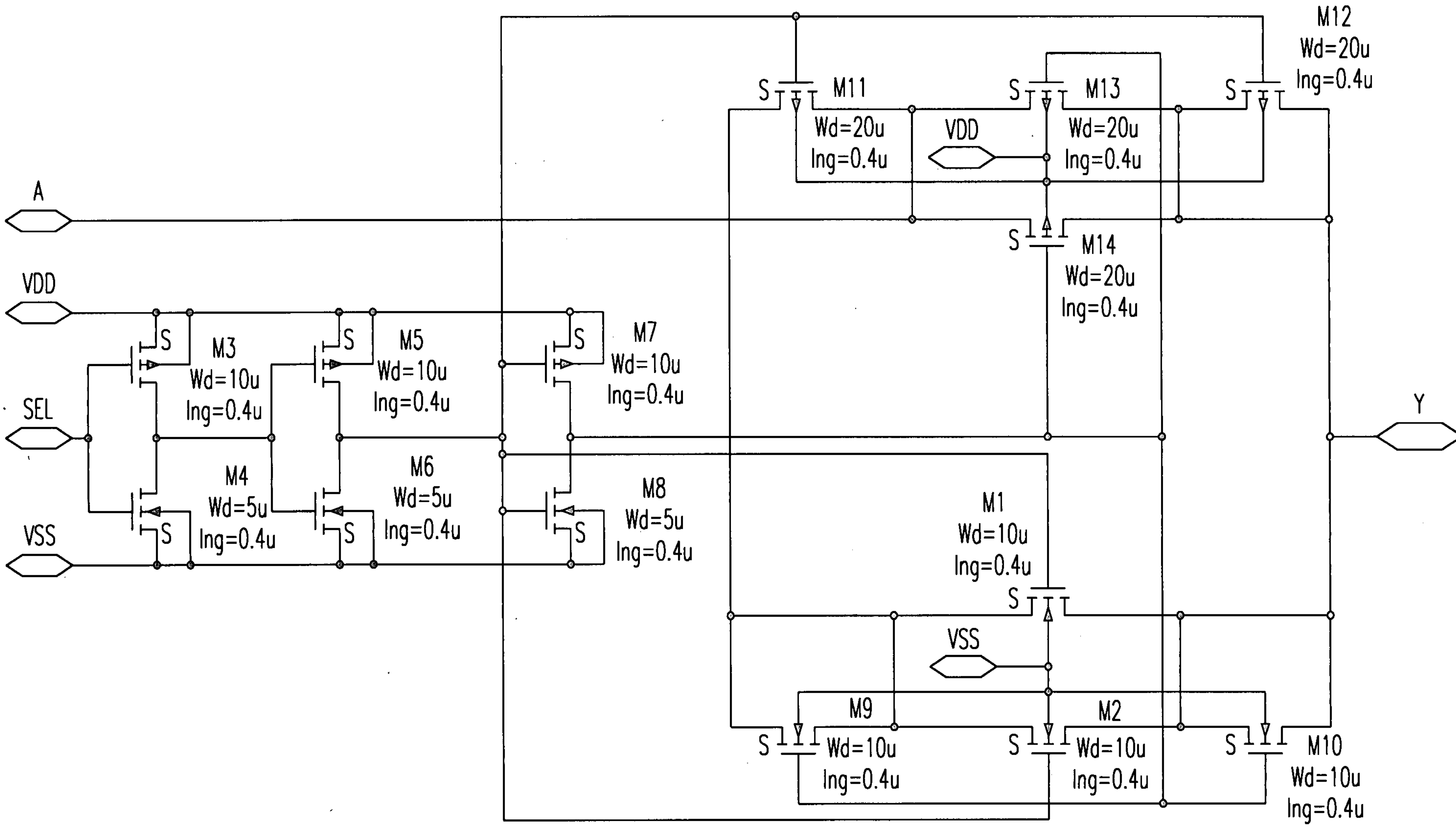


FIG.132

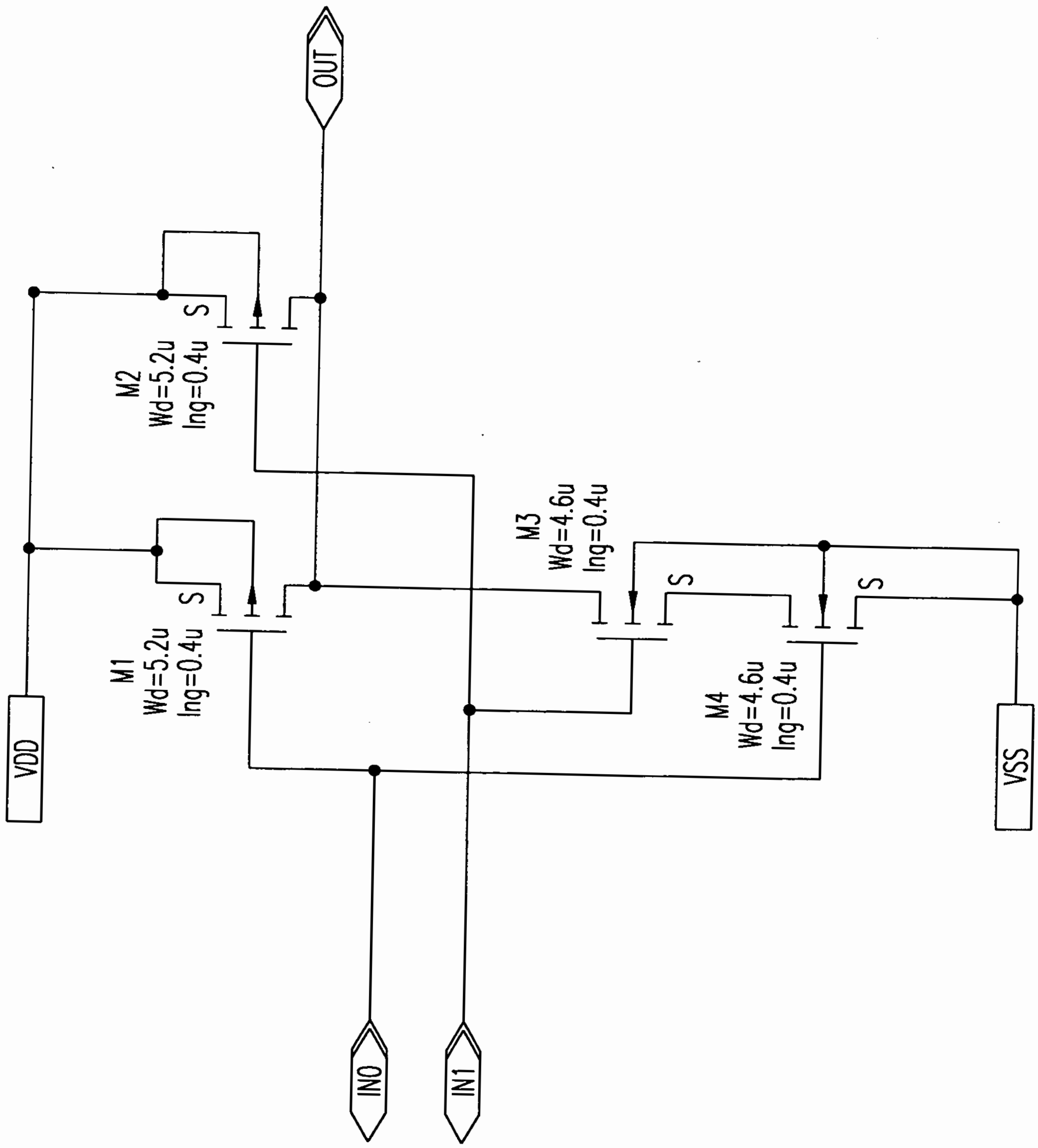

OUT
M2
Wd=5.2u
lng=0.4u
S
M1
Wd=5.2u
lng=0.4u
S
M3
Wd=4.6u
lng=0.4u
S
M4
Wd=4.6u
lng=0.4u
S
VDD
VSS
IN0
IN1

FIG.133

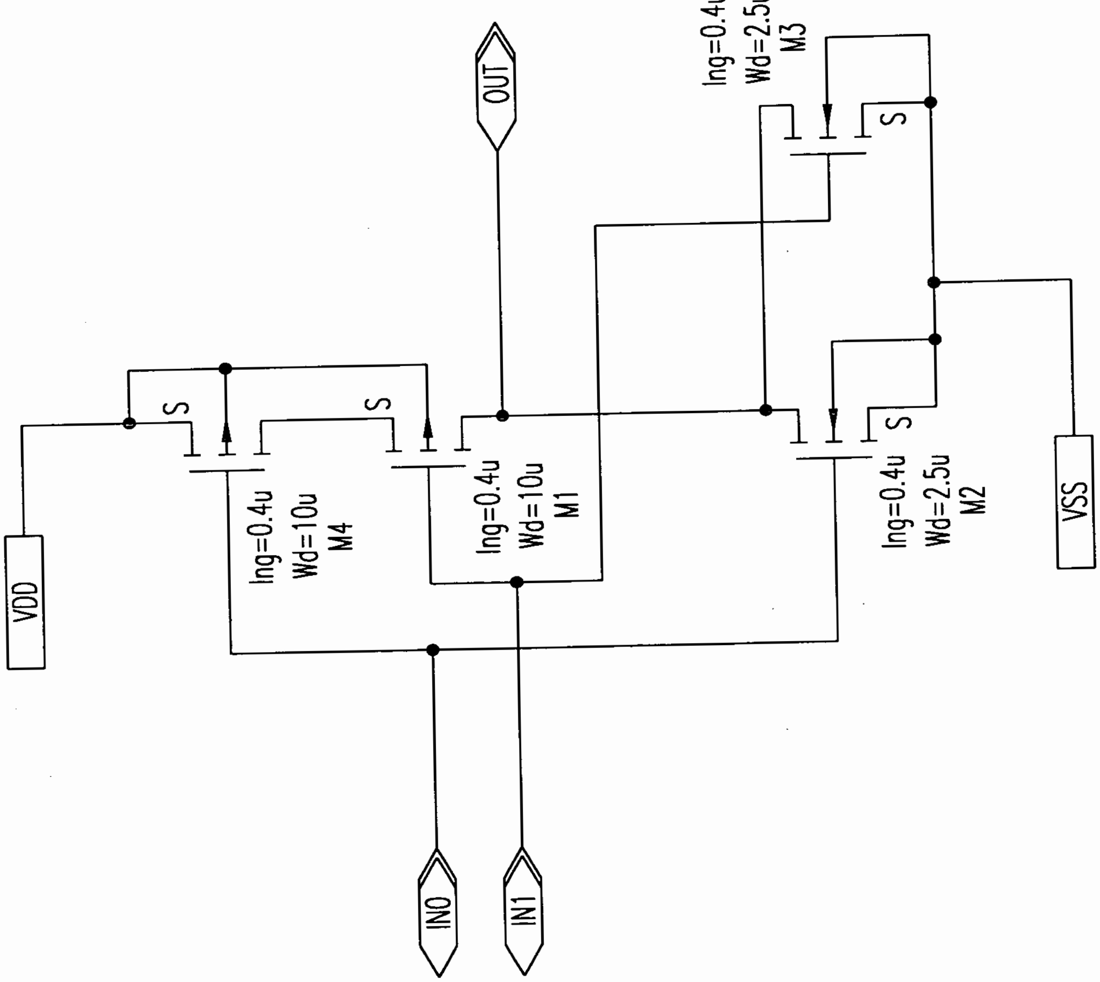

OUT
lng=0.4u
Wd=2.5u
M3
S
S
S
lng=0.4u
Wd=10u
M4
lng=0.4u
Wd=10u
M1
S
lng=0.4u
Wd=2.5u
M2
VDD
VSS
IN0
IN1

FIG.134

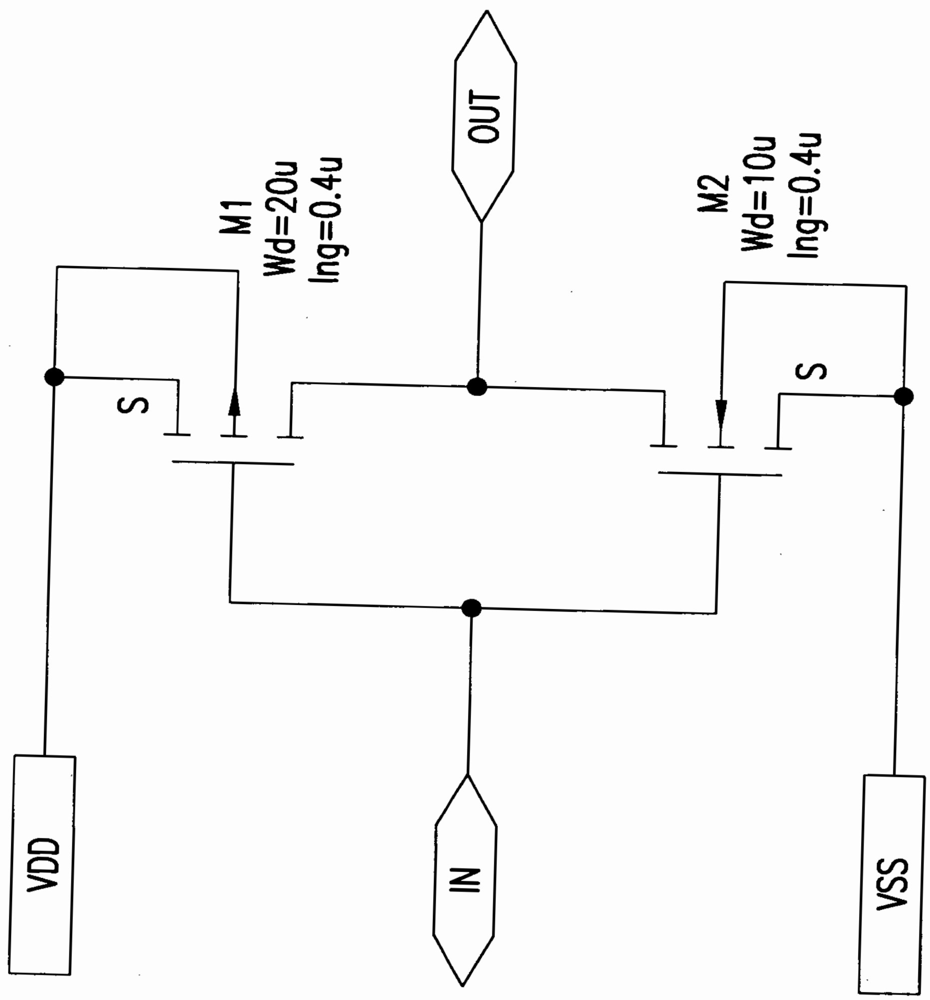


FIG.135

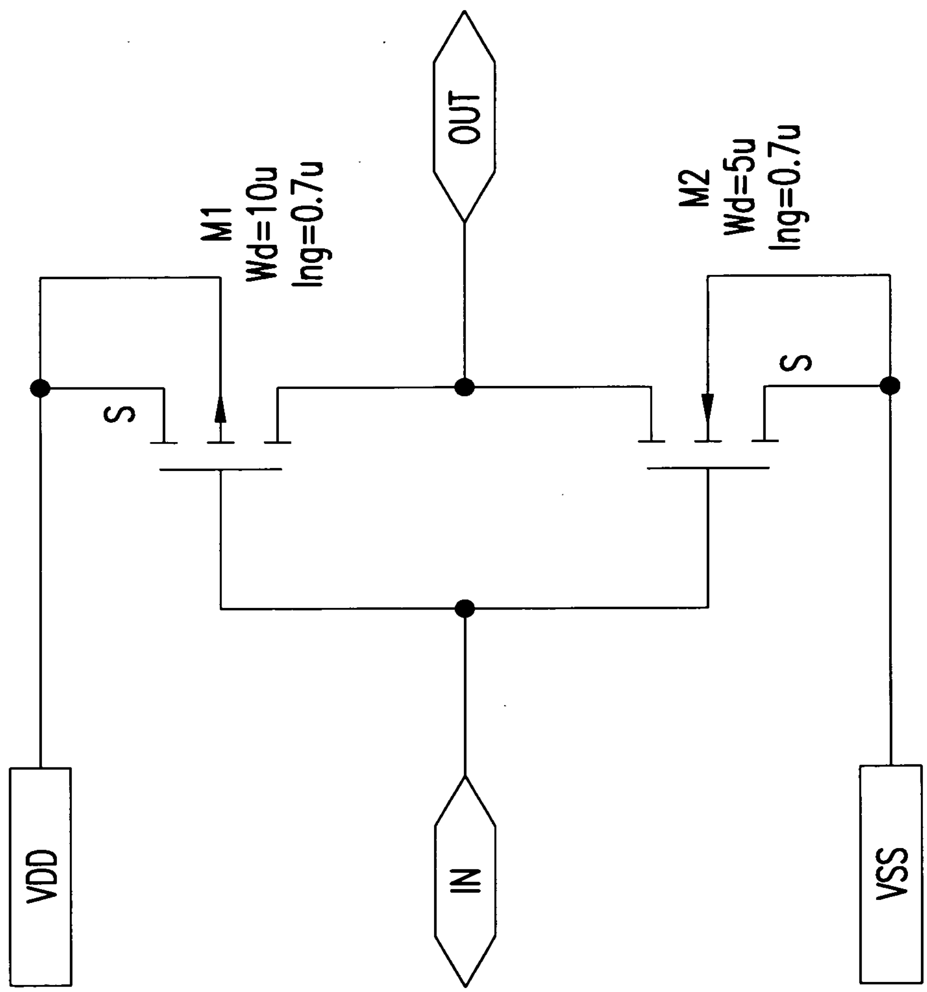


FIG.136

Replacement Sheet
Sheet 312 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

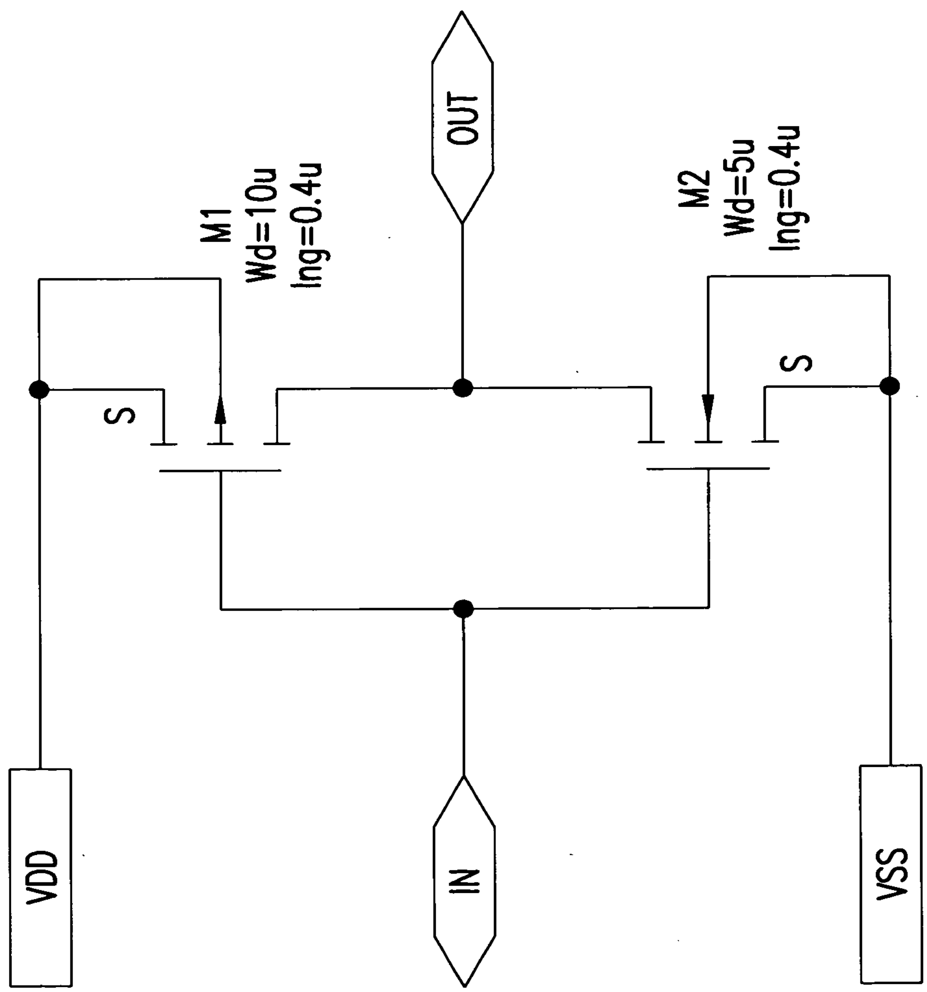


FIG.137

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

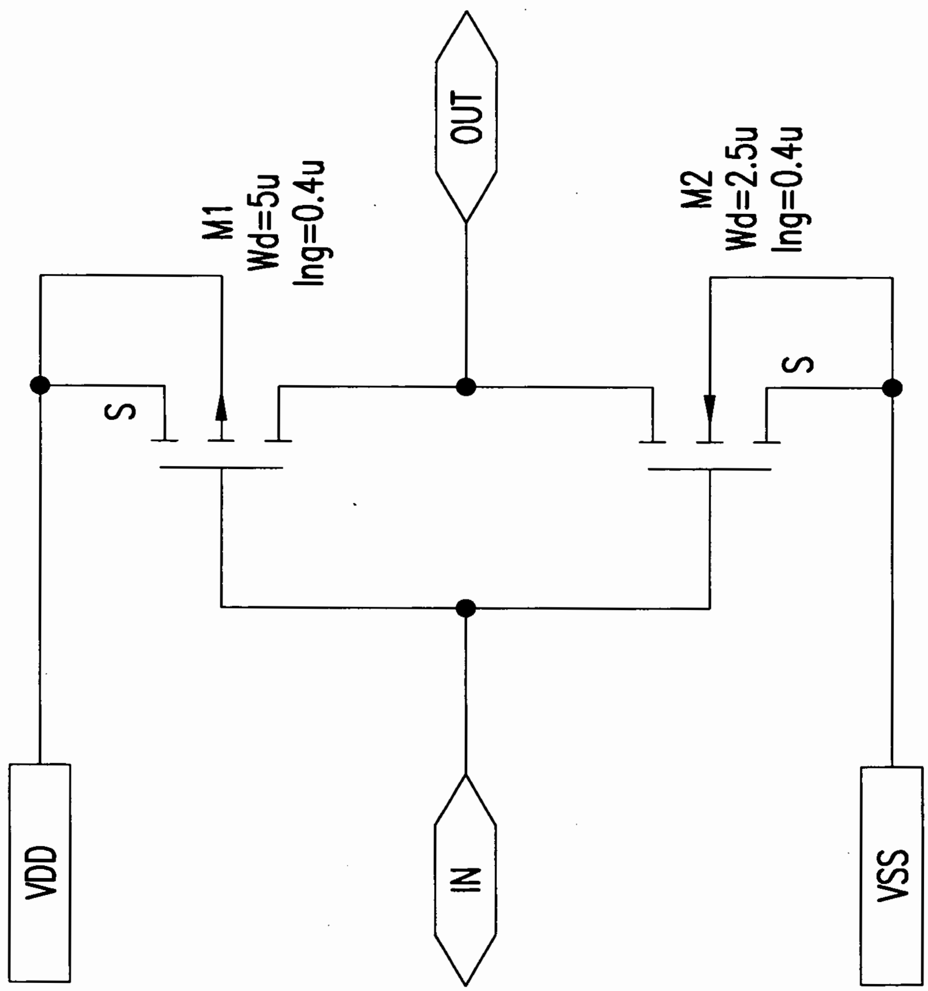


FIG.138

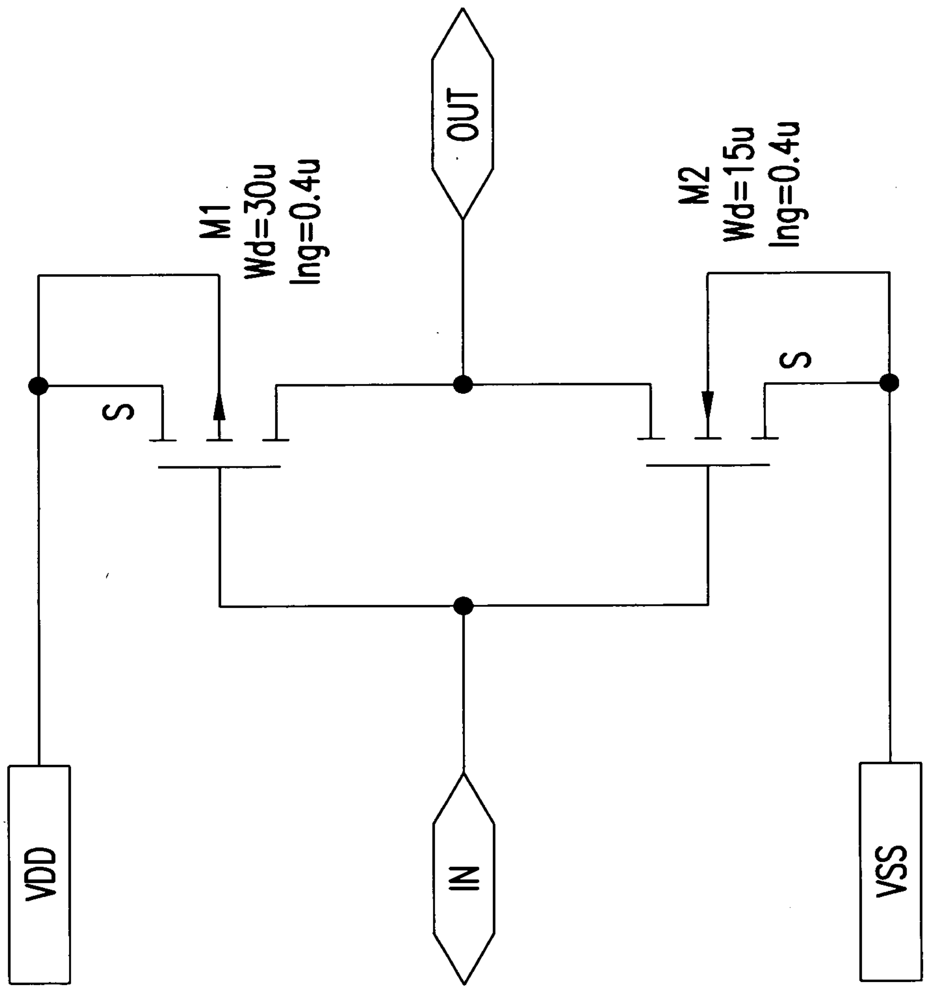


FIG.139

Replacement Sheet
Sheet 315 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

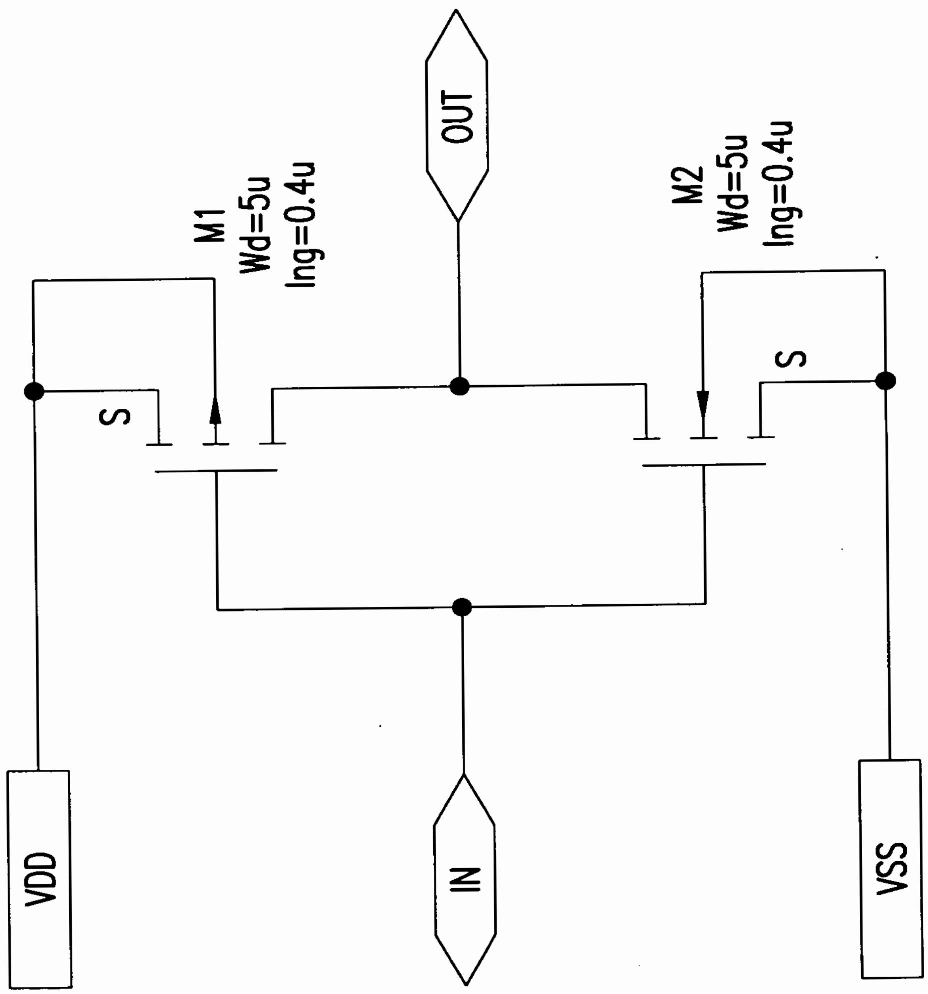


FIG.140

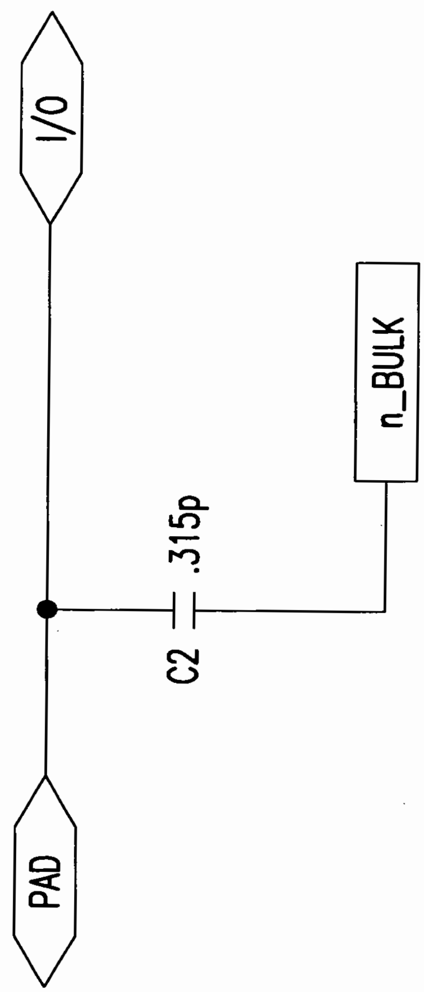


FIG. 141

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

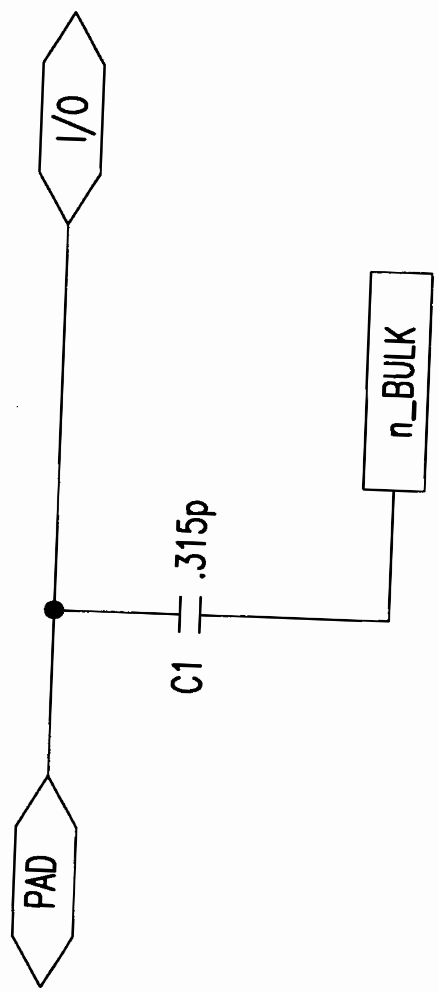


FIG.142

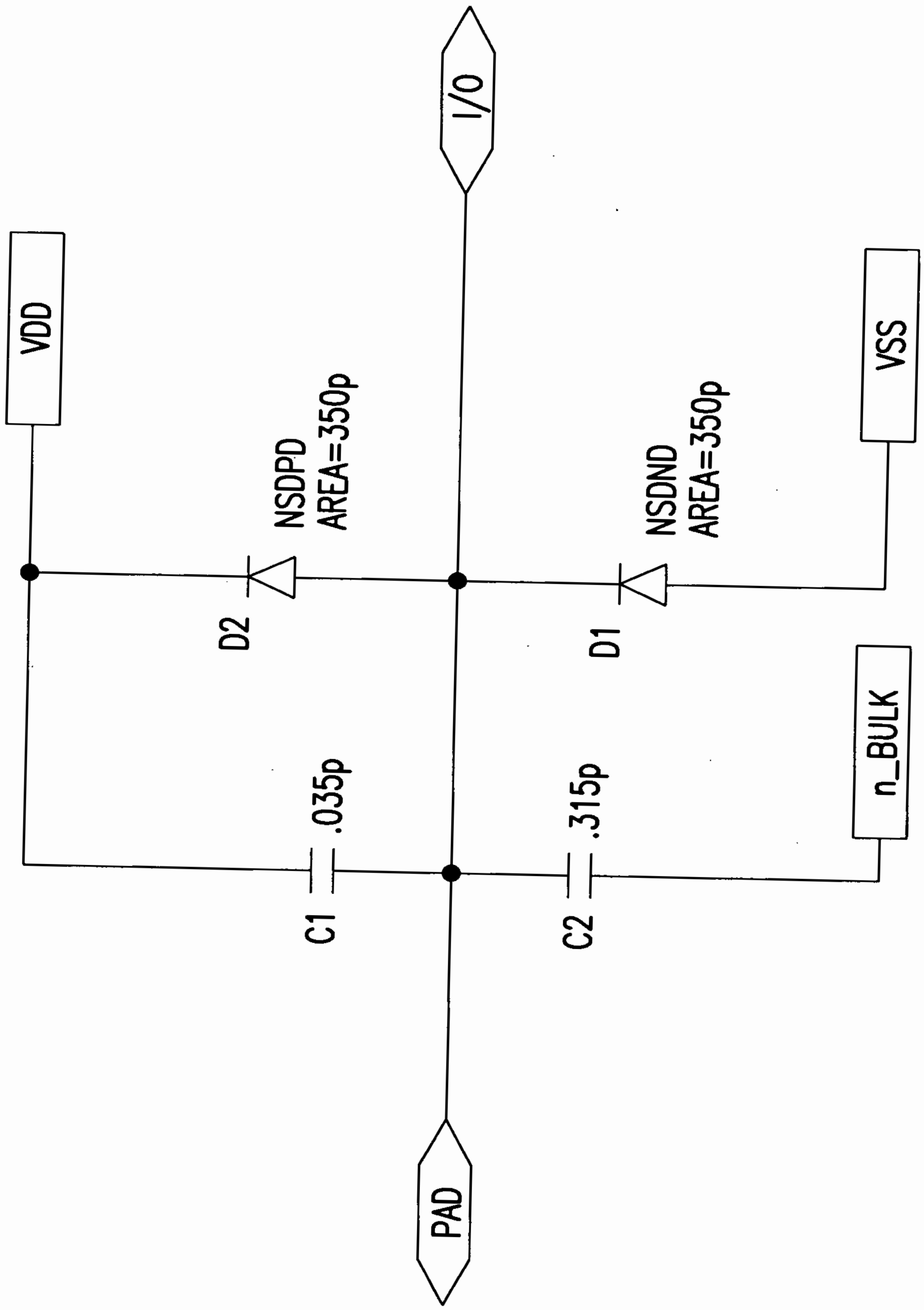

VDD
I/O
VSS
D2
NSDPD
AREA=350p
D1
NSDND
AREA=350p
n_BULK
C1
.035p
C2
.315p
PAD

FIG.143

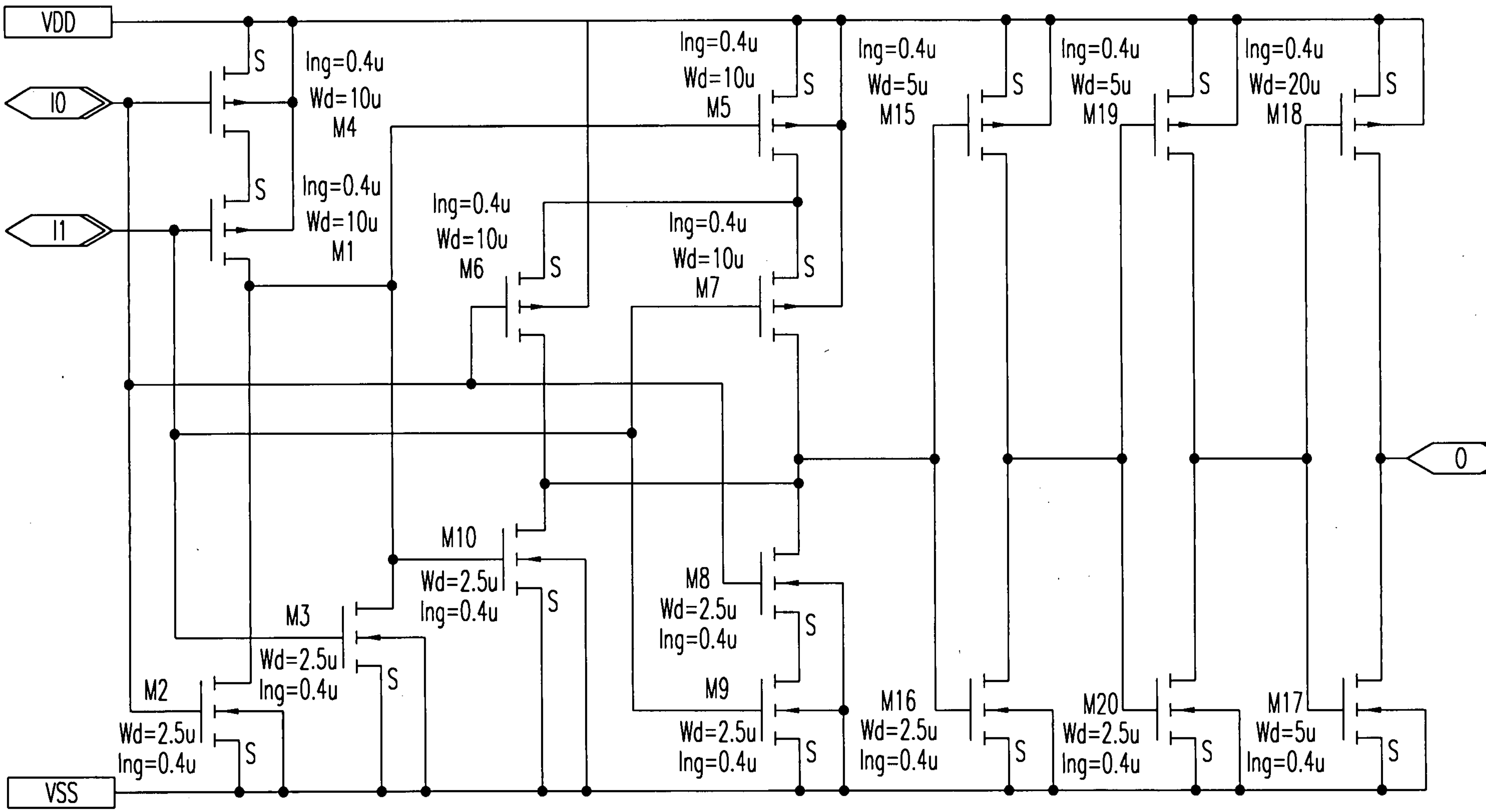


FIG.144

Replacement Sheet
Sheet 319 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

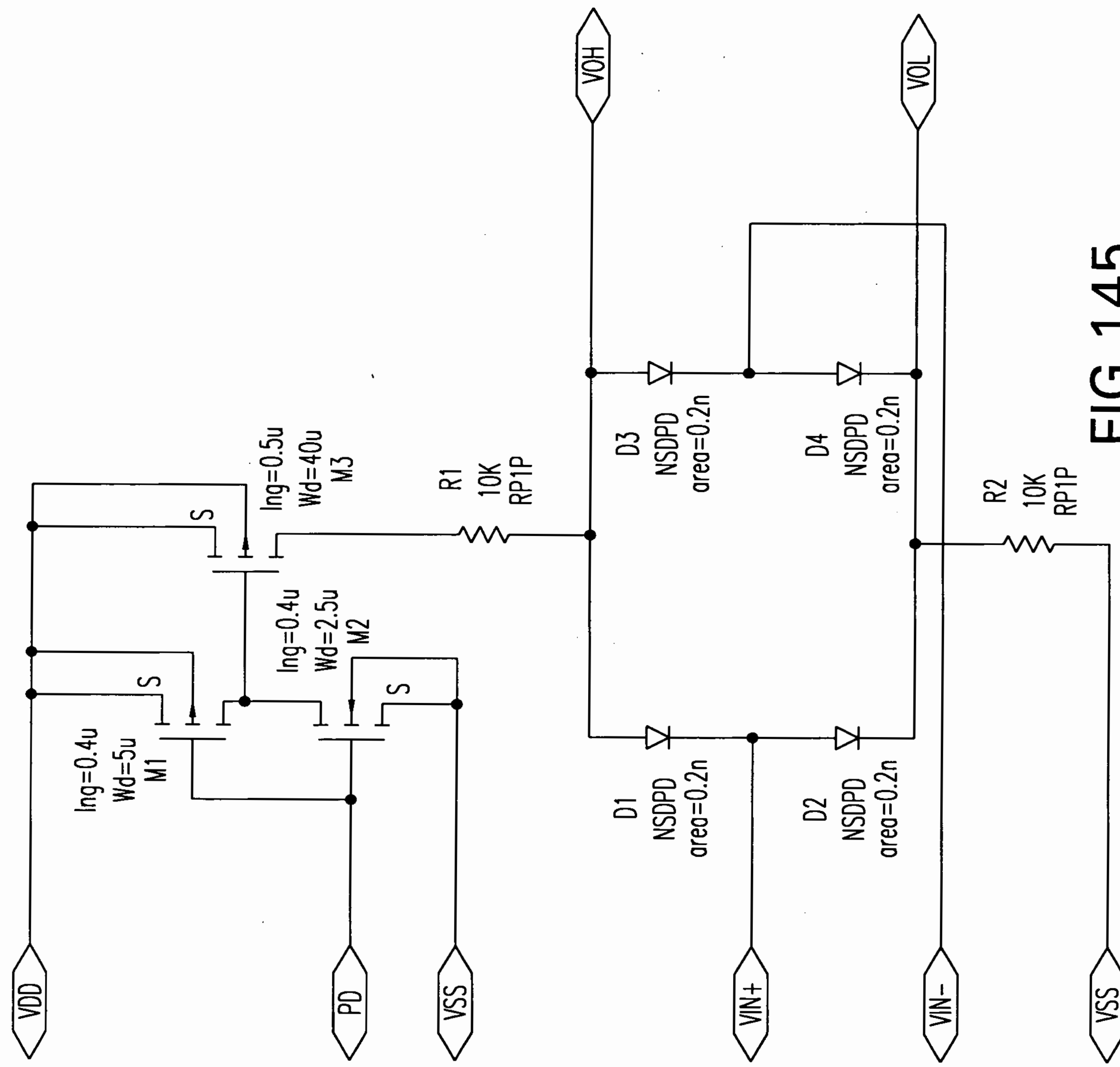

VOH
VOL
lng=0.5u
Wd=40u
M3
S
R1
10K
RP1P
D3
NSDPD
area=0.2n
D4
NSDPD
area=0.2n
lng=0.4u
Wd=2.5u
M2
S
S
lng=0.4u
Wd=5u
M1
D1
NSDPD
area=0.2n
D2
NSDPD
area=0.2n
R2
10K
RP1P
VDD
PD
VSS
VIN+
VIN-
VSS

FIG.145

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

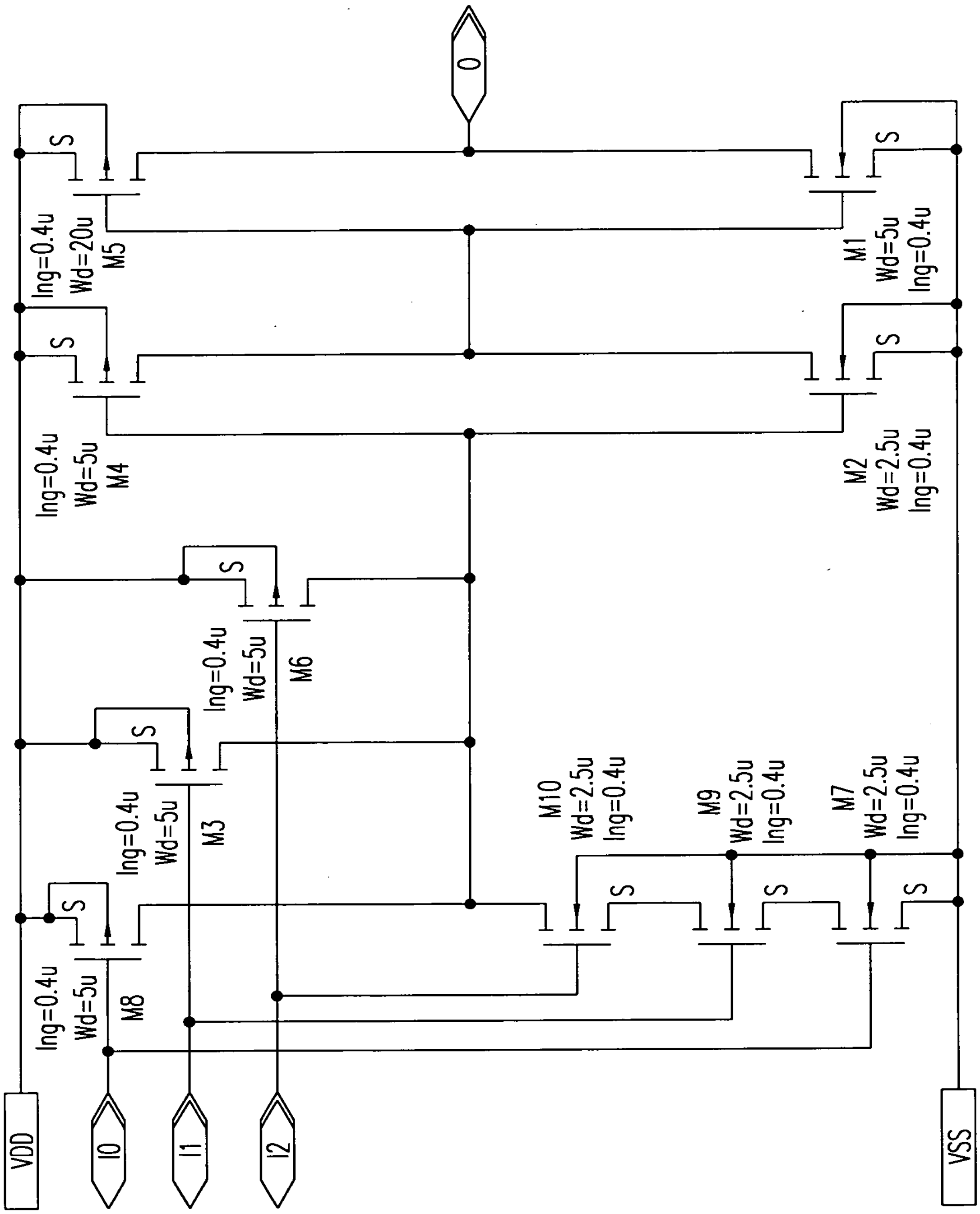


FIG.146

Replacement Sheet
Sheet 322 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

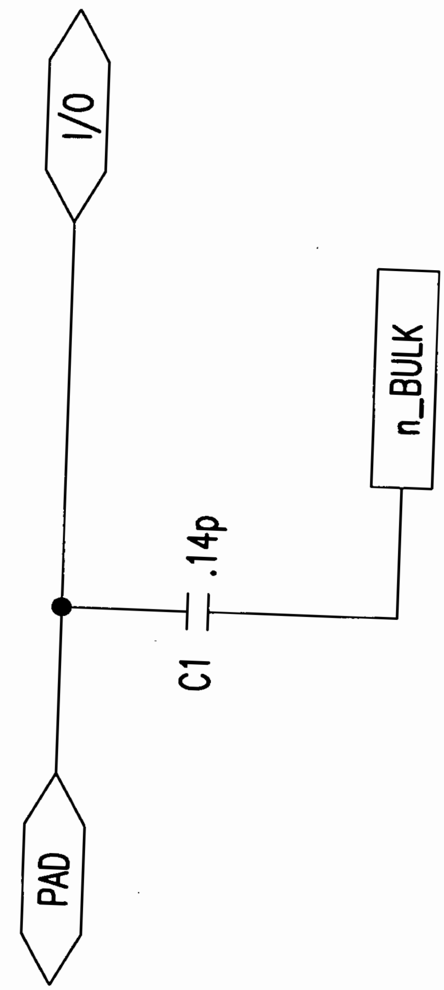


FIG.147

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

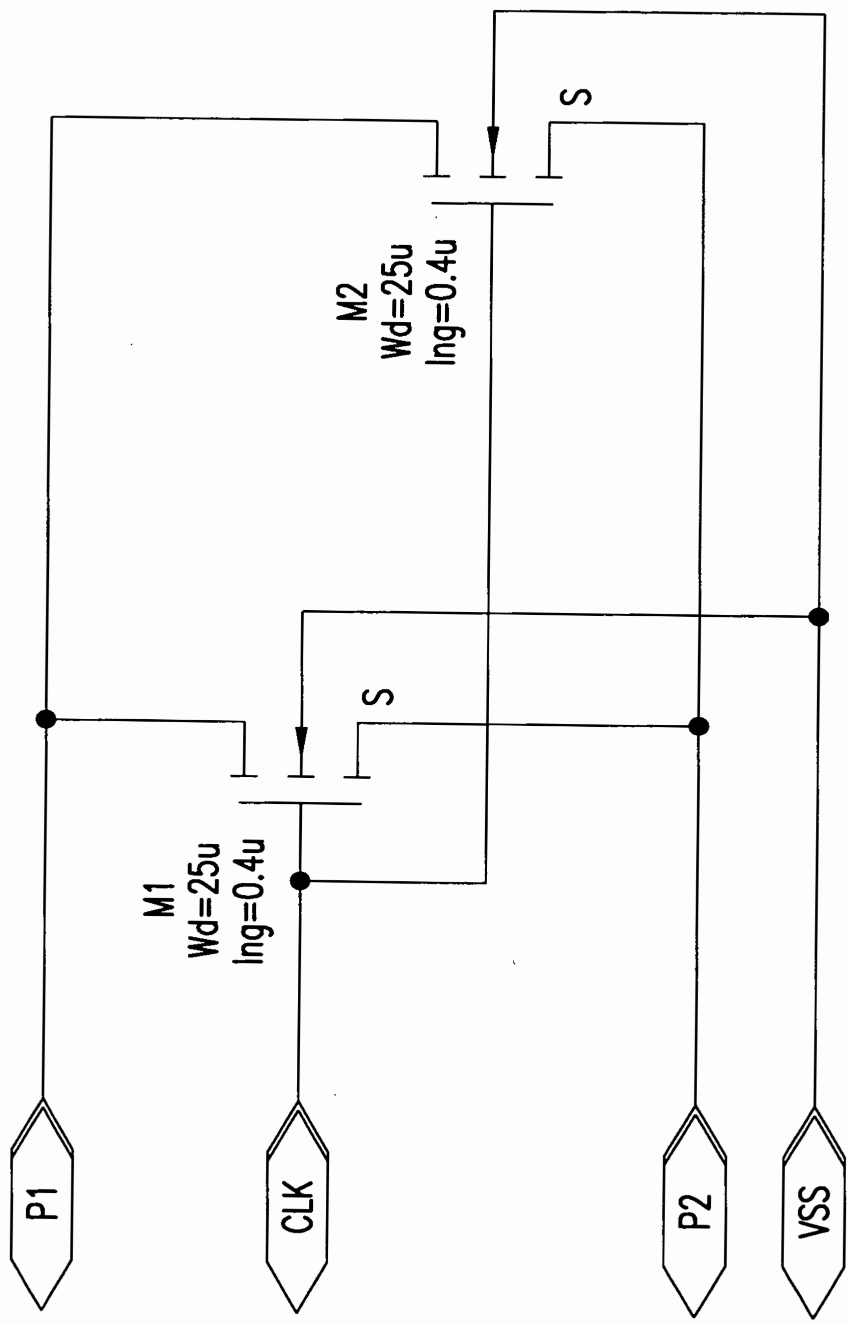


FIG. 148

Replacement Sheet
Sheet 324 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

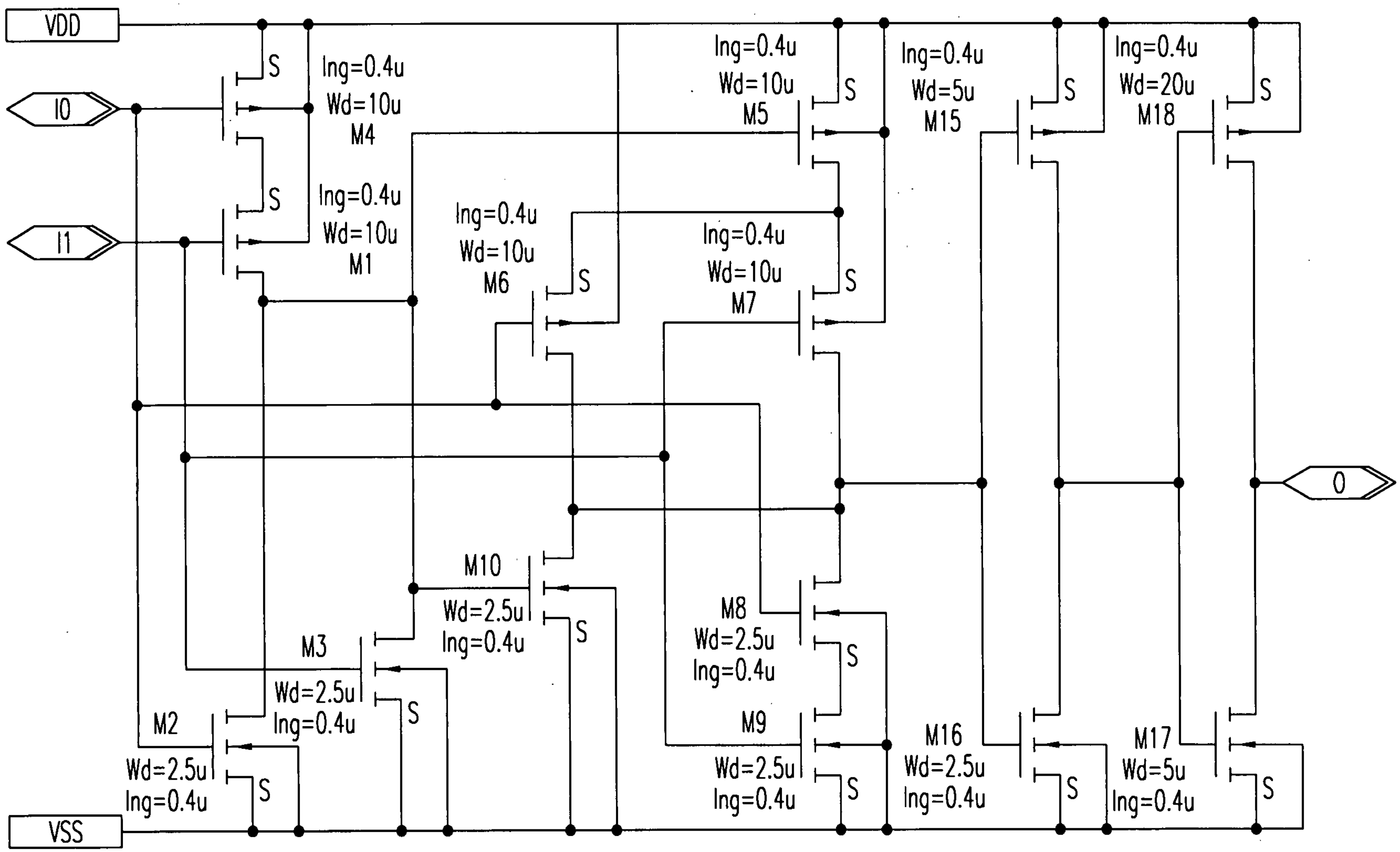


FIG.149

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

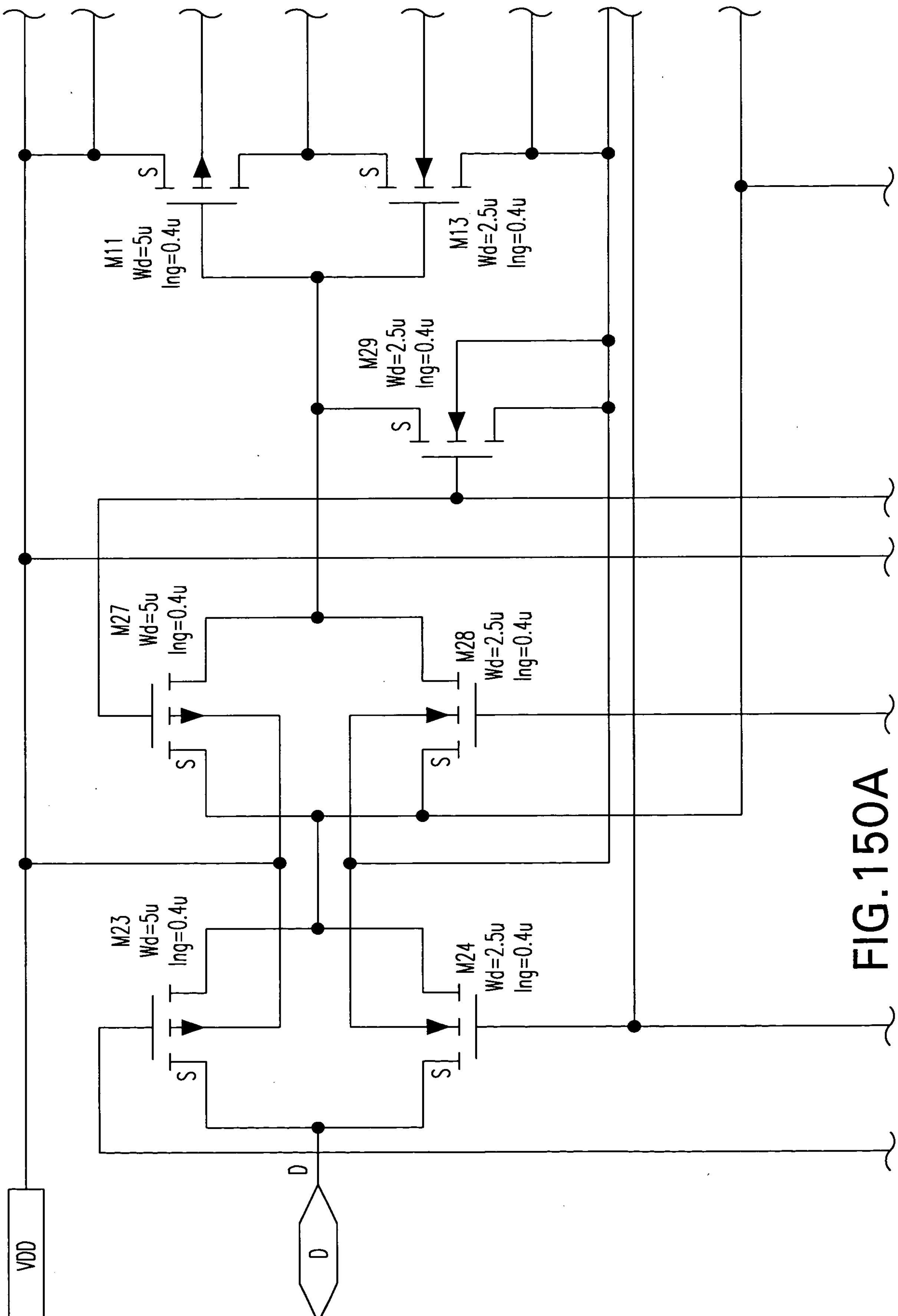


FIG.150A

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

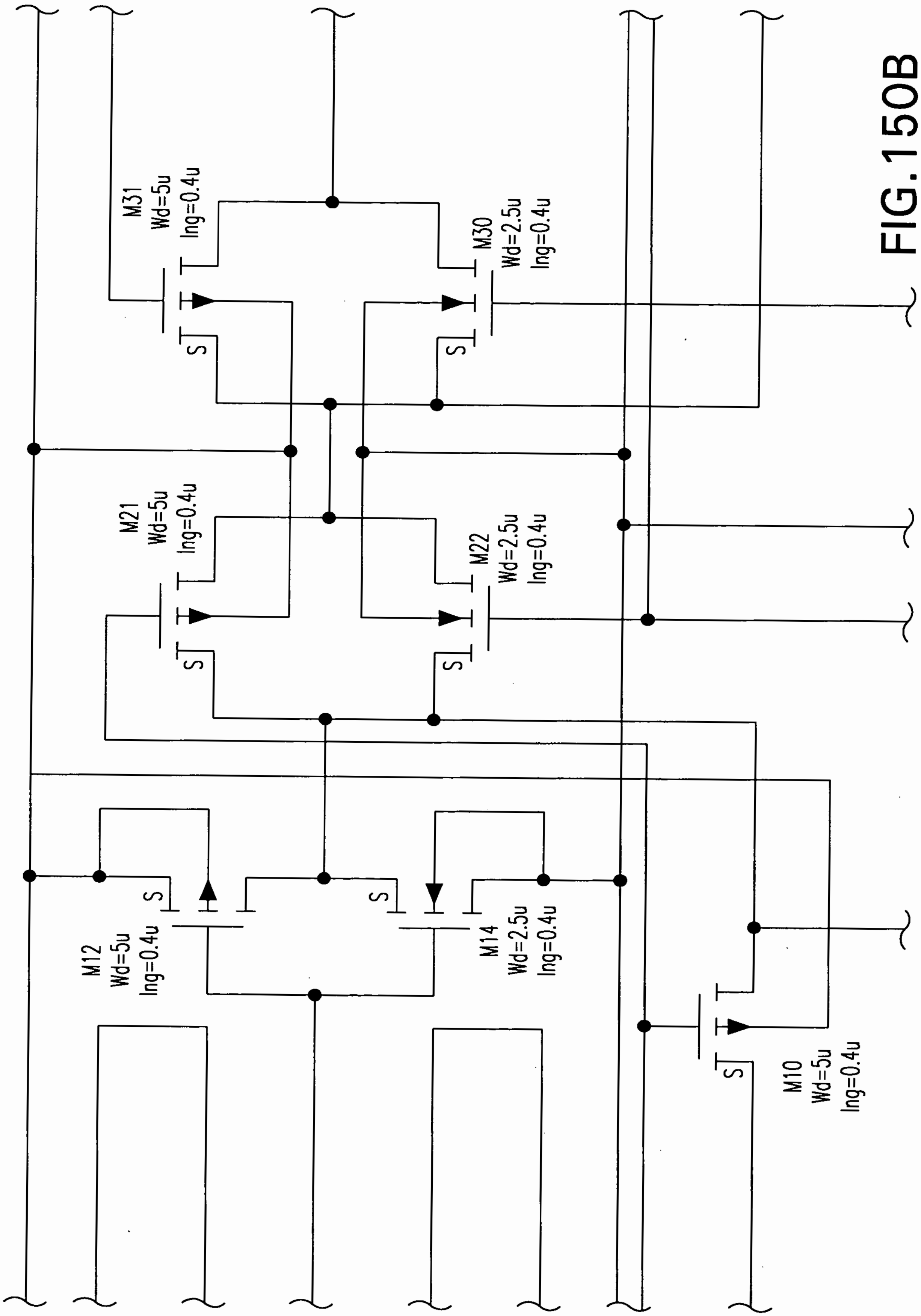


FIG.150B

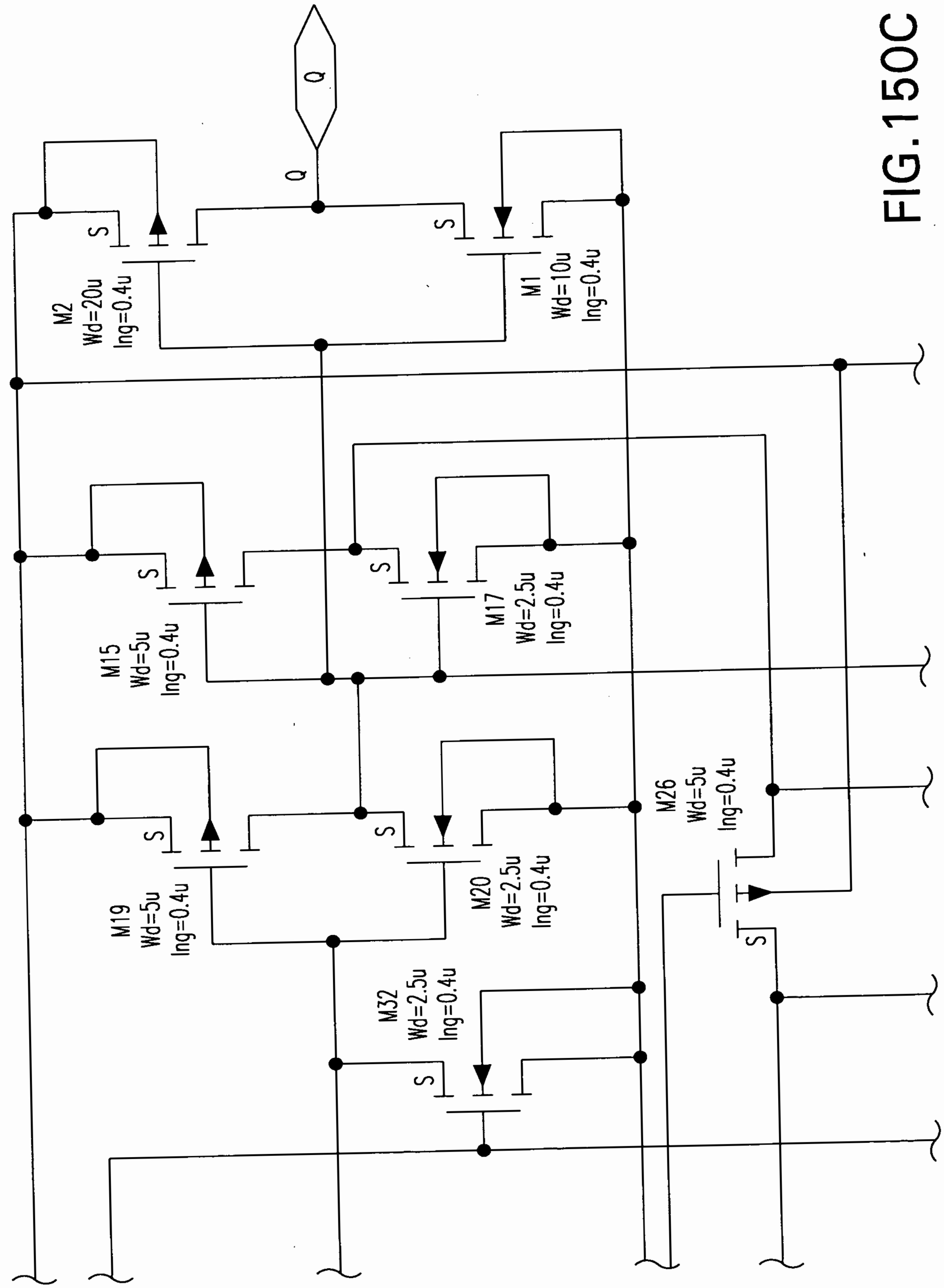

Q
Q
S
M2
Wd=20u
lng=0.4u
S
M1
Wd=10u
lng=0.4u
S
M15
Wd=5u
lng=0.4u
S
M17
Wd=2.5u
lng=0.4u
S
M19
Wd=5u
lng=0.4u
S
M20
Wd=2.5u
lng=0.4u
M26
Wd=5u
lng=0.4u
S
M32
Wd=2.5u
lng=0.4u
S

FIG. 150C

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

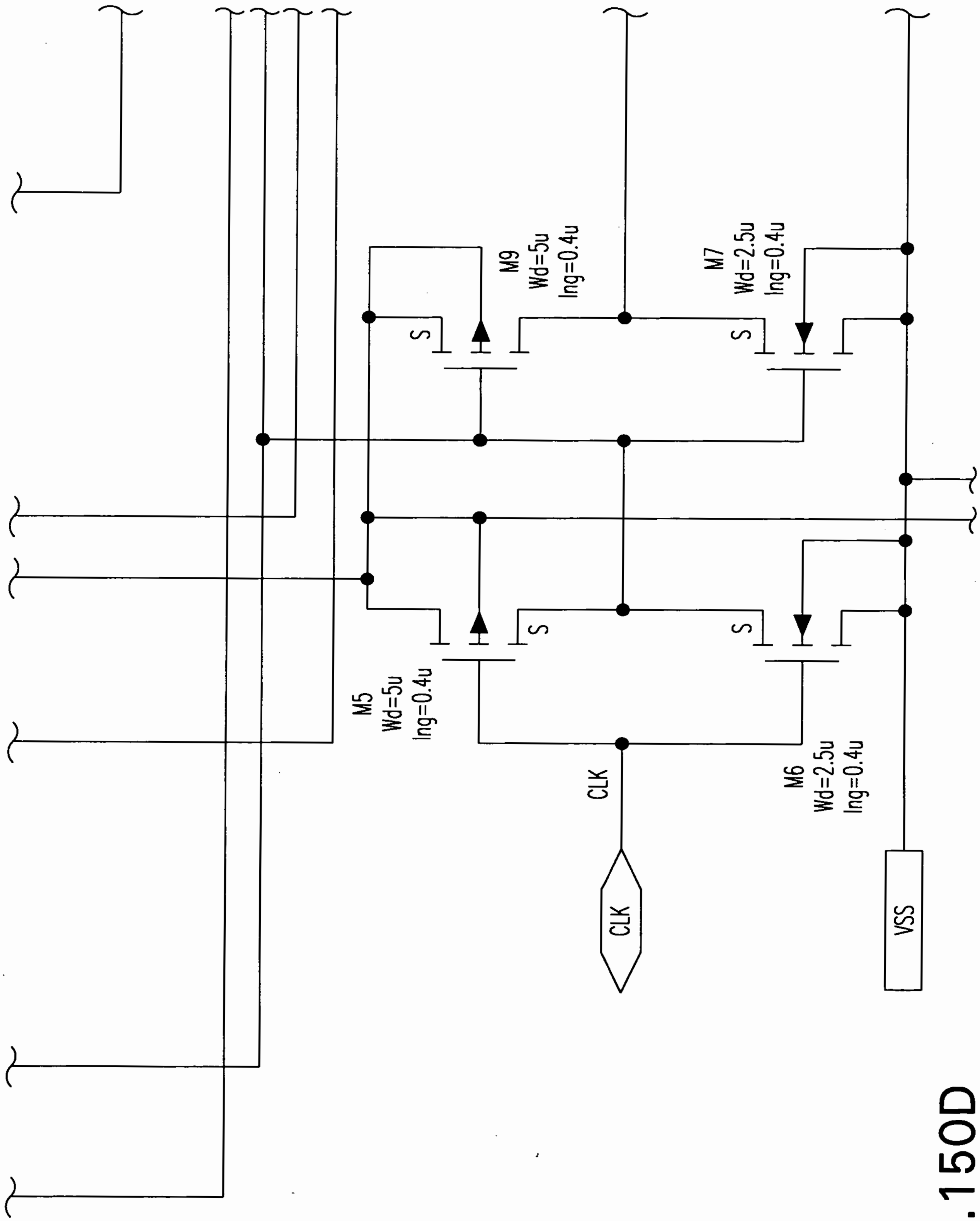


FIG.150D

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

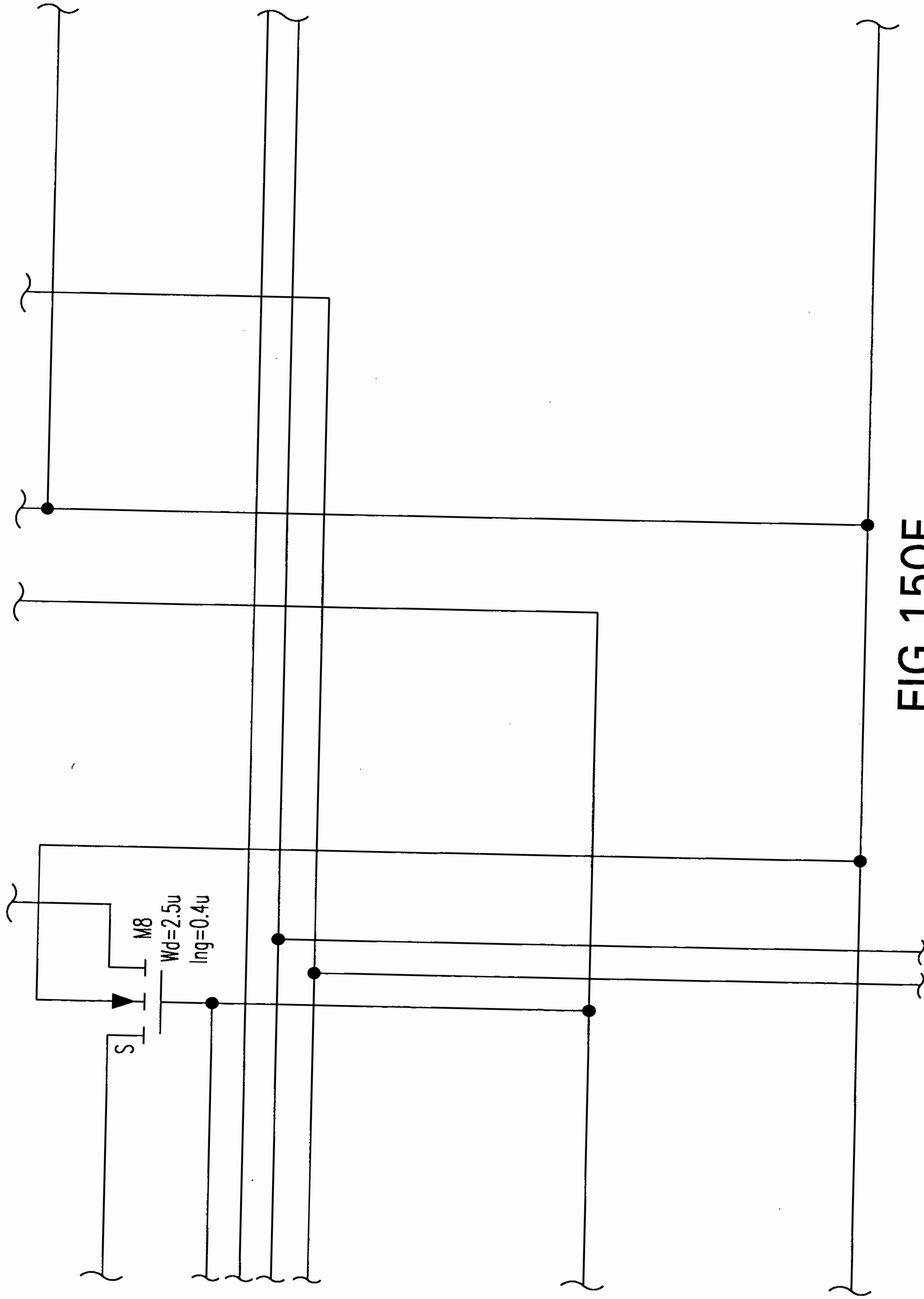


FIG.150E

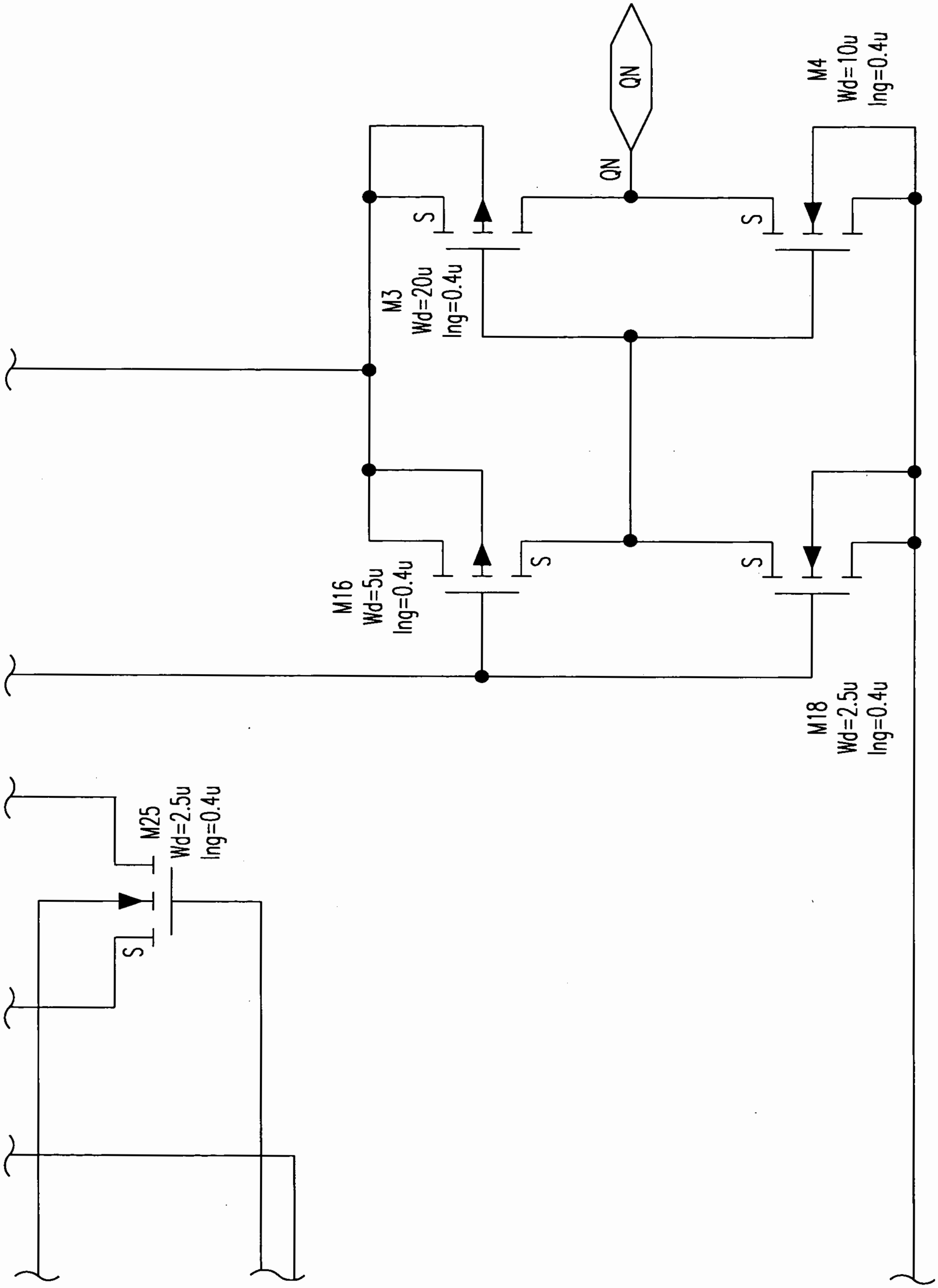

QN
QN
M4
Wd=10u
lng=0.4u
M3
Wd=20u
lng=0.4u
M16
Wd=5u
lng=0.4u
M18
Wd=2.5u
lng=0.4u
M25
Wd=2.5u
lng=0.4u
S
S
S
S
S
S

FIG. 150F

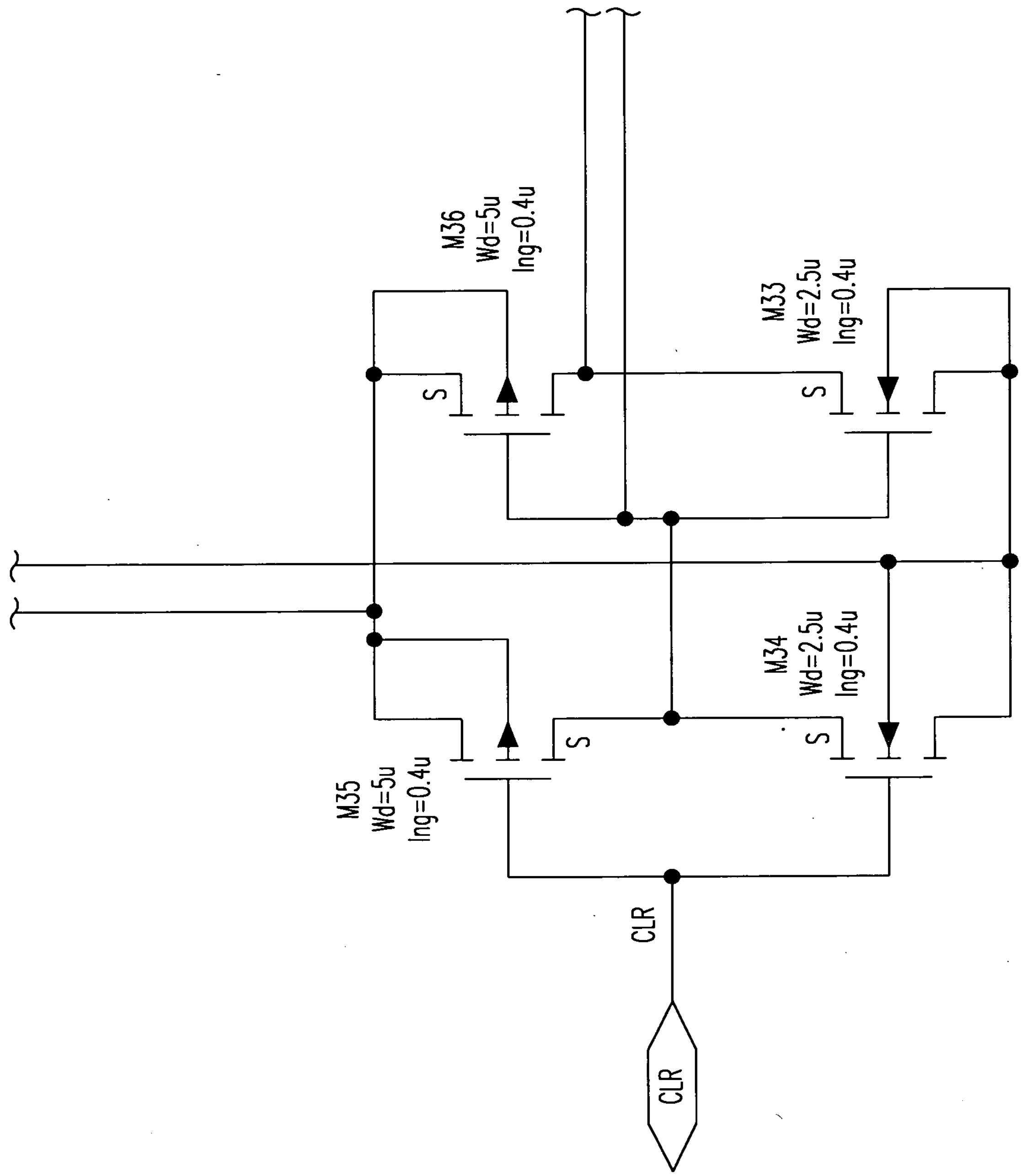
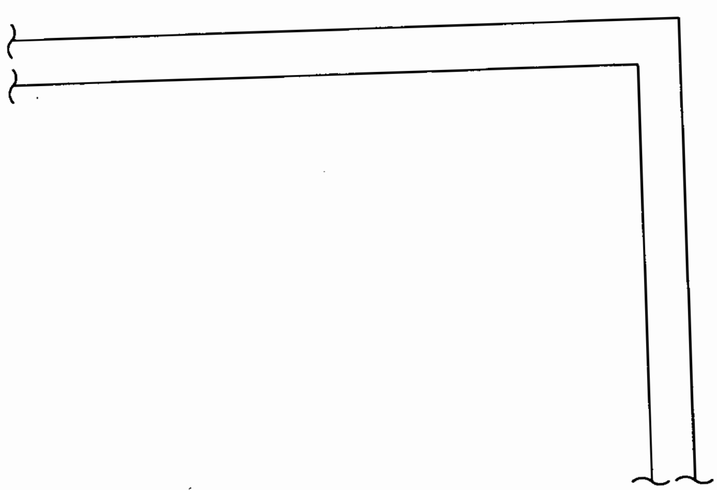

M36
Wd=5u
lng=0.4u
M33
Wd=2.5u
lng=0.4u
M34
Wd=2.5u
lng=0.4u
M35
Wd=5u
lng=0.4u
S
S
S
S
CLR
CLR

FIG.150G

FIG.150H



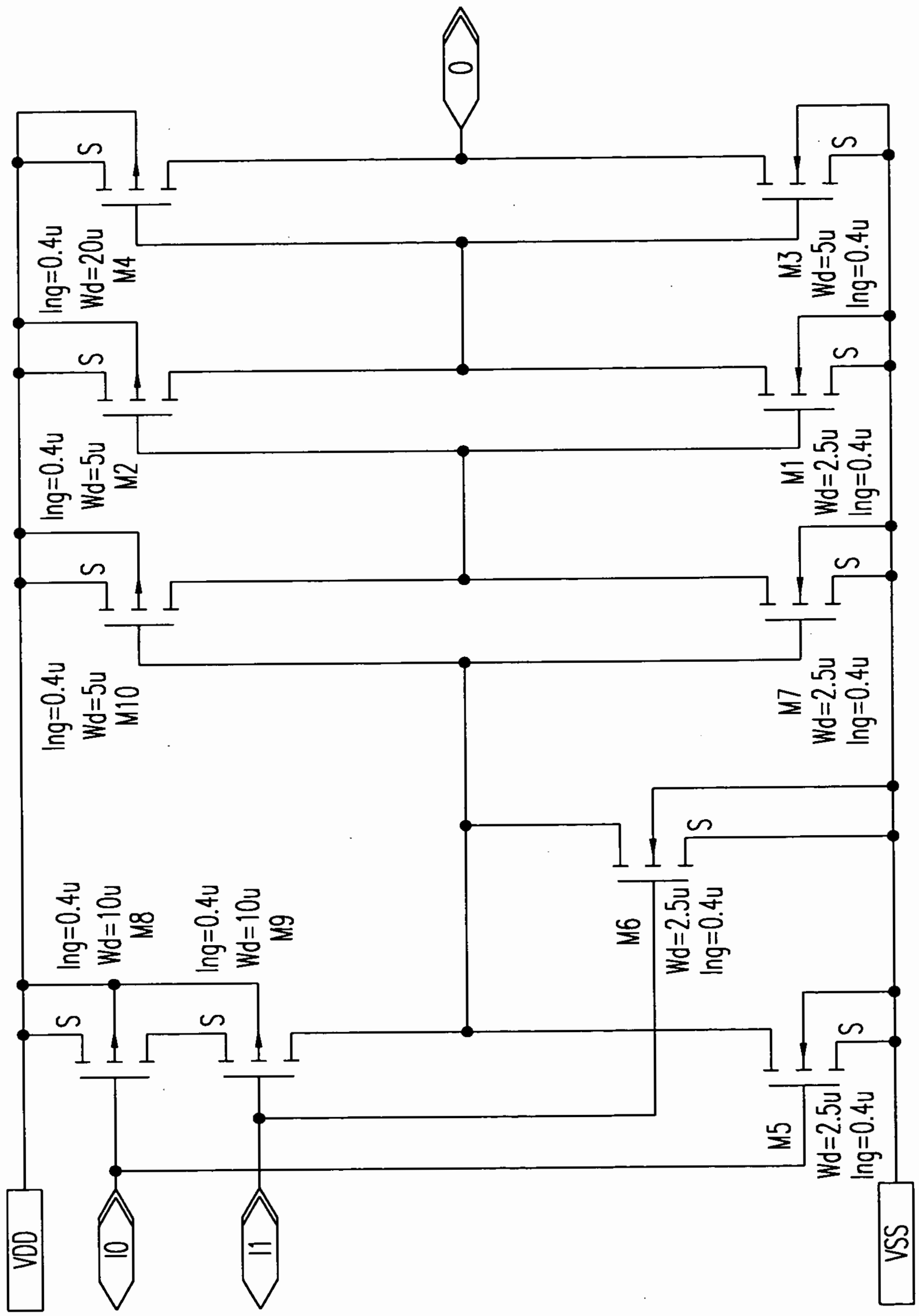

O
S
lng=0.4u
Wd=20u
M4
M3
Wd=5u
lng=0.4u
lng=0.4u
Wd=5u
M2
M1
Wd=2.5u
lng=0.4u
lng=0.4u
Wd=5u
M10
M7
Wd=2.5u
lng=0.4u
lng=0.4u
Wd=10u
M8
lng=0.4u
Wd=10u
M9
M6
Wd=2.5u
lng=0.4u
M5
Wd=2.5u
lng=0.4u
VDD
I0
I1
VSS

FIG.151

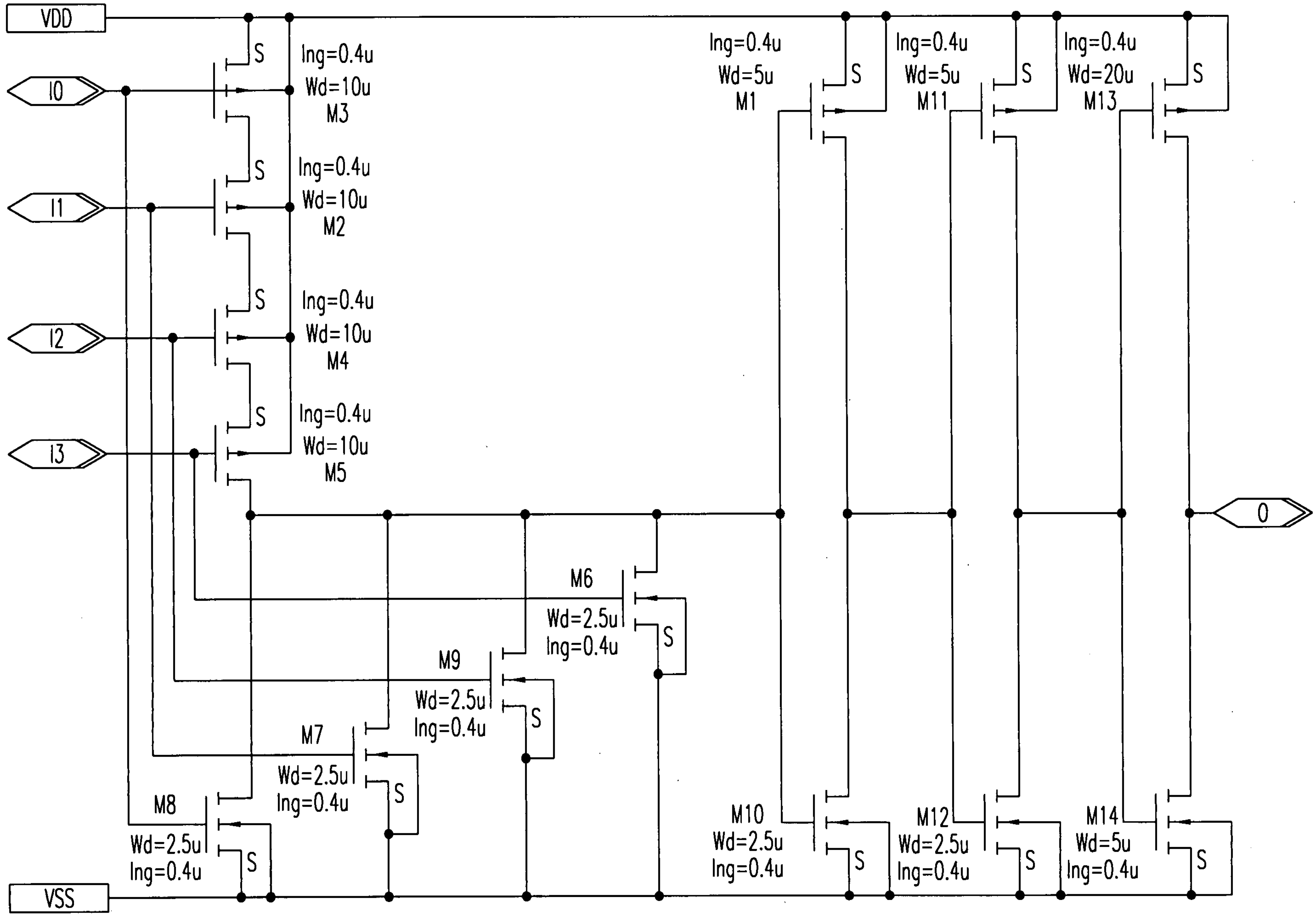


FIG.152

Replacement Sheet
Sheet 334 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

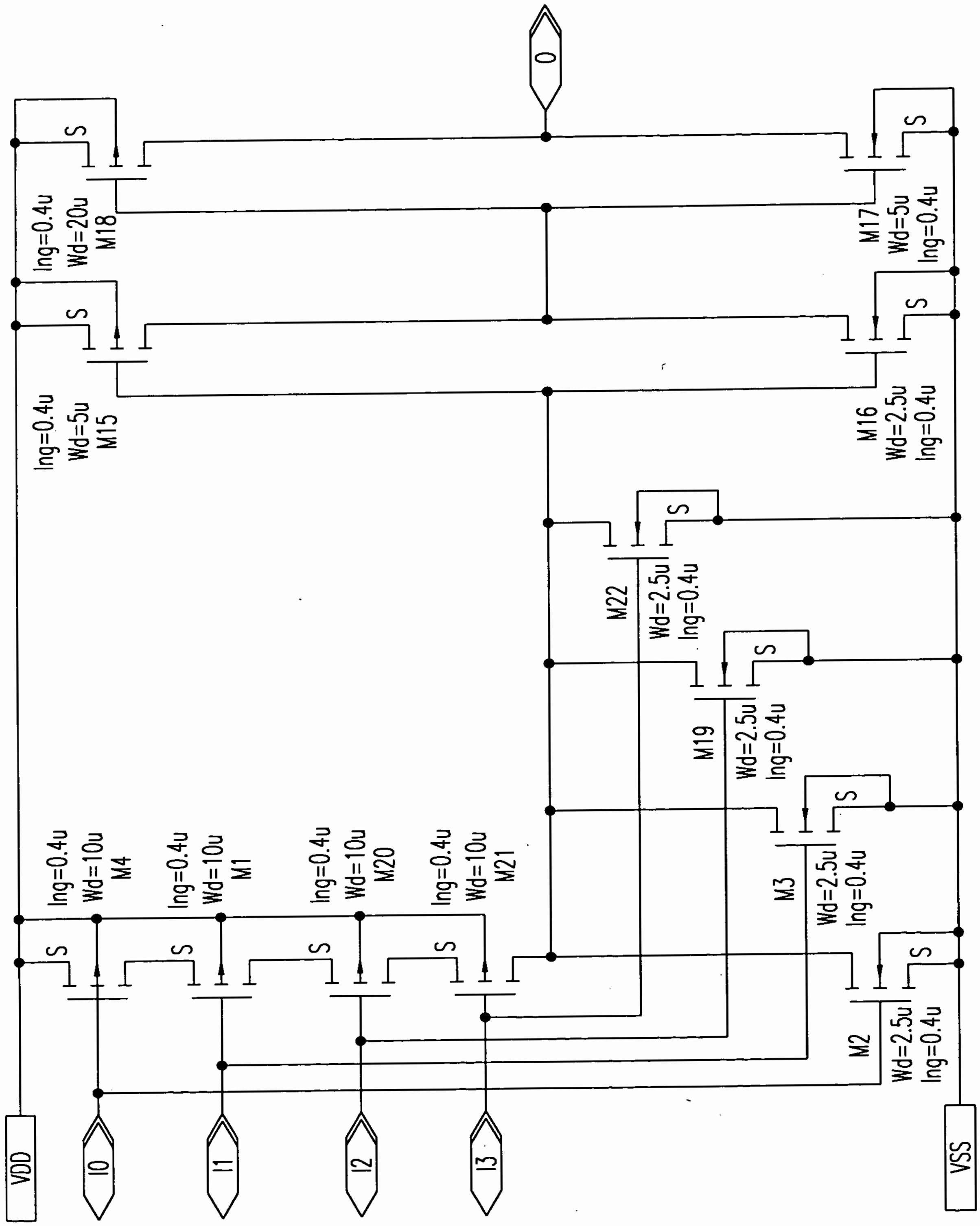

O
lng=0.4u
Wd=20u
M18
M17
Wd=5u
lng=0.4u
lng=0.4u
Wd=5u
M15
M16
Wd=2.5u
lng=0.4u
M22
Wd=2.5u
lng=0.4u
M19
Wd=2.5u
lng=0.4u
M3
Wd=2.5u
lng=0.4u
M2
Wd=2.5u
lng=0.4u
lng=0.4u
Wd=10u
M4
lng=0.4u
Wd=10u
M1
lng=0.4u
Wd=10u
M20
lng=0.4u
Wd=10u
M21
S
VDD
I0
I1
I2
I3
VSS

FIG.153

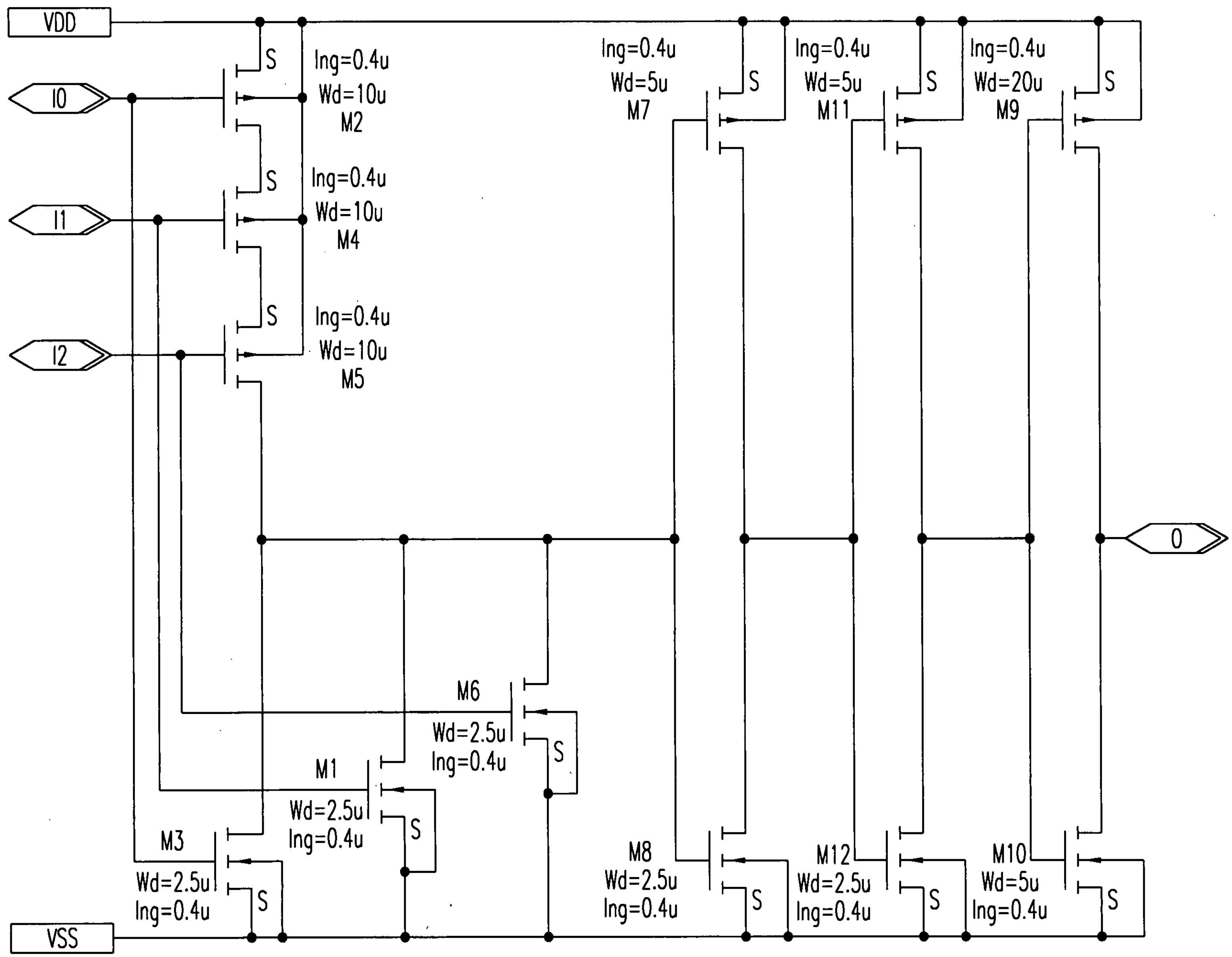


FIG.154

Replacement Sheet
Sheet 336 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit...

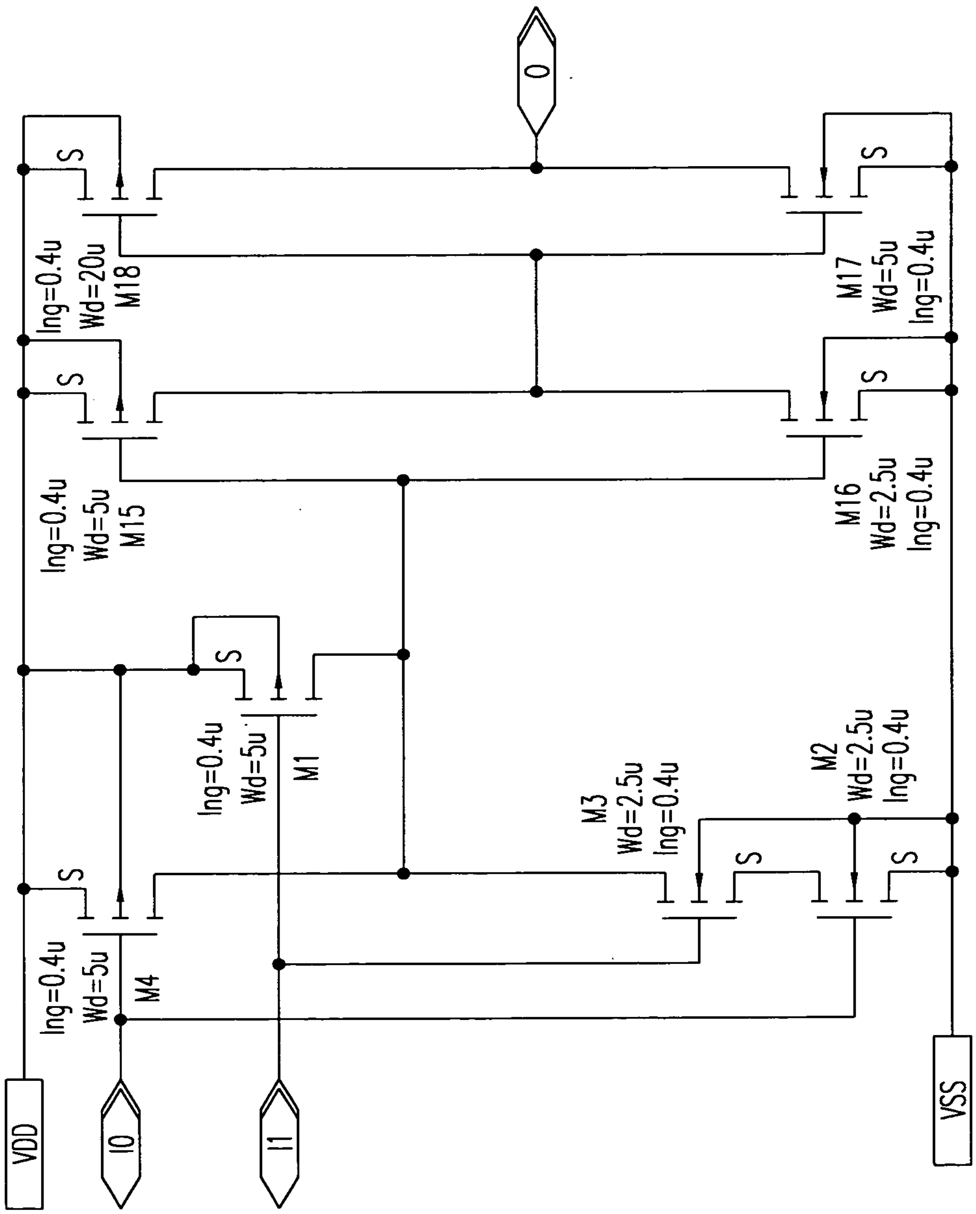

O
S
lng=0.4u
Wd=20u
M18
M17
Wd=5u
lng=0.4u
lng=0.4u
Wd=5u
M15
M16
Wd=2.5u
lng=0.4u
lng=0.4u
Wd=5u
M1
M3
Wd=2.5u
lng=0.4u
M2
Wd=2.5u
lng=0.4u
lng=0.4u
Wd=5u
M4
VDD
I0
I1
VSS

FIG. 155

Replacement Sheet
Sheet 338 of 349
Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

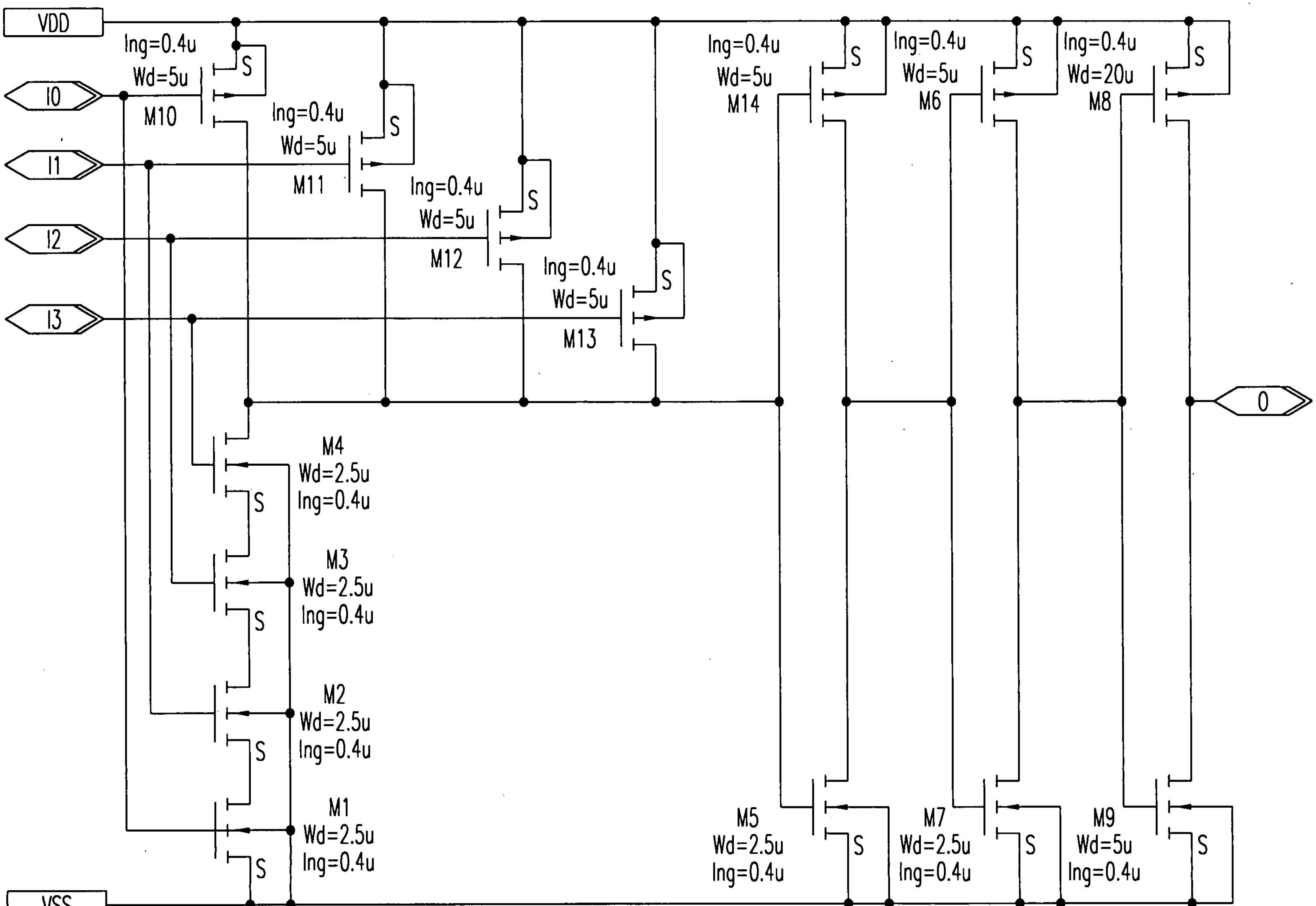


FIG.156

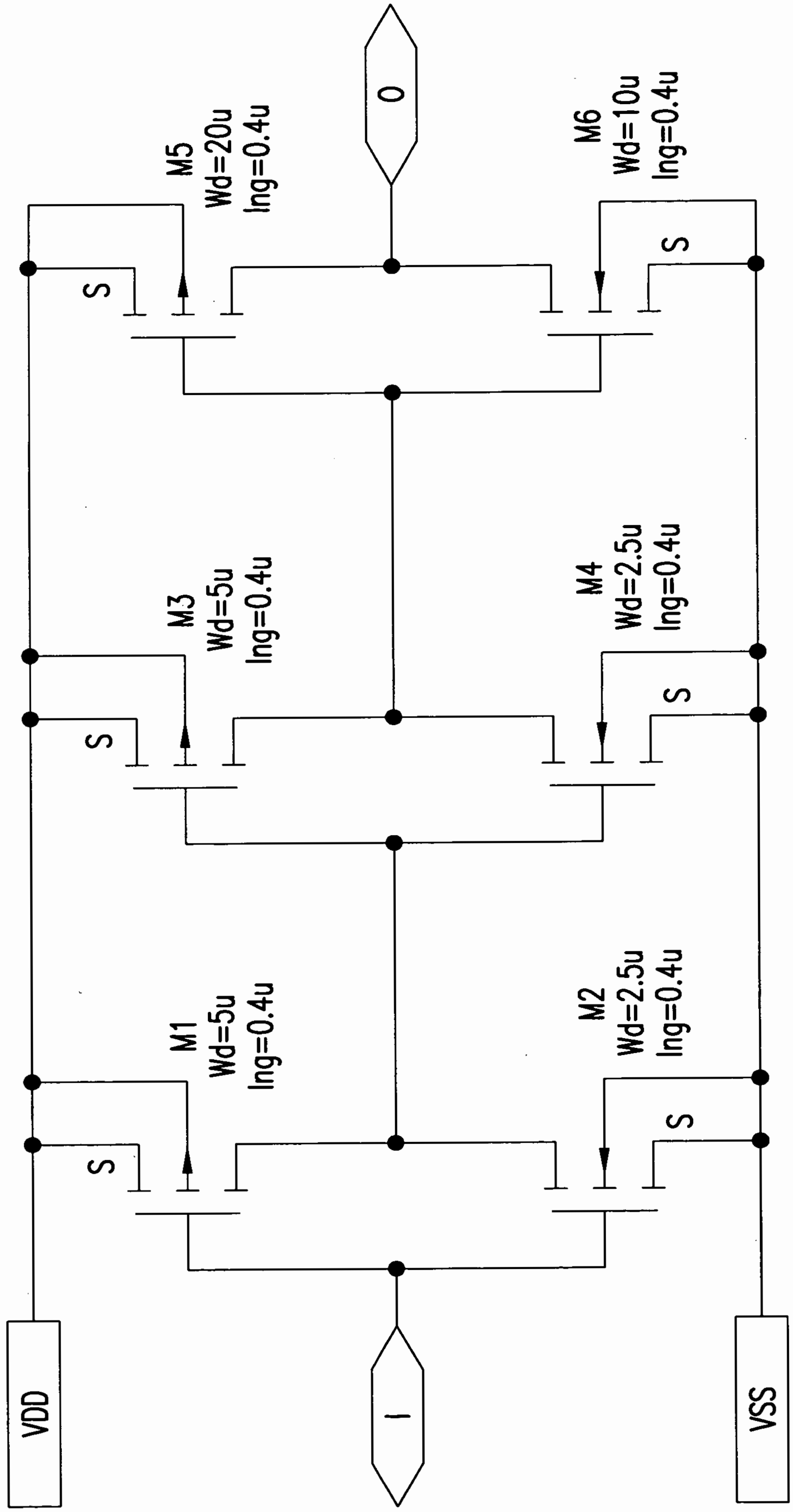

O
M5
Wd=20u
lng=0.4u
M6
Wd=10u
lng=0.4u
M3
Wd=5u
lng=0.4u
M4
Wd=2.5u
lng=0.4u
M1
Wd=5u
lng=0.4u
M2
Wd=2.5u
lng=0.4u
S
S
S
S
S
S
VDD
I
VSS

FIG.157

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

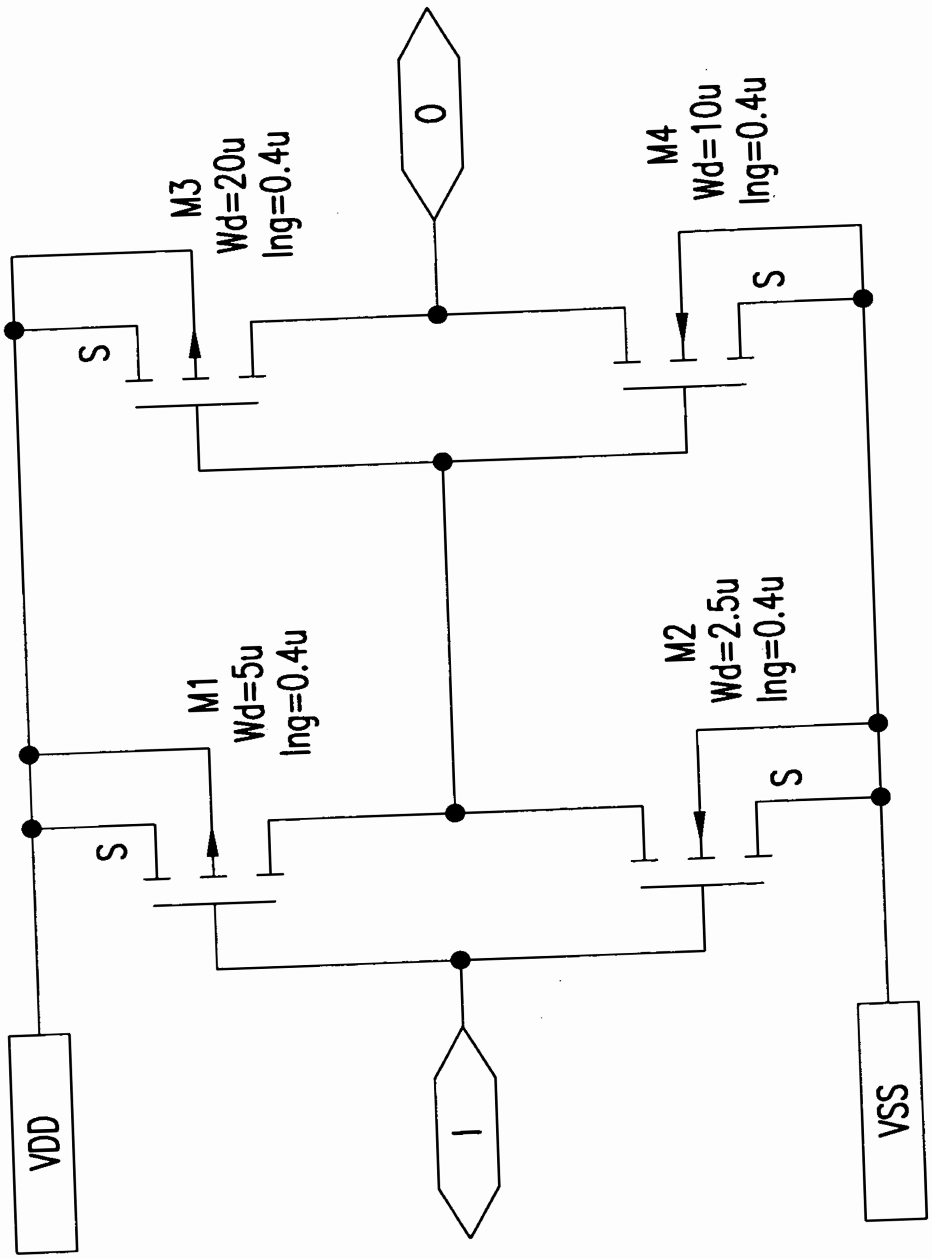


FIG.158

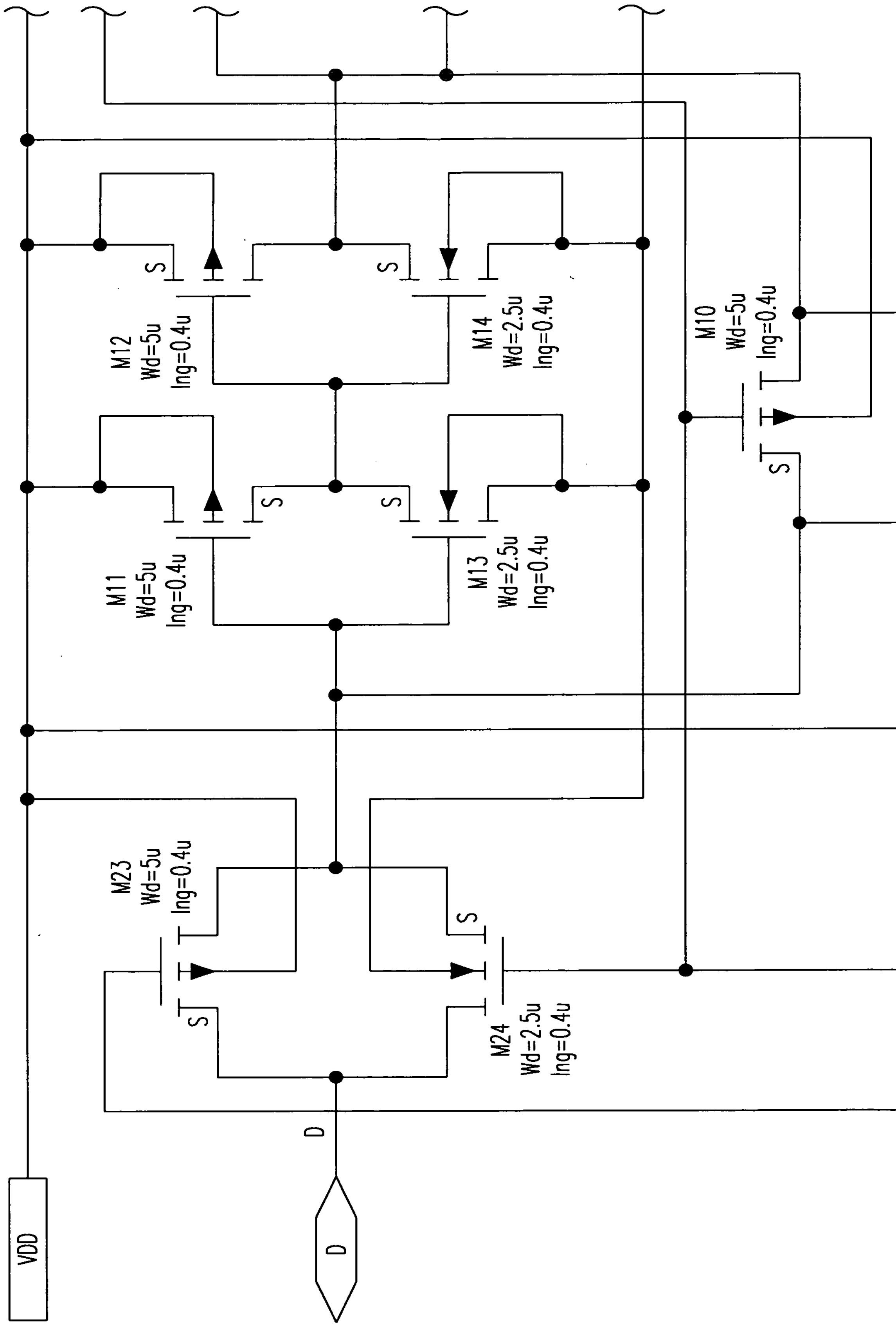
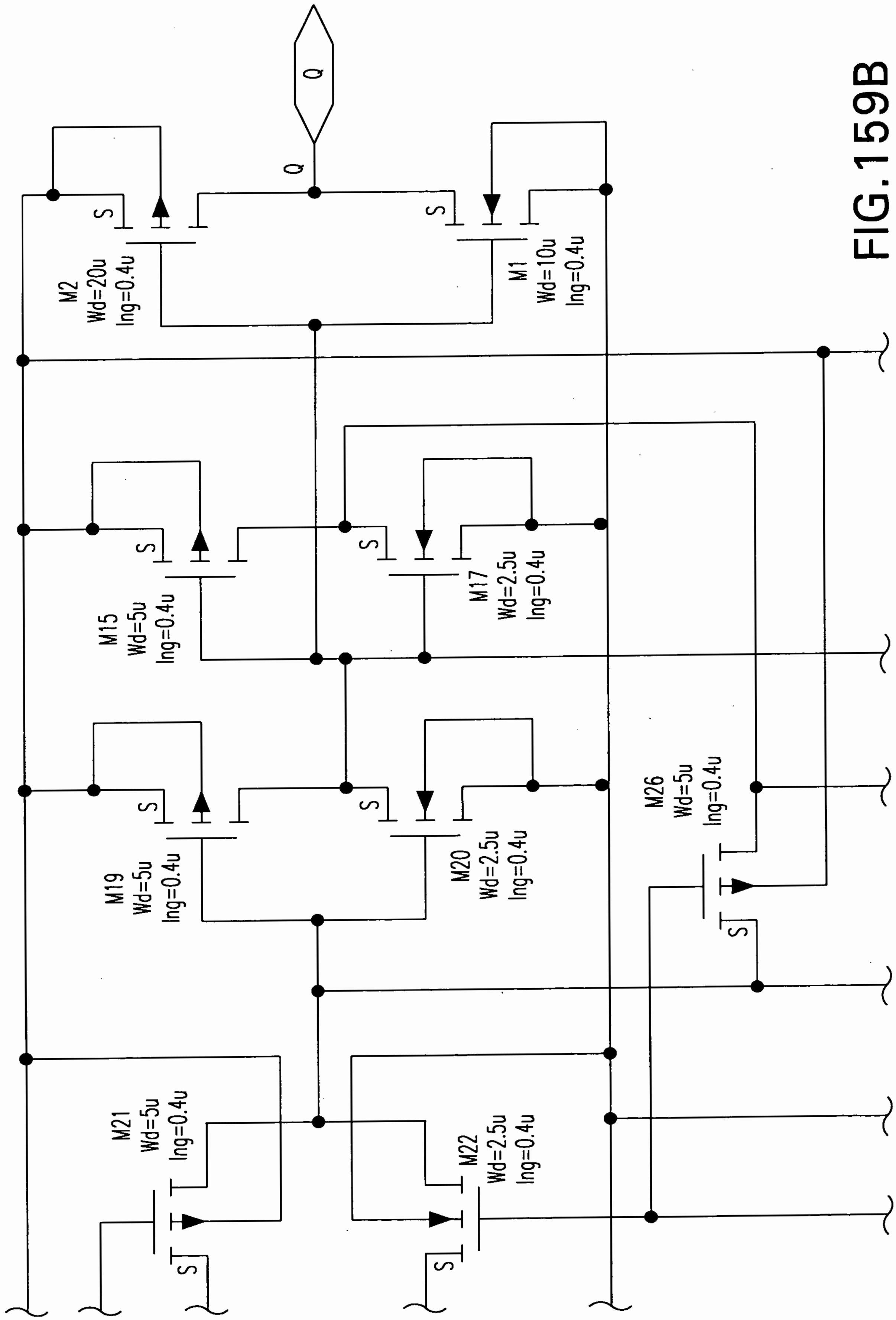

M12
Wd=5u
lng=0.4u
M14
Wd=2.5u
lng=0.4u
M10
Wd=5u
lng=0.4u
M11
Wd=5u
lng=0.4u
M13
Wd=2.5u
lng=0.4u
M23
Wd=5u
lng=0.4u
M24
Wd=2.5u
lng=0.4u
S
D
VDD

FIG.159A


Q
Q
M2
Wd=20u
lng=0.4u
M1
Wd=10u
lng=0.4u
M15
Wd=5u
lng=0.4u
M17
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lng=0.4u
M19
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lng=0.4u
M21
Wd=5u
lng=0.4u
M22
Wd=2.5u
lng=0.4u
S

FIG.159B

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

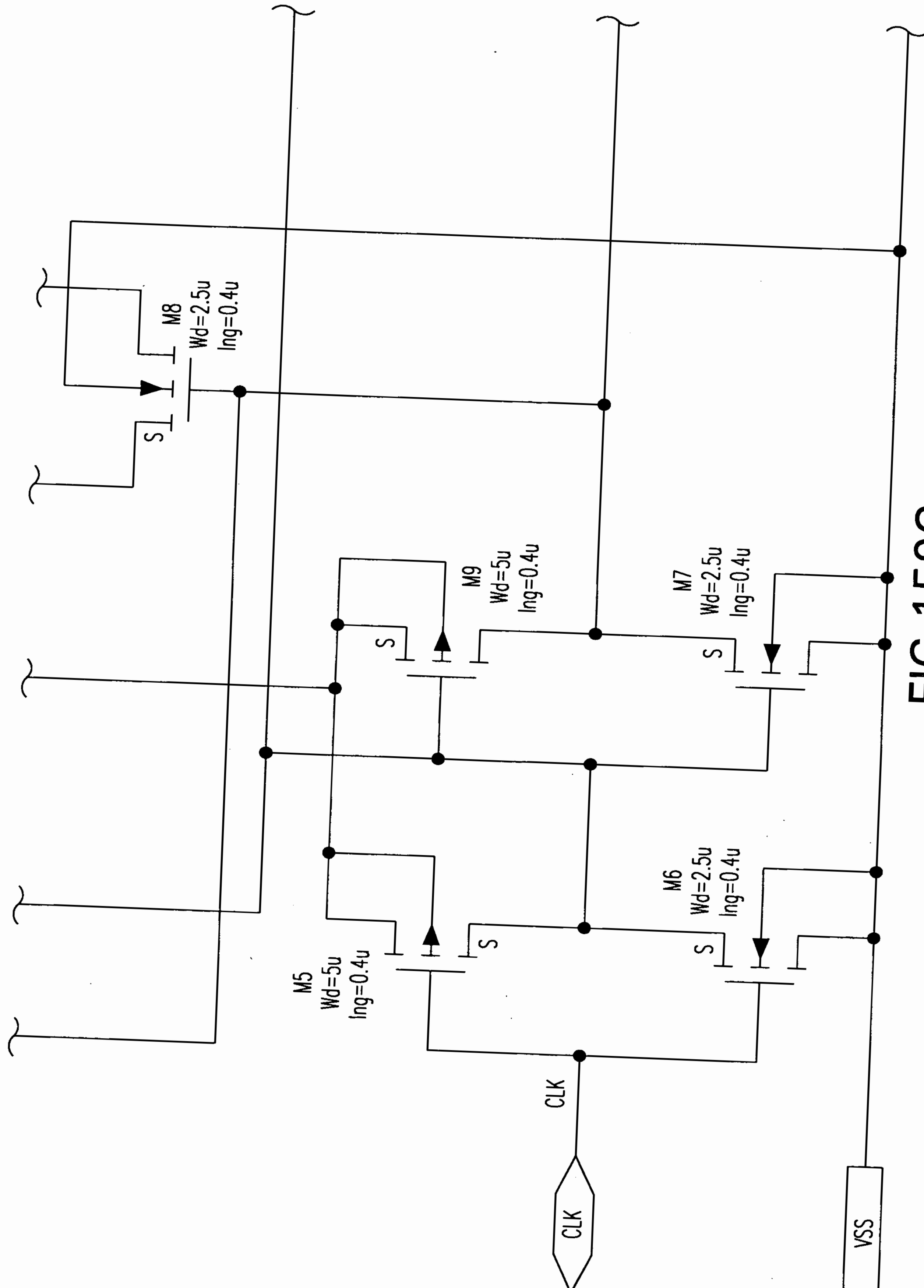

FIG. 159C

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology
Including Multi-Phase Embodiments and Circuit

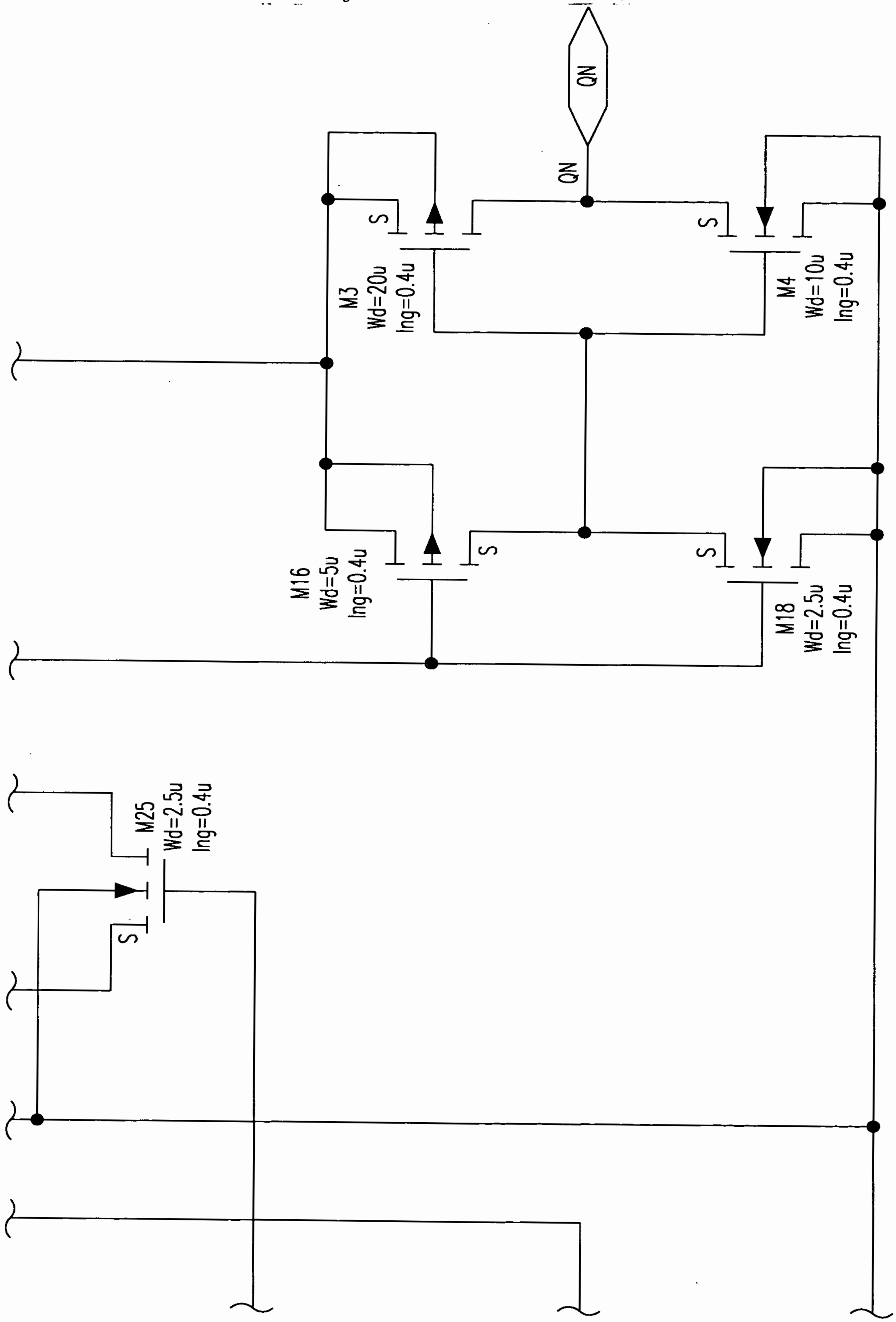

FIG.159D

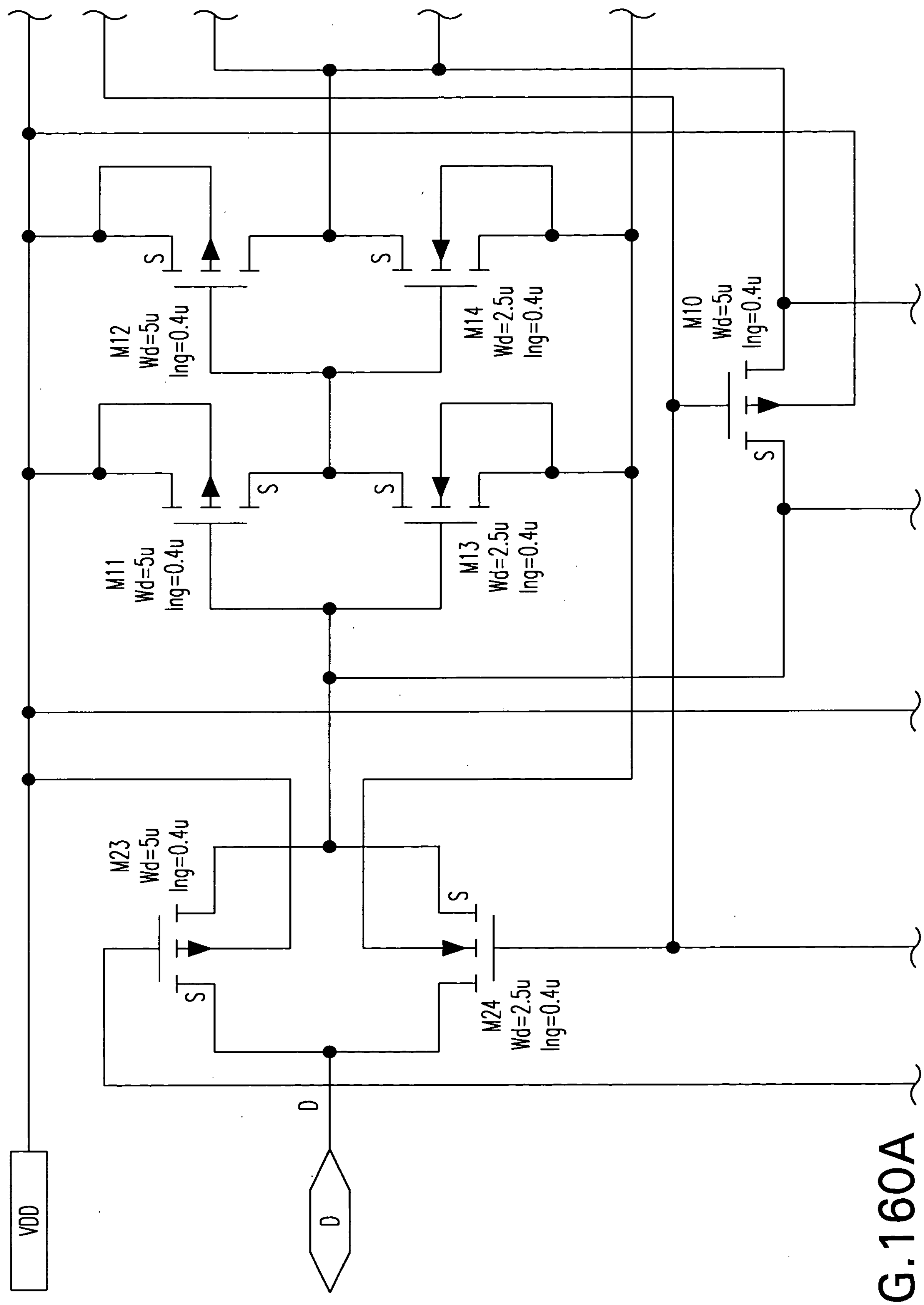
M12
Wd=5u
lng=0.4u
M14
Wd=2.5u
lng=0.4u
M10
Wd=5u
lng=0.4u
M11
Wd=5u
lng=0.4u
M13
Wd=2.5u
lng=0.4u
M23
Wd=5u
lng=0.4u
M24
Wd=2.5u
lng=0.4u
S
D
VDD

FIG.160A

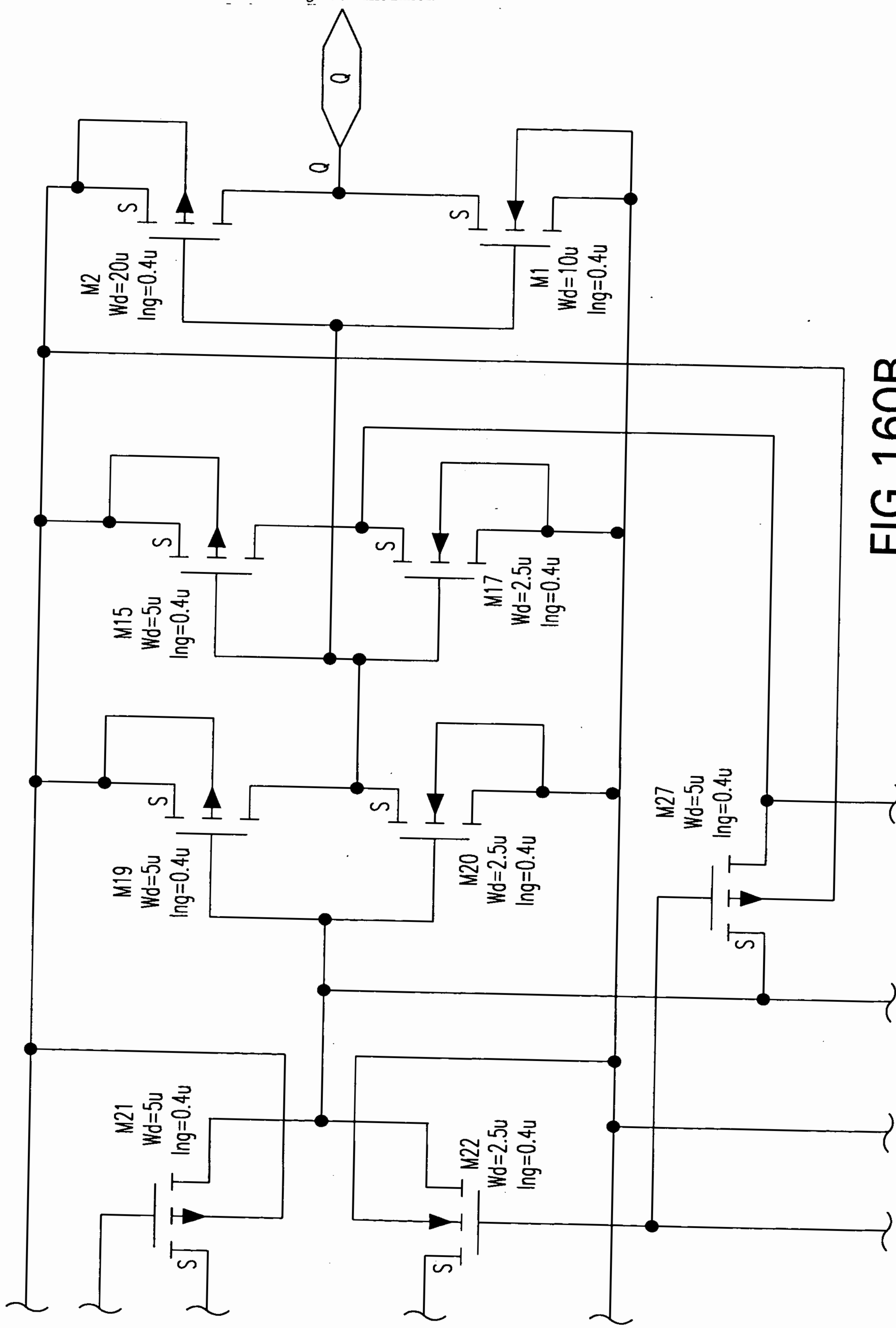
Q
Q
M2
Wd=20u
lng=0.4u
M1
Wd=10u
lng=0.4u
M15
Wd=5u
lng=0.4u
M17
Wd=2.5u
lng=0.4u
M19
Wd=5u
lng=0.4u
M20
Wd=2.5u
lng=0.4u
M27
Wd=5u
lng=0.4u
M21
Wd=5u
lng=0.4u
M22
Wd=2.5u
lng=0.4u
S

FIG.160B

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

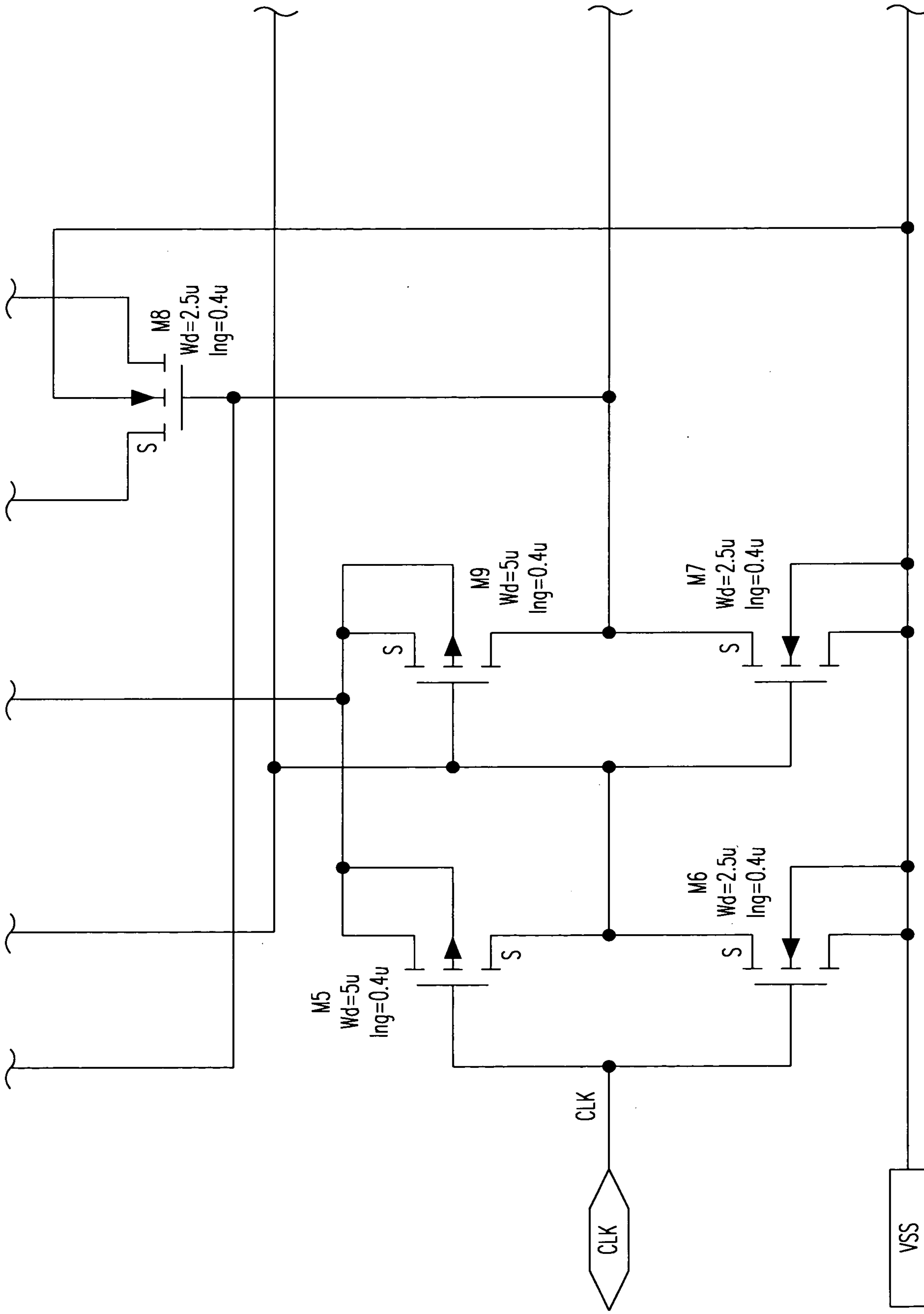

FIG.160C

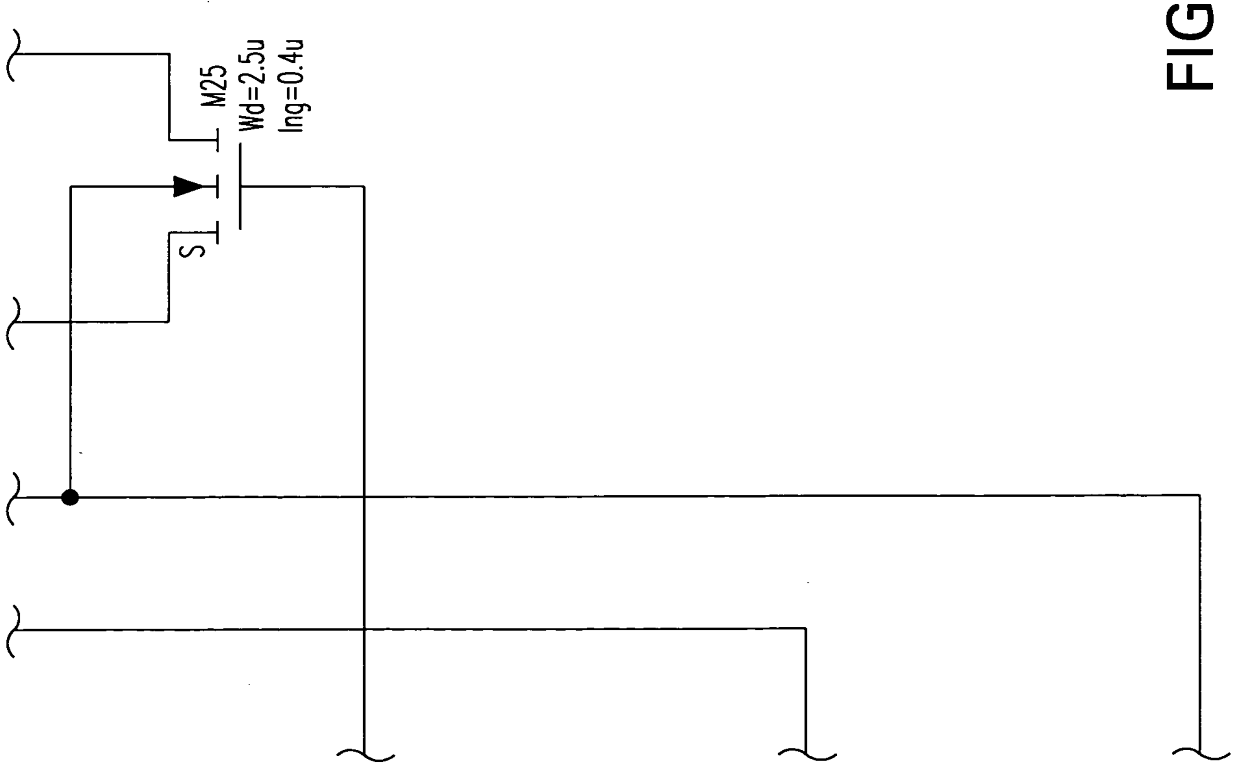

FIG.160D

Appl. No. 09/632,856; Filed: Aug 4, 2000
Dkt No. 1744.0630003; Group Unit: 2634
Inventors: Sorrells et al.
Tel. No.: 202-371-2600
For: Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit

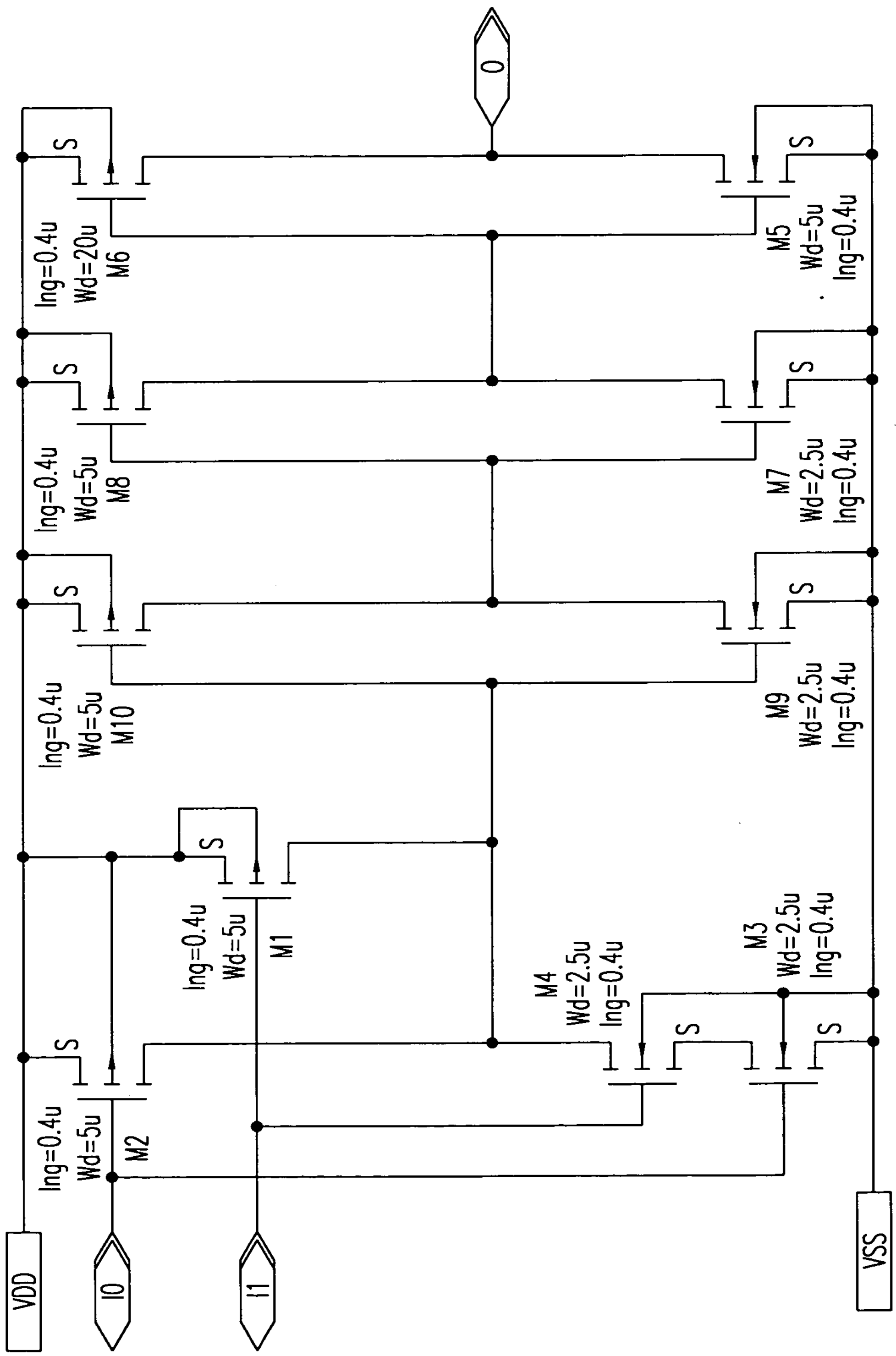

FIG.161

IMage / $

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Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
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Alexandria, Virginia 22313-1450

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7590 09/10/2004

Sterne Kessler Goldstein & Fox P L L C
Suite 600 1100 New York Avenue N W
Washington, DC 20005-3934

OIPE JC174 DEC 10 2004 PATENT & TRADEMARK OFFICE

12/13/2004 EAREGAY2 00000158 09632856

01 FC:1501 1400.00 OP
02 FC:8001 3.00 OP

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(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/632,856	08/04/2000	David F. Sorrells	1744.0630003	2377

TITLE OF INVENTION: WIRELESS LOCAL AREA NETWORK (WLAN) USING UNIVERSAL FREQUENCY TRANSLATION TECHNOLOGY INCLUDING MULTI-PHASE EMBODIMENTS AND CIRCUIT IMPLEMENTATIONS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1330	$0	$1330	12/10/2004

EXAMINER	ART UNIT	CLASS-SUBCLASS
KIM, KEVIN	2634	375-222000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Sterne, Kessler, Goldstein & Fox P.L.L.C.
2 ____
3 ____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: ParkerVision, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Jacksonville, Florida

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:
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- ☐ Publication Fee (No small entity discount permitted)
- ☒ Advance Order - # of Copies 1

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- ☒ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized by charge ~~the required fee(s)~~ any deficiencies in, or credit any overpayment, to Deposit Account Number 19-0036 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.
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Authorized Signature JTA Helvey Date 12/10/04

Typed or printed name Jeffrey T. Helvey Registration No. 44,757

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PTO/SB/17 (10-04v2)
Approved for use through 07/31/2006. OMB 0651-0032
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FEE TRANSMITTAL for FY 2005

Effective 10/01/2004. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 1,403.00

Complete if Known	
Application Number	09/632,856
Filing Date	August 4, 2000
First Named Inventor	David F. Sorrells
Examiner Name	Kim, Kevin
Art Unit	2634
Attorney Docket No.	1744.0630003

METHOD OF PAYMENT (check all that apply)

☐ Check ☒ Credit card ☐ Money Order ☒ Other ☐ None

☐ Deposit Account: **Charge any deficiencies or credit any overpayments in the fees to Deposit Acct. No. 19-0036.

Deposit Account Number: 19-0036

Deposit Account Name: Sterne, Kessler, Goldstein & Fox P.L.L.C.

The Director is authorized to: *(check all that apply)*

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☐ Charge any additional fee(s) or any underpayment of fee(s)

☐ Charge fee(s) indicated below, **except for the filing fee**

to the above-identified deposit account.

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Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
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1002	350	2002	175	Design filing fee	
1003	550	2003	275	Plant filing fee	
1004	790	2004	395	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 0.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims		Fee from below		Fee Paid
Total Claims	32	-** 40 =	0	X	$18.00	=	$0.00
Independent Claims	5	-** 5 =	0	X	$88.00	=	$0.00
Multiple Dependent					$300.00	=	$0.00

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	88	2201	44	Independent claims in excess of 3
1203	300	2203	150	Multiple dependent claim, if not paid
1204	88	2204	44	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0.00

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	430	2252	215	Extension for reply within second month	
1253	980	2253	490	Extension for reply within third month	
1254	1,530	2254	765	Extension for reply within fourth month	
1255	2,080	2255	1,040	Extension for reply within fifth month	
1401	340	2401	170	Notice of Appeal	
1402	340	2402	170	Filing a brief in support of an appeal	
1403	300	2403	150	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,370	2453	685	Petition to revive - unintentional	
1501	1,370	2501	685	Utility issue fee (or reissue)	$1,400.00
1502	490	2502	245	Design issue fee	
1503	660	2503	330	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	790	2809	395	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR 1.129(b))	
1801	790	2801	395	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) Advance copies of patent. $3.00

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 1,403.00

SUBMITTED BY

(Complete *(if applicable)*)

Name *(Print/Type)*	Jeffrey T. Helvey	Registration No. *(Attorney/Agent)*	44,757	Telephone	(202) 371-2600
Signature	JTHelvey			Date	12/10/04

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09/632,856UA

Indicate quantity of a single type of artifact received but not scanned. Create individual artifact folder/box and artifact number for each Artifact Type.

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  Doc Code: Computer — Artifact Type Code: P
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  Doc Code: Artifact — Artifact Type Code: S
- content unspecified or combined [✓] IDS References
  Doc Code: Artifact — Artifact Type Code: U

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Doc Code: Artifact — Artifact Type Code: C

[ ] Microfilm(s)
Doc Code: Artifact — Artifact Type Code: F

[ ] Video tape(s)
Doc Code: Artifact — Artifact Type Code: V

[ ] Model(s)
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[ ] Other, description: ____________________
Doc Code: Artifact — Artifact Type Code: Z

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Serial No./Control No. 09/632856
Reviewed By: K. SMITH Phone: 308 9210 ext. 118

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☐ The compact discs are unreadable.

☐ The files on the compact discs are not in ASCII.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/632,856	08/04/2000	David F. Sorrells	1744.0630003	2377

7590 11/16/2005

Sterne Kessler Goldstein & Fox P L L C
Suite 600 1100 New York Avenue N W
Washington, DC 20005-3934

EXAMINER	
KIM, KEVIN	

ART UNIT	PAPER NUMBER
2634	

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PTO-90C (Rev. 10/03)

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APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
09/632,856	08/04/2004	David F. Sorrells	1744.0630003

EXAMINER	
Kim, Kevin	
ART UNIT	**PAPER**
	3

DATE MAILED:

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Commissioner for Patents

Attachments: Information Disclosure Statements (PTO 1449s)

Kevin Kim

KEVIN KIM
PATENT EXAMINER

PTO-90C (Rev.04-03)

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on November 12, 2004 was filed after the mailing date of the Notice of Allowability on September 10, 2004. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has been considered by the examiner. In addition, the previously submitted IDS on July 25, 2002, June 9, 2003, January 23, 2004, August 19, 2004 has been considered and initialed and dated copies of PTO-1449s are hereby returned to applicant.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Y. Kim whose telephone number is 571-272-3039. The examiner can normally be reached on 8AM --5PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Vanderpuye can be reached on 571-272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kevin Kim

KEVIN KIM
PATENT EXAMINER

● PRINTER RUSH ●
(PTO ASSISTANCE)

CORRESPONDENCE
HARD COPY

Application :	09/632856	**Examiner :**	Kim, K.	**GAU :**	2638
From:	AMW	**Location:**	IDC FMF FDC	**Date:**	12/5/05

Tracking #: ____________ Week Date: ____________

DOC CODE	DOC DATE	MISCELLANEOUS
☒ 1449	11-16-2005	☐ Continuing Data
☐ IDS		☐ Foreign Priority
☐ CLM		☐ Document Legibility
☐ IIFW		☐ Fees
☐ SRFW		☐ Other
☐ DRW		
☐ OATH		
☐ 312		
☐ SPEC		

[RUSH] **MESSAGE:** Please initial or strike each entry on each page of the 11-16-2005 1449 document.

See p. 68-72 in EDAN.

THANK YOU, AMW

[XRUSH] **RESPONSE:**

INITIALS:

NOTE: This form will be included as part of the official USPTO record, with the Response document coded as XRUSH.

REV 10/04

Ebn

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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/632,856	08/04/2000	David F. Sorrells	1744.0630003	2377

7590 01/12/2006

Sterne Kessler Goldstein & Fox P L L C
Suite 600 1100 New York Avenue N W
Washington, DC 20005-3934

EXAMINER	
KIM, KEVIN	
ART UNIT	**PAPER NUMBER**
2634	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Supplemental Notice of Allowability	Application No.	Applicant(s)	
	09/632,856	SORRELLS ET AL.	
	Examiner	**Art Unit**	
	Kevin Y. Kim	2638	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed on 7-27-2004*.

2. ☒ The allowed claim(s) is/are *42-71,77 renumbered as 1-32*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
   1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

KEVIN KIM
PATENT EXAMINER

OIPE JC19
AUG 1 9 2004
PATENT & TRADEMARK OFFICE

FORM PTO-1449 THIRD SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	INVENTORS SORRELLS *et al.*	
	FILING DATE August 4, 2000	ART UNIT 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF56	6,687,493 B1	02/2004	Sorrells *et al.*			
	AG56	6,694,128 B1	02/2004	Sorrells *et al.*			
	AH56	6,031,217	02/2000	Aswell *et al.*			
	AI56	5,955,992	09/1999	Shattil			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL23	DE 196 48 915 A1	06/1998	DE			Yes (Doc. AO59)
	AM						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN		
	AO	59	English Translation of German Patent Publication No. DE 196 48 915 A1, 10 pages.
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	AQ		
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EXAMINER	DATE CONSIDERED 11/09/05

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

300146_1.DOC

FORM PTO-1449 THIRD SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	INVENTORS SORRELLS *et al.*	
	FILING DATE August 4, 2000	ART UNIT 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
K	AA57	5,999,561	12/1999	Naden *et al.*			
	AB57	6,686,879 B2	02/2004	Shattil			
	AC57	6,704,549 B1	03/2004	Sorrells *et al.*			
	AD57	6,704,558 B1	03/2004	Sorrells *et al.*			
	AE57	5,490,176	02/1996	Peltier			
	AF57	5,970,053	10/1999	Schick *et al.*			
	AG57	6,078,630	06/2000	Prasanna			
	AH57	6,600,911 B1	07/2003	Morishige *et al.*			
K	AI57	5,179,731	01/1993	Tränkle *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

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EXAMINER [illegible signature]	DATE CONSIDERED 11/03/05

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	INVENTORS SORRELLS *et al.*	
	FILING DATE August 4, 2000	ART UNIT 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
K	AA58	5,589,793	12/1996	Kassapian			
	AB58	4,510,467	04/1985	Chang *et al.*			
	AC58	4,772,853	09/1988	Hart			
	AD58	4,972,436	11/1990	Halim *et al.*			
	AE58	5,012,245	04/1991	Scott *et al.*			
	AF58	5,422,909	06/1995	Love *et al.*			
	AG58	5,440,311	08/1995	Gallagher *et al.*			
	AH58	5,926,513	07/1999	Suominen *et al.*			
K	AI58	5,995,030	11/1999	Cabler			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

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EXAMINER	DATE CONSIDERED
/K/	11/07/01

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FORM PTO-1449 THIRD SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	INVENTORS SORRELLS *et al.*	
	FILING DATE August 4, 2000	ART UNIT 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
K	AA59	6,047,026	04/2000	Chao *et al.*			
	AB59	6,049,573	04/2000	Song			
	AC59	6,076,015	06/2000	Hartley *et al.*			
	AD59	6,144,331	11/2000	Jiang			
	AE59	5,058,107	10/1991	Stone *et al.*			
	AF59	5,757,858	05/1998	Black *et al.*			
	AG59	6,531,979 B1	03/2003	Hynes			
	AH59	6,018,262	01/2000	Noro *et al.*			
k	AI59	4,761,798	08/1988	Griswold, Jr. *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
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	AL						Yes No
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OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

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EXAMINER	DATE CONSIDERED
K	11/07/05

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	INVENTORS SORRELLS *et al.*	
	FILING DATE August 4, 2000	ART UNIT 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
K	AA60	5,982,315	11/1999	Bazarjani *et al.*			
	AB60	6,459,721 B1	10/2002	Mochizuki *et al.*			
	AC60	6,151,354	11/2000	Abbey			
	AD60	6,169,733 B1	01/2001	Lee			
	AE60	6,363,262 B1	03/2002	McNicol			
	AF60	6,697,603 B1	02/2004	Lovinggood *et al.*			
	AG60	5,262,222	01/1994	Fattouche *et al.*			
	AH60	5,949,827	09/1999	DeLuca *et al.*			
K	AI60	6,014,176	01/2000	Nayebi *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
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	INVENTORS SORRELLS *et al.*	
	FILING DATE August 4, 2000	ART UNIT 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
K	AA61	5,678,226	10/1997	Li *et al.*			
	AB61	5,760,632	06/1998	Kawakami *et al.*			
	AC61	6,160,280	12/2000	Bonn *et al.*			
	AD61	5,481,570	01/1996	Winters			
	AE61	5,745,846	04/1998	Myer *et al.*			
K	AF61	5,345,239	09/1994	Madni *et al.*			
	AG						
	AH						
	AI						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
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/a	11/07/05

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300146_1.DOC

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CORRESPONDENCE HARD COPY

Application :	09/632856	**Examiner :**	Kim, K.	**GAU :**	2638
From:	AMW	**Location:**	IDC **FMF** FDC	**Date:**	12/5/05

Tracking #: ____________ Week Date: ____________

DOC CODE	**DOC DATE**	**MISCELLANEOUS**
☒ 1449	11-16-2005	☐ Continuing Data
☐ IDS		☐ Foreign Priority
☐ CLM		☐ Document Legibility
☐ IIFW		☐ Fees
☐ SRFW		☐ Other
☐ DRW		
☐ OATH		
☐ 312		
☐ SPEC		

[RUSH] **MESSAGE:** Please initial or strike each entry on each page of the 11-16-2005 1449 document.

See p. 68-72 in EDAN.

THANK YOU, AMW

[XRUSH] **RESPONSE:**

Pages 68-72 of IDS have been initialed and signed

INITIALS: K.

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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/632,856	08/04/2000	David F. Sorrells	1744.0630003	2377

7590 02/02/2006

Sterne Kessler Goldstein & Fox P L L C
Suite 600 1100 New York Avenue N W
Washington, DC 20005-3934

EXAMINER	
KIM, KEVIN	
ART UNIT	**PAPER NUMBER**
2634	

DATE MAILED: 02/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

aa

Response to Rule 312 Communication	Application No.	Applicant(s)	
	09/632,856	SORRELLS ET AL.	
	Examiner	Art Unit	
	Kevin Y. Kim	2638	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☒ The amendment filed on *10 December 2004* under 37 CFR 1.312 has been considered, and has been:

   a) ☐ entered.

   b) ☒ entered as directed to matters of form not affecting the scope of the invention.

   c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
   Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

   d) ☐ disapproved. See explanation below.

   e) ☐ entered in part. See explanation below.

KEVIN KIM
PATENT EXAMINER

K. Kim 1/30/06

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(PTO ASSISTANCE)

CORRESP.
HC

Application :	09/632856	**Examiner :**	Kim, K.	**GAU :**	2638
From:	AMW / (A)	**Location:**	IDC **(FMF)** FDC	**Date:**	2/24/06

2nd REQUEST

Tracking #: ______ Week Date: ______

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☐ 312		
☐ SPEC		

[RUSH] **MESSAGE:** Please initial or strike each entry on each page of the 11-16-2005 1449 document. Specifically, please see page 60 of 76.

Thank you,
AMW

[XRUSH] **RESPONSE:**

INITIALS:

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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7590 03/17/2006

Sterne Kessler Goldstein & Fox P L L C
Suite 600 1100 New York Avenue N W
Washington, DC 20005-3934

EXAMINER	
KIM, KEVIN	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 03/17/2006

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PTO-90C (Rev. 10/03)

H'A

Supplemental Notice of Allowability	Application No. 09/632,856	Applicant(s) SORRELLS ET AL.	
	Examiner Kevin Y. Kim	Art Unit 2638	

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2. ☒ The allowed claim(s) is/are 42-71,77.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
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   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
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   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
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7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

KEVIN KIM
PATENT EXAMINER

K. Kim 3/9/06

FORM PTO-1449 SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	APPLICANT David F. SORRELLS et al.	
	FILING DATE August 4, 2000	GROUP 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
✓	AJ22	JP 5-327356	12/1993	JP	H03D	7/00	No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED
[illegible]	11/03/04

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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(PTO ASSISTANCE)

CORRESP.
HC

Application :	09/632856	**Examiner :**	Kim, K.	**GAU :**	2638
From:	AMW / (R)	**Location:**	IDC **FMF** FDC	**Date:**	2/24/06

2nd REQUEST

Tracking #: ______ Week Date: ______

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DOC CODE	DOC DATE	MISCELLANEOUS
☒ 1449	11-16-2005	☐ Continuing Data
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[RUSH] **MESSAGE:** Please initial or strike each entry on each page of the 11-16-2005 1449 document. Specifically, please see page 60 of 76.

Thank You,
AMW

[XRUSH] **RESPONSE:**

Page 60 of IDS has been signed and dated

INITIALS: K

NOTE: This form will be included as part of the official USPTO record, with the Response document coded as XRUSH.
REV 10/04

July 10, 2007

WRITER'S DIRECT NUMBER:
(202) 772-8675
INTERNET ADDRESS:
JHELVEY@SKGF.COM

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Art Unit 2611

Attn: Certificate of Correction Branch

Re: U.S. Utility Patent
Patent No. 7,110,444 B1; Issued: September 19, 2006
For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations**
Inventors: Sorrells *et al.*
Our Ref: 1744.0630003

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Request for Certificate of Correction Under 37 C.F.R. § 1.322;
2. Exhibit A (4 pages of Examiner-initialed PTO-1449 forms); and
3. Form PTO/SB/44 (5 pages).

The above listed documents are being electronically submitted through EFS-Web.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

JTH Helvey

Jeffrey T. Helvey
Attorney for Patentees
Registration No. 44,757

JTH/jeg
Enclosures

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent of: Sorrells *et al.* Patent. No.: 7,110,444 B1 Issued: September 19, 2006 For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations**	Confirmation No.: 2377 Art Unit: 2611 Examiner: Kim, Kevin Atty. Docket: 1744.0630003

Request for Certificate of Correction Under 37 C.F.R. § 1.322

Attn: Certificate of Correction Branch

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

It is hereby requested that a Certificate of Correction under 37 C.F.R. § 1.322 be issued for the above-captioned United States Patent. This Certificate of Correction is being requested due to mistakes which appear in the printed patent. These mistakes were made by the U.S. Patent and Trademark Office.

Specifically, the printed patent contains the following errors for which a Certificate of Correction is respectfully requested:

In Section (56), References Cited, a number of references that were cited and considered are missing. The specific references are those that were listed on pages 15-18 of the Information Disclosure Statement PTO-1449 form, filed December 15, 2004.

Copies of these Examiner-initialed pages are enclosed as Exhibit A for the convenience of the Examiner.

Remarks

The above-noted corrections do not involve such changes in the patent as would constitute new matter or would require reexamination.

A completed Form PTO/SB/44 accompanies this request, with the above-noted corrections printed thereon. Accordingly, a Certificate of Correction is believed proper and issuance thereof is respectfully requested.

The Commissioner is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Jeff Helvey

Jeffrey T. Helvey
Attorney for Patentees
Registration No. 44,757

Date: 7/10/07

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
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632947_1.DOC

Exhibit A

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	APPLICANT Sorrells et al.	
	FILING DATE August 4, 2000	GROUP 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA15	4,870,659	09/1989	Oishi *et al.*	375	82	
	AB15	4,871,987	10/1989	Kawase	332	100	
	AC15	4,885,587	12/1989	Wiegand *et al.*	42	14	
	AD15	4,885,756	12/1989	Fontanes *et al.*	375	82	
	AE15	4,888,557	12/1989	Puckette, IV *et al.*	329	341	
	AF15	4,890,302	12/1989	Muilwijk	375	80	
	AG15	4,893,316	01/1990	Janc *et al.*	375	44	
	AH15	4,893,341	01/1990	Gehring	381	7	
	AI15	4,894,766	01/1990	De Agro	363	159	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ15	JP 6-237276	08/1994	JP	H04L	27/20	No
	AK15	JP 8-23359	01/1996	JP	H04L	27/20	No
	AL15	JP 47-2314	02/1972	JP	—	—	Yes (Doc. AP53)
	AM15	JP 58-7903	01/1983	JP	H03C	1/02	Partial (Doc. AQ53)

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	15	Karasawa, Y. *et al.*, "A New Prediction Method for Tropospheric Scintillation on Earth-Space Paths," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. 36, No. 11, pp. 1608-1614 (November 1988).
	AO	15	Kirsten, J. and Fleming, J., "Undersampling reduces data-acquisition costs for select applications," *EDN*, Cahners Publishing, Vol. 35, No. 13, pp. 217-222, 224, 226-228 (June 21, 1990).
	AP	15	Lam, W.K. *et al.*, "Measurement of the Phase Noise Characteristics of an Unlocked Communications Channel Identifier," *Proceedings Of the 1993 IEEE International Frequency Control Symposium*, IEEE, pp. 283-288 (June 2-4, 1993).
	AQ	15	Lam, W.K. *et al.*, "Wideband sounding of 11.6 Ghz transhorizon channel," *Electronics Letters*, IEE, Vol. 30, No. 9, pp. 738-739 (April 28, 1994).
	AR	15	Larkin, K.G., "Efficient demodulator for bandpass sampled AM signals," *Electronics Letters*, IEE, Vol. 32, No. 2, pp. 101-102 (January 18, 1996).

EXAMINER	DATE CONSIDERED
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

:ODMA\MHODMA\SKGF_DC1;32458;1

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	APPLICANT Sorrells et al.	
	FILING DATE August 4, 2000	GROUP 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
K	AA16	4,896,152	01/1990	Tiemann	340	853	
	AB16	4,902,979	02/1990	Puckette, IV	329	343	
	AC16	4,908,579	03/1990	Tawfik *et al.*	328	167	
	AD16	4,910,752	03/1990	Yester, Jr. *et al.*	375	75	
	AE16	4,914,405	04/1990	Wells	331	25	
	AF16	4,920,510	04/1990	Senderowicz *et al.*	364	825	
	AG16	4,922,452	05/1990	Larsen *et al.*	365	45	
	AH16	4,931,921	06/1990	Anderson	363	163	
	AI16	4,944,025	07/1990	Gehring *et al.*	455	207	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ16	JP 58-133004	08/1983	JP	H03D	1/00	No
	AK16	JP 60-58705	04/1985	JP	H03D	7/00	No
	AL16	JP 4-123614	04/1992	JP	H03K	19/0175	No
	AM16	JP 4-127601	04/1992	JP	H03D	7/00	No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	16	Lau, W.H. *et al.*, "Analysis of the Time Variant Structure of Microwave Line-of-sight Multipath Phenomena," *IEEE Global Telecommunications Conference & Exhibition*, IEEE, pp. 1707-1711 (November 28 - December 1, 1988).
	AO	16	Lau, W.H. *et al.*, "Improved Prony Algorithm to Identify Multipath Components," *Electronics Letters*, IEE, Vol. 23, No. 20, pp. 1059-1060 (September 24, 1987).
	AP	16	Lesage, P. and Audoin, C., "Effect of Dead-Time on the Estimation of the Two-Sample Variance," *IEEE Transactions on Instrumentation and Measurement*, IEEE Instrumentation and Measurement Society, Vol. IM-28, No. 1, pp. 6-10 (March 1979).
	AQ	16	Liechti, C.A., "Performance of Dual-gate GaAs MESFET's as Gain-Controlled Low-Noise Amplifiers and High-Speed Modulators," *IEEE Transactions on Microwave Theory and Techniques*, IEEE Microwave Theory and Techniques Society, Vol. MTT-23, No. 6, pp. 461-469 (June 1975).
K	AR	16	Linnenbrink, T.E. *et al.*, "A One Gigasample Per Second Transient Recorder," *IEEE Transactions on Nuclear Science*, IEEE Nuclear and Plasma Sciences Society, Vol. NS-26, No. 4, pp. 4443-4449 (August 1979).

EXAMINER	DATE CONSIDERED
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:ODMA\MHODMA\SKGF_DC1;32466;1

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	APPLICANT Sorrells et al.	
	FILING DATE August 4, 2000	GROUP 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA17	4,955,079	09/1990	Connerney *et al.*	455	325	
	AB17	4,965,467	10/1990	Bilterijst	307	352	
	AC17	4,967,160	10/1990	Quievy *et al.*	328	16	
	AD17	4,970,703	11/1990	Hariharan *et al.*	367	138	
	AE17	4,982,353	01/1991	Jacob *et al.*	364	724.10	
	AF17	4,984,077	01/1991	Uchida	358	140	
	AG17	4,995,055	02/1991	Weinberger *et al.*	375	5	
	AH17	5,003,621	03/1991	Gailus	455	209	
	AI17	5,005,169	04/1991	Bronder *et al.*	370	76	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ17	JP 5-175730	07/1993	JP	H03D	1/00	No
	AK17	JP 5-175734	07/1993	JP	H03D	3/00	No
	AL17	JP 7-154344	06/1995	JP	H04B	14/06	No
	AM17	JP 7-307620	11/1995	JP	H03D	1/18	No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	17	Liou, M.L., "A Tutorial on Computer-Aided Analysis of Switched-Capacitor Circuits," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 987-1005 (August 1983).
	AO	17	Lo, P. *et al.*, "Coherent Automatic Gain Control," *IEE Colloquium on Phase Locked Techniques*, IEE, pp. 2/1-2/6 (March 26, 1980).
	AP	17	Lo, P. *et al.*, "Computation of Rain Induced Scintillations on Satellite Down-Links at Microwave Frequencies," *Third International Conference on Antennas and Propagation (ICAP 83)*, pp. 127-131 (April 12-15, 1983).
	AQ	17	Lo, P.S.L.O. *et al.*, "Observations of Amplitude Scintillations on a Low-Elevation Earth-Space Path," *Electronics Letters*, IEE, Vol. 20, No. 7, pp. 307-308 (March 29, 1984).
K	AR	17	Madani, K. and Aithison, C.S., "A 20 Ghz Microwave Sampler," *IEEE Transactions on Microwave Theory and Techniques*, IEEE Microwave Theory and Techniques Society, Vol. 40, No. 10, pp. 1960-1963 (October 1992).

EXAMINER	DATE CONSIDERED

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:ODMA\MHODMA\SKGF_DC1;32468;1

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	APPLICANT Sorrells *et al.*	
	FILING DATE August 4, 2000	GROUP 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
K	AA18	5,006,810	04/1991	Popescu	328	167	
	AB18	5,010,585	04/1991	Garcia	455	118	
	AC18	5,014,304	05/1991	Nicollini *et al.*	379	399	
	AD18	5,015,963	05/1991	Sutton	329	361	
	AE18	5,017,924	05/1991	Guiberteau *et al.*	342	195	
	AF18	5,020,149	05/1991	Hemmie	455	325	
	AG18	5,020,154	05/1991	Zierhut	455	608	
	AH18	5,052,050	09/1991	Collier *et al.*	455	296	
	AI18	5,065,409	11/1991	Hughes *et al.*	375	91	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ18	JP 55-66057	05/1980	JP	G06K	7/10	No
	AK18	JP 63-65587	03/1988	JP	G06K	7/10	No
	AL18	JP 63-153691	06/1988	JP	G06K	17/00	No
	AM18	EP 0 276 130 A2&A3	07/1988	EP	H03D	7/00	N/A

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	18	Marsland, R.A. *et al.*, "130 Ghz GaAs monolithic integrated circuit sampling head," *Appl. Phys. Lett.*, American Institute of Physics, Vol. 55, No. 6, pp. 592-594 (August 7, 1989).
	AO	18	Martin, K. and Sedra, A.S., "Switched-Capacitor Building Blocks for Adaptive Systems," *IEEE Transactions on Circuits and Systems*, IEEE Circuits and Systems Society, Vol. CAS-28, No. 6, pp. 576-584 (June 1981).
	AP	18	Marzano, F.S. and d'Auria, G., "Model-based Prediction of Amplitude Scintillation variance due to Clear-Air Tropospheric Turbulence on Earth-Satellite Microwave Links," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. 46, No. 10, pp. 1506-1518 (October 1998).
	AQ	18	Matricciani, E., "Prediction of fade durations due to rain in satellite communication systems," *Radio Science*, American Geophysical Union, Vol. 32, No. 3, pp. 935-941 (May-June 1997).
K	AR	18	McQueen, J.G., "The Monitoring of High-Speed Waveforms," *Electronic Engineering*, Morgan Brothers Limited, Vol. XXIV, No. 296, pp. 436-441 (October 1952).

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:ODMA\MHODMA\SKGF_DC1;32468;1

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO: 7,110,444 B1

DATED: September 19, 2006

INVENTORS: Sorrells *et al.*

It is certified that error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below.

Section (56)
Under "U.S. Patent Documents", please insert the following citations:

4,870,659	09/1989	Oishi et al.
4,871,987	10/1989	Kawase
4,885,587	12/1989	Wiegand et al.
4,885,756	12/1989	Fontanes et al.
4,888,557	12/1989	Puckette, IV et al.
4,890,302	12/1989	Muilwijk
4,893,316	01/1990	Janc et al.
4,893,341	01/1990	Gehring
4,894,766	01/1990	De Agro
4,896,152	01/1990	Tiemann
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4,908,579	03/1990	Tawfik et al.
4,910,752	03/1990	Yester, Jr. et al.
4,914,405	04/1990	Wells
4,920,510	04/1990	Senderowicz et al.
4,922,452	05/1990	Larsen et al.
4,931,921	06/1990	Anderson
4,944,025	07/1990	Gehring et al.
4,955,079	09/1990	Connerney et al.
4,965,467	10/1990	Bilterijst
4,967,160	10/1990	Quievy et al.
4,970,703	11/1990	Hariharan et al.
4,982,353	01/1991	Jacob et al.
4,984,077	01/1991	Uchida
4,995,055	02/1991	Weinberger et al.

MAILING ADDRESS OF SENDER (Please do not use customer number below):

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Atty. Dkt. No. 1744.0630003

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CERTIFICATE OF CORRECTION

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5,006,810	04/1991	Popescu
5,010,585	04/1991	Garcia
5,014,304	05/1991	Nicollini et al.
5,015,963	05/1991	Sutton
5,017,924	05/1991	Guiberteau et al.
5,020,149	05/1991	Hemmie
5,020,154	05/1991	Zierhut
5,052,050	09/1991	Collier et al.
5,065,409	11/1991	Hughes et al.

Under "Foreign Patent Documents", please insert the following citations:

JP 6-237276	08/1994
JP 8-23359	01/1996
JP 47-2314	02/1972
JP 58-7903	01/1983
JP 58-133004	08/1983
JP 60-58705	04/1985
JP 4-123614	04/1992
JP 4-127601	04/1992
JP 5-175730	07/1993
JP 5-175734	07/1993

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(Also Form PTO-1050)

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CERTIFICATE OF CORRECTION

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JP 63-153691	06/1988
EP 0 276 130 A2&A3	07/1988

Under "Other Publications", please insert the following citations:

Karasawa, Y. *et al.*, "A New Prediction Method for Tropospheric Scintillation on Earth-Space Paths," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. 36, No. 11, pp. 1608-1614 (November 1988).

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Lau, W.H. *et al.*, "Analysis of the Time Variant Structure of Microwave Line-of-sight Multipath Phenomena," *IEEE Global Telecommunications Conference & Exhibition*, IEEE, pp. 1707-1711 (November 28 - December 1, 1988).

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Linnenbrink, T.E. *et al.*, "A One Gigasample Per Second Transient Recorder," *IEEE Transactions on Nuclear Science*, IEEE Nuclear and Plasma Sciences Society, Vol. NS-26, No. 4, pp. 4443-4449 (August 1979).
Liou, M.L., "A Tutorial on Computer-Aided Analysis of Switched-Capacitor Circuits," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 987-1005 (August 1983).
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Lo, P. *et al.*, "Computation of Rain Induced Scintillations on Satellite Down-Links at Microwave Frequencies," *Third International Conference on Antennas and Propagation (ICAP 83)*, pp. 127-131 (April 12-15, 1983).
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Marzano, F.S. and d'Auria, G., "Model-based Prediction of Amplitude Scintillation variance due to Clear-Air Tropospheric Turbulence on Earth-Satellite Microwave Links," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. 46, No. 10, pp. 1506-1518 (October 1998).
Matricciani, E., "Prediction of fade durations due to rain in satellite communication systems," *Radio Science*, American Geophysical Union, Vol. 32, No. 3, pp. 935-941 (May-June 1997).
McQueen, J.G., "The Monitoring of High-Speed Waveforms," *Electronic Engineering*, Morgan Brothers Limited, Vol. XXIV, No. 296, pp. 436-441 (October 1952).

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1100 New York Avenue, NW
Washington DC 20005-3934
Atty. Dkt. No. 1744.0630003

Electronic Acknowledgement Receipt

EFS ID:	1954200
Application Number:	09632856
International Application Number:	
Confirmation Number:	2377
Title of Invention:	WIRELESS LOCAL AREA NETWORK (WLAN) USING UNIVERSAL FREQUENCY TRANSLATION TECHNOLOGY INCLUDING MULTI-PHASE EMBODIMENTS AND CIRCUIT IMPLEMENTATIONS
First Named Inventor/Applicant Name:	David F. Sorrells
Correspondence Address:	Sterne Kessler Goldstein & Fox P L L C - Suite 600 1100 New York Avenue N W - Washington DC 20005-3934 US (202)371-2540 -
Filer:	Jeffrey Thomas Helvey/Jason Geider
Filer Authorized By:	Jeffrey Thomas Helvey
Attorney Docket Number:	1744.0630003
Receipt Date:	10-JUL-2007
Filing Date:	04-AUG-2000
Time Stamp:	14:14:58
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Certificate of Correction	17440630003_rcc.pdf	575849 e283f74e90fd46d41007f9333037454fb0e054b6	no	13
Warnings:					
Information:					
		Total Files Size (in bytes):	575849		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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August 6, 2007

Sterne Kessler Goldstein & Fox P L L C
Suite 600 1100 New York Avenue N W
Washington DC 20005-3934

Patent No. : 7,110,444 B1
Inventor(s) : David F. Sorrells, et al.
Issued : September 19, 2006
For **WIRELESS LOCAL AREA NETWORK (WLAN) USING UNIVERSAL FREQUENCY TRANSLATION TECHNOLOGY INCLUDING MULTI-PHASE EMBODIMENTS AND CIRCUIT IMPLEMENTATIONS**
Doc. No. **1744.0630003**

To Whom It May Concern:

The Certificate of Correction issued on August 7, 2007 , issued in error, in that error(s) was made in identifying the patent number and/or keying text/corrections, i.e.:

On the second and third page of the issued cofc, in the heading, the page numbering is labeled incorrectly. The label should be displayed on second page as --Page 2 of 4-- and on third page as --Page 3 of 4--..

Therefore, a certificate of correction will be issued to correct (supersede) the Certificate of Correction containing error(s), made during preparation of the Certificate of Correction, as noted above.

No further response is required, from applicants (attorney). However, errors discovered by attorney, other than as noted and described above, should be noted on *a copy* of the Certificate of Correction that was issued in error, accompanied by a signed transmittal letter and submitted directed to this Branch.

Antonio Johnson
(703) 308-9390 ext. 111
For Cecelia Newman, Supervisor
Decisions & Certificates of Correction Branch
(703) 305-8309 / 703-308-9390 ext. 102
cbn

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,110,444 B1 Page 1 of 4
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This certificate supersedes certificate of correction issued August 7, 2007.

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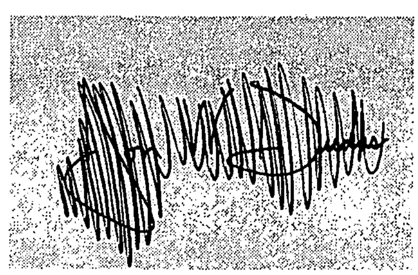
Seventh Day of August, 2007



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Madani, K. and Aithison, C.S., "A 20 Ghz Microwave Sampler," *IEEE Transactions on Microwave Theory and Techniques*, IEEE Microwave Theory and Techniques Society, Vol. 40, No. 10, pp. 1960-1963 (October 1992).

Marsland, R.A. *et al.*, "130 Ghz GaAs monolithic integrated circuit sampling head," *Appl. Phys. Lett.*, American Institute of Physics, Vol. 55, No. 6, pp. 592-594 (August 7, 1989).

Martin, K. and Sedra, A.S., "Switched-Capacitor Building Blocks for Adaptive Systems," *IEEE Transactions on Circuits and Systems*, IEEE Circuits and Systems Society, Vol. CAS-28, No. 6, pp. 576-584 (June 1981).

Marzano, F.S. and d'Auria, G., "Model-based Prediction of Amplitude Scintillation variance due to Clear-Air Tropospheric Turbulence on Earth-Satellite Microwave Links," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. 46, No. 10, pp. 1506-1518 (October 1998).

Matricciani, E., "Prediction of fade durations due to rain in satellite communication systems," *Radio Science*, American Geophysical Union, Vol. 32, No. 3, pp. 935-941 (May-June 1997).

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,110,444 B1 Page 4 of 4
APPLICATION NO. : 09/632856
DATED : September 19, 2006
INVENTOR(S) : Sorrells et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Section (56)
Under "Other Publications", please insert the following citations (cont'd):
McQueen, J.G., "The Monitoring of High-Speed Waveforms," *Electronic Engineering*, Morgan Brothers Limited, Vol. XXIV, No. 296, pp. 436-441 (October 1952).

This certificate supersedes Certificate of Correction issued August 7, 2007.

Signed and Sealed this

Twenty-eighth Day of August, 2007

Jon W. Dudas

JON W. DUDAS
Director of the United States Patent and Trademark Office

PTO/SB/80 (11-08)
Approved for use through 11/30/2011. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:

☑ Practitioners associated with the Customer Number: 22913

OR

☑ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:

☑ The address associated with Customer Number: 22913

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

Assignee Name and Address:

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	David F. Sorrells	Date	10-27-2011
Name	David F. Sorrells	Telephone	904-732-6100
Title	CTO		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: David F. Sorrells, et al.

Application No./Patent No.: 7110444 Filed/Issue Date: Sep. 19, 2006

Titled: Wireless Local Area Network (WLAN) using Universal Frequency Translation Technology including Multi-Phase Embodiments and Circuit Implementations

ParkerVision, Inc , a corporation
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.

states that it is:

1. [X] the assignee of the entire right, title, and interest in;

2. [ ] an assignee of less than the entire right, title, and interest in
(The extent (by percentage) of its ownership interest is ______ %); or

3. [ ] the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

A. [X] An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 011298, Frame 0868, or for which a copy therefore is attached.

OR

B. [ ] A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: ______ To: ______
The document was recorded in the United States Patent and Trademark Office at
Reel ______, Frame ______, or for which a copy thereof is attached.

2. From: ______ To: ______
The document was recorded in the United States Patent and Trademark Office at
Reel ______, Frame ______, or for which a copy thereof is attached.

3. From: ______ To: ______
The document was recorded in the United States Patent and Trademark Office at
Reel ______, Frame ______, or for which a copy thereof is attached.

[ ] Additional documents in the chain of title are listed on a supplemental sheet(s).

[X] As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Rick D. Nydegger (signature) 3/20/12
Signature Date

Rick D. Nydegger Attorney of Record
Printed or Typed Name Title

"FEE ADDRESS" INDICATION FORM

Address to:
Mail Stop M Correspondence
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

- OR -

Fax to:
571-273-6500

INSTRUCTIONS: The issue fee must have been paid for application(s) listed on this form. In addition, only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. **When to check the first box below**: If you have a Customer Number to represent the fee address. **When to check the second box below**: If you have no Customer Number representing the desired fee address, in which case a completed Request for Customer Number (PTO/SB/125) must be attached to this form. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:

☑ Customer Number: 22913

OR

☐ The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
7110444	

Completed by (check one):

☐ Applicant/Inventor

☑ Attorney or Agent of record 28651 (Reg. No.)

☐ Assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

☐ Assignee recorded at Reel ________ Frame ________

[signature]
Signature

Rick D. Nydegger
Typed or printed name

801-533-9800
Requester's telephone number

3/20/12
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more that one signature is required, see below*.

☐ *** Total of ____________ forms are submitted.**

Electronic Acknowledgement Receipt

EFS ID:	12346875
Application Number:	09632856
International Application Number:	
Confirmation Number:	2377
Title of Invention:	WIRELESS LOCAL AREA NETWORK (WLAN) USING UNIVERSAL FREQUENCY TRANSLATION TECHNOLOGY INCLUDING MULTI-PHASE EMBODIMENTS AND CIRCUIT IMPLEMENTATIONS
First Named Inventor/Applicant Name:	David F. Sorrells
Correspondence Address:	Sterne Kessler Goldstein & Fox P L L C - Suite 600 1100 New York Avenue N W - Washington DC 20005-3934 US (202)371-2600 -
Filer:	Rick D. Nydegger/Caitlyn Ellis
Filer Authorized By:	Rick D. Nydegger
Attorney Docket Number:	1744.0630003
Receipt Date:	20-MAR-2012
Filing Date:	04-AUG-2000
Time Stamp:	14:40:57
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		PV63-3_POA.pdf	402565 8865c337499908350c1de99866bfaef16444e56d	yes	3

Multipart Description/PDF files in .zip description

Document Description	Start	End
Power of Attorney	1	1
Assignee showing of ownership per 37 CFR 3.73(b).	2	2
Change of Address	3	3

Warnings:

Information:

Total Files Size (in bytes):	402565

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/632,856	08/04/2000	David F. Sorrells	

CONFIRMATION NO. 2377

POA ACCEPTANCE LETTER

OC000000053294055

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Salt Lake City, UT 84111

Date Mailed: 03/22/2012

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/20/2012.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/dtvernon/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/632,856	08/04/2000	David F. Sorrells	1744.0630003

CONFIRMATION NO. 2377

Sterne Kessler Goldstein & Fox P L L C
Suite 600 1100 New York Avenue N W
Washington, DC 20005-3934

POWER OF ATTORNEY NOTICE

OC000000053294034

Date Mailed: 03/22/2012

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/20/2012.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/dtvernon/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

$ 2634
BOX SEQ
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*Admitted only in Virginia
•Practice Limited to Federal Agencies

OIPE JC177
DEC 15 2004
PATENT & TRADEMARK OFFICE

December 15, 2004

WRITER'S DIRECT NUMBER:
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Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Art Unit 2634

Re: U.S. Utility Patent Application
Application No. 09/632,856; Filed: August 4, 2000
For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations**
Inventors: Sorrells *et al.*
Our Ref: 1744.0630003

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Resubmission of Information Disclosure Statements;

2. Copy of Information Disclosure Statement with cited references (as required by USPTO rules at the time of filing) filed on July 25, 2002;

3. Copy of Supplemental Information Disclosure Statement with cited references (as required by USPTO rules at the time of filing) filed on June 9, 2003;

4. Copy of Second Supplemental Information Disclosure Statement with cited references (as required by USPTO rules at the time of filing) filed on January 23, 2004;

5. Copy of Third Supplemental Information Disclosure Statement with cited references (as required by USPTO rules at the time of filing) filed on August 19, 2004;

6. Copy of Fourth Supplemental Information Disclosure Statement with cited references (as required by USPTO rules at the time of filing) filed on November 12, 2004;

7. A compact Disc labeled "Sterne1B" in PDF format;

8. A compact Disc labeled "Sterne2B" in PDF format;

9. A compact Disc labeled "Disc 3" in PDF format; and

10. Return postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Jeffrey T. Helvey
Attorney for Applicants
Registration No. 44,757

JTH/agj
344041_1.DOC

OIPE JC17
DEC 15 2004
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
Sorrells *et al.*
Application No.: 09/632,856
Filed: August 4, 2000
For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations**

Confirmation No.: 2377
Art Unit: 2634
Examiner: Kim, Kevin
Atty. Docket: 1744.0630003

Resubmission of Information Disclosure Statements

Attn: Mail Stop Issue Fee

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

During prosecution of the subject application, Applicants timely filed an Information Disclosure Statement and Supplemental Information Disclosure Statements on July 25, 2002, June 9, 2003, January 23, 2004, August 19, 2004 and November 12, 2004. However, at the time of Allowance, Applicants had not yet received back the Examiner-initialed PTO-1449 forms indicating that the references were considered. Applicants hereby resubmit the Information Disclosure Statement and Supplemental Information Disclosure Statements, as they were filed on July 25, 2002, June 9, 2003, January 23, 2004, August 19, 2004 and November 12, 2004, so that the Examiner can consider the references and return the initialed PTO-1449 forms. Copies of the references which were provided with the aforementioned filings (as required by applicable PTO rules at the time of filing) are hereby also re-submitted for the convenience of the Examiner.

It is respectfully requested that the Examiner initial and return a copy of the enclosed PTO-1449s, and indicate in the official file wrapper of this patent application that the documents listed have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

JTH Helvey

Jeffrey T. Helvey
Attorney for Applicants
Registration No. 44,757

Date: 12/18/04

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

JTH/JEG/agj
344027_1.DOC

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

OIPE JC177 DEC 15 2004 PATENT & TRADEMARK OFFICE

In re application of:

Sorrells *et al.*

Appl. No. 09/632,856

Filed: August 4, 2000

For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations**

Art Unit: 2634

Examiner: Ghayour, M.

Atty. Docket: 1744.0630003

Information Disclosure Statement

Commissioner for Patents
Washington, D.C. 20231

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98.

In addition to providing hard copies of the documents as required by applicable rules (see box 6 below), Applicants herewith provide two Compact Discs labeled "Sterne1B" and "Sterne2B" having stored thereon searchable electronic copies (in PDF format) of the documents listed on the PTO-1449. More specifically, the "Sterne1B" CD contains electronic copies of documents AA1-AR1, AA2-AR2, AA3-AR3, AA4-AR4, AA5-AR5, AA6-AR6, AA7-AR7, AA8-AR8, AA9-AR9, AA10-AR10, AA11-AR11, AA12-AR12, AA13-AL13, AN13-AR13, AA14-AI14, AN14-AR14, AA15-AI15, AN15-AR15, AA16-AI16, AN16-AR16, AA17-AI17, AN17-AR17, AA18-AI18, AN18-AR18, AA19-AI19, AN19-AR19, AA20-AI20, AN20-AR20, AA21-AI21, AN21-AR21, AA22-AI22, AN22-AR22, AA23-AI23, AN23-AR23, AA24-AI24, AN24-AR24, AA25-AI25, AN25-AR25,

AA26-AI26, AN26-AR26, AA27-AI27, AN27-AR27, AA28-AI28, AN28-AR28, AA29-AI29, AN29-AR29, AA30-AI30, AN30-AR30, AA31-AI31, AN31-AR31, AA32-AI32, AN32-AR32, AA33-AI33, AN33-AR33, AA34-AI34, AN34-AR34, AA35-AI35, AN35-AR35, AA36-AI36, AN36-AR36, AA37-AI37, AN37-AR37, AA38-AI38, AN38-AR38, AA39-AI39 and AN39-AR39, and the "Sterne2B" CD contains electronic copies of documents AA40-AI40, AA41-AI41, AA42-AI42, AA43-AI43, AA44-AI44, AA45-AI45, AA46-AB46, AM10, AJ11-AM11, AJ12-AM12, AJ13-AL13, AP50-AR50 and AN51-AP51. Documents AC46-AI46, AA47-AI47, AA48-AI48, AA49-AD49, AM13, AJ14-AM14, AJ15-AM15, AJ16-AM16, AJ17-AM17, AJ18-AM18, AJ19, AK19, AQ51, AR51, AN52-AR52, AN53-AR53, AN54-AR54, AN55-AR55 and AN56 have not yet been scanned. The file names on the CDs correspond to the identifiers on the PTO-1449. It is noted that the CDs are being provided in addition to hard copies of the documents for the convenience of the Examiner.

Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

Applicants provide the following comments regarding the documents:

Documents AD1, AL1, AO1, AC2, AF2, AG2, AI2, AC5, AG5, AB6, AF7, AI7, AB8, AF8, AG9, AK9, AO9, AO11, AA12, AE14, AN14, AB15, AE15, AH15, AO15, AF16, AD18, AG18, AB20, AC20, AQ20, AA22, AH22, AI23, AC24, AF26, AC30, AH31, AC32, AA33, AR33, AH34, AP35 and AO48 were included with Petitions to Make Special pleadings in co-owned related U.S. Patent Nos. 6,061,551, 6,061,555, 6,049,706 and 6,091,940.

Documents AM4, AH6, AL7, AJ9, AM9, AC17, AA20, AG20, AG21, AA24, AD24, AG24, AI31, AA32, AG34, AD36 and AQ37 were cited in searches performed at Applicants' request by the European Patent Office's Searching Authority in the above-referenced co-owned related patents.

Documents AA6, AD6, AO6, AE7, AE8, AA11, AE11, AH11, AI12, AB13, AD13, AH13, AC14, AG14, AE16, AB17, AF19, AD20, AN21, AG23, AH27, AI27, AI28, AH29, AG30, AD37, AR40, AO49 and AQ49 were suggested or identified by potential licensees.

Documents AH5, AH17, AD21, AB34, AE34, AB36, AI36 and AI38 were cited by the Examiner in the above-referenced co-owned related patents.

Documents AR21, AN22-AR22, AN23-23, AN24-AR24, AN25-AR25, AN26-AR26, AN27-AR27, AN28-AR28, AN29-AR29, AN30-AR30, AN31-AR31, AN32-AR32 and AN33-AP33 are press releases issued by assignee ParkerVision, Inc.

Documents AP6-AR6 and AN7-AP7 are copies of Declarations (including Exhibits) made by Messrs. Bultman, Cook, Holtz, Looke, Moses, Parker, and Sorrells, filed in the above-referenced co-owned related patents.

Documents AJ1, AL9, AJ10, AA19, AC25, AB30 and AF32 were cited in search reports in the corresponding foreign applications of the above-referenced co-owned related patents.

Documents AK9, AC17, AD36 and AD40 were listed in a search report issued by the International Searching Authority in PCT application serial number PCT/US00/21359, filed August 4, 2000, entitled "Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology," directed to related subject matter.

Documents AM10, AJ11, AK11 and AE40 were listed in a communication issued by the International Preliminary Examination Authority in PCT application serial number PCT/US00/01108, filed January 19, 2000, entitled "Frequency Translation and Embodiments Thereof Such as the Family Radio Service," directed to related subject matter.

Documents AI7, AJ9, AK9, AG20, AG21, AB30 and AI43 were listed in a written opinion issued by the International Preliminary Examination Authority in PCT application serial number PCT/US00/23923, filed October 18, 1999, entitled "Applications of Frequency Translation," directed to related subject matter.

Documents AA44, AL11, AM11 and AQ50 were listed in a communication issued by the International Searching Authority in PCT application serial number PCT/US00/09911, filed April 14, 2000, entitled "Method And System For Down-converting an Electromagnetic Signal, And Transforms For Same," directed to related subject matter.

Documents AB44 and AC44 were cited by an Examiner in co-pending U.S. Patent Application Serial No. 09/293,342, filed April 16, 1999, entitled "Method and System for Down-Converting Electromagnetic Signals Including Resonant Structures for Enhanced Energy Transfer," directed to related subject matter.

Documents AD44-AI44 and AA45-AD45 were cited by an Examiner in co-pending U.S. Patent Application Serial No. 09/261,129, filed March 3, 1999, entitled "Applications of Universal Frequency Translation," directed to related subject matter.

Documents AE45, AF45, AJ12 and AK12 were listed in a search report issued by the International Searching Authority in PCT application serial number PCT/US00/27555, filed October 6, 2000, entitled "DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," directed to related subject matter.

Documents AG45, AH45, AL12 and AM12 were listed in a search report issued by the International Searching Authority in PCT application serial number PCT/US00/34771, filed January 21, 2000, entitled "Phase Comparator Using Undersampling," directed to related subject matter.

Documents AI45, AJ13-AL13 and AB46 were listed in a search report issued by the International Searching Authority in PCT application serial number PCT/US00/27281, filed October 4, 2000, entitled "Frequency Converter and Method," directed to related subject matter.

Document AA46 was cited by an Examiner in co-pending U.S. Patent Application Serial No. 09/293,580, filed April 16, 1999, entitled "Method and System for Frequency Up-Conversion with a Variety of Transmitted Configurations," directed to related subject matter.

Document AC46 was cited by an Examiner in co-pending U.S. Patent Application Serial No. 09/670,831, filed September 28, 2000, entitled "Universal Frequency Translation, Embodiments Thereof, and a Web Site and Web Pages Directed to Same," directed to related subject matter.

Document AD46 was cited by an Examiner in co-pending U.S. Patent Application Serial No. 09/293,095, filed April 16, 1999, entitled "Method and System for Down-Converting an Electromagnetic Signal Having Optimized Switch Structures," directed to related subject matter.

Documents AD35, AE46-AI46 and AA47 were cited by an Examiner in co-pending U.S. Patent Application Serial No. 09/293,342, filed April 16, 1999, entitled "Method and System for Down-Converting Electromagnetic Signals Including Resonant Structures for Enhanced Energy Transfer," directed to related subject matter.

Documents AJ1, AK9-AM9, AG28, AB30, AA32, AN52 and AP55 were cited in an Examination Report in co-pending European Patent Application Serial No. 99954905.8, filed October 18, 1999, entitled "Integrated Frequency Translation and Selectivity with a Variety of Filter Embodiments," directed to related subject matter.

Documents AM13, AJ14, AK14 and AQ51 were cited in an Examination Report in co-pending Japanese Patent Application No. 2000-577,765, filed June 21, 2000, entitled "Method and System for Ensuring Reception of a Communications Signal," directed to related subject matter.

Documents AL14, AM14, AJ15 and AK15 were cited in an Examination Report in co-pending Japanese Patent Application No. 2000-577,761, filed June 20, 2000, entitled "Method and System for Frequency Up-conversion," directed to related subject matter.

Documents AL15, AM15, AJ16-AM16 and AJ17-AM17 were cited in an Examination Report in co-pending Japanese Patent Application No. 2000-577,764, filed June 21, 2000, entitled "Applications of Frequency Translation," directed to related subject matter.

Documents AJ18-AL18, AB47, AC47 and AE47-AG47 were cited by an Examiner in co-pending U.S. Patent Application Serial No. 09/489,675, filed January 24, 2000, entitled "Bar Code Scanner Using Universal Frequency Translation Technology for Up-Conversion and Down-Conversion," directed to related subject matter.

Documents AC24 and AD47 were cited by an Examiner in co-pending U.S. Patent Application Serial No. 09/376,509, filed August 18, 1999, entitled "Method and System for Ensuring Reception of a Communications Signal," directed to related subject matter.

Documents AH47, AI47 and AA48-AE48 are co-owned patents which are directed to related subject matter.

Documents AI43, AH47 and AH48 were cited by an Examiner in co-pending U.S. Patent Application Serial No. 09/293,283, filed April 16, 1999, entitled "Integrated Frequency Translation and Selectivity with a Variety of Filter Embodiments," directed to related subject matter.

Documents AA38 and AG48 were cited by an Examiner in co-pending U.S. Patent Application Serial No. 09/476,091, filed January 3, 2000, entitled "Image-Reject Down-Converter and Embodiments Thereof, Such as the Family Radio Service," directed to related subject matter.

Documents AK19 and AF48 were listed in a search report issued by the International Searching Authority in PCT application serial number PCT/US01/15111, filed October 5, 2001, entitled "Method and Apparatuses Relating to a Universal Platform Module and Enabled by Universal Frequency Translation Technology," directed to related subject matter.

Documents AI48 and AA49 were cited by an Examiner in co-pending U.S. Patent Application Serial No. 09/567,963, filed May 10, 2000, entitled "Frequency Synthesizer Using Universal Frequency Translation Technology," directed to related subject matter.

Document AB49 is a copy of co-pending U.S. Patent Application Serial No. 09/525,615, filed March 14, 2000, entitled "Method, System, and Apparatus for Balanced Frequency Up-Conversion of a Baseband Signal," directed to related subject matter. In the copy provided, the claims are shown as amended on June 6, 2001.

Document AC49 is a copy of co-pending U.S. Patent Application Serial No. 09/632,855, filed August 14, 2000, entitled "Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments," directed to related subject matter. In the copy provided, the claims are shown as amended on June 12, 2001.

Document AD49 is a copy of co-pending U.S. Patent Application Serial No. 09/632,857, filed August 14, 2000, entitled "Wireless Local Area Network (WLAN) Technology and Applications Including Techniques of Universal Frequency Translation," directed to related subject matter. In the copy provided, the claims are shown as amended on June 6, 2001.

It is noted that some of these documents could be classified in more than one of the above categories.

The other documents in the PTO-1449 do not fall within the above categories.

This statement should not be construed as a representation that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below.

☒ 1. This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits. No statement or fee is required.

☐ 2. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection or Notice of Allowance.

☐ a. I hereby state that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ c. Attached is our check no._____ in the amount of _____ in payment of the fee under 37 C.F.R. § 1.17(p).

☐ 3. This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. A separate Petition to the Group Director, requesting consideration of this Information Disclosure Statement, is concurrently submitted herewith, along with our Check No. ________ in the amount of $ _____ in payment of the fee under 37 C.F.R. § 1.17(i).

☐ a. I hereby state that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ 4. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.

☒ 5. Concise explanations of the relevance of the non-English language documents AJ1, AK1, AJ6, AK7, AJ8-AL8, AK11-AM11, AJ12, AM13, AJ14-AM14, AJ15-AM15, AJ16-AM16, AJ17-AM17, AJ18-AL18, AQ50 and AQ51 appear below:

Document AJ1 (DE 42 37 692 C1) appears to be a receiver for a digital radio signal. The corresponding U.S. Patent No. 5,493,721 is enclosed as document AG28 on the attached PTO-1449.

Document AK1 (EP 0 035 166 A1) appears to describe a digitized receiver. A copy of the English language abstract of document AK1 is enclosed as document AQ8 on the attached PTO-1449.

Document AJ6 (EP 0 785 635 A1) appears to describe a method and apparatus for frequency diversity transmission using a plurality of uncorrelated carriers. A copy of the English language abstract of document AJ6 is enclosed as document AP8 on the attached PTO-1449.

Document AK7 (FR 2 743 231 A1) is the corresponding French application of document AJ6 (EP 0 785 635 A1), which is described above.

Document AJ8 (JP 2-39632) appears to describe a transmitter for frequency diversity. A copy of the English language abstract of document AJ8 is enclosed as document AO8 on the attached PTO-1449.

Document AK8 (JP 2-131629) appears to describe a transmitter-receiver for frequency diversity. A copy of the English language abstract of document AK8 is enclosed as document AN8 on the attached PTO-1449.

Document AL8 (JP 2-276351) appears to describe an FSK demodulating circuit. A copy of the English language abstract of document AL8 is enclosed as document AR7 on the attached PTO-1449.

Document AK11 (FR 2245130) appears to describe a converter. A partial English language translation of document AK11 is enclosed as document AP50 on the attached PTO-1449.

Document AL11 (DE 3541031) appears to describe a method and device for demodulating high-frequency modulated signals. An English translation of document AL11 is enclosed as document AR50 on the attached PTO-1449.

Document AM11 (EP 0 732 803) appears to describe a procedure and device for demodulation by sampling. An English translation of document AM11 is enclosed as document AN51 on the attached PTO-1449.

Document AJ12 (DE 19735798) appears to describe a transceiver. An English translation of document AJ12 is enclosed as document AP51 on the attached PTO-1449.

Document AM13 (JP 56-114451) appears to describe a system for diversity radio transmission. The corresponding U.S. Patent No. 4,363,132 is enclosed as document AF8 on the attached PTO-1449.

Document AJ14 (JP 8-32556) appears to describe a data transmitter-receiver. A copy of the English language abstract of document AJ14 is enclosed as document AO52 on the attached PTO-1449.

Document AK14 (JP 8-139524) appears to describe a frequency converting circuit and radio communication device. A copy of the English language abstract of document AK14 is enclosed as document AP52 on the attached PTO-1449.

Document AL14 (JP 59-144249) appears to describe a pulse signal transmission system. A copy of the English language abstract of document AL14 is enclosed as document AQ52 on the attached PTO-1449.

Document AM14 (JP 63-54002) appears to describe a microwave burst signal generator which incorporates a FET frequency multiplier. A copy of the English language abstract of document AM14 is enclosed as document AR52 on the attached PTO-1449.

Document AJ15 (JP 6-237276) appears to describe a quadrature modulator. A copy of the English language abstract of document AJ15 is enclosed as document AN53 on the attached PTO-1449.

Document AK15 (JP 8-23359) appears to describe a digital quadrature modulation device. A copy of the English language abstract of document AK15 is enclosed as document AO53 on the attached PTO-1449.

Document AL15 (JP 47-2314) appears to describe a demodulator. An English language translation of document AL15 is enclosed as document AP53 on the attached PTO-1449.

Document AM15 (JP 58-7903) appears to describe a switched capacitor modulator. A partial English language translation of document AM15 is enclosed as document AQ53 on the attached PTO-1449.

Document AJ16 (JP 58-133004) appears to describe an amplitude detector. A copy of the English language abstract of document AJ16 is enclosed as document AR53 on the attached PTO-1449.

Document AK16 (JP 60-58705) appears to describe a frequency converting circuit. A copy of the English language abstract of document AK16 is enclosed as document AN54 on the attached PTO-1449.

Document AL16 (JP 4-123614) appears to describe a level converting circuit. A copy of the English language abstract of document AL16 is enclosed as document AO54 on the attached PTO-1449.

Document AM16 (JP 4-127601) appears to describe a frequency conversion circuit. A copy of the English language abstract of document AM16 is enclosed as document AP54 on the attached PTO-1449.

Document AJ17 (JP 5-175730) appears to describe a time division direct receiver. A copy of the English language abstract of document AJ17 is enclosed as document AQ54 on the attached PTO-1449.

Document AK17 (JP 5-175734) appears to describe an FM demodulator. A copy of the English language abstract of document AK17 is enclosed as document AR54 on the attached PTO-1449.

Document AL17 (JP 7-154344) appears to describe a receiver for receiving modulated carrier signals and an IQ mixer/demodulator using it's receiving constitution. A copy of the English language abstract of document AL17 is enclosed as document AN55 on the attached PTO-1449.

Document AM17 (JP 7-307620) appears to describe a bottom detection circuit. A copy of the English language abstract of document AM17 is enclosed as document AO55 on the attached PTO-1449.

Document AJ18 (JP 55-66057) appears to describe a bar-code detection circuit. A copy of the English language abstract of document AJ18 is enclosed as document AQ55 on the attached PTO-1449.

Document AK18 (JP 63-65587) appears to describe a wireless light pen device. A copy of the English language abstract of document AK18 is enclosed as document AR55 on the attached PTO-1449.

Document AL18 (JP 63-153691) appears to describe a data transfer for a semiconductor data carrier system. A copy of the English language abstract of document AL18 is enclosed as document AN56 on the attached PTO-1449.

Document AQ50 (Fest *et al.*) appears to discuss analog-digital converters. An English translation of document AQ50 is enclosed as document AO51 on the attached PTO-1449.

Document AQ51 (Miki *et al.*) appears to describe modulation systems. A partial English-language translation of document AQ51 is enclosed as document AR51 on the attached PTO-1449.

☒ 6. Copies of documents AM18, AJ19, AK19, AF48-AI48, AA49-AD49 and AP53 are enclosed. Copies of the remaining documents were submitted to the Patent Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application

No. 09/525,615, filed March 14, 2000, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

It is respectfully requested that the Examiner initial and return a copy of the enclosed PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

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July 25, 2002

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Commissioner for Patents
Washington, D.C. 20231

Art Unit: 2634

Re: U.S. Utility Patent Application
Appl. No. 09/632,856; Filed: August 4, 2000
For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations**
Inventors: Sorrells *et al.*
Our Ref: 1744.0630003/MQL/JTH

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Information Disclosure Statement;

2. A list of the cited documents on Forms PTO-1449 (56 pages);

3. A copy of the twelve (12) documents cited on Forms PTO-1449;

4. A compact Disc labeled "Sterne1B" in PDF format;

5. A compact Disc labeled "Sterne2B" in PDF format; and

6. Return postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

for Patrick E. Garrett 39,987

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

JTH/slw
Enclosures

SKGF_DC1:38454.1

		Due Date:	N/A
Applicants:	Sorrells *et al.*	**Art Unit:**	2634
		Examiner:	To be Assigned
Application No.:	09/632,856	**Docket:**	1744.0630003
Filed:	August 4, 2000	**Atty:**	MQL/JTH

For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations**

When receipt stamp is placed hereon, the USPTO acknowledges receipt of the following documents:

1. SKGF Cover Letter;
2. Information Disclosure Statement;
3. A list of the cited documents on Forms PTO-1449 (56 pages);
4. A copy of the twelve (12) documents cited on Forms PTO-1449;
5. A compact Disc labeled "Sterne1B" in PDF format;
6. A compact Disc labeled "Sterne2B" in PDF format; and
7. Return postcard.

Art Unit: 2634

<u>Please Date Stamp And Return To Our Courier</u>

SKGF_DC1:38434.1

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	APPLICANT Sorrells *et al.*	
	FILING DATE August 4, 2000	GROUP 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA1	2,057,613	10/1936	Gardner	250	8	
	AB1	2,241,078	05/1941	Vreeland	179	15	
	AC1	2,270,385	01/1942	Skillman	179	15	
	AD1	2,283,575	05/1942	Roberts	250	6	
	AE1	2,358,152	09/1944	Earp	179	171.5	
	AF1	2,410,350	10/1946	Labin *et al.*	179	15	
	AG1	2,451,430	10/1948	Barone	250	8	
	AH1	2,462,069	02/1949	Chatterjea *et al.*	250	17	
	AI1	2,462,181	02/1949	Grosselfinger	250	17	

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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ1	DE 42 37 692 C1	03/1994	DE	H04B	1/26	No
	AK1	EP 0 035 166 A1	09/1981	EP	H04B	1/26	No
	AL1	EP 0 193 899 B1	06/1990	EP	G01S	7/52	N/A
	AM1	EP 0 380 351 A2	08/1990	EP	H03H	17/04	N/A

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	1	Aghvami, H. *et al.*, "Land Mobile Satellites Using the Highly Elliptic Orbits- The UK T-SAT Mobile Payload," *Fourth International Conference on Satellite Systems for Mobile Communications and Navigation*, IEE, pp. 147-153 (October 17-19, 1988).
	AO	1	Akers, N.P. *et al.*, "RF Sampling Gates: a Brief Review," *IEE Proceedings*, IEE, Vol. 133, Part A, No. 1, pp. 45-49 (January 1986).
	AP	1	Al-Ahmad, H.A.M. *et al.*, "Doppler Frequency Correction for a Non-Geostationary Communications Satellite. Techniques for CERS and T-SAT," *Electronics Division Colloquium on Low Noise Oscillators and Synthesizers*, IEE, pp. 4/1-4/5 (January 23, 1986).
	AQ	1	Ali, I. *et al.*, "Doppler Characterization for LEO Satellites," *IEEE Transactions on Communications*, IEEE, Vol. 46, No. 3, pp. 309-313 (March 1998).
	AR	1	Allan, D.W., "Statistics of Atomic Frequency Standards," *Proceedings Of The IEEE Special Issue on Frequency Stability*, IEEE, pp. 221-230 (February 1966).

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	APPLICANT Sorrells *et al.*	
	FILING DATE August 4, 2000	GROUP 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA2	2,472,798	06/1949	Fredendall	178	44	
	AB2	2,497,859	02/1950	Boughtwood *et al.*	250	8	
	AC2	2,499,279	02/1950	Peterson	332	41	
	AD2	2,802,208	08/1957	Hobbs	343	176	
	AE2	2,985,875	05/1961	Grisdale *et al.*	343	100	
	AF2	3,023,309	02/1962	Foulkes	250	17	
	AG2	3,069,679	12/1962	Sweeney *et al.*	343	200	
	AH2	3,104,393	09/1963	Vogelman	343	200	
	AI2	3,114,106	12/1963	McManus	325	56	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ2	EP 0 380 351 A3	02/1991	EP	H03H	17/04	N/A
	AK2	EP 0 411 840 A2	02/1991	EP	G01R	33/36	N/A
	AL2	EP 0 411 840 A3	07/1991	EP	G01R	33/36	N/A
	AM2	EP 0 411 840 B1	10/1995	EP	G01R	33/36	N/A

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	2	Allstot, D.J. *et al.*, "MOS Switched Capacitor Ladder Filters," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-13, No. 6, pp. 806-814 (December 1978).
	AO	2	Allstot, D.J. and Black Jr. W.C., "Technological Design Considerations for Monolithic MOS Switched-Capacitor Filtering Systems," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 967-986 (August 1983).
	AP	2	Alouini, M. *et al.*, "Channel Characterization and Modeling for Ka-Band Very Small Aperture Terminals," *Proceedings Of the IEEE*, IEEE, Vol. 85, No. 6, pp. 981-997 (June 1997).
	AQ	2	Andreyev, G.A. and Ogarev, S.A., "Phase Distortions of Keyed Millimeter-Wave Signals in the Case of Propagation in a Turbulent Atmosphere," *Telecommunications and Radio Engineering*, Scripta Technica, Vol. 43, No. 12, pp. 87-90 (December 1988).
	AR	2	Antonetti, A. *et al.*, "Optoelectronic Sampling in the Picosecond Range," *Optics Communications*, North-Holland Publishing Company, Vol. 21, No. 2, pp. 211-214 (May 1977).

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	APPLICANT Sorrells *et al.*	
	FILING DATE August 4, 2000	GROUP 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA3	3,118,117	01/1964	King *et al.*	332	22	
	AB3	3,226,643	12/1965	McNair	325	40	
	AC3	3,258,694	06/1966	Shepherd	325	145	
	AD3	3,383,598	05/1968	Sanders	325	163	
	AE3	3,384,822	05/1968	Miyagi	325	30	
	AF3	3,454,718	07/1969	Perreault	178	66	
	AG3	3,523,291	08/1970	Pierret	340	347	
	AH3	3,548,342	12/1970	Maxey	332	9	
	AI3	3,555,428	01/1971	Perreault	325	320	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ3	EP 0 423 718 A2	04/1991	EP	H04N	7/01	N/A
	AK3	EP 0 423 718 A3	08/1992	EP	H04N	7/01	N/A
	AL3	EP 0 486 095 A1	05/1992	EP	H03D	3/00	N/A
	AM3	EP 0 486 095 B1	02/1997	EP	H03D	3/00	N/A

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	3	Austin, J. *et al.*, "Doppler Correction of the Telecommunication Payload Oscillators in the UK T-SAT," *18th European Microwave Conference*, Microwave Exhibitions and Publishers Ltd., pp. 851-857 (September 12 - 15, 1988).
	AO	3	Auston, D.H., "Picosecond optoelectronic switching and gating in silicon," *Applied Physics Letters*, American Institute of Physics, Vol. 26, No. 3, pp. 101-103 (February 1, 1975).
	AP	3	Baher, H., "Transfer Functions for Switched-Capacitor and Wave Digital Filters," *IEEE Transactions on Circuits and Systems*, IEEE Circuits and Systems Society, Vol. CAS-33, No. 11, pp. 1138-1142 (November 1986).
	AQ	3	Baines, R., "The DSP Bottleneck," *IEEE Communications Magazine*, IEEE Communications Society, pp. 46-54 (May 1995).
	AR	3	Banjo, O.P. and Vilar, E., "Binary Error Probabilities on Earth-Space Links Subject to Scintillation Fading," *Electronics Letters*, IEE, Vol. 21, No. 7, pp. 296-297 (March 28, 1985).

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	APPLICANT Sorrells *et al.*	
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA4	3,617,892	11/1971	Hawley *et al.*	325	145	
	AB4	3,621,402	11/1971	Gardner	328	37	
	AC4	3,623,160	11/1971	Giles *et al.*	340	347 DA	
	AD4	3,626,417	12/1971	Gilbert	343	203	
	AE4	3,629,696	12/1971	Bartelink	324	57 R	
	AF4	3,662,268	05/1972	Gans *et al.*	325	56	
	AG4	3,689,841	09/1972	Bello *et al.*	325	39	
	AH4	3,714,577	01/1973	Hayes	325	145	
	AI4	3,717,844	02/1973	Barret *et al.*	340	5 R	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ4	EP 0 512 748 A2	11/1992	EP	H04N	9/64	N/A
	AK4	EP 0 512 748 A3	07/1993	EP	H04N	9/64	N/A
	AL4	EP 0 512 748 B1	11/1998	EP	H04N	9/64	N/A
	AM4	EP 0 548 542 A1	06/1993	EP	H03B	19/14	N/A

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	AN	4	Banjo, O.P. and Vilar, E., "The Dependence of Slant Path Amplitude Scintillations on Various Meteorological Parameters," *Fifth International Conference on Antennas and Propagation (ICAP 87) Part 2: Propagation*, IEE, pp. 277-280 (March 30 - April 2, 1987).
	AO	4	Banjo, O.P. and Vilar, E. "Measurement and Modeling of Amplitude Scintillations on Low-Elevation Earth-Space Paths and Impact on Communication Systems," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. COM-34, No. 8, pp. 774-780 (August 1986).
	AP	4	Banjo, O.P. *et al.*, "Tropospheric Amplitude Spectra Due to Absorption and Scattering in Earth-Space Paths," *Fourth International Conference on Antennas and Propagation (ICAP 85)*, IEE, pp. 77-82 (April 16-19, 1985).
	AQ	4	Basili,P. *et al.*, "Case Study of Intense Scintillation Events on the OTS Path," *IEEE Transactions on Antennas and Propagation*, IEEE, Vol. 38, No. 1, pp. 107-113 (January 1990).
	AR	4	Basili, P. *et al.*, "Observation of High C^2 and Turbulent Path Length on OTS Space-Earth Link," *Electronics Letters*, IEE, Vol. 24, No. 17, pp. 1114-1116 (August 18, 1988).

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	AA5	3,735,048	05/1973	Tomsa *et al.*	179	15 BM	
	AB5	3,806,811	04/1974	Thompson	325	146	
	AC5	3,868,601	02/1975	MacAfee	332	45	
	AD5	3,949,300	04/1976	Sadler	325	31	
	AE5	3,967,202	06/1976	Batz	325	31	
	AF5	3,980,945	09/1976	Bickford	325	30	
	AG5	3,987,280	10/1976	Bauer	235	150.53	
	AH5	3,991,277	11/1976	Hirata	179	15 FD	
	AI5	4,003,002	01/1977	Snijders *et al.*	332	10	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ5	EP 0 632 288 A2	01/1995	EP	G01S	13/75	N/A
	AK5	EP 0 632 288 A3	07/1996	EP	G01S	13/75	N/A
	AL5	EP 0 696 854 A1	02/1996	EP	H04B	1/26	N/A
	AM5	EP 0 782 275 A2	07/1997	EP	H04B	7/02	N/A

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	AN	5	Blakey, J.R. *et al.*, "Measurement of Atmospheric Millimetre-Wave Phase Scintillations in an Absorption Region," *Electronics Letters*, IEE, Vol. 21, No. 11, pp. 486-487 (May 23, 1985).
	AO	5	Burgueño, A. *et al.*, "Influence of rain gauge integration time on the rain rate statistics used in microwave communications," *annales des tèlècommunications*, International Union of Radio Science, pp. 522-527 (September/October 1988).
	AP	5	Burgueño, A. *et al.*, "Long-Term Joint Statistical Analysis of Duration and Intensity of Rainfall Rate with Application to Microwave Communications," *Fifth International Conference on Antennas and Propagation (ICAP 87) Part 2: Propagation*, IEE, pp. 198-201 (March 30 - April 2, 1987).
	AQ	5	Burgueño, A. *et al.*, "Long Term Statistics of Precipitation Rate Return Periods in the Context of Microwave Communications," *Sixth International Conference on Antennas and Propagation (ICAP 89) Part 2: Propagation*, IEE, pp. 297-301 (April 4-7, 1989).
	AR	5	Burgueño, A. *et al.*, "Spectral Analysis of 49 Years of Rainfall Rate and Relation to Fade Dynamics," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. 38, No. 9, pp. 1359-1366 (September 1990).

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA6	4,013,966	03/1977	Campbell	325	363	
	AB6	4,019,140	04/1977	Swerdlow	322	65	
	AC6	4,035,732	07/1977	Lohrmann	325	446	
	AD6	4,047,121	09/1977	Campbell	331	76	
	AE6	4,066,841	01/1978	Young	178	66 R	
	AF6	4,066,919	01/1978	Huntington	307	353	
	AG6	4,081,748	03/1978	Batz	325	56	
	AH6	4,130,765	12/1978	Arakelian *et al.*	307	220 R	
	AI6	4,130,806	12/1978	Van Gerwen *et al.*	325	487	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ6	EP 0 785 635 A1	07/1997	EP	H04B	1/713	No
	AK6	EP 0 795 978 A2	09/1997	EP	H04L	5/06	N/A
	AL6	EP 0 837 565 A1	04/1998	EP	H04B	1/69	N/A
	AM6	EP 0 862 274 A1	09/1998	EP	H03M	1/06	N/A

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	AN	6	Catalan, C. and Vilar, E., "Approach for satellite slant path remote sensing," *Electronics Letters*, IEE, Vol. 34, No. 12, pp. 1238-1240 (June 11, 1998).
	AO	6	Chan, P. et al., "A Highly Linear 1-GHz CMOS Downconversion Mixer," *European Solid State Circuits Conference*, IEEE Communication Society, pp. 210-213 (September 22-24, 1993).
	AP	6	Copy of Declaration of Michael J. Bultman filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 2 pages.
	AQ	6	Copy of Declaration of Robert W. Cook filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 2 pages.
	AR	6	Copy of Declaration of Alex Holtz filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 3 pages.

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA7	4,142,155	02/1979	Adachi	325	47	
	AB7	4,170,764	10/1979	Salz *et al.*	332	17	
	AC7	4,204,171	05/1980	Sutphin, Jr.	328	167	
	AD7	4,210,872	07/1980	Gregorian	330	9	
	AE7	4,245,355	01/1981	Pascoe *et al.*	455	326	
	AF7	4,253,066	02/1981	Fisher *et al.*	329	50	
	AG7	4,253,069	02/1981	Nossek	330	107	
	AH7	4,308,614	12/1981	Fisher *et al.*	370	119	
	AI7	4,320,361	03/1982	Kikkert	332	16 R	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ7	EP 0 874 499 A2	10/1998	EP	H04L	25/06	N/A
	AK7	FR 2 743 231 A1	07/1997	FR	H04B	7/12	No
	AL7	GB 2 161 344 A	01/1986	GB	H04B	7/12	N/A
	AM7	GB 2 215 945 A	09/1989	GB	H04L	27/00	N/A

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	7	Copy of Declaration of Richard C. Looke filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 2 pages.
	AO	7	Copy of Declaration of Charley D. Moses, Jr. filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 2 pages.
	AP	7	Copy of Declaration of Jeffrey L. Parker and David F. Sorrells, with attachment Exhibit 1, filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 130 pages.
	AQ	7	Dewey, R.J. and Collier, C.J., "Multi-Mode Radio Receiver," *Electronics Division Colloquium on Digitally Implemented Radios*, IEE, pp. 3/1-3/5 (October 18, 1985).
	AR	7	DIALOG File 347 (JAPIO) English Language Patent Abstract for JP 2-276351, 1 page (November 13, 1990 - Date of publication of application).

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	AA8	4,320,536	03/1982	Dietrich	455	325	
	AB8	4,346,477	08/1982	Gordy	455	257	
	AC8	4,355,401	10/1982	Ikoma *et al.*	375	5	
	AD8	4,356,558	10/1982	Owen *et al.*	364	724	
	AE8	4,360,867	11/1982	Gonda	363	158	
	AF8	4,363,132	12/1982	Collin	455	52	
	AG8	4,365,217	12/1982	Berger *et al.*	333	165	
	AH8	4,370,572	01/1983	Cosand *et al.*	307	353	
	AI8	4,389,579	06/1983	Stein	307	353	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ8	JP 2-39632	02/1990	JP	H04B	7/12	No
	AK8	JP 2-131629	05/1990	JP	H04B	7/12	No
	AL8	JP 2-276351	11/1990	JP	H04L	27/22	No
	AM8	WO 80/01633 A1	08/1980	PCT	H04J	1/08	N/A

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	AN	8	DIALOG File 347 (JAPIO) English Language Patent Abstract for JP 2-131629, 1 page (May 21, 1990 - Date of publication of application).
	AO	8	DIALOG File 347 (JAPIO) English Language Patent Abstract for JP 2-39632, 1 page (February 8, 1990 - Date of publication of application).
	AP	8	DIALOG File 348 (European Patents) English Language Patent Abstract for EP 0 785 635 A1, 3 pages (December 26, 1996 - Date of publication of application).
	AQ	8	DIALOG File 348 (European Patents) English Language Patent Abstract for EP 35166 A1, 2 pages (February 18, 1981 - Date of publication of application).
	AR	8	"DSO takes sampling rate to 1 Ghz," *Electronic Engineering*, Morgan Grampian Publishers, Vol. 59, No. 723, pp. 77 and 79 (March 1987).

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA9	4,392,255	07/1983	Del Giudice	455	328	
	AB9	4,430,629	02/1984	Betzl *et al.*	333	165	
	AC9	4,446,438	05/1984	Chang *et al.*	328	127	
	AD9	4,456,990	06/1984	Fisher *et al.*	370	119	
	AE9	4,472,785	09/1984	Kasuga	364	718	
	AF9	4,479,226	10/1984	Prabhu *et al.*	375	1	
	AG9	4,481,490	11/1984	Huntley	332	41	
	AH9	4,481,642	11/1984	Hanson	375	9	
	AI9	4,485,488	11/1984	Houdart	455	327	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ9	WO 94/05087 A1	03/1994	PCT	H03M	1/00	N/A
	AK9	WO 96/02977 A1	02/1996	PCT	H04B	1/26	N/A
	AL9	WO 96/08078 A1	03/1996	PCT	H03D	3/00	N/A
	AM9	WO 96/39750 A1	12/1996	PCT	H04B	1/26	N/A

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	AN	9	Erdi, G. and Henneuse, P.R., "A Precision FET-Less Sample-and-Hold with High Charge-to-Droop Current Ratio," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-13, No. 6, pp. 864-873 (December 1978).
	AO	9	Faulkner, N.D. and Vilar, E., "Subharmonic Sampling for the Measurement of Short Term Stability of Microwave Oscillators," *IEEE Transactions on Instrumentation and Measurement*, IEEE, Vol. IM-32, No. 1, pp. 208-213 (March 1983).
	AP	9	Faulkner, N.D. *et al.*, "Sub-Harmonic Sampling for the Accurate Measurement of Frequency Stability of Microwave Oscillators," *CPEM 82 Digest: Conference on Precision Electromagnetic Measurements*, IEEE, pp. M-10 and M-11 (1982).
	AQ	9	Faulkner, N.D. and Vilar, E., "Time Domain Analysis of Frequency Stability Using Non-Zero Dead-Time Counter Techniques," *CPEM 84 Digest Conference on Precision Electromagnetic Measurements*, IEEE, pp. 81-82 (1984).
	AR	9	Filip, M. and Vilar, E., "Optimum Utilization of the Channel Capacity of a Satellite Link in the Presence of Amplitude Scintillations and Rain Attenuation," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. 38, No. 11, pp. 1958-1965 (November 1990).

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	AA10	4,504,803	03/1985	Lee *et al.*	332	31 R	
	AB10	4,517,519	05/1985	Mukaiyama	329	126	
	AC10	4,517,520	05/1985	Ogawa	329	145	
	AD10	4,518,935	05/1985	van Roermund	333	173	
	AE10	4,521,892	06/1985	Vance *et al.*	375	88	
	AF10	4,563,773	07/1986	Dixon, Jr. *et al.*	455	327	
	AG10	4,577,157	03/1986	Reed	329	50	
	AH10	4,583,239	04/1986	Vance	375	94	
	AI10	4,591,736	05/1986	Hirao *et al.*	307	267	

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	AK10	WO 98/00953 A1	01/1998	PCT	H04L	27/26	N/A
	AL10	WO 98/24201 A1	06/1998	PCT	H04H	1/00	N/A
	AM10	EP 0 099 265 A1	01/1984	EP	H03D	3/04	N/A

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	AN	10	Fukahori, K., "A CMOS Narrow-Band Signaling Filter with Q Reduction," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-19, No. 6, pp. 926-932 (December 1984).
	AO	10	Fukuchi, H. and Otsu, Y., "Available time statistics of rain attenuation on earth-space path," *IEE Proceedings-H: Microwaves, Antennas and Propagation*, IEE, Vol. 135, Pt. H, No. 6, pp. 387-390 (December 1988).
	AP	10	Gibbins, C.J. and Chadha, R., "Millimetre-wave propagation through hydrocarbon flame," *IEE Proceedings*, IEE, Vol. 134, Pt. H, No.2 , pp. 169-173 (April 1987).
	AQ	10	Gilchrist, B. *et al.*, "Sampling hikes performance of frequency synthesizers," *Microwaves & RF*, Hayden Publishing, Vol. 23, No. 1, pp. 93-94 and 110 (January 1984).
	AR	10	Gossard, E.E., "Clear weather meteorological effects on propagation at frequencies above 1 Ghz," *Radio Science*, American Geophysical Union, Vol. 16, No. 5, pp. 589-608 (September - October 1981).

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	AA11	4,602,220	07/1986	Kurihara	331	19	
	AB11	4,603,300	07/1986	Welles, II *et al.*	329	50	
	AC11	4,612,464	09/1986	Ishikawa *et al.*	307	496	
	AD11	4,612,518	09/1986	Gans *et al.*	332	21	
	AE11	4,616,191	10/1986	Galani *et al.*	331	4	
	AF11	4,621,217	11/1986	Saxe *et al.*	315	1	
	AG11	4,628,517	12/1986	Schwarz *et al.*	375	40	
	AH11	4,634,998	01/1987	Crawford	331	1 A	
	AI11	4,648,021	03/1987	Alberkrack	363	157	

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	AJ11	EP 0 560 228 A1	09/1993	EP	H03D	7/12	N/A
	AK11	FR 2 245 130	04/1975	FR	H03K	5/13	Yes (See AP50)
	AL11	DE 35 41 031 A1	05/1986	DE	H03D	3/00	Yes (See AR50)
	AM11	EP 0 732 803 A1	09/1996	EP	H03D	3/00	Yes (See AN51)

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	AN	11	Gregorian, R. *et al.*, "Switched-Capacitor Circuit Design," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 941-966 (August 1983).
	AO	11	Groshong *et al.*, "Undersampling Techniques Simplify Digital Radio," *Electronic Design*, Penton Publishing, pp. 67-68, 70, 73-75 and 78 (May 23, 1991).
	AP	11	Grove, W.M., "Sampling for Oscilloscopes and Other RF Systems: Dc through X-Band," *IEEE Transactions on Microwave Theory and Techniques*, IEEE, pp. 629-635 (December 1966).
	AQ	11	Haddon, J. *et al.*, "Measurement of Microwave Scintillations on a Satellite Down-Link at X-Band," *Antennas and Propagation*, IEE, pp. 113-117 (1981).
	AR	11	Haddon, J. and Vilar, E., "Scattering Induced Microwave Scintillations from Clear Air and Rain on Earth Space Paths and the Influence of Antenna Aperture," *IEEE Transactions on Antennas and Propagation*, IEEE, Vol. AP-34, No. 5, pp. 646-657 (May 1986).

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	AA12	4,651,034	03/1987	Sato	307	556	
	AB12	4,675,882	06/1987	Lillie *et al.*	375	80	
	AC12	4,688,253	08/1987	Gumm	381	7	
	AD12	4,716,376	12/1987	Daudelin	329	107	
	AE12	4,716,388	12/1987	Jacobs	333	173	
	AF12	4,718,113	01/1988	Rother *et al.*	455	209	
	AG12	4,726,041	02/1988	Prohaska *et al.*	375	91	
	AH12	4,733,403	03/1988	Simone	375	103	
	AI12	4,734,591	03/1988	Ichitsubo	307	219.1	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ12	DE 197 35 798 C1	07/1998	DE	H04L	27/00	Yes (See AP51)
	AK12	WO 98/40968 A2&A3	09/1998	PCT	H03L	7/08	N/A
	AL12	EP 0 529 836 A1	03/1993	EP	H03L	7/089	N/A
	AM12	EP 0 795 955 A2&A3	09/1997	EP	H03D	13/00	N/A

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	AN	12	Hafdallah, H. *et al.*, "2-4 Ghz MESFET Sampler," *Electronics Letters*, IEE, Vol. 24, No. 3, pp. 151-153 (February 4, 1988).
	AO	12	Herben, M.H.A.J., "Amplitude and Phase Scintillation Measurements on 8-2 km Line-Of-Sight Path at 30 Ghz," *Electronics Letters*, IEE, Vol. 18, No. 7, pp. 287-289 (April 1, 1982).
	AP	12	Hewitt, A. *et al.*, "An 18 Ghz Wideband LOS Multipath Experiment," *International Conference on Measurements for Telecommunication Transmission Systems - MTTS 85*, IEE, pp. 112-116 (November 27-28, 1985)
	AQ	12	Hewitt, A. *et al.*, "An Autoregressive Approach to the Identification of Multipath Ray Parameters from Field Measurements," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. 37, No. 11, pp. 1136-1143 (November 1989).
	AR	12	Hewitt, A. and Vilar, E., "Selective fading on LOS Microwave Links: Classical and Spread-Spectrum Measurement Techniques," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. 36, No. 7, pp. 789-796 (July 1988).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA13	4,737,969	04/1988	Steel *et al.*	375	67	
	AB13	4,743,858	05/1988	Everard	330	10	
	AC13	4,745,463	05/1988	Lu	358	23	
	AD13	4,751,468	06/1988	Agoston	328	133	
	AE13	4,757,538	07/1988	Zink	381	7	
	AF13	4,768,187	08/1988	Marshall	370	69.1	
	AG13	4,769,612	09/1988	Tamakoshi *et al.*	328	167	
	AH13	4,785,463	11/1988	Janc *et al.*	375	1	
	AI13	4,791,584	12/1988	Greivenkamp, Jr.	364	525	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ13	EP 0 817 369 A2&A3	01/1998	EP	H03D	7/00	N/A
	AK13	WO 91/18445 A1	11/1991	PCT	H03D	7/18	N/A
	AL13	WO 99/23755 A1	05/1999	PCT	H03D	7/16	N/A
	AM13	JP 56-114451	09/1981	JP	H04B	7/02	No

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	AN	13	Hospitalier, E., "Instruments for Recording and Observing Rapidly Varying Phenomena," *Science Abstracts*, IEE, Vol. VII, pp. 22-23 (1904).
	AO	13	Howard, I.M. and Swansson, N.S., "Demodulating High Frequency Resonance Signals for Bearing Fault Detection," *The Institution of Engineers Australia Vibration and Noise Conference*, Institution of Engineers, Australia, pp. 115-121 (September 18-20, 1990).
	AP	13	Hu, X., *A Switched-Current Sample-and-Hold Amplifier for FM Demodulation*, Thesis for Master of Applied Science, Dept. of Electrical and Computer Engineering, University of Toronto, UMI Dissertation Services, pp. 1-64 (1995).
	AQ	13	Hung, H-L. A. *et al.*, "Characterization of Microwave Integrated Circuits Using An Optical Phase-Locking and Sampling System," *IEEE MTT-S Digest*, IEEE, pp. 507-510 (1991).
	AR	13	Hurst, P.J., "Shifting the Frequency Response of Switched-Capacitor Filters by Nonuniform Sampling," *IEEE Transactions on Circuits and Systems*, IEEE Circuits and Systems Society, Vol. 38, No. 1, pp. 12-19 (January 1991).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA14	4,801,823	01/1989	Yokoyama	307	353	
	AB14	4,806,790	02/1989	Sone	307	353	
	AC14	4,810,904	03/1989	Crawford	307	353	
	AD14	4,810,976	03/1989	Cowley *et al.*	331	117 R	
	AE14	4,811,362	03/1989	Yester, Jr. *et al.*	375	75	
	AF14	4,819,252	04/1989	Christopher	375	122	
	AG14	4,833,445	05/1989	Buchele	341	118	
	AH14	4,862,121	08/1989	Hochschild *et al.*	333	173	
	AI14	4,868,654	09/1989	Juri *et al.*	358	133	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ14	JP 8-32556	02/1996	JP	H04L	1/04	No
	AK14	JP 8-139524	05/1996	JP	H03D	7/00	No
	AL14	JP 59-144249	08/1984	JP	H04L	27/00	No
	AM14	JP 63-54002	03/1988	JP	H03B	19/114	No

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	AN	14	Itakura, T., "Effects of the sampling pulse width on the frequency characteristics of a sample-and-hold circuit," *IEE Proceedings Circuits, Devices and Systems,* IEE, Vol. 141, No. 4, pp. 328-336 (August 1994).
	AO	14	Janssen, J.M.L., "An Experimental 'Stroboscopic' Oscilloscope for Frequencies up to about 50 Mc/s: I. Fundamentals," *Philips Technical Review,* Philips Research Laboratories, Vol. 12, No. 2, pp. 52-59 (August 1950).
	AP	14	Janssen, J.M.L. and Michels, A.J., "An Experimental 'Stroboscopic' Oscilloscope for Frequencies up to about 50 Mc/s: II. Electrical Build-Up," *Philips Technical Review*, Philips Research Laboratories, Vol. 12, No. 3, pp. 73-82 (September 1950).
	AQ	14	Jondral, V.F. *et al.*, "Doppler Profiles for Communication Satellites," *Frequenz*, Herausberger, pp. 111-116 (May-June 1996).
	AR	14	Kaleh, G.K., "A Frequency Diversity Spread Spectrum System for Communication in the Presence of In-band Interference," *1995 IEEE Globecom*, IEEE Communications Society, pp. 66-70 (1995).

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA15	4,870,659	09/1989	Oishi *et al.*	375	82	
	AB15	4,871,987	10/1989	Kawase	332	100	
	AC15	4,885,587	12/1989	Wiegand *et al.*	42	14	
	AD15	4,885,756	12/1989	Fontanes *et al.*	375	82	
	AE15	4,888,557	12/1989	Puckette, IV *et al.*	329	341	
	AF15	4,890,302	12/1989	Muilwijk	375	80	
	AG15	4,893,316	01/1990	Janc *et al.*	375	44	
	AH15	4,893,341	01/1990	Gehring	381	7	
	AI15	4,894,766	01/1990	De Agro	363	159	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ15	JP 6-237276	08/1994	JP	H04L	27/20	No
	AK15	JP 8-23359	01/1996	JP	H04L	27/20	No
	AL15	JP 47-2314	02/1972	JP	---	---	Yes (Doc. AP53)
	AM15	JP 58-7903	01/1983	JP	H03C	1/02	Partial (Doc. AQ53)

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	AN	15	Karasawa, Y. *et al.*, "A New Prediction Method for Tropospheric Scintillation on Earth-Space Paths," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. 36, No. 11, pp. 1608-1614 (November 1988).
	AO	15	Kirsten, J. and Fleming, J., "Undersampling reduces data-acquisition costs for select applications," *EDN*, Cahners Publishing, Vol. 35, No. 13, pp. 217-222, 224, 226-228 (June 21, 1990).
	AP	15	Lam, W.K. *et al.*, "Measurement of the Phase Noise Characteristics of an Unlocked Communications Channel Identifier," *Proceedings Of the 1993 IEEE International Frequency Control Symposium*, IEEE, pp. 283-288 (June 2-4, 1993).
	AQ	15	Lam, W.K. *et al.*, "Wideband sounding of 11.6 Ghz transhorizon channel," *Electronics Letters*, IEE, Vol. 30, No. 9, pp. 738-739 (April 28, 1994).
	AR	15	Larkin, K.G., "Efficient demodulator for bandpass sampled AM signals," *Electronics Letters*, IEE, Vol. 32, No. 2, pp. 101-102 (January 18, 1996).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA16	4,896,152	01/1990	Tiemann	340	853	
	AB16	4,902,979	02/1990	Puckette, IV	329	343	
	AC16	4,908,579	03/1990	Tawfik *et al.*	328	167	
	AD16	4,910,752	03/1990	Yester, Jr. *et al.*	375	75	
	AE16	4,914,405	04/1990	Wells	331	25	
	AF16	4,920,510	04/1990	Senderowicz *et al.*	364	825	
	AG16	4,922,452	05/1990	Larsen *et al.*	365	45	
	AH16	4,931,921	06/1990	Anderson	363	163	
	AI16	4,944,025	07/1990	Gehring *et al.*	455	207	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ16	JP 58-133004	08/1983	JP	H03D	1/00	No
	AK16	JP 60-58705	04/1985	JP	H03D	7/00	No
	AL16	JP 4-123614	04/1992	JP	H03K	19/0175	No
	AM16	JP 4-127601	04/1992	JP	H03D	7/00	No

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	AN	16	Lau, W.H. *et al.*, "Analysis of the Time Variant Structure of Microwave Line-of-sight Multipath Phenomena," *IEEE Global Telecommunications Conference & Exhibition*, IEEE, pp. 1707-1711 (November 28 - December 1, 1988).
	AO	16	Lau, W.H. *et al.*, "Improved Prony Algorithm to Identify Multipath Components," *Electronics Letters*, IEE, Vol. 23, No. 20, pp. 1059-1060 (September 24, 1987).
	AP	16	Lesage, P. and Audoin, C., "Effect of Dead-Time on the Estimation of the Two-Sample Variance," *IEEE Transactions on Instrumentation and Measurement*, IEEE Instrumentation and Measurement Society, Vol. IM-28, No. 1, pp. 6-10 (March 1979).
	AQ	16	Liechti, C.A., "Performance of Dual-gate GaAs MESFET's as Gain-Controlled Low-Noise Amplifiers and High-Speed Modulators," *IEEE Transactions on Microwave Theory and Techniques*, IEEE Microwave Theory and Techniques Society, Vol. MTT-23, No. 6, pp. 461-469 (June 1975).
	AR	16	Linnenbrink, T.E. *et al.*, "A One Gigasample Per Second Transient Recorder," *IEEE Transactions on Nuclear Science*, IEEE Nuclear and Plasma Sciences Society, Vol. NS-26, No. 4, pp. 4443-4449 (August 1979).

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U.S. PATENT DOCUMENTS

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	AA17	4,955,079	09/1990	Connerney *et al.*	455	325	
	AB17	4,965,467	10/1990	Bilterijst	307	352	
	AC17	4,967,160	10/1990	Quievy *et al.*	328	16	
	AD17	4,970,703	11/1990	Hariharan *et al.*	367	138	
	AE17	4,982,353	01/1991	Jacob *et al.*	364	724.10	
	AF17	4,984,077	01/1991	Uchida	358	140	
	AG17	4,995,055	02/1991	Weinberger *et al.*	375	5	
	AH17	5,003,621	03/1991	Gailus	455	209	
	AI17	5,005,169	04/1991	Bronder *et al.*	370	76	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ17	JP 5-175730	07/1993	JP	H03D	1/00	No
	AK17	JP 5-175734	07/1993	JP	H03D	3/00	No
	AL17	JP 7-154344	06/1995	JP	H04B	14/06	No
	AM17	JP 7-307620	11/1995	JP	H03D	1/18	No

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	AN	17	Liou, M.L., "A Tutorial on Computer-Aided Analysis of Switched-Capacitor Circuits," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 987-1005 (August 1983).
	AO	17	Lo, P. *et al.*, "Coherent Automatic Gain Control," *IEE Colloquium on Phase Locked Techniques*, IEE, pp. 2/1-2/6 (March 26, 1980).
	AP	17	Lo, P. *et al.*, "Computation of Rain Induced Scintillations on Satellite Down-Links at Microwave Frequencies," *Third International Conference on Antennas and Propagation (ICAP 83)*, pp. 127-131 (April 12-15, 1983).
	AQ	17	Lo, P.S.L.O. *et al.*, "Observations of Amplitude Scintillations on a Low-Elevation Earth-Space Path," *Electronics Letters*, IEE, Vol. 20, No. 7, pp. 307-308 (March 29, 1984).
	AR	17	Madani, K. and Aithison, C.S., "A 20 Ghz Microwave Sampler," *IEEE Transactions on Microwave Theory and Techniques*, IEEE Microwave Theory and Techniques Society, Vol. 40, No. 10, pp. 1960-1963 (October 1992).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA18	5,006,810	04/1991	Popescu	328	167	
	AB18	5,010,585	04/1991	Garcia	455	118	
	AC18	5,014,304	05/1991	Nicollini *et al.*	379	399	
	AD18	5,015,963	05/1991	Sutton	329	361	
	AE18	5,017,924	05/1991	Guiberteau *et al.*	342	195	
	AF18	5,020,149	05/1991	Hemmie	455	325	
	AG18	5,020,154	05/1991	Zierhut	455	608	
	AH18	5,052,050	09/1991	Collier *et al.*	455	296	
	AI18	5,065,409	11/1991	Hughes *et al.*	375	91	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ18	JP 55-66057	05/1980	JP	G06K	7/10	No
	AK18	JP 63-65587	03/1988	JP	G06K	7/10	No
	AL18	JP 63-153691	06/1988	JP	G06K	17/00	No
	AM18	EP 0 276 130 A2&A3	07/1988	EP	H03D	7/00	N/A

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	AN	18	Marsland, R.A. *et al.*, "130 Ghz GaAs monolithic integrated circuit sampling head," *Appl. Phys. Lett.*, American Institute of Physics, Vol. 55, No. 6, pp. 592-594 (August 7, 1989).
	AO	18	Martin, K. and Sedra, A.S., "Switched-Capacitor Building Blocks for Adaptive Systems," *IEEE Transactions on Circuits and Systems*, IEEE Circuits and Systems Society, Vol. CAS-28, No. 6, pp. 576-584 (June 1981).
	AP	18	Marzano, F.S. and d'Auria, G., "Model-based Prediction of Amplitude Scintillation variance due to Clear-Air Tropospheric Turbulence on Earth-Satellite Microwave Links," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. 46, No. 10, pp. 1506-1518 (October 1998).
	AQ	18	Matricciani, E., "Prediction of fade durations due to rain in satellite communication systems," *Radio Science*, American Geophysical Union, Vol. 32, No. 3, pp. 935-941 (May-June 1997).
	AR	18	McQueen, J.G., "The Monitoring of High-Speed Waveforms," *Electronic Engineering*, Morgan Brothers Limited, Vol. XXIV, No. 296, pp. 436-441 (October 1952).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA19	5,083,050	01/1992	Vasile	307	529	
	AB19	5,091,921	02/1992	Minami	375	88	
	AC19	5,095,533	03/1992	Loper *et al.*	455	245	
	AD19	5,095,536	03/1992	Loper	455	324	
	AE19	5,111,152	05/1992	Makino	329	300	
	AF19	5,113,094	05/1992	Grace *et al.*	307	529	
	AG19	5,113,129	05/1992	Hughes	323	316	
	AH19	5,122,765	06/1992	Pataut	332	105	
	AI19	5,124,592	06/1992	Hagino	307	520	

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	AJ19	WO 95/01006 A1	01/1995	PCT	H03M	1/66	N/A
	AK19	WO 97/08839 A2&A3	03/1997	PCT	H04B	1/04	N/A
	AL19						Yes No
	AM19						Yes No

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	AN	19	Merkelo, J. and Hall, R.D., "Broad-Band Thin-Film Signal Sampler," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-7, No. 1, pp. 50-54 (February 1972).
	AO	19	Merlo, U. *et al.*, "Amplitude Scintillation Cycles in a Sirio Satellite-Earth Link," *Electronics Letters*, IEE, Vol. 21, No. 23, pp. 1094-1096 (November 7, 1985).
	AP	19	Morris, D., "Radio-holographic reflector measurement of the 30-m millimeter radio telescope at 22 Ghz with a cosmic signal source," *Astronomy and Astrophysics*, Springer-Verlag, Vol. 203, No. 2, pp. 399-406 (September (II) 1988).
	AQ	19	Moulsley, T.J. *et al.*, "The efficient acquisition and processing of propagation statistics," *Journal of the Institution of Electronic and Radio Engineers*, IERE, Vol. 55, No. 3, pp. 97-103 (March 1985).
	AR	19	Ndzi, D. *et al.*, "Wide-Band Statistical Characterization of an Over-the-Sea Experimental Transhorizon Link," *IEE Colloquium on Radio Communications at Microwave and Millimetre Wave Frequencies*, IEE, pp. 1/1-1/6 (December 16, 1996).

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	AA20	5,136,267	08/1992	Cabot	333	174	
	AB20	5,140,705	08/1992	Kosuga	455	318	
	AC20	5,150,124	09/1992	Moore *et al.*	342	68	
	AD20	5,151,661	09/1992	Caldwell *et al.*	328	14	
	AE20	5,159,710	10/1992	Cusdin	455	304	
	AF20	5,170,414	12/1992	Silvian	375	59	
	AG20	5,172,070	12/1992	Hiraiwa *et al.*	329	304	
	AH20	5,191,459	03/1993	Thompson *et al.*	359	133	
	AI20	5,204,642	04/1993	Ashgar *et al.*	331	135	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ20						Yes No
	AK20						Yes No
	AL20						Yes No
	AM20						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	20	Ndzi, D. *et al.*, "Wideband Statistics of Signal Levels and Doppler Spread on an Over-The-Sea Transhorizon Link," *IEE Colloquium on Propagation Characteristics and Related System Techniques for Beyond Line-of-Sight Radio*, IEE, pp. 9/1-9/6 (November 24, 1997).
	AO	20	"New zero IF chipset from Philips," *Electronic Engineering*, United News & Media, Vol. 67, No. 825, p. 10 (September 1995).
	AP	20	Ohara, H. *et al.*, "First monolithic PCM filter cuts cost of telecomm systems," *Electronic Design*, Hayden Publishing Company, Vol. 27, No. 8, pp. 130-135 (April 12, 1979).
	AQ	20	Oppenheim, A.V. *et al.*, *Signals and Systems*, Prentice-Hall, pp. 527-531 and 561-562 (1983).
	AR	20	Ortgies, G., "Experimental Parameters Affecting Amplitude Scintillation Measurements on Satellite Links," *Electronics Letters*, IEE, Vol. 21, No. 17, pp. 771-772 (August 15, 1985).

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	AA21	5,212,827	05/1993	Meszko *et al.*	455	219	
	AB21	5,214,787	05/1993	Karkota, Jr.	455	3.2	
	AC21	5,220,583	06/1993	Solomon	375	82	
	AD21	5,220,680	06/1993	Lee	455	102	
	AE21	5,222,144	06/1993	Whikehart	381	15	
	AF21	5,230,097	07/1993	Currie *et al.*	455	226.1	
	AG21	5,239,686	08/1993	Downey	455	78	
	AH21	5,241,561	08/1993	Barnard	375	1	
	AI21	5,249,203	09/1993	Loper	375	97	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ21						Yes No
	AK21						Yes No
	AL21						Yes No
	AM21						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	21	Pärssinen et al., "A 2-GHz Subharmonic Sampler for Signal Downconversion," *IEEE Transactions on Microwave Theory and Techniques*, IEEE, Vol. 45, No. 12, 7 pages (December 1997).
	AO	21	Peeters, G. *et al.*, "Evaluation of Statistical Models for Clear-Air Scintillation Prediction Using Olympus Satellite Measurements," *International Journal of Satellite Communications*, John Wiley and Sons, Vol. 15, No. 2, pp. 73-88 (March-April 1997).
	AP	21	Perrey, A.G. and Schoenwetter, H.K., *NBS Technical Note 1121: A Schottky Diode Bridge Sampling Gate*, U.S. Dept. of Commerce, pp. 1-14 (May 1980).
	AQ	21	Poulton, K. *et al.*, "A 1-Ghz 6-bit ADC System," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-22, No. 6, pp. 962-969 (December 1987).
	AR	21	Press Release, "Parkervision, Inc. Announces Fiscal 1993 Results," Lippert/Heilshorn and Associates, 2 Pages (April 6, 1994).

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

::ODMA\MHODMA\SKGF_DC1;32466;1

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	APPLICANT Sorrells *et al.*	
	FILING DATE August 4, 2000	GROUP 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA22	5,251,218	10/1993	Stone *et al.*	370	120	
	AB22	5,251,232	10/1993	Nonami	375	5	
	AC22	5,260,970	11/1993	Henry *et al.*	375	10	
	AD22	5,263,194	11/1993	Ragan	455	316	
	AE22	5,263,196	11/1993	Jasper	455	324	
	AF22	5,267,023	11/1993	Kawasaki	358	23	
	AG22	5,278,826	01/1994	Murphy *et al.*	370	76	
	AH22	5,282,023	01/1994	Scarpa	358	36	
	AI22	5,287,516	02/1994	Schaub	375	88	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ22						Yes No
	AK22						Yes No
	AL22						Yes No
	AM22						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	22	Press Release, "Parkervision, Inc. Announces the Appointment of Michael Baker to the New Position of National Sales Manager," Lippert/Heilshorn and Associates, 1 Page (April 7, 1994).
	AO	22	Press Release, "Parkervision's Cameraman Well-Received By Distance Learning Market," Lippert/Heilshorn and Associates, 2 Pages (April 8, 1994).
	AP	22	Press Release, "Parkervision, Inc. Announces First Quarter Financial Results," Lippert/Heilshorn and Associates, 2 Pages (April 26, 1994).
	AQ	22	Press Release, "Parkervision, Inc. Announces The Retirement of William H. Fletcher, Chief Financial Officer," Lippert/Heilshorn and Associates, 1 Page (May 11, 1994).
	AR	22	Press Release, "Parkervision, Inc. Announces New Cameraman System II™ At Infocomm Trade Show," Lippert/Heilshorn and Associates, 3 Pages (June 9, 1994).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA23	5,293,398	03/1994	Hamao *et al.*	375	1	
	AB23	5,303,417	04/1994	Laws	455	314	
	AC23	5,307,517	04/1994	Rich	455	306	
	AD23	5,315,583	05/1994	Murphy *et al.*	370	18	
	AE23	5,321,852	06/1994	Seong	455	182.1	
	AF23	5,325,204	06/1994	Scarpa	348	607	
	AG23	5,337,014	08/1994	Najle *et al.*	324	613	
	AH23	5,339,054	08/1994	Taguchi	332	100	
	AI23	5,339,459	08/1994	Schiltz *et al.*	455	333	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ23						Yes No
	AK23						Yes No
	AL23						Yes No
	AM23						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	23	Press Release, "Parkervision, Inc. Announces Appointments to its National Sales Force," Lippert/Heilshorn and Associates, 2 Pages (June 17, 1994).
	AO	23	Press Release, "Parkervision, Inc. Announces Second Quarter and Six Months Financial Results," Lippert/Heilshorn and Associates, 3 Pages (August 9, 1994).
	AP	23	Press Release, "Parkervision, Inc. Announces Third Quarter and Nine Months Financial Results," Lippert/Heilshorn and Associates, 3 Pages (October 28, 1994).
	AQ	23	Press Release, "Parkervision, Inc. Announces First Significant Dealer Sale of Its *Cameraman*® System II," Lippert/Heilshorn and Associates, 2 Pages (November 7, 1994).
	AR	23	Press Release, "Parkervision, Inc. Announces Fourth Quarter and Year End Results," Lippert/Heilshorn and Associates, 2 Pages (March 1, 1995).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA24	5,355,114	10/1994	Sutterlin *et al.*	340	310 A	
	AB24	5,361,408	11/1994	Watanabe *et al.*	455	324	
	AC24	5,369,800	11/1994	Takagi *et al.*	455	59	
	AD24	5,375,146	12/1994	Chalmers	375	103	
	AE24	5,379,040	01/1995	Mizomoto *et al.*	341	143	
	AF24	5,379,141	01/1995	Thompson *et al.*	359	125	
	AG24	5,388,063	02/1995	Takatori *et al.*	364	724.17	
	AH24	5,390,364	02/1995	Webster *et al.*	455	52.3	
	AI24	5,400,084	03/1995	Scarpa	348	624	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ24						Yes No
	AK24						Yes No
	AL24						Yes No
	AM24						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	24	Press Release, "Parkervision, Inc. Announces Joint Product Developments With VTEL," Lippert/Heilshorn and Associates, 2 Pages (March 21, 1995).
	AO	24	Press Release, "Parkervision, Inc. Announces First Quarter Financial Results," Lippert/Heilshorn and Associates, 3 Pages (April 28, 1995).
	AP	24	Press Release, "Parkervision Wins Top 100 Product Districts' Choice Award," Parkervision Marketing and Manufacturing Headquarters, 1 Page (June 29, 1995).
	AQ	24	Press Release, "Parkervision National Sales Manager Next President of USDLA," Parkervision Marketing and Manufacturing Headquarters, 1 Page (July 6, 1995).
	AR	24	Press Release, "Parkervision Granted New Patent," Parkervision Marketing and Manufacturing Headquarters, 1 Page (July 21, 1995).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA25	5,404,127	04/1995	Lee *et al.*	340	310.02	
	AB25	5,410,541	04/1995	Hotto	370	76	
	AC25	5,410,743	04/1995	Seely *et al.*	455	326	
	AD25	5,412,352	05/1995	Graham	332	103	
	AE25	5,416,803	05/1995	Janer	375	324	
	AF25	5,422,913	06/1995	Wilkinson	375	347	
	AG25	5,423,082	06/1995	Cygan *et al.*	455	126	
	AH25	5,428,638	06/1995	Cioffi *et al.*	375	224	
	AI25	5,428,640	06/1995	Townley	375	257	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ25						Yes No
	AK25						Yes No
	AL25						Yes No
	AM25						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	25	Press Release, "Parkervision, Inc. Announces Second Quarter and Six Months Financial Results," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (July 31, 1995).
	AO	25	Press Release, "Parkervision, Inc. Expands Its Cameraman System II Product Line," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (September 22, 1995).
	AP	25	Press Release, "Parkervision Announces New Camera Control Technology," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 25, 1995).
	AQ	25	Press Release, "Parkervision, Inc. Announces Completion of VTEL/Parkervision Joint Product Line," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 30, 1995).
	AR	25	Press Release, "Parkervision, Inc. Announces Third Quarter and Nine Months Financial Results," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 30, 1995).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA26	5,434,546	07/1995	Palmer	332	151	
	AB26	5,438,692	08/1995	Mohindra	455	324	
	AC26	5,444,415	08/1995	Dent *et al.*	329	302	
	AD26	5,444,416	08/1995	Ishikawa *et al.*	329	341	
	AE26	5,444,865	08/1995	Heck *et al.*	455	86	
	AF26	5,446,421	08/1995	Kechkaylo	332	100	
	AG26	5,446,422	08/1995	Mattila *et al.*	332	103	
	AH26	5,448,602	09/1995	Ohmori *et al.*	375	347	
	AI26	5,451,899	09/1995	Lawton	329	302	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ26						Yes No
	AK26						Yes No
	AL26						Yes No
	AM26						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	26	Press Release, "Parkervision's Cameraman Personal Locator Camera System Wins Telecon XV Award," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (November 1, 1995).
	AO	26	Press Release, "Parkervision, Inc. Announces Purchase Commitment From VTEL Corporation," Parkervision Marketing and Manufacturing Headquarters, 1 Page (February 26, 1996).
	AP	26	Press Release, "ParkerVision, Inc. Announces Fourth Quarter and Year End Results," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (February 27, 1996).
	AQ	26	Press Release, "ParkerVision, Inc. Expands its Product Line," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (March 7, 1996).
	AR	26	Press Release, "ParkerVision Files Patents for its Research of Wireless Technology," Parkervision Marketing and Manufacturing Headquarters, 1 Page (March 28, 1996).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA27	5,454,007	09/1995	Dutta	375	322	
	AB27	5,454,009	09/1995	Fruit *et al.*	372	202	
	AC27	5,463,356	10/1995	Palmer	332	117	
	AD27	5,463,357	10/1995	Hobden	332	151	
	AE27	5,465,071	11/1995	Kobayashi *et al.*	329	315	
	AF27	5,465,410	11/1995	Hiben *et al.*	455	266	
	AG27	5,465,415	11/1995	Bien	455	326	
	AH27	5,471,162	11/1995	McEwan	327	92	
	AI27	5,479,120	12/1995	McEwan	327	91	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ27						Yes No
	AK27						Yes No
	AL27						Yes No
	AM27						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	27	Press Release, "Parkervision, Inc. Announces First Significant Sale of Its Cameraman® Three-Chip System," Parkervision Marketing and Manufacturing Headquarters, 2 pages (April 12, 1996).
	AO	27	Press Release, "Parkervision, Inc. Introduces New Product Line For Studio Production Market," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (April 15, 1996).
	AP	27	Press Release, "Parkervision, Inc. Announces Private Placement of 800,000 Shares," Parkervision Marketing and Manufacturing Headquarters, 1 Page (April 15, 1996).
	AQ	27	Press Release, "Parkervision, Inc. Announces First Quarter Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (April 30, 1996).
	AR	27	Press Release, "ParkerVision's New Studio Product Wins Award," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (June 5, 1996).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA28	5,479,447	12/1995	Chow *et al.*	375	260	
	AB28	5,483,193	01/1996	Kennedy *et al.*	329	300	
	AC28	5,483,549	01/1996	Weinberg *et al.*	375	200	
	AD28	5,483,691	01/1996	Heck *et al.*	455	234.2	
	AE28	5,490,173	02/1996	Whikehart *et al.*	375	316	
	AF28	5,493,581	02/1996	Young *et al.*	375	350	
	AG28	5,493,721	02/1996	Reis	455	339	
	AH28	5,495,200	02/1996	Kwan *et al.*	327	554	
	AI28	5,495,202	02/1996	Hsu	327	113	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ28						Yes No
	AK28						Yes No
	AL28						Yes No
	AM28						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	28	Press Release, "Parkervision, Inc. Announces Second Quarter and Six Months Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (August 1, 1996).
	AO	28	Press Release, "Parkervision, Inc. Announces Third Quarter and Nine Months Financial Results," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 29, 1996).
	AP	28	Press Release, "PictureTel and ParkerVision Sign Reseller Agreement," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 30, 1996).
	AQ	28	Press Release, "CLI and ParkerVision Bring Enhanced Ease-of-Use to Videoconferencing," CLI/Parkervision, 2 Pages (January 20, 1997).
	AR	28	Press Release, "Parkervision, Inc. Announces Fourth Quarter and Year End Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (February 27, 1997).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA29	5,495,500	02/1996	Jovanovich *et al.*	375	206	
	AB29	5,499,267	03/1996	Ohe *et al.*	375	206	
	AC29	5,500,758	03/1996	Thompson *et al.*	359	189	
	AD29	5,517,688	05/1996	Fajen *et al.*	455	333	
	AE29	5,519,890	05/1996	Pinckley	455	307	
	AF29	5,523,719	06/1996	Longo *et al.*	327	557	
	AG29	5,523,726	06/1996	Kroeger *et al.*	332	103	
	AH29	5,523,760	06/1996	McEwan	342	89	
	AI29	5,539,770	07/1996	Ishigaki	375	206	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ29						Yes No
	AK29						Yes No
	AL29						Yes No
	AM29						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	29	Press Release, "Parkervision, Inc. Announces First Quarter Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (April 29, 1997).
	AO	29	Press Release, "NEC and Parkervision Make Distance Learning Closer," NEC America, 2 Pages (June 18, 1997).
	AP	29	Press Release, "Parkervision Supplies JPL with Robotic Cameras, Cameraman Shot Director for Mars Mission," Parkervision Marketing and Manufacturing Headquarters, 2 pages (July 8, 1997).
	AQ	29	Press Release, "ParkerVision and IBM Join Forces to Create Wireless Computer Peripherals," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (July 23, 1997).
	AR	29	Press Release, "ParkerVision, Inc. Announces Second Quarter and Six Months Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (July 31, 1997).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA30	5,555,453	09/1996	Kajimoto *et al.*	455	266	
	AB30	5,557,641	09/1996	Weinberg	375	295	
	AC30	5,557,642	09/1996	Williams	375	316	
	AD30	5,579,341	11/1996	Smith *et al.*	375	267	
	AE30	5,579,347	11/1996	Lindquist *et al.*	375	346	
	AF30	5,584,068	12/1996	Mohindra	455	324	
	AG30	5,592,131	01/1997	Labreche *et al.*	332	103	
	AH30	5,602,847	02/1997	Pagano *et al.*	370	484	
	AI30	5,602,868	02/1997	Wilson	375	219	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ30						Yes No
	AK30						Yes No
	AL30						Yes No
	AM30						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	<u>30</u>	Press Release, "Parkervision, Inc. Announces Private Placement of 990,000 Shares," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (September 8, 1997).
	AO	<u>30</u>	Press Release, "Wal-Mart Chooses Parkervision for Broadcast Production," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 24, 1997).
	AP	<u>30</u>	Press Release, "Parkervision, Inc. Announces Third Quarter Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (October 30, 1997).
	AQ	<u>30</u>	Press Release, "ParkerVision Announces Breakthrough in Wireless Radio Frequency Technology," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (December 10, 1997).
	AR	<u>30</u>	Press Release, "Parkervision, Inc. Announces the Appointment of Joseph F. Skovron to the Position of Vice President, Licensing - Wireless Technologies," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (January 9, 1998).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA31	5,604,732	02/1997	Kim *et al.*	370	342	
	AB31	5,608,531	03/1997	Honda *et al.*	386	1	
	AC31	5,610,946	03/1997	Tanaka *et al.*	375	269	
	AD31	RE 35,494	04/1997	Nicollini	327	554	
	AE31	5,617,451	04/1997	Mimura *et al.*	375	340	
	AF31	5,619,538	04/1997	Sempel *et al.*	375	328	
	AG31	5,621,455	04/1997	Rogers *et al.*	348	6	
	AH31	5,630,227	05/1997	Bella *et al.*	455	324	
	AI31	5,640,415	06/1997	Pandula	375	202	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ31						Yes No
	AK31						Yes No
	AL31						Yes No
	AM31						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	<u>31</u>	Press Release, "Parkervision Announces Existing Agreement with IBM Terminates-- Company Continues with Strategic Focus Announced in December," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (January 27, 1998).
	AO	<u>31</u>	Press Release, "Laboratory Tests Verify Parkervision Wireless Technology," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (March 3, 1998).
	AP	<u>31</u>	Press Release, "Parkervision, Inc. Announces Fourth Quarter and Year End Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (March 5, 1998).
	AQ	<u>31</u>	Press Release, "Parkervision Awarded Editors' Pick of Show for NAB 98," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (April 15, 1998).
	AR	<u>31</u>	Press Release, "Parkervision Announces First Quarter Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (May 4, 1998).

EXAMINER	DATE CONSIDERED

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA32	5,640,424	06/1997	Banavong *et al.*	375	316	
	AB32	5,640,428	06/1997	Abe *et al.*	375	334	
	AC32	5,640,698	06/1997	Shen *et al.*	455	323	
	AD32	5,648,985	07/1997	Bjerede *et al.*	375	219	
	AE32	5,650,785	07/1997	Rodal	342	357	
	AF32	5,661,424	08/1997	Tang	327	105	
	AG32	5,663,878	09/1997	Walker	363	159	
	AH32	5,663,986	09/1997	Striffler	375	260	
	AI32	5,668,836	09/1997	Smith *et al.*	375	316	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ32						Yes No
	AK32						Yes No
	AL32						Yes No
	AM32						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	<u>32</u>	Press Release, "Parkervision 'DIRECT2DATA' Introduced in Response to Market Demand," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (July 9, 1998).
	AO	<u>32</u>	Press Release, "Parkervision Expands Senior Management Team," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (July 29, 1998).
	AP	<u>32</u>	Press Release, "Parkervision Announces Second Quarter and Six Month Financial Results," Parkervision Marketing and Manufacturing Headquarters, 4 Pages (July 30, 1998).
	AQ	<u>32</u>	Press Release, "Parkervision Announces Third Quarter and Nine Month Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (October 30, 1998).
	AR	<u>32</u>	Press Release, "Questar Infocomm, Inc. Invests $5 Million in Parkervision Common Stock," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (December 2, 1998).

EXAMINER	DATE CONSIDERED

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA33	5,680,078	10/1997	Ariie	332	178	
	AB33	5,680,418	10/1997	Croft *et al.*	375	346	
	AC33	5,689,413	11/1997	Jaramillo *et al.*	363	146	
	AD33	5,699,006	12/1997	Zele *et al.*	327	341	
	AE33	5,705,955	01/1998	Freeburg *et al.*	331	14	
	AF33	5,710,998	01/1998	Opas	455	324	
	AG33	5,714,910	02/1998	Skoczen *et al.*	331	3	
	AH33	5,715,281	02/1998	Bly *et al.*	375	344	
	AI33	5,721,514	02/1998	Crockett *et al.*	331	3	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ33						Yes No
	AK33						Yes No
	AL33						Yes No
	AM33						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	33	Press Release, "Parkervision Adds Two New Directors," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (March 5, 1999).
	AO	33	Press Release, "Parkervision Announces Fourth Quarter and Year End Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (March 5, 1999).
	AP	33	Press Release, "Joint Marketing Agreement Offers New Automated Production Solution," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (April 13, 1999).
	AQ	33	"Project COST 205: Scintillations in Earth-satellite links," *Alta Frequenza: Scientific Review in Electronics*, AEI, Vol. LIV, No. 3, pp. 209-211 (May-June, 1985).
	AR	33	Razavi, B., *RF Microelectronics*, Prentice-Hall, pp. 147-149 (1998).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA34	5,724,002	03/1998	Hulick	329	361	
	AB34	5,724,653	03/1998	Baker *et al.*	455	296	
	AC34	5,729,577	03/1998	Chen	375	334	
	AD34	5,729,829	03/1998	Talwar *et al.*	455	63	
	AE34	5,732,333	03/1998	Cox *et al.*	455	126	
	AF34	5,736,895	04/1998	Yu *et al.*	327	554	
	AG34	5,737,035	04/1998	Rotzoll	348	725	
	AH34	5,742,189	04/1998	Yoshida *et al.*	327	113	
	AI34	5,748,683	05/1998	Smith *et al.*	375	347	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ34						Yes No
	AK34						Yes No
	AL34						Yes No
	AM34						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	<u>34</u>	Reeves, R.J.D., "The Recording and Collocation of Waveforms (Part 1)," *Electronic Engineering*, Morgan Brothers Limited, Vol. 31, No. 373, pp. 130-137 (March 1959).
	AO	<u>34</u>	Reeves, R.J.D., "The Recording and Collocation of Waveforms (Part 2)," *Electronic Engineering*, Morgan Brothers Limited, Vol. 31, No. 374, pp. 204-212 (April 1959).
	AP	<u>34</u>	Rein, H.M. and Zahn, M., "Subnanosecond-Pulse Generator with Variable Pulsewidth Using Avalanche Transistors," *Electronics Letters*, IEE, Vol. 11, No. 1, pp. 21-23 (January 9, 1975).
	AQ	<u>34</u>	Riad, S.M. and Nahman, N.S., "Modeling of the Feed-through Wideband (DC to 12.4 Ghz) Sampling-Head," *IEEE MTT-S International Microwave Symposium Digest*, IEEE, pp. 267-269 (June 27-29, 1978).
	AR	<u>34</u>	Rizzoli, V. *et al.*, "Computer-Aided Noise Analysis of MESFET and HEMT Mixers," *IEEE Transactions on Microwave Theory and Techniques*, IEEE, Vol. 37, No. 9, pp. 1401-1410 (September 1989).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA35	RE 35,829	06/1998	Sanderford, Jr.	375	200	
	AB35	5,760,645	06/1998	Comte *et al.*	329	304	
	AC35	5,764,087	06/1998	Clark	327	105	
	AD35	5,767,726	06/1998	Wang	327	356	
	AE35	5,768,118	06/1998	Faulk *et al.*	363	72	
	AF35	5,771,442	06/1998	Wang *et al.*	455	93	
	AG35	5,777,692	07/1998	Ghosh	348	725	
	AH35	5,777,771	07/1998	Smith	359	180	
	AI35	5,786,844	07/1998	Rogers *et al.*	348	6	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ35						Yes No
	AK35						Yes No
	AL35						Yes No
	AM35						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	35	Rowe, H.E., *Signals and Noise in Communication Systems*, D. Van Nostrand Company, Inc., Princeton, New Jersey, including, for example, Chapter V, Pulse Modulation Systems (1965).
	AO	35	Rücker, F. and Dintelmann, F., "Effect of Antenna Size on OTS Signal Scintillations and Their Seasonal Dependence," *Electronics Letters*, IEE, Vol. 19, No. 24, pp. 1032-1034 (November 24, 1983).
	AP	35	Russell, R. and Hoare, L., "Millimeter Wave Phase Locked Oscillators," *Military Microwaves '78 Conference Proceedings*, Microwave Exhibitions and Publishers, pp. 238-242 (October 25-27, 1978).
	AQ	35	Sabel, L.P., "A DSP Implementation of a Robust Flexible Receiver/Demultiplexer for Broadcast Data Satellite Communications," *The Institution of Engineers Australia Communications Conference*, Institution of Engineers, Australia, pp. 218-223 (October 16-18, 1990).
	AR	35	Salous, S., "IF digital generation of FMCW waveforms for wideband channel characterization," *IEE Proceedings-I*, IEE, Vol. 139, No. 3, pp. 281-288 (June 1992).

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA36	5,793,801	08/1998	Fertner	375	219	
	AB36	5,793,818	08/1998	Claydon *et al.*	375	326	
	AC36	5,802,463	09/1998	Zuckerman	455	208	
	AD36	5,809,060	09/1998	Cafarella *et al.*	375	206	
	AE36	5,818,582	10/1998	Fernandez *et al.*	356	318	
	AF36	5,825,254	10/1998	Lee	331	25	
	AG36	5,834,985	11/1998	Sundegård	332	100	
	AH36	5,864,754	01/1999	Hotto	455	280	
	AI36	5,881,375	03/1999	Bonds	455	118	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ36						Yes No
	AK36						Yes No
	AL36						Yes No
	AM36						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	36	"Sampling Loops Lock Sources to 23 Ghz," *Microwaves & RF*, Penton Publishing, p. 212 (September 1990).
	AO	36	Sasikumar, M. *et al.*, "Active Compensation in the Switched-Capacitor Biquad," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 1008-1009 (August 1983).
	AP	36	Saul, P.H., "A GaAs MESFET Sample and Hold Switch," *Fifth European Solid State Circuits Conference-ESSCIRC 79*, IEE, pp. 5-7 (1979).
	AQ	36	Shen, D.H. *et al.*, "A 900-MHZ RF Front-End with Integrated Discrete-Time Filtering," *IEEE Journal of Solid-State Circuits*, IEEE Solid-State Circuits Council, Vol. 31, No. 12, pp. 1945-1954 (December 1996).
	AR	36	Shen, X.D. and Vilar, E., "Anomalous transhorizon propagation and meteorological processes of a multilink path," *Radio Science*, American Geophysical Union, Vol. 30, No. 5, pp. 1467-1479 (September-October 1995).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA37	5,892,380	04/1999	Quist	327	172	
	AB37	5,894,239	04/1999	Bonaccio *et al.*	327	176	
	AC37	5,896,562	04/1999	Heinonen	455	76	
	AD37	5,900,747	05/1999	Brauns	327	9	
	AE37	5,901,054	05/1999	Leu *et al.*	363	41	
	AF37	5,901,187	05/1999	Iinuma	375	347	
	AG37	5,901,344	05/1999	Opas	455	76	
	AH37	5,901,347	05/1999	Chambers *et al.*	455	234.1	
	AI37	5,901,348	05/1999	Bang *et al.*	455	254	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ37						Yes No
	AK37						Yes No
	AL37						Yes No
	AM37						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	37	Shen, X. and Tawfik, A.N., "Dynamic Behaviour of Radio Channels Due to Trans-Horizon Propagation Mechanisms," *Electronics Letters*, IEE, Vol. 29, No. 17, pp. 1582-1583 (August 19, 1993).
	AO	37	Shen, X. *et al.*, "Modeling Enhanced Spherical Diffraction and Troposcattering on a Transhorizon Path with aid of the parabolic Equation and Ray Tracing Methods," *IEE Colloquium on Common modeling techniques for electromagnetic wave and acoustic wave propagation*, IEE, pp. 4/1-4/7 (March 8, 1996).
	AP	37	Shen, X. and Vilar, E., "Path loss statistics and mechanisms of transhorizon propagation over a sea path," *Electronics Letters*, IEE, Vol. 32, No. 3, pp. 259-261 (February 1, 1996).
	AQ	37	Shen, D. *et al.*, "A 900 MHZ Integrated Discrete-Time Filtering RF Front-End," *IEEE International Solid State Circuits Conference*, IEEE, Vol. 39, pp. 54-55 and 417 (February 1996).
	AR	37	Spillard, C. *et al.*, "X-Band Tropospheric Transhorizon Propagation Under Differing Meteorological Conditions," *Sixth International Conference on Antennas and Propagation (ICAP 89) Part 2: Propagation*, IEE, pp. 451-455 (April 4-7, 1989).

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA38	5,901,349	05/1999	Guegnaud *et al.*	455	302	
	AB38	5,903,178	05/1999	Miyatsuji *et al.*	327	308	
	AC38	5,903,187	05/1999	Claverie *et al.*	329	342	
	AD38	5,903,196	05/1999	Salvi *et al.*	331	16	
	AE38	5,903,421	05/1999	Furutani *et al.*	361	58	
	AF38	5,903,553	05/1999	Sakamoto *et al.*	370	338	
	AG38	5,903,595	05/1999	Suzuki	375	207	
	AH38	5,903,609	05/1999	Kool *et al.*	375	261	
	AI38	5,903,827	05/1999	Kennan *et al.*	455	326	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ38						Yes No
	AK38						Yes No
	AL38						Yes No
	AM38						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	38	Stafford, K.R. *et al.*, "A Complete Monolithic Sample/Hold Amplifier," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-9, No. 6, pp. 381-387 (December 1974).
	AO	38	Staruk, W. Jr. *et al.*, "Pushing HF Data Rates," *Defense Electronics*, EW Communications, Vol. 17, No. 5, pp. 211, 213, 215, 217, 220 and 222 (May 1985).
	AP	38	Stephenson, A.G., "Digitizing multiple RF signals requires an optimum sampling rate," *Electronics*, McGraw-Hill, pp. 106-110 (March 27, 1972).
	AQ	38	Sugarman, R., "Sampling Oscilloscope for Statistically Varying Pulses," *The Review of Scientific Instruments*, American Institute of Physics, Vol. 28, No. 11, pp. 933-938 (November 1957).
	AR	38	Sylvain, M., "Experimental probing of multipath microwave channels," *Radio Science*, American Geophysical Union, Vol. 24, No. 2, pp. 160-178 (March-April 1989).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA39	5,903,854	05/1999	Abe *et al.*	455	575	
	AB39	5,905,449	05/1999	Tsubouchi *et al.*	340	925.69	
	AC39	5,907,149	05/1999	Marckini	235	487	
	AD39	5,907,197	05/1999	Faulk	307	119	
	AE39	5,911,116	06/1999	Nosswitz	455	83	
	AF39	5,911,123	06/1999	Shaffer *et al.*	455	554	
	AG39	5,914,622	06/1999	Inoue	327	172	
	AH39	5,920,199	07/1999	Sauer	324	678	
	AI39	5,943,370	08/1999	Smith	375	334	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ39						Yes No
	AK39						Yes No
	AL39						Yes No
	AM39						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	39	Takano, T., "NOVEL GaAs Pet Phase Detector Operable To Ka Band," *IEEE MT-S Digest*, IEEE, pp. 381-383 (1984).
	AO	39	Tan, M.A., "Biquadratic Transconductance Switched-Capacitor Filters," *IEEE Transactions on Circuits and Systems- I: Fundamental Theory and Applications*, IEEE Circuits and Systems Society, Vol. 40, No. 4, pp. 272-275 (April 1993).
	AP	39	Tanaka, K. *et al.*, "Single Chip Multisystem AM Stereo Decoder IC," *IEEE Transactions on Consumer Electronics*, IEEE Consumer Electronics Society, Vol. CE-32, No. 3, pp. 482-496 (August 1986).
	AQ	39	Tawfik, A.N., "Amplitude, Duration and Predictability of Long Hop Trans-Horizon X-band Signals Over the Sea," *Electronics Letters*, IEE, Vol. 28, No. 6, pp. 571-572 (March 12, 1992).
	AR	39	Tawfik, A.N. and Vilar, E., "Correlation of Transhorizon Signal Level Strength with Localized Surface Meteorological Parameters," *Eighth International Conference on Antennas and Propagation*, Electronics Division of the IEE, pp. 335-339 (March 30- April 2, 1993).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA40	4,017,798	04/1977	Gordy *et al.*	325	42	
	AB40	4,032,847	06/1977	Unkauf	325	323	
	AC40	4,253,067	02/1981	Caples *et al.*	329	110	
	AD40	4,393,395	07/1983	Hacke *et al.*	358	23	
	AE40	4,816,704	03/1989	Fiori, Jr.	307	519	
	AF40	4,841,265	06/1989	Watanabe *et al.*	333	194	
	AG40	4,943,974	07/1990	Motamedi	375	1	
	AH40	5,115,409	05/1992	Stepp	364	841	
	AI40	5,353,306	10/1994	Yamamoto	375	14	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ40						Yes No
	AK40						Yes No
	AL40						Yes No
	AM40						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	40	Tawfik, A.N. and Vilar, E., "Dynamic Structure of a Transhorizon Signal at X-band Over a Sea Path," *Sixth International Conference on Antennas and Propagation (ICAP 89) Part 2: Propagation*, IEE, pp. 446-450 (April 4-7, 1989).
	AO	40	Tawfik, A.N. and Vilar, E., "Statistics of Duration and Intensity of Path Loss in a Microwave Transhorizon Sea-Path," *Electronics Letters*, IEE, Vol. 26, No. 7, pp. 474-476 (March 29, 1990).
	AP	40	Tawfik, A.N. and Vilar, E., "X-Band Transhorizon Measurements of CW Transmissions Over the Sea- Part 1: Path Loss, Duration of Events, and Their Modeling," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. 41, No. 11, pp. 1491-1500 (November 1993).
	AQ	40	Temes, G.C. and Tsividis, T., "The Special Section on Switched-Capacitor Circuits," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 915-916 (August 1983).
	AR	40	Thomas, G.B., *Calculus and Analytic Geometry*, Third Edition, Addison-Wesley Publishing, pp. 119-133 (1960).

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA41	5,515,014	05/1996	Troutman	332	178	
	AB41	5,563,550	10/1996	Toth	329	347	
	AC41	5,574,755	11/1996	Persico	375	295	
	AD41	5,604,592	02/1997	Kotidis *et al.*	356	357	
	AE41	5,638,396	06/1997	Klimek	372	92	
	AF41	5,675,392	10/1997	Nayebi *et al.*	348	584	
	AG41	5,694,096	12/1997	Ushiroku *et al.*	333	195	
	AH41	5,757,870	05/1998	Miya *et al.*	375	367	
	AI41	5,768,323	06/1998	Kroeger *et al.*	375	355	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ41						Yes No
	AK41						Yes No
	AL41						Yes No
	AM41						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	41	Tomassetti, Q., "An Unusual Microwave Mixer," *16th European Microwave Conference*, Microwave Exhibitions and Publishers, pp. 754-759 (September 8-12, 1986).
	AO	41	Tortoli, P. *et al.*, "Bidirectional Doppler Signal Analysis Based on a Single RF Sampling Channel," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, IEEE Ultrasonics, Ferroelectrics, and Frequency Control Society, Vol. 41, No. 1, pp. 1-3 (January 1984).
	AP	41	Tsividis, Y. and Antognetti, P. (Ed.), *Design of MOS VLSI Circuits for Telecommunications*, Prentice-Hall, p. 304 (1985).
	AQ	41	Tsividis, Y., "Principles of Operation and Analysis of Switched-Capacitor Circuits," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 926-940 (August 1983).
	AR	41	Tsurumi, H. and Maeda, T., "Design Study on a Direct Conversion Receiver Front-End for 280 MHZ, 900 MHZ, and 2.6 Ghz Band Radio Communication Systems," *41st IEEE Vehicular Technology Conference*, IEEE Vehicular Technology Society, pp. 457-462 (May 19-22, 1991).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA42	5,770,985	06/1998	Ushiroku *et al.*	333	193	
	AB42	5,778,022	07/1998	Walley	375	206	
	AC42	5,812,546	09/1998	Zhou *et al.*	370	342	
	AD42	5,818,869	10/1998	Miya *et al.*	375	206	
	AE42	5,844,449	12/1998	Abeno *et al.*	332	105	
	AF42	5,872,446	02/1999	Cranford, Jr. *et al.*	323	315	
	AG42	5,909,447	06/1999	Cox *et al.*	370	508	
	AH42	5,933,467	08/1999	Sehier *et al.*	375	350	
	AI42	5,952,895	09/1999	McCune, Jr. *et al.*	332	128	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ42						Yes No
	AK42						Yes No
	AL42						Yes No
	AM42						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	42	Valdmanis, J.A. *et al.*, "Picosecond and Subpicosend Optoelectronics for Measurements of Future High Speed Electronic Devices," *IEDM Technical Digest*, IEEE, pp. 597-600 (December 5-7, 1983).
	AO	42	van de Kamp, M.M.J.L., "Asymmetric signal level distribution due to tropospheric scintillation," *Electronics Letters*, IEE, Vol. 34, No. 11, pp. 1145-1146 (May 28, 1998).
	AP	42	Vasseur, H. and Vanhoenacker, D., "Characterization of tropospheric turbulent layers from radiosonde data," *Electronics Letters*, IEE, Vol. 34, No. 4, pp. 318-319 (February 19, 1998).
	AQ	42	Verdone, R., "Outage Probability Analysis for Short-Range Communication Systems at 60 Ghz in ATT Urban Environments," *IEEE Transactions on Vehicular Technology*, IEEE Vehicular Technology Society, Vol. 46, No. 4, pp. 1027-1039 (November 1997).
	AR	42	Vierira-Ribeiro, S.A., *Single-IF DECT Receiver Architecture using a Quadrature Sub-Sampling Band-Pass Sigma-Delta Modulator*, Thesis for Degree of Master's of Engineering, Carleton University, UMI Dissertation Services, pp. 1-180 (April 1995).

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA43	5,960,033	09/1999	Shibano *et al.*	375	207	
	AB43	6,041,073	03/2000	Davidovici *et al.*	375	148	
	AC43	6,054,889	04/2000	Kobayashi	327	357	
	AD43	6,084,922	07/2000	Zhou *et al.*	375	316	
	AE43	6,125,271	09/2000	Rowland *et al.*	455	313	03/06/1998
	AF43	6,147,340	11/2000	Levy	250	214 R	09/29/1998
	AG43	6,147,763	11/2000	Steinlechner	356	484	12/27/1999
	AH43	6,150,890	11/2000	Damgaard *et al.*	331	14	09/30/1998
	AI43	5,126,682	06/1992	Weinberg *et al.*	329	304	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ43						Yes No
	AK43						Yes No
	AL43						Yes No
	AM43						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	43	Vilar, E. *et al.*, "A Comprehensive/Selective MM-Wave Satellite Downlink Experiment on Fade Dynamics," *Tenth International Conference on Antennas and Propagation*, Electronics Division of the IEE, pp. 2.98-2.101 (April 14-17, 1997).
	AO	43	Vilar, E. *et al.*, "A System to Measure LOS Atmospheric Transmittance at 19 Ghz," *AGARD Conference Proceedings No. 346: Characteristics of the Lower Atmosphere Influencing Radio Wave Propagation*, AGARD, pp. 8-1 - 8-16 (October 4-7, 1983).
	AP	43	Vilar, E. and Smith, H., "A Theoretical and Experimental Study of Angular Scintillations in Earth Space Paths," *IEEE Transactions on Antennas and Propagation*, IEEE, Vol. AP-34, No. 1, pp. 2-10 (January 1986).
	AQ	43	Vilar, E. *et al.*, "A Wide Band Transhorizon Experiment at 11.6 Ghz," *Eighth International Conference on Antennas and Propagation*, Electronics Division of the IEE, pp. 441-445 (March 30- April 2, 1993).
	AR	43	Vilar, E. and Matthews, P.A., "Amplitude Dependence of Frequency in Oscillators," *Electronics Letters*, IEE, Vol. 8, No. 20, pp. 509-511 (October 5, 1972).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA44	5,841,811	11/1998	Song	375	235	
	AB44	4,051,475	09/1977	Campbell	343	180	
	AC44	5,953,642	09/1999	Feldtkeller *et al.*	455	195.1	
	AD44	4,653,117	03/1987	Heck	455	209	
	AE44	5,859,878	01/1999	Phillips *et al.*	375	316	
	AF44	5,894,496	04/1999	Jones	455	126	
	AG44	5,915,278	06/1999	Mallick	73	658	
	AH44	6,028,887	02/2000	Harrison *et al.*	375	206	
	AI44	6,081,691	06/2000	Renard *et al.*	455	12.1	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ44						Yes No
	AK44						Yes No
	AL44						Yes No
	AM44						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	44	Vilar, E. *et al.*, "An experimental mm-wave receiver system for measuring phase noise due to atmospheric turbulence," *Proceedings of the 25th European Microwave Conference*, Nexus House, pp. 114-119 (1995).
	AO	44	Vilar, E. and Burgueño, A., "Analysis and Modeling of Time Intervals Between Rain Rate Exceedances in the Context of Fade Dynamics," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. 39, No. 9, pp. 1306-1312 (September 1991).
	AP	44	Vilar, E. *et al.*, "Angle of Arrival Fluctuations in High and Low Elevation Earth Space Paths," *Fourth International Conference on Antennas and Propagation (ICAP 85)*, Electronics Division of the IEE, pp. 83-88 (April 16-19, 1985).
	AQ	44	Vilar, E., "Antennas and Propagation: A Telecommunications Systems Subject," *Electronics Division Colloquium on Teaching Antennas and Propagation to Undergraduates*, IEE, pp. 7/1-7/6 (March 8, 1988).
	AR	44	Vilar, E. *et al.*, "CERS*. Millimetre-Wave Beacon Package and Related Payload Doppler Correction Strategies," *Electronics Division Colloquium on CERS- Communications Engineering Research Satellite*, IEE, pp. 10/1-10/10 (April 10, 1984).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA45	6,121,819	09/2000	Traylor	327	359	04/06/1998
	AB45	6,144,236	11/2000	Vice *et al.*	327	113	02/01/1998
	AC45	6,144,846	11/2000	Durec	455	323	12/31/1997
	AD45	6,175,728 B1	01/2001	Mitama	455	323	03/03/1998
	AE45	5,705,949	01/1998	Alelyunas *et al.*	329	304	
	AF45	5,883,548	03/1999	Assard *et al.*	329	306	
	AG45	4,484,143	11/1984	French *et al.*	329	50	
	AH45	5,841,324	11/1998	Williams	331	17	
	AI45	4,855,894	08/1989	Asahi *et al.*	363	157	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ45						Yes No
	AK45						Yes No
	AL45						Yes No
	AM45						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	45	Vilar, E. and Moulsley, T.J., "Comment and Reply: Probability Density Function of Amplitude Scintillations," *Electronics Letters*, IEE, Vol. 21, No. 14, pp. 620-622 (July 4, 1985).
	AO	45	Vilar, E. *et al.*, "Comparison of Rainfall Rate Duration Distributions for ILE-IFE and Barcelona," *Electronics Letters*, IEE, Vol. 28, No. 20, pp. 1922-1924 (September 24, 1992).
	AP	45	Vilar, E., "Depolarization and Field Transmittances in Indoor Communications," *Electronics Letters*, IEE, Vol. 27, No. 9, pp. 732-733 (April 25, 1991).
	AQ	45	Vilar, E. and Larsen, J.R., "Elevation Dependence of Amplitude Scintillations on Low Elevation Earth Space Paths," *Sixth International Conference on Antennas and Propagation (ICAP 89) Part 2: Propagation*, IEE, pp. 150-154 (April 4-7, 1989).
	AR	45	Vilar, E. *et al.*, "Experimental System and Measurements of Transhorizon Signal Levels at 11 Ghz," *18th European Microwave Conference*, Microwave Exhibitions and Publishers Ltd., pp. 429-435 (September 12 - 15, 1988).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA46	5,319,799	06/1994	Morita	455	78	
	AB46	5,801,654	09/1998	Traylor	341	144	
	AC46	5,369,404	11/1994	Galton	341	143	
	AD46	3,716,730	02/1973	Cerny, Jr.	307	295	
	AE46	4,080,573	03/1978	Howell	325	439	
	AF46	4,334,324	06/1982	Hoover	455	333	
	AG46	4,369,522	01/1983	Cerny, Jr. *et al.*	455	333	
	AH46	5,465,418	11/1995	Zhou *et al.*	455	332	
	AI46	5,513,389	04/1996	Reeser *et al.*	455	311	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ46						Yes No
	AK46						Yes No
	AL46						Yes No
	AM46						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	46	Vilar, E. and Matthews, P.A., "Importance of Amplitude Scintillations in Millimetric Radio Links," *Proceedings of the 4th European Microwave Conference*, Microwave Exhibitions and Publishers, pp. 202-206 (September 10-13, 1974).
	AO	46	Vilar, E. and Haddon, J., "Measurement and Modeling of Scintillation Intensity to Estimate Turbulence Parameters in an Earth-Space Path," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. AP-32, No. 4, pp. 340-346 (April 1984).
	AP	46	Vilar, E. and Matthews, P.A., "Measurement of Phase Fluctuations on Millimetric Radiowave Propagation," *Electronics Letters*, IEE, Vol. 7, No. 18, pp. 566-568 (September 9, 1971).
	AQ	46	Vilar, E. and Wan, K.W., "Narrow and Wide Band Estimates of Field Strength for Indoor Communications in the Millimetre Band," *Electronics Division Colloquium on Radiocommunications in the Range 30-60 Ghz*, IEE, pp. 5/1-5/8 (January 17, 1991).
	AR	46	Vilar, E. and Faulkner, N.D., "Phase Noise and Frequency Stability Measurements. Numerical Techniques and Limitations," *Electronics Division Colloquium on Low Noise Oscillators and Synthesizer*, IEE, 5 pages (January 23, 1986).

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA47	5,959,850	09/1999	Lim	363	17	
	AB47	5,157,687	10/1992	Tymes	375	1	
	AC47	5,945,660	08/1999	Nakasuji *et al.*	235	462.46	
	AD47	6,091,939	07/2000	Banh	455	102	
	AE47	6,091,941	07/2000	Moriyama *et al.*	455	126	
	AF47	6,098,886	08/2000	Swift *et al.*	235	472.01	01/21/1998
	AG47	6,215,475 B1	04/2001	Meyerson *et al.*	345	173	06/07/1995
	AH47	6,049,706	04/2000	Cook *et al.*	455	313	
	AI47	6,061,551	05/2000	Sorrells *et al.*	455	118	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ47						Yes No
	AK47						Yes No
	AL47						Yes No
	AM47						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	47	Vilar, E. and Senin, S., "Propagation phase noise identified using 40 Ghz satellite downlink," *Electronics Letters*, IEE, Vol. 33, No. 22, pp. 1901-1902 (October 23, 1997).
	AO	47	Vilar, E. *et al.*, "Scattering and Extinction: Dependence Upon Raindrop Size Distribution in Temperate (Barcelona) and Tropical (Belem) Regions," *Tenth International Conference on Antennas and Propagation*, Electronics Division of the IEE, pp. 2.230-2.233 (April 14-17, 1997).
	AP	47	Vilar, E. and Haddon, J., "Scintillation Modeling and Measurement - A Tool for Remote-Sensing Slant Paths," *AGARD Conference Proceedings No. 332: Propagation Aspects of Frequency Sharing, Interference And System Diversity*, AGARD, pp. 27-1 - 27-13 (October 18-22, 1982).
	AQ	47	Vilar, E., "Some Limitations on Digital Transmission Through Turbulent Atmosphere," *International Conference on Satellite Communication Systems Technology,* Electronics Division of the IEE, pp. 169-187 (April 7-10, 1975).
	AR	47	Vilar, E. and Matthews, P.A., "Summary of Scintillation Observations in a 36 Ghz Link Across London," *International Conference on Antennas and Propagation Part 2: Propagation,* IEE, pp. 36-40 (November 28-30, 1978).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA48	6,061,555	05/2000	Bultman *et al.*	455	313	
	AB48	6,091,940	07/2000	Sorrells *et al.*	455	118	
	AC48	6,266,518 B1	07/2001	Sorrells *et al.*	455	118	08/18/1999
	AD48	6,353,735 B1	03/2002	Sorrells *et al.*	455	118	08/23/1999
	AE48	6,370,371 B1	04/2002	Sorrells *et al.*	455	323	03/03/1999
	AF48	5,628,055	05/1997	Stein	455	89	
	AG48	5,678,220	10/1997	Fournier	455	302	
	AH48	5,926,065	07/1999	Wakai *et al.*	329	304	
	AI48	3,622,885	11/1971	Oberdorf *et al.*	325	40	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ48						Yes No
	AK48						Yes No
	AL48						Yes No
	AM48						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	48	Vilar, E. *et al.*, "Wideband Characterization of Scattering Channels," *Tenth International Conference on Antennas and Propagation*, Electronics Division of the IEE, pp. 2.353-2.358 (April 14-17, 1997).
	AO	48	Vollmer, A., "Complete GPS Receiver Fits on Two Chips," *Electronic Design*, Penton Publishing, pp. 50, 52, 54 and 56 (July 6, 1998).
	AP	48	*Voltage and Time Resolution in Digitizing Oscilloscopes: Application Note 348*, Hewlett Packard, pp. 1-11 (November 1986).
	AQ	48	Wan, K.W. *et al.*, "A Novel Approach to the Simultaneous Measurement of Phase and Amplitude Noises in Oscillator," *Proceedings of the 19th European Microwave Conference*, Microwave Exhibitions and Publishers Ltd., pp. 809-813 (September 4-7, 1989).
	AR	48	Wan, K.W. *et al.*, "Extended Variances and Autoregressive/Moving Average Algorithm for the Measurement and Synthesis of Oscillator Phase Noise," *Proceedings Of the 43rd Annual Symposium on Frequency Control*, IEEE, pp. 331-335 (1989).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA49	4,483,017	11/1984	Hampel *et al.*	382	17	
	AB49	09/525,615		Sorrells *et al.*			03/14/2000
	AC49	09/632,855		Sorrells *et al.*			08/14/2000
	AD49	09/632,857		Sorrells *et al.*			08/14/2000
	AE49						
	AF49						
	AG49						
	AH49						
	AI49						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ49						Yes No
	AK49						Yes No
	AL49						Yes No
	AM49						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	49	Wan, K.W. *et al.*, "Wideband Transhorizon Channel Sounder at 11 Ghz," *Electronics Division Colloquium on High Bit Rate UHF/SHF Channel Sounders - Technology and Measurement*, IEE, pp. 3/1-3/5 (December 3, 1993).
	AO	49	Wang, H., "A 1-V Multigigahertz RF Mixer Core in 0.5 - μm CMOS," *IEEE Journal of Solid-State Circuits*, IEEE Solid-State Circuits Society, Vol. 33, No. 12, pp. 2265-2267 (December 1998).
	AP	49	Watson, A.W.D. *et al.*, "Digital Conversion and Signal Processing for High Performance Communications Receivers," *Digital Processing of Signals in Communications*, Institution of Electronic and Radio Engineers, pp. 367-373 (April 22nd -26th, 1985).
	AQ	49	Weast, R.C. *et al.* (Ed.), *Handbook of Mathematical Tables*, Second Edition, The Chemical Rubber Co., pp. 480-485 (1964).
	AR	49	Wiley, R.G., "Approximate FM Demodulation Using Zero Crossings," *IEEE Transactions on Communications*, IEEE, Vol. COM-29, No. 7, pp. 1061-1065 (July 1981).

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA50						
	AB50						
	AC50						
	AD50						
	AE50						
	AF50						
	AG50						
	AH50						
	AI50						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ50						Yes No
	AK50						Yes No
	AL50						Yes No
	AM50						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	50	Worthman, W., "Convergence... Again," *RF Design*, Primedia, p. 102 (March 1999).
	AO	50	Young, I.A. and Hodges, D.A., "MOS Switched-Capacitor Analog Sampled-Data Direct-Form Recursive Filters," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-14, No. 6, pp. 1020-1033 (December 1979).
	AP	50	Translation of Specification and Claims of FR Patent No. 2245130, 3 pages.
	AQ	50	Fest, Jean-Pierre, "Le Convertisseur A/N Revolutionne Le Recepteur Radio," *Electronique*, JMJ (Publisher), No. 54, pp. 40-42 (December 1995).
	AR	50	Translation of DE Patent No. 35 41 031 A1, 22 pages.

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA51						
	AB51						
	AC51						
	AD51						
	AE51						
	AF51						
	AG51						
	AH51						
	AI51						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ51						Yes No
	AK51						Yes No
	AL51						Yes No
	AM51						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	51	Translation of EP Patent No. 0 732 803 A1, 9 pages.
	AO	51	Fest, Jean-Pierre, "The A/D Converter Revolutionizes the Radio Receiver," *Electronique*, JMJ (Publisher), No. 54, 3 pages (December 1995). (Translation of Doc. AQ50).
	AP	51	Translation of German Patent No. DE 197 35 798 C1, 8 pages.
	AQ	51	Miki, S. and Nagahama, R., *Modulation System II*, Common Edition 7, Kyoritsu Publishing Co., Ltd., pp. 146-154 (April 30, 1956).
	AR	51	Miki, S. and Nagahama, R., *Modulation System II*, Common Edition 7, Kyoritsu Publishing Co., Ltd., pp. 146-149 (April 30, 1956). (Partial Translation of Doc. AQ51).

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA52						
	AB52						
	AC52						
	AD52						
	AE52						
	AF52						
	AG52						
	AH52						
	AI52						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ52						Yes No
	AK52						Yes No
	AL52						Yes No
	AM52						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	52	Rabiner, L.R. and Gold, B., *Theory And Application Of Digital Signal Processing*, Prentice-Hall, Inc., pp. xiii-xii and 40-46 (1975).
	AO	52	English-language Abstract of Japanese Patent Publication No. 08-032556, from *http://www1.ipdl.jpo.go.jp,* 2 Pages (February 2, 1996 - Date of publication of application).
	AP	52	English-language Abstract of Japanese Patent Publication No. 08-139524, from *http://www1.ipdl.jpo.go.jp,* 2 Pages (May 31, 1996 - Date of publication of application).
	AQ	52	English-language Abstract of Japanese Patent Publication No. 59-144249, from *http://www1.ipdl.jpo.go.jp,* 2 Pages (August 18, 1984 - Date of publication of application).
	AR	52	English-language Abstract of Japanese Patent Publication No. 63-054002, from *http://www1.ipdl.jpo.go.jp,* 2 Pages (March 8, 1988 - Date of publication of application).

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	APPLICANT Sorrells *et al.*	
	FILING DATE August 4, 2000	GROUP 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA53						
	AB53						
	AC53						
	AD53						
	AE53						
	AF53						
	AG53						
	AH53						
	AI53						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ53						Yes No
	AK53						Yes No
	AL53						Yes No
	AM53						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	53	English-language Abstract of Japanese Patent Publication No. 06-237276, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (August 23, 1994 - Date of publication of application).
	AO	53	English-language Abstract of Japanese Patent Publication No. 08-023359, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (January 23, 1996 - Date of publication of application).
	AP	53	Translation of Japanese Patent Publication No. 47-2314, 7 pages.
	AQ	53	Partial Translation of Japanese Patent Publication No. 58-7903, 3 pages.
	AR	53	English-language Abstract of Japanese Patent Publication No. 58-133004, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (August 8, 1993 - Date of publication of application).

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

::ODMA\MHODMA\SKGF_DC1;32486;1

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	APPLICANT Sorrells *et al.*	
	FILING DATE August 4, 2000	GROUP 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA54						
	AB54						
	AC54						
	AD54						
	AE54						
	AF54						
	AG54						
	AH54						
	AI54						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ54						Yes No
	AK54						Yes No
	AL54						Yes No
	AM54						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	54	English-language Abstract of Japanese Patent Publication No. 60-058705, from *http://www1.ipdl.jpo.go.jp,* 2 Pages (April 4, 1985 - Date of publication of application).
	AO	54	English-language Abstract of Japanese Patent Publication No. 04-123614, from *http://www1.ipdl.jpo.go.jp,* 2 Pages (April 23, 1992 - Date of publication of application).
	AP	54	English-language Abstract of Japanese Patent Publication No. 04-127601, from *http://www1.ipdl.jpo.go.jp,* 2 Pages (April 28, 1992 - Date of publication of application).
	AQ	54	English-language Abstract of Japanese Patent Publication No. 05-175730, from *http://www1.ipdl.jpo.go.jp,* 2 Pages (July 13, 1993 - Date of publication of application).
	AR	54	English-language Abstract of Japanese Patent Publication No. 05-175734, from *http://www1.ipdl.jpo.go.jp,* 2 Pages (July 13, 1993 - Date of publication of application).

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

::ODMA\MHODMA\SKGF_DC1;32468;1

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	APPLICANT Sorrells *et al.*	
	FILING DATE August 4, 2000	GROUP 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA55						
	AB55						
	AC55						
	AD55						
	AE55						
	AF55						
	AG55						
	AH55						
	AI55						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ55						Yes No
	AK55						Yes No
	AL55						Yes No
	AM55						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	55	English-language Abstract of Japanese Patent Publication No. 07-154344, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (June 16, 1995 - Date of publication of application).
	AO	55	English-language Abstract of Japanese Patent Publication No. 07-307620, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (November 21, 1995 - Date of publication of application).
	AP	55	Oppenheim, A.V. and Schafer, R.W., *Digital Signal Processing*, Prentice-Hall, pp. vii-x, 6-35, 45-78, 87-121 and 136-165 (1975).
	AQ	55	English-language Abstract of Japanese Patent Publication No. 55-066057, from *http://www1.ipdl.jpo.go.jp*, 1 Page (May 19, 1980 - Date of publication of application).
	AR	55	English-language Abstract of Japanese Patent Publication No. 63-065587, from *http://www1.ipdl.jpo.go.jp*, 1 Page (March 24, 1988 - Date of publication of application).

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

::ODMA\MHODMA\SKGF_DC1;32468;1

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	APPLICANT Sorrells *et al.*	
	FILING DATE August 4, 2000	GROUP 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA56						
	AB56						
	AC56						
	AD56						
	AE56						
	AF56						
	AG56						
	AH56						
	AI56						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ56						Yes No
	AK56						Yes No
	AL56						Yes No
	AM56						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	56	English-language Abstract of Japanese Patent Publication No. 63-153691, from *http://www1.ipdl.jpo.go.jp,* 1 Page (June 27, 1988 - Date of publication of application).
	AO	56	
	AP	56	
	AQ	56	
	AR	56	

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

::ODMA\MHODMA\SKGF_DC1;32466;1

Sterne Kessler Goldstein Fox
ATTORNEYS AT LAW

June 9, 2003

WRITER'S DIRECT NUMBER:
(202) 772-8674
INTERNET ADDRESS:
MLEE@SKGF.COM

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Group Art Unit 2634

Re: U.S. Utility Patent Application
Appl. No. 09/632,856; Filed: August 4, 2000
For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations**
Inventors: David F. SORRELLS *et al.*
Our Ref: 1744.0630003

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Second Preliminary Amendment Under 37 C.F.R. § 1.115 in the Revised Format of the Pre-OG Notice Dated January 31, 2003;

2. Supplemental Information Disclosure Statement;

3. A listing of the cited documents on Form PTO-1449 *(4 pages)*;

4. Copies of the cited documents (AE49-AI49; AL19-AM19; AO56-AR56; AA50-AI50; AJ20-AM20; AN57-AQ57; AA51-AF51; AJ21-AM21; AJ22); and

5. One (1) return postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

Enclosures

::ODMA\MHODMA\SKGF_DC1;138439;1

Sterne Kessler Goldstein Fox
ATTORNEYS AT LAW

OIPE JC177
DEC 1 5 2004
PATENT & TRADEMARK

January 23, 2004

WRITER'S DIRECT NUMBER:
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INTERNET ADDRESS:
MLEE@SKGF.COM

FILE COPY

Art Unit 2634

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Re: U.S. Utility Patent Application
Appl. No. 09/632,856; Filed: August 4, 2000
For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementation**
Inventors: Sorrells *et al.*
Our Ref: 1744.0630003

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Second Supplemental Information Disclosure Statement;

2. A list of the cited documents on Forms PTO-1449 (6 pages);

3. A compact Disc labeled "Disc 3" in PDF format (which contains electronic copies of the cited documents);

4. Copies of cited documents: AA56, AB56, AC56, AD56, AE56, AN59; and

5. Return postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

MQL/JTH/agj
SKGF\DC1\222608.1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 2377
David F. SORRELLS *et al.*	Art Unit: 2634
Appl. No. 09/632,856	Examiner: Chin, Stephen
Filed: August 4, 2000	Atty. Docket: 1744.0630003
For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations**	

Supplemental Information Disclosure Statement

Commissioner for Patents
Washington, D.C. 20231

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98. The reference numbering on the accompanying Form PTO-1449 for this Supplemental Information Disclosure Statement is a continuation of the numbering in Applicants' Information Disclosure Statement filed on July 25, 2002 in connection with the above-captioned application.

Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

Applicants provide the following comments regarding the documents:

Document AE49 is a co-owned patent which is directed to related subject matter.

Document AF49 was cited in an Office Action in co-pending U.S. Patent Application Serial No. 09/489,675, filed January 24, 2000, entitled "Bar Code Scanner Using Universal Frequency Translation Technology for Up-Conversion and Down-Conversion," directed to related subject matter. Also cited in said Office Action was U.S. Patent No. 6,091,940, which was cited in Applicants' Information Disclosure Statement filed on July 25, 2002 in connection with the above-captioned application.

Documents AG49-AI49 and AA50-AC50 were cited in an Office Action in co-pending U.S. Patent Application Serial No. 09/476,092, filed January 3, 2000, entitled "Analog Zero IF FM Decoder and Embodiments Thereof, Such as the Family Radio Service," directed to related subject matter.

Documents AL19, AM19 and AD50 were cited in an International Search Report in PCT Appl. No. PCT/US01/08969, filed March 22, 2001, entitled, "Integrated Frequency Translation and Selectivity with a Gain Control Functionality, and Applications Thereof," directed to related subject matter. Also cited in said Search Report were U.S. Patent Nos. 4,888,557 and 5,801,654 and PCT Publication Nos. WO 96/02977 and WO 96/39750, which were cited in Applicants' Information Disclosure Statement filed on July 25, 2002 in connection with the above-captioned application.

Document AJ20 was cited in an Office Action in co-pending Japanese Patent Application Serial No. 2000-577,764, filed June 21, 2000, entitled "Applications of

Universal Frequency Translation,". Also cited in said Office Action was Japanese Patent Publication No. 58-133004, which was cited in Applicants' Information Disclosure Statement filed on July 25, 2002 in connection with the above-captioned application.

Documents AK20, AL20, AJ21, AK21, AL21, AP56 and AQ56 were cited in an International Search Report in PCT Appl. No. PCT/US01/12086, filed April 13, 2001, entitled, "Frequency Converter," directed to related subject matter. Also cited in said International Search Report was U.S. Patent No. 5,844,449, which was cited in Applicants' Information Disclosure Statement filed on July 25, 2002 in connection with the above-captioned application.

Document AE50 was cited in an Office Action in co-pending U.S. Patent Application Serial No. 09/376,509, filed August 18, 1999, entitled "Method and System for Ensuring Reception of a Communications Signal," directed to related subject matter.

Documents AM21 and AJ22 were cited in an Official Notice of Rejection in co-pending Japanese Patent Application No. 2000-577,765, filed June 21, 2000, entitled "Method and System for Ensuring Reception of a Communications Signal," directed to related subject matter. Also cited in said Rejection were Japanese Patent Publication Nos. 56-114451, 8-32556 and 8-139524, which were cited in Applicants' Information Disclosure Statement filed on July 25, 2002 in connection with the above-captioned application.

Documents AF50-AH50, AA51, AC51 and AF51 were cited in and Office Action in co-pending U.S. Patent Application Serial No. 09/476,330, filed January 3, 2000, entitled "Multi-Mode, Multi-Band Communication System," directed to related subject matter.

Document AI50 was cited in an Office Action in co-pending U.S. Patent Application Serial No. 09/567,963, filed May 10, 2000, entitled "Frequency Synthesizer Using Universal Frequency Translation Technology," directed to related subject matter.

Documents AB51, AD51 and AE51 were cited in an Office Action in co-pending U.S. Patent Appl. No. 09/526,041, filed March 14, 2000, entitled, "DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," directed to related subject matter.

The other documents in the PTO-1449 do not fall within the above categories.

It is noted that some of these documents could be classified in more than one of the above categories.

This statement should not be construed as a representation that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below.

☒ 1. This Information Disclosure Statement is being filed before the mailing of a first Office Action. No statement or fee is required.

☐ 2. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection or Notice of Allowance.

☐ a. I hereby state that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ c. Attached is our Check No. 32067 in the amount of $_______ in payment of the fee under 37 C.F.R. § 1.17(p).

☐ 3. This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. A separate Petition to the Group Director, requesting consideration of this Information Disclosure Statement, is concurrently submitted herewith, along with our Check No. ________ in the amount of $ _____ in payment of the fee under 37 C.F.R. § 1.17(i).

☐ a. I hereby state that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ 4. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.

☒ 5. Concise explanations of the relevance of non-English language documents AJ20-AL20, AK21, AM21 and AJ22 appear below:

Document AJ20 (JP 60-130203) appears to describe a frequency converter. A copy of the English language translation of document AJ20 is enclosed as document AO56 on the attached PTO-1449.

Document AK20 (DE 196 27 640 A1) appears to describe a mixer. Document AK20 is a counterpart German application of U.S. Patent No. 5,680,078, which was cited in Applicants' Information Disclosure Statement filed on July 25, 2002 in connection with the above-captioned application.

Document AL20 (EP 0 087 336 A1) appears to describe a transistorized mixer for microwave transmitters. The granted version of document AL20 is cited as document AM20 (EP 0 087 336 B1) and contains an English-language version of the claims.

Document AK21 (FR 2 669 787 A1) appears to describe a symmetrical super high frequency mixer. A copy of the English-language abstract of document AK21 is enclosed as document AR56 on the attached PTO-1449.

Document AM21 (JP 61-30821) appears to describe a squelch device. A copy of the English-language abstract of document AM21 is enclosed as document AP57 on the attached PTO-1449.

Document AJ22 (JP 5-327356) appears to describe a frequency converter. A copy of the English-language abstract of document AJ22 is enclosed as document AQ57 on the attached PTO-1449.

☐ 6. Copies of the documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No. __________, filed _________, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

It is respectfully requested that the Examiner initial and return a copy of the enclosed PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

Date: June 9, 2003

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

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OIPE JC17
DEC 1 5 2004
PATENT & TRADEMARK OFFICE

		Due Date:	None
Applicants:	David F. SORRELLS *et al.*	**Art Unit:**	2634
		Examiner:	Chin, Stephen
Application No.:	09/632,856	**Docket:**	1744.0630003
Filed:	August 4, 2000	**Atty:**	MQL/JEW

For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementations**

When receipt stamp is placed hereon, the USPTO acknowledges receipt of the following documents:

1. SKGF Cover Letter;
2. Second Preliminary Amendment Under 37 C.F.R. § 1.115 in the Revised Format of the Pre-OG Notice Dated January 31, 2003;
3. Supplemental Information Disclosure Statement;
4. A listing of the cited documents on Form PTO-1449 *(4 pages)*;
5. Copies of the cited documents (AE49-AI49; AL19-AM19; AO56-AR56; AA50-AI50; AJ20-AM20; AN57-AQ57; AA51-AF51; AJ21-AM21; AJ22); and
6. One (1) return postcard.

Please Date Stamp And Return To Our Courier

OIPE JC98
JUN 0 9 2003
PATENT & TRADEMARK OFFICE

::ODMA\MHODMA\SKGF_DC1;138454;1

Sterne, Kessler, Goldstein & Fox P.L.L.C.
1100 New York Avenue, NW
Washington, DC 20005-3934

FORM PTO-1449 SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	APPLICANT David F. SORRELLS *et al.*	
	FILING DATE August 4, 2000	GROUP 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AE49	6,421,534 B1	07/2002	Cook *et al.*			08/18/1999
	AF49	6,330,244 B1	12/2001	Swartz *et al.*			01/16/1998
	AG49	4,384,357	05/1983	deBuda *et al.*			
	AH49	4,470,145	09/1984	Williams			
	AI49	5,600,680	02/1997	Mishima *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL19	EP 0 254 844 A2	02/1988	EP	H03D	7/00	N/A
	AM19	EP 0 632 577 A1	01/1995	EP	H03D	7/16	N/A

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AO	56	Translation of Japanese Patent Publication No. 60-130203, 3 pages (July 11, 1985- Date of publication of application).
	AP	56	Razavi, B., "A 900-MHz/1.8-Ghz CMOS Transmitter for Dual-Band Applications," *Symposium on VLSI Circuits Digest of Technical Papers*, IEEE, pp. 128-131 (1998).
	AQ	56	Ritter, G.M., "SDA, A New Solution for Transceivers," *16th European Microwave Conference*, Microwave Exhibitions and Publishers, pp. 729-733 (September 8, 1986).
	AR	56	DIALOG File 351 (Derwent WPI) English Language Patent Abstract for FR 2 669 787, 1 page (May 29, 1992- Date of publication of application).

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

::ODMA\MHODMA\SKGF_DC1;94515;1

FORM PTO-1449 SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	APPLICANT David F. SORRELLS *et al.*	
	FILING DATE August 4, 2000	GROUP 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA50	5,606,731	02/1997	Pace *et al.*			
	AB50	5,870,670	02/1999	Ripley *et al.*			
	AC50	6,314,279 B1	11/2001	Mohindra			06/29/1998
	AD50	5,633,815	05/1997	Young			
	AE50	3,246,084	04/1966	Kryter			
	AF50	3,702,440	11/1972	Moore			
	AG50	3,767,984	10/1973	Shinoda *et al.*			
	AH50	3,852,530	12/1974	Shen			
	AI50	4,220,977	09/1980	Yamanaka			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ20	JP 60-130203	07/1985	JP	H03D	7/00	Yes (Doc. AO56)
	AK20	DE 196 27 640 A1	01/1997	DE	H03D	7/12	No
	AL20	EP 0 087 336 A1	08/1983	EP	H03D	7/12	No
	AM20	EP 0 087 336 B1	07/1986	EP	H03D	7/12	No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	57	Akos, D.M. *et al.*, "Direct Bandpass Sampling of Multiple Distinct RF Signals," *IEEE Transactions on Communications*, IEEE, Vol. 47, No. 7, pp. 983-988 (July 1999).
	AO	57	Patel, M. *et al.*, "Bandpass Sampling for Software Radio Receivers, and the Effect of Oversampling on Aperture Jitter," *VTC 2002*, IEEE, pp. 1901-1905 (2002).
	AP	57	English-language Abstract of Japanese Patent Publication No. 61-030821, 1 Page (February 13, 1986- Date of publication of application).
	AQ	57	English-language Abstract of Japanese Patent Publication No. 05-327356, 1 Page (December 10, 1993 - Date of publication of application).

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

::ODMA\MHODMA\SKGF_DC1;94515;1

FORM PTO-1449 SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	APPLICANT David F. SORRELLS *et al.*	
	FILING DATE August 4, 2000	GROUP 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA51	5,016,242	05/1991	Tang			
	AB51	5,937,013	08/1999	Lam *et al.*			01/03/1997
	AC51	6,014,551	01/2000	Pesola *et al.*			07/16/1997
	AD51	6,073,001	06/2000	Sokoler			05/08/1998
	AE51	6,085,073	07/2000	Palermo *et al.*			03/02/1998
	AF51	6,400,963 B1	06/2002	Glöckler *et al.*			05/21/1999

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ21	EP 0 789 449 A2	08/1997	EP	H03D	7/12	N/A
	AK21	FR 2 669 787 A1	05/1992	FR	H03D	7/14	No
	AL21	GB 2 324 919 A	11/1998	GB	H03D	7/18	N/A
	AM21	JP 61-30821	02/1986	JP	H04B	1/10	No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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FORM PTO-1449 SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	APPLICANT David F. SORRELLS *et al.*	
	FILING DATE August 4, 2000	GROUP 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ22	JP 5-327356	12/1993	JP	H03D	7/00	No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

::ODMA\MHODMA\SKGF_DC1;94515;1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No. 2377
Sorrells *et al.*	Art Unit: 2634
Appl. No. 09/632,856	Examiner: Kim, Kevin
Filed: August 4, 2000	Atty. Docket: 1744.0630003
For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementation**	

Second Supplemental Information Disclosure Statement

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98. The numbering on this Second Supplemental Information Disclosure Statement is a continuation of the numbering in Applicants' Supplemental Information Disclosure Statement filed on June 9, 2003 in connection with the above-captioned application.

In addition to providing hard copies of the documents as required by applicable rules (see box 7 below), Applicants herewith provide a Compact Disc labeled "Disc 3" having stored thereon searchable electronic copies (in PDF format) of many of the documents listed on the PTO-1449. More specifically, the CD contains electronic copies of documents AG51-AI51, AA52-AI52, AA53-AI53, AA54-AG54, AK22, AL22, AM22, AJ23, AK23, AR57 and AN58-AR58. In addition, the CD contains electronic copies of documents AC46-AI46, AA47-AI47, AA48-AI48, AA49, AE49-AI49, AA50-AI50, AA51-AF51, AM13, AJ14-AM14, AJ15-AM15, AJ16-AM16, AJ17-AM17, AJ18-AM18, AJ19-AM19, AJ20-AM20, AJ21-AM21, AJ22, AQ51, AR51, AN52-AR52, AN53-AR53, AN54-AR54, AN55-AR55, AN56-AR56 and AN57-AQ57, all of which were cited in previous Information Disclosure Statements. Documents AH54, AI54, AA55-AI55, AA56-AE56 and AN59 have not yet been scanned. The file names on the CD correspond to the identifiers on the PTO-1449s. It is noted that the CD is being provided in addition to hard copies of the documents (as required by applicable rules) for the convenience of the Examiner.

Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

Applicants provide the following comments regarding the documents:

Document AH51 was cited in an Office Action in related U.S. Patent Application Serial No. 09/476,092, filed January 3, 2000, entitled "Analog Zero IF FM Decoder and Embodiments Thereof, Such as the Family Radio Service," directed to related subject matter. Also cited in the Office Action were U.S. Patent Nos. 5,600,680 and 5,606,731, which have already been cited in the present application in the Supplemental Information Disclosure Statement, filed June 9, 2003.

Documents AI51, AA52, AF52, AA55 and AI55 are co-owned patents which are directed to related subject matter.

Documents AB52, AE56, AN58-AP58 and AN59 were cited in Office Actions in related U.S. Patent Appl. No. 09/567,977, filed May 10, 2000, entitled, "Optical Down-converter Using Universal Frequency Translation Technology," directed to related subject matter.

Documents AE52 and AJ23 were cited in an Invitation to Pay Additional Fees in related PCT Appl. No. PCT/US01/43077, filed November 14, 2001, entitled "Method and Apparatus for a Parallel Correlator and Applications Thereof," directed to related subject matter.

Documents AG52-AI52 and AA53 were cited in an Office Action in related U.S. Patent Application No. 09/986,764, filed November 9, 2001, entitled "Method and Apparatus for Reducing DC Offsets in a Communication System," directed to related subject matter.

Documents AB53-AE53 were cited in an International Search Report in related PCT Application No. PCT/US02/35861, filed November 8, 2002, entitled "Method and Apparatus for Reducing DC Offsets in a Communication System," directed to related subject matter.

Documents AF53-AI53 and AA54-AC54 were cited in an Office Action in related U.S. Patent Application No. 09/476,093, filed January 3, 2000, entitled "Family Radio

System with Multi-Mode and Multi-Band Functionality," directed to related subject matter.

Documents AD54-AG54 were cited in an International Search Report in related PCT Application No. PCT/US03/16403, filed May 27, 2003, entitled "Method and Apparatus for DC Offset Removal in a Radio Frequency Communication Channel," directed to related subject matter.

Documents AH54 and AI54 were cited in an Office Action in related U.S. Patent Application No. 09/550,642, filed April 14, 2000, entitled "Method and System for Down-converting an Electromagnetic Signal, and Transforms for Same," directed to related subject matter.

Documents AB55-AF55 were cited in an Office Action in related U.S. Patent Application No. 09/548,923, filed April 13, 2000, entitled "Method and System for Frequency Conversion with Modulation Embodiments," directed to related subject matter. Also cited in the Office Action were U.S. Patent Nos. 6,091,940 and 6,353,735, which have already been cited in the present application in the Information Disclosure Statement, filed July 25, 2002.

Documents AG55 and AH55 were cited in an Office Action in related U.S. Patent Application No. 09/543,867, filed April 5, 2000, entitled "Automated Meter Reader Applications of Universal Frequency Translation," directed to related subject matter.

Documents AA56 and AB56 were cited in an Office Action in related U.S. Patent Application No. 10/317,181, filed December 12, 2002, entitled "Differential Frequency Down-Conversion Using Techniques of Universal Frequency Translation Technology," directed to related subject matter.

Documents AC56 and AD56 were cited in an Office Action in related U.S. Patent Application No. 10/317,165, filed December 12, 2002, entitled "Method and Apparatus for Reducing DC Offsets in Communication Systems Using Universal Frequency Translation Technology," directed to related subject matter.

Documents AK22-AM22, AA52, AB52 and AQ58 were cited in an International Search Report in related PCT Appl. No. PCT/US01/15555, filed May 16, 2001, entitled, "Apparatus, System, and Method for Down-Converting and Up-Converting Electromagnetic Signals," directed to related subject matter. Also cited the International Search Report were U.S. Patent Nos. 4,888,557, 5,454,007, 5,640,698 and 5,705,949, and PCT Publication No. WO 96/02977, which have already been cited in the present application in the Information Disclosure Statement, filed July 25, 2002.

Document AK23 was cited in an Office Action in related Japanese Patent Application No. 2000-577,764, filed June 21, 2000, entitled "Applications of Frequency Translation," directed to related subject matter.

The other documents in the PTO-1449 do not fall within the above categories.

This statement should not be construed as a representation that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below.

□ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this information disclosure statement.

■ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits. No statement or fee is required.

□ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

□ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

□ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

□ c. Attached is our PTO-2038 Credit Card Payment Form in the amount of ______ in payment of the fee under 37 C.F.R. § 1.17(p).

□ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. Enclosed find our Check No. ________ in the amount of $ _____ in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

□ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ 5. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.

■ 6. A concise explanation of the relevance of non-English language document AK23 appears below:

Document AK23 (JP 9-36664) appears to describe a frequency conversion circuit. A copy of the English-language abstract of document AK23 is enclosed as document AR58.

■ 7. Copies of documents AA56-AE56 and AN59 are enclosed. Copies of the remaining documents were submitted to the Patent Office in Information Disclosure Statements that comply with 37 C.F.R. § 1.98(a)-(c) in Application No. <u>09/525,615</u>, filed <u>March 14, 2000</u>, and Appl. No. <u>09/526,041</u>, filed <u>March 14, 2000</u>, which are both relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

It is respectfully requested that the Examiner initial and return a copy of the enclosed PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

Date: 1/23/04

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

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Sterne Kessler Goldstein Fox
ATTORNEYS AT LAW

August 19, 2004

WRITER'S DIRECT NUMBER:
(202) 772-8675
INTERNET ADDRESS:
JHELVEY@SKGF.COM

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

FILE COPY

Art Unit 2634

Re: U.S. Utility Patent Application
Appl. No. 09/632,856; Filed: August 4, 2000
For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementation**
Inventors: Sorrells *et al.*
Our Ref: 1744.0630003

Sir:

Transmitted herewith for appropriate action are the following documents:

1. SKGF Cover Letter;

2. Fee Transmittal (Form PTO/SB/17);

3. Third Supplemental Information Disclosure Statement;

4. Form PTO-1449 (<u>6</u> pages);

5. Return postcard; and

6. PTO-2038 Credit Card Payment Form for $<u>180.00</u> to cover:
$<u>180.00</u> for IDS Late Filing Surcharge.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

1100 New York Avenue, NW : Washington, DC 20005 : 202.371.2600 : 202.371.2540

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

J.H. Helvey

Jeffrey T. Helvey
Attorney for Applicants
Registration No. 44,757

JTH/agj
301413_1.DOC

Applicants:	Sorrells *et al.*	**Art Unit:**	2634
		Examiner:	Kim, Kevin
Application No.:	09/632,856	**Docket:**	1744.0630003
Filed:	August 4, 2000	**Atty:**	MQL/JTH
For:	**Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementation**		

When receipt stamp is placed hereon, the USPTO acknowledges receipt of the following documents:

1. SKGF Cover Letter;
2. Second Supplemental Information Disclosure Statement;
3. A list of the cited documents on Forms PTO-1449 (6 pages);
4. A compact Disc labeled "Disc 3" in PDF format (which contains electronic copies of the cited documents);
5. Copies of cited documents: AA56, AB56, AC56, AD56, AE56, AN59; and
6. Return postcard.

Please Date Stamp and Return to Our Courier

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 New York Avenue, NW
Washington, DC 20005-3934

FORM PTO-1449 SECOND SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	APPLICANTS Sorrells *et al.*	
	FILING DATE August 4, 2000	GROUP 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG51	6,230,000 B1	05/2001	Tayloe			
	AH51	5,483,695	01/1996	Pardoen			
	AI51	6,542,722 B1	04/2003	Sorrells *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						
	AK22	EP 0 643 477 A2 & A3	03/1995	EP			N/A
	AL22	EP 0 877 476 A1	11/1998	EP			N/A
	AM22	EP 0 977 351 A1	02/2000	EP			N/A

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN		
	AO		
	AP		
	AQ		
	AR	57	Tayloe, D., "A Low-noise, High-performance Zero IF Quadrature Detector/Preamplifier," *RF Design*, Primedia Business Magazines & Media, Inc., pp. 58, 60, 62 and 69 (March 2003).

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

FORM PTO-1449 SECOND SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	APPLICANTS Sorrells *et al.*	
	FILING DATE August 4, 2000	GROUP 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA52	6,560,301 B1	05/2003	Cook *et al.*			
	AB52	6,098,046	08/2000	Cooper *et al.*			
	AC52	5,564,097	10/1996	Swanke			
	AD52	5,898,912	04/1999	Heck *et al.*			
	AE52	4,660,164	04/1987	Leibowitz			
	AF52	6,580,902 B1	06/2003	Sorrells *et al.*			
	AG52	4,857,928	08/1989	Gailus *et al.*			
	AH52	5,389,839	02/1995	Heck			
	AI52	5,471,665	11/1995	Pace *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ23	WO 00/31659 A1	06/2000	PCT			N/A
	AK23	JP 9-36664	02/1997	JP			No
	AL						
	AM						

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	58	Dines, J.A.B., "Smart Pixel Optoelectronic Receiver Based on a Charge Sensitive Amplifier Design," *IEEE Journal of Selected Topics in Quantum Electronics*, IEEE, Vol. 2, No. 1, pp. 117-120 (April 1996).
	AO	58	Simoni, A. *et al.*, "A Digital Camera for Machine Vision," *20th International Conference on Industrial Electronics, Control and Instrumentation*, IEEE, pp. 879-883 (September 1994).
	AP	58	Stewart, R.W. and Pfann, E., "Oversampling and sigma-delta strategies for data conversion," *Electronics & Communication Engineering Journal*, IEEE, pp. 37-47 (February 1998).
	AQ	58	Rudell, J.C. *et al.*, "A 1.9-Ghz Wide-Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 32, No. 12, pp. 2071-2088 (December 1997).
	AR	58	English-language Abstract of Japanese Patent Publication No. 09-036664, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (February 7, 1997 - Date of publication of application).

EXAMINER	DATE CONSIDERED

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FORM PTO-1449 SECOND SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	APPLICANTS Sorrells *et al.*	
	FILING DATE August 4, 2000	GROUP 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA53	6,327,313 B1	12/2001	Traylor *et al.*			
	AB53	5,751,154	05/1998	Tsugai			
	AC53	5,793,817	08/1998	Wilson			
	AD53	6,225,848 B1	05/2001	Tilley *et al.*			
	AE53	6,313,685 B1	11/2001	Rabii			
	AF53	3,614,627	10/1971	Runyan *et al.*			
	AG53	3,940,697	02/1976	Morgan			
	AH53	4,016,366	04/1977	Kurata			
	AI53	4,045,740	08/1977	Baker			

FOREIGN PATENT DOCUMENTS

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	AJ						
	AK						
	AL						
	AM						

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	59	Simoni, A. *et al.*, "A Single-Chip Optical Sensor with Analog Memory for Motion Detection," *IEEE Journal of Solid-State Circtuits*, IEEE, Vol. 30, No. 7, pp. 800-806 (July 1995).
	AO		
	AP		
	AQ		
	AR		

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	APPLICANTS Sorrells *et al.*	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA54	4,115,737	09/1978	Hongu *et al.*			
	AB54	5,710,992	01/1998	Sawada *et al.*			
	AC54	5,790,587	08/1998	Smith *et al.*			
	AD54	4,740,675	04/1988	Brosnan *et al.*			
	AE54	5,483,600	01/1996	Werrbach			
	AF54	6,011,435	01/2000	Takeyabu *et al.*			
	AG54	6,321,073 B1	11/2001	Luz *et al.*			
	AH54	6,026,286	02/2000	Long			
	AI54	6,178,319 B1	01/2001	Kashima			

FOREIGN PATENT DOCUMENTS

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	APPLICANTS Sorrells *et al.*	
	FILING DATE August 4, 2000	GROUP 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA55	6,634,555 B1	10/2003	Sorrells *et al.*			
	AB55	3,736,513	05/1973	Wilson			
	AC55	4,488,119	12/1984	Marshall			
	AD55	4,633,510	12/1986	Suzuki *et al.*			
	AE55	5,369,789	11/1994	Kosugi *et al.*			
	AF55	5,416,449	05/1995	Joshi			
	AG55	5,438,329	08/1995	Gastouniotis *et al.*			
	AH55	6,611,569 B1	08/2003	Schier *et al.*			
	AI55	6,647,250 B1	11/2003	Bultman *et al.*			

FOREIGN PATENT DOCUMENTS

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	AA56	5,682,099	10/1997	Thompson *et al.*			
	AB56	6,094,084	07/2000	Abou-Allam *et al.*			
	AC56	6,067,329	05/2000	Kato *et al.*			
	AD56	6,516,185 B1	02/2003	MacNally			
	AE56	6,608,647 B1	08/2003	King			
	AF						
	AG						
	AH						
	AI						

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::ODMA\MHODMA\SKGF_DC1;219917;1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 2377
SORRELLS *et al.*	Art Unit: 2634
Appl. No.: 09/632,856	Examiner: Kim, Kevin
Filed: August 4, 2000	Atty. Docket: 1744.0630003
For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementation**	

Third Supplemental Information Disclosure Statement

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98. The numbering on this Third Supplemental Information Disclosure Statement is a continuation of the numbering in Applicants' Second Supplemental Information Disclosure Statement filed on January 23, 2004 in connection with the above-captioned application.

Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

Applicants provide the following comments regarding the documents:

Documents AL23, AI56, AA57, AB57, AO59, and AF61 were cited in an Office Action in related U.S. Patent Application No. 09/669,634, filed September 26, 2000, entitled "High Frequency Translator and Method of High Frequency Translation," directed to related subject matter. Also cited in said Office Action were U.S. Patent Nos. 6,049,706; 6,421,534; and 6,560,301, which have already been cited in the present application.

Documents AF56, AG56, AAC7, and AD57 are co-owned patents which are directed to related subject matter.

Documents AF56, AG56, AC57, AD57, and AI59 were cited in a Notice of Allowance in related U.S. Patent Application No. 09/838,387, filed April 20, 2001, entitled "Method and System for Down-Converting and Up-Converting an Electromagnetic Signal, and Transforms for Same," directed to related subject matter. Also cited in said Notice of Allowance were U.S. Patent Nos. 5,937,013; 6,061,551; and 6,647,250, which have already been cited in the present application.

Document AH56 was cited in an Office Action in related U.S. Patent Application No. 09/567,977, filed May 10, 2000, entitled "Optical Down-converter Using Universal Frequency Translation Technology," directed to related subject matter.

Documents AE57-AH57 were cited in an Office Action in related U.S. Patent Application No. 09/567,978, filed May 10, 2000, entitled "Carrier and Clock Recovery Using Universal Frequency Translation," directed to related subject matter. Also cited in said Office Action was U.S. Patent No. 5,937,013, which has already been cited in the present application.

Documents AI57 and AA58 were cited in a Notice of Allowance in related U.S. Patent Application No. 10/330,219, filed December 30, 2002, entitled "Methods and Systems for Down-Converting Electromagnetic Signals, and Applications Thereof," directed to related subject matter.

Documents AB58-AI58 and AA59-AD59 were cited in an Office Action in related U.S. Patent Application No. 09/566,188, filed May 5, 2000, entitled "Integrated Frequency Translation and Selectivity with Gain Control Functionality, and Applications Thereof," directed to related subject matter.

Documents AE59-AG59 were cited in an Office Action in related U.S. Patent Application No. 09/569,044, filed May 10, 2000, entitled "Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled by Universal Frequency Translation Technology," directed to related subject matter. Also cited in said Office Action were U.S. Patent Nos. 2,057,613; 2,241,078; 2,283,575; 2,358,152; 2,410,350; 2,451,430; 2,472,798; 4,653,117; and 5,241,561, which have already been cited in the present application.

Document AH59 was cited in an Office Action in related U.S. Patent Application No. 10/289,377, filed November 7, 2002, entitled "Method and Apparatus for Reducing DC Offsets in a Communication System," directed to related subject matter. Also cited in said Office Action were U.S. Pat. Nos. 5,471,665; 5,793,817; and 5,898,912, which have already been cited in the present application.

Documents AA60 and AB60 were cited in an Office Action in related U.S. Patent Application No. 09/525,185, filed March 14, 2000, entitled "Spread Spectrum Applications of Universal Frequency Translation Technology," directed to related subject matter. Also cited in said Office Action were U.S. Patent Nos. 5,339,459; 5,369,789; and 5,937,013, which have already been cited in the present application.

Documents AC60-AF60 were cited in an Office Action in related U.S. Patent Application No. 09/569,045, filed May 10, 2000, entitled "Methods and Apparatuses Relating to a Universal Platform Module and Enabled by Universal Frequency Translation Technology," directed to related subject matter. Also cited in said Office Action were U.S. Patent Nos. 5,339,459 and 5,557,641, which have already been cited in the present application.

Documents AG60-AI60 were cited in an Office Action in related U.S. Patent Application No. 09/590,955, filed June 9, 2000, entitled "Phase-Shifting Applications of Universal Frequency Translation," directed to related subject matter. Also cited in said Office Action was U.S. Patent No. 5,339,459, which has already been cited in the present application in a previous Information Disclosure Statement.

Documents AA61-AC61 were cited in an Office Action in related U.S. Patent Application No. 09/550,642, filed April 14, 2000, entitled, "Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same," directed to related subject matter.

Documents AD61 and AE61 were cited in an Office Action in related U.S. Patent Application No. 10/317,165, filed December 12, 2002, entitled, "Method and Apparatus for Reducing DC Offsets in Communication Systems Using Universal Frequency Translation Technology," directed to related subject matter.

The other documents in the PTO-1449 do not fall within the above categories.

It is noted that some of these documents could be classified in more than one of the above categories.

This statement should not be construed as a representation that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below.

☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this information disclosure statement.

☐ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits. No statement or fee is required.

☒ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

   ☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☒ c. Attached is our PTO-2038 Credit Card Payment Form in the amount of **$180.00** in payment of the fee under 37 C.F.R. § 1.17(p).

☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. Enclosed find our PTO-2038 Credit Card Payment Form in the amount of $_________ in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ 5. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.

☒ 6. A concise explanation of the relevance of the non-English language documents appears below:

Document AL23 (DE 196 48 915 A1) appears to describe a process of frequency conversion. An English-language translation of document AL23 is enclosed as document AO59.

☐ 7. Copies of the documents are submitted herewith.

☒ 8. Copies of the documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No 09/525,615, filed March 14, 2000, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

☐ 9. No copies of U.S. patents and patent application publications cited on the attached Form PTO-1449 are submitted in accordance with 1276 OG 55 because this application was filed after June 30, 2003.

☒ 10. It is expected that the examiner will review the prosecution and cited art in the parent application nos. 09/525,615 and 09/526,041 in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution history has been reviewed in connection with the present application.

It is respectfully requested that the Examiner initial and return a copy of the enclosed PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

JTH Helvey

Jeffrey T. Helvey
Attorney for Applicants
Registration No. 44,757

Date: 8/19/04

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

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OIPE
DEC 15 2004
PATENT & TRADEMARK OFFICE

Applicants:	Sorrells *et al.*	**Due Date:**	NONE
		Art Unit:	2634
		Confirmation No.:	2377
Application No.:	09/632,856	**Examiner:**	Kim, Kevin
Filed:	August 4, 2000	**Docket:**	1744.0630003
For:	**Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementation**	**Atty:**	JTH

When receipt stamp is placed hereon, the USPTO acknowledges receipt of the following documents:

1. SKGF Cover Letter;
2. Fee Transmittal (Form PTO/SB/17);
3. Third Supplemental Information Disclosure Statement;
4. Form PTO-1449 (6 pages);
5. Return postcard; and
6. PTO-2038 Credit Card Payment Form for $180.00 to cover: $180.00 for IDS Late Filing Surcharge.

OIPE JC174
AUG 19 2004
PATENT & TRADEMARK OFFICE

Please Date Stamp and Return to Our Courier

Sterne, Kessler, Goldstein & Fox
1100 New York Avenue, NW
Washington, DC 20005

FORM PTO-1449 THIRD SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	INVENTORS SORRELLS *et al.*	
	FILING DATE August 4, 2000	ART UNIT 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF56	6,687,493 B1	02/2004	Sorrells *et al.*			
	AG56	6,694,128 B1	02/2004	Sorrells *et al.*			
	AH56	6,031,217	02/2000	Aswell *et al.*			
	AI56	5,955,992	09/1999	Shattil			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL23	DE 196 48 915 A1	06/1998	DE			Yes (Doc. AO59)
	AM						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN		
	AO	59	English Translation of German Patent Publication No. DE 196 48 915 A1, 10 pages.
	AP		
	AQ		
	AR		

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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FORM PTO-1449 THIRD SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	INVENTORS SORRELLS *et al.*	
	FILING DATE August 4, 2000	ART UNIT 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA57	5,999,561	12/1999	Naden *et al.*			
	AB57	6,686,879 B2	02/2004	Shattil			
	AC57	6,704,549 B1	03/2004	Sorrells *et al.*			
	AD57	6,704,558 B1	03/2004	Sorrells *et al.*			
	AE57	5,490,176	02/1996	Peltier			
	AF57	5,970,053	10/1999	Schick *et al.*			
	AG57	6,078,630	06/2000	Prasanna			
	AH57	6,600,911 B1	07/2003	Morishige *et al.*			
	AI57	5,179,731	01/1993	Tränkle *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

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FORM PTO-1449 THIRD SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	INVENTORS SORRELLS *et al.*	
	FILING DATE August 4, 2000	ART UNIT 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA58	5,589,793	12/1996	Kassapian			
	AB58	4,510,467	04/1985	Chang *et al.*			
	AC58	4,772,853	09/1988	Hart			
	AD58	4,972,436	11/1990	Halim *et al.*			
	AE58	5,012,245	04/1991	Scott *et al.*			
	AF58	5,422,909	06/1995	Love *et al.*			
	AG58	5,440,311	08/1995	Gallagher *et al.*			
	AH58	5,926,513	07/1999	Suominen *et al.*			
	AI58	5,995,030	11/1999	Cabler			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM						Yes No

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FORM PTO-1449 THIRD SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	INVENTORS SORRELLS *et al.*	
	FILING DATE August 4, 2000	ART UNIT 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA59	6,047,026	04/2000	Chao *et al.*			
	AB59	6,049,573	04/2000	Song			
	AC59	6,076,015	06/2000	Hartley *et al.*			
	AD59	6,144,331	11/2000	Jiang			
	AE59	5,058,107	10/1991	Stone *et al.*			
	AF59	5,757,858	05/1998	Black *et al.*			
	AG59	6,531,979 B1	03/2003	Hynes			
	AH59	6,018,262	01/2000	Noro *et al.*			
	AI59	4,761,798	08/1988	Griswold, Jr. *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

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EXAMINER	DATE CONSIDERED

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FORM PTO-1449 THIRD SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	INVENTORS SORRELLS *et al.*	
	FILING DATE August 4, 2000	ART UNIT 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA60	5,982,315	11/1999	Bazarjani *et al.*			
	AB60	6,459,721 B1	10/2002	Mochizuki *et al.*			
	AC60	6,151,354	11/2000	Abbey			
	AD60	6,169,733 B1	01/2001	Lee			
	AE60	6,363,262 B1	03/2002	McNicol			
	AF60	6,697,603 B1	02/2004	Lovinggood *et al.*			
	AG60	5,282,222	01/1994	Fattouche *et al.*			
	AH60	5,949,827	09/1999	DeLuca *et al.*			
	AI60	6,014,176	01/2000	Nayebi *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
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	AL						Yes No
	AM						Yes No

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FORM PTO-1449 THIRD SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	INVENTORS SORRELLS *et al.*	
	FILING DATE August 4, 2000	ART UNIT 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA61	5,678,226	10/1997	Li *et al.*			
	AB61	5,760,632	06/1998	Kawakami *et al.*			
	AC61	6,160,280	12/2000	Bonn *et al.*			
	AD61	5,481,570	01/1996	Winters			
	AE61	5,745,846	04/1998	Myer *et al.*			
	AF61	5,345,239	09/1994	Madni *et al.*			
	AG						
	AH						
	AI						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
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	AM						Yes No

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
Sorrells *et al.*
Appl. No.: 09/632,856
Filed: August 4, 2000
For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementation**

Confirmation No.: 2377
Art Unit: 2634
Examiner: Kim, Kevin
Atty. Docket: 1744.0630003

Fourth Supplemental Information Disclosure Statement

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98. The numbering on this Fourth Supplemental Information Disclosure Statement is a continuation of the numbering in Applicants' Third Supplemental Information Disclosure Statement filed on August 19, 2004 in connection with the above-captioned application.

Applicants have listed publication dates on the attached Form PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

Applicants provide the following comments regarding the documents:

Documents AP59 and AE63 were cited in an Office Action, mailed September 21, 2004, in related U.S. Patent Application No. 09/567,977, filed May 10, 2000, entitled "Optical Down-converter Using Universal Frequency Translation," directed to related subject matter.

Document AG61 was cited in an Office Action, mailed August 17, 2004, in related U.S. Patent Application No. 09/476,093, filed January 3, 2000, entitled "Communication System Method With Multi-Mode and Multi-Band Functionality and Embodiments Thereof, Such as the Family Radio Service," directed to related subject matter.

Documents AH61 and AI61 were cited in a Notice of Allowance, mailed August 18, 2004, in related U.S. Patent Application No. 09/525,615, filed March 14, 2000, entitled "Method, System, and Apparatus for Balanced Frequency Up-conversion of a Baseband Signal and 4-Phase Receiver and Transceiver Embodiments," directed to related subject matter.

Documents AA62-AF62, mailed August 25, 2004, were cited in an Office Action in related U.S. Patent Application No. 10/290,323, filed November 8, 2002, entitled "Method and Apparatus for DC Offset Removal in a Radio Frequency Communication Channel," directed to related subject matter.

Documents AG62-AI62 were cited in an Office Action, mailed September 8, 2004, in related U.S. Patent Application No. 09/632,857, filed August 4, 2000, entitled "Wireless Local Area Network (WLAN) Technology and Applications Including Techniques of Universal Frequency Translation," directed to related subject matter.

Documents AA63-AD63 were cited in an Office Action, mailed September 8, 2004, in related U.S. Patent Application No. 09/986,764, filed November 9, 2001, entitled "Method and Apparatus for Reducing DC Offsets in a Communication System," directed to related subject matter.

Documents AF63-AI63 were cited in a Notice of Allowance, mailed September 27, 2004, in related U.S. Patent Application No. 09/987,193, filed November 13, 2001, entitled "Method and Apparatus for a Parallel Correlator and Applications Thereof," directed to related subject matter.

Document AA64 was cited in an Office Action, mailed September 29, 2004, in related U.S. Patent Application No. 09/632,857, filed August 4, 2000, entitled " Wireless Local Area Network (WLAN) Technology and Applications Including Techniques of Universal Frequency Translation," directed to related subject matter.

This statement should not be construed as a representation that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below.

☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this information disclosure statement.

☐ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed within three months of the date of filing of a national application other than a continued prosecution application (CPA), OR within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, OR before the mailing date of a first Office Action on the merits OR before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.

☐ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ c. Attached is our PTO-2038 Credit Card Payment Form in the amount of ____________ in payment of the fee under 37 C.F.R. § 1.17(p).

☒ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. Enclosed find our PTO-2038 Credit Card Payment Form in the amount of **$180.00** in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

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☐ 5. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.

☐ 6. A concise explanation of the relevance of non-English language documents appears below:

☒ 7. A copy of document AP59 is submitted. However, in accordance with 37 C.F.R. § 1.98(a)(2), no copies of U.S patents and patent application publications cited on the attached Form PTO-1449 are submitted.

☐ 8. Copies of the documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No.__________, filed ____________, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

☐ 9. It is expected that the examiner will review the prosecution and cited art in the parent application no. _______, filed ______, and indicate in the next communication from the office that the art cited in the earlier prosecution histories have been reviewed in connection with the present application.

It is respectfully requested that the Examiner initial and return a copy of the enclosed Form PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

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OIPE JC177
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November 12, 2004

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FILE COPY

Art Unit 2634

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Re: U.S. Utility Patent Application
Application No. 09/632,856; Filed: August 4, 2000
For: **Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementation**
Inventors: Sorrells *et al.*
Our Ref: 1744.0630003

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Fee Transmittal (Form PTO/SB/17);

2. Fourth Supplemental Information Disclosure Statement;

3. Form PTO-1449 (4 pages);

4. Copy of (1) cited document (Document No. AP59);

5. Return postcard; and

6. PTO-2038 Credit Card Payment Form for $180.00 to cover:
$180.00 for submission of an Information Disclosure Statement.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Jeff Helvey

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JTH/agj
333749_1.DOC

OIPE JC177
DEC 1 5 2004
PATENT & TRADEMARK OFFICE

Applicants:	Sorrells *et al.*	**Due Date:**	NONE
		Art Unit:	2634
		Confirmation No.:	2377
Application No.:	09/632,856	**Examiner:**	Kim, Kevin
Filed:	August 4, 2000	**Docket:**	1744.0630003
For:	**Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementation**	**Atty:**	JTH

When receipt stamp is placed hereon, the USPTO acknowledges receipt of the following documents:

1. SKGF Cover Letter;
2. Fee Transmittal (Form PTO/SB/17);
3. Fourth Supplemental Information Disclosure Statement;
4. Form PTO-1449 (4 pages);
5. Copy of (1) cited document (Document No. AP59);
6. Return postcard; and
7. PTO-2038 Credit Card Payment Form for $180.00 to cover: $180.00 for submission of an Information Disclosure Statement.

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Please Date Stamp and Return to Our Courier

Sterne, Kessler, Goldstein & Fox
1100 New York Avenue, NW
Washington, DC 20005

FORM PTO-1449	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
FOURTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	INVENTORS Sorrells *et al.*	
	FILING DATE August 4, 2000	ART UNIT 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG61	4,132,952	01/1979	Hongu *et al.*			
	AH61	5,260,973	11/1993	Watanabe			
	AI61	6,307,894 B2	10/2001	Eidson *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN		
	AO		
	AP	59	Deboo, Gordon J., *Integrated Circuits and Semiconductor Devices*, 2nd Edition, McGraw-Hill, Inc., pp. 41-45 (1977).
	AQ		
	AR		

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

330642_1.DOC

FORM PTO-1449 FOURTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0630003	APPLICATION NO. 09/632,856
	INVENTORS Sorrells *et al.*	
	FILING DATE August 4, 2000	ART UNIT 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA62	4,441,080	04/1984	Saari			
	AB62	4,873,492	10/1989	Myer			
	AC62	5,697,074	12/1997	Makikallio *et al.*			
	AD62	5,784,689	07/1998	Kobayashi			
	AE62	6,335,656 B1	01/2002	Goldfarb *et al.*			
	AF62	6,690,232 B2	02/2004	Ueno *et al.*			
	AG62	5,636,140	06/1997	Lee *et al.*			
	AH62	6,366,622 B1	04/2002	Brown *et al.*			
	AI62	6,600,795 B1	07/2003	Ohta *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM						Yes No

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA63	4,250,458	02/1981	Richmond *et al.*			
	AB63	5,760,629	06/1998	Urabe *et al.*			
	AC63	6,084,465	07/2000	Dasgupta			
	AD63	6,204,789 B1	03/2001	Nagata			
	AE63	6,064,054	05/2000	Waczynski *et al.*			
	AF63	5,218,562	06/1993	Basehore *et al.*			
	AG63	5,239,496	08/1993	Vancraeynest			
	AH63	5,896,304	04/1999	Tiemann *et al.*			
	AI63	6,005,903	12/1999	Mendelovicz			

FOREIGN PATENT DOCUMENTS

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA64	5,834,979	11/1998	Yatsuka			
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						

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	AM						Yes No

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