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[54] **SUBHARMONIC QUADRATURE SAMPLING RECEIVER AND DESIGN**

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[52] **U.S. Cl.** **375/340**; 375/376

[58] **Field of Search** 375/340, 342, 375/373, 376, 326, 229, 325, 324

[56] **References Cited**

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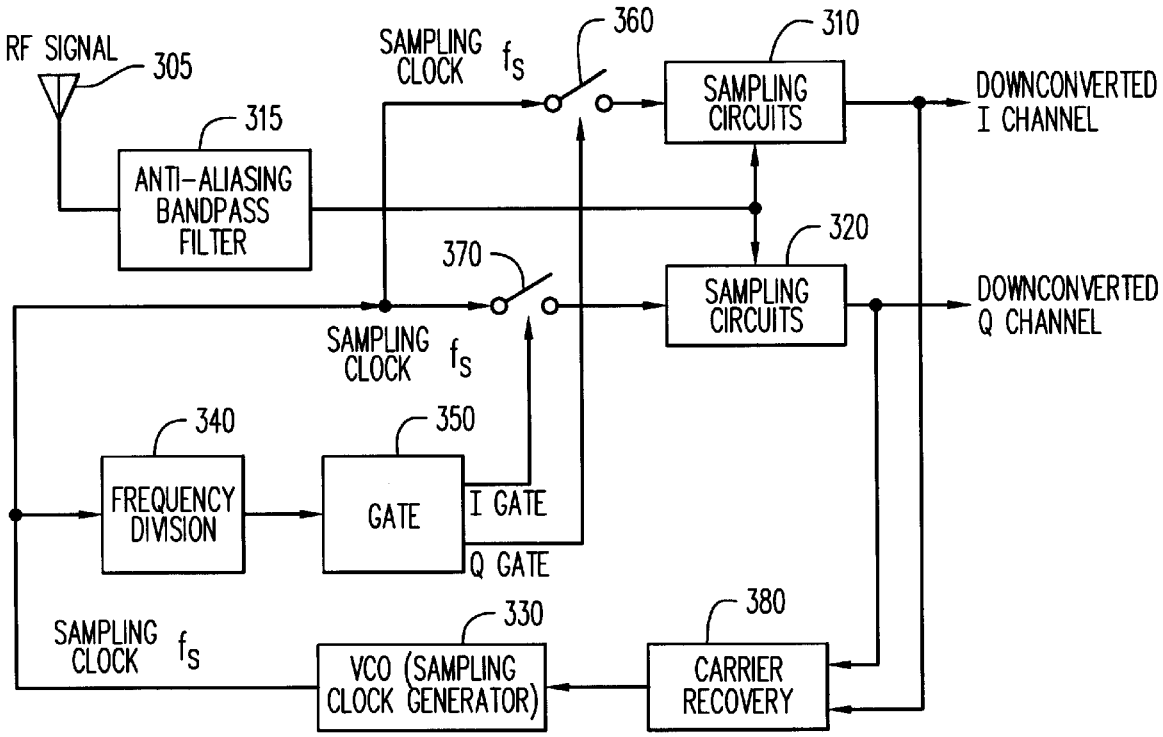
[57] **ABSTRACT**

A receiver for down-converting a modulated carrier into its in-phase (I) and quadrature (Q) components for further processing is proposed. This is accomplished using a sampling method in which the signal is sampled directly using a sampling circuit which is driven by a single sampling clock frequency substantially lower than the carrier frequency while allowing the I and Q components to be precisely obtained. Each of the signal samples comprises sub-samples taken successively which represent the in-phase, quadrature, negative in-phase and negative quadrature components of the signal. The negative components permit flexible application of the invention in several modes, including differential mode for the removal of common-mode noise. The invention is useful because it provides an integrated circuit means for precisely obtaining I and Q components of a very high frequency modulated carrier. This greatly eases the difficulty of implementing receiver architectures such as direct down-conversion or low-IF receivers, which permit on-chip integration of traditionally difficult-to-integrate components such as IF filters and VCO circuits while eliminating the need for image-rejection filters.

21 Claims, 2 Drawing Sheets



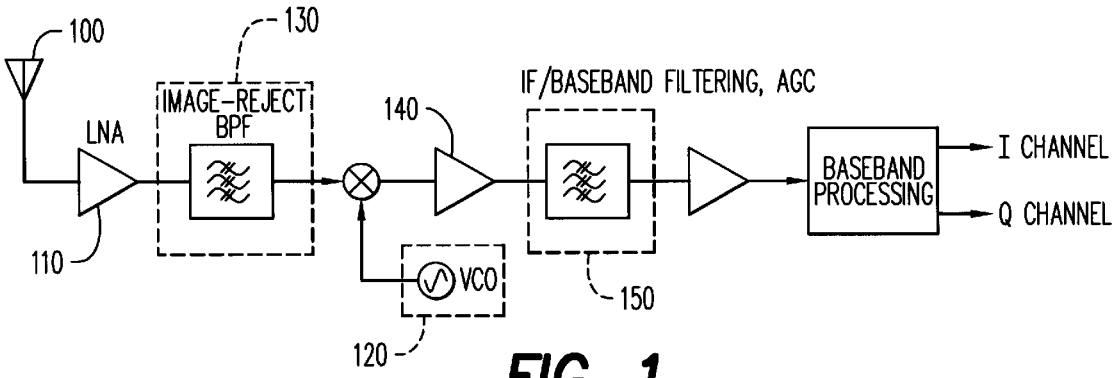


FIG. 1

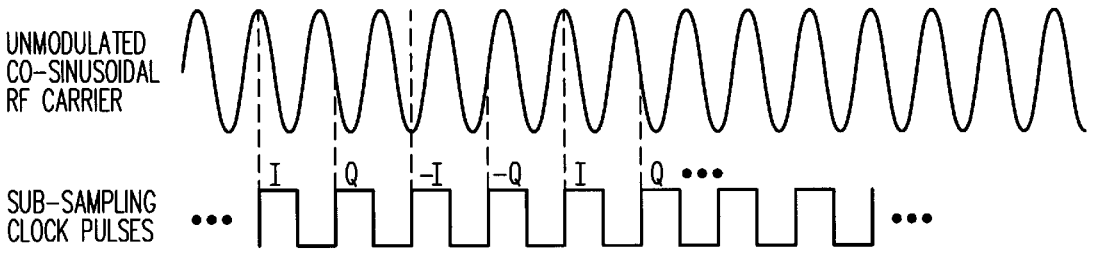


FIG. 2A

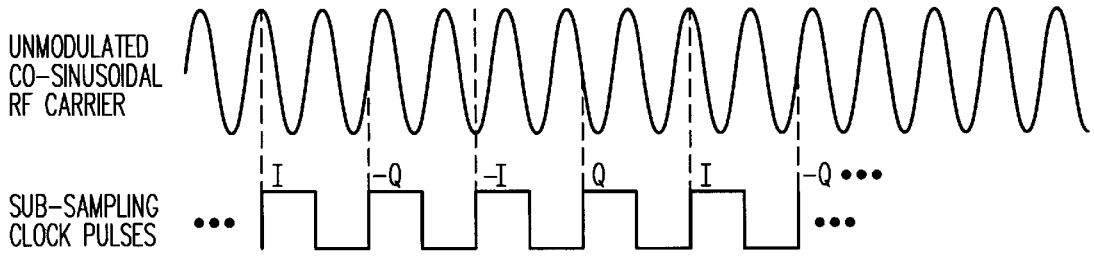


FIG. 2B

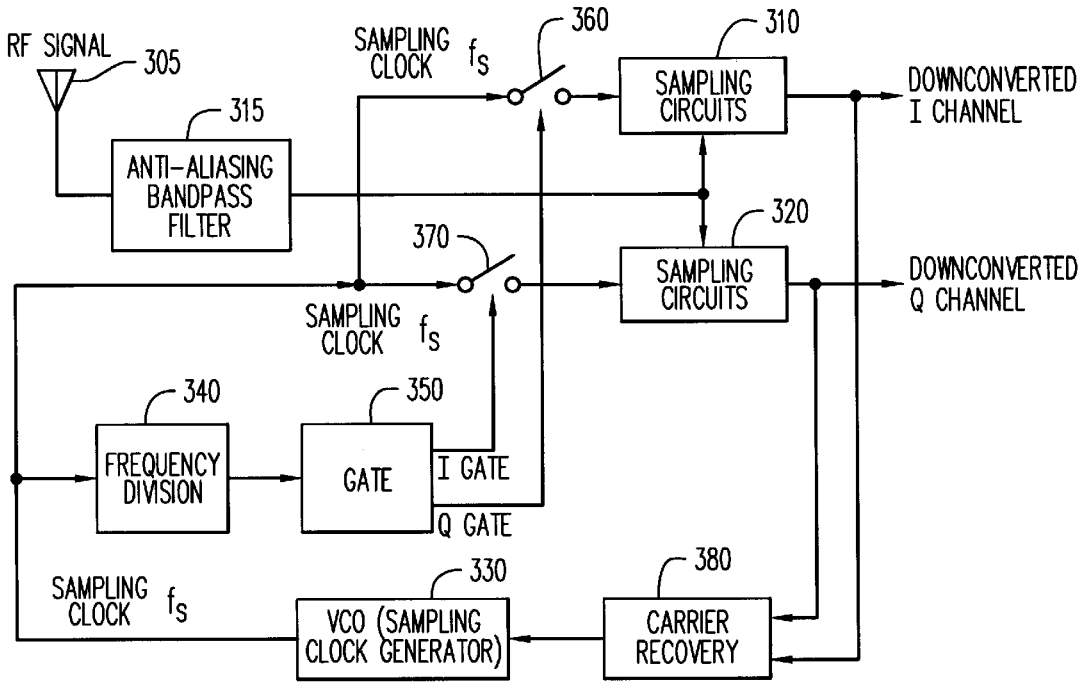


FIG. 3

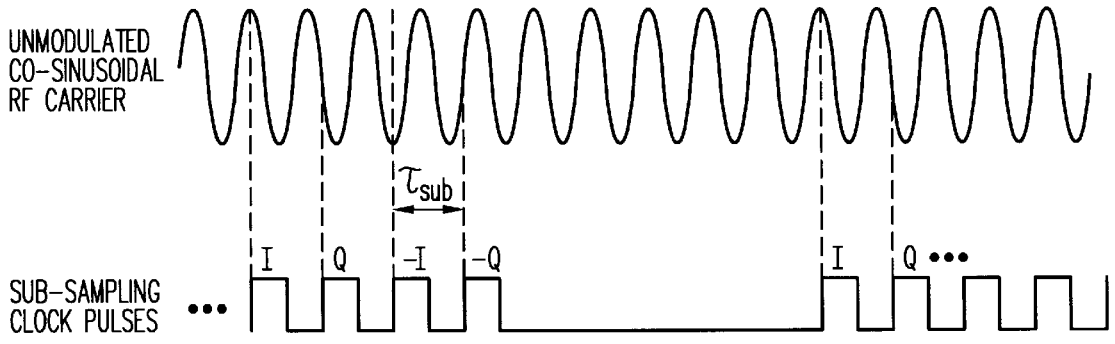


FIG. 4

SUBHARMONIC QUADRATURE SAMPLING RECEIVER AND DESIGN

FIELD OF THE INVENTION

The present invention relates to high-speed receivers for narrow-band communication systems. In particular it relates to high speed receivers which perform quadrature demodulation by sub-harmonic sampling of incoming information carrying RF signals. It also relates to a method for accurately separating the in-phase (I) and quadrature (Q) components of a modulated signal.

BACKGROUND OF THE INVENTION

In modern wireless communication systems, it is the task of the receiver to recover with high sensitivity and accuracy baseband signal data or messages which have been transmitted or broadcast by way of modulation on an radio frequency (RF) carrier. With the advent and popularity of mobile hand-held communication systems which operate in the gigahertz region, it is the goal of communication engineers to monolithically integrate the complete high-speed receiver circuit onto a single integrated circuit (IC) chip, the so-called single-chip receiver, so that very light weight handsets can be made available at an affordable price. Indeed, studies of handheld portable and mobile technologies indicate that cost savings by integration alone are in the region of 20–30%. Apart from the direct benefits of size and cost reduction, the benefit associated with the reduction in power consumption, e.g. heat dissipation and battery operation time, is also considerable.

There are however major hurdles which lie on the way to monolithic integration of digital receivers. Firstly, conventional high frequency receivers comprises a large number of discrete components for radio frequency (RF) signal processing. These components often introduce parasitics and other unknowns which are much less repeatable and predictable than circuits made from the IC process. Individual trimming and tuning of such components which are required to make up for the parasitic and other unknown effects further increase costs. On-chip integration of all such components would thus appear to provide an obvious solution. In addition, reduction of off-chip components also minimises the number of power-hungry drivers which are needed to overcome packaging and interconnect parasitics. However, adaptation of current technologies to integrating some of these passive components on-chip is expensive and requires a change of process which requires money and time.

Secondly, monolithic integration of a high speed digital receiver means that high-speed, low-noise small-signal front-end circuitries and high-density, low-power analogue and digital baseband processing circuitries must be put close together. Finding an integrated circuit technology with the right balance of cost and performance is not an easy compromise.

RECEIVER DESIGNS

Heterodyne Receiver

The heterodyne receiver design, as illustrated in FIG. **1**, is the most widely used topology for handsets for mobile communication systems. In this design, the RF signal received by the antenna **100** of the receiver is firstly amplified by a low-noise amplifier **110** which determines largely the overall noise figure of the complete receiver system. The amplified signal is then down-converted to a fixed intermediate frequency (IF) which is characteristic of the system for further processing. Down-conversion is usually performed

by mixing the received RF signal with a pure sinusoidal signal produced by a tunable local oscillator **120** (LO). The local oscillator frequency (f_{LO}) is chosen so that the IF, LO, RF frequencies are related by the formula:

$$f_{IF}=|f_{LO}-f_{RF}|$$

After the down conversion, the IF signal is further amplified by amplifier **140**, filtered by a highly selective IF filter **150** and processed until the embedded signal data is finally recovered.

From the formula above, it is clear that an RF signal which is present at a frequency $f_{LO}+f_{IF}$ as well as one which is present at a frequency $f_{LO}-f_{IF}$ will both be down converted to the IF. In typical applications, only one of these is the desired signal, while the other undesired RF signal is referred to as the "image" signal. To avoid receiving the undesirable image signal, an image-rejection filter **130** which substantially suppresses the image signal is always introduced before the mixer stage. To achieve high image rejection, a high performance image rejection filter must be used. Alternatively, a relatively high IF frequency may be chosen so that the stringent requirements on the image rejection filters may be lessened. Indeed, IF frequencies in the range of 10–100 MHz are quite common. Nevertheless, RF and IF filters are indispensable in such receivers if high performance is to be attained.

One of the greatest challenge in achieving monolithic heterodyne receiver design is the on-chip integration of high performance RF and IF filters using commercially available integrated circuit processing technology. In practice, most RF and IF filters have to be realised by means of off-chip discrete components.

Homodyne Receiver

Another commonly known alternative receiver topology which may be used is the homodyne, or direct conversion, receiver design. In this design, the LO and RF carrier frequency are identical and the IF frequency is therefore zero. When the RF signal is mixed with the LO signal, baseband signal is directly obtained and the problem of image signal is not present.

While the conventional direct conversion approach looks promising, it has several drawbacks which adversely limit its performance:

1) the weak RF signal is shifted directly into a noisy DC environment where DC drift, 1/F noise and other low-frequency noise exist. These adverse conditions put a heavy demand on the quality of amplification and the dynamic range provided by the RF circuitries,
2) non-linearity of mixer circuits causes intermodulation distortion of the received signal which means that a highly linear mixer is required,
3) local oscillator signal leakage can jam the receiver since the LO and RF frequency are the same, and
4) very accurate I and Q demodulation at RF is required to recover any signal which is asymmetric about the carrier, including a broad class of signals such as single-sideband or digitally phase-modulated signals. Imbalances in the phase and amplitude of I and Q conversion produce DC drift which will cause particular problems in systems where the baseband modulation, e.g. GMSK, contains energy at or near DC.

Low-IF-Heterodyne Receiver

Another alternative approach is the low-IF heterodyne design which is a modified version of the heterodyne receiver relying on high precision image-reject mixers which greatly reduces the demand on an image-reject filter. Combination of a low IF with high-precision image-reject

mixers means that the resulting IF signal can be easily processed by low-frequency on-chip filtering without the need of off-chip filters which are necessary for high-IF systems.

However, it is well known that if image-reject mixers are to achieve good image rejection, they must have very precise I and Q phase and amplitude matching. For example, a 40 dB image rejection would typically require a phase and amplitude matching of 1 degree and 0.2 dB respectively. The image rejection requirements of 60–70 dB in Global System of Mobile Communication (GSM) mean that an even higher degree of matching precision is required. In the past, such low-IF systems have not been considered practicable since image-reject mixers assembled with hybrid mounted components cannot deliver such precision without tuning. Furthermore, it is also difficult to integrate these components on-chip.

Advances in circuit design and IC technology in the past decade have mitigated many of the problems associated with the homodyne or low-IF systems. For example, increased levels of integration at RF permits high gain amplifiers and AGC circuits to be implemented on-chip, compensating mixer noise at baseband. Adequate isolation between mixer and the RF section combined with shielding alleviates the problem of LO jamming. The imbalances between the I and Q component offsets can be corrected using digital signal processing techniques which were not available a decade ago. However, mixer design remains a challenging issue particularly because of the inherently non-linear nature of their function, which makes their performance sensitive to spurious response.

To circumvent the difficulties surrounding the design of a high-performance high-frequency image-reject mixer suitable for homodyne or low-IF receivers, it is the object of the present invention to provide a high performance quadrature demodulation receiver which performs signal mixing by way of direct sampling of the RF signal which demodulates the signal accurately to the I and Q components. This invention makes possible full utilization of the advantages of linear switches which are readily available in CMOS technology.

This mixing and sampling technique is further refined by applying subharmonic sampling, i.e., sampling below the Nyquist rate, by relying on the fact that the baseband information signals are usually of a narrowband nature. This approach is partly based on the well known principle that down-conversion can be achieved by sampling a modulated carrier at a sub-harmonic frequency. When the sampling frequency is twice the modulation bandwidth, direct-conversion is achieved.

By deliberately under-sampling the RF signal, the receiver circuit is capable of capturing the narrowband signal variation and thereby downconverting the RF signal without a high-power and high bandwidth system. Naturally, pre-mixer anti-aliasing filter would be necessary to mitigate the wideband noise which would otherwise be aliased into an output of half the sample rate.

This sub-harmonic sampling techniques is applicable to both the homodyne and low-IF heterodyne designs. The two major advantages of this approach are firstly that the LO (i.e. the sampling frequency) and RF frequencies are now different, alleviating greatly the LO jamming problem. Secondly, because of the lower LO frequencies, low-speed supporting LO circuits such as oscillators using high-Q resonators, and phase-locking circuits using high Q resonators can be used, making possible many interesting low-power designs.

SUMMARY OF THE INVENTION

According to the present invention, there is provided a quadrature demodulation receiver for narrow-band communication systems comprising means for directly sampling an incoming signal which is modulated on a radio-frequency carrier at a sampling frequency which can be substantially lower than the carrier frequency to demodulate said signal into its in-phase and quadrature components, wherein said sampling means comprises means for obtaining main samples each of which comprises a plurality of sub-samples which are separated by a fixed time delay and which represent the in-phase and quadrature signal components taken for that sampling period.

Preferably, the said sampling means comprises means for firstly locking the in-phase sample to a sub-harmonic of the carrier frequency in a manner similar to conventional coherent receivers, and wherein the sub-samples are then taken at instants which correspond substantially to the in-phase and quadrature sample of the carrier frequency.

Preferably, the said sampling means comprises means for taking four sub-samples which represent the in-phase (I), the quadrature (Q), negative of the in-phase (−I) and negative of the quadrature (−Q)components. Naturally, the components need not be arranged in such an order.

In a preferred embodiment, the time delay, $\tau_{sub.}$, between successive sub-samples within the same sample is substantially equal to five quarters of the period of the un-modulated carrier frequency, i.e. $\tau_{sub.}=(5/4)\tau_{RF}$. Preferably, the time delay, τ_{sub}, between successive sub-samples within the same sample is substantially equal to τ_{RF} (N+¼), where τ_{RF} is the period of the un-modulated carrier frequency and N is a non-zero natural number.

Preferably, the time delay, $\tau_{sub.}$, between successive sub-samples within the same sample is substantially equal to $\tau_{RF}(N+(2M+1)/4)$, where τ_{RF} is the period of the un-modulated carrier frequency, N is a non-zero natural number and M is a natural number including zero.

Preferably, the sampling frequency is substantially equal to the carrier frequency divided by (4N+2M+1) where N is any natural number and M is any natural number including zero.

Preferably, the sampling frequency is also substantially equal to the carrier frequency divided by (4N+2M+K+1), where N, M and K are natural numbers and N is non zero.

In another preferred embodiment, the sampling frequency is equal to the sum of the carrier (RF) and intermediate (IF) frequency divided by the factor (4N+2M+1) where N is any natural number and M is any natural number including zero.

According to another aspect of the present invention, there is provided a direct sub-harmonic sampling method for quadrature demodulation for receivers for communication systems comprising demodulating an incoming narrow-band modulated signal on a carrier frequency into its in-phase and quadrature components by direct sampling, wherein said sampling is performed at a sampling frequency which is substantially lower than the carrier frequency, and comprising obtaining main samples each of which comprises a plurality of sub-samples which are separated by a fixed time delay, wherein said sub-samples represent the in-phase and quadrature signal components taken for that sampling period.

Preferably, the sampling is performed by first locking or tuning the in-phase sampling clock to a subharmonic of the carrier frequency in a manner similar to conventional coherent receivers (e.g. with a PLL or closed loop). However, the

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