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United States Patent [19]

Schiltz et al.

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[54] **HIGH SPEED SAMPLE AND HOLD CIRCUIT AND RADIO CONSTRUCTED THEREWITH**

[75] Inventors: **Thomas E. Schiltz**, Chandler; **Carl R. Nuckolls**, Fountain Hills, both of Ariz.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **985,477**

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[51] **Int. Cl.**[5] **H04B 1/28**; H03K 5/159

[52] **U.S. Cl.** **455/333**; 455/313; 455/318; 307/353

[58] **Field of Search** 455/313, 318, 323, 319, 455/343, 333, 334, 316; 307/352, 353; 328/151

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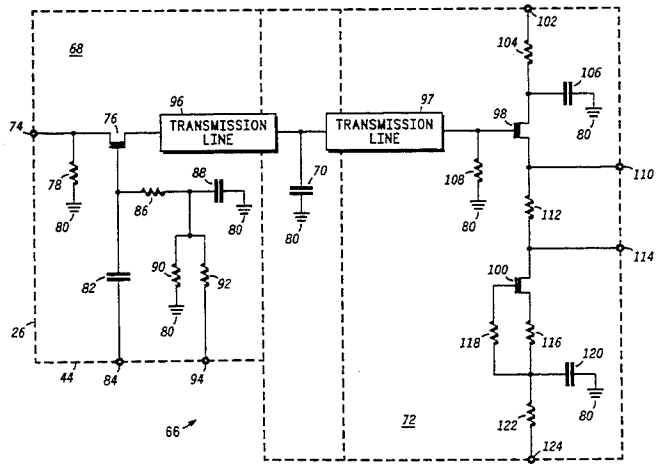
Primary Examiner—Reinhard J. Eisenzopf
Assistant Examiner—Nguyen Vo
Attorney, Agent, or Firm—Frederick M. Fliegel; Robert M. Handy

[57] **ABSTRACT**

A sample and hold circuit is formed within an integrated circuit and has a small, substantially linear hold capacitance. The circuit includes a sampling switch, a hold capacitor, and a buffer amplifier. The buffer amplifier includes a common drain FET and a constant current source FET. The common drain FET provides an input which couples to the hold capacitor. The constant current FET isolates the source of the common drain FET from ground. The sample and hold circuit may be used as a wide bandwidth mixer. In a radio application, a pulse generator provides a stream of pulses in which the sampling rate times an integer number equals the RF frequency minus the IF frequency. The width of the sampling pulse is less than the period of an RF signal. In an oscillator application, the sample and hold circuit operates as a mixer in a frequency multiplying phase locked loop.

17 Claims, 3 Drawing Sheets



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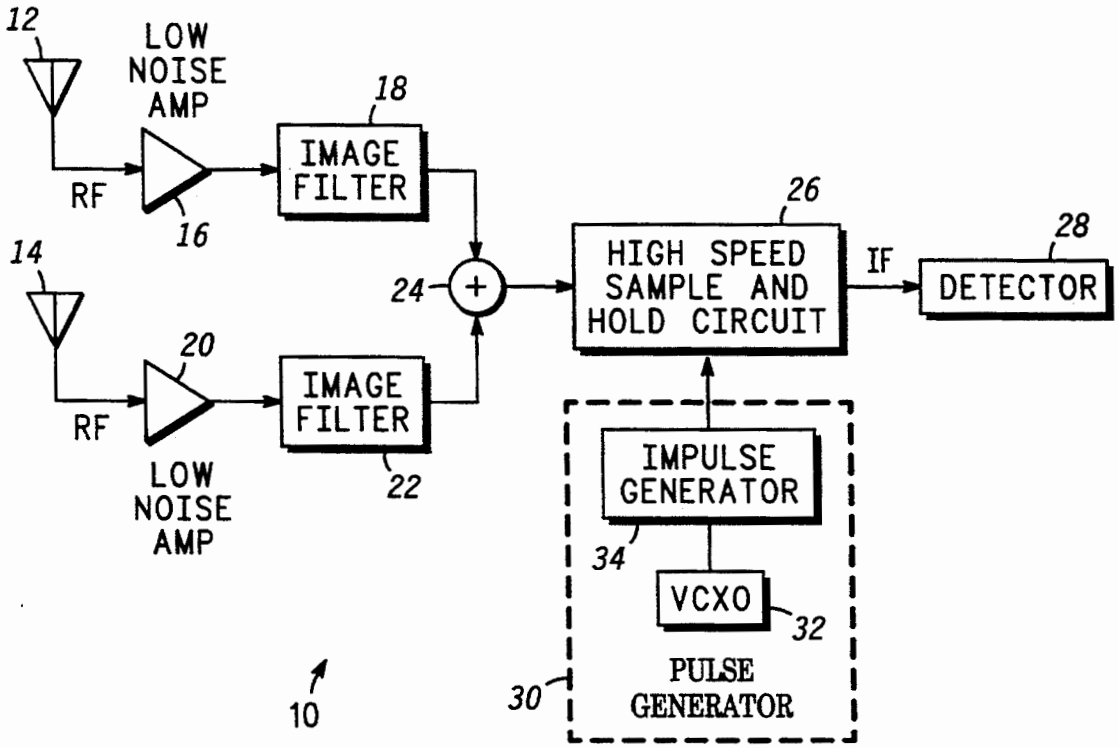
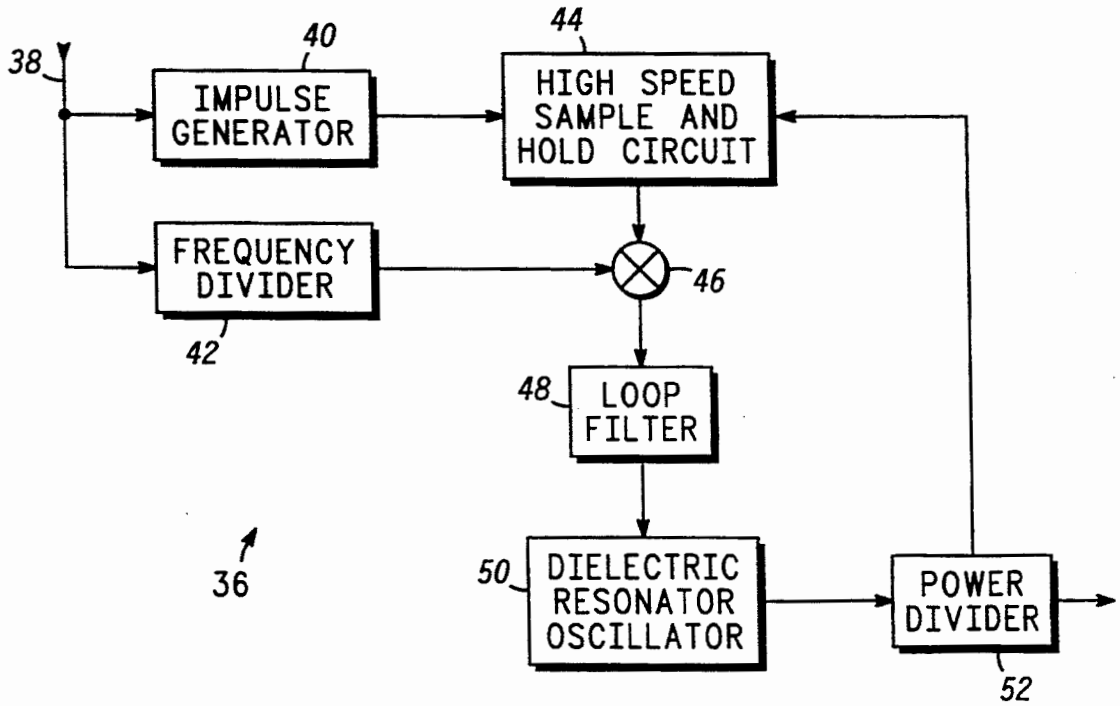


FIG. 1

FIG. 2



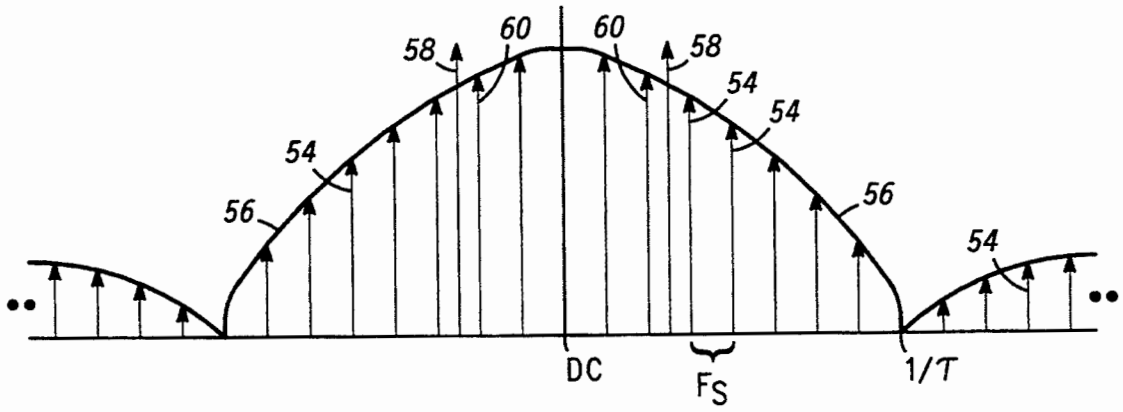
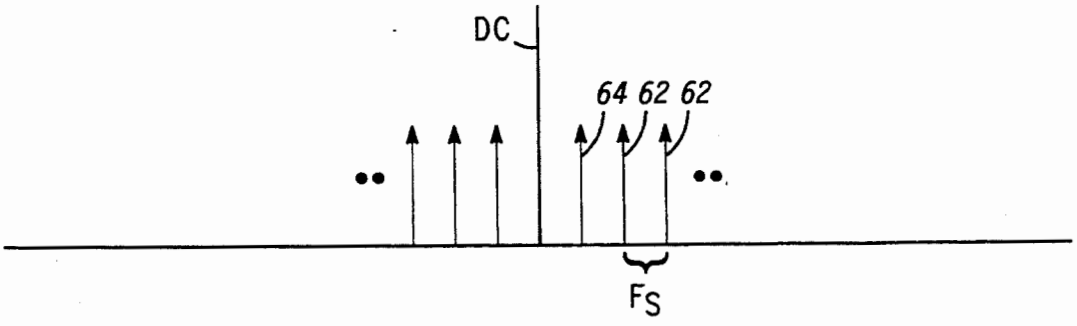


FIG. 3

FIG. 4



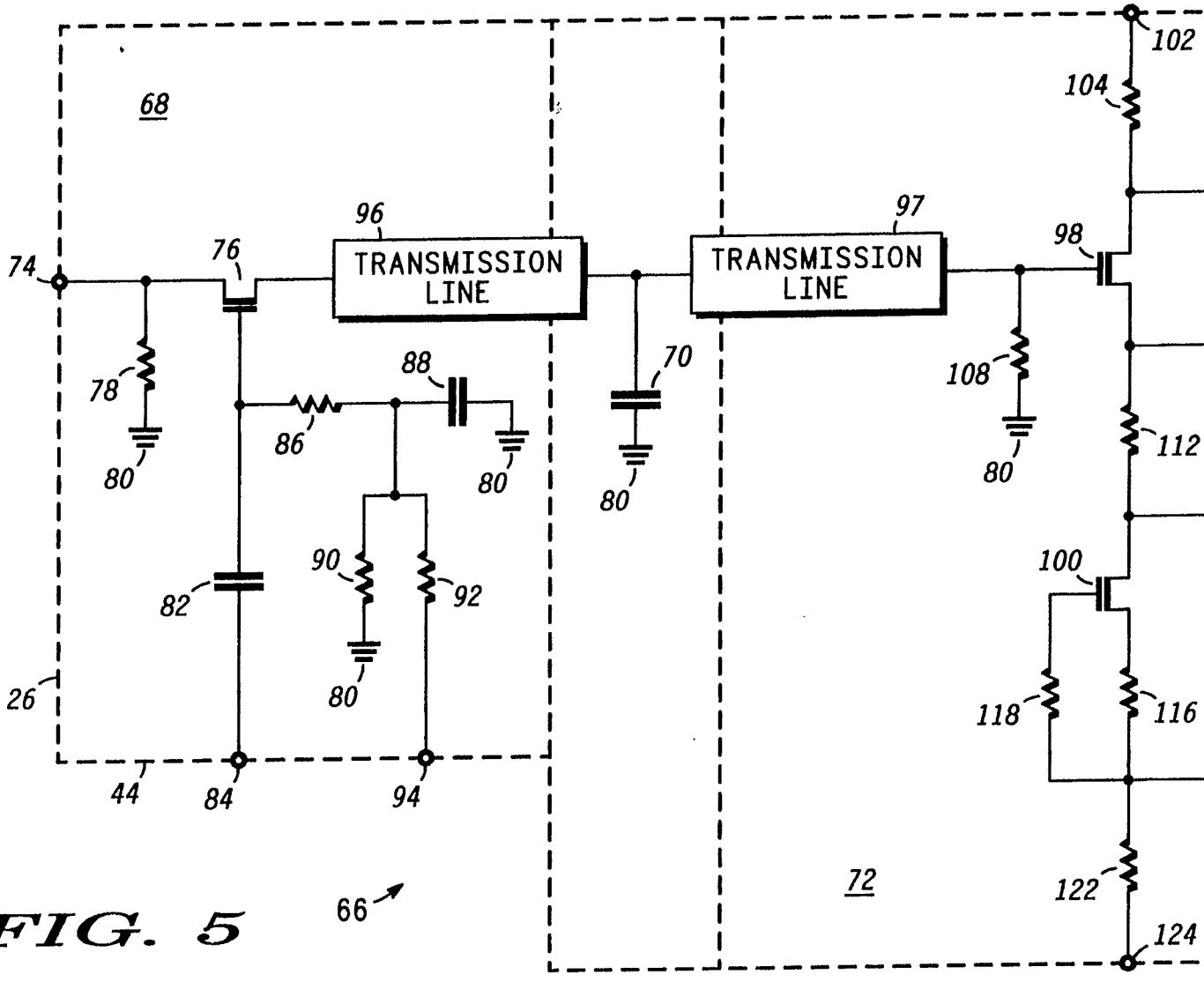


FIG. 5

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