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Assadian et al.

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[54] **PEAK DETECTOR CIRCUIT**

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[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

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[22] Filed: **Jan. 23, 1998**

[51] **Int. Cl.**[6] **G01R 19/00**

[52] **U.S. Cl.** **327/62**; 327/58

[58] **Field of Search** 327/58–62, 65, 327/74, 75, 76, 77, 89, 88; 323/315

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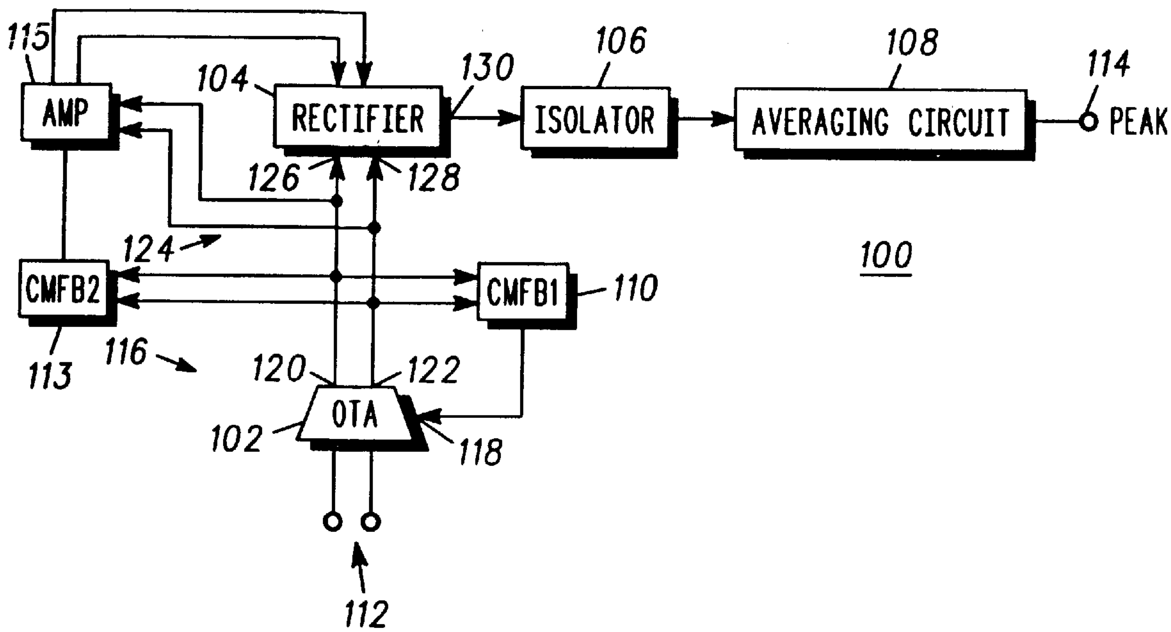
Primary Examiner—Toan Tran
Attorney, Agent, or Firm—Brian M. Mancini

[57] **ABSTRACT**

A peak detector circuit (**100**) includes an output transconductance amplifier (**102**), a current rectifier (**104**) and an averaging circuit (**108**). The current rectifier includes an amplifier (**115**) which reduces input impedance of the current rectifier to increase the operating frequency of the peak detector circuit. An isolator (**106**) employs a current mirror (**509**) with a cascode transistor (**512**) having a bias potential which is dynamically adjusted to achieve accurate mirroring. An amplifier of a common mode feedback circuit (**110**) has improved linearity.

11 Claims, 3 Drawing Sheets



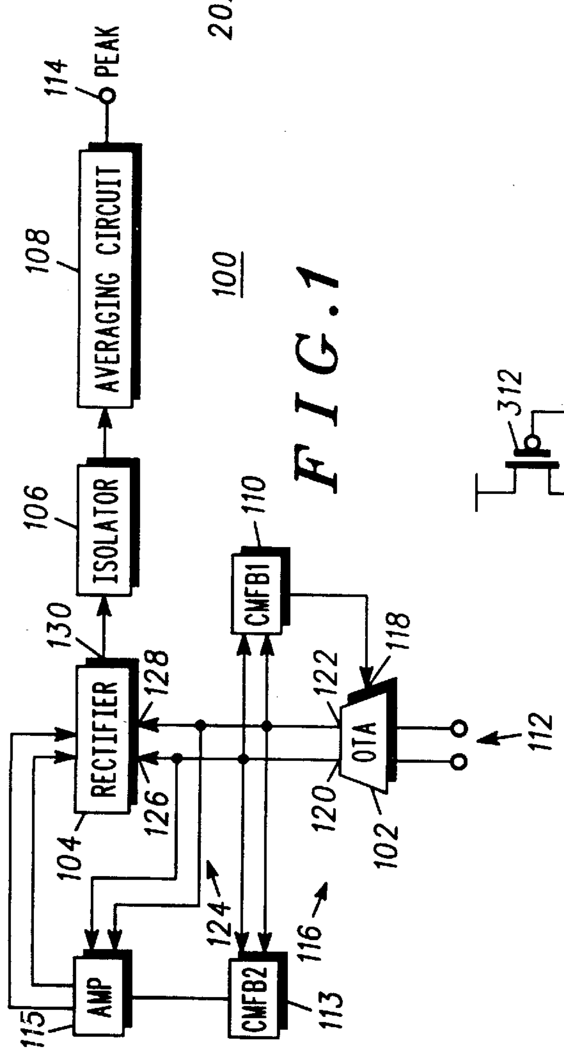


FIG. 1

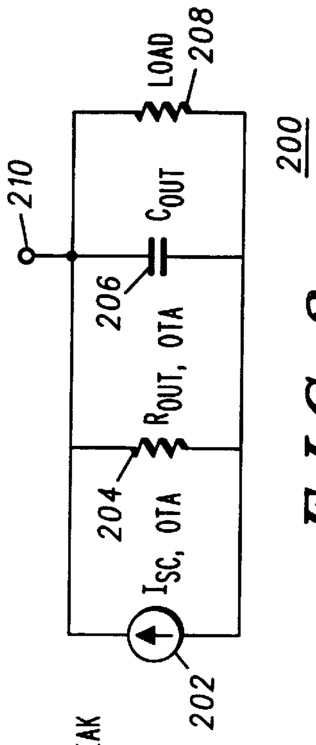


FIG. 2

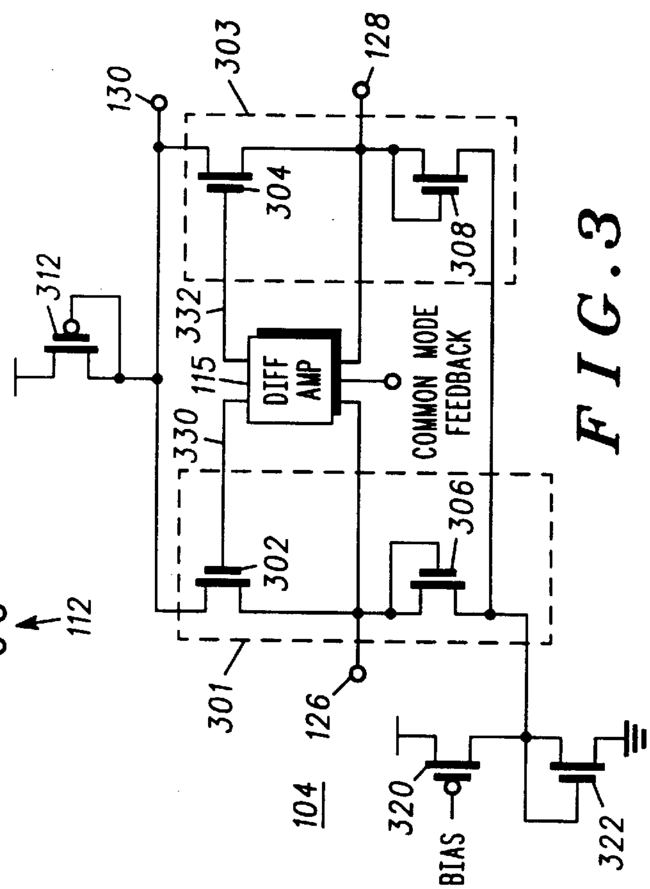


FIG. 3

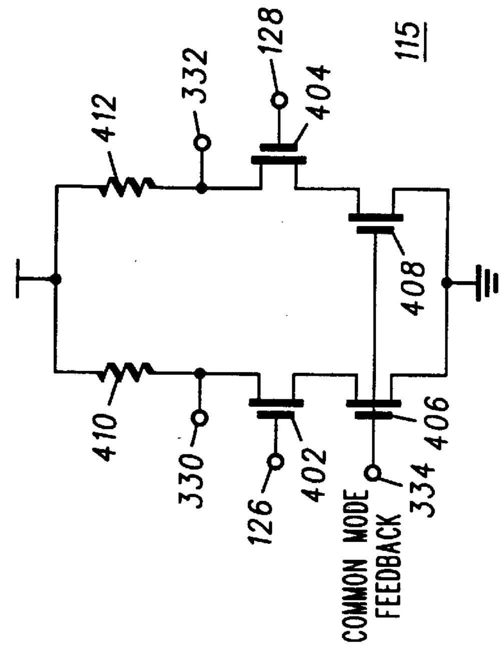


FIG. 4

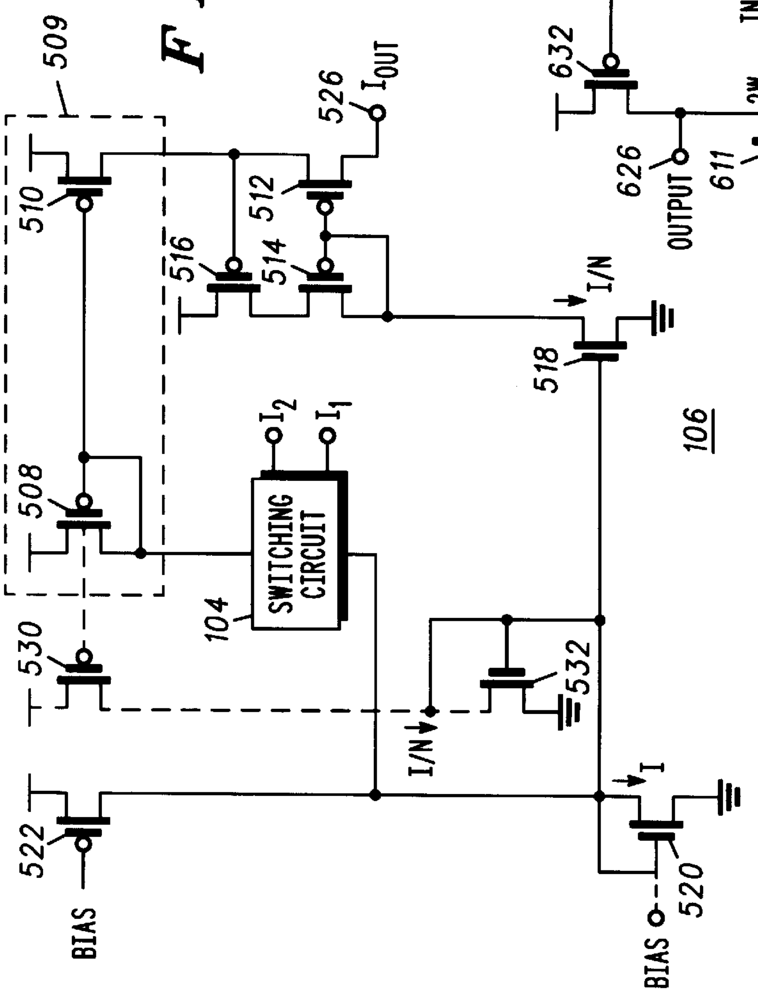

509
510
508
530
522
BIAS
516
514
512
526
I_{OUT}
SWITCHING CIRCUIT
104
I_2
I_1
I/N
518
106
532
I
520
BIAS

FIG. 5

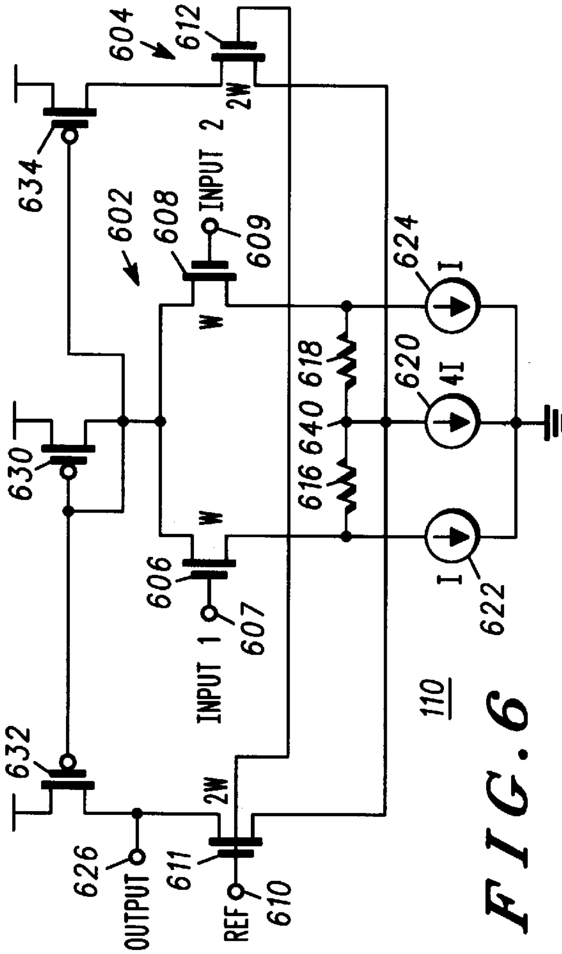

604
612
634
602
608
INPUT 2
609
2W
W
630
618
640
616
624
620
4I
I
606
607
INPUT 1
622
632
626
OUTPUT
611
REF
610
110

FIG. 6

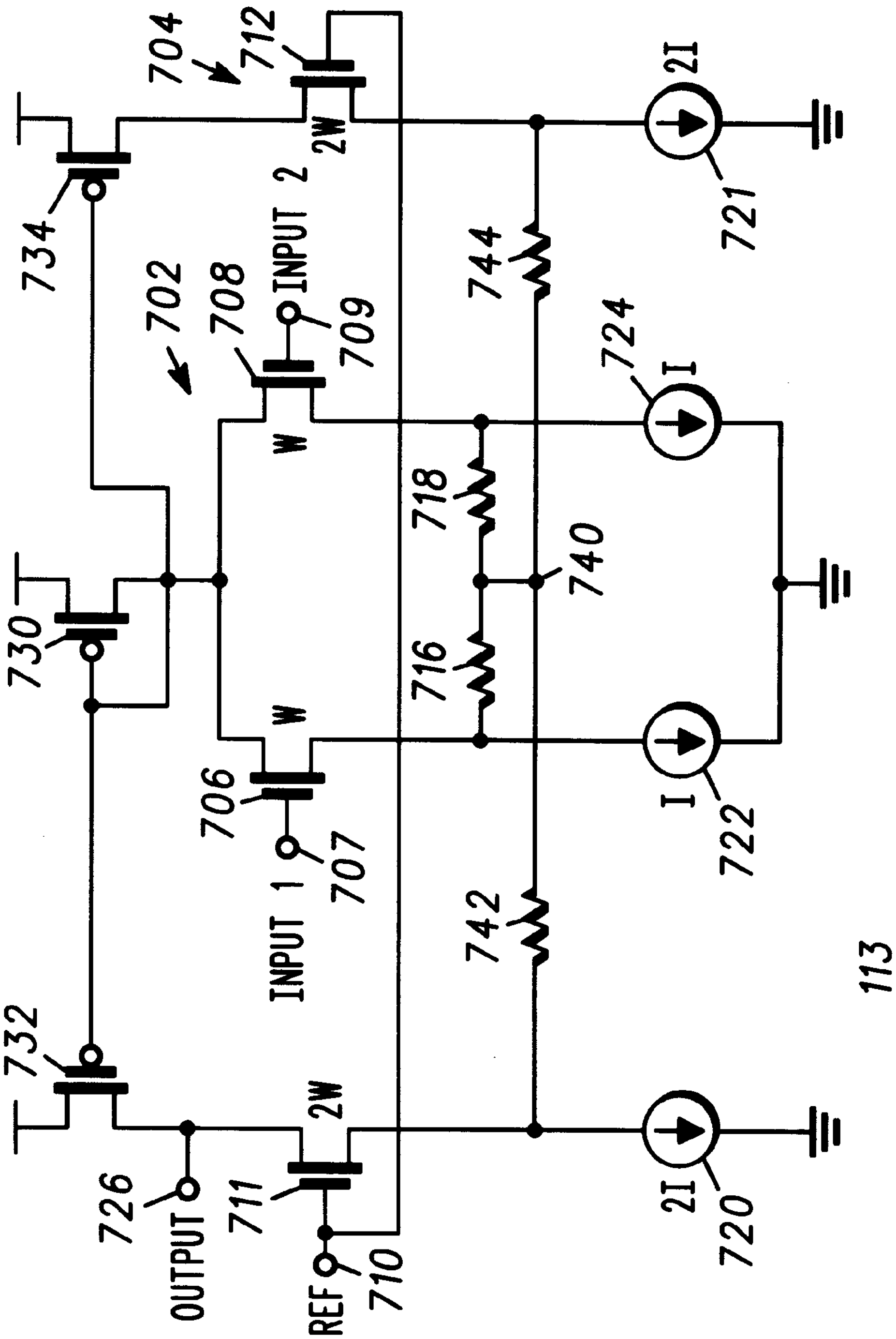

704
712
734
702
708
INPUT 2
709
2W
W
744
721
2I
724
I
718
740
730
716
706
707
INPUT 1
722
742
732
726
OUTPUT
711
REF
710
720
113

FIG. 7

PEAK DETECTOR CIRCUIT

FIELD OF THE INVENTION

The present invention generally relates to peak detector circuits. More particularly, the present invention relates to peak detector circuits capable of reliable operation at high frequencies.

BACKGROUND OF THE INVENTION

Peak detector circuits have a variety of applications, including in cellular telephones. In general, a peak detector operates by detecting a time varying input voltage and storing charge on a capacitor to produce a voltage equal to the maximum detected input voltage. Another known type of peak detector converts input voltage to a current and integrates the current. This second type of peak detector may be implemented in complementary metal oxide semiconductor (CMOS) technology, which enhances its applicability. For example, the CMOS peak detector may be integrated on a single integrated circuit with other circuit elements to reduce the cost and size of the overall circuit. Also, the CMOS peak detector may be operated at relatively low operating voltages, such as 3.0 V.

However, known CMOS peak detector designs have been limited to relatively low speed or low frequency applications. In one known design, the maximum input frequency is only 12 MHz, which is too low for many applications.

Accordingly, there is a need in the art for an improved peak detector circuit operable at input frequencies above 12 MHz.

BRIEF DESCRIPTION OF THE DRAWINGS

The features of the present invention, which are believed to be novel, are set forth with particularity in the appended claims. The invention, together with further objects and advantages thereof, may best be understood by making reference to the following description, taken in conjunction with the accompanying drawings, in the several figures of which like reference numerals identify identical elements, and wherein:

FIG. **1** is a block diagram of a peak detector circuit in accordance with the present invention;

FIG. **2** is a circuit model of a portion of the peak detector circuit of FIG. **1**;

FIG. **3** is a circuit diagram of a current rectifier for use in the peak detector circuit of FIG. **1**;

FIG. **4** is a circuit diagram of a differential amplifier for use in the current rectifier of FIG. **3**;

FIG. **5** is a circuit diagram of an isolator for use in the peak detector circuit of FIG. **1**;

FIG. **6** is a circuit diagram of a common mode feedback circuit for use in the peak detector circuit of FIG. **1**; and

FIG. **7** is a circuit diagram of an alternative embodiment of a common mode feedback circuit for use in the peak detector circuit of FIG. **1**.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

Referring now to FIG. **1**, it shows a block diagram of a peak detector circuit **100** in accordance with the present invention. The peak detector circuit **100** includes an operational transconductance amplifier (OTA) **102**, a current rectifier **104**, an isolator **106** and an averaging circuit **108**. The peak detector circuit **100** further includes a first com-

mon mode feedback circuit **110**, a second common mode feedback circuit **113** and an amplifier **115**. In operation, the peak detector circuit receives an input voltage and produces an output signal having signal values indicative of peak values of the input voltage.

The OTA **102** has an input **112** for receiving the input voltage, an output **116** and a feedback input **118**. An operational transconductance amplifier (OTA) is a circuit that produces an output current proportional to a differential input voltage. The ratio of the output current to the input voltage is the transconductance, g_m, of the amplifier. The OTA **102** produces an OTA output signal including an output current at the output **116** in response to the input voltage and a feedback signal received at the feedback input **118**. The output current is a time varying, generally alternating current (AC) current and may include a direct current (DC) component. In the illustrated embodiment, the output **116** of OTA **102** is a differential output. The output **116** includes a first output **120** and a second output **122**. That is, currents of substantially equal amplitude and opposite phase are provided at the first output **120** and the second output **122**.

The current rectifier **104** has an input **124** including first input **126** and second input **128** coupled to the OTA and an output **130**. The current rectifier **104** produces a signal at the output **130** in response to the output current from the OTA. The current rectifier **104** in the illustrated embodiment full wave rectifies the input current to produce the signal at the output **130**. Thus, the current rectifier **104** operates as an integrator, integrating the current received from the OTA **102**. In accordance with the present invention, the current rectifier **104** includes an amplifier which decreases input impedance of the current rectifier **104** to increase operating frequency of the peak detector circuit. Detailed structure and operation of the current rectifier **104** will be described below in conjunction with FIG. **3**.

The isolator **106** is coupled between the current rectifier **104** and the averaging circuit **108**. The isolator **106** operates to buffer the output **130** of the current rectifier **104** from loading by the averaging circuit **108**. Detailed structure and operation of the isolator **106** will be described below in conjunction with FIG. **5**.

The averaging circuit **108** averages the output signal received from the current rectifier **104** and the isolator **106**. The averaging circuit **108** may be any suitable combination of passive components. The averaging circuit **108** produces an output signal at output **114** having a signal value indicative of peak values of the differential input voltage at the input **112**.

The first common mode feedback circuit **110** provides the feedback signal to the feedback input **118** of the OTA **102**. Structure and operation of the first common mode feedback circuit **110** will be described below in conjunction with FIG. **6**. The second common mode feedback circuit **113** provides a feedback signal to the amplifier **115**. Structure and operation of the second common mode feedback circuit **113** will be described below in conjunction with FIG. **7**. The amplifier **115** improves frequency response of the peak detector in a manner to be described in conjunction with FIGS. **4** and **5** below.

FIG. **2** is a circuit model of a portion of the peak detector circuit of FIG. **1**. In FIG. **2**, the OTA **102** is modelled as a current source **202**, output resistance **204** and output capacitance **206**. The current rectifier **104** (FIG. **1**) is modelled as a load resistance **208**. The load resistance **208** is coupled in parallel with the output resistance **204** and output capacitance **206**.

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