CCD and CMOS Imaging Array Technologies: Technology Review

Stuart A. Taylor

Technical Report EPC-1998-106

Xerox Research Centre Europe
Cambridge Laboratory
61 Regent Street
Cambridge CB2 1AB

Tel: +44 1223 341500
Fax: +44 1223 341510

CCD and CMOS Imaging Array Technologies
- Technology Review -

Stuart A Taylor
Xerox Research Centre Europe
Cambridge, UK.
staylor@xrce.xerox.com

Abstract
This paper provides an overview of both CCD (charged coupled device) and CMOS (complimentary metal oxide semiconductor) imaging array technologies. CCDs have been in existence for nearly 30 years and the technology has matured to the point where very large, consistent (low numbers of defects) devices can now be produced. However, CCDs suffer from a number of drawbacks, including cost, complex power supplies and support electronics. CMOS imaging arrays, on the other hand, are still in their infancy, but are set to develop rapidly and offer a number of potential benefits over CCDs. This review provides an overview of both CCD and CMOS imaging technology, and includes explanations of how images are captured and read out from the imaging arrays. Also covered are issues such as performance characteristics, cost considerations and the future of imaging arrays. This review does not provide details of colour sensors, colour filter arrays and colour interpolation, etc., as these will be the subject of a separate report.

Introduction to CCDs
The Charged Coupled Device (CCD) was invented in 1970 by Willard Boyle and George Smith at Bell Laboratories, USA [Sharma97]. The idea originated from research into magnetic bubble memories, and as with many great inventions, Smith is quoted as saying "[we] invented charged-coupled devices in an hour" [Lucent96]. In the intervening twenty-eight years, CCDs have found their way into a huge range of products including fax machines, photocopiers, cameras, scanners and even children's toys.

CCDs consist of thousands (or millions) of light sensitive cells or pixels that are capable of producing an electrical charge proportional to the amount of light they receive. Typically, the pixels are arranged in either a single line (linear array CCDs) or in a two-dimensional grid (area array CCDs). The particular application will, in general, dictate the type of CCD that is used. Flatbed scanners, for example, use linear array CCDs and, in this case, it is necessary to progressively move the CCD over the object being imaged (or vice versa) while capturing multiple one-dimensional images in order to build up the final two-dimensional image. Digital cameras, on the other hand, normally use area array CCDs, thus allowing the full two-dimensional image to be captured within a single exposure.

One of the fundamental parameters of a CCD is resolution, which is equal to the total number of pixels that makes up the light sensitive area of the device. One of the first area array CCDs, manufactured by Fairchild in 1974, had a resolution of 100x100 [Oregon97]. Today, the largest commercially available device is approximately 9000x7000 or roughly 63 million pixels [Pixelv97]. Other parameters that characterise CCDs will be discussed in more detail later.

CCDs are in essence integrated circuits (ICs) and are hence rather like computer chips. However, to allow light to fall on the silicon chip (or die) a small glass window is inserted in front of the chip. Conventional ICs are usually encapsulated in a black plastic body to primarily provide mechanical strength, but this also shields them from light, which can affect their normal operation. CCDs are manufactured using metal-oxide-semiconductor (MOS) fabrication techniques, and each pixel can be thought of as a MOS capacitor that converts photons (light) into electrical charge, and stores the charge prior to readout.

Examples of CCD Arrays

Before moving on to explain the operation of CCDs in more detail, it is useful to illustrate what CCDs actually look like. The following table shows three different devices for comparison, along with their respective pixel counts. The transfer method will be explained in a subsequent section.

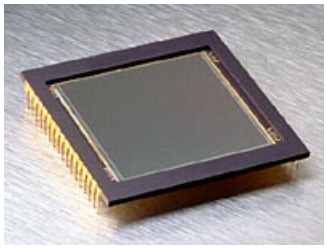
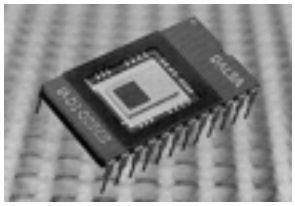
	Manufacturer: Kodak Type: area array Pixel count: 4096x4096 Transfer method: full frame transfer
	Manufacturer: Dalsa Type: area array Pixel count: 256x256 Transfer method: frame transfer
	Manufacturer: Kodak Type: linear array Pixel count: 5000 Transfer method: full frame transfer

Table 1 – Examples of CCD Arrays [Kodak98, Dalsa98]

CCD Fundamentals

As mentioned above, each pixel that makes up a CCD is essentially a MOS capacitor, of which there are two types: *surface channel* and *buried channel*. The two differ only slightly in their fabrication, however; buried channel capacitors offer major advantages, and because of this, nearly all CCDs manufactured today use this preferred structure.

A schematic cross section of a buried channel capacitor is shown in Figure 1 [Sharma97, SITe94]. The device is typically built on a p-type silicon substrate (approx 300µm thick) with an n-type layer (approx 1µm thick) formed on the surface. Next, a thin silicon dioxide layer (approx 0.1µm thick) is grown followed by a metal electrode (or gate). The application of a

positive voltage to the electrode reverse biases the p-n junction and this causes a potential well to form in the n-type silicon directly below the electrode. Incident light generates electron-hole pairs in the depletion region, and due to the applied voltage, the electrons migrate upwards into the n-type silicon layer and are trapped in the potential well [Muncaster85]. The build up of negative charge is thus directly proportional to the level of incident light.

Once the exposure time (also known as the integration time) has elapsed, the charge trapped in the potential well is transferred out of the CCD before being converted to an equivalent digital value.

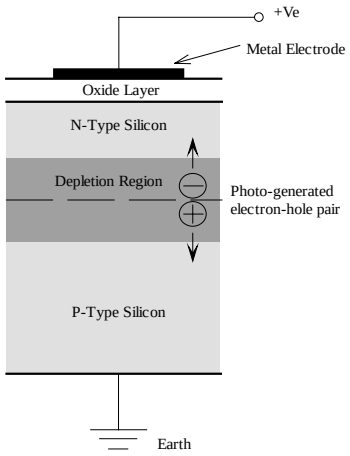


Figure 1 - Buried Channel Capacitor CCD Pixel

An illustration of a practical buried channel capacitor is shown in Figure 2 [SITe94]. This diagram also shows the channel stops, which are usually created by heavily doping these regions to form p-type semiconductor. In addition, a thick layer of oxide, the field oxide, is applied over these regions. The purpose of the channel stops is to minimise the diffusion of electrons from one pixel to another.

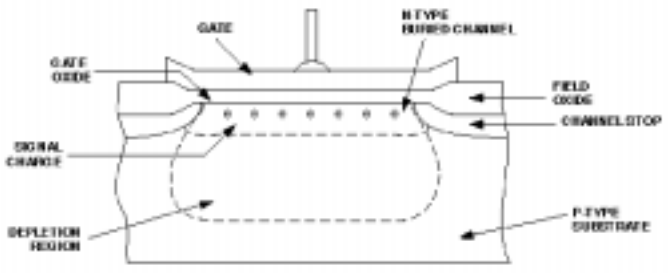


Figure 2 – Practical Buried Channel Capacitor (From [SITe94])

The Charge Readout Process

The charge readout process takes place in two stages. The first involves moving the pixel charges across the surface of the array. The second involves reading out the pixel charges into a register prior to being digitised.

The charge transfer process can be explained as follows. Each pixel is divided into a number of distinct areas known as *phases* [Gallagher]. Three-phase sensors tend to be the most common form due principally to high yields and high process tolerances, although one, two, and four phase formats do exist [SITe94]. Taking a three phase sensor as an example (see Figure 3), the integration period, phases 1 and 2 will be in charge holding mode, and phase 3 will be in charge blocking mode (a). At the end of the integration period, when it is time to transfer the captured image out of the array, the following process takes place. Phase 1 is placed in charge blocking mode, which has the effect of transferring the total charge of phases 1 and 2 into only phase 2 (b). Phase 3 is then placed in charge holding mode, which allows the charge in phase 2 to distribute itself evenly between phases 2 and 3 (c). Next, phase 2 is placed in charge blocking mode, forcing the charge into phase 3 (d). This process repeats, until, as illustrated by (g), the charge from pixel two has been moved into pixel one. An alternative representation [Oregon97] of the charge readout process is illustrated in Figure 4.

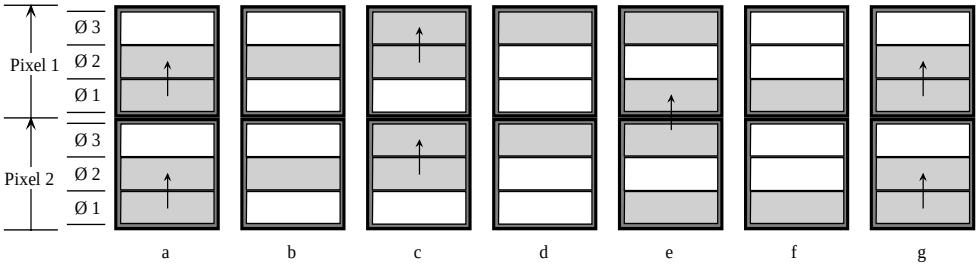


Figure 3 - Charge Transfer

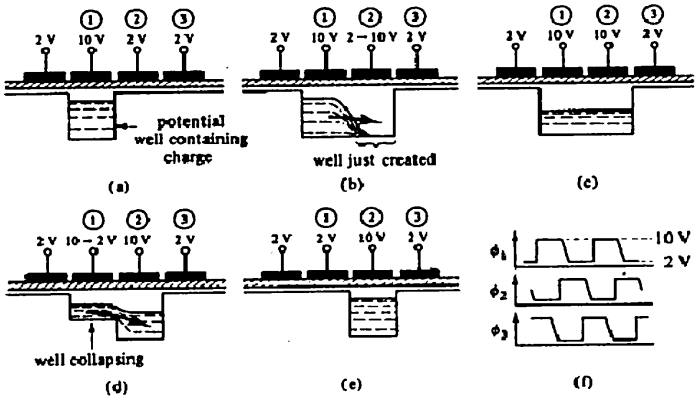


Figure 4 - Charge Transfer; Alternative Representation (From [Oregon97])

The second stage of the readout process occurs after each row of pixels has been transferred by one complete row. Located adjacent to the top row of pixels is one additional row of pixels called the readout register. As the charge from each row of pixels is moved up one row, the charge from the top row will be moved into the readout register. At this point, the charge values in the readout register are transferred horizontally into the readout stage, from which they are then sent to an analogue-to-digital converter (ADC) before being stored in memory. This process is illustrated in Figure 5 .

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.