1.   My name is Jack Lee. I am over the age of twenty-one (21) years, of sound mind, and capable of making the statements set forth in this Declaration. I am competent to testify about the matters set forth herein. All the facts and statements contained herein are within my personal knowledge and they are, in all things, true and correct.

2.   I have been asked by Qualcomm Inc. ("Qualcomm") to submit this declaration in support of its challenge to the validity of certain claims of U.S. Patent No. 6,534,805 ("the '805 Patent").

I.   Education and Experience

3.   My *curriculum vitae* is attached as Exhibit 1022.

4.   I received my Bachelor of Science and Master of Science Degrees in Electrical Engineering from University of California at Los Angeles in 1980 and 1981, respectively and my Ph.D. degree in electrical engineering from University of California at Berkeley in 1988.

5.   I have more than 35 years of experience as an electrical engineer in integrated circuit and semiconductor device design, fabrication, and testing. I began my career at the TRW Microelectronics Center in 1981 and joined the faculty at The University of Texas at Austin in 1988.

6.   I have published over 550 journal publications and conference proceedings, 6 book and book chapters, and have 9 issued patents. I have been recognized with many teaching and research awards. I have supervised and graduated more than 40 Ph.D. students. I am a fellow of the Institute of Electrical and Electronic Engineers (IEEE) and have been a Distinguished Lecturer for the IEEE Electron Devices Society.

7.   At The University of Texas at Austin, I teach undergraduate circuit analysis and design courses, as well as graduate level courses. One graduate course that I developed is entitled "Nanoscale Device Physics and Technologies," which focuses on the topics of current research on ultra-small high-speed semiconductor devices used in integrated circuits and is designed for graduate students wishing to pursue research in the nanotechnology area.

8.   Having the above knowledge and experience, I am well qualified to offer the opinions I express in this declaration.

II.   Compensation

9.   In consideration for my services, my work on this case is being billed to Qualcomm at an hourly rate of $650 per hour, independent of the outcome of this proceeding. I am also being reimbursed for reasonable expenses I incur in relation to my services provided for this proceeding.

III. Legal Considerations

10. My understanding of the law is based on information provided by counsel for Qualcomm.

11. I understand that a U.S. Patent document is presumed to have sufficient description to include sufficient detail for a person of ordinary skill in the art to make and use the subject matter that document describes.

12. I understand that a claimed invention is obvious and, therefore, not patentable if the subject matter claimed would have been considered obvious to a person of ordinary skill in the art (POSITA) at the time that the invention was made. I understand that a claim can be obvious in view of a single prior art reference (e.g., via modification of that prior art reference) or multiple prior art references (e.g., via a combination of two or more prior art references), if such a modification or combination was within the skill of a POSITA. I understand that there must be some articulated reasoning with some rational underpinning to support a conclusion of obviousness. I further understand that exemplary rationales that may support a conclusion of obviousness include: (1) simply arranging old elements in a way in which each element performs the same function it was known to perform, and the arrangement yields expected results, (2) merely substituting one element for another known element in the field, if the substitution yields no more than a predictable result, (3) combining elements in a way that was "obvious to try" because of a design

need or market pressure, where there was a finite number of identified, predictable solutions, (4) that design incentives or other market forces in a field would have prompted variations in a work that were predictable to a person of ordinary skill in the art, and (5) that there was some teaching, suggestion, or motivation in the prior art that would have led a POSITA to modify the prior art reference or to combine prior art references to arrive at the claimed invention, among other rationales.

13.   I understand that a claim term is interpreted according to its ordinary and customary meaning as a POSITA would have understood the term in light of the surrounding claim language, other claims, the specification, and the patent's prosecution history, which are referred to as intrinsic evidence. I also understand that prior art references cited in the patent's prosecution history are considered intrinsic evidence. I further understand that evidence outside the patent and its prosecution history (e.g., dictionaries and technical articles), may inform the context in which a POSITA would have understood the claims of a patent. I understand this ordinary and customary meaning applies absent unique circumstances, such as where a patent clearly expresses an intent to set forth a special meaning for a term, or a claim term does not convey any particular structure to a POSITA (e.g., "means").

IV. Task Summary

14. I have been asked to review the '805 Patent. I have been asked to provide my opinions from the perspective of a person of ordinary skill, having knowledge of the relevant art, as of April 9, 2001, and the opinions stated in this declaration are from that perspective. The qualifications and abilities of such a person are described in Section VI below.

15. In preparing this declaration, I have considered this patent and its prosecution and reexamination history as well as the general knowledge of those familiar with the field of semiconductor design and manufacturing, and specifically SRAM cells, as of April 9, 2001.

16. I have also reviewed the references that form the basis for Qualcomm's challenge to the '805 Patent, including the publications listed in the following table:

Exhibit No.	Description
1001	U.S. Patent No. 6,534,805 (with *Ex Parte* Reexamination Certificate Appended)
1002	Omitted
1003	Omitted
1004	U.S. Patent No. 6,417,549 ("Oh")
1005	R. Jacob Baker et al., CMOS Circuit Design, Layout And Simulation, IEEE Press (1998) ("CMOS Circuit Design")
1006	Prosecution History for U.S. Patent Application No. 09/829,510
1007	*Ex Parte* Reexamination History for U.S. Patent No. 6,534,805
1008	Ishida, et al., "A Novel 6T-SRAM Cell Technology Designed with Rectangular Patterns Scalable beyond 0.18 μm Generation and Desirable for Ultra High Speed Operation," IEDM 98, IEEE 1998,

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