Robert J. Murphy
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Los Gatos, California 95030
(408) 396-6098

Abstract: More than 45 Years of experience in management,design, hands-on development & debug of: High speed, high complexity, high density and high volume commercial semiconductor products including Full Custom Microprocessors, E^2CMOS and BiCMOS PALs, CMOS and NMOS SRAMs, CCDS and RAD Hard SOS CMOS.

| **Founder & Owner** | **Firenza, LLC.** |
| **4/98 – PRESENT** | **Los Gatos, CA.** |

Founded company to respond to the growing needs of the semiconductor industry to license quality high performance building blocks for Semi-Custom and ASIC designs. Developed business plan, cultivated customers and managed the efforts of Design Professionals to deliver world class building blocks in 0.25u 0.18u, 0.13u, 65nM & 14nM processes. Provided circuit design reviews on 65 nM Major Microprocessor. Designed EFUSE circuit for another 65 nM Microprocessor. Debugged and provided layout based solutions for 65 nM process latch-up issue. Designed 28nM & 14nM SRAM circuits. Developed custom 10Ghz SRAMs IP Blocks for custom processor in 14nM process.

Performed Expert Witness work on the following cases:

NeoMagic Corporation v. Trident Microsystems, Inc.
D. Del., C.A. No. 98-699-RRM, Client: Trident, Year: 1999

Rambus, Inc. v. Infineon Technologies AG,
           Infineon Technologies North America Corp.,
              And
           Infineon Technologies Holding North America, Inc.
Eastern D. Virginia, C.A. No. 3:00cv524, Client: Rambus, Year: 2001

Micron v, Rambus, Inc.
D. Del., C.A. No. 00-792-(RRM), Client: Rambus Year: 2001

Hynix Semiconductor Inc. et al. v. Rambus, Inc.
Northern D. Calif., Case No. CV 00-20905 RMW
Client: Rambus, Year: 2005

Rambus, Inc. v. Hynix Semiconductor Inc. et al.
Northern D. Calif., Case Nos. C-05-00334, C-05-02298,
C-06-00244, C-00-20905 RMW, Client: Rambus Year: 2007

Toshiba v. Hynix
International Trade Commission, Investigation No. 337-TA-592
Client: Toshiba Year: 2007

UniRAM Technology, Inc. v. MONOLITHIC SYSTEM TECHNOLOGY, TAIWAN
SEMICONDUCTOR MANUFACTURING COMPANY, LTD, & TSMC NORTH AMERICA
Northern D. Calif., Case No. CV-04-01268-VRW
Client: UniRAM Year: 2008

Perego, et al. v. Drehmel, et al.
U.S.P.T.O., Patent Interference No. 105,467 (Bd. Pat, App.& Int.)
Client: Rambus Year: 2007

Reexamination proceedings involving various U.S. Patents in the
Farmwald / Horowitz Family derived from Application No. 07/510,898
Client: Rambus Year: 2011

Reexamination proceedings involving U.S. Patents #'s 7,210,016;
7,177,998, Client: Rambus, Year: 2009

Reexamination proceedings involving U.S. Patents #'s 7,287,119;
7,330,952; 7,330,953; 7,360,050; Client: Rambus, Year: 2010

Reexamination proceedings involving U.S. Patents #'s 7,287,109;
6,591,353; 6,470,405; Client: Rambus, Year: 2009

*In The Matter Of: CERTAIN MLC FLASH MEMORY DEVICES AND
PRODUCTS CONTAINING SAME,* International Trade Commission,
Investigation No. 337-TA-683, Client: BTG, Year: 2009

e.Digital Corporation v. Toshiba America Information Systems Inc.
Southern D. California, Case No, '13CV2909 BEN BGS, Client: Toshiba,
Year: 2013, Matter: Flash Memory File System in a Handheld Record
and Playback Device

*In The Matter Of: CERTAIN STATIC RANDOM ACCESS MEMORIES AND
PRODUCTS CONTAINING SAME,* International Trade Commission,
Investigation No. 337-TA-792,Client: GSI Year: 2013

*In The Matter Of: CERTAIN WIRELESS COMMUNICATIONS EQUIPMENT AND
ARTICLES THEREIN,* International Trade Commission,
Investigation No. 337-TA-866, Client: Ericcson Year: 2013,
Matter: Wireless Communication Equipment & Power Supplies

Solid State Storage Solutions, Inc. v. STEC, INC., OCZ TECHNOLOGY,
INC., CORSAIR MEMORY, TEXAS MEMORY SYSTEMS, INC., PNY TECHNOLOGIES,
INC., PATRIOT MEMORY LLC, FUSION-IO, INC., OTHER WORLD COMPUTING,
INC., and MUSKIN, INC. Eastern D. Texas, Case No. 2:11-cv-00391-
JRG-RSP, Client: Solid State Year: 2012

GSI Technology, Inc. v. UNITED MEMORIES INC. and INTEGRATED SILICON
SOLUTION, INC., Northern D. Calif., Case No. 13-cv-1081-PSG
Client: GSI Year: 2015, Matter: Static RAM Memory Devices & Features

GSI Technology, Inc. v. CYPRESS SEMICONDUCTOR CORP.
Northern D. Calif., Case No. 5:11-cv-03613-EJD
Client: GSI, Year: 2015, Matter: Static RAM Memory Devices &
Features

Career History for Robert J. Murphy (Cont'd)

CYPRESS SEMICONDUCTOR CORP. v. GSI Technology, Inc. Northern D. Calif., Case Nos. 3:13-cv-02013-JST (JCS), 4:13-cv-03757-JST (JCS), Client: GSI, Year: 2015, Matter: Static RAM Memory Devices & Features

Petition for *Inter Partes* Review involving U.S. Patents nos. 6,292,403 (Case IPR2014-00121) and 6,069,839 (Case IPR2014-00202), Client: GSI, Year: 2015, Matter: Static RAM Memory Devices & Features

Petition for *Inter Partes* Review involving U.S. Patent no. 6,058,045 (Case IPR2014-00113), Client: Toshiba, Year: 2015, Matter: DRAM Memory & Features for Display Operations

Petition for *Inter Partes* Review involving U.S. Patent no. 5,687,132 (Case IPR2014-00317), Client: Toshiba, Year: 2015, Matter: DRAM Memory & Features for Display Operations

*In The Matter Of: CERTAIN INTEGRATED CIRCUITS AND PRODUCTS CONTAINING THE SAME, U.S. ITC Inv. No. 337-TA-920, Client: Freescale, Year: 2014, Matter: C*ircuitry for timing operations within memory circuits and to bond pad structures and layouts used on integrated circuits.

Freescale Semiconductor, Inc. v. MediaTek Inc., et al.*,* Northern D. of California, Case No. 5:14cv02185BLF, Client: Freescale, Year: 2014, Matter: Circuitry for timing operations within memory circuits and to bond pad structures and layouts used on integrated circuits.

Petition for *Inter Partes* Review involving U.S. Patent no. 5,500,819 (Case IPR2014-00418), Client: Toshiba, Year: 2015, Matter: DRAM Memory & Features for Display Operations

Intellectual Ventures I LCC et al. v. Toshiba Corporation et al. D, Del., C.A. No. 13-453-SLR-SRF, Client: Toshiba, Year: 2017, Matter: DRAM Memory & Features for Display Operations

In The Matter Of: CERTAIN MEMORY MODULES AND COMPONENTS THEREOF, AND PRODUCTS CONTAINING SAME, U.S. ITC Inv. No. 337-TA-1023, Client: Netlist, Year: 2017, Matter: Features of DRAM Memory Modules

Petition for *Inter Partes* Review involving U.S. Patent no. 8,489,837 (Case IPR2017-00548), Client: Netlist, Year: 2017, Matter: Features of DRAM Memory Modules

In The Matter Of: CERTAIN MEMORY MODULES AND COMPONENTS THEREOF, U.S. ITC Inv. No. 337-TA-1089, Client: Netlist, Year: 2018, Matter: Features of DRAM Memory Modules

Petition for *Inter Partes* Review involving U.S. Patent no. 9,535,623 (Case IPR2018-00303), Client: Netlist, Year: 2018, Matter: Features of DRAM Memory Modules

> PHENIX LONGHORN, LLC v. WISTRON CORP. et al.
> Eastern D. Texas, Case No. 2:17-cv-000711-RWS, Client: Phenix, Year:
> 2018, Matter: Gamma Reference Generator for Monitors & Televisions
>
> Petition for *Inter Partes* Review involving U.S. Patent no.
> 7,233,305 (Case IPR2018-01255), Client: Phenix, Year: 2018,
> Matter: Gamma Reference Generator for Monitors & Televisions
>
> PHENIX LONGHORN, LLC v. TEXAS INSTRUMANTS INC.
> Eastern D. Texas, Case No. 2:18-cv-00020-RWS, Client: Phenix,
> Year: 2018, Matter: Gamma Reference Generator for Monitors &
> Televisions

Director of Engineering   **Silicon Graphics Inc.**
     6/92 – 4/98   **Mountain View, CA.**

     Beast Program: Hired, managed and directed circuit designers on this 500
MHz design. Responsible for the scheduling and design reviews for all custom
circuit design on the chip. Supported CAD tool development with test structures,
test cases and debug.

     T5 (R10000) Program: Assisted in the final completion of this processor.
Took my team of people down to the project in it's late stages and managed 10%
of the Units (3) on the chip. Was a key member of the schedule review team.

   TFP (R8000) Program: Managed the design and implementation of the Floating
Point Chip for SGI's POWER CHALLENGE systems. Directed the re-design of a large
Tag Ram done for SGI by Toshiba. Managed a group of Toshiba's engineers in the
US and interacted with their counterparts in Japan to debug and repair the
design. The repaired design was fully functional with speeds of 110 MHz.

The redesign was accomplished while holding 16 lots of silicon in the fab. All
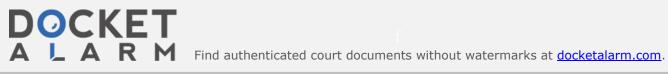of the lots were saved and parts delivered to SGI on time.

     Major accomplishments included:

   * Hired over 20 people.
   * Managed a total team of 30 people.
   * Developed extensive relationships with our Japanese Partners.
   * Hired contractors as needed for specific expertise
   * Directed the development and implementation of world class
       PLL designs onto the whole SGI campus.
   * Developed internal circuit design resources via training and
             assignment selection.

Director of Engineering   **Weitek Corp.**
     2/89 - 6/92   **Sunnyvale, CA**

     Initially hired as a Design Manager with responsibility for putting a
single chip into production. One year later, was managing the company's most

important product along with others. Developed circuitry which gave the company world-class performance in memory, output drivers, and Electro-Static Discharge (ESD). Promoted to Director (1990). Managed the circuit design, architecture and layout groups. This included budgeting, staffing, and resource allocation for multiple programs, the largest of which was over 400K transistors. Responsible for the technical and administrative management of a staff that included 20 engineers and 5 layout people.

     Major accomplishments included:

*   Managed the product design and release to production of a 40 MHz SPARC
        combined IU/FPU product
*   Managed the development and release to production of a
        Floating Point Coprocessor that works with the Intel i486.
*   Directed the redesign and release to production of two products,
        completed by other managers, which were not production worthy.
*   Aided Manufacturing in the pre- and post-production
        release management of our silicon foundries. This included
        modeling, process issues and production/testing problems.
*   Increased the staff by more than 50% in a one year period.
•   Delivered multiple projects on time.

Senior Engineering Manager   **National Semiconductor Corp.**
      10/83 - 2/89   **Santa Clara, CA**

     As the design manager and chief technical contributor for the E2CMOS PAL group, was a member of a team of three responsible for the introduction of three second-sourced products. Enlarged the design staff, established methodology and set circuit design criteria for new products under development.

The group's actions enabled the product line to go from zero revenue to greater than $1 million/month in just 12 months. Prior to the start up of the E2CMOS PAL group, designed a Bi-CMOS PAL using lateral Ti-W fuses.

     Major accomplishments included:

*   Doubled the reliability of the second-sourced devices.
*   Participated fully in all aspects of the second-sourcing
    licensing agreement.
*   Designed the world's first BiCMOS PAL, which was given as
    a paper at the ISSCC conference in 1986.
*   Developed the methodology and theory to improve lateral
    Ti-W fuse blowing circuitry.

Program Manager   **RCA**
      4/82 - 10/83   **Sommerville, NJ**

     Lead an inter-divisional program to develop 2 micron CMOS technology and a 64K SRAM for the commodity market. Responsible for a team of 15 people who:

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Sync your system to PACER to automate legal marketing.

fastcase
Smarter legal research.