## United States Patent [19]

#### **Cowles**

## [11]

**Patent Number:** 

5,729,504

**Date of Patent:** [45]

Mar. 17, 1998

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Primary Examiner-David C. Nelms Assistant Examiner—F. Niranjan Attorney, Agent, or Firm-Schwegman, Lundberg, Woessner & Kluth, P.A.

#### ABSTRACT [57]

An integrated circuit memory device is described which can operate at high data speeds. The memory device can either store or retrieve data from the memory in a burst access operation. The burst operations latch a memory address from external address lines and internally generates additional memory addresses. The integrated circuit memory can output data in a continuous stream while new rows of the memory are accessed. A method and circuit are described for outputting a burst of data stored in a first row of the memory while accessing a second row of the memory.

### 20 Claims, 7 Drawing Sheets

136 141
RAS* CONTINUOUS MODE
WE* 153
118139
114 5
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126 130
AO-A9 116 8 128 8 MEMORY ARRAY
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142
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## [54] CONTINUOUS BURST EDO MEMORY DEVICE [75] Inventor: Timothy B. Cowles, Boise, Id.

[73] Assignee: Micron Technology, Inc., Boise, Id.

[21] Appl. No.: 572,487

Dec. 14, 1995 [22] Filed:

Int. CL<sup>6</sup> ...... G11C 8/00 395/496

[58] Field of Search ....... 365/236, 238.5, 365/239; 395/496

[56]

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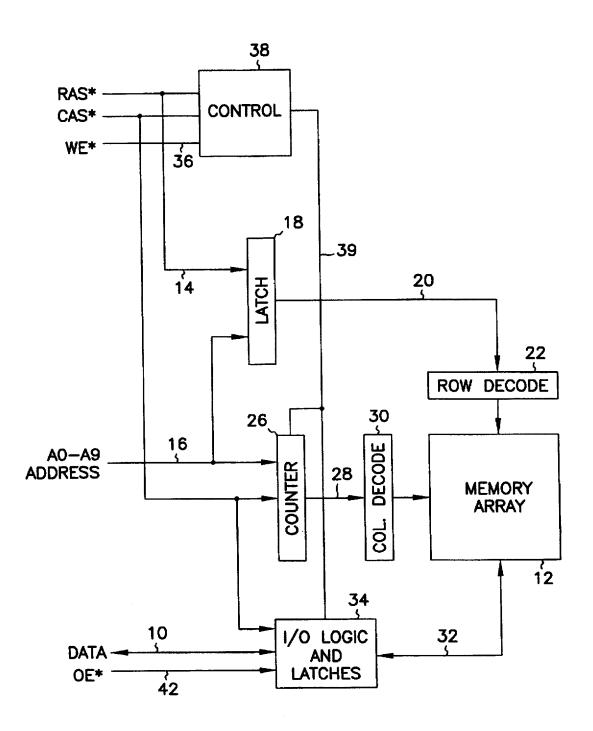


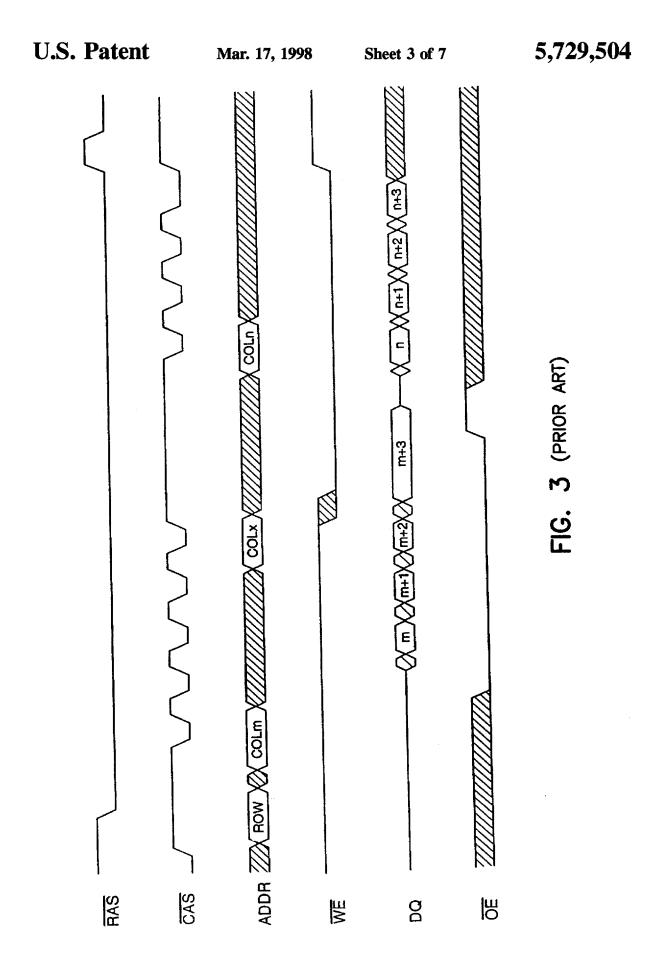
FIG. 1 (PRIOR ART)



FIG. 2 PRIOR ART)

	Starti	Starting Column	lumn		
Burst Lenath	A <sub>2</sub>	Address A <sub>1</sub>	s A <sub>o</sub>	Linear	Interleave
	>	>	0	0-1	1-0
	>	>	-	1-0	1-0
	>	0	0	0-1-2-3	0-1-2-3
	>	0	-	1-2-3-0	1-0-3-2
	>	-	0	2-3-0-1	2-3-0-1
	>	-	-	3-0-1-2	3-2-1-0
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	-	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	-	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	-	-	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	-	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	-	0	-	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	-	-	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	-	-	-	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0





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