

**IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION**

JOLED INC.,

Plaintiff,

v.

SAMSUNG ELECTRONICS AMERICA,
INC., SAMSUNG DISPLAY CO., LTD.,
AND SAMSUNG ELECTRONICS CO.,
LTD.,

Defendants.

CASE NO. 6:20-cv-00559-ADA

DEFENDANTS' PROPOSED CLAIM CONSTRUCTIONS

Pursuant to the Court's Scheduling Order (Dkt. 24) and the Updated Standing Order Governing Proceedings—Patent Cases (Dkt. 22), Defendants Samsung Electronics America, Inc. ("SEA"), Samsung Display Co., Ltd. ("SDC"), and Samsung Electronics Co., Ltd. ("SEC") (collectively, "Defendants") hereby provide the following proposed constructions for claim terms from U.S. Patent Nos. 9,728,130 ("the '130 Patent"), 9,922,597 ("the '597 Patent"), 9,997,108 ("the '108 Patent"), 10,134,336 ("the '336 Patent"), and 10,198,992 ("the '992 Patent") (collectively, the "Asserted Patents") the parties previously identified for construction. The proposed constructions listed below are subject to the reservation of rights set forth in Defendants' January 25 Identification of Proposed Claim Terms for Construction. In addition, Defendants state that their review and analysis of the claim terms, the proposed constructions, and the supporting evidence, is ongoing, and the Scheduling Order requires the parties to meet and confer regarding their proposed constructions. Defendants reserve the right to add or drop claim terms, modify any of the claim language sought to be construed, and/or modify any of their proposed constructions, based on their continued review and analysis, the meet-and-confer process, or otherwise.

| Term | Defendants' Proposed Construction |
|---|---|
| <p>“a gate driver circuit which includes a first gate driver circuit, a second gate driver circuit” ('130, cls. 1, 13)</p> <p>“a gate driver circuit which includes a first gate driver circuit and a second gate driver circuit” ('597, cls. 1, 16) ('108, cls. 1, 16)</p> <p>“the gate driver circuit includes a first gate driver circuit and a second gate driver circuit” ('336, cls. 10, 18)</p> <p>“a gate driver circuit including a first gate driver circuit connected to the plurality of first gate signal lines and a second gate driver circuit connected to the plurality of second gate signal lines” ('992, cls. 1, 8, 10)</p> <p><i>Samsung identified</i></p> | <p><i>a gate driver circuit which contains two separate shift registers, the first shift register controlling a first gate signal line and the second shift register controlling a second gate signal line, and which may contain other circuitry</i> ('130, cls. 1, 13) ('597, cls. 1, 16) ('108, cls. 1, 16)</p> <p><i>the gate driver circuit contains two separate shift registers, the first shift register controlling a first gate signal line and the second shift register controlling a second gate signal line, and may contain other circuitry</i> ('336, cls. 10, 18)</p> <p><i>a gate driver circuit which contains two separate shift registers, the first shift register controlling and connected to the first gate signal lines and the second shift register controlling and connected to the second gate signal lines, and which may contain other circuitry</i> ('992, cls. 1, 8, 10)</p> |
| <p>“the first switching transistor and the second switching transistor are independently on/off controlled by the first gate driver circuit and the second gate driver circuit” ('130, cl. 1)</p> <p>“independently on/off controlling the first switching transistor and the second switching transistor by the first gate driver circuit and the second gate driver circuit” ('130, cl. 13)</p> <p>“wherein, by the first gate driver circuit and the second gate driver circuit, the first switch transistor is independently on/off controlled from the second switch transistor and the third switch transistor” ('597, cl. 4) ('108, cl. 4)</p> | <p><i>the first switch transistor is controlled by the first gate driver circuit and the second switch transistor is controlled by the second gate driver circuit, such that the two transistors are, at different points in time, (i) both in an on state, (ii) both in an off state, and (iii) in opposite states</i> ('130, cl. 1)</p> <p><i>controlling the first switching transistor by the first gate driver circuit and controlling the second switch transistor by the second gate driver circuit, such that the two transistors are, at different points in time, (i) both in an on state, (ii) both in an off state, and (iii) in opposite states</i> ('130, cl. 13)</p> <p><i>wherein the first switch transistor is controlled by the first gate driver circuit and the second and third switch transistors are controlled by the second gate driver circuit, such that the first and second switch transistors are, at different points in time, (i) both in an on state, (ii) both in an off state, and (iii) in opposite states, and the first and third switch transistors are, at different</i></p> |

| Term | Defendants' Proposed Construction |
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| <p>“wherein the first switch transistor and the second switch transistor are independently on/off controlled by the first gate driver circuit and the second gate driver circuit” (’336, cl. 11)</p> <p>“the first gate driver circuit and second gate driver circuit control the first gate signal line and the second gate signal line independently” (’336, cl. 18)</p> <p><i>Samsung identified</i></p> | <p><i>points in time, (i) both in an on state, (ii) both in an off state, and (iii) in opposite states</i> (’597, cl. 4) (’108, cl. 4)</p> <p><i>wherein the first switch transistor is controlled by the first gate driver circuit and the second switch transistor is controlled by the second gate driver circuit, such that the two transistors are, at different points in time, (i) both in an on state, (ii) both in an off state, and (iii) in opposite states</i> (’336, cl. 11)</p> <p><i>the first gate driver circuit controls the first gate signal line and the second gate driver circuit controls the second gate signal line, such that the two lines have, at different points in time, (i) both an on signal, (ii) both an off signal, and (iii) the opposite signals</i> (’336, cl. 18)</p> |
| <p>“the first gate driver circuit is configured to select the plurality of first gate signal lines as a block simultaneously” (’108, cl. 6) (’992, cls. 6, 14)</p> <p>“selecting, by the first gate driver circuit, the plurality of first gate signal lines as a block simultaneously” (’108, cl. 20)</p> <p>“selecting the plurality of first gate signal lines via the first gate driver circuit as a block simultaneously” (’992, cl. 8)</p> <p><i>Samsung identified</i></p> | <p><i>the first gate driver circuit is configured to output an on voltage to the control line, which applies the voltage simultaneously to the plurality of first gate signal lines as a block</i> (’108, cl. 6) (’992, cls. 6, 14)</p> <p><i>outputting an on voltage, by the first gate driver circuit, to the control line, which applies the voltage simultaneously to the plurality of first gate signal lines as a block</i> (’108, cl. 20)</p> <p><i>outputting an on voltage by the first gate driver circuit to the control line, which applies the voltage simultaneously to the plurality of first gate signal lines as a block</i> (’992, cl. 8)</p> |
| <p>“the source driver circuit [is/being] provided as a semiconductor chip and [is/being] attached to the EL display apparatus” (’130, cls. 1, 13)</p> <p><i>Samsung identified</i></p> | <p>Indefinite. (’130, cls. 1, 13)</p> |
| <p>“the second gate driver circuit is arranged at a second side of the display screen” (’130, cl. 4)</p> | <p><i>the second gate driver circuit is not located on the same side of the display screen as the first gate driver circuit</i> (’130, cl. 4)</p> |

| Term | Defendants' Proposed Construction |
|---|---|
| <p><i>Samsung identified</i></p> <p>“initially resetting the pixel circuit” (’597, cls. 1, 16) (’108, cls. 1, 16)</p> <p>“initially resets the pixel circuit” / (’108, cls. 1, 16)</p> <p>“resetting...[a/the] second pixel” (’597, cls. 16, 17) (’108, cls. 16, 17)</p> <p><i>Samsung identified</i></p> | <p><i>initially turning off the driving transistor of the pixel circuit</i> (’597, cls. 1, 16) (’108, cls. 1, 16)</p> <p><i>initially turns off the driving transistor of the pixel circuit</i> (’108, cls. 1, 16)</p> <p><i>turning off the driving transistor of...[a/the] second pixel</i> (’597, cls. 16, 17) (’108, cls. 16, 17)</p> |
| <p>“initially resets [a/the] gate terminal of the driving transistor” / (’597, cls. 1, 6, 16) (’108, cls. 7, 9, 18)</p> <p>“a gate terminal of the driving transistor is initially reset” / (’597, cl. 16)</p> <p>“[a/the] gate terminal of the driving transistor is reset” (’597, cl. 17) (’108, cls. 17, 19)</p> <p><i>Samsung identified</i></p> | <p><i>initially applies an OFF signal to [a/the] gate terminal of the driving transistor to turn the driving transistor off</i> (’597, cls. 1, 6, 16) (’108, cls. 7, 9, 18)</p> <p><i>an OFF signal is initially applied to a gate terminal of the driving transistor to turn the driving transistor off</i> (’597, cl. 16)</p> <p><i>an OFF signal is applied to [a/the] gate terminal of the driving transistor to turn the driving transistor off</i> (’597, cl. 17) (’108, cls. 17, 19)</p> |
| <p>“initially resetting the pixel circuit” (’597, cls. 1, 16) (’108, cls. 1, 16)</p> <p>“initially resets a gate terminal of the driving transistor” (’597, cls. 1, 6, 16) (’108, cls. 7, 9, 18)</p> <p>“resetting . . . a second pixel” (’597, cls. 16, 17) (’108, cls. 16, 17)</p> <p><i>JOLED identified</i></p> | <p>(See above constructions).</p> |

| Term | Defendants' Proposed Construction |
|---|---|
| <p>“when the third switch transistor initially resets the gate terminal of the driving transistor” (’597, cls. 1, 16)</p> <p>“when the third switch transistor initially resets the pixel circuit” (’108, cl. 1)</p> <p>“when the third switch transistor initially resets the pixel circuit” (’108, cl. 16)</p> <p><i>Samsung identified</i></p> | <p><i>when the third switch transistor of the Nth row initially resets the gate terminal of the driving transistor of the Nth row</i> (’597, cls. 1, 16)</p> <p><i>when the third switch transistor of the Nth pixel row initially resets the pixel circuit of the Nth pixel row</i> (’108, cl. 1)</p> <p><i>when the third switch transistor of the Nth pixel row initially resets the pixel circuit of the Nth pixel row</i> (’108, cl. 16)</p> |
| <p>“the first switch transistor of the Nth row is controlled in an OFF state by the first gate driver circuit” (’597, cl. 10)</p> <p>“the first switch transistor of the Nth pixel row is controlled in an OFF state by the first gate driver circuit” (’108, cl. 11)</p> <p><i>Samsung identified</i></p> | <p><i>the first switch transistor of the Nth row is connected to the first gate driver circuit or alternatively indefinite.</i> (’597, cl. 10)</p> <p><i>the first switch transistor of the Nth pixel row is connected to the first gate driver circuit or alternatively indefinite.</i> (’108, cl. 11)</p> |
| <p>“the gate driver circuit is configured to change a ratio of an area of the plurality of band-shaped non-display regions on the display screen to an area of the plurality of band-shaped display regions on the display screen depending on at least one of a brightness adjustment, a type of image data, or whether a display image is a motion image or a still image” (’336, cls. 1, 19)</p> <p>“the gate driver circuit is configured to change a number of divisions by which the display screen is divided into the plurality of band-shaped non-display regions and the plurality of band-shaped display regions depending on the type of image data” (’336, cl. 6)</p> <p>“type of image data” (’336, cls. 1, 6, 19)</p> | <p>Indefinite (’336, cls. 1, 6, 19)</p> |

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