UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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XILINX, INC.,
Petitioner,

v.

FG SRC LLC,
Patent Owner.

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IPR2021-00633
Patent 7,149,867 B2

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Before KALYAN K. DESHPANDE, GREGG I. ANDERSON, and
KARA L. SZPONDOWSKI, *Administrative Patent Judges.*

SZPONDOWSKI, *Administrative Patent Judge.*

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314
Granting Motion for Joinder
35 U.S.C. 315(c), 37 C.F.R. § 42.122(b)

I.   INTRODUCTION

Xilinx, Inc. ("Petitioner") filed a Petition requesting *inter partes* review of claims 1–19 of U.S. Patent 7,149,867 B2 (Ex. 1001, "the '867 patent"). Paper 2 ("Pet."). Concurrently, Petitioner filed a Motion for Joinder pursuant to 35 U.S.C. § 315(c) and 37 C.F.R. § 42.122(b), seeking to be joined as a party to *Intel Corp. v. FG SRC LLC*, Case IPR2020-01449 (PTAB March 3, 2021) ("the Intel IPR"), which also concerns claims 1–19 of the '867 patent. Paper 3 ("Motion").   Patent Owner FG SRC LLC ("Patent Owner") filed an Opposition to Petitioner's Motion for Joinder and Motion for Additional Discovery. Paper 7 ("Opposition").[1] With our authorization, Petitioner filed a Reply to Patent Owner's Opposition to Petitioner's Motion for Joinder (Paper 9, "Reply") and Patent Owner filed a Sur-reply in Support of Its Opposition to Petitioner's Motion for Joinder (Paper 10, "Sur-Reply"). In addition, Patent Owner filed a Preliminary Response to the Petition. Paper 12 ("Prelim. Resp.").

We have jurisdiction under 35 U.S.C. §§ 6, 314 and 37 C.F.R. § 42.4. For the reasons discussed below, we determine institution of *inter partes* review is warranted on the same grounds instituted in the Intel IPR and grant Petitioner's Motion for Joinder.

II.   BACKGROUND

A.   Real Parties in Interest

Petitioner identifies itself as the sole real party in interest. Pet. 1. Patent Owner identifies FG SRC LLC as the sole real party in interest. Paper 5, 2.

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[1] Patent Owner's Motion for Additional Discovery was denied. *See* Paper 11.

B. Related Matters

The parties advise that the '867 patent is the subject of the following district court litigations:

FG SRC LLC v. Intel Corporation, 6:20-cv-00315-ADA (W.D. Tex.) filed April 24, 2020 ("the related district court proceeding");

FG SRC LLC v. Xilinx, Inc., 1:20-cv-00601-LPS (D. Del), filed April 30, 2020; and

SRC Labs, LLC et al., v. Amazon Web Services, Inc., et al., 2:18-cv-00317-JLR (W.D. Wash.), filed February 26, 2018.
Pet. 1–2; Paper 5, 2.

The Parties also advise that the '867 patent is currently pending in the Intel IPR, and Petitioner advises that the '867 patent was the subject of IPR2019-00103 (institution denied on May 10, 2019). Pet. 2; Paper 5, 2.

C. The '867 Patent (Ex. 1001)

The '867 patent issued from Application No. 10/869,200 filed June 16, 2004, and claims the benefit of Provisional Application No. 60/479,339, filed June 18, 2003. Ex. 1001, codes [21], [22], [60]. The '867 patent is titled "System and Method of Enhancing Efficiency and Utilization of Memory Bandwidth in Reconfigurable Hardware" and is generally directed to "enhancing the efficiency and utilization of memory bandwidth in reconfigurable hardware" and "implementing explicit memory hierarchies in reconfigurable processors that make efficient use of off-board, on-board, on-chip storage and available algorithm locality." *Id.* at code [57], 1:15–24.

1. Background and Summary of the Problem

The '867 patent explains that microprocessors "have enjoyed annual performance gains averaging about 50% per year," where most of the gains were attributable to higher clock processor speeds, more memory bandwidth,

and increasing utilization of instruction level parallelism ("ILP") at execution time. *Id.* at 1:26–30. However, as microprocessor speeds increased, designing memory hierarchies that could keep up became challenging. *Id.* at 1:31–33. Therefore, "there has been significant effort spent on the development of memory hierarchies that can maintain high bandwidth efficiency and utilization with faster microprocessors." *Id.* at 1:48–50.

The '867 explains that one approach to improving bandwidth efficiency and utilization in memory hierarchies is the utilization of cache memories. *Id.* at 1:51–53. In designing cache memories, there are a number of considerations to take into account, such as the width of the cache line, cache associativity, how cache lines are replaced due to a capacity or conflict miss, the write policy for the cache, and the size and speed of the cache. *Id.* at 1:59–3:15. For example, wide cache lines are more efficient for programs that exhibit a high degree of spatial locality (i.e., it is likely that other data within the same cache line will be needed). *Id.* at 1:64–2:4. However, narrow cache lines are more efficient for programs that have low levels of spatial locality. *Id.* at 2:4–7. The '867 patent states that the various considerations and tradeoffs makes cache design challenging for a multipurpose computer that executes a wide variety of programs in that "it is very difficult to design a single cache structure that is optimized for many different programs." *Id.* at 3:28–30. Cache designers try to derive the program behavior of the "average" program, and optimize the cache for the "average" program. *Id.* at 3:32–36. As a result, the cache is sub-optimal for most programs, because most programs that actually run on the microprocessor are not "average." *Id.* at 3:36–39.

2. The Claimed Invention of the '867 Patent

According to the '867 patent, because of the foregoing issues, there was a growing need to develop improved memory hierarchies that limited overhead of a memory hierarchy without also reducing bandwidth efficiency and utilization. *Id.* at 3:57–60. To address this need, the '867 patent describes a system including a memory hierarchy and a reconfigurable processor that includes a data prefetch unit. *Id.* at 4:4–10, 5:60–62, 6:9–13, 7:34–48. The '867 patent states that a "Reconfigurable Processor" is "a computing device that contains reconfigurable components such as FPGAs [(field programmable gate arrays)] and can, through reconfiguration, instantiate an algorithm as hardware." *Id.* at 5:26–29. The '867 patent states that a "Data prefetch Unit" is "a functional unit [a set of logic that performs a specific operation] that moves data between members of a memory hierarchy [a collection of memories]," where such "movement may be as simple as a copy, or as complex as an indirect indexed strided copy into a unit stride memory." *Id.* at 5:34–43.

Figure 1 of the '867 patent, reproduced below, shows a reconfigurable processor (RP) 100 of the claimed invention. *Id.* at 4:38–40.

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