

**IN THE UNITED STATES DISTRICT COURT  
FOR THE WESTERN DISTRICT OF TEXAS  
AUSTIN DIVISION**

FG SRC LLC,

Plaintiff,

v.

INTEL CORPORATION,

Defendant.

Case No. 1:20-cv-00834-ADA

JURY TRIAL DEMANDED

**PLAINTIFF FG SRC LLC'S OPENING CLAIM CONSTRUCTION BRIEF**

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EXHIBIT	DESCRIPTION
A	U.S. Patent No. 7,149,867
B	Declaration of Ryan Kastner, Ph.D., dated November 17, 2020, referred to herein as “Kastner Dec.”
C	Excerpt from Ryan Kastner, Ph.D., et al. Parallel Programming for FPGAs 18 (2020), available at <a href="http://kastner.ucsd.edu/hlsbook/">http://kastner.ucsd.edu/hlsbook/</a> .

Plaintiff FG SRC LLC (“SRC”) submits its opening claim construction brief which includes proper constructions and related argument for the disputed terms of U.S. Patent No. 7,149,867 (“’867 patent”).

## I. GENERAL TECHNICAL BACKGROUND

### A. Processor Types

The ’867 patent relates to the use of reconfigurable processors, such as Field Programmable Gate Arrays (“FPGAs”). Ex. A 1:16-24, 5:26-29. An FPGA is an integrated circuit that contains an array of programmable logic blocks and memory elements connected via programmable interconnect. Kastner Dec. ¶ 14. A user can program an FPGA to perform a specific function by configuring the logic blocks and interconnect. *Id.* This enables the user to create a hardware accelerated implementation of an algorithm by programming the FPGA in a manner that efficiently executes the algorithm. *Id.* In other words, with a reconfigurable processor such as an FPGA, the hardware adapts to the algorithm.

This can be contrasted with implementing the algorithm with software on a CPU or microprocessor. *Id.* ¶ 15. A CPU executes the algorithm by performing a sequence of instructions (e.g., arithmetic, logical, memory (load/store)) that implement the algorithm. *Id.* A different algorithm can be implemented on the CPU by changing the instructions. *Id.* The CPU is flexible; it can implement almost any algorithm. *Id.* Because the CPU hardware is fixed, it cannot be customized towards the algorithm like an FPGA implementation. *Id.* These customizations allow FPGA implementations to be orders of magnitude more efficient than implementing that algorithm as software on a CPU. *Id.*

In addition to FPGAs and CPUs, Application-Specific Integrated Circuits (“ASICs”) can also be used to execute algorithms. *Id.* ¶ 16. ASICs use custom logic and are manufactured specifically to perform one application. *Id.* Because an ASIC is purpose-built for one application, it is very

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