EXHIBIT B

IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION

FG SRC LLC, Plaintiff, v. INTEL CORPORATION, Defendant.	CIVIL ACTION NO. 1:20-CV-00834-ADA JURY TRIAL DEMANDED

DECLARATION OF RYAN KASTNER, PH.D. IN SUPPORT OF FG SRC LLC'S OPENING CLAIM CONSTRUCTION BRIEF

I hereby declare as follows:

1. I have been asked by counsel for Plaintiff FG SRC LLC ("SRC") to offer my opinions regarding claim construction for certain terms.

2. In connection with the preparation of this Declaration, I have reviewed materials including the following:

- U.S. Patent No. 7,149,867 (the "'867 patent");
- The file wrapper for the '867 patent;
- The parties' respective claim constructions as set forth in SRC's Opening Claim Construction Brief;
- SRC's Identification of Extrinsic Evidence for Claim Construction and materials cited therein;
- Defendant Intel Corporation's ("Intel") Identification of Extrinsic Evidence for Claim Construction and materials cited therein; and
- any additional materials cited herein or in SRC's Opening Claim Construction Brief.

3. All of the opinions stated in this Declaration are based on my personal knowledge and professional judgment. I am over 18 years old and if called as a witness, I am prepared to testify competently about them. I declare that all statements made herein are within my knowledge and believed to be true and correct.

I. EXPERIENCE AND QUALIFICATIONS

4. I have over twenty (20) years of experience as a computer scientist and engineer, specifically in the areas of hardware acceleration, hardware design, and embedded systems. I have worked extensively on and with FPGAs and other systems for hardware implementation and acceleration of algorithms.

5. I am currently a Professor in the Department of Computer Science and Engineering at the University of California San Diego. I co-direct the Wireless Embedded Systems Graduate Program, the Engineers for Exploration Program, and lead the Kastner Research group with the goal of developing accelerated computer systems using FPGAs for applications including computer vision, bioinformatics, and communication systems.

6. I completed dual bachelor's degrees in Electrical Engineering and Computer Engineering at Northwestern University and went on to receive a master's degree in engineering from the same university. Afterward, I received my Ph.D. in Computer Science from the University of California Los Angeles, with a focus in embedded and reconfigurable systems. Following my doctoral degree, I became an Assistant Professor at the University of California Santa Barbara and established a research group to advance hardware research in reconfigurable computing, hardware security, and underwater sensor networks.

7. In 2007 I began my current position as a professor at the University of California San Diego where I have continued my research into hardware acceleration, hardware security, and

embedded systems. Our achievements have included developing systems for automated fish identification, cell sorting, optical cardiac imaging, fast 3D object reconstruction, and high-speed genome reconstruction.

8. In addition to my work at UCSD, I co-founded Tortuga Logic, a hardware security company, in order to bring developments from my research group to market. The company has since achieved great success and been awarded contracts with the U.S. Department of Defense among many other clients.

9. I am a named inventor on five U.S. patents for inventions relating to hardware design, security, and computer science generally, with two additional applications in the works.

a. System and Method for Eliminating Common Subexpressions in a Linear System (with Farzan Fallah and Anup Hosangadi) (USPTO: 7,895,420, Feb. 22, 2011).

b. Designing Digital Processors Using a Flexibility Metric (with Ali Irturk), (USPTO: 8,812,285, Aug. 19, 2014).

c. Method and Systems for Detecting and Isolating Hardware Timing Channels (with Jason Oberg, Sarah Meiklejohn, and Timothy Sherwood) (USPTO:9,305,166, Apr. 5, 2014**).**

d. Method and System Providing Multi-Level Security to Gate Level Information Flow (with Jason Oberg, Wei Hu, Timothy Sherwood, and Mohit Tiwari), (USPTO: 10,083,305, Sep. 25, 2018).

e. Generating Hardware Security Logic (with Jason Oberg, Jonathan Valamehr, and Timothy Sherwood) (USPTO: 10, 289,873, May 14, 2019).

f. Method and System for Detecting Hardware Trojans and Unintentional

Design Flaws (with Wei Hu and Jason Oberg) (USPTO Application No: 2018/0032760, filed July 207, 2017).

g. Techniques for Improving Security of Circuitry Designs Based on a Hardware Description Language (with Armaiti Ardenshiricham and Wei Hu) (USPTO Application No: 2019/0286763, filed Mar. 14, 2019).

10. I have authored multiple books, including "Parallel Programming for FPGAs" published by *ArXiv e-prints* (arXiv: 1805.03648), "Handbook on FPGA Design Security" published by *Springer* (ISBN: 9789048191567), "Arithmetic Optimization Techniques for Hardware and Software Design" published by *Cambridge University Press* (ISBN: 9780521880992), and "Synthesis Techniques and Optimizations for Reconfigurable Systems" published by *Kluwer Academic Publishers* (ISBN: 1402075983). I have authored or co-authored at least 61 refereed journal papers on numerous topics regarding hardware design, reconfigurable computing, security, and computer science generally. Additionally, my research group and I have authored or co-authored at least 158 refereed conference papers on similar topics. I have supervised doctoral dissertations and master's theses on a broad range of topics across electrical and computer engineering, computer science, and data science. I have developed and taught courses regarding embedded systems, systems programming, hardware design, and robotics, among other topics.

11. A more complete list of my qualifications and experience is set forth in my curriculum vitae, a true and correct copy of which is attached hereto as Exhibit 1.

12. I am being paid for work in this matter. My compensation is in no way dependent upon the outcome of this litigation nor do I have a personal interest in the outcome of this litigation.

II. LEVEL OF ORDINARY SKILL IN THE ART

13. A person of ordinary skill in the art ("POSITA") at the time of the filing of the '867

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