Proceedings

International Conference on Computer Design

VLSI in Computers and Processors

October 12-15, 1997

Austin, Texas

Sponsored by

IEEE Computer Society Technical Committee on Design Automation

IEEE Circuits and Systems Society

Los Alamitos, California

Washington • Brussels • Tokyo

DOCKET ALARM

Find authenticated court documents without watermarks at docketalarm.com.

Copyright © 1997 by The Institute of Electrical and Electronics Engineers, Inc.
All rights reserved

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries may photocopy beyond the limits of US copyright law, for private use of patrons, those articles in this volume that carry a code at the bottom of the first page, provided that the per-copy fee indicated in the code is paid through the Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

Other copying, reprint, or republication requests should be addressed to: IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, P.O. Box 133, Piscataway, NJ 08855-1331.

The papers in this book comprise the proceedings of the meeting mentioned on the cover and title page. They reflect the authors' opinions and, in the interests of timely dissemination, are published as presented and without change. Their inclusion in this publication does not necessarily constitute endorsement by the editors, the IEEE Computer Society, or the Institute of Electrical and Electonics Engineers, Inc.

IEEE Computer Society Order Number PR08026
ISBN 0-8186-8026-X
ISBN 0-8186-8207-8 (case)
ISBN 0-8186-8208-6 (microfiche)
IEEE Order Plan Catalog Number 97CB36149
ISSN 1063-6404

Additional copies may be ordered from:

IEEE Computer Society
Customer Service Center
10662 Los Vaqueros Circle
P.O. Box 3014
Los Alamitos, CA 90720-1314
Tel: + 1-714-821-8380
Fax: + 1-714-821-4641
E-mail: cs.books@computer.org

IEEE Service Center
445 Hoes Lane
P.O. Box 1331
Piscataway, NJ 08855-1331
Tel: + 1-908-981-1393
Fax: + 1-908-981-9667
mis.custserv@computer.org

IEEE Computer Society
13, Avenue de l'Aquilon
B-1200 Brussels
BELGIUM
Tel: + 32-2-770-2198
Fax: + 32-2-770-8505
euro.ofc@computer.org

IEEE Computer Society
Ooshima Building
2-19-1 Minami-Aoyama
Minato-ku, Tokyo 107
JAPAN
Tel: + 81-3-3408-3118
Fax: + 81-3-3408-3553
tokyo.ofc@computer.org

Editorial production by Ian Torwick

Cover design by Joseph Daigle/Studio Productions

Printed in the United States of America by Technical Communication Services

DOCKET ALARM
Find authenticated court documents without watermarks at docketalarm.com.

Table of Contents

ICCD '97 Conference Program

1997 Technical Program

Welcome to ICCD'97 xiv
Program Committee xvi
Additional Referees xix

Session 1.1: Keynote Speech
Intelligent RAM (IRAM): the Industrial Setting, Applications, and Architectures 2
D. Patterson, K. Asanovic, A. Brown, R. Fromm, J. Golbus, B. Gribstad, K. Keeton, C. Kozyrakis, D. Martin, S. Perissakis, R. Thomas, N. Treuhaft, and K Yelick, University of California at Berkeley, California

Session 1.2: CAD Plenary
Chair: Andreas Kuehlmann, IBM T. J. Watson Research Center
A Brief History of the Future of Semiconductor Electronic Design Automation 10
Ron Rohrer, TBD Consultants

Concurrent Sessions 1.3

Session 1.3.1: Special Session: Industrial Applications of Formal Verification
Organizer and Chair: Andreas Kuehlmann, IBM T. J. Watson Research Center
Formal Implementation Verification of the Bus Interface Unit for the Alpha 21264 Microprocessor 16
G.P. Bischoff, K.S. Brace, S. Jain, and R. Razdan
Intertwined Development and Formal Verification of a 60x bus Model 25
M. Kaufmann and C. Pixley
Formally Specifying and Mechanically Verifying Programs for the Motorola Complex Arithmetic Processor DSP 31
B.C. Brock and W.A. Hunt, Jr.
BIST-Based Fault Diagnosis in the Presence of Embedded Memories 37
J. Savir
Built-in Self Test for Content Addressable Memories 48
Y.-S. Kang, J.-C. Lee, and S. Kang
Pseudo-Random Pattern Testing of Bridging Faults 54
N.A. Touba and E.J. McCluskey

Session 1.3.3: Simulation and Power Estimation
Chair: Teng-Sheng Moh, Silicon Valley Research, Inc.
Novel Simulation of Deep-Submicron MOSFET Circuits 62
S. Bruma and R.H.J.M. Otten
Time-Stamped Transition Density for the Estimation of Delay Dependent Switching Activities 68
H. Choi and S.H. Hwang

DOCKET ALARM
Find authenticated court documents without watermarks at docketalarm.com.

Power Compiler: A Gate-Level Power Optimization and Synthesis System 74
B. Chen and I. Nedelchev

Session 1.3.4: Branch Prediction
Chair: Jim Bondi, Texas Instruments

Elastic History Buffer: A Low-Cost Method to Improve Branch Prediction Accuracy 82
M.-D. Tarlescu, K.B. Theobald, and G.R. Gao

Design Optimization for High-Speed Per-address Two-level Branch Predictors 88
I.-C.K. Chen, C.-C. Lee, M.A. Postiff, and T.N. Mudge

PA-8000: A Case Study of Static and Dynamic Branch Prediction 97
C. Burch

Concurrent Sessions 1.4

Session 1.4.1: New Techniques for Gate-Sizing and Retiming
Chair: Derek Beatty, Motorola, Inc.

Discrete Drive Selection for Continuous Sizing 110
R. Haddad, L.P.P.P. van Ginneken, and N. Shenoy

Continuous Retiming: Algorithms and Applications 116
P. Pan

Optimal Clock Period Clustering for Sequential Circuits with Retiming 122
A.K. Karandikar, P. Pan, and C.L. Liu

Session 1.4.2: Circuit Modeling
Chair: Sandip Kundu, IBM Corp.

Comparison between nMOS Pass-Transistor logic style vs. CMOS Complementary Cells 130
R. Mehrotra, M. Pedram, and X. Wu

Circuit-Based Description and Modeling of Electromagnetic Noise Effects in Packaged Low-Power Electronics 136
A.C. Cangellaris, W. Pinello, and A. Ruehli

Transistor-Level Sizing and Timing Verification of Domino Circuits in the Power PC Microprocessor 143
A. Dharchoudhury, D. Blaauw, J. Norton, S. Pullela, and J. Dunning

Session 1.4.3: Novel Architectures
Chair: Greg Fisher, Printronix Corporation

Architectural Adaptation for Application-Specific Locality Optimization 150
X. Zhang, A. Dasdan, M. Schulz, R.K. Gupta, and A.A. Chien

A New Processor Architecture for Digital Signal Transport Systems 157
M. Inamori, K. Ishii, A. Tsutsui, K. Shirakawa H. Nakada, and T. Miyazaki

Short Papers

PROPHID: A Heterogeneous Multi-Processor Architecture for Multimedia 164
J.A. Leijten, J.L. van Meerbergen, A.A. Timmer, and J.A.G. Jess

DOCKET ALARM
Find authenticated court documents without watermarks at docketalarm.com.

Enhanced Compression Techniques to Simplify Program Decompression and Execution 170
M. Breternitz, Jr. and R. Smith

Session 1.4.4: Low Power Architectures
Chair: Tim Brodnax, IBM

A Low Power Approach to Floating Point Adder Design 178
R.V.K. Pillai, D. Al-Khalili, and A.J. Al-Khalili
Design and Implementation of Low-Power Digit-Serial Multipliers 186
Y.-N. Chang, J.H. Satyanarayana, and K.K. Parhi
On Complexity Reduction of FIR Digital Filters Using Constrained Least Squares Solution 196
K. Muhammad and K. Roy

Concurrent Session 1.5

Session 1.5.1: Timing Optimization for Deep Submicron Technology
Chair: Masahiro Fujita, Fujitsu Laboratories of America

An Integrated Placement and Synthesis Approach for Timing Closure of PowerPC™ Microprocessors 206
S. Hojat and P. Villarrubia
Post-Layout Circuit Speed-up by Event Elimination 211
H. Vaishnav, C.-K. Lee, and M. Pedram
Clustering and Load Balancing for Buffered Clock Tree Synthesis 217
A.D. Mehta, Y.-P. Chen, N. Menezes, D.F. Wong, and L.T. Pileggi
CMOS Gate Delay Models for General RLC Loading 224
R. Arunachalam, F. Dartu, and L.T. Pileggi

Session 1.5.2: Special Session: The G4 S/390 Microprocessor
Organizer: Andreas Kuehlmann, IBM T. J. Watson Research Center
Chair: Sumit Dasgupta, IBM

Design Methodology for the High-Performance G4 S/390 Microprocessor 232
K.L. Shepard, S. Carey, D.K. Beece, R. Hatch, and G. Northrop
A High-Frequency Custom CMOS S/390 Microprocessor 241
C.F. Webb and J.S. Liptay
High Performance CMOS Circuit Techniques for the G-4 S/390 Microprocessor 247
J. Warnock, L. Sigal, B. Curran, and Y. Chan
A 400 MHz, 144Kb CMOS ROM MACRO for an IBM S/390-Class Microprocessor 253
A. Tuminaro

Session 1.5.3: Multiprocessor Communication
Chair: Wai-Chi Fang, Jet Propulsion Laboratory

A Comparative Evaluation of Hierarchical Network Architecture of the HP-Convex Exemplar 258
R. Castaneda, X. Zhang, and J.M. Hoover, Jr.

DOCKET ALARM
Find authenticated court documents without watermarks at docketalarm.com.

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.