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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	SRC028
First Inventor	Daniel Poznanovic et al.
Title	SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE
Express Mail Label No.	EV331755319US

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPLICATION ELEMENTS

1. ☒ Fee Transmittal Form (submit an original and a duplicate for fee processing)
2. ☐ Applicant claims small entity status. See 37 CFR 1.27
3. ☒ Specification [total pages 26]
   (preferred Arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R&D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. ☒ Drawing(s) [total sheets 12]
5. ☒ Oath or Declaration [total pages 3]
   a. ☒ Newly executed (original or copy)
   b. ☐ Copy from prior appl. (37 C.F.R. § 1.63(d)) (for continuation/divisional with Box 18 completed)
      i. ☐ DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in prior application, see 37 C.F.R. §§ 1.63(d)(2) and1.33(b).
6. ☐ Application Data Sheet. (See 37 CFR 1.76
7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program (Appendix)
8. Nucleotide and/or Amino Acid Sequence Submission (if *applicable, all necessary)*
   a. ☐ Computer Readable Form
   b. ☐ Specification Sequence Listing on:
      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ paper
   c. ☐ Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. ☒ Assignment Papers (coversheet/document(s))
10. ☐ 37 CFR. 3.73(b) Statement (*when there is an assignee*) ☒ Power of Attorney
11. ☐ English Translation Document
12. ☐ IDS & Form PTO/SB/08A ☐ Copies of IDS Citations
13. ☐ Preliminary Amendment
14. ☒ Return Receipt Postcard (MPEP 503)
15. ☐ Certified Copy of Priority Document(s)
16. ☐ Nonpublication Request Under 35 USC 122(b)(2)(B)(i).Applicant must attach form PTO/SB/35
17. ☒ Other: Certificate of Mailing by Express Mail

18. **If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:**

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: __/_____

Prior application information: *Examiner:* _____ *Group/Art Unit:* _____

FOR CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted form the submitted application parts.

19. CORRESPONDENCE ADDRESS

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(Signature)		Date	16 Aug 2004

\\\CS - 80404/0033 - 68264 v1

EXPRESS MAIL NO. EV331755319US
Attorney Docket No. SRC028
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Daniel Poznanovic, David E. Caliga, and Jeffrey Hammes Serial No. NEW Filed: Herewith	For: SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE

CERTIFICATE OF MAILING BY EXPRESS MAIL

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Alexandria, VA 22313-1450

Sir:

The undersigned hereby certifies that the following documents:

1. Utility Patent Application Transmittal;
2. Fee Transmittal and $928 filing fee;
3. Utility Patent Application- 22 pgs. Spec, 3 pgs. Claims, 1 pg. Abstract;
4. Executed Declaration for Utility Patent Application;
5. 12 sheets of drawings;
6. Recordation Form Cover Sheet PTO 1595 with Executed Assignment and Recording Fee of $40.00;
7. Return postcard; and
8. Certificate of Mailing By Express Mail

relating to the above application, were deposited as "Express Mail", Mailing Label No. EV331755319US, with the United States Postal Service, addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

16 June 2004
Date

Mailer

16 June 2004
Date

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FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT **($) 968.00**

Complete if Known	
Application Number	--------
Filing Date	Herewith
First Named Inventor	Daniel Poznanovic et al.
Examiner Name	
Group / Art Unit	
Attorney Docket No.	SRC028

METHOD OF PAYMENT (check all that apply)

☒ check ☐ credit card ☐ money order ☐ other ☐ none

☐ Deposit Account

Deposit Account Number: **50-1123**

Deposit Account Name: **Hogan & Hartson L.L.P.**

The Director is authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☒ Credit any overpayments

☒ Charge any additional fee(s) or any underpayment of fee(s)

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee ($)	Small Entity Fee ($)	Fee Description	Fee Paid
770	385	Utility Filing Fee	770.00
340	170	Design filing fee	
530	265	Plant filing fee	
770	385	Reissue filing fee	
160	80	Provisional filing fee	

SUBTOTAL (1) **($) 770.00**

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims		Fee from below		Fee Paid
Total Claims	24	-20**=	4	X 18	=	72.00
Independent Claims	4	-3**=	1	X 86	=	86.00
Multiple Dependent					=	

**or number previously paid, if greater; For Reissues, see below*

Large Entity Fee ($)	Small Entity Fee ($)	Fee Description
18	9	Claims in excess of 20
86	43	Independent claims in excess of 3
290	145	Multiple dependent claim, if not paid
86	43	**Reissue independent claims over original patent
18	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) **($) 158.00**

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee ($)	Small Entity Fee ($)	Fee Description	Fee Paid
130	65	Surcharge – late filing fee or oath	
50	25	Surcharge – late provisional filing fee or cover sheet	
130	130	Non-English specification	
2,520	2,520	For filing a request for ex parte reexamination	
920*	920*	Requesting publication of SIR prior to Examiner action	
1,840*	1,840*	Requesting publication of SRI after Examiner action	
110	55	Extension for reply within first month	
420	210	Extension for reply within second month	
950	475	Extension for reply within third month	
1,480	740	Extension for reply within fourth month	
2,010	1,005	Extension for reply within fifth month	
330	165	Notice of Appeal	
330	165	Filing a brief in support of an appeal	
290	145	Request for oral hearing	
1,510	1,510	Petition to institute a public use proceeding	
110	55	Petition to revive – unavoidable	
1,330	665	Petition to revive – unintentional	
1,330	664	Utility issue fee (or reissue)	
480	240	Design issue fee	
640	320	Plant issue fee	
130	130	Petitions to the Commissioner	
50	50	Processing fee under 37 CFR 1.17(q)	
180	180	Submission of Info Disclosure Stmt	
40	40	Recording each patent assignment per property (times number of properties)	40.00
770	385	Filing a submission after final rejection (37 CFR § 1.129(a))	
770	385	For each additional invention to be examined (37 CFR §1.129(b))	
770	385	Request for Continued Examination	
900	900	Request for expedited examination of a design application	
Other fee (specify)		.....	

*Reduced by Basic Fling Fee Paid **SUBTOTAL (3)** **($) 40.00**

SUBMITTED BY Complete *(if applicable)*

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Signature				Date	16 June 2004

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SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE

1. Related Applications.

[0001] The present invention claims the benefit of U.S. Provisional Patent application Serial No. 60/479,339 filed on June 18, 2003, which is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention.

[0002] The present invention relates, in general, to enhancing the efficiency and utilization of memory bandwidth in reconfigurable hardware. More specifically, the invention relates to implementing explicit memory hierarchies in reconfigurable processors that make efficient use of off-board, on-board, on-chip storage and available algorithm locality. These explicit memory hierarchies avoid many of the tradeoffs and complexities found in the traditional memory hierarchies of microprocessors.

2. Relevant Background.

[0003] Over the past 30 years, microprocessors have enjoyed annual performance gains averaging about 50% per year. Most of the gains can be attributed to higher processor clock speeds, more memory bandwidth and increasing utilization of instruction level parallelism (ILP) at execution time.

[0004] As microprocessors and other dense logic devices (DLDs) consume data at ever-increasing rates it becomes more of a challenge to design memory hierarchies that can keep up. Two measures of the gap between the microprocessor and memory hierarchy are bandwidth efficiency and bandwidth

utilization. Bandwidth efficiency refers to the ability to exploit available locality in a program or algorithm. In the ideal situation, when there is maximum bandwidth efficiency, all available locality is utilized. Bandwidth utilization refers to the amount of memory bandwidth that is utilized during a calculation. Maximum bandwidth utilization occurs when all available memory bandwidth is utilized.

[0005] Potential performance gains from using a faster microprocessor can be reduced or even negated by a corresponding drop in bandwidth efficiency and bandwidth utilization. Thus, there has been significant effort spent on the development of memory hierarchies that can maintain high bandwidth efficiency and utilization with faster microprocessors.

[0006] One approach to improving bandwidth efficiency and utilization in memory hierarchies has been to develop ever more powerful processor caches. These caches are high-speed memories (typically SRAM) in close proximity to the microprocessor that try to keep copies of instructions and data the microprocessor may soon need. The microprocessor can store and retrieve data from the cache at a much higher rate than from a slower, more distant main memory.

[0007] In designing cache memories, there are a number of considerations to take into account. One consideration is the width of the cache line. Caches are arranged in lines to help hide memory latency and exploit spatial locality. When a load suffers a cache miss, a new cache line is loaded from main memory into the cache. The assumption is that a program being executed by the microprocessor has a high degree of spatial locality, making it likely that other memory locations in the cache line will also be required.

[0008] For programs with a high degree of spatial locality (e.g., stride-one access), wide cache lines are more efficient since they reduce the number of times a processor has to suffer the latency of a memory access. However, for programs with lower levels of spatial locality, or random access, narrow lines

are best as they reduce the wasted bandwidth from the unused neighbors in the cache line. Caches designed with wide cache lines perform well with programs that have a high degree of spatial locality, but generally have poor gather/scatter performance. Likewise, caches with short cache lines have good gather/scatter performance, but loose efficiency executing programs with high spatial locality because of the additional runs to the main memory.

[0009] Another consideration in cache design is cache associativity, which refers to the mapping between locations in main memory and cache sectors. At one extreme of cache associativity is a direct-mapped cache, while at another extreme is a fully associative cache. In a direct mapped-cache, a specific memory location can be mapped to only a single cache line. Direct-mapped caches have the advantage of being fast and easy to construct in logic. The disadvantage is that they suffer the maximum number of cache conflicts. At the other extreme, a fully associative cache allows a specific location in memory to be mapped to any cache line. Fully associative caches tend to be slower and more complex due to the large amount of comparison logic they need, but suffer no cache conflict misses. Oftentimes, caches fall between the extremes of direct-mapped and fully associative caches. A design point between the extremes is a k-set associative cache, where each memory location can map to k cache sectors. These caches generally have less overhead than fully associative caches, and reduce cache conflicts by increasing the value of k.

[0010] Another consideration in cache design is how cache lines are replaced due to a capacity or conflict miss. In a direct-mapped cache, there is only one possible cache line that can be replaced due to a miss. However, in caches with higher levels of associativity, cache lines can be replaced in more that one way. The way the cache lines are replaced is referred to as the replacement policy.

[0011] Options for the replacement policy include least recently used (LRU), random replacement, and first in—first out (FIFO). LRU is used in the majority of circumstances where the temporal locality set is smaller than the cache size, but it is normally more expensive to build in hardware than a random replacement cache. An LRU policy can also quickly degrade depending on the working set size. For example, consider an iterative application with a matrix size of N bytes running through a LRU cache of size M bytes. If N is less than M, then the policy has the desired behavior of 100% cache hits, however, if N is only slightly larger than M, the LRU policy results in 0% cache hits as lines are removed just as they are needed.

[0012] Another consideration is deciding on a write policy for the cache. Write-through caches send data through the cache hierarchy to main memory. This policy reduces cache coherency issues for multiple processor systems and is best suited for data that will not be re-read by the processor in the immediate future. In contrast, write-back caches place a copy of the data in the cache, but does not immediately update main memory. This type of caching works best when a data just written to the cache is quickly requested again by the processor.

[0013] In addition to write-through and write-back caches, another kind of write policy is implemented in a write-allocate cache where a cache line is allocated on a write that misses in cache. Write-allocate caches improve performance when the microprocessor exhibits a lot of write followed by read behavior. However, when writes are not subsequently read, a write-allocate cache has a number of disadvantages: When a cache line is allocated, it is necessary to read the remaining values from main memory to complete the cache line. This adds unnecessary memory read traffic during store operations. Also, when the data is not read again, potentially useful data in the cache is displaced by the unused data.

[0014] Another consideration is made between the size and the speed of the cache: small caches are typically much faster than larger caches, but store less data and fewer instructions. Less data means a greater chance the cache will not have data the microprocessor is requesting (i.e., a cache miss) which can slow everything down while the data is being retrieved from the main memory.

[0015] Newer cache designs reduce the frequency of cache misses by trying to predict in advance the data that the microprocessor will request. An example of this type of cache is one that supports speculative execution and branch prediction. Speculative execution allows instructions that likely will be executed to start early based on branch prediction. Results are stored in a cache called a reorder buffer and retired if the branch was correctly predicted. Of course, when mis-predictions occur instruction and data bandwidth are wasted.

[0016] There are additional considerations and tradeoffs in cache design, but it should be apparent from the considerations described hereinbefore that it is very difficult to design a single cache structure that is optimized for many different programs. This makes cache design particularly challenging for a multipurpose microprocessor that executes a wide variety of programs. Cache designers try to derive the program behavior of "average" program constructed from several actual programs that run on the microprocessor. The cache is optimized for the average program, but no actual program behaves exactly like the average program. As a result, the designed cache ends up being sub-optimal for nearly every program actually executed by the microprocessor. Thus, there is a need for memory hierarchies that have data storage and retrieval characteristics that are optimized for actual programs executed by a processor.

[0017] Designers trying to develop ever more efficient caches optimized for a variety of actual programs also face another problem: as caches add additional features, the overhead needed to implement the added features also grows.

Caches today have so much overhead that microprocessor performance may be reaching a point of diminishing returns as the overhead starts to cut into performance. In the Intel Pentium III processor for example, more than half of the 10 million transistors are dedicated to instruction cache, branch prediction, out-of-order execution and superscalar logic. The situation has prompted predictions that as microprocessors grow to a billion transistors per chip, performance increases will drop to about 20% per year. Such a prediction, if borne out, could have a significant impact on technology growth and the computer business.

[0018] Thus, there is a growing need to develop improved memory hierarchies that limit the overhead of a memory hierarchy without also reducing bandwidth efficiency and utilization.

SUMMARY OF THE INVENTION

[0019] Accordingly, an embodiment of the invention includes a reconfigurable processor that includes a computational unit and a data access unit coupled to the computational unit, where the data access unit retrieves data from an on-processor memory and supplies the data to the computational unit, and where the computational unit and the data access unit are configured by a program.

[0020] The present invention also involves a reconfigurable processor that includes a first memory of a first type and a data prefetch unit coupled to the memory, where the data prefetch unit retrieves data from a second memory of a second type different from the first type, and the first and second memory types and the data prefetch unit are configured by a program.

[0021] Another embodiment of the invention includes a reconfigurable hardware system that includes a common memory, also referred to as external memory, and one or more reconfigurable processors coupled to the common memory, where at least one of the reconfigurable processors includes a data prefetch unit to read and write data between the unit and the common memory,

and where the data prefetch unit is configured by a program executed on the system.

[0022] Another embodiment of the invention includes a method of transferring data that includes transferring data between a memory and a data prefetch unit in a reconfigurable processor, transferring data between the prefetch unit and a data access unit, and transferring the data between a computational unit and the data access unit, where the computational unit, data access unit and the data prefetch unit are configured by a program.

[0023] Additional embodiments of the invention are set forth in part in the description that follows, and in part will become apparent to those skilled in the art upon examination of the following specification, or may be learned by the practice of the invention. The advantages of the invention may be realized and attained by means of the instrumentalities, combinations, compositions, and methods particularly pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] Figure 1 shows a reconfigurable processor in which the present invention may be implemented;

[0025] Figure 2 shows computational logic as might be loaded into a reconfigurable processor;

[0026] Figure 3 shows a reconfigurable processor as in Figure 1, but with the addition of data access units;

[0027] Figure 4 shows a reconfigurable processor as in Figure 3, but with the addition of data prefetch units;

[0028] Figure 5 shows reconfigurable processor with the inclusion of external memory;

[0029] Figure 6 shows reconfigurable processors with external memory and with an intelligent memory controller;

[0030] Figure 7 shows a reconfigurable processor having a combination of data prefetch units and data access units feeding computational logic;

[0031] Figure 8 shows the bandwidth efficiency and utilization gains obtained when utilizing a data prefetch unit and an intelligent memory controller to perform strided memory references;

[0032] Figure 9A and Figure 9B show the bandwidth efficiency and utilization gains obtained when utilizing a data prefetch unit and an intelligent memory controller to perform subset memory references in X-Y plane;

[0033] Figure 10A and Figure 10B show the bandwidth efficiency and utilization gains obtained when utilizing a data prefetch unit and an intelligent memory controller to perform subset memory references in X-Z plane;

[0034] Figure 11A and Figure 11B show the bandwidth efficiency and utilization gains obtained when utilizing a data prefetch unit and an intelligent memory controller to perform subset memory references in Y-Z plane;

[0035] Figure 12A and Figure 12B show the bandwidth efficiency and utilization gains obtained when utilizing a data prefetch unit and an intelligent memory controller to perform subset memory references in a mini-cube;

[0036] Figure 13 shows the bandwidth efficiency and utilization gains obtained when utilizing a data prefetch unit and an intelligent memory controller to perform indirect memory references;

[0037] Figure 14 shows the bandwidth efficiency and utilization gains obtained when utilizing a data prefetch unit and an intelligent memory controller to perform strided memory reference together with computation.

DETAILED DESCRIPTION

1. Definitions:

[0038] Direct execution logic (DEL) - is an assemblage of dynamically reconfigurable functional elements that enables a program to establish an optimized interconnection among selected functional units in order to implement a desired computational, data prefetch and/or data access functionality for maximizing the parallelism inherent in the particular code.

[0039] Reconfigurable Processor – is a computing device that contains reconfigurable components such as FPGAs and can, through reconfiguration, instantiate an algorithm as hardware.

[0040] Reconfigurable Logic – is composed of an interconnection of functional units, control, and storage that implements an algorithm and can be loaded into a Reconfigurable Processor.

[0041] Functional Unit – is a set of logic that performs a specific operation. The operation may for example be arithmetic, logical, control, or data movement. Functional units are used as building blocks of reconfigurable logic.

[0042] Macro – is another name for a functional unit.

[0043] Memory Hierarchy – is a collection of memories

[0044] Data prefetch Unit – is a functional unit that moves data between members of a memory hierarchy. The movement may be as simple as a copy, or as complex as an indirect indexed strided copy into a unit stride memory.

[0045] Data access Unit – is a functional unit that accesses a component of a memory hierarchy, and delivers data directly to computational logic.

[0046] Intelligent Memory Control Unit – is a control unit that has the ability to select data from its storage according to a variety of algorithms that can be selected by a data requestor, such as a data prefetch unit.

[0047] Bandwidth Efficiency – is defined as the percentage of contributory data transferred between two points. Contributory data is data that actually participates in the recipients processing.

[0048] Bandwidth Utilization – is defined as the percentage of maximum bandwidth between two points that is actually used to pass contributory data.

2. Description

[0049] A reconfigurable processor (RP) 100 implements direct executable logic (DEL) to perform computation, as well a memory hierarchy for maintaining input data and computational results. DEL is an assemblage of dynamically reconfigurable functional elements that enables a program to establish an optimized interconnection among selected functional units in order to implement a desired computational, data prefetch and/or data access functionality for maximizing the parallelism inherent in the particular code. The term DEL may also be used to refer to the set of constructs such as code, data, configuration variables, and the like that can be loaded into RP 100 to cause RP 100 to implement a particular assemblage of functional elements.

[0050] Figure 1 presents an RP 100, which may be implemented using field programmable gate arrays (FPGAs) or other reconfigurable logic devices, that can be configured and reconfigured to contain functional units and interconnecting circuits, and a memory hierarchy comprising on-board memory banks 104, on-chip block RAM 106, registers wires, and a connection 108 to external memory. On-chip reconfigurable components 102 create memory structures such as registers, FIFOs, wires and arrays using block RAM. Dual-ported memory 106 is shared between on-chip reconfigurable components 102. The reconfigurable processor 100 also implements user-defined computational

logic (e.g., such as DEL 200 shown in Figure 2) constructed by programming an FPGA to implement a particular interconnection of computational functional units. In a particular implementation, a number of RPs 100 are implemented within a memory subsystem of a conventional computer, such as on devices that are physically installed in dual inline memory module (DIMM) sockets of a computer. In this manner the RPs 100 can be accessed by memory operations and so coexist well with a more conventional hardware platform. It should be noted that, although the exemplary implementation of the present invention illustrated includes six banks of dual ported memory 104 and two reconfigurable components 102, any number of memory banks and/or reconfigurable components may be used depending upon the particular implementation or application.

[0051] Any computer program, including complex graphics processing programs, word processing programs, database programs and the like, is a collection of algorithms that interact to implement desired functionality. In the common case in which static computing hardware resources are used (e.g., a conventional microprocessor), the computer program is compiled into a set of executable code (i.e., object code) units that are linked together to implement the computer program on the particular hardware resources. The executable code is generated specifically for a particular hardware platform. In this manner, the computer program is adapted to conform to the limitations of the static hardware platform. However, the compilation process makes many compromises based on the limitations of the static hardware platform.

[0052] Alternatively, an algorithm can be defined in a high level language then compiled into DEL. DEL can be produced via a compiler from high level programming languages such as C or FORTRAN or may be designed using a hardware definition language such as Verilog, VHDL or a schematic capture tool. Computation is performed by reconfiguring a reconfigurable processor with the DEL and flowing data through the computation. In this manner, the

hardware resources are essentially adapted to conform to the program rather than the program being adapted to conform to the hardware resources.

[0053] For purposes of this description a single reconfigurable processor will be presented first. A sample of computational logic 201 is shown in Figure 2. This simple assemblage of functional units performs computation of two results ("A+B" and "A+B-(B*C)) from three input variables or operands "A", "B" and "C". In practice, computational units 201 can be implemented to perform very simple or arbitrarily complex computations. The input variables (operands) and output or result variables may be of any size necessary for a particular application. Theoretically, any number of operands and result variables may be used/generated by a particular DEL. Great complexity of computation can be supported by adding additional reconfigurable chips and processors.

[0054] For greatest performance the DEL 200 is constructed as parallel pipelined logic blocks composed of computational functional units capable of taking data and producing results with each clock pulse. The highest possible performance that can be achieved is computation of a set of results with each clock pulse. To achieve this, data should be available at the same rate the computation can consume the data. The rate at which data can be supplied to DEL 200 is determined, at least in significant part, by the memory bandwidth utilization and efficiency. Maximal computational performance can be achieved with parallel and pipelined DEL together with maximizing the memory bandwidth utilization and efficiency. Unlike conventional static hardware platforms, however, the memory hierarchy provided in a RP 100 is reconfigurable. In accordance with the present invention, through the use of data access units and associated memory hierarchy components, computational demands and memory bandwidth can be matched.

[0055] High memory bandwidth efficiency is achieved when only data required for computation is moved within the memory hierarchy. Figure 3 shows a simple logic block 300 comprising computational functional units 301, control

(not shown), and data access functional units 303. The data access unit 303 presents data directly to the computational logic 301. In this manner, data is moved from a memory device 305 to the computational logic and from the computational logic back into a memory device 305 or block RAM memory 307 within an RP 100.

[0056] Figure 4 illustrates the logic block 300 with an addition of a data prefetch unit 401. The data prefetch unit 401 moves data from one member of the memory hierarchy 305 to another 308. Data prefetch unit 401 operates independently of other functional units 301, 302 and 303 and can therefore operate prior to, in parallel with, or after computational logic. This independence of operation permits hiding the latency associated with obtaining data for use in computation. The data prefetch unit deposits data into the memory hierarchy within RP 100, where computational logic 301, 302 and 303 can access it through data access units. In the example of Figure 4, prefetch unit 401 is configured to deposit data into block RAM memory 308. Hence, the prefetch units 401 may be operated independently of logic block 300 that uses prefetched data.

[0057] An important feature of the present invention is that many types of data prefetch units can be defined so that the prefetch hardware can be configured to conform to the needs of the algorithms currently implemented by the computational logic. The specific characteristics of the prefetch can be matched with the needs of the computational logic and the format and location of data in the memory hierarchy. For example, Figure 9A and Figure 9B show an external memory that is organized in a 128 byte (16 word) block structure. This organization is optimized for stride 1 access of cache based computers. A stride 128 access can result in a very inefficient use of bandwidth from the memory, since an extra 120 bytes of data is moved for every 8 bytes of requested data yielding a 6.25% bandwidth efficiency.

[0058] Figure 5 shows an example of data prefetch in which there are no bandwidth gains since all data fetched from external memory blocks is also transferred and used in computational units 301 through memory bank access units 303. However, bandwidth utilization is increased due to the ability of the data prefetch units 501 to initiate a data transfer in advance of the requirement for data by computational logic.

[0059] In accordance with an embodiment of the present invention, data prefetch units 601 are configured to communicate with an intelligent memory controller 603 in Figure 6 and can extract only the desired 8 bytes of data, discard the remainder of the memory block, and transmit to the data prefetch unit only the requested portion of the stride 128 data. The prefetch units 601 then delivers that data to the appropriate memory components within the memory hierarchy of the logic block 300.

[0060] Figure 6 shows the prefetch units 601 delivering data to the RP's onboard memory banks 305. An onboard memory bank data access unit 303 then delivers the data to computational logic 301 when required. The data prefetch units 501 couple with an intelligent memory controller 601 in the implementation of Figure 6 that supports a strided reference pattern, which yields a 100% bandwidth efficiency in contrast to the 6.25% efficiency. Although illustrated as a single block of external memory, multiple numbers of external memories may be employed as well.

[0061] In Figure 7, the combination of data prefetch units 701 and data access units 703 feeding computational logic 301 such that bandwidth efficiency and utilization are maximized is shown in Figure 7. In this example strided data prefetch units 701 fetch only the required data words from external memory. Figure 8 demonstrates the efficiency gains enabled by this combination. Prefetch units 701 deliver the data into stream memory components 705 that is accessed by stream data access units 703. The stream data access units 703 fetch data from the stream based on valid data bits that are provided to the

stream by the data prefetch units 701 as data is presented to the stream. Use of the stream data access unit allows computational logic to be activated upon initiation of the data prefetch operation. This, in turn, allows computation to start with the arrival of the first data item, signaled by valid data bits. Computational logic 301 does not have to await arrival of a complete buffer of data in order to proceed. This elimination of latency increases the bandwidth utilization, by allowing data transfer to continue uninterrupted and in parallel with computation.

[0062] Figure 8 illustrates the efficiency gains enabled by the configuration of Figure 7. Figure 8 shows a plurality of memory blocks 800 in which only one memory element 801 exists in each memory block 800. The configuration of Figure 7 allows the desired portions 801 of each memory block 800 to be compacted into a transfer buffer 805. The desired data elements 801 are compacted in order. Since only the contents of the transfer buffer 805 need be transferred to the computational logic, a significant increase in transfer efficiency can be realized.

[0063] Figures 9A/9B, 10A/10B, 11A/11B and 12A/12B show bandwidth efficiency gains that are achieved in various situations when a subset of stored data is required for computation. Applications store data in a specific order in memory. However it is often the case that the actual reference pattern required during computation is different from the ordering of data in memory. Figures 9A/9B, 10A/10B, 11A/11B and 12A/12B show an example of a X,Y,Z coordinate oriented data which is stored such that striding though the X axis is the most efficient for retrieving blocked data.

[0064] Coupling data prefetch units in the RP 100 with an intelligent memory controller 601 in the external memory yields a significant improvement in bandwidth efficiency and utilization. Four examples are presented in the Figures 9A/9B, 10A/10B, 11A/11B and 12A/12B in which the shaded memory locations indicate desired data. The Figures illustrate an intelligent memory

controller's response to each of four different data prefetch unit's requests for data. Again, an important feature of the present invention is the ability to implement various kinds or styles of prefetch units to meet the needs of a particular algorithm being implemented by computational elements 301. For ease of illustration, each example shows the same set of computational logic, however, in most cases the function being implemented by components 301 would change and therefore alter the decision as to which prefetch strategy is most appropriate. In accordance with the present invention, the prefetch units are implemented in a manner that is optimized for the implemented computational logic.

[0065] Figure 9A/9B shows response to a request from an XY-slice data prefetch unit. Figure 10A/10B shows response to a XZ-slice data prefetch unit request. Figure 11A/11B shows response to a YZ-slice data prefetch unit request. Figure 12A/12D shows the response to a SubCube data prefetch unit request. In each of these examples the data prefetch units are configured to pass information to the intelligent memory controller 601 to identify the type of request that is being made, as well as a data address and parameters, in this case, defining the slice size or sub-cube size.

[0066] One of the largest bandwidth efficiency and utilization gains can be seen in the case of a Gather data prefetch unit working in cooperation with an intelligent memory controller 601. Figure 13 illustrates the activity in the external memory controller 601. In this example an index array 1301 and a data array 1303 reside in memory. A gather data prefetch unit in an RP 100 requests a gather by specifying the access type as "gather", and providing a pointer to index array 1301, and another pointer to the data array 1303. The memory controller uses the index array 1301 to select desired data elements, indicated by shading, and then delivers an in order stream of data to the prefetch unit. Gains are made by delivering only requested data from transfer buffer 1305 (not the remainder of a data block as in cache line oriented systems) by eliminating the need to transfer an index array either to the

processor or to the memory controller, and by eliminating the start/stop time required when the data is not streamed to the requestor.

[0067] A further bandwidth efficiency and utilization gain is made when coupling a data prefetch unit with memory controller capable of computation. Figure 14 illustrates activity in a cooperating memory controller having a computational component 1407 in response to a data prefetch unit. Here the prefetch units requests a "strided compute", providing parameters for an operator, and addresses, and strides for data to be operated upon. In Figure 14, the data to be operated on comprises "X" data 1401 and "Y" data 1403. The data 1401 and 1403 are processed by computational component 1407 to generate a resultant value that is a specified function of X and Y as indicated by F(X,Y) in Figure 14. The resultant values are then passed to the requesting prefetch unit via transfer buffer 1405. In this case only computed results are passed and no operand data need to transferred. Accordingly, where the desired data, indicated by shading in Figure 14, resides across multiple blocks, efficiency is achieved not only by avoiding transfer of the undesired data surrounding the desired data, but also because only the result is transferred, not the original data 1401/1403.

EXAMPLES

[0068] Some programming examples utilizing the memory hierarchy of the present invention will now be illustrated. The first example illustrates how a computational intensive matrix multiplication problem may be handled by the explicitly parallel and addressable storage of the present invention.

1. Example 1: Explicit Parallel and Addressable Storage

[0069] Consider the matrix multiplication C = A x B, where:

A is a matrix of size M rows by 64 columns;

B is a matrix of size 64 rows by N columns; and

C is a matrix of size M rows by N columns.

The size and shape of this problem typically arises in the context of LU decomposition in linear algebra libraries (e.g., LAPACK). The operation count for this problem would be 2*M*N*64, and the total data necessary to transport would be (M*64 + N*64 + M*N), making the problem quite computationally intensive.

[0070] The dot-product formulation of the matrix multiplication may be represented as the following a triple-nested loop:

```
for (i = 0; I<m; I++) {
   for (j = 0; j< n; j++) {
      sum = 0;
for (k = 0; k < 64; k++) {
   sum += A[k*m*I] * B[j*64+k];
  }
  C1[i+j+mm] = sum;
 }
}
```

[0071] On a conventional microprocessor with static execution resources, these loops would be arranged to give stride-one data access where possible and also block or tile these uses to facilitate data cache hits on the B and A matrices, which are read many times. With the configurable memory hierarchy of the present invention, matrix B may be stored in on-board BRAM memory 307 and rows of matrix A in registers.

[0072] The rows of matrix B may be stored in independently, locally declared BRAM arrays (B0, B1, . . . B63). The rows are stored as independent memory structures, and may be accessed in parallel. Rows of matrix A may be stored in 64 registers described with scalar variables. With these explicit data structures, the following pseudo code can describe the matrix multiplication:

```
Load B into BRAM;

for (i = 0; i< m; i++) {

Load ith Row of A into registers A00 to A63;

For (j = 0; j< n; j++) {

   C[i+j+m] +=

A00 * b0[j] +

A01 * b1[j] +

A02 * b2[j] +  //inner loop produces

A03 * b3[j] +  //128 results per

A04 * b4[j] +  //clock cycle.  64 rows

A05 * b5[j] +  //of B are read in

A06 * b6[j] +  //parallel

. . .

A63 * b63[j];
```

[0073] The code is designed to minimize the amount of data motion. The A and B matrices are read once and the C matrix is written just once at it is produced. When computational resources permit, the i loop could also be

unrolled to process multiple rows of matrix A against matrix B in the inner loop. Processing two rows of A, for example, would produce 256 computational results per clock cycle.

2. Example 2: Irregular Memory Access

[0074] Benchmarks have been developed for measuring the ability of a computer system to perform indirect updates. An indirect update, written in the C programming language, looks like:

```
for (I = 0; I < N; I++) {

A[Index[I]]) = A[Index[I]] + B[I];

}
```

Typically, A is a large array, and Index has an unpredictable distribution. The benchmark generally forces memory references to miss in cache, and for entire cache lines to be brought in for single-word updates. The problem gets worse as memories get further away from processors and cache lines become wider.

[0075] In this example, the arrays have 64-bit data. To complete one iteration of this loop, 24 bytes of information is required from memory and 8 bytes are written back for a total of 32 bytes of memory motion per iteration. On an implicit architecture with cache-lines of width W bytes, each iteration results in the following memory bus traffic:

1. Index[I]: 8 bytes per iteration due to stride-1 nature;
2. B[I]: 8 bytes per iteration due to stride-1 nature; and
3. A[Index[I]]: W bytes read and written per iteration.

The total amount of bus traffic is 2*W + 16 bytes per iteration. On an average microprocessor today, W = 128 so an iteration of this loop results in 272 bytes

of memory traffic when only 32 bytes is algorithmically required, making only 12% of the data moved as being useful for the problem.

[0076] In addition, because microprocessors rely on wide cache lines and hardware pre-fetching strategies to amortize the long latency to main memory, only a small number of outstanding cache-line misses are typically tolerated. Because of the irregular nature of this example, hardware pre-fetching provides little benefit, making it difficult to keep the memory bus saturated, even with the large amount of wasted memory traffic. Bus utilization on the microprocessor processing only consumes about 700 MB/sec of the 3.2 GB/sec available, or 22%. Combining the poor bus utilization with the relatively small amount of data that is useful results in the microprocessor executing at about 2.5% of peak.

[0077] The memory hierarchy of the present invention does not require that memory traffic be organized in a cache-line structure, permitting loop iteration to be accomplished with the minimum number of bytes (in this case 32 bytes of memory traffic). In addition, data pre-fetch functional units may be fully pipelined, allowing full use of available memory bus bandwidth. Data storing may be handled in a similar pipelined fashion. An example of the pseudo code that performs the random update in the memory hierarchy looks like:

```
for (i=0; I < N-Gather_size; I=I+Gather_size) {
   gather ( A, Index, I, A_local, Gather_size)
   for (j=); j < Gather_size; j++) {
     A_local[j] = A_local[j] + B[j];
  }
  scatter (A_local, Index, &A[I], Gather_size);
}
```

[0078] This loop will pipeline safely as described by the pseudo code provided that the index vector has no repeated values within each Gather_size segment. If repeats are present, then logic within the gather unit can preprocess the Index vector and B vector into safe sub-lists that can be safely pipelined with little or no overhead.

Conclusion

[0079] It should be apparent that the scaleable, programmable memory mechanisms enabled by the present invention are available to the exploit available algorithm locality and thereby achieve up to 100% bandwidth efficiency. In addition, the scaleable computational resources can be leveraged to attain 100% bandwidth utilization. As a result, the present invention provides a programmable computational system that delivers the maximum possible performance for any memory bus speed. This combination of efficiency and utilization yields orders of magnitude performance benefit compared with implicit models when using an equivalent memory bus.

[0080] Although the invention has been described and illustrated with a certain degree of particularity, it is understood that the present disclosure has been made only by way of example, and that numerous changes in the combination and arrangement of parts can be resorted to by those skilled in the art without departing from the spirit and scope of the invention, as hereinafter claimed.

WE CLAIM:

1. A reconfigurable processor comprising:

a first memory having a first characteristic memory type; and

a data prefetch unit coupled to the memory, wherein the data prefetch unit retrieves data from a second memory of second characteristic memory type and wherein the memory types and data prefetch unit are configured by a program.

2. The reconfigurable processor of claim 1, wherein the processor does not have a cache to store data from the memory.

3. The reconfigurable processor of claim 1, wherein the data retrieved from the memory is not a cache line-sized unit of contiguous data.

4. The reconfigurable processor of claim 1, wherein the data prefetch unit is coupled to a memory controller that controls the transfer of the data between the memory and the data prefetch unit.

5. The reconfigurable processor of claim 1, wherein the data prefetch unit receives processed data from on-processor memory and writes the processed data to an external off-processor memory memory.

6. The reconfigurable processor of claim 1, wherein the data prefetch unit comprises at least one register from the reconfigurable processor.

7. The reconfigurable processor of claim 1, wherein the data prefetch unit is disassembled when another program is executed on the reconfigurable processor.

8. The reconfigurable processor of claim 1 wherein said prefetch unit is operative to retrieve data from a processor memory.

9. The reconfigurable processor of claim 8 wherein said processor memory is a microprocessor memory.

10. The reconfigurable processor of claim 8 wherein said processor memory is a reconfigurable processor memory.

11. A reconfigurable hardware system, comprising:

a common memory; and

one or more reconfigurable processors coupled to the common memory, wherein at least one of the reconfigurable processors includes a data prefetch unit to read and write data between the unit and the common memory, and wherein the data prefetch unit is configured by a program executed on the system.

12. The reconfigurable hardware system of claim 11, comprising a memory controller coupled to the common memory and the data prefetch unit.

13. The reconfigurable hardware system of claim 11, wherein the reconfigurable processor is not coupled to a cache.

14. The reconfigurable hardware system of claim 11, wherein the data written and read between the data prefetch unit and the common memory is not a cache line-sized unit of contiguous data.

15. The reconfigurable hardware system of claim 11, wherein the at least of the reconfigurable processors also includes a computational unit coupled to the data access unit.

16. The reconfigurable hardware system of claim 15, wherein the computational unit is supplied the data by the data access unit.

17. A method of transferring data comprising:

transferring data between a memory and a data prefetch unit in a reconfigurable processor; and

transferring the data between a computational unit and the data access unit, wherein the computational unit and the data access unit, and the data prefetch unit are configured by a program.

18. The method of claim 17, wherein the data is written to the memory, said method comprising:

transferring the data from the computational unit to the data access unit; and

writing the data to the memory from the data prefetch unit.

19. The method of claim 17, wherein the data is read from the memory, said method comprising:

transferring the data from the memory to the data prefetch unit; and

reading the data directly from the data prefetch unit to the computational unit through a data access unit.

20. The method of claim 19, wherein all the data transferred from the memory to the data prefetch unit is processed by the computational unit.

21. The method of claim 19, wherein the data is selected by the data prefetch unit based on an explicit request from the computational unit.

22. The method of claim 17, wherein the data transferred between the memory and the data prefetch unit is not a complete cache line.

23. The method of claim 17, wherein a memory controller coupled to the memory and the data prefetch unit, controls the transfer of the data between the memory and the data prefetch unit.

24. A reconfigurable processor comprising:

a computational unit; and

a data access unit coupled to the computational unit, wherein the data access unit retrieves data from memory and supplies the data to the computational unit, and wherein the computational unit and the data access unit are configured by a program.

ABSTRACT OF THE DISCLOSURE

[0081] A reconfigurable processor that includes a computational unit and a data prefetch unit coupled to the computational unit, where the data prefetch unit retrieves data from a memory and supplies the data to the computational unit through memory and a data access unit, and where the data prefetch unit, memory, and data access unit is configured by a program. Also, a reconfigurable hardware system that includes a common memory; and one or more reconfigurable processors coupled to the common memory, where at least one of the reconfigurable processors includes a data prefetch unit to read and write data between the unit and the common memory, and where the data prefetch unit is configured by a program executed on the system. In addition, a method of transferring data that includes transferring data between a memory and a data prefetch unit in a reconfigurable processor; and transferring the data between a computational unit and the data prefetch unit.

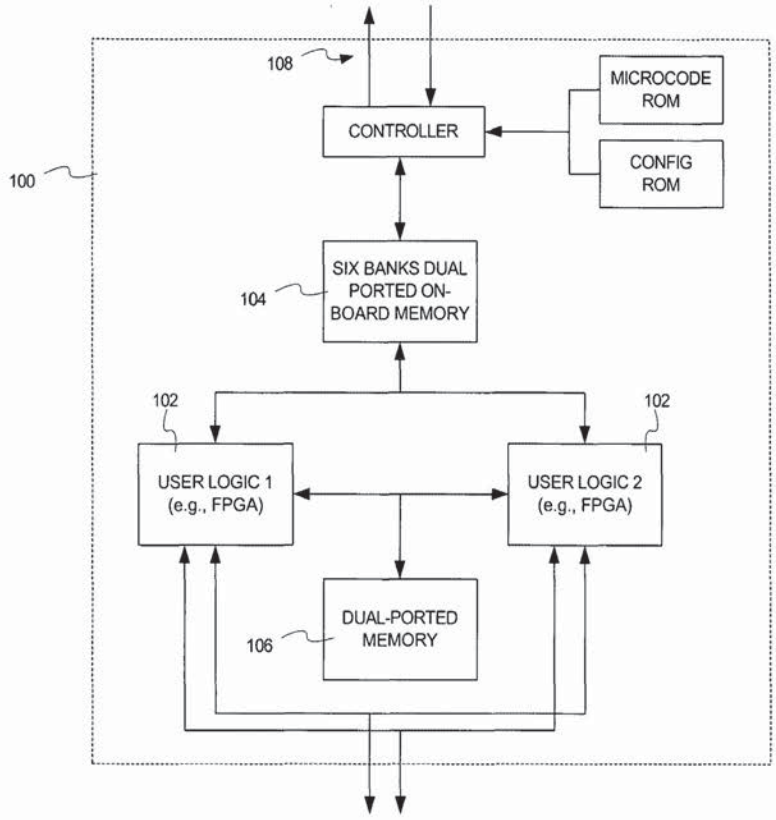
108
MICROCODE ROM
CONTROLLER
CONFIG ROM
100
SIX BANKS DUAL PORTED ON-BOARD MEMORY
104
102
102
USER LOGIC 1 (e.g., FPGA)
USER LOGIC 2 (e.g., FPGA)
DUAL-PORTED MEMORY
106

FIG. 1

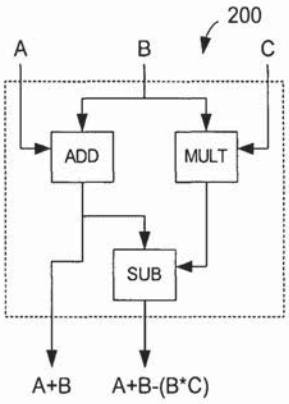
200
A
B
C
ADD
MULT
SUB
A+B
A+B-(B*C)

FIG. 2

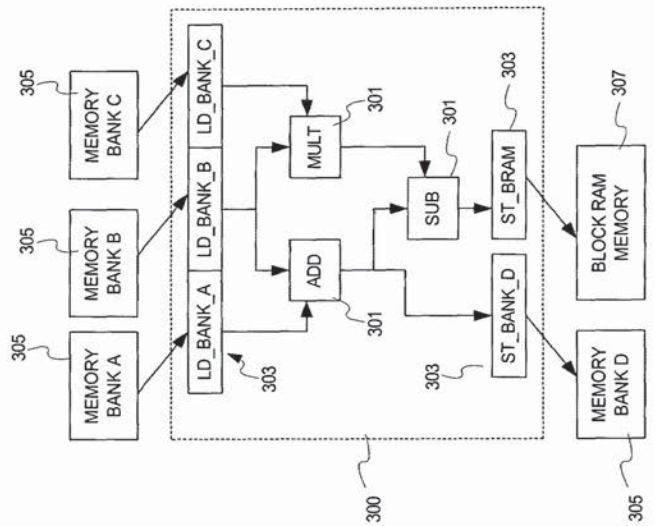
MEMORY BANK A
MEMORY BANK B
MEMORY BANK C
MEMORY BANK D
305
LD_BANK_A
LD_BANK_B
LD_BANK_C
303
ADD
MULT
SUB
301
ST_BANK_D
ST_BRAM
303
BLOCK RAM MEMORY
307
300

FIG. 3

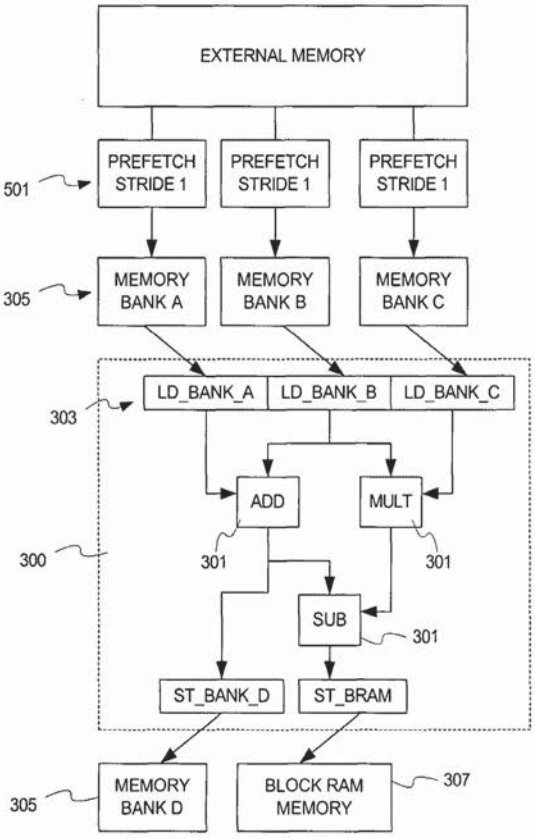
EXTERNAL MEMORY
PREFETCH STRIDE 1
PREFETCH STRIDE 1
PREFETCH STRIDE 1
501
MEMORY BANK A
MEMORY BANK B
MEMORY BANK C
305
LD_BANK_A
LD_BANK_B
LD_BANK_C
303
ADD
MULT
300
301
301
SUB
301
ST_BANK_D
ST_BRAM
MEMORY BANK D
BLOCK RAM MEMORY
307
305

FIG. 5

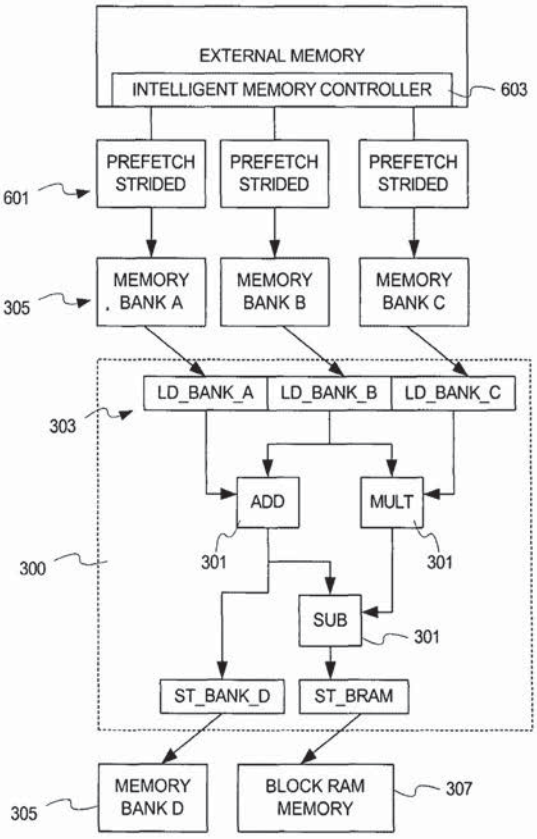
EXTERNAL MEMORY
INTELLIGENT MEMORY CONTROLLER
603
PREFETCH STRIDED
PREFETCH STRIDED
PREFETCH STRIDED
601
MEMORY BANK A
MEMORY BANK B
MEMORY BANK C
305
LD_BANK_A
LD_BANK_B
LD_BANK_C
303
ADD
MULT
300
301
301
SUB
301
ST_BANK_D
ST_BRAM
MEMORY BANK D
BLOCK RAM MEMORY
307
305

FIG. 6

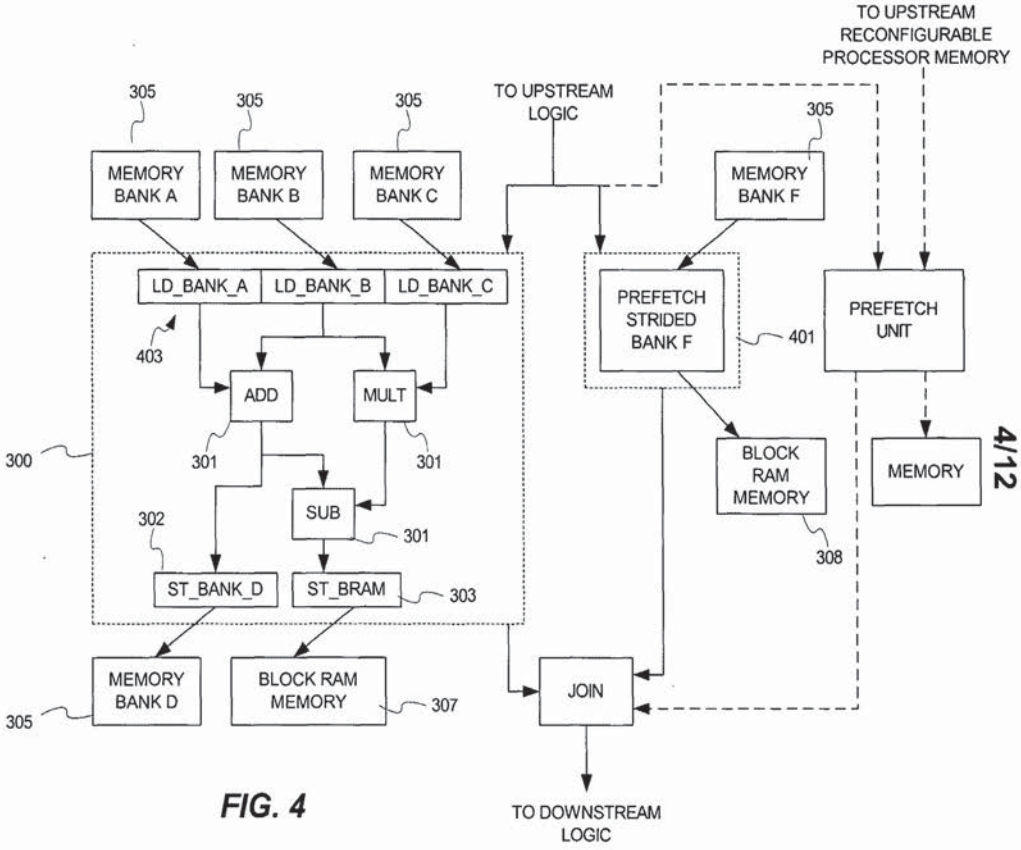
TO UPSTREAM RECONFIGURABLE PROCESSOR MEMORY
TO UPSTREAM LOGIC
305
MEMORY BANK A
MEMORY BANK B
MEMORY BANK C
MEMORY BANK F
LD_BANK_A
LD_BANK_B
LD_BANK_C
403
ADD
MULT
SUB
ST_BANK_D
ST_BRAM
303
300
301
302
PREFETCH STRIDED BANK F
401
PREFETCH UNIT
BLOCK RAM MEMORY
308
MEMORY
MEMORY BANK D
BLOCK RAM MEMORY
307
JOIN
TO DOWNSTREAM LOGIC

FIG. 4

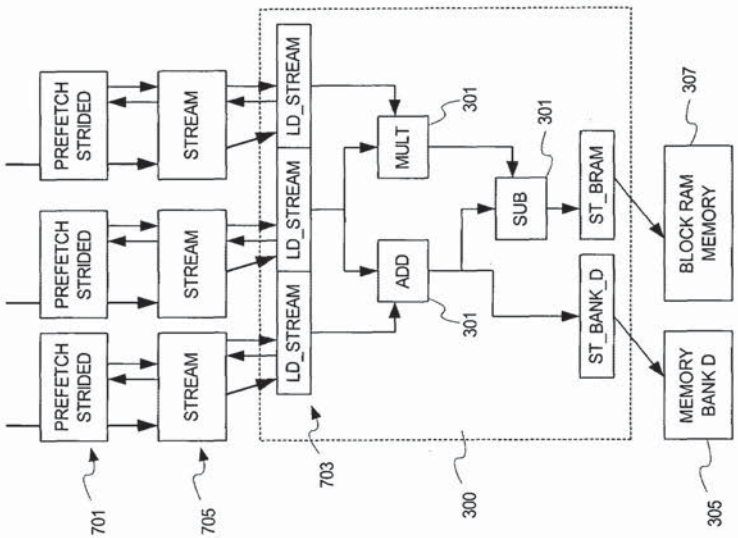
PREFETCH STRIDED
PREFETCH STRIDED
PREFETCH STRIDED
STREAM
STREAM
STREAM
LD_STREAM
LD_STREAM
LD_STREAM
MULT
ADD
SUB
ST_BRAM
ST_BANK_D
BLOCK RAM MEMORY
MEMORY BANK D
301
301
301
307
701
705
703
300
305

FIG. 7

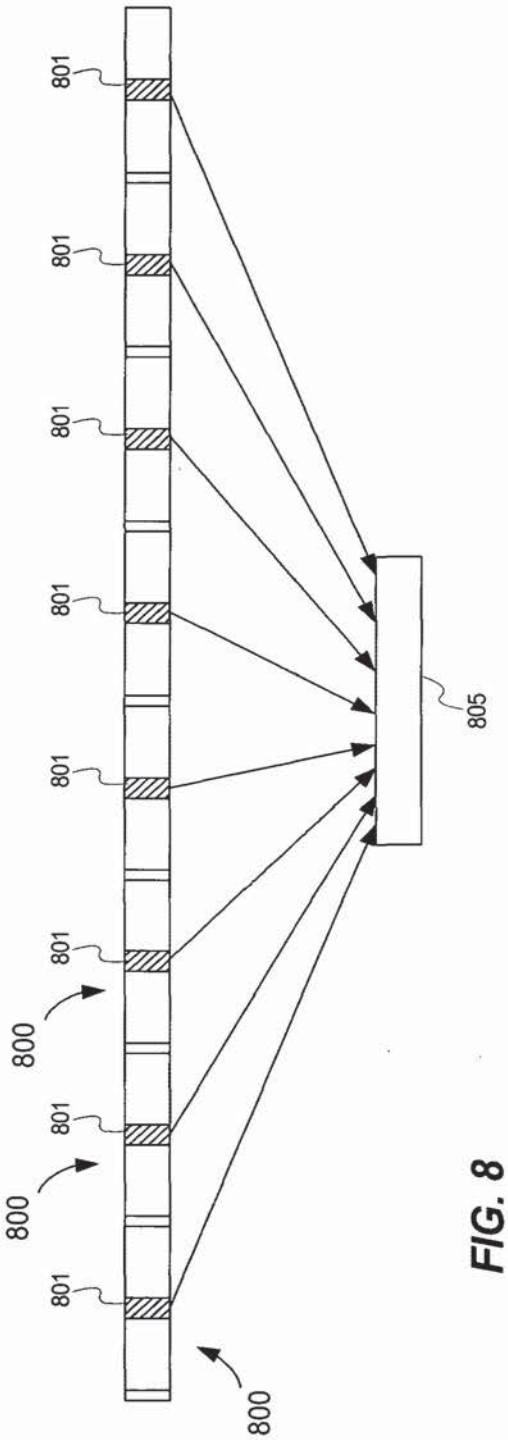

FIG. 8

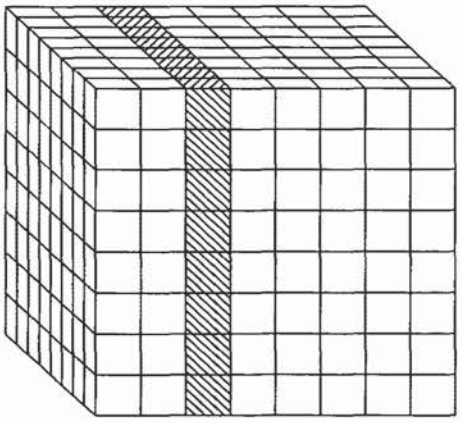

FIG. 9A

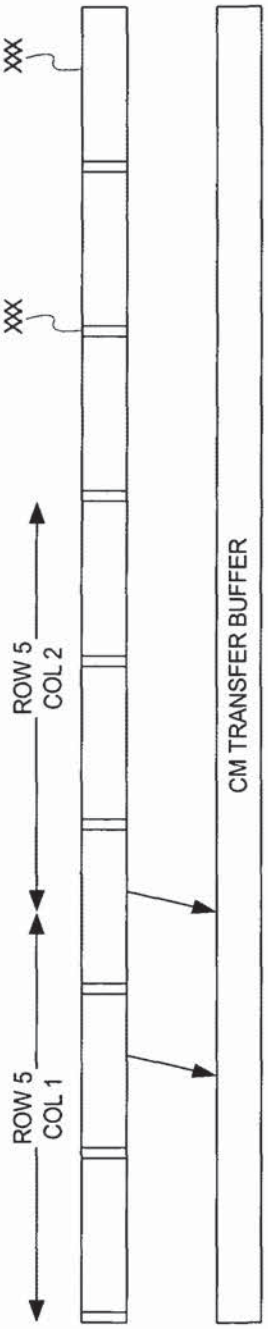

FIG. 9B

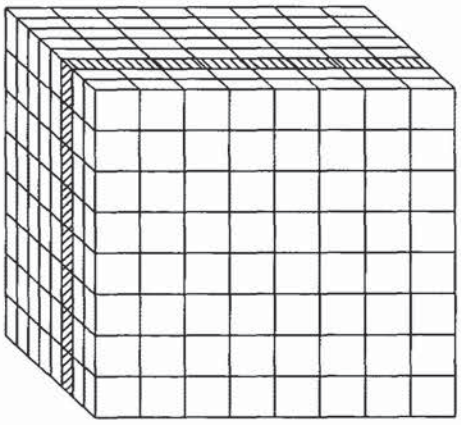

FIG. 10A

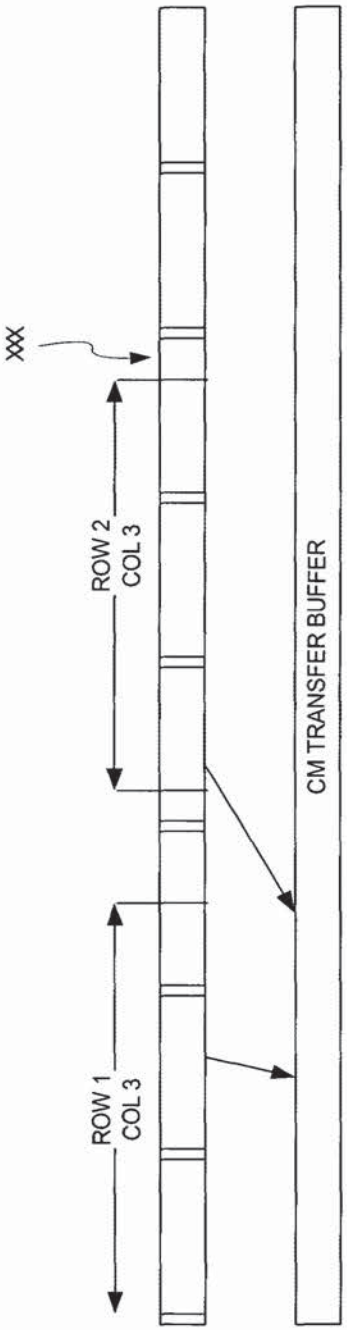

FIG. 10B

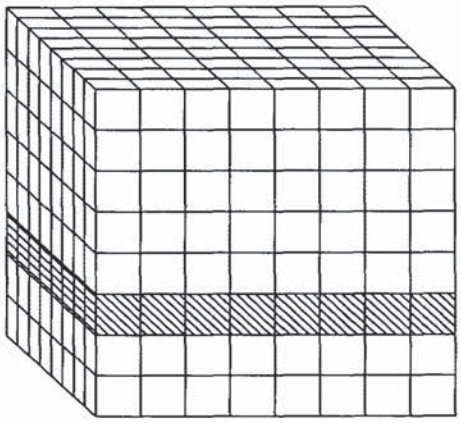

FIG. 11A

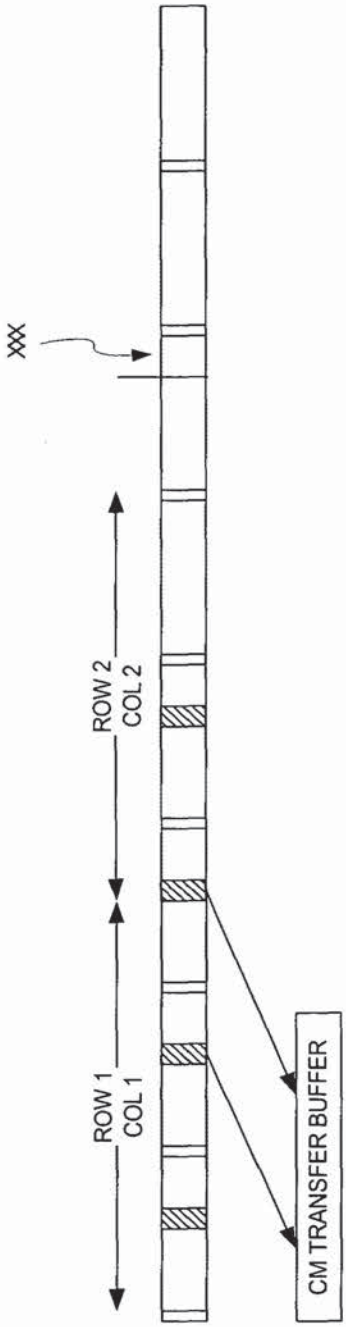

FIG. 11B

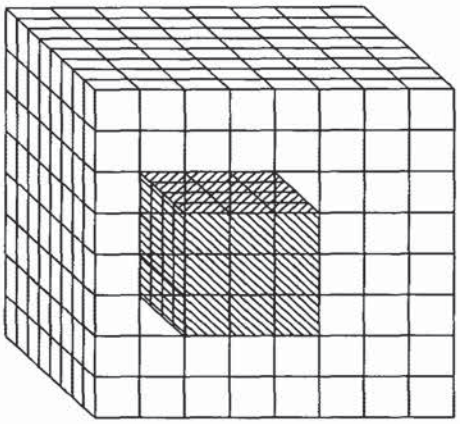

FIG. 12A

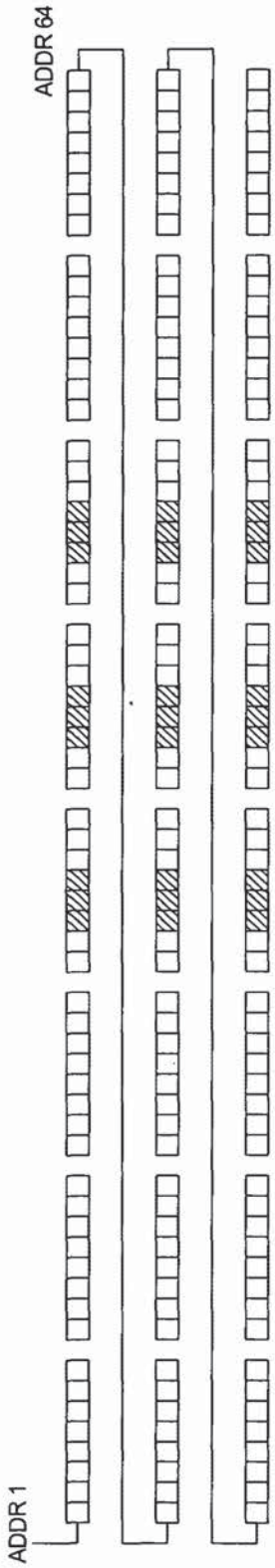

FIG. 12B

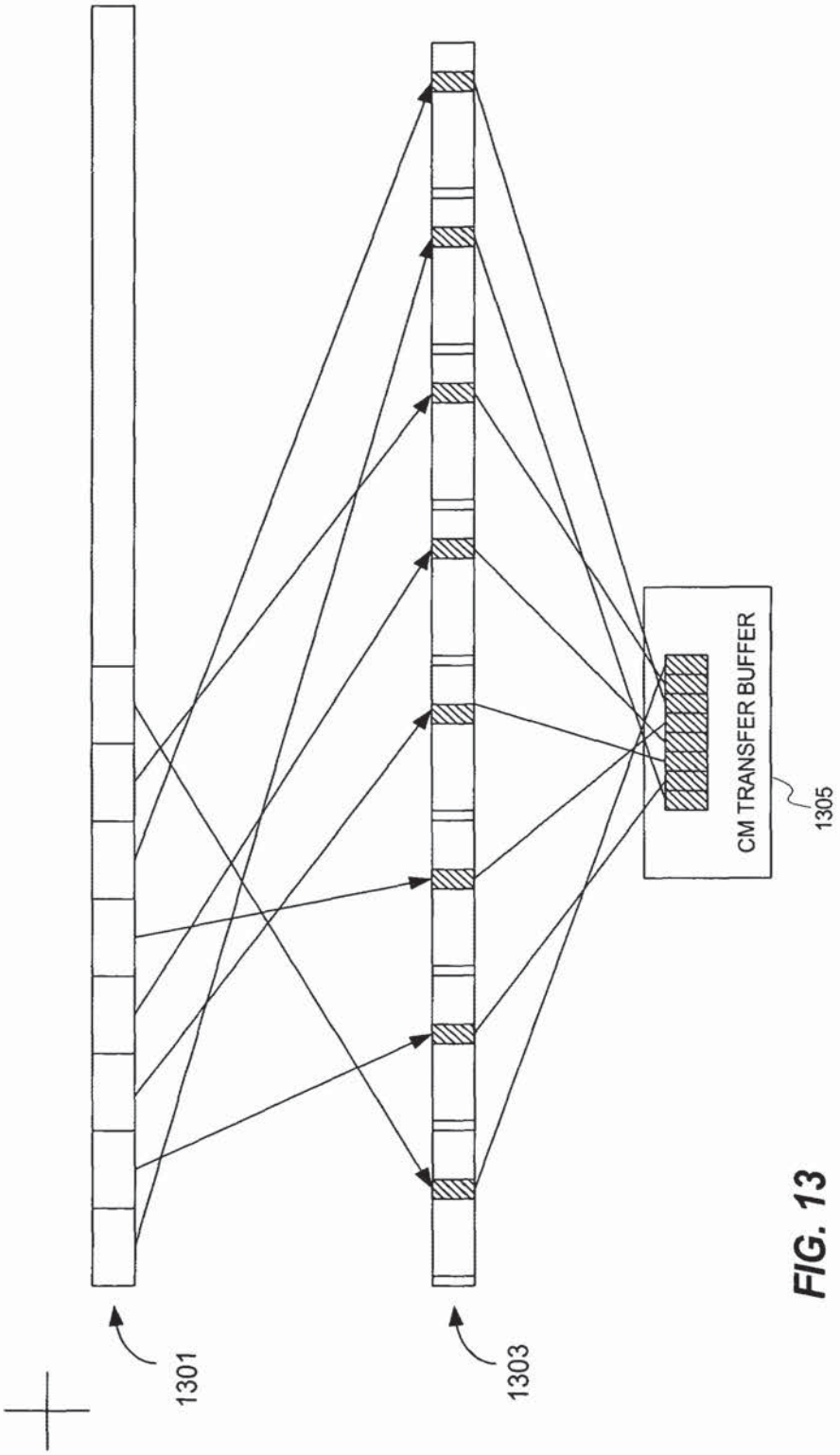

FIG. 13

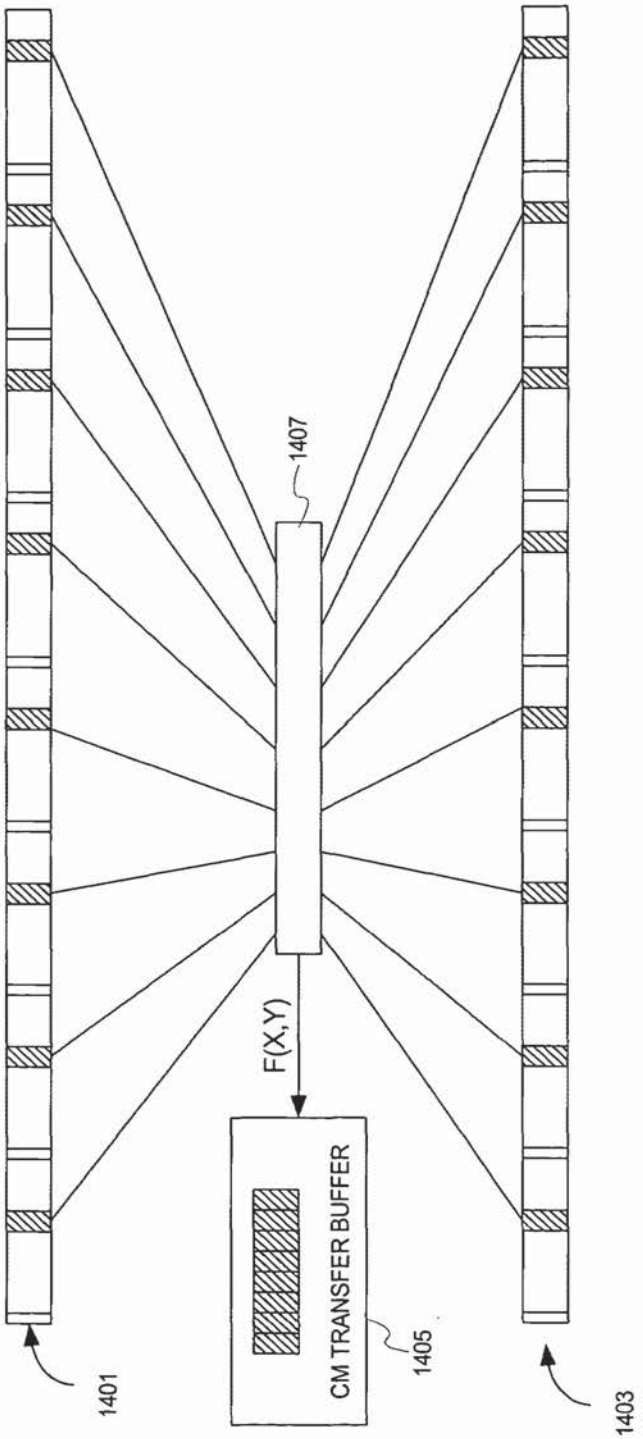

FIG. 14

PTO/SB/01 (08-03)

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)		
	Attorney Docket No.	SRC028
	First Named Inventor	Daniel Poznanovic et al.
	COMPLETE IF KNOWN	
	Application Number	--------
☒ Declaration Submitted with Initial Filing OR ☐ Declaration Submitted after Initial Filing--surcharge 37 CFR 1.16(e) required	Filing Date	Herewith
	Art Unit	
	Examiner Name	

I hereby declare that:

Each inventor's residence, mailing address, and citizenship are as stated below next to their name.

I believe the inventor(s) named below to be the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE

the specification of which

☒ is attached hereto

OR

☐ was filed on (MM/DD/YYYY) _____ as U.S. Application No. or PCT International Application No. _____

and was amended on (MM/DD/YYYY) _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C § 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent or inventor's or plant breeder's rights certificate(s), or § 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Appl. No.(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? Yes	No
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application nos. are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Date (MM/DD/YYYY)
60/479,339	**06/18/2003**

DECLARATION – Utility or Design Patent Application

I hereby claim the benefit under 35 U.S.C. 120 of any U.S. application(s) or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application

U.S. Parent Application or PCT Parent No.	Parent Filing Date (MM/DD/YY)	Parent Patent No. (if applicable)

☐ Additional U.S. or PCT international application nos. listed on PTO/SB/02B attached hereto.

As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent Trademark Office connected therewith:

☒ Customer Number **25235**
OR
☐ Registered practitioner(s) name/registration number listed below

Name	Registration Number	Name	Registration Number

☐ Additional registered practitioner(s) named on supplemental sheet PTO/SB/02C attached hereto.

Direct all correspondence to: ☒ Customer Number **25235** OR ☐ Correspondence address below

Name					
Address					
City		**State**		**ZIP**	
Country		**Telephone**		**Fax**	

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor: ☐ A petition has been filed for this unsigned inventor.

Given Name (first and middle [if any])	Family Name or Surname
Daniel	**Poznanovic**

Inventor's Signature						Date 6-16-04	
Residence City	**Colorado Springs**	State	**Colorado**	Country	**USA**	Citizenship	**USA**
Mailing Address	**1136 Middle Creek Parkway**						
City	**Colorado Springs**	State	**Colorado**	ZIP	**80921**	Country	**USA**

☒ Additional inventors or a legal representative are being named on the _1__supplemental additional inventor(s) sheet(s) PTO/SB/02A or 02LR attached hereto.

DECLARATION	ADDITIONAL INVENTOR(S) Supplemental Sheet Page __1__ of __1___

Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor					
Given Name (first and middle [if any])		Family Name or Surname					
David E.		**Caliga**					
Inventor's Signature	D J Caliga					Date	6/16/2004
Residence: City	**Colorado Springs**	State	**CO**	Country	**USA**	Citizenship	**USA**
Mailing Address	**8445 Lauralwood Lane**						
City	**Colorado Springs**	State	**CO**	ZIP	**80919**	Country	**USA**

Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor					
Given Name (first and middle [if any])		Family Name or Surname					
Jeffrey		**Hammes**					
Inventor's Signature	Jeffrey F Hammes					Date	6-16-04
Residence: City	**Colorado Springs**	State	**CO**	Country	**USA**	Citizenship	**USA**
Mailing Address	**870 Vindicator Dr., #311**						
City	**Colorado Springs**	State	**CO**	ZIP	**80919**	Country	**USA**

Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor					
Given Name (first and middle [if any])		Family Name or Surname					
Inventor's Signature						Date	
Residence: City		State		Country		Citizenship	
Mailing Address							
City		State		ZIP		Country	

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

06/21/2004 HVUONG1 00000046 10869200

01 FC:1001	770.00 OP
02 FC:1202	72.00 OP
03 FC:1201	86.00 OP

PTO-1556
(5/87)

*U.S. Government Printing Office: 2002 — 489-267/69033

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2003

Application or Docket Number: 10869 200

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	24	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	24 minus 20=	* 4
INDEPENDENT CLAIMS	4 minus 3 =	* 1
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	385.00	OR	BASIC FEE	770.00
XS 9=		OR	XS18=	72
X43=		OR	X86=	86
+145=		OR	+290=	—
TOTAL		OR	TOTAL	928

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

FORM PTO-875 (Rev. 10/03) Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	103	reconfigur$3 adj (processor micro-processor CPU processor)	US-PGPUB; USPAT	OR	ON	2004/12/11 17:39
S2	125	reconfigur$3 adj (processor micro-processor CPU microprocessor)	US-PGPUB; USPAT	OR	ON	2004/11/26 15:49
S3	6	reconfigur$3 adj (processor micro-processor CPU microprocessor) and "711".clas.	US-PGPUB; USPAT	OR	ON	2004/11/26 15:50
S4	0	reconfigur$3 adj (processor micro-processor CPU microprocessor) and prefetch	US-PGPUB; USPAT	OR	ON	2004/11/26 15:50
S5	11	711/170-173.ccls. and dynamic near3 logic	US-PGPUB; USPAT	OR	ON	2004/12/02 16:34
S6	847	smc.as.	US-PGPUB; USPAT	OR	ON	2004/12/02 16:34
S7	0	smc.as. and "711".clas.	US-PGPUB; USPAT	OR	ON	2004/12/02 16:34
S8	0	smc.as. and "712".clas.	US-PGPUB; USPAT	OR	ON	2004/12/02 16:34
S9	0	(smc and computers) .as. and "712".clas.	US-PGPUB; USPAT	OR	ON	2004/12/02 16:35
S10	0	(smc and computers) .as.	US-PGPUB; USPAT	OR	ON	2004/12/02 16:35
S11	0	(smc and computers).as.	US-PGPUB; USPAT	OR	ON	2004/12/02 16:35
S12	9	(src and computers).as.	US-PGPUB; USPAT	OR	ON	2004/12/02 16:45
S13	72	711/170.ccls. and dynamic$4 near3 configur$5	US-PGPUB; USPAT	OR	ON	2004/12/02 16:39
S14	2	711/170.ccls. and dynamic$4 near3 configur$5 with cache	US-PGPUB; USPAT	OR	ON	2004/12/02 16:39
S15	196	reconfigurable adj processor	US-PGPUB; USPAT	OR	ON	2004/12/02 17:32
S16	4	"206189".ap.	US-PGPUB; USPAT	OR	ON	2004/12/02 17:34
S17	1	"5024031".pn.	US-PGPUB; USPAT	OR	ON	2004/12/03 11:14
S18	5	"869200".ap.	US-PGPUB; USPAT	OR	ON	2004/12/03 15:30
S19	1401	711/170.ccls.	US-PGPUB; USPAT	OR	ON	2004/12/03 15:30
S20	376	711/170.ccls. and (reconfigur$5 rearrang$4 application adj specific)	US-PGPUB; USPAT	OR	ON	2004/12/03 18:33

S21	93	711/170.ccls. and matrix	US-PGPUB; USPAT	OR	ON	2004/12/03 15:54
S22	50	711/170.ccls. and fpga	US-PGPUB; USPAT	OR	ON	2004/12/03 16:40
S23	186	712/15.ccls.	US-PGPUB; USPAT	OR	ON	2004/12/03 16:41
S24	230	711/170.ccls. and (application near2 specific application-specific)	US-PGPUB; USPAT	OR	ON	2004/12/03 18:18
S25	196	reconfigurable adj processor	US-PGPUB; USPAT	OR	ON	2004/12/03 18:18
S26	129	S25 and fpga	US-PGPUB; USPAT	OR	ON	2004/12/13 11:21
S27	6	S26 and memory with reconfiguring	US-PGPUB; USPAT	OR	ON	2004/12/03 18:30
S28	34	711/170.ccls. and ((reconfigur$5 rearrang$4) and application adj specific)	US-PGPUB; USPAT	OR	ON	2004/12/03 18:34
S29	50	711/170.ccls. and FPGA	US-PGPUB; USPAT	OR	ON	2004/12/13 16:42
S30	208	711/170.ccls. and reconfig$7	US-PGPUB; USPAT	OR	ON	2004/12/14 15:49
S31	1	"6779131".pn.	US-PGPUB; USPAT	OR	ON	2004/12/13 11:25
S32	0	("6779131").URPN.	USPAT	OR	ON	2004/12/13 11:26
S33	9	("5892896" | "6060339" | "6081463" | "6154851" | "6204562" | "6363502" | "6405324" | "6483755" | "6530005").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2004/12/13 11:42
S34	12	direct adj execution adj logic	US-PGPUB; USPAT; USOCR	OR	ON	2004/12/13 11:47
S35	4	711/170.ccls. and programmable adj logic adj blocks	US-PGPUB; USPAT; USOCR	OR	ON	2004/12/13 12:16
S36	5	"869200".ap.	US-PGPUB; USPAT; USOCR	OR	ON	2004/12/13 12:16
S37	3	711/171-172.ccls. and FPGA	US-PGPUB; USPAT	OR	ON	2004/12/13 16:42
S38	50	711/170.ccls. and FPGA	US-PGPUB; USPAT	OR	ON	2004/12/13 16:42
S39	50	711/170.ccls. and FPGA	US-PGPUB; USPAT; USOCR	OR	ON	2004/12/13 16:42

S40	3	711/171-172.ccls. and FPGA	US-PGPUB; USPAT; USOCR	OR	ON	2004/12/13 16:43
S41	8	711/173.ccls. and FPGA	US-PGPUB; USPAT; USOCR	OR	ON	2004/12/13 16:43
S42	78	711/170.ccls. and reprogram$5	US-PGPUB; USPAT	OR	ON	2004/12/14 15:49
S43	78	711/171-172.ccls. and (reprogram$5 reconfig$6)	US-PGPUB; USPAT	OR	ON	2004/12/14 15:50
S44	70	S43 not S42	US-PGPUB; USPAT	OR	ON	2004/12/14 15:51
S45	346	711/170-172.ccls. and ((configur$5).ti. (configur$6).ab.)	US-PGPUB; USPAT	OR	ON	2004/12/14 15:52
S46	14	711/170-172.ccls. and ((configur$5).ti. (configur$6).ab.) and prefetch	US-PGPUB; USPAT	OR	ON	2004/12/14 15:52
S47	73	711/170-172.ccls. and ((configur$5).ti. (configur$6).ab.) and bandwidth	US-PGPUB; USPAT	OR	ON	2004/12/14 15:52
S48	6	711/170-172.ccls. and ((configur$5).ti. (configur$6).ab.) and vhdl	US-PGPUB; USPAT	OR	ON	2004/12/14 15:52
S49	35	711/170-172.ccls. and ((configur$5).ti. (configur$6).ab.) and matrix	US-PGPUB; USPAT	OR	ON	2004/12/14 15:53
S50	12	711/170-172.ccls. and ((configur$5).ti. (configur$6).ab.) and parallelism	US-PGPUB; USPAT	OR	ON	2004/12/14 15:53
S51	1	"6553477".pn.	US-PGPUB; USPAT	OR	ON	2004/12/17 11:03
S52	3	711/170-173.ccls. and reconfigurable adj processor	US-PGPUB; USPAT; JPO	OR	ON	2004/12/30 20:10
S53	9	("20030046530" | "5737524" | "5872919" | "5915104" | "5953512" | "6000014" | "6104415" | "6216219" | "6339819").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2004/12/30 19:28
S54	207	reconfigurable adj processor	US-PGPUB; USPAT; JPO	OR	ON	2004/12/30 19:29
S55	515	reconfigurable adj2 processor	US-PGPUB; USPAT; JPO	OR	ON	2004/12/30 19:29
S56	308	S55 not S54	US-PGPUB; USPAT; JPO	OR	ON	2004/12/30 19:39

S57	104	S55 and ("711" "713").clas.	US-PGPUB; USPAT; JPO	OR	ON	2004/12/30 19:42
S58	7	(adaptive adj processor) and ("711" "713").clas.	US-PGPUB; USPAT; JPO	OR	ON	2004/12/30 19:43
S59	3	S58 not S57	US-PGPUB; USPAT; JPO	OR	ON	2004/12/30 19:43
S60	0	"008128".pa.	US-PGPUB; USPAT; JPO	OR	ON	2004/12/30 20:10
S61	5	"008128".ap.	US-PGPUB; USPAT; JPO	OR	ON	2004/12/30 20:14
S62	34	src adj computers	US-PGPUB; USPAT; JPO	OR	ON	2004/12/30 20:15
S63	15	711/118.ccls. and reconfigurable near3 (memory cache RAM random adj access adj memory processor)	US-PGPUB; USPAT	OR	ON	2005/01/03 13:19
S64	6	711/117.ccls. and reconfigurable near3 (memory cache RAM random adj access adj memory processor)	US-PGPUB; USPAT	OR	ON	2005/01/03 11:58
S65	4	"859051".ap.	US-PGPUB; USPAT	OR	ON	2005/01/03 12:06
S66	1	"6678790".pn.	US-PGPUB; USPAT	OR	ON	2005/01/03 12:29
S67	2	"021492".ap.	US-PGPUB; USPAT	OR	ON	2005/01/10 07:41

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/869,200	06/16/2004	Daniel Poznanovic	SRC028	5929

25235 7590 01/14/2005

HOGAN & HARTSON LLP
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1200 SEVENTEENTH ST
DENVER, CO 80202

EXAMINER	
THOMAS, SHANE M	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 01/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/869,200	POZNANOVIC ET AL.	
	Examiner	Art Unit	
	Shane M Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 June 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is responsive to the application filed 6/16/2004. Claims 1-24 are presented for examination.

The examiner requests, in response to this Office action, any reference(s) known to qualify as prior art under 35 U.S.C. sections 102 or 103 with respect to the invention as defined by the independent and dependent claims. That is, any prior art (including any products for sale) similar to the claimed invention that could reasonably be used in a 102 or 103 rejection. This **request** does not require applicant to perform a search. This request is not intended to interfere with or go beyond that **required** under 37 C.F.R. 1.56 or 1.105.

The request may be fulfilled by asking the attorney(s) of record handling prosecution and the inventor(s)/assignee for references qualifying as prior art. A simple statement that the query has been made and no prior art found is sufficient to fulfill the request. Otherwise, the fee and certification requirements of 37 CFR section 1.97 are waived for those documents submitted in reply to this request. This waiver extends only to those documents within the scope of this request that are included in the application's first complete communication responding to this requirement. Any supplemental replies subsequent to the first communication responding to this request and any information disclosures beyond the scope of this are subject to the fee and certification requirements of 37 CFR section 1.97.

In the event prior art documentation is submitted, a discussion of relevant passages, figs. etc. with respect to the claims is requested. The examiner is looking for specific references to 102/103 prior art that identify independent and dependent claim limitations. Since applicant is

most knowledgeable of the present invention and submitted art, his/her discussion of the reference(s) with respect to the instant claims is essential. **A response to this inquiry is greatly appreciated.**

The examiner also requests, in response to this Office action, that support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line no(s). in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

Drawings

The element --computation logic 201-- of paragraph 53 should be corrected to 200 as per figure 2.

Claim Objections

Claims 1-23 are objected to because of the following informalities:

As per claim 1, the term -- the memory-- of line 3 should be amended to read --the *first* memory-- since --*the* memory-- has not been previously defined. Appropriate correction is required.

As per claim 2, the term --the processor-- should be amended to --the *reconfigurable* processor since the term --*the* processor-- has not been previously defined in the claims.

As per claim 5, line 3, the term --memory-- has been mistakenly duplicated.

As per claim 8, the term --prefetch unit-- should be amended to --*data* prefetch unit-- since the term --prefetch unit-- has not been previously defined in the claims.

As per claim 11, the term --the unit-- should be amended to --the data prefetch unit-- since the term --the unit-- has not been previously defined in the claim.

As per claim 15, the term --at least of the-- of line 2 should be corrected to read --at least *one* of--.

As per claim 17, the term --the data access unit-- of lines 4-5 should be amended to --*a* data access unit-- since the term --*the* data access unit-- has not been previously defined in the claim.

Claims 3,4,6,7,9,10, 12-14,16, and 18-23, are objected to as being dependent on objected claims.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-10, 13, and 14, are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As per claim 1, the terms --first characteristic type-- and --second characteristic type-- are not clearly defined in the Applicant's specification. Applicant is reminded of **37 C.F.R. 1.75 (d)(1)** which states that the claim or claims must conform to the invention as set forth in the remainder of the specification and the terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description. (See 1.58(a).) The phrases --first characteristic type-- and --second characteristic type-- are not terms of art; nonetheless, for the purposes of examination, the Examiner shall regard the terms as meaning any type of memory (e.g. a SRAM, Flash Rom, DRAM, hard disk, etc.).

As per claims 2 and 13, the Applicant's disclosure does not explicitly mention that the reconfigurable processors cannot have a cache. The disclosure mentions in the Background section, and specifically in paragraphs 16-17, the drawbacks of having a hard-wired cache in a system; however, the Detailed Description does not explicitly state that the reconfigurable processor as taught by the Applicant *cannot* contain a cache. It appears to the Examiner that no specific (hard-wired) cache memory is included in the reconfigurable processor as taught in the disclosure; rather an on-board memory and user-logic can be configured based on a program (paragraph 52). Therefore, for the purposes of examination, the Examiner shall interpret the claim such that the reconfigurable processor of claim 1 does not contain a *hard-wired* (specific) cache.

As per claims 3 and 14, it follows from the rejection for claims 2 and 13, that since Applicant's disclosure does not explicitly state that a reconfigurable processor *cannot* have a cache, the disclose further does not explicitly teach that the reconfigurable processor cannot have

a cache line-sized unit of contiguous data. For the purposes of examination and based on the discussion of claim 2 above, the Examiner shall interpret the limitation of claim 3 such that the reconfigurable processor of claim 1 does not have a *hard-wired* (specific) cache line-sized unit of contiguous data being retrieved from the [second] memory.

As per claim 4, it is not clear to which memory the term –the memory—refers as –the memory lacks antecedent basis--. For the purposes of examination, the Examiner shall interpret the term –the memory—to indicate the –second memory—of claim 1.

As per claim 7, the term --disassembled-- is not known to be a term of art, and further, not specifically defined in the Applicant's specification. Nonetheless, for the purposes of examination, the Examiner shall regard the term --disassembled-- with the broadest reasonable interpretation. Refer to **37 C.F.R. 1.75 (d)(1)**.

Claims 5, 6, and 8-10, are rejected as being dependent on rejected base claim 1.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2-4,8-10, and 15-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 2, it is not clear which memory (first or second memory) the term --the memory-- is referring to since --the memory-- lacks antecedent basis. The Examiner recommends amending the term --the memory-- to overcome this rejection. Nonetheless, for the purposes of examination, the Examiner shall interpret the claim as --the first memory--.

As per claim 3, it is not clear which memory (first or second memory) the term --the memory-- is referring to since --the memory-- lacks antecedent basis. The Examiner recommends amending the term --the memory-- to overcome this rejection. Nonetheless, for the purposes of examination, the Examiner shall interpret the claim as --the second memory--.

As per claim 4, it is not clear which memory (first or second memory) the term --the memory-- is referring to since --the memory-- lacks antecedent basis. The Examiner recommends amending the term --the memory-- to overcome this rejection. Nonetheless for the purposes of examination, the Examiner shall interpret that claim as --the second memory--.

As per claim 8, it is not clear whether the processor memory is the same as the second memory or if the processor memory is a separate (third) memory since the data prefetch unit is claimed as retrieving data from both a second memory and a processor memory. The Examiner shall interpret the second memory as being a processor memory.

As per claims 15 and 17, it is not clear if the term --the data access unit-- is referring to --the data prefetch unit-- or is a new entity being defined by the claim since the term --*the* data access unit-- lacks antecedent basis. Nonetheless, for the purposes of examination, the Examiner shall regard the term --the data access unit-- to be a separate entity based in part from the Applicant descriptions of the drawings on page 8 showing that the data prefetch unit and data access unit are distinct entities.

As per claim 19, it is not clear whether the term --a data access unit-- is the same data access unit that has been defined in claim 17 or the --a data access unit-- is a different data access unit that performs the limitation of claim 19 and does not perform the limitation of the data

access unit of claim 17. For the purposes of examination, the Examiner shall interpret the --a data access unit-- as --*the* data access unit-- [of claim 17].

As per claims 9-10 and 16-23, the claims are rejected as being dependent on rejected claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Paulraj (U.S. Patent Application Publication No. 2003/0084244).

As per claim 1, Paulraj shows a reconfigurable processor in figure 6 and a first memory (L1) having a first characteristc memory type (line size, blocking factor, associativity, etc.) and a second memory (L2) having a second characteristic memory type (line size, blocking factor, associativity, etc.). Refer to paragraph 23. Paulraj further teaches a functional unit 102 that executes applications using the memories L1 and L2 (paragraph 9). As is known in the art, a cache memory controller is often used to access and move data between a memory hierarchy. The Examiner is considering a data prefetch unit to be the logic assocatied with the moving, and only the moving, of data between the first and second memories (L1 and L2) since Paulraj shows

a connection between the levels of cache in figure 6. This logic as well as the first and second memory types (L1 and L2) are configued by a program – refer to paragraphs 23-24. The data prefetch unit as defined by the Examiner must be configued as well by the program when moving data since the cache line size and blocking factor can change, so different amounts of data can be exchanged for the same access when different programs run.

As per claims 2 and 13, as taught in paragraphs 23 and 29 of Paulraj, no specific cache is present in the system of Paulraj. Rather, an FPGA is utilized as representing a caching hierarchy and is optimized based on the memory needs of a specific program running on the reconfigurable processor.

As per claims 3 and 14, Paulraj teaches in paragraph 23 that a specific cache line size of contiguous data is not retrieved since the data line size is optimized based on the memory needs of the program when executing on the reconfigurable processor. Refer also to paragraph 29.

As per claim 4, Paulraj teaches that a load/store unit is used to access the caches (L1-L3) in order to determine if cache data is present in the cache hierarchy (paragraph 6). Since the functional unit 102 (figure 6) is responsible for accessing the programmable memory unit 104, the Examiner is therefore considering the load/store unit logic of the programmable memory unit that is responsible for for accessing the L1 and L2 caches (first and second memory types) to be a memory controller. It can be seen that the memory controller, as defined by the Examiner, controls the transfer of data between the memory (assuming second memory L2) and the data prefetch unit, since the memory controller (load/store unit logic) is responsible for retrieving the data from the cache if a hit occurs (paragraph 4).

As per claim 5, as taught in paragraph 1, an external memory (element 18, figure 1) is generaly coupled to a microprocessor and holds data to be used by the microcontroller during program execution. The Examiner is considering the process of writing data back to the external memory from the FPGA memory 104 containing the caches (on-board memory), such as during a write-back scheme as known in the art, to be performed by the data prefetch unit portion of the functional logic as defined above by the Examiner. The data prefetch logic, as defined above, is responsible for all of the transfer of data into, out of, and between the FPGA memory 104.

As per claim 6, the Examiner is regarding a --register-- in its broadest reasonable sense and it thus considering it be to be a unit of logic. Therefore, the portion of the function logic that is responsible for the movement of data (as defined above to be the data prefetch unit) is being considered by the Examiner as containing a --register-- portion of the reconfigurable processor since, for instance, the blocking factor and line size of the programmable memory 112 can change, a --register-- or portion of the reconfigurable processor must be set in order to indicate the currnet line size and blocking factor when a given application is being run on the reconfigurable processor at a given point in time. Refer to paragraph 23.

As per claim 7, the Examiner is considering the process of --disassembling the data prefetch unit-- as modifying the data prefetch unit logic of the fucntion logic 102 every time the program being executed by the reconfigurable processor changes. It can be seen that the data prefetch unit changes during these intervals since the cache line size, blocking factor, and associativity of the FPGA changes when optimal for the next program to be executed (refer to paragraph 23). Thus it can be seen that the data prefetch unit logic is --disassembled-- when another program is executed by the reconfigurable processor of Paulraj.

As per claim 8, as can be seen that the FPGA memory 112, that comprises the first and second memories (L1 and L2) and which is accessed by the data prefetch unit of the functional unit 102 as discussed above, is a --processor memory-- (part of cpu 110). Therefore, since the data pretech unit can access the L2 cache as discussed above in the rejection of claim 1, the data prefetch unit can retrive data from the L2 portion of --processor memory--112.

As per claim 9, as shown in figure 1 and taught in paragraph 1 of Paulraj, the system 10 is actually a microprocessor, which contains a memory controller 14. The main difference between the prior art of figure 1 and the invention of Paulraj in figure 6 is that the memroy hierarchy is configurable and accessed by a fucntional unit in lieu of a separate memory controller logic (paragraph 9). Therefore, since the memory controller logic for accessing the cache hierarchy is still contained within cpu 110 of figure 6, it can be seen that the cpu 110 is actually a microprocessor. It follows that the --processor memory-- 112 is therefore a --microprocessor memory--.

As per claim 10, since the cpu 110 of figure 6 is a reconfigurable processer (able to reconfigure its memory heirarchy to match the needs of the application it is currently running), it can be seen that the cpu memory 112 is a reconfigurable processor memory.

As per claim 11, Paulraj depicts a reconfigurable hardware system in figure 6. Paulraj further teaches in paragraph 26 that when a particular application is to be run by the reconfigrable processor 110, a configuration vector is retrieved to program the programmable memory 112 (figure 6). As shown in figure 6, the step of accesing the configuration vector is executed outside of the reconfigurable processor 110. Therefore, the Examiner is considering the memory that contains the configuration vectors to be a--common memory-- and a data

prefetch unit (reconfiguration unit 106 executing on the reconfigurable processor 110) accessing the common memory in order to determine how to program the memory 112 (paragraph 29). The data prefetch unit 106 is --configured-- by an application to be excuted on the sysem 110 since when a new application is to be executed, the data prefetch unit is called upon (or configured) to access the configuration vector for the particular application.

As per claim 12, the Examiner is considering a --memory controller-- to be the system portion utilized when creating a new configuration vector for an application. Such a process occurs in figure 5 and taught in paragraghs 23-25 of Paulraj. When a new configuration vector is created by analizing performance information that has been collected for the application. The Examiner is thereby considering the --memory controller-- to be the element of the reconfigurable hardware system that is associated with storing the new configuration vector into the common memory so that the vector can be accessed later when the same application is run again.

As per claim 15, the Examiner is considering the reconfiguration module 106 of the reconfigurable processsor 110, as comprising two distinct elements: a --computational unit-- and a --data access unit--. The data access unit is the element that is responsible for accessing the configuration vector as taught in paragraph 29 of Paulraj; or in other words, the Examiner is considering the --data access unit-- to be the same as the --memory controler-- defined in the rejection of claim 12. The Examiner is further considering the --computational unit-- of the rconfiguration module 106 to be the element that sets up the programmable memory module 104 using the configuration vector that was accessed by the --data access unit-- (paragraph 29).

As per claim 16, as taught by Paulraj in paragraph 29, the --data access unit-- supplies the configuration vector to the --computational unit-- in order to set up the programmable memory 104 as required by the application to be run on the reconfurable processor 110.

As per claim 17, the Examiner is considering a --data prefetch unit-- to be the reconfiguration unit 106 of reconfigurable processor 110 (figure 6). As taught in paragraph 26 and 29 of Paulraj, the --data prefetch unit-- accesses a memory in order to determine if a configuration vector is known for a given application, and if so, the vector is retrieved (from the memory). If this --data-- (configuration vector) is not known then a simulation is performed with the application in order to collect performance information. The Examiner is considering the element that executes and collects the performance data as being a --computational unit-- and the element of Paulraj that stores the configuration vector, once determined, to be a --data access unit-- since it stores the vector into the --memory-- from which it can be later retrieved (step 212 of figure 5). The --computational unit--, --data access unit--, and the --data prefetch unit-- are all --configured-- by a program (application) since (1) a new application configures the computational unit portion of the reconfiguration unit to perform a simulation in order to determine the optimal memory hierarchy organization; (2) the new application configures the --data access unit-- to store and retrieve (step 212) the configuration vector for that particular application; and (3) the --data prefetch unit-- is configured by the application to determine if a configuration file exists for the application and if so, the data prefetch unit is configured by the program the programmable memory 112 in order to optimize the programmable memory for that particular application.

As per claim 18, the --data-- (configuration vector) is transferred from the

--computational unit-- to the --data access unit-- when the configuration unit has created a configuration vector (step 208 of figure 5). The --data-- is written to the memory --from-- the --data prefetch unit-- since the data prefetch unit (reconfiguration unit 106) is the element that executed the beginning of the configuration vector creation process (step 200 of figure 5). Refer to paragraph 26. Thus the Examiner is considering the data as being written --from-- the data prefetch unit.

As per claim 19, as taught in paragraph 26, if the configuration vector is known, the vector is retrieved from the memory to the data prefetch unit (reconfiguration unit 106). The data is read directly from the data prefetch unit when a request to create a configuration vector is made for a new application as shown in figure 6 since the data prefetch unit is responsible for being the vector creation process. The data is directed from the data prefetch unit (reconfigure logic) to be read from the memory by the data access unit to the computational unit where it is processed to produce a configuration vector.

As per claim 20, as stated above, the configuration vector (--data--) is created by the computational unit via acquired simulation data. The configuration vector is the resultant product that is transferred from the memory to the data prefect unit when it is determined that the configuration vector for the application is available (paragraph 26). Thus --all-- of the data that is transferred is processed by the computational unit (albeit before the transfer occurs) since the data prefetch unit required the entire configuration vector in order to set up the programmable memory 112.

As per claim 21, Paulraj shows in paragraph 26 that an explicit request for the configuration vector for the current application results in the data (if it exists) selected for the optimal configuration of the programmable memory 112 for that application.

As per claim 22, the Examiner is not considering the data (configuration vector) to be the size of a complete cache line since the data is used to create a cache hierarchy. In other words, the caches (L1-L3) of the programmable memory 112 are not programmed when the data is transferred from the memory to the data prefetch unit; therefore, the data cannot be a complete cache line.

As per claim 23, since the Examiner defined the portion of the reconfiguration unit that accesses the configuration file (data) from the memory, the Examiner is defining the logic that controls the actual transfer of that data to the data prefetch unit (portion of the reconfiguration unit that executes the fetch of the configuration vector and then programs the programmable memory 112) to be a --memory controller--. Thus the data access unit determines whether a configuration vector exists for an application and if so, the memory controller sends that data to the data prefetch unit.

As per claim 24, The Examiner is considering the element that executes and collects the performance data as being a --computational unit-- and the element of Paulraj that stores and retrieves the configuration vector, once determined, to be a --data access unit-- since it stores the vector into the --memory-- from which it can be later retrieved (step 212 of figure 5). The --computational unit-- and --data access unit -- are --configured-- by a program (application) since (1) a new application causes in the configuration of the computational unit portion of the reconfiguration unit to perform a simulation in order to determine the optimal memory hierarchy

organization for the application and (2) the new application causes the configuration of the --data access unit-- to store and retrieve (step 212) the configuration vector for that particular application. Refer to paragraphs 25-27.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Poznanovic (U.S. Patent Application Publication No. 2003/0046530) teaches a reconfigurable processor (figure 2) which can be reprogrammed based on a program.

Vondran (U.S. Patent No. 6,243,791) illustrates an example of the operation of a cache controller in a cache hierarchy (column 1, lines 54-67).

Otterness (U.S. Patent No. 6,460,122) further teaches common operation of a cache controller in column 21, lines 1-16.

Darling (U.S. Patent No. 6,714,041) teaches a reconfigurable system (figure 5) that is able to be reprogrammed based on a program.

Burton (U.S. Patent Application Publication No. 2003/0088737) teaches uncached device operations in a reconfigurable processor system.

Gschwind et al. (U.S. Patent Application Publication No. 2003/0046492) teaches a reconfigurable memory array which can be operated as a cache or a non-cache memory.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M Thomas whose telephone number is (703) 605-0725.

Please note: the aforementioned number will change to (571) 272-4188 effective October 19, 2004. The examiner can normally be reached M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached on (703) 305-3821, which will change to (571) 272-4182 effective October 19, 2004. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane M. Thomas

MATTHEW ANDERSON
PRIMARY EXAMINER
GROUP 2100

Notice of References Cited	Application/Control No. 10/869,200	Applicant(s)/Patent Under Reexamination POZNANOVIC ET AL.	
	Examiner Shane M Thomas	Art Unit 2186	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-2003/0084244 A1	05-2003	Paulraj, Dominic	711/118
	B	US-2003/0046530 A1	03-2003	Poznanovic, Daniel	713/100
	C	US-6,243,791	06-2001	Vondran, Jr., Gary Lee	711/120
	D	US-6,460,122	10-2002	Otterness et al.	711/154
	E	US-6,714,041	03-2004	Darling et al.	326/38
	F	US-2003/0088737	05-2003	Burton, Lee	711/118
	G	US-2003/0046492 A1	03-2003	Gschwind et al.	711/118
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FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	"Summary: The Cache Read/Write Process," The PC Guide, 2001, www.pcguide.com/ref/mbsys/cache/func.htm.
	V	Chien et al., "Safe and Protected Execution for the Morph/AMRM Reconfigurable Processor," IEEE, 1999, pp 1-13.
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims

Application No.	Applicant(s)	
10/869,200	POZNANOVIC ET AL.	
Examiner	**Art Unit**	
Shane M Thomas	2186	

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
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Search Notes

Application No.	Applicant(s)	
10/869,200	POZNANOVIC ET AL.	
Examiner	**Art Unit**	
Shane M Thomas	2186	

SEARCHED			
Class	Subclass	Date	Examiner
711	170-173	12/2/2004	SMT
712	15	12/3/2004	SMT

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
Inventor Name Seach	12/3/2004	SMT
IEEE Seach	12/3/2004	SMT
EAST Search	1/10/2005	SMT

4-12-05

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Client Matter No. 80404.0033.001
Express Mail No.: EV330612115US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No. 10/869,200 Application of: POZNANOVIC Filed: June 16, 2004 Art Unit: 2186 Examiner: THOMAS, Shane M Attorney Docket No. SRC028 For: SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE	Confirmation No.: 5929 Customer No.: **25235**

AMENDMENT AND RESPONSE PURSUANT TO OFFICE ACTION DATED JANUARY 14, 2005

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the office communication mailed January 14, 2005 please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Amendments to the Drawings begin on page 7 of this paper and include both an attached replacement sheet and an annotated sheet showing changes.

Remarks/Arguments begin on page 8 of this paper.

\\\BO - 80404/0033 - 175820 v1

An **Appendix** including 1 sheet of amended drawing figures is attached following page 8 of this paper.

A. Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A reconfigurable processor comprising:

a first memory having a first characteristic memory bandwidth and/or memory utilization ~~type~~; and

a data prefetch unit coupled to the first memory, wherein the data prefetch unit retrieves data from a second memory of second characteristic memory bandwidth and/or memory utilization and place the retrieved data in the first memory ~~type~~ and wherein at least the first ~~the~~ memory ~~types~~ and data prefetch unit are configured by a program.

2. (Currently Amended) The reconfigurable processor of claim 1, wherein the reconfigurable processor does not have a cache to store data from the first memory.

3. (Currently Amended) The reconfigurable processor of claim 1, wherein the second memory has a characteristic line size and the data retrieved from the second memory is not a ~~cache~~ line-sized unit of contiguous data.

4. (Currently Amended) The reconfigurable processor of claim 1, wherein the data prefetch unit is coupled to a memory controller that controls the transfer of the data between the second memory and the data prefetch unit.

5. (Currently Amended) The reconfigurable processor of claim 1, wherein the data prefetch unit receives processed data from on-processor memory and writes the processed data to an external off-processor ~~memory~~ memory.

6. (Original) The reconfigurable processor of claim 1, wherein the data prefetch unit comprises at least one register from the reconfigurable processor.

7. (Original) The reconfigurable processor of claim 1, wherein the data prefetch unit is disassembled when another program is executed on the reconfigurable processor.

8. (Currently Amended) The reconfigurable processor of claim 1 wherein said second memory comprises a processor memory and said data prefetch unit is operative to retrieve data from [[a]] the processor memory.

9. (Original) The reconfigurable processor of claim 8 wherein said processor memory is a microprocessor memory.

10. (Original) The reconfigurable processor of claim 8 wherein said processor memory is a reconfigurable processor memory.

11. (Currently Amended) A reconfigurable hardware system, comprising:

a common memory; and

one or more reconfigurable processors coupled to the common memory, wherein at least one of the reconfigurable processors includes a data prefetch unit to read and write data between the data prefetch unit and the common memory, and wherein the data prefetch unit is configured by a program executed on the system.

12. (Original) The reconfigurable hardware system of claim 11, comprising a memory controller coupled to the common memory and the data prefetch unit.

13. (Currently Amended) The reconfigurable hardware system of claim 11, wherein the one or more reconfigurable processors are [[is]] not coupled to a cache.

14. (Currently Amended) The reconfigurable hardware system of claim 11, wherein the common memory has a characteristic line size and the data written and read between the data prefetch unit and the common memory is not a ~~cache~~ line-sized unit of contiguous data.

15. (Currently Amended) The reconfigurable hardware system of claim 11, wherein the at least one of the reconfigurable processors also includes a computational unit coupled to ~~the~~ a data access unit.

16. (Original) The reconfigurable hardware system of claim 15, wherein the computational unit is supplied the data by the data access unit.

17. (Currently Amended) A method of transferring data comprising:

transferring data between a memory and a data prefetch unit in a reconfigurable processor; and

transferring the data between a computational unit and ~~the~~ a data access unit, wherein the computational unit and the data access unit, and the data prefetch unit are configured by a program.

18. (Original) The method of claim 17, wherein the data is written to the memory, said method comprising:

transferring the data from the computational unit to the data access unit; and

writing the data to the memory from the data prefetch unit.

19. (Currently Amended) The method of claim 17, wherein the data is read from the memory, said method comprising:

transferring the data from the memory to the data prefetch unit; and

reading the data directly from the data prefetch unit to the computational unit through [[a]] the data access unit.

20. (Original) The method of claim 19, wherein all the data transferred from the memory to the data prefetch unit is processed by the computational unit.

21. (Original) The method of claim 19, wherein the data is selected by the data prefetch unit based on an explicit request from the computational unit.

22. (Original) The method of claim 17, wherein the data transferred between the memory and the data prefetch unit is not a complete cache line.

23. (Original) The method of claim 17, wherein a memory controller coupled to the memory and the data prefetch unit, controls the transfer of the data between the memory and the data prefetch unit.

24. (Original) A reconfigurable processor comprising:

a computational unit; and

a data access unit coupled to the computational unit, wherein the data access unit retrieves data from memory and supplies the data to the computational unit, and wherein the computational unit and the data access unit are configured by a program.

REMARKS/ARGUMENTS

Claims 1-24 remain in the application. Claims 1, 2, 5, 8, 11, 15 and 17 are amended to address informalities noted in the Office action. No new matter is added by these amendments.

A. Drawings.

The correction made to Fig. 2 is believed to overcome the objection to the drawings.

B. Claim Objections

Claims 1, 2, 5, 8, 11, 15 and 17 are amended to overcome the objections stated in the office action. It is respectfully requested that the objections to claims 1-23 be withdrawn.

C. Rejections under 35 U.S.C. 112.

Claims 1-10, 13 and 14 were rejected under 35 U.S.C. 112. This rejection is respectfully traversed.

Specifically, the Office action questions the reference to a first characteristic memory type and a second characteristic memory type in claim 1. This is illustrated, for example, in Fig. 3 in which a logic block 300 moves data from a first memory 305 having a first characteristic memory type to a second memory 307 having a second characteristic memory type. As set out in the paragraphs [0007]-[0016] of the specification, for example, the memory characteristics may include one or more of the following characteristics: line size, associativity, replacement policy, write policy, and cache size, all of which provide varying memory bandwidth efficiency and/or memory bandwidth utilization. The amendment to claim 1 is believed to clarify this feature of the invention and overcome the objections raised in the Office action.

With respect to claims 2 and 13, the examiner's interpretation that claims 2 and 13 do not require a hard-wired cache is accurate. It is noted that these limitations appear in claims 2 and 13, not claim 1.

The amendments to claims 3, 4 and 14 are believed to clarify the questions raised in the Office action.

Claims 2-4, 8-10 and 15-23 were rejected under 35 U.S.C. 112 as indefinite. The amendments to claims 2, 3, 4, 8, 15 and 17 are believed to overcome the rejections.

D. Rejections under 35 U.S.C. 102.

Claims 1-24 were rejected under 35 U.S.C. 102 based upon Paulraj. This rejection is respectfully traversed.

Independent claim 1 calls for a reconfigurable processor. As set out in Applicant's specification at paragraph [0039], a reconfigurable processor is a computing device that instantiates an algorithm as hardware. Although the reference show a reconfigurable cache, Paulraj does not show or suggest a reconfigurable processor that instantiates an algorithm as hardware. Moreover, nothing in Paulraj would suggest the rather significant changes required to replace the CPU with a reconfigurable processor. For at least these reasons claim 1 is not anticipated nor made obvious by Paulraj.

Claims 2-10 that depend from claim 1 are allowable over Paulraj for at least the same reasons as claim 1 as well as the limitations that are presented in those claims.

Claim 11 calls for a reconfigurable hardware system comprising one or more reconfigurable processors. As noted above with respect to claim 1, Paulraj does not show or suggest even one reconfigurable processor. For at least these reasons claim 11 and claims 12-16 that depend from claim 11 are believed to be allowable over Paulraj.

Independent claim 17 calls for, among other things, transferring data between a memory and a data prefetch unit in a reconfigurable processor. As noted above, Paulraj does not show or suggest a reconfigurable processor, nor transferring data between a memory and a data prefetch unit in a reconfigurable

processor. For at least these reasons claim 17 and claims 18-23 that depend from claim 17 are allowable over Paulraj.

Claim 24 calls for a reconfigurable processor having a computational unit and a data access unit that are configured by a program. Paulraj does not show a reconfigurable processor. Moreover, the element of Paulraj that stores and retrieves the configuration vector is not configurable by a program. Similarly, the element that executes and collects performance data is not configurable by a program. Paulraj does not suggest making these elements configurable.

E. Conclusion.

The references that were cited but not relied upon are no more relevant than the references that were relied upon. In view of all of the above, the claims are now believed to be allowable and the case in condition for allowance which action is respectfully requested. Should the Examiner be of the opinion that a telephone conference would expedite the prosecution of this case, the Examiner is requested to contact Applicants' attorney at the telephone number listed below.

Any fee deficiency associated with this submittal may be charged to Deposit Account No. 50-1123.

Respectfully submitted,

April 11, 2005

Stuart T. Langley, Reg. No. 33,940
Hogan & Hartson LLP
One Tabor Center
1200 17th Street, Suite 1500
Denver, Colorado 80202
(720) 406-5335 Tel
(303) 899-7333 Fax

B. Amendments to the Drawings:

The attached sheet of drawings includes changes to Fig. 2. This sheet which includes Figs. 1-2 replaces the original sheet including Fig. 1-2. In Figure 2, element 201 is correctly identified.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes

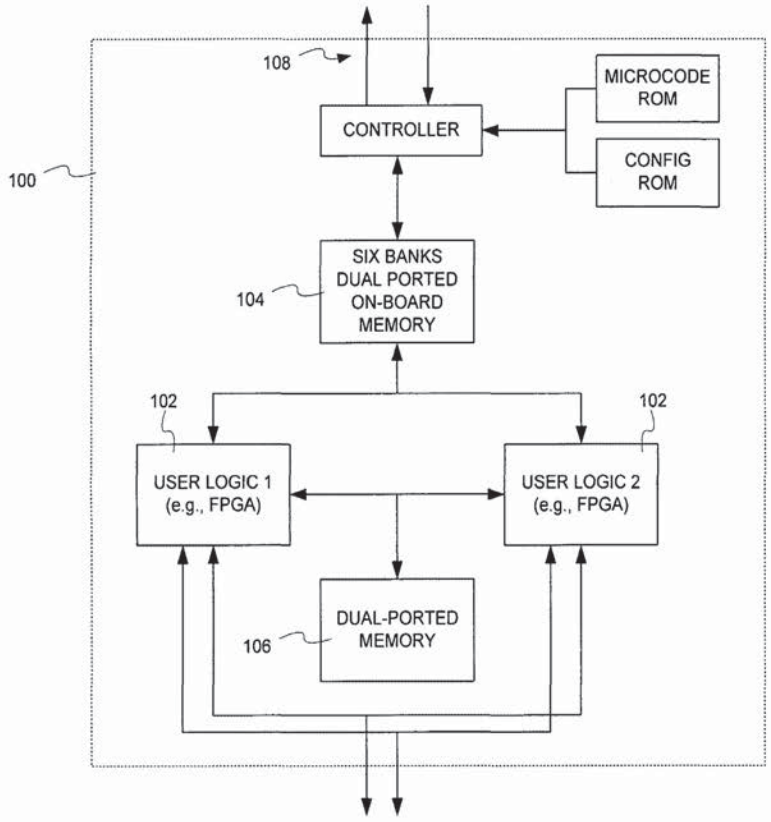

FIG. 1

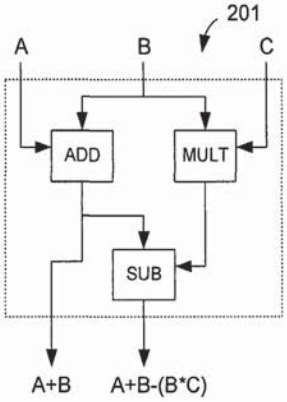

FIG. 2

REPLACEMENT SHEET

1/12

Client Matter No. 80404.0033.001
Express Mail No.: EV330612115US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No. 10/869,200	Confirmation No.: 5929
Application of: POZNANOVIC	Customer No.: **25235**
Filed: June 16, 2004	
Art Unit: 2186	
Examiner: THOMAS, Shane M	
Attorney Docket No. SRC028	
For: SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE	

CERTIFICATE OF MAILING BY EXPRESS MAIL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The undersigned hereby certifies that the following documents:

- Amendment and Response Pursuant to Office Action(10 pages);
- Replacement drawing sheet (1 sheet);
- Information Disclosure Statement and copies of 3 references;
- Certificate of Mailing by Express Mail (1 page); and
- Return Receipt Postcard

relating to the above application, were deposited as "Express Mail", Mailing Label No. EV330612115US with the United States Postal Service, addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on April 11, 2005.

April 11, 2005
Date

Mailer

April 11, 2005
Date

Stuart T. Langley, Reg. No. 33,940
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1200 17th Street, Suite 1500
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(720) 406-5335 Tel
(303) 899-7333 Fax

\\\BO - 80404/0033 - 175820 v1

Express Mail No.EV330612115US
Attorney Docket No. SRC028
Client/Matter No. 80404.0033.001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Daniel Poznanovic, David E. Caliga, and Jeffrey Hammes Serial No. 10/809,200 Filed: June 16, 2004 For: SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE	Group Art Unit: 2186 Examiner: Thomas, Shane M. Confirmation No.: 5929

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. 1.97

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby submits for filing under 37 CFR 1.97 a disclosure statement. In submitting these references, no representation is made or implied that the references are or are not material to the examination of this application. The patents, publications or other information of which Applicant is presently aware are listed in Form PTO/SB/08A submitted herewith and copies of all such patents and publications are attached hereto.

No fee is believed due for this submittal pursuant Examiner's request for references in the Office Action dated January 14, 2005. However, any fee deficiency associated with this submittal may be charged to Deposit Account No. 50-1123.

Respectfully submitted,

4/11/05
Date

Stuart T. Langley, Reg. No. 33,940
HOGAN & HARTSON LLP
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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Application Number	10/809,200
Filing Date	June 16, 2004
First Named Inventor	Daniel Poznanovic et al.
Art Unit	2186
Examiner Name	Thomas, Shane M.
Attorney Docket No.	SRC028

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.[1]	Document No. No. – Kind Code[2]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-6,076,152	06/13/2000	Huppenthal et al.	
		US-6,247,110	06/12/2001	Huppenthal et al.	
		US-6,356,983	03/12/2002	Parks	
		US-6,594,736	06/15/2003	Parks	
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Examiner Initials	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns. Lines Where Relevant Passages or Relevant Figures Appear	T[6]

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) and application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Substitute for form 1449A/PTO				Application Number	10/809,200
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date	June 16, 2004
				First Named Inventor	Daniel Poznanovic et al.
				Art Unit	2186
(Use as many sheets as necessary)				Examiner Name	Thomas, Shane M.
Sheet	2	of	2	Attorney Docket No.	SRC028

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s) publisher, city and/or country where published	T[2]
.		**DALLY, BILL, HANRAHAN, PAT, FEDKIW, RON, "A Streaming Supercomputer", September 18, 2001, pp. 1-17.**	
		DALLY, WILLIAM J. et al., "Merrimac: Supercomputing with Streams", SC'03, November 15-21, 2003, Phoenix, AZ, 7 pages.	
		"Code Development and Porting Issues", SRC Computer, Inc., SRC-6E C Programming Environment v1.3 Guide, April 11, 2003, pp. 17-26.	

EXAMINER SIGNATURE		DATE CONSIDERED	

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[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) and application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2003

Application or Docket Number: 10869 200

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	24	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	24 minus 20=	* 4
INDEPENDENT CLAIMS	4 minus 3 =	* 1
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	385.00	OR	BASIC FEE	770.00
XS 9=		OR	X$18=	72
X43=		OR	X86=	86
+145=		OR	+290=	—
TOTAL		OR	TOTAL	928

CLAIMS AS AMENDED - PART II

4-1-05

AMENDMENT A	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 24	Minus	** 24	=
Independent	* 4	Minus	*** 4	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Certificate of Transmission under 37 CFR 1.8

Serial No. 10/869,200

Application of: Daniel Poznanovic, David E. Caliga, and Jeffrey Hammes

Filed: June 16, 2004

Art Unit: 2186

Examiner: Thomas, Shane M.

Attorney Docket No. SRC028

For: SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE

Confirmation No.: 5929

Customer No.: **25235**

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office

1. Information Disclosure Statement based on an International Search report.

on 6 June 2005
Date

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No. of Pages
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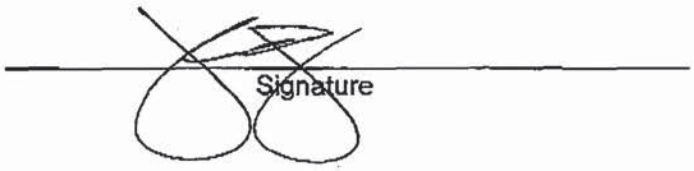

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Julie Lange
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Client Reference No. 80404.0033.001 Fax No. 719-448-5922

Attorney Docket No. SRC028
Client/Matter No. 80404.0033.001
Via Facsimile

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Confirmation No.: 5929
Daniel Poznanovic, David E. Caliga, Jeffrey Hammes	Examiner: Thomas, Shane M.
Serial No. 10/869,200	Art Unit: 2186
Filed: June 16, 2004	
For: SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE	

INFORMATION DISCLOSURE STATEMENT BASED ON AN INTERNATIONAL SEARCH REPORT

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

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Pursuant to 37 C.F.R. § 1.97(c), it is hereby certified that each item in this Information Disclosure Statement was cited in a communication from a foreign patent office (copy enclosed) in counterpart European application, PCT/US04/19663, mailed 31 MAY 2005, not more than three months prior to the filing of the statement (37 C.F.R. Section 1.97(e)). No petition fee is believed required, however, any fees associated with this communication may be made to Deposit Account No. 50-1123.

Respectfully submitted,

Date: 06 JUN 2005

William J. Kubida, Reg. No. 29,664
HOGAN & HARTSON
One Tabor Center
1200 17th Street, Suite 1500
Denver, Colorado 80202
(719) 448-5909 Tel
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Substitute for form 1449A/PTO				Application Number	10/869,200
				Filing Date	June 16, 2004
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				First Named Inventor	Daniel Poznanovic et al.
				Art Unit	2186
(Use as many sheets as necessary)				Examiner Name	Thomas, Shane M.
Sheet	1	of	1	Attorney Docket No.	SRC028

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.[1]	Document No. – Kind Code[2]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-2003/0084244 A1	05/01/2003	Paulraj	Entire Document
		US-2003/0046530 A1	03/06/2003	Poznanovic	
		US-			
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Serial No. 10/869,200

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Filed: June 16, 2004

Art Unit: 2186

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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) and application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	117	reconfigur$3 adj (processor micro-processor CPU processor)	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L3	143	reconfigur$3 adj (processor micro-processor CPU microprocessor)	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L4	6	reconfigur$3 adj (processor micro-processor CPU microprocessor) and "711".clas.	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L5	0	reconfigur$3 adj (processor micro-processor CPU microprocessor) and prefetch	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L7	12	711/170-173.ccls. and dynamic near3 logic	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L8	909	smc.as.	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L9	0	smc.as. and "711".clas.	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L10	0	smc.as. and "712".clas.	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L11	0	(smc and computers) .as. and "712".clas.	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L12	0	(smc and computers) .as.	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L13	0	(smc and computers).as.	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L14	10	(src and computers).as.	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L15	87	711/170.ccls. and dynamic$4 near3 configur$5	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L16	3	711/170.ccls. and dynamic$4 near3 configur$5 with cache	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L18	260	reconfigurable adj processor	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L19	4	"206189".ap.	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L20	1	"5024031".pn.	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L21	6	"869200".ap.	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L22	1694	711/170.ccls.	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L23	449	711/170.ccls. and (reconfigur$5 rearrang$4 application adj specific)	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54

L24	102	711/170.ccls. and matrix	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L25	58	711/170.ccls. and fpga	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L26	197	712/15.ccls.	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L27	276	711/170.ccls. and (application near2 specific application-specific)	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L28	260	reconfigurable adj processor	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L29	179	L28 and fpga	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L30	9	L29 and memory with reconfiguring	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L31	43	711/170.ccls. and ((reconfigur$5 rearrang$4) and application adj specific)	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L32	58	711/170.ccls. and FPGA	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L33	251	711/170.ccls. and reconfig$7	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L34	1	"6779131".pn.	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L35	0	("6779131").URPN.	USPAT	OR	ON	2005/07/06 13:54
L36	9	("5892896" | "6060339" | "6081463" | "6154851" | "6204562" | "6363502" | "6405324" | "6483755" | "6530005").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2005/07/06 13:54
L37	16	direct adj execution adj logic	US-PGPUB; USPAT; USOCR	OR	ON	2005/07/06 13:54
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L39	6	"869200".ap.	US-PGPUB; USPAT; USOCR	OR	ON	2005/07/06 13:54
L40	4	711/171-172.ccls. and FPGA	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L41	58	711/170.ccls. and FPGA	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L42	58	711/170.ccls. and FPGA	US-PGPUB; USPAT; USOCR	OR	ON	2005/07/06 13:54

L43	4	711/171-172.ccls. and FPGA	US-PGPUB; USPAT; USOCR	OR	ON	2005/07/06 13:54
L44	9	711/173.ccls. and FPGA	US-PGPUB; USPAT; USOCR	OR	ON	2005/07/06 13:54
L45	88	711/170.ccls. and reprogram$5	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L46	81	711/171-172.ccls. and (reprogram$5 reconfig$6)	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L47	72	L46 not L45	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L48	402	711/170-172.ccls. and ((configur$5).ti. (configur$6).ab.)	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L49	16	711/170-172.ccls. and ((configur$5).ti. (configur$6).ab.) and prefetch	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L50	90	711/170-172.ccls. and ((configur$5).ti. (configur$6).ab.) and bandwidth	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L51	6	711/170-172.ccls. and ((configur$5).ti. (configur$6).ab.) and vhdl	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L52	39	711/170-172.ccls. and ((configur$5).ti. (configur$6).ab.) and matrix	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L53	13	711/170-172.ccls. and ((configur$5).ti. (configur$6).ab.) and parallelism	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L54	1	"6553477".pn.	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L55	3	711/170-173.ccls. and reconfigurable adj processor	US-PGPUB; USPAT; JPO	OR	ON	2005/07/06 13:54
L56	9	("20030046530" | "5737524" | "5872919" | "5915104" | "5953512" | "6000014" | "6104415" | "6216219" | "6339819").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2005/07/06 13:54
L57	264	reconfigurable adj processor	US-PGPUB; USPAT; JPO	OR	ON	2005/07/06 13:54
L58	589	reconfigurable adj2 processor	US-PGPUB; USPAT; JPO	OR	ON	2005/07/06 13:54
L59	325	L58 not L57	US-PGPUB; USPAT; JPO	OR	ON	2005/07/06 13:54

L60	113	L58 and ("711" "713").clas.	US-PGPUB; USPAT; JPO	OR	ON	2005/07/06 13:54
L61	8	(adaptive adj processor) and ("711" "713").clas.	US-PGPUB; USPAT; JPO	OR	ON	2005/07/06 13:54
L62	4	L61 not L60	US-PGPUB; USPAT; JPO	OR	ON	2005/07/06 13:54
L63	0	"008128".pa.	US-PGPUB; USPAT; JPO	OR	ON	2005/07/06 13:54
L64	6	"008128".ap.	US-PGPUB; USPAT; JPO	OR	ON	2005/07/06 13:54
L65	37	src adj computers	US-PGPUB; USPAT; JPO	OR	ON	2005/07/06 13:54
L66	7	711/117.ccls. and reconfigurable near3 (memory cache RAM random adj access adj memory processor)	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L67	15	711/118.ccls. and reconfigurable near3 (memory cache RAM random adj access adj memory processor)	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L68	4	"859051".ap.	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L69	1	"6678790".pn.	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L70	2	"021492".ap.	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L71	1	"6563746".pn.	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L72	2	("6574682" "5860111").pn.	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L73	4	("6026402" "6633515").pn. "20030169283" "20030136846"	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
L74	2	"20030208658" "20030194458"	US-PGPUB; USPAT	OR	ON	2005/07/06 13:54
S63	15	711/118.ccls. and reconfigurable near3 (memory cache RAM random adj access adj memory processor)	US-PGPUB; USPAT	OR	ON	2005/01/03 13:19
S64	6	711/117.ccls. and reconfigurable near3 (memory cache RAM random adj access adj memory processor)	US-PGPUB; USPAT	OR	ON	2005/01/03 11:58

S65	4	"859051".ap.	US-PGPUB; USPAT	OR	ON	2005/01/03 12:06
S66	1	"6678790".pn.	US-PGPUB; USPAT	OR	ON	2005/01/03 12:29
S67	2	"021492".ap.	US-PGPUB; USPAT	OR	ON	2005/01/10 07:41
S68	1	"6563746".pn.	US-PGPUB; USPAT	OR	ON	2005/07/05 17:20
S69	2	("6574682" "5860111").pn.	US-PGPUB; USPAT	OR	ON	2005/07/05 17:21
S70	4	("6026402" "6633515").pn. "20030169283" "20030136846"	US-PGPUB; USPAT	OR	ON	2005/07/05 17:22
S71	2	"20030208658" "20030194458"	US-PGPUB; USPAT	OR	ON	2005/07/05 17:22

PALM INTRANET

Day : Wednesday
Date: 7/6/2005
Time: 14:00:10

Inventor Name Search Result

Your Search was:

Last Name = POZNANOVIC
First Name = DANIEL

Application#	Patent#	Status	Date Filed	Title	Inventor Name 11
60479339	Not Issued	159	06/18/2003	BANDWIDTH EFFICIENCY AND UTILIZATION USING DIRECT EXECUTION LOGIC	POZNANOVIC, DANIEL
60422722	Not Issued	159	10/31/2002	GENERAL PURPOSE RECONFIGURABLE COMPUTING HARDWARE AND SOFTWARE	POZNANOVIC, DANIEL
60286979	Not Issued	159	04/30/2001	DELIVERING ACCELERATION: THE POTENTIAL FOR INCREASED HPC APPLICATION PERFORMANCE USING RECONFIGURABLE LOGIC	POZNANOVIC, DANIEL
11140718	Not Issued	020	05/31/2005	INTERFACE FOR INTEGRATING RECONFIGURABLE PROCESSORS INTO A GENERAL PURPOSE COMPUTING SYSTEM	POZNANOVIC, DANIEL
10869200	Not Issued	071	06/16/2004	SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE	POZNANOVIC, DANIEL
10285389	Not Issued	080	10/31/2002	DEBUGGING AND PERFORMANCE PROFILING USING CONTROL-DATAFLOW GRAPH REPRESENTATIONS WITH RECONFIGURABLE HARDWARE EMULATION	POZNANOVIC, DANIEL
10285299	Not Issued	092	10/31/2002	PROCESS FOR CONVERTING PROGRAMS IN HIGH-LEVEL PROGRAMMING LANGUAGES TO A UNIFIED EXECUTABLE FOR HYBRID COMPUTING PLATFORMS	POZNANOVIC, DANIEL
10285298	Not Issued	094	10/31/2002	SYSTEM AND METHOD FOR PARTITIONING CONTROL-DATAFLOW GRAPH REPRESENTATIONS	POZNANOVIC, DANIEL
10278345	Not Issued	041	10/23/2002	SYSTEM AND METHOD FOR EXPLICT COMMUNICATION OF MESSAGES BETWEEN PROCESSES RUNNING ON DIFFERENT NODES IN A CLUSTERED MULTIPROCESSOR SYSTEM	POZNANOVIC, DANIEL
10011835	Not Issued	071	12/05/2001	INTERFACE FOR INTEGRATING RECONFIGURABLE PROCESSORS INTO A GENERAL PURPOSE COMPUTING SYSTEM	POZNANOVIC, DANIEL

Inventor Search Completed: No Records to Display.

PALM INTRANET

Day : Wednesday
Date: 7/6/2005
Time: 14:00:25

Inventor Name Search Result

Your Search was:

Last Name = CALIGA
First Name = DAVID

Application#	Patent#	Status	Date Filed	Title	Inventor Name 7
60479339	Not Issued	159	06/18/2003	BANDWIDTH EFFICIENCY AND UTILIZATION USING DIRECT EXECUTION LOGIC	CALIGA, DAVID E.
60422722	Not Issued	159	10/31/2002	GENERAL PURPOSE RECONFIGURABLE COMPUTING HARDWARE AND SOFTWARE	CALIGA, DAVID E.
10869200	Not Issued	071	06/16/2004	SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE	CALIGA, DAVID E.
10285318	Not Issued	030	10/31/2002	MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR ENHANCING PARALLELISM AND PERFORMANCE OF COMPUTATIONAL FUNCTIONS	CALIGA, DAVID E.
10278345	Not Issued	041	10/23/2002	SYSTEM AND METHOD FOR EXPLICT COMMUNICATION OF MESSAGES BETWEEN PROCESSES RUNNING ON DIFFERENT NODES IN A CLUSTERED MULTIPROCESSOR SYSTEM	CALIGA, DAVID

Inventor Search Completed: No Records to Display.

Search Another: Inventor Last Name: CALIGA First Name: DAVID Search

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Day : Wednesday
Date: 7/6/2005
Time: 14:00:34

Inventor Name Search Result

Your Search was:

Last Name = HAMMES
First Name = JEFFREY

Application#	Patent#	Status	Date Filed	Title	Inventor Name 10
60479339	Not Issued	159	06/18/2003	BANDWIDTH EFFICIENCY AND UTILIZATION USING DIRECT EXECUTION LOGIC	HAMMES, JEFFREY
60422722	Not Issued	159	10/31/2002	GENERAL PURPOSE RECONFIGURABLE COMPUTING HARDWARE AND SOFTWARE	HAMMES, JEFFREY
10869200	Not Issued	071	06/16/2004	SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE	HAMMES, JEFFREY
10345082	Not Issued	030	01/14/2003	MAP COMPILER PIPELINED LOOP STRUCTURE	HAMMES, JEFFREY
10285401	Not Issued	094	10/31/2002	EFFICIENCY OF RECONFIGURABLE HARDWARE	HAMMES, JEFFREY
10285399	Not Issued	061	10/31/2002	SYSTEM AND METHOD FOR CONVERTING CONTROL FLOW GRAPH REPRESENTATIONS TO CONTROL-DATAFLOW GRAPH REPRESENTATIONS	HAMMES, JEFFREY
10285389	Not Issued	080	10/31/2002	DEBUGGING AND PERFORMANCE PROFILING USING CONTROL-DATAFLOW GRAPH REPRESENTATIONS WITH RECONFIGURABLE HARDWARE EMULATION	HAMMES, JEFFREY
10285299	Not Issued	092	10/31/2002	PROCESS FOR CONVERTING PROGRAMS IN HIGH-LEVEL PROGRAMMING LANGUAGES TO A UNIFIED EXECUTABLE FOR HYBRID COMPUTING PLATFORMS	HAMMES, JEFFREY
10285298	Not Issued	094	10/31/2002	SYSTEM AND METHOD FOR PARTITIONING CONTROL-DATAFLOW GRAPH REPRESENTATIONS	HAMMES, JEFFREY

Inventor Search Completed: No Records to Display.

Search Another: Inventor Last Name: HAMMES First Name: JEFFREY Search

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/869,200	06/16/2004	Daniel Poznanovic	SRC028	5929

25235 7590 07/12/2005

HOGAN & HARTSON LLP
ONE TABOR CENTER, SUITE 1500
1200 SEVENTEENTH ST.
DENVER, CO 80202

EXAMINER	
THOMAS, SHANE M	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/869,200	POZNANOVIC ET AL.	
	Examiner	Art Unit	
	Shane M. Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/11/05 & 6/6/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is responsive to the amendment filed 4/11/2005.

All previously outstanding objections and rejections to the Applicant's disclosure and claims not contained in this Action have been respectfully withdrawn by the Examiner hereto.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 4/11/2005 has NOT been considered by the Examiner as the Application Number field on the Form 1449 reflects application number 10/809,200.

The information disclosure statement (IDS) submitted on 6/6/2005 was filed after the mailing date of the non-final Office action on 1/14/2005. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Response to Amendment

The rejections of claims 1,3,8, and 14 have been modified to reflect the amendments to the respective claims.

Response to Arguments

Applicant's arguments filed 4/11/2005 have been fully considered but they are not persuasive.

Claims 2,3,13, and 14 remain rejected under 35 U.S.C. 112, first paragraph. While the Applicant's response on page 8 has verified the Examiner's assumption regarding the claim limitations of claims 2,3,13, and 14, no correction or amendment has been executed by the Applicant to overcome the rejection. The Applicant's specification does not disclose that a reconfigurable processor cannot have a cache nor a cache line-sized unit of contiguous data. As such the Examiner has maintained the rejections.

As per the Applicant's arguments regarding claim 1, the Applicant states on page 9 of the Response that Paulraj shows a reconfigurable cache but not a reconfigurable processor. The Examiner disagrees. While the caching system 112 (figure 6) of Paulraj is configurable (step 214, figure 5), it is also shown as being an element of CPU 110. Therefore since, the cache 112 is reconfigurable, it is justified that the processor 110, itself, is also reconfigurable as the reconfiguration of the FPGA module 112 occurs *within* the processor. As such, the CPU 110 can be construed as a --reconfigurable-- processor.

As per the Applicant's arguments regarding claim 11, the Examiner has shown in above in the discussion of claim 1 that Paulraj teaches a reconfigurable processor as claimed by the Applicant.

As per the Applicant's arguments regarding claim 17, the Examiner has shown above in the discussion of claim 1 that Paulraj teaches a reconfigurable processor as claimed by the Applicant. Further, the data prefetch unit, as defined in the rejection by the Examiner, is the

portion of the reconfiguration unit that accesses the memory; the memory stores a vector corresponding to an optimal configuration for a particular application program (¶26). Data is transferred between the memory and the data prefetch unit in a reconfigurable processor since the reconfiguration unit 106 can be part of a reconfigurable processor 100 as shown in figure 4 (¶22).

As per the Applicant's arguments regarding claim 24, the Examiner has modified the rejection to better explain how the prior art reference of Paulraj teaches the limitations of claim 24.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 2,3,13, and 14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As per claims 2 and 13, the Applicant's disclosure does not explicitly mention that the reconfigurable processors cannot have a cache. The disclosure mentions in the Background section, and specifically in paragraphs 16-17, the drawbacks of having a hard-wired cache in a system; however, the Detailed Description does not explicitly state that the reconfigurable

processor as taught by the Applicant *cannot* contain a cache. It appears to the Examiner that no specific (hard-wired) cache memory is included in the reconfigurable processor as taught in the disclosure; rather an on-board memory and user-logic can be configured based on a program (paragraph 52). Therefore, for the purposes of examination, the Examiner shall interpret the claim such that the reconfigurable processor of claim 1 does not contain a *hard-wired* (specific) cache.

As per claims 3 and 14, it follows from the rejection for claims 2 and 13, that since Applicant's disclosure does not explicitly state that a reconfigurable processor *cannot* have a cache, the disclose further does not explicitly teach that the reconfigurable processor cannot have a cache line-sized unit of contiguous data. For the purposes of examination and based on the discussion of claim 2 above, the Examiner shall interpret the limitation of claim 3 such that the reconfigurable processor of claim 1 does not have a *hard-wired* (specific) cache line-sized unit of contiguous data being retrieved from the second memory.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Paulraj (U.S. Patent Application Publication No. 2003/0084244).

As per claim 1, Paulraj shows a reconfigurable processor in figure 6 and a first memory (L1) having a first characteristc memory utilization and a second memory (L2) having a second characteristic memory utilization. It is well known in the art that L1 caches have a higher utilziation rate than a lower-level cache such as L2. Paulraj teaches in ¶1 that upon a command from a processor, a search for the requested data is begines with the highest level cache (L1) and [if a miss occurs] continues next to the next level cache (L2). Thus it is inherent that the memory utilziation characteristc of the L1 cache of the reconfigurable processor 110 in figure 6 is greater than the memory utilziation characteristic of the L2 cache (and likewise for the L3 cache) as the L2 cache would only be utilzied when a miss to the L1 cache occurred. In other words, the reconfigurable processor *always* utilizes the L1 cache for a memory access and the *only* utilzies the L2 cache for requested data when the data is not in the L1 cache. Therefore, the cache utilziation characteristics of the --first memory-- and the --second memory-- are different.

Paulraj further teaches a functional unit 102 that executes applications using the memories L1 and L2 (paragraph 9). As is known in the art, a cache memory controller is often used to access and move data between a memory hierarchy. The Examiner is considering a data prefetch unit to be the logic assocatied with the moving, and only the moving, of data between the first and second memories (L1 and L2) since Paulraj shows a connection between the levels of cache in figure 6. This logic as well as the first and second memory types (L1 and L2) are configued by a program – refer to paragraphs 23-24. The data prefetch unit as defined by the Examiner must be configued as well by the program when moving data since the cache line size and blocking factor can change, so different amounts of data can be exchanged for the same access when different programs run.

As per claims 2 and 13, as taught in paragraphs 23 and 29 of Paulraj, no specific cache is present in the system of Paulraj. Rather, an FPGA is utilized as representing a caching hierarchy and is optimized based on the memory needs of a specific program running on the reconfigurable processor.

As per claims 3 and 14, Paulraj teaches in paragraph 23 that a specific [cache] line size of contiguous data is not retrieved since the data line size is optimized based on the memory needs of the program when executing on the reconfigurable processor. Refer also to paragraph 29. Further, it is therefore inherent that the second memory have a charactersitic line size since Paulraj teaches in ¶¶22-23 that a best line size for the memory arrangement for a particular program is determined and utilzied when that program is run. For example, a line-size characteristic would be ultized when transferring data from the L2 cache to the L1 cache.

As per claim 4, Paulraj teaches that a load/store unit is used to access the caches (L1-L3) in order to determine if cache data is present in the cache hierarchy (paragraph 6). Since the functional unit 102 (figure 6) is responsible for accessing the programmable memory unit 104, the Examiner is therefore considering the load/store unit logic of the programmable memory unit that is responsible for for accessing the L1 and L2 caches (first and second memory types) to be a memory controller. It can be seen that the memory controller, as defined by the Examiner, controls the transfer of data between the memory (assuming second memory L2) and the data prefetch unit, since the memory controller (load/store unit logic) is responsible for retrieving the data from the cache if a hit occurs (paragraph 4).

As per claim 5, as taught in paragraph 1, an external memory (element 18, figure 1) is generaly coupled to a microprocessor and holds data to be used by the microcontroller during program execution. The Examiner is considering the process of writing data back to the external memory from the FPGA memory 104 containing the caches (on-board memory), such as during a write-back scheme as known in the art, to be performed by the data prefetch unit portion of the functional logic as defined above by the Examiner. The data prefetch logic, as defined above, is responsible for all of the transfer of data into, out of, and between the FPGA memory 104.

As per claim 6, the Examiner is regarding a --register-- in its broadest reasonable sense and it thus considering it be to be a unit of logic. Therefore, the portion of the function logic that is responsible for the movement of data (as defined above to be the data prefetch unit) is being considered by the Examiner as containing a --register-- portion of the reconfigurable processor since, for instance, the blocking factor and line size of the programmable memory 112 can change, a --register-- or portion of the reconfigurable processor must be set in order to indicate

the currnet line size and blocking factor when a given application is being run on the reconfigurable processor at a given point in time. Refer to paragraph 23.

As per claim 7, the Examiner is considering the process of --disassembling the data prefetch unit-- as modifying the data prefetch unit logic of the fucntion logic 102 every time the program being executed by the reconfigurable processor changes. It can be seen that the data prefetch unit changes during these intervals since the cache line size, blocking factor, and associativity of the FPGA changes when optimal for the next program to be executed (refer to paragraph 23). Thus it can be seen that the data prefetch unit logic is --disassembled-- when another program is executed by the reconfigurable processor of Paulraj.

As per claim 8, as can be seen that the FPGA memory 112, that comprises the first and second memories (L1 and L2) and which is accessed by the data prefetch unit of the functional unit 102 as discussed above, is a --processor memory-- (part of cpu 110). It can also be seen that the --second memory-- (L2) is also a --processor memory-- since it is contained within reconfigurable processor 110. Therefore, since the data pretech unit can access the L2 cache as discussed above in the rejection of claim 1, the data prefetch unit can retrive data from the L2 portion of --processor memory--112.

As per claim 9, as shown in figure 1 and taught in paragraph 1 of Paulraj, the system 10 is actually a microprocessor, which contains a memory controller 14. The main difference between the prior art of figure 1 and the invention of Paulraj in figure 6 is that the memroy hierarchy is configurable and accessed by a fucntional unit in lieu of a separate memory controller logic (paragraph 9). Therefore, since the memory controller logic for accessing the

cache hierarchy is still contained within cpu 110 of figure 6, it can be seen that the cpu 110 is actually a microprocessor. It follows that the --processor memory-- 112 is therefore a --microprocessor memory--.

As per claim 10, since the cpu 110 of figure 6 is a reconfigurable processer (able to reconfigure its memory heirarchy to match the needs of the application it is currently running), it can be seen that the cpu memory 112 is a reconfigurable processor memory.

As per claim 11, Paulraj depicts a reconfigurable hardware system in figure 6. Paulraj further teaches in paragraph 26 that when a particular application is to be run by the reconfigrable processor 110, a configuration vector is retrieved to program the programmable memory 112 (figure 6). As shown in figure 6, the step of accesing the configuration vector is executed outside of the reconfigurable processor 110. Therefore, the Examiner is considering the memory that contains the configuration vectors to be a--common memory-- and a data prefetch unit (reconfiguration unit 106 executing on the reconfigurable processor 110) accessing the common memory in order to determine how to program the memory 112 (paragraph 29). The data prefetch unit 106 is --configured-- by an application to be excuted on the sysem 110 since when a new application is to be executed, the data prefetch unit is called upon (or configured) to access the configuration vector for the particular application.

As per claim 12, the Examiner is considering a --memory controller-- to be the system portion utilized when creating a new configuration vector for an application. Such a process occurs in figure 5 and taught in paragraghs 23-25 of Paulraj. When a new configuration vector is created by analizing performance information that has been collected for the application. The Examiner is thereby considering the --memory controller-- to be the element of the

reconfigurable hardware system that is associated with storing the new configuration vector into the common memory so that the vector can be accessed later when the same application is run again.

As per claim 15, the Examiner is considering the reconfiguration module 106 of the reconfigurable processsor 110, as comprising two distinct elements: a --computational unit-- and a --data access unit--. The data access unit is the element that is responsible for accessing the configuration vector as taught in paragraph 29 of Paulraj; or in other words, the Examiner is considering the --data access unit-- to be the same as the --memory controler-- defined in the rejection of claim 12. The Examiner is further considering the --computational unit-- of the rconfiguration module 106 to be the element that sets up the programmable memory module 104 using the configuration vector that was accessed by the --data access unit-- (paragraph 29).

As per claim 16, as taught by Paulraj in paragraph 29, the --data access unit-- supplies the configuration vector to the --computational unit-- in order to set up the programmable memory 104 as required by the application to be run on the reconfurable processor 110.

As per claim 17, the Examiner is considering a --data prefetch unit-- to be the reconfiguration unit 106 of reconfigurable processor 110 (figure 6). As taught in paragraph 26 and 29 of Paulraj, the --data prefetch unit-- accesses a memory in order to determine if a configuration vector is known for a given application, and if so, the vector is retrieved (from the memory). If this --data-- (configuration vector) is not known then a simulation is performed with the application in order to collect performance information. The Examiner is considering the element that executes and collects the performance data as being a --computational unit-- and the element of Paulraj that stores the configuration vector, once determined, to be a --data access

unit-- since it stores the vector into the --memory-- from which it can be later retrieved (step 212 of figure 5). The --computational unit--, --data access unit--, and the --data prefetch unit-- are all --configured-- by a program (application) since (1) a new application configures the computational unit portion of the reconfiguration unit to perform a simulation in order to determine the optimal memory hierarchy organization; (2) the new application configures the --data access unit-- to store and retrieve (step 212) the configuration vector for that particular application; and (3) the --data prefetch unit-- is configured by the application to determine if a configuration file exists for the application and if so, the data prefetch unit is configured by the program the programmable memory 112 in order to optimize the programmable memory for that particular application.

As per claim 18, the --data-- (configuration vector) is transferred from the --computational unit-- to the --data access unit-- when the configuration unit has created a configuration vector (step 208 of figure 5). The --data-- is written to the memory --from-- the --data prefetch unit-- since the data prefetch unit (reconfiguration unit 106) is the element that executed the beginning of the configuration vector creation process (step 200 of figure 5). Refer to paragraph 26. Thus the Examiner is considering the data as being written --from-- the data prefetch unit.

As per claim 19, as taught in paragraph 26, if the configuration vector is known, the vector is retrieved from the memory to the data prefetch unit (reconfiguration unit 106). The data is read directly from the data prefetch unit when a request to create a configuration vector is made for a new application as shown in figure 6 since the data prefetch unit is responsible for being the vector creation process. The data is directed from the data prefetch unit (reconfigure

logic) to be read from the memory by the data access unit to the computational unit where it is processed to produce a configuration vector.

As per claim 20, as stated above, the configuration vector (--data--) is created by the computational unit via acquired simulation data. The configuration vector is the resultant product that is transferred from the memory to the data prefect unit when it is determined that the configuration vector for the application is available (paragraph 26). Thus --all-- of the data that is transferred is processed by the computational unit (albeit before the transfer occurs) since the data prefetch unit required the entire configuration vector in order to set up the programmable memory 112.

As per claim 21, Paulraj shows in paragraph 26 that an explicit request for the configuration vector for the current application results in the data (if it exists) selected for the optimal configuration of the programmable memory 112 for that application.

As per claim 22, the Examiner is not considering the data (configuration vector) to be the size of a complete cache line since the data is used to create a cache hierarchy. In other words, the caches (L1-L3) of the programmable memory 112 are not programmed when the data is transferred from the memory to the data prefetch unit; therefore, the data cannot be a complete cache line.

As per claim 23, since the Examiner defined the portion of the reconfiguration unit that accesses the configuration file (data) from the memory, the Examiner is defining the logic that controls the actual transfer of that data to the data prefetch unit (portion of the reconfiguration unit that executes the fetch of the configuration vector and then programs the programmable memory 112) to be a --memory controller--. Thus the data access unit determines whether a

configuration vector exists for an application and if so, the memory controller sends that data to the data prefetch unit.

As per claim 24, Paulraj shows a reconfigurable processor in figure 6 that comprises a computation unit 110 and a data access unit (elements 120 and 114, which comprise the reconfiguration unit 106 of figure 4 - ¶28). In figure 6, the data access unit can be seen as being coupled to the computational unit. The data access unit retrieves data (configuration vector) from a memory internal to the data access unit (i.e. reconfiguration unit) and supplies the data to the computation unit in the form of modifications to the cache FPGA module 112. Refer to ¶23.

The computation unit is configured by the program (application) that is to be executed on it by the run-time profile that is created and stored by the reconfiguration unit (¶22), thereby creating the optimal configuration of the different caches. The data access unit (specifically the memory portion used to store configuration profiles for the different application programs) is configured by the program that is to run on the reconfigurable processor. When a new program is to be run, [as a result] the program configures the reconfiguration unit to collect statistics regarding the memory usages (caches L1, L2, and L3) of the program and a configuration vector is associated with the respective program and stored in the reconfiguration unit. Refer to ¶¶23-24. When a program is known, the program [as a result] configures the data access unit (reconfiguration unit) to retrieve the associated configuration vector and apply it to the FPGA memory of the reconfigurable processor (¶29).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Magoshi (U.S. Patent Application Publication No. 2003/0208658) teaches the memory utilization characteristics of an L1 and an L2 cache in figure 2. As shown, the L1 cache is always accessed (high memory utilization) upon an access request from a processor and the L2 cache is only accessed (lower memory utilization) when a miss occurs with respect to the L1 cache.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M. Thomas whose telephone number is (571) 272-4188. The examiner can normally be reached on M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane M. Thomas

HONG CHONG KIM
PRIMARY EXAMINER

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Application Number	10/809,200
Filing Date	June 16, 2004
First Named Inventor	Daniel Poznanovic et al.
Art Unit	2186
Examiner Name	Thomas, Shane M.
Attorney Docket No.	SRC028

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.[1]	Document No. No. – Kind Code[2]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		~~US-6,076,152~~	~~06/13/2000~~	~~Huppenthal et al.~~	
		~~US-6,247,110~~	~~06/12/2001~~	~~Huppenthal et al.~~	
		~~US-6,356,983~~	~~03/12/2002~~	~~Parks~~	
		~~US-6,594,736~~	~~06/15/2003~~	~~Parks~~	
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				Art Unit	2186
(Use as many sheets as necessary)				Examiner Name	Thomas, Shane M.
Sheet	2	of	2	Attorney Docket No.	SRC028

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Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s) publisher, city and/or country where published	T[2]
		~~DALLY, BILL, HANRAHAN, PAT, FEDKIW, RON, "A Streaming Supercomputer", September 18, 2001, pp. 1-17.~~	
		~~DALLY, WILLIAM J. et al., "Merrimac: Supercomputing with Streams", SC'03, November 15-21, 2003, Phoenix, AZ, 7 pages.~~	
		~~"Code Development and Porting Issues", SRC Computer, Inc., SRC-6E C Programming Environment v1.3 Guide, April 11, 2003, pp. 17-26.~~	

EXAMINER SIGNATURE	Shane M. Thomas	DATE CONSIDERED	7/11/05

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SMT		US-2003/0084244 A1	05/01/2003	Paulraj	Entire Document
SMT		US-2003/0046530 A1	03/06/2003	Poznanovic	
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EXAMINER SIGNATURE	Shane M. Thomas	DATE CONSIDERED	7/5/05

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Notice of References Cited	Application/Control No. 10/869,200	Applicant(s)/Patent Under Reexamination POZNANOVIC ET AL.	
	Examiner Shane M. Thomas	Art Unit 2186	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-2003/0208658	11-2003	Magoshi, Hidetaka	711/122
	B	US-			
	C	US-			
	D	US-			
	E	US-			
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Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination	
10/869,200	POZNANOVIC ET AL.	
Examiner	**Art Unit**	
Shane M. Thomas	2186	

SEARCHED			
Class	Subclass	Date	Examiner
711	170-173	7/6/2005	
712	15	7/6/2005	

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
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Updated East Search	7/6/2005	
Inventor Name Search	7/6/2005	

Index of Claims

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√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
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Claim		Date								
Final	Original	1/5/05	7/6/05							
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UNITED STATES PATENT AND TRADEMARK OFFICE

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BIBDATASHEET

Bib Data Sheet

CONFIRMATION NO. 5929

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/869,200	06/16/2004 RULE	711	2186	SRC028

APPLICANTS

Daniel Poznanovic, Colorado Springs, CO;

David E. Caliga, Colorado Springs, CO;
Jeffrey Hammes, Colorado Springs, CO;

** CONTINUING DATA **********

This appln claims benefit of 60/479,339 06/18/2003

YES SMT

** FOREIGN APPLICATIONS **********

NONE SMT

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 08/04/2004

Foreign Priority claimed ☐ yes ☒ no 35 USC 119 (a-d) conditions met ☐ yes ☐ no ☐ Met after Allowance Verified and Acknowledged _____ SMT Examiner's Signature Initials	STATE OR COUNTRY CO	SHEETS DRAWING 12	TOTAL CLAIMS 24	INDEPENDENT CLAIMS 4

ADDRESS
25235
HOGAN & HARTSON LLP
ONE TABOR CENTER, SUITE 1500
1200 SEVENTEENTH ST
DENVER , CO
80202

TITLE
System and method of enhancing efficiency and utilization of memory bandwidth in reconfigurable hardware

FILING FEE RECEIVED 928	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Certificate of Transmission under 37 CFR 1.8

Serial No. 10/869,200
Application of: Daniel Poznanovic, David E. Caliga, and Jeffrey Hammes
Filed: June 16, 2004
Art Unit: 2186
Examiner: Thomas, Shane M.
Attorney Docket No. SRC028
For: SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE
Confirmation No.:

Customer No.: **25235**

I hereby certify that this correspondence with the following documents are being facsimile transmitted to the United States Patent and Trademark Office:

1. Amendment and Response after Final (8 Pages)
2. Certificate of Transmission under 37 CFR 1.8 (1 page)

on 8/26/05
Date

9
No. of Pages
(incl. Coversheet)

to centralized fax number: 571.273.8300

J C Schubert
Signature

Joan C. Schubert
Typed or printed name of person signing Certificate

Note: Each paper must have its own certificate of transmission, or its certificate must identify each submitted paper.

Client Matter No.: 80404.0033.001

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Client Matter No. 80404.0033.001
Express Mail No.: Via Facsimile

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No. 10/869,200	Confirmation No.: 5929
Application of: Daniel Poznanovic, et al.	Customer No.: **25235**
Filed: June 16, 2004	**EXPEDITED PROCEDURE UNDER 37 C.F.R. 1.116**
Art Unit: 2186	
Examiner: Thomas, Shane M.	
Attorney Docket No. SRC028	
For: SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE	

AMENDMENT AND RESPONSE PURSUANT TO OFFICE ACTION DATED JULY 12, 2005

MAIL STOP AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the office communication mailed July 12, 2005 please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A reconfigurable processor that instantiates an algorithm as hardware comprising:

a first memory having a first characteristic memory bandwidth and/or memory utilization; and

a data prefetch unit coupled to the first memory, wherein the data prefetch unit retrieves data from a second memory of second characteristic memory bandwidth and/or memory utilization and place the retrieved data in the first memory and wherein at least the first memory and data prefetch unit are configured by a program.

2. (Cancelled)

3. (Cancelled)

4. (Previously Presented) The reconfigurable processor of claim 1, wherein the data prefetch unit is coupled to a memory controller that controls the transfer of the data between the second memory and the data prefetch unit.

5. (Previously Presented) The reconfigurable processor of claim 1, wherein the data prefetch unit receives processed data from on-processor memory and writes the processed data to an external off-processor memory.

6. (Original) The reconfigurable processor of claim 1, wherein the data prefetch unit comprises at least one register from the reconfigurable processor.

7. (Original) The reconfigurable processor of claim 1, wherein the data prefetch unit is disassembled when another program is executed on the reconfigurable processor.

8. (Previously Presented) The reconfigurable processor of claim 1 wherein said second memory comprises a processor memory and said data prefetch unit is operative to retrieve data from the processor memory.

9. (Original) The reconfigurable processor of claim 8 wherein said processor memory is a microprocessor memory.

10. (Original) The reconfigurable processor of claim 8 wherein said processor memory is a reconfigurable processor memory.

11. (Currently Amended) A reconfigurable hardware system, comprising:

a common memory; and

one or more reconfigurable processors that can instantiate an algorithm as hardware coupled to the common memory, wherein at least one of the reconfigurable processors includes a data prefetch unit to read and write data between the data prefetch unit and the common memory, and wherein the data prefetch unit is configured by a program executed on the system.

12. (Original) The reconfigurable hardware system of claim 11, comprising a memory controller coupled to the common memory and the data prefetch unit.

13. (Cancelled)

14. (Cancelled)

15. (Previously Presented) The reconfigurable hardware system of claim 11, wherein the at least one of the reconfigurable processors also includes a computational unit coupled to a data access unit.

16. (Original) The reconfigurable hardware system of claim 15, wherein the computational unit is supplied the data by the data access unit.

17. (Previously Presented) A method of transferring data comprising:

transferring data between a memory and a data prefetch unit in a reconfigurable processor; and

transferring the data between a computational unit and a data access unit, wherein the computational unit and the data access unit, and the data prefetch unit are configured by a program.

18. (Original) The method of claim 17, wherein the data is written to the memory, said method comprising:

transferring the data from the computational unit to the data access unit; and

writing the data to the memory from the data prefetch unit.

19. (Previously Presented) The method of claim 17, wherein the data is read from the memory, said method comprising:

transferring the data from the memory to the data prefetch unit; and

reading the data directly from the data prefetch unit to the computational unit through the data access unit.

20. (Original) The method of claim 19, wherein all the data transferred from the memory to the data prefetch unit is processed by the computational unit.

21. (Original) The method of claim 19, wherein the data is selected by the data prefetch unit based on an explicit request from the computational unit.

22. (Original) The method of claim 17, wherein the data transferred between the memory and the data prefetch unit is not a complete cache line.

23. (Original) The method of claim 17, wherein a memory controller coupled to the memory and the data prefetch unit, controls the transfer of the data between the memory and the data prefetch unit.

24. (Currently Amended) A reconfigurable processor comprising:

a computational unit; and

a data access unit coupled to the computational unit, wherein the data access unit retrieves data from memory and supplies the data to the computational unit, and wherein the computational unit and the data access unit are configured by a program to instantiate an algorithm as hardware.

REMARKS/ARGUMENTS

Claims 1, 4-12 and 15-24 remain in the application. Claims 2, 3, 13 and 14 are cancelled. Claims 1, 11 and 24 are amended to more distinctly describe the subject matter of the invention.

A. Rejections under 35 U.S.C. 112.

The cancellation of claims 2, 3, 13, 14 renders the rejection under 35 U.S.C. 112 moot. However, the concept of a configurable processor that does not have a cache is believed to be supported by the claims themselves, and the subject matter of these claims is not waived.

B. Rejections under 35 U.S.C. 102.

Claims 1-24 were rejected under 35 U.S.C. 102 based upon Paulraj. This rejection is respectfully traversed.

Claim 1 is amended to adopt language from the definition of "reconfigurable processor" appearing in paragraph 39 of the specification as filed. This amendment is not believed to raise any new issues nor require further search because this meaning of reconfigurable processor is consistent with the application as filed and consistent with the definition of that term asserted in prior remarks submitted on April 11, 2005.

As amended, independent claim 1 calls for a reconfigurable processor that instantiates an algorithm as hardware. Although the reference show a reconfigurable cache, Paulraj does not show or suggest a reconfigurable processor that instantiates an algorithm as hardware. Moreover, nothing in Paulraj would suggest the rather significant changes required to replace the CPU with a reconfigurable processor that can instantiate an algorithm as hardware. For at least these reasons claim 1 is not anticipated nor made obvious by Paulraj.

Claims 2-10 that depend from claim 1 are allowable over Paulraj for at least the same reasons as claim 1 as well as the limitations that are presented in those claims.

Claim 11 calls for a reconfigurable hardware system comprising one or more reconfigurable processors that can instantiate an algorithm as hardware. As noted above with respect to claim 1, Paulraj does not show or suggest even one reconfigurable processor that can instantiate an algorithm as hardware. For at least these reasons claim 11 and claims 12-16 that depend from claim 11 are believed to be allowable over Paulraj.

Independent claim 17 calls for, among other things, transferring data between a memory and a data prefetch unit in a reconfigurable processor. Paulraj does not show or suggest a data prefetch unit, nor does Paulraj suggest transferring data between a memory and a data prefetch unit in a reconfigurable processor. The cited portions of Paulraj deal with retrieving a configuration vector but do not use the work "data prefetch unit" or or describe any functional unit that operates in the same way as a data prefetch unit. Moreover, even if the broad construction set out in the Office action is applied, Paulraj does not suggest configuring the computational unit, data access unit and the data prefetch unit by a program. Paulraj simply cannot suggest this configurability because the computational unit in Paulraj is not configurable. For at least these reasons claim 17 and claims 18-23 that depend from claim 17 are allowable over Paulraj.

Claim 24 as amended is believed to clarify that the term "configured" as used in the claims refers to configuration that allows the configured device to instantiate an algorithm as hardware. Loading a software program into a general purpose computational device such as shown in Paulraj does not result in the instantiation of an algorithm as hardware. Accordingly, claim 24 is believed to be allowable over the relied on reference.

C. Conclusion.

In view of all of the above, the claims are now believed to be allowable and the case in condition for allowance which action is respectfully requested. Should the Examiner be of the opinion that a telephone conference would

expedite the prosecution of this case, the Examiner is requested to contact Applicants' attorney at the telephone number listed below.

Any fee deficiency associated with this submittal may be charged to Deposit Account No. 50-1123.

Respectfully submitted,

August 26, 2005

Stuart T. Langley, Reg. No. 33,940
Hogan & Hartson LLP
One Tabor Center
1200 17th Street, Suite 1500
Denver, Colorado 80202
(720) 406-5335 Tel
(303) 899-7333 Fax

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2003

Application or Docket Number: 10869 200

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	24	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	24 minus 20=	* 4
INDEPENDENT CLAIMS	4 minus 3 =	* 1
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	385.00	OR	BASIC FEE	770.00
XS 9=		OR	XS18=	72
X43=		OR	X86=	86
+145=		OR	+290=	—
TOTAL		OR	TOTAL	928

CLAIMS AS AMENDED - PART II

4-11-05

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 24	Minus	** 24	= —
Independent	* 4	Minus	*** 4	= 0
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
XS 9=		OR	XS18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 20	Minus	** 24	= —
Independent	* 4	Minus	*** 4	= —
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
XS 9=		OR	XS18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
XS 9=		OR	XS18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/869,200	06/16/2004	Daniel Poznanovic	SRC028	5929

25235 7590 09/01/2005

HOGAN & HARTSON LLP
ONE TABOR CENTER, SUITE 1500
1200 SEVENTEENTH ST
DENVER, CO 80202

EXAMINER	
THOMAS, SHANE M	
ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 09/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Advisory Action Before the Filing of an Appeal Brief	Application No. 10/869,200	Applicant(s) POZNANOVIC ET AL.	
	Examiner Shane M. Thomas	Art Unit 2186	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 26 August 2005 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: *See Continuation Sheet*. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1-24*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). _____
13. ☐ Other: _____.

Continuation of 3. NOTE: The amendment to the claims has changed the scope of independent claims 1,11, and 24, and as such, further search and consideration are required.

HONG CHONG KIM
PRIMARY EXAMINER

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AUG 2 6 2005

Client Matter No. 80404.0033.001
Express Mail No.: Via Facsimile

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No. 10/869,200	Confirmation No.: 5929
Application of: Daniel Poznanovic, et al.	Customer No.: **25235**
Filed: June 16, 2004	**EXPEDITED PROCEDURE UNDER 37 C.F.R. 1.116**
Art Unit: 2186	
Examiner: Thomas, Shane M.	
Attorney Docket No. SRC028	
For: SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE	

Do Not Enter.
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AMENDMENT AND RESPONSE PURSUANT TO OFFICE ACTION DATED JULY 12, 2005

MAIL STOP AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the office communication mailed July 12, 2005 please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

Index of Claims

Application No.	Applicant(s)	
10/869,200	POZNANOVIC ET AL.	
Examiner	**Art Unit**	
Shane M. Thomas	2186	

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	+	Restricted	I	Interference	O	Objected

Claim		Date								
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PTO/SB/30 (08/03)
Approved for use through 07/31/2006. OMB 0651-0031
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	10/869,200
Filing Date	June 16, 2004
First Named Inventor	Daniel Poznanovic, et al.
Group Art Unit	2186
Examiner Name	THOMAS, Shane M.
Attorney Docket Number	SRC028

This is a Request for Continued Examination (RCE) under 37 C.F.R. 1.114 of the above-identified application.

Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 C.F.R. 1.114 Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

   a. ☒ Previously submitted. If a final Office Action is outstanding, any amendments filed after the final Office Action may be considered as a submission even if this box is not checked.

      i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

      ii. ☐ Other _____

   b. ☐ Enclosed

      i. ☐ Amendment/Reply

      ii. ☐ Affidavit(s)/Declaration(s)

      iii. ☐ Information Disclosure Statement (IDS)

      iv. ☐ Other _____

2. Miscellaneous

   a. ☐ Suspension of action on the above-identified application is requested under 37 C.F.R. 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 C.F.R. 1.17(i) **required**)

   b. ☐ Other

3. Fees The RCE fee under 37 C.F.R. 1.17(e) is required by 37 C.F.R. 1.114 when the RCE is filed.

   a. ☒ The Director is hereby authorized to charge the following fees, or credit any overpayments, to Deposit Account No. 50-1123

      i. ☐ RCE fee required under 37 C.F.R 1.17(e)

      ii. ☐ Extension of time fee (37 C.F.R 1.136 and 1.17)

      iii. ☒ Other: Charge any additional fees or credit any overpayments **for this filing**

   b. ☒ Check in the amount of $790.00 enclosed

   c. ☐ Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Name (Print/Type)	Stuart T. Langley	*Registration No. (Attorney/Agent)*	33,940
Signature		*Date*	September 12, 2005

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage in an envelope addressed to: Mail Stop RCE, Commissioner For Patents, P.O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

Name (Print/Type)	Stuart T. Langley		
Signature		*Date*	September 12, 2005

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Client/Matter No. 80404.0033.001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No. 10/869,200	Art Unit: 2186
Application of: Daniel Poznanovic, et al.	Confirmation No.: 5929
Filed: June 16, 2004	Customer No.: **25235**
Examiner: THOMAS, Shane M.	
Attorney Docket No. SRC028	
For: SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE	

CERTIFICATE OF MAILING BY EXPRESS MAIL

MAIL STOP RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The undersigned hereby certifies that the following documents:

- Request for Continued Examination;
- Check in the amount of $790.00;
- Certificate of Mailing by Express Mail; and
- Return Receipt Postcard

relating to the above application, were deposited as "Express Mail", Mailing Label No. EV544475732US with the United States Postal Service, addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

9/12/05
Date

Stu Langley
Mailer

9/12/05
Date

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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2876	711/170-173.ccls.	US-PGPUB; USPAT	OR	ON	2005/10/15 14:30
L2	30	1 and reconfigurable near3 (processor multiprocessor cache CPU (processing adj unit))	US-PGPUB; USPAT	OR	ON	2005/10/15 14:31
S152	733	((configurable reconfigurable "re-configurable") adj (processor (processing adj unit) CPU microprocessor "micro-processor" cache))	US-PGPUB; USPAT	OR	ON	2005/10/15 09:38
S153	270	S152 and fpga	US-PGPUB; USPAT	OR	ON	2005/10/15 09:38
S154	11	S153 and "711".clas.	US-PGPUB; USPAT	OR	ON	2005/10/15 09:52
S155	20	direct adj execut$3 adj logic	US-PGPUB; USPAT	OR	ON	2005/10/15 09:55
S156	16	memory adj algorithm adj processor	US-PGPUB; USPAT	OR	ON	2005/10/15 11:03
S157	6	"869200".ap.	US-PGPUB; USPAT	OR	ON	2005/10/15 14:30

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/869,200	06/16/2004	Daniel Poznanovic	SRC028	5929

25235 7590 10/19/2005

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DENVER, CO 80202

EXAMINER	
THOMAS, SHANE M	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/869,200	POZNANOVIC ET AL.	
	Examiner	Art Unit	
	Shane M. Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-12 and 15-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-12 and 15-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is responsive to the amendment filed 8/26/2005. Claims 1,11, and 24. have been amended; claims 2,3,13, and 14 have been canceled. Claims 1,4-12, and 15-24 are pending.

Continued Examination Under 37 CFR 1.1 1 4

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection on 9/12/2005. Since this application is eligible for continued examination under 37 CFR 1.1 14, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/26/2005 has been entered.

All previously outstanding objections and rejections to the Applicant's disclosure and claims not contained in this Action have been respectfully withdrawn by the Examiner hereto.

Response to Amendment

The rejections of claims 1,11,17, and 24 have been modified to reflect the amendments and/or Applicant's arguments to the respective claims.

Response to Arguments

Applicant's arguments filed 8/26/2005 have been fully considered but they are not persuasive for the following reasons.

Applicant argues on page 6 of the response that the prior art reference of Paulraj "does not show or suggest a reconfigurable processor that instantiates an algorithm as hardware." The Examiner respectfully traverses. Paulraj teaches in the abstract for one, that the system described determines "an optimal configuration of memory for a particular *application*." The Applicant teaches in ¶55 of the originally filed disclosure that "any computer program [i.e. application] is a collection of algorithms." Therefore it can be seen that since the processor 100 of Paulraj can reconfigure the memory 104 based on the application (or computer program) that is to execute on the processor, that so to can the reconfigurable processor system of Paulraj "instantiate an algorithm (i.e. an application) as hardware (i.e. the FPGA module 104 that is used as a cache memory)."

As per the Applicant's arguments regarding claim 11, the Examiner has shown in above in the discussion of claim 1 that Paulraj teaches a reconfigurable processor 100, as claimed by the Applicant, that instantiates an algorithm as hardware.

As per the Applicant's arguments regarding claim 17 on page 7, the Applicant argues that the prior art reference of Paulraj "does not show or suggest a data prefetch unit, nor suggest transferring data between a memory and a data prefetch unit in a reconfigurable processor. As explained in the Examiner's previous rejection of claim 17, the Examiner is considering the reconfiguration unit 106 of Paulraj to be a --data prefetch unit-- since Paulraj teaches that the unit 106 *prefetches* a configuration vector (i.e. retrieves data from an inherent and non-shown

memory) and sets up a programmable memory module 104 (i.e. cache) *before* executing the application relating to the configuration vector (refer to ¶24 and ¶29). Figure 4 of Paulraj clearly shows the --data prefetch unit-- 106 being in a reconfigurable processor 100. Although the cited reference does not explicitly use the phrase "data prefetch unit," and may or may not perform all of the functionality of a "data prefetch unit," as discussed in the Applicants disclosure, the reconfiguration unit 106 performs the ***claimed*** *functionality* of the "data prefetch unit" as discussed above (i.e. merely transferring data between a memory in a reconfigurable processor).

Further, the Applicant argues regarding claim 17 that "Paulraj does not suggest configuring the computational unit, data access unit, and the data prefetch unit by a program. Paulraj simply cannot suggest this configurability because the computational unit in Paulraj is not configurable." The Examiner respectfully traverses. All of the computational, data access, and data prefetch units are configured by a program, as immediately discussed. As defined by the Examiner, the "computational unit" of Paulraj is being considered to be the element of the system of Paulraj that executes and collects the performance data regarding how a specific application utilizes memory in order to determine an optimal memory configuration as discusses in ¶27. Figure 5 of Paulraj shows a method for creating a configuration vector by using the --computational unit-- in steps 204-206. The Examiner is considering the inherent *program* that is being executed in order to perform the steps of figure 5 to be the *program* that configures the computational unit. Therefore, it can be seen that Paulraj *does* suggest configuring the computational unit by a program. The *program* of figure 5 *configures* the computational unit to collect data for a specific application's memory usage statistics in order to create a configuration vector that allows the system of Paulraj to optimally reconfigure the programmable memory

module 104. Thus the computational unit can be configured to collect memory usage statistics for a plurality of applications that are to be executed by the reconfigurable processor 100 of Paulraj (¶23).

The same reasoning applies to the data access and data prefetch units. The *program* that is executing the steps of figure 5 (i.e. running on the system of Paulraj that implements the method) *configures* the data access unit to retrieve/store a configuration vector (step 212) based on if a new configuration vector had to be created and further *configures* the data prefetch unit to search for a configuration vector and retrieve that vector if found (steps 200 and 212).

As per the Applicant's arguments regarding claim 24 "that loading a software program into a general purpose computational device such as shown in Paulraj does not result in the instantiation of an algorithm as hardware." The Examiner respectfully traverses. Once the software program has been loaded into the computational unit, a variety of simulations are performed and memory usage statistics are gathered by the computational unit in order to create a configuration vector as taught in ¶¶23-24. This vector allows the programmable memory module 104 of Paulraj to be reconfigured to the most optimal memory configuration for that specific software program (¶26). As discussed supra, a software program or application is a collection of "algorithms"; therefore, the configuration vector for a particular software program allows the system of Paulraj to instantiate a software program as hardware since the configuration vector represents optimal configuration of the hardware (programmable memory module 104 - element 112 of figure 6).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Paulraj (U.S. Patent Application Publication No. 2003/0084244).

As per claim 1, Paulraj shows a reconfigurable processor in figure 6 and a first memory (L1) having a first characteristc memory utilization and a second memory (L2) having a second characteristic memory utilization. It is well known in the art that L1 caches have a higher utilziation rate than a lower-level cache such as L2. Paulraj teaches in ¶1 that upon a command from a processor, a search for the requested data is begines with the highest level cache (L1) and [if a miss occurs] continues next to the next level cache (L2). Thus it is inherent that the memory utilziation characteristc of the L1 cache of the reconfigurable processor 110 in figure 6 is greater than the memory utilziation characteristic of the L2 cache (and likewise for the L3 cache) as the L2 cache would only be utilzied when a miss to the L1 cache occurred. In other words, the reconfigurable processor *always* utilizes the L1 cache for a memory access and the *only* utilzies the L2 cache for requested data when the data is not in the L1 cache. Therefore, the cache utilziation characteristics of the --first memory-- and the --second memory-- are different.

Paulraj further teaches a functional unit 102 that executes applications using the memories L1 and L2 (paragraph 9). As is known in the art, a cache memory controller is often used to access and move data between a memory hierarchy. The Examiner is considering a data prefetch unit to be the logic assocatied with the moving, and only the moving, of data between the first and second memories (L1 and L2) since Paulraj shows a connection between the levels of cache in figure 6. This logic as well as the first and second memory types (L1 and L2) are configued by a program – refer to paragraphs 23-24. The data prefetch unit as defined by the Examiner must be configued as well by the program when moving data since the cache line size and blocking factor can change, so different amounts of data can be exchanged for the same access when different programs run.

The reconfigurable processor of Paulraj has the ability to collect memory usage statistics for a particular application and based on those statistics, create a configuration vector as taught in ¶¶23-24. This vector allows the programmable memory module 104 of Paulraj to be reconfigured to the most optimal memory configuration for that specific software program (¶26). As defined by the Applicant in ¶55 of the originally filed specification, a software program or application is a collection of "algorithms"; therefore, the configuration vector for a particular software program allows the system of Paulraj to instantiate a software program as hardware since the configuration vector represents optimal configuration of the hardware (programmable memory module 104 - element 112 of figure 6).

As per claims 2 and 13, as taught in paragraphs 23 and 29 of Paulraj, no specific cache is present in the system of Paulraj. Rather, an FPGA is utilized as representing a caching hierarchy