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Paper 53
Entered: March 1, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION and XILINX, INC.,[1]
Petitioner,

v.

FG SRC LLC,
Patent Owner.

IPR2020-01449
Patent 7,149,867 B2

Before KALYAN K. DESHPANDE, GREGG I. ANDERSON, and KARA L. SZPONDOWSKI, *Administrative Patent Judges*.

SZPONDOWSKI, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
Denying Patent Owner's Motion to Amend
35 U.S.C. § 318(a)

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[1] Xilinx, Inc. filed a motion for joinder and a petition in IPR2021-00633, which were granted, and, therefore, Xilinx, Inc. has been joined as petitioner in this proceeding.

I. INTRODUCTION

We instituted an *inter partes* review of claims 1–19 of U.S. Patent 7,149,867 B2 (Ex. 1001, "the '867 patent"), in response to a Petition (Paper 1, "Pet") filed by Intel Corporation ("Petitioner"). Paper 13 ("Dec."). During the trial, FG SRC LLC ("Patent Owner") filed a Response (Paper 34, "PO Resp."), Petitioner filed a Reply (Paper 40, "Reply"), and Patent Owner filed a Sur-reply (Paper 44, "Sur-reply").

Patent Owner also filed a Motion to Amend the claims of the '867 patent. Paper 26. After considering Petitioner's Opposition to the Motion to Amend (Paper 36), we issued Preliminary Guidance on Patent Owner's Motion (Paper 38). Patent Owner subsequently filed a Revised Motion to Amend the claims of the '867 patent that includes proposed substitute claims 20–38. Paper 41 ("Mot. Amend"). Petitioner opposed Patent Owner's Revised Motion to Amend (Paper 45, "Opp. Amend"), Patent Owner replied (Paper 49, "Reply Amend"), and Petitioner filed a Sur-reply (Paper 50, "Sur-reply Amend").

An oral hearing was held on January 6, 2022, and a copy of the transcript was entered into the record. Paper 52 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6. This Decision is a Final Written Decision under 35 U.S.C. § 318(a) as to the patentability of the claims on which we instituted trial. Based on the complete record, Petitioner has shown, by a preponderance of the evidence, that claims 1–19 of the '867 patent are unpatentable. We also deny Patent Owner's Revised Motion to Amend, because Patent Owner has not met its burden in asserting that proposed substitute claims 20–38 have written description support in the original application that issued as the '867 patent.

II. BACKGROUND

A. Real Parties in Interest

Petitioner identifies Intel Corporation as the sole real party in interest. Pet. 2. Patent Owner identifies FG SRC LLC as the sole real party in interest. Paper 4, 2.

B. Related Matters

The parties advise that the '867 patent is the subject of the following district court litigations:

FG SRC LLC v. Intel Corporation, 6:20-cv-00315-ADA (W.D. Tex.), filed April 24, 2020 ("the co-pending district court litigation");

FG SRC LLC v. Xilinx, Inc., 1:20-cv-00601-LPS (D. Del.), filed April 30, 2020; and

SRC Labs, LLC et al. v. Amazon Web Services, Inc., et al., 2:18-cv-00317-JLR (W.D. Wash.), filed February 26, 2018.

Pet. 2; Paper 4, 2. Petitioner also advises that the '867 patent was the subject of IPR2019-00103 (institution denied on May 10, 2019). Pet. 2.

C. The '867 Patent (Ex. 1001)

The '867 patent issued from Application No. 10/869,200 filed June 16, 2004, and claims the benefit of Provisional Application No. 60/479,339, filed June 18, 2003. Ex. 1001, codes (21), (22), (60). The '867 patent is titled "System and Method of Enhancing Efficiency and Utilization of Memory Bandwidth in Reconfigurable Hardware" and is generally directed to "enhancing the efficiency and utilization of memory bandwidth in reconfigurable hardware" and "implementing explicit memory hierarchies in reconfigurable processors that make efficient use of off-board, on-board, on-chip storage and available algorithm locality." *Id.* at code (57), 1:15–24.

According to the '867 patent, there was a growing need to develop improved memory hierarchies that limited overhead of a memory hierarchy without also reducing bandwidth efficiency and utilization. Ex. 1001, 3:57–60. The '867 patent describes a system including a memory hierarchy and a reconfigurable processor that includes a data prefetch unit. *Id.* at 4:4–10, 5:60–62, 6:9–13, 7:34–48. The '867 patent states that a "Reconfigurable Processor" is "a computing device that contains reconfigurable components such as FPGAs [(field programmable gate arrays)] and can, through reconfiguration, instantiate an algorithm as hardware." *Id.* at 5:26–29. The '867 patent states that a "Data prefetch Unit" is "a functional unit [a set of logic that performs a specific operation] that moves data between members of a memory hierarchy [a collection of memories]," where such "movement may be as simple as a copy, or as complex as an indirect indexed strided copy into a unit stride memory." *Id.* at 5:34–43.

Figure 1 of the '867 patent, reproduced below, shows a reconfigurable processor (RP) 100 of the claimed invention. *Id.* at 4:38–40.

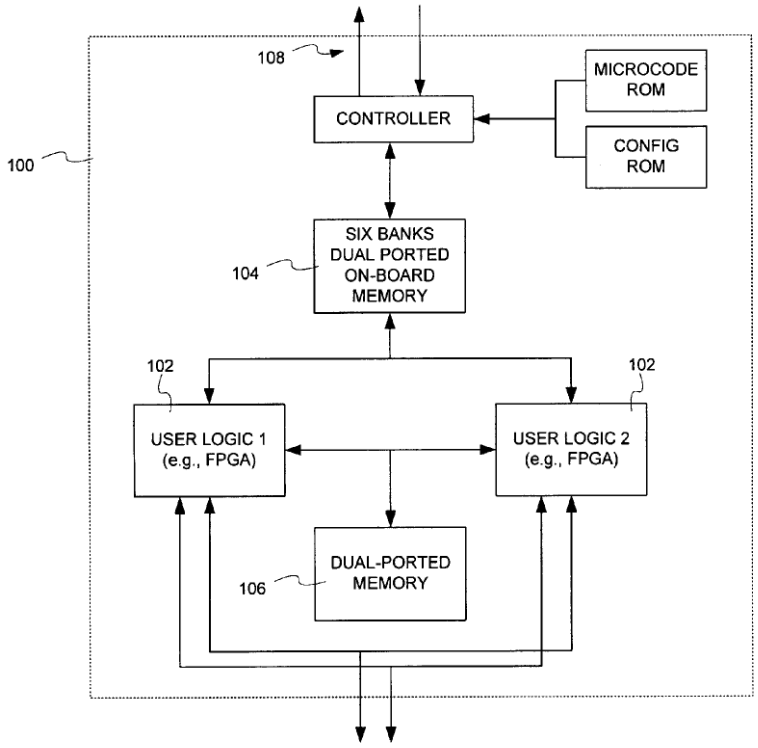

FIG. 1

Figure 1 depicts a reconfigurable processor (RP) 100. *Id.* at 4:38–40.

Figure 1 depicts reconfigurable processor 100, which "may be implemented using field programmable gate arrays (FPGAs) or other reconfigurable logic devices, that can be configured and reconfigured to contain functional units and interconnecting circuits, and a memory hierarchy comprising on-board memory banks 104, on-chip block RAM 106, registers wires, and a connection 108 to external memory." *Id.* at 6:5–11. In addition, "[o]n-chip reconfigurable components 102 create memory structures such as registers, FIFOs, wires and arrays using block RAM." *Id.* at 6:11–14. "Dual-ported memory 106 is shared between on-chip reconfigurable components 102." *Id.* at 6:14–15. "The reconfigurable processor 100 also implements user-defined computational logic . . . constructed by programming an FPGA to implement a particular interconnection of computational functional units." *Id.* at 6:15–19. "In a

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