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Salim

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(54) **PROGRAMMABLE PACKET SWITCHING
DEVICE**

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U.S.C. 154(b) by 0 days.

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(51) **Int. Cl.**⁷ **H04L 12/56**

(52) **U.S. Cl.** **370/389**; 370/401

(58) **Field of Search** 370/389, 392,
370/401, 402, 403, 404, 405

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Primary Examiner—Chau Nguyen

Assistant Examiner—D. Trinh

(57) **ABSTRACT**

A packet processing apparatus comprises a programmable
hardware discriminator for receiving incoming packets, and
selecting bits from any part of the incoming packets, a
decision table for storing information relating to how the
packets are to be processed, programmable hardware search-
ing logic for accessing the information in the table according
to the selected bits, and a packet handler for processing the
packets according to the result of the access. Since many
networking processing tasks can be broken down into bit
selection and table searching, this generic type of arrange-
ment will suit a wide variety of applications. It facilitates
developing logic directly in hardware which can reduce the
effort needed to convert a working prototype into a product
ready for use in the field, e.g. for handling new protocol
components.

1 Claim, 14 Drawing Sheets

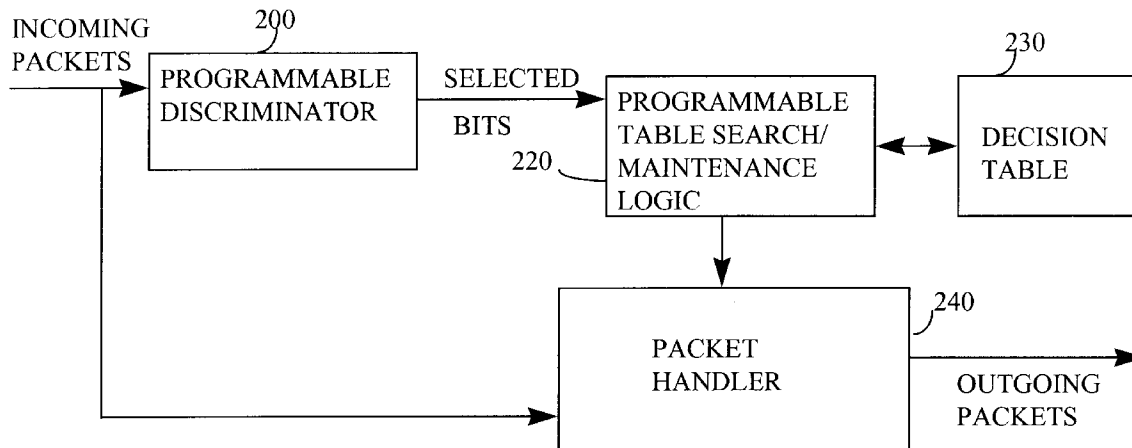


FIG. 1 PRIOR ART

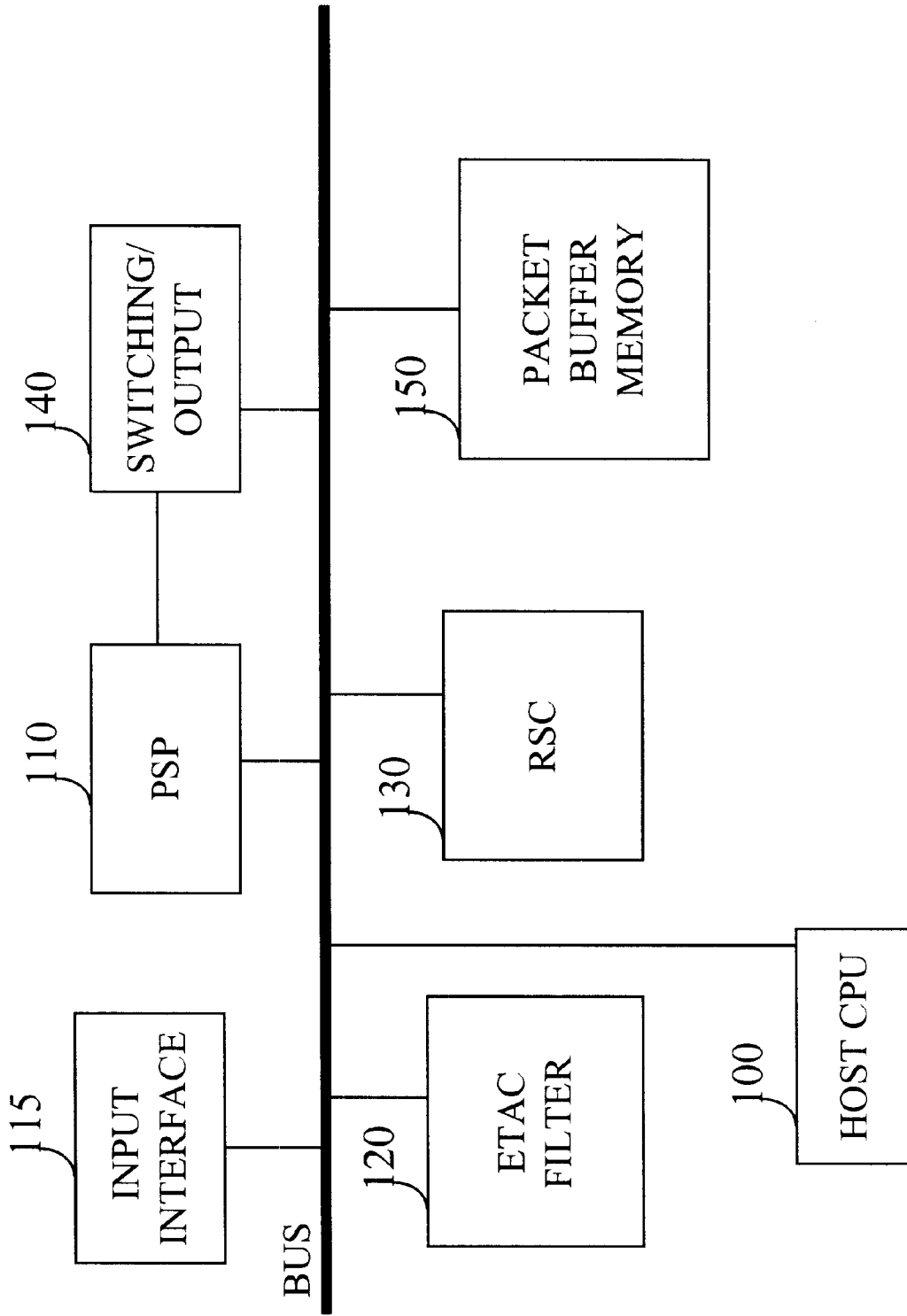
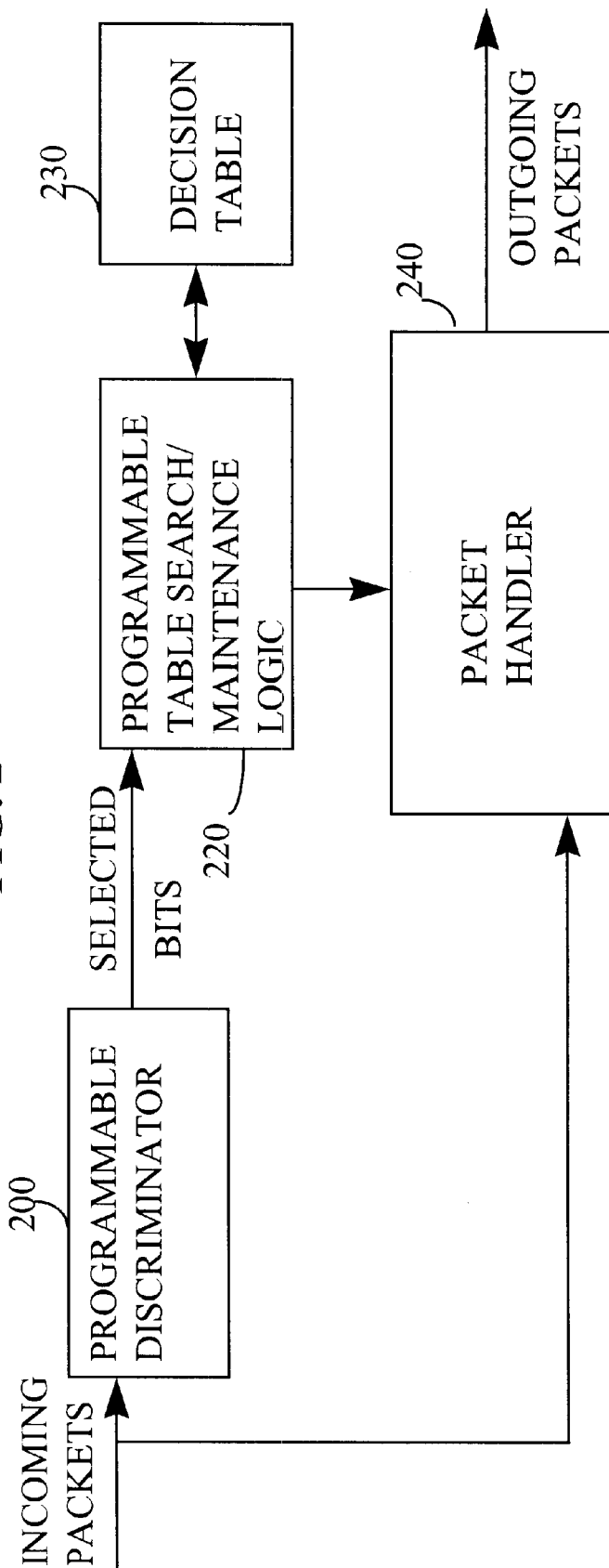


FIG. 2



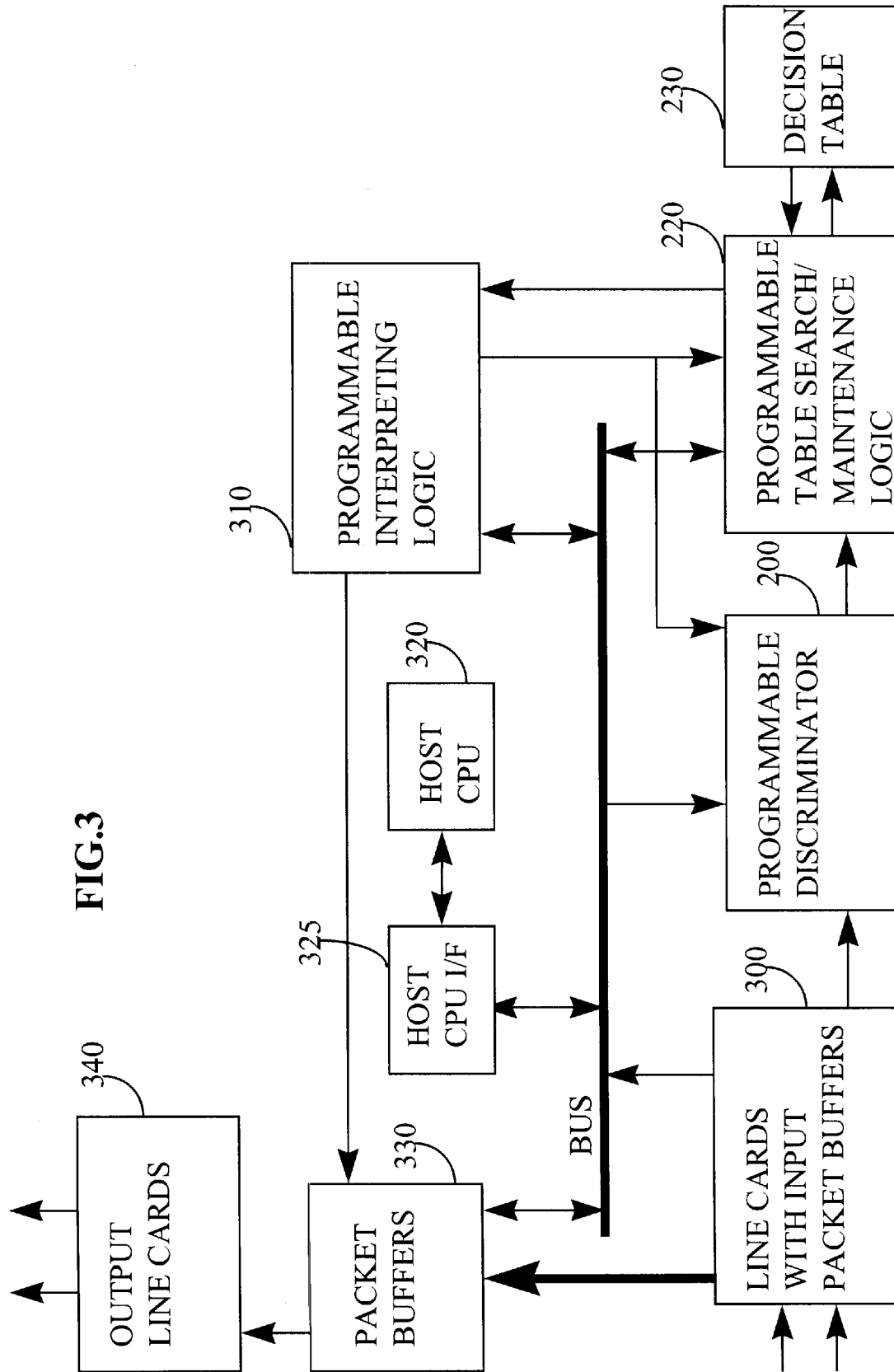
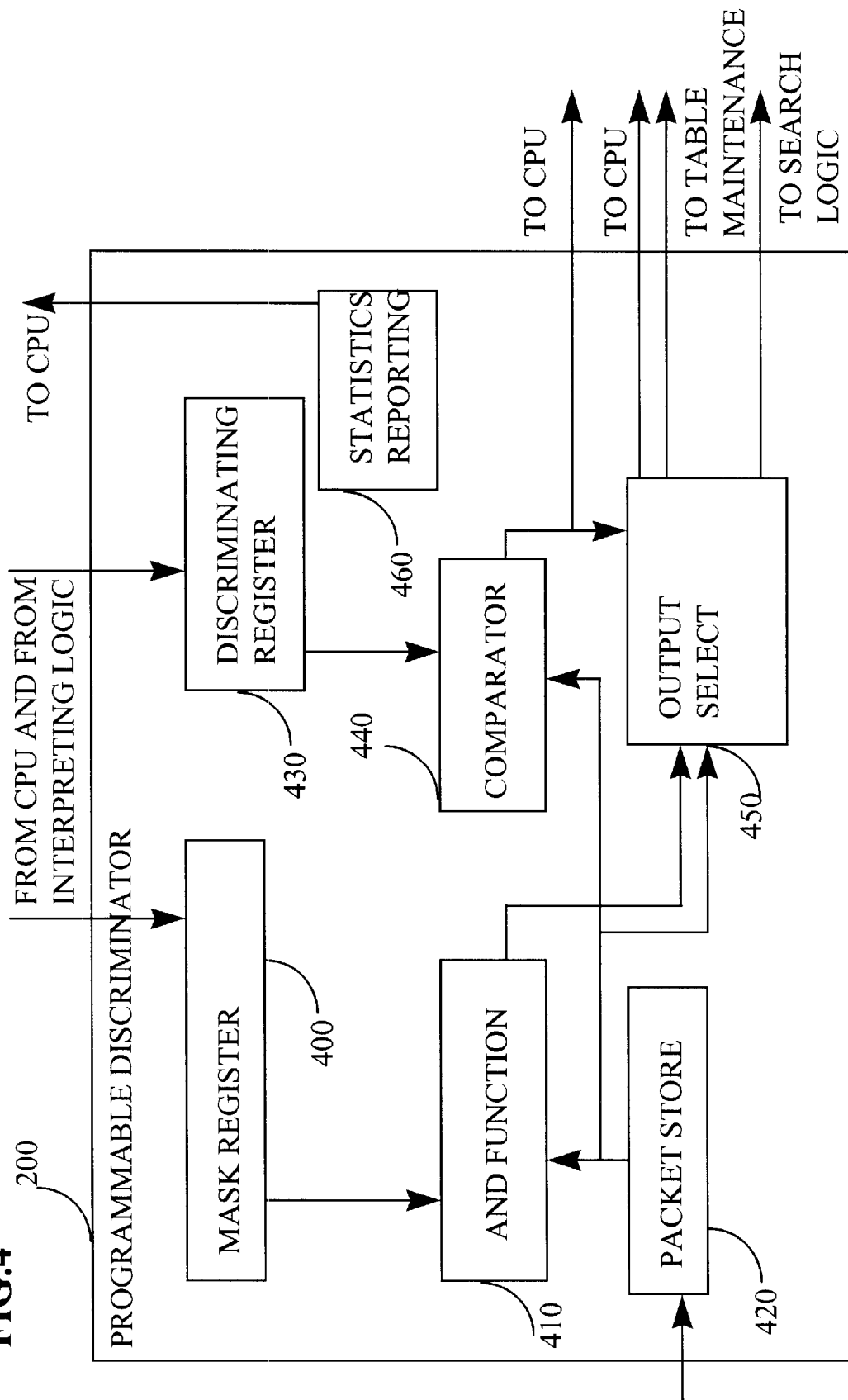


FIG. 3

FIG.4



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