

**Patent Number:** 

### US005956336A

## **United States Patent** [19]

Loschke et al.

5,956,336

**Date of Patent:** Sep. 21, 1999 [45]

[54]	APPARATUS AND METHOD FOR
	CONCURRENT SEARCH CONTENT
	ADDRESSABLE MEMORY CIRCUIT

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Wade Jones, all of Austin, Tex.

[73] Assignee: Motorola, Inc., Schaumburg, Ill.

Appl. No.: 08/722,587 [21]

[22] Filed: Sep. 27, 1996

[51] Int. Cl.<sup>6</sup> ...... H04L 12/28

**U.S. Cl.** ...... **370/392**; 370/395; 370/429 [52] [58]

370/383, 392, 393, 395, 397, 409, 416, 429; 365/49, 190, 189.12, 230.02; 395/200,

200.2, 200.21

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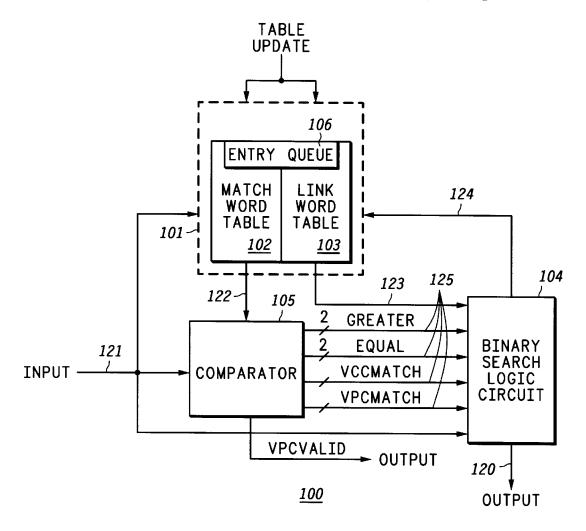
Primary Examiner—Ajit Patel Assistant Examiner—Chiho Andrew Lee Attorney, Agent, or Firm-Lee E. Chastain

**ABSTRACT** [57]

[11]

A circuit and method is provided for implementing a content addressable memory circuit (100) in which an output word is produced which corresponds to the content of a reference word containing an ATM header. According to a first aspect, a binary search logic circuit (104) binarily searches the memory array (101) to find a match word whose content is equal to that of the reference word. Output signals indicate either that a match has been found or that the binary searching of the memory array (101) should continue at addresses either above or below the location address of the match word. According to a second aspect, the content addressable memory circuit (100) performs a concurrent search of switching identifiers, virtual circuit identifiers and virtual path identifiers, to determine if a virtual path connection or virtual circuit connection exists for an ATM header.

12 Claims, 8 Drawing Sheets





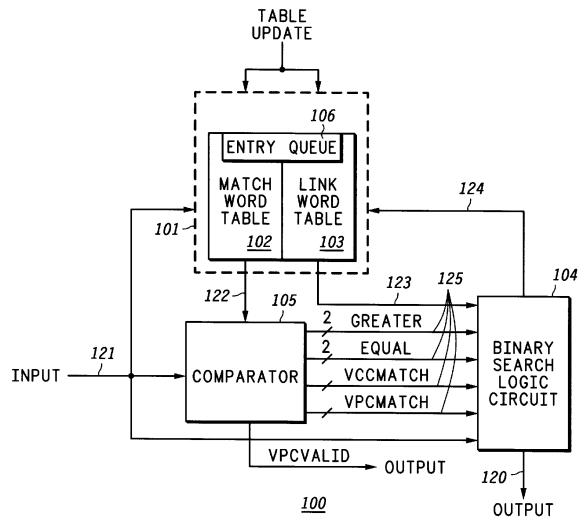


FIG.1



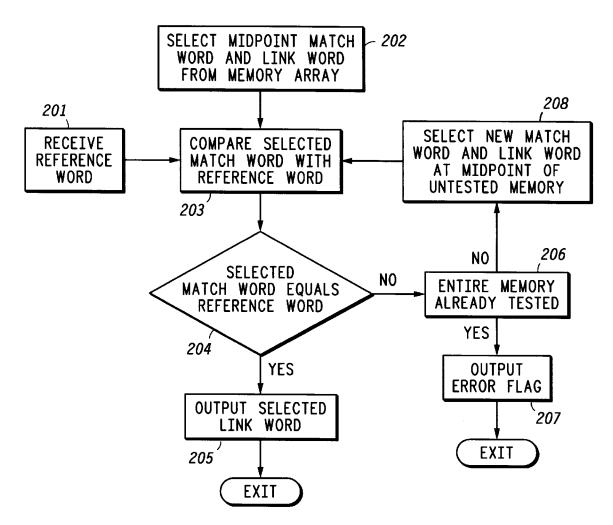


FIG.2

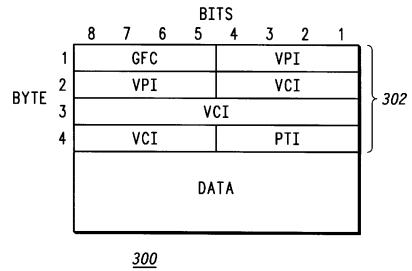


FIG.3



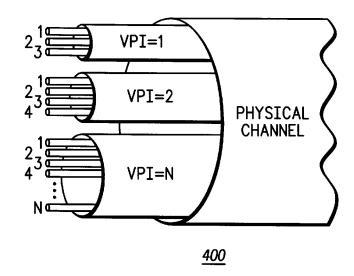


FIG.4

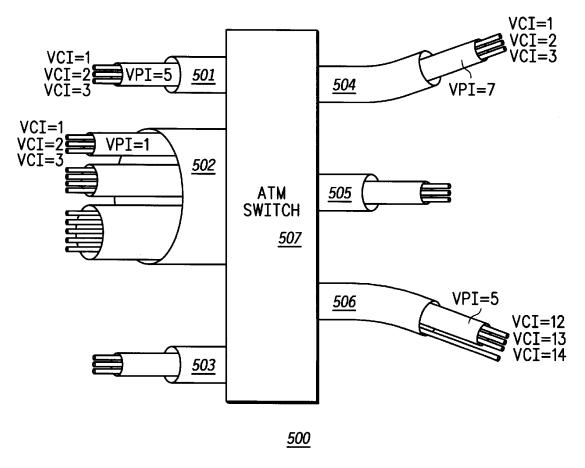


FIG.5

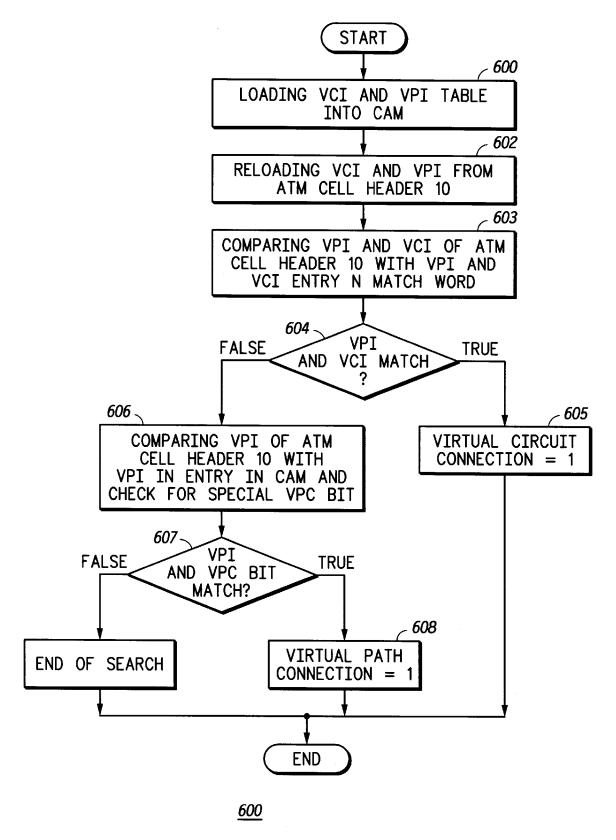


FIG.6



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