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**Howard et al.**

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(54) **APPARATUS AND METHOD FOR AWAKENING BUS CIRCUITRY FROM A LOW POWER STATE**

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(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(65) **Prior Publication Data**

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**Related U.S. Application Data**

(63) Continuation of application No. 09/340,762, filed on Jun. 28, 1999, now Pat. No. 6,460,143.

(51) **Int. Cl.**<sup>7</sup> ..... **G06F 1/26**

(52) **U.S. Cl.** ..... **713/323**

(58) **Field of Search** ..... 713/300, 310, 713/320, 323, 324, 340

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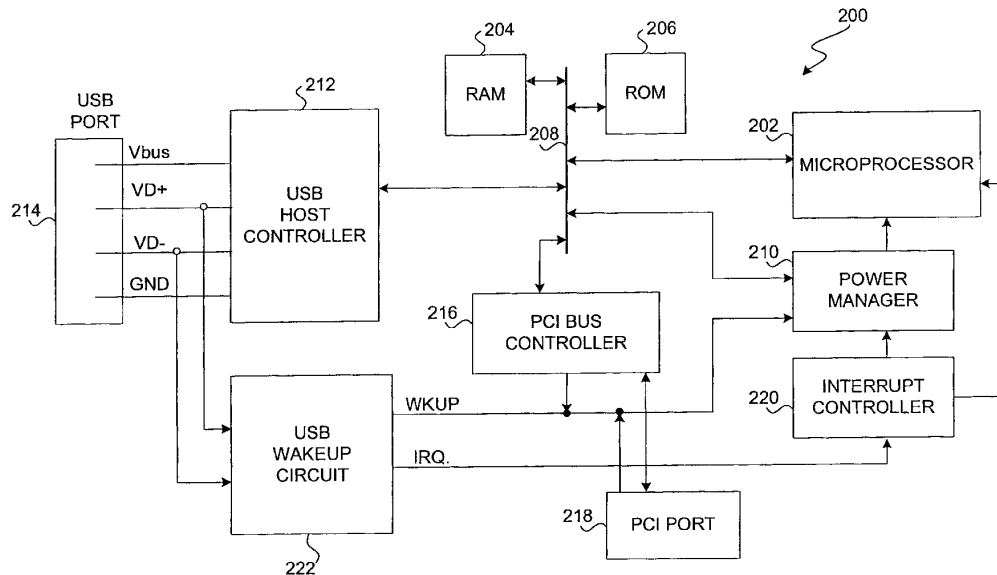
*Primary Examiner*—Glenn A. Auve

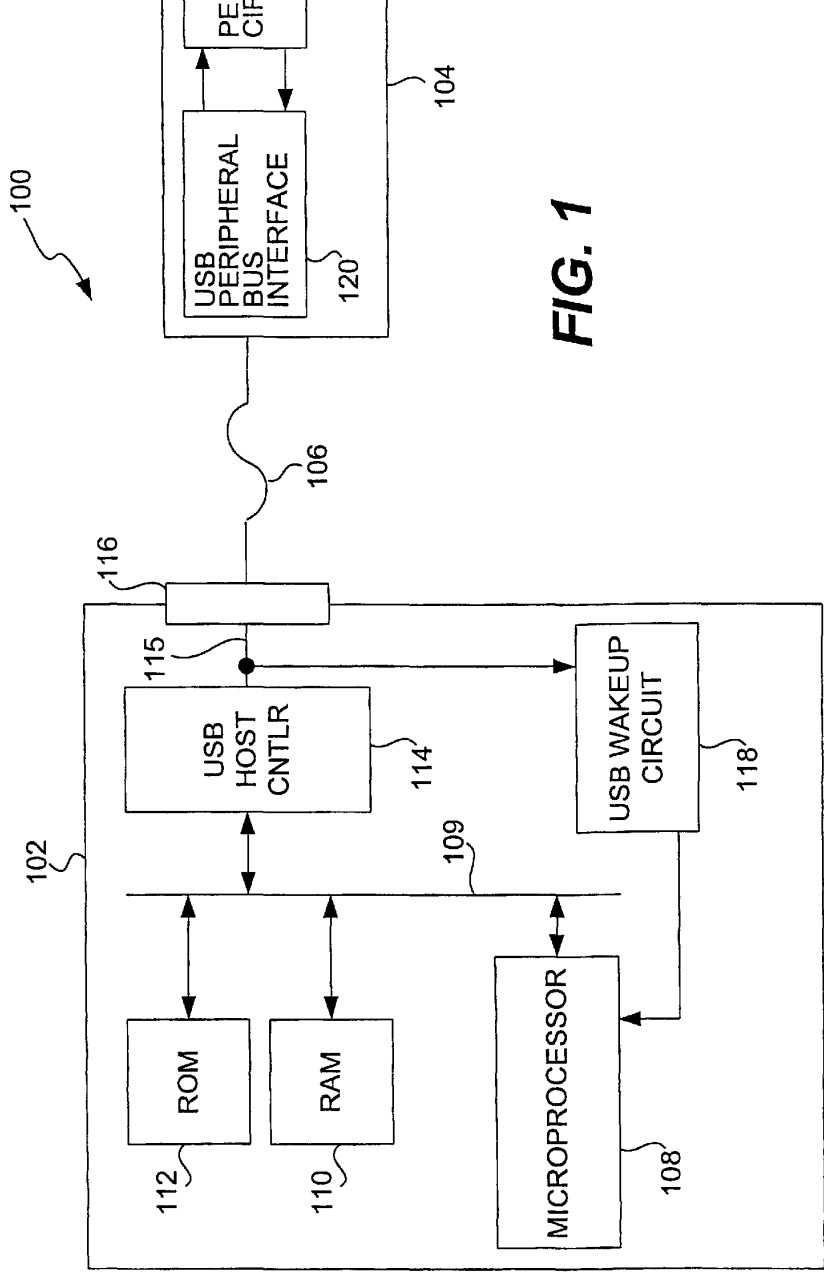
(74) *Attorney, Agent, or Firm*—Beyer Weaver & Thomas, LLP

**ABSTRACT**

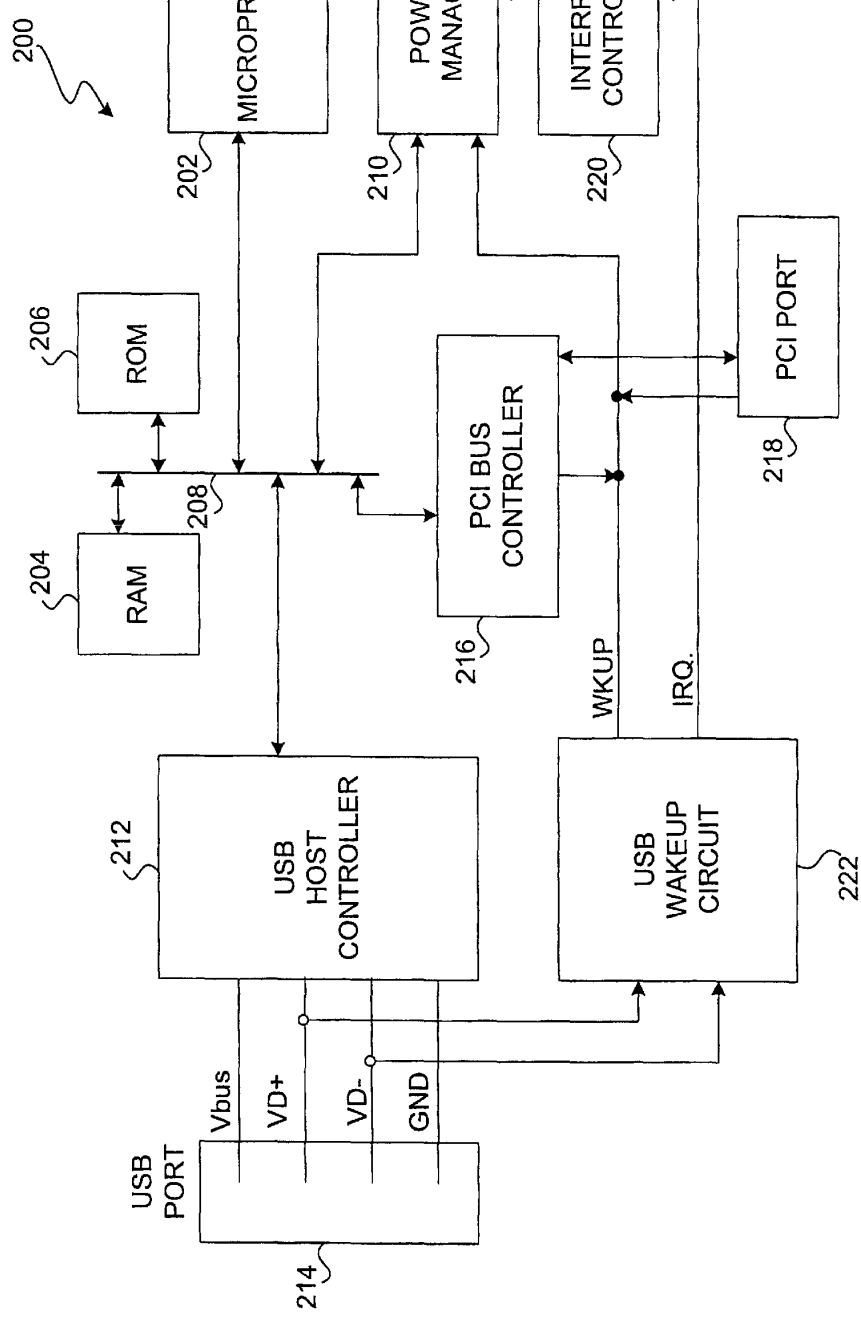
(57) Apparatus and techniques for awakening bus circuitry from an inactive state as needed are described. The bus circuitry forms part of a computer system and is placed in the inactive state (i.e., shut down) when not needed so as to conserve power. The bus circuitry is associated with a bus and can be awakened out of the inactive state when certain bus events, including resume, connect or disconnect, occur on the bus. The invention is particularly advantageous for computing devices (e.g., portable computers, desktop computers, server computers) where it is desirable to shut down bus circuitry as well as other circuitry (e.g., microprocessor) when not needed so as to reduce power consumption.

**15 Claims, 10 Drawing Sheets**

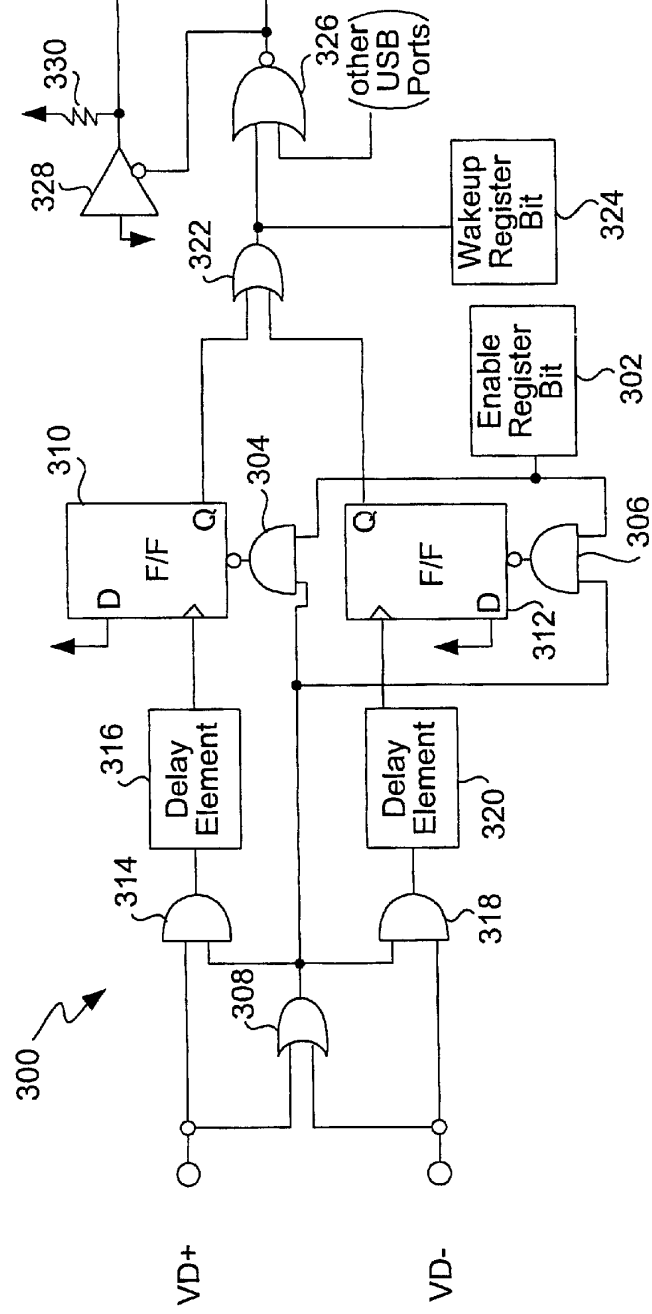




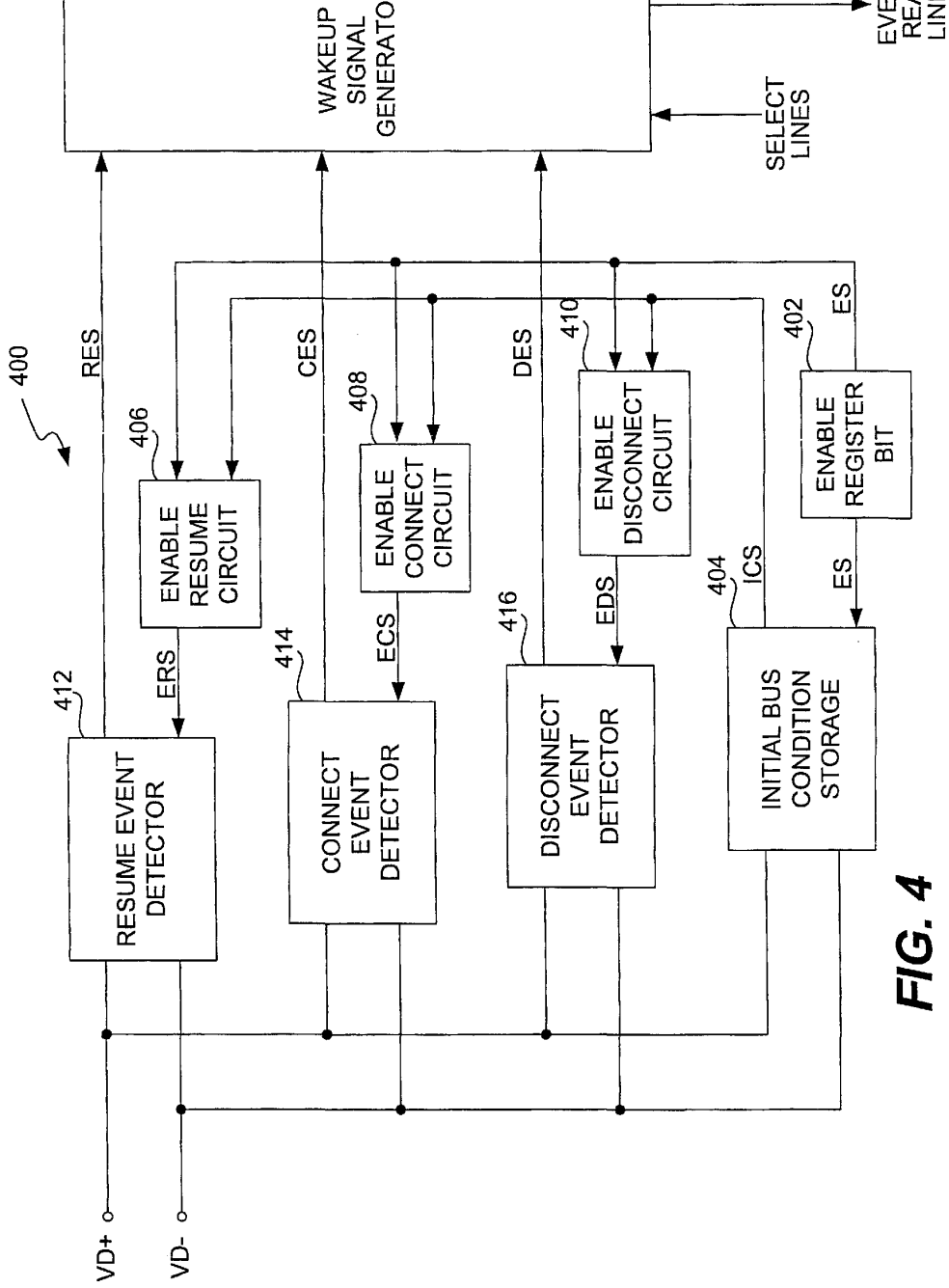
**FIG. 1**



**FIG. 2**



**FIG. 3**



**FIG. 4**

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