UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LG Electronics, Inc. and LG Electronics U.S.A., Inc.,

Petitioners,

Case No. IPR2021-00581

Patent No. 6,411,941 B1

DECLARATION OF SHAHIN NAZARIAN, PH.D., UNDER 37 C.F.R. § 1.68 IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW

I, Shahin Nazarian, Ph.D., do hereby declare as follows:

1. I am making this Declaration at the request of LG Electronics, Inc. and LG Electronics U.S.A., Inc. in the matter of the Inter Partes Review of U.S. 6,411,941 ("the '941 Patent").

2. I am being compensated for my work in this matter at my standard hourly rate. I am also being reimbursed for reasonable and customary expenses associated with my work and testimony in this proceeding. My compensation is not contingent on the outcome of this matter or the specifics of my testimony.

3. My qualifications and professional experience are described in my *Curriculum Vitae*, a copy of which is attached to my declaration as Appendix A.

4. I have reviewed the declaration of Dr. Andrew Wolfe ("Wolfe Decl." (Ex. 1003)), submitted in IPR2020-01609. I agree with Dr. Wolfe's opinions and analysis and adopt it as my own. Accordingly, it is my opinion that claims 1–3, 6–14, and 16 ("the Challenged Claims") of the '941 Patent would have been obvious to a person having ordinary skill in the art ("POSA") at the time of the alleged invention.

5. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and that these statements were made with knowledge that willful false statements

and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code.

Dated: 2/23/21

Shahin Nazarian, Ph.D.

SHAHIN NAZARIAN

(US CITIZEN)

Associate Professor of Engineering Practice

Department of Electrical Engineering, USC
3740 McClintock Ave., Los Angeles, CA 90089
shahin.nazarian@usc.edu
http://sportlab.usc.edu/~shahin/
Mobile: (626) 200-7893

EDUCATION

Ph.D., Electrical Engineering, University of Southern California, Los Angeles, CA — Major GPA: 4.0/4.0
Minor: Computer Science

MSCENG, Computer Engineering, University of Southern California — Major GPA: 4.0/4.0

M.Sc., Electrical Engineering – Electronics, University of Tehran (UT), Tehran

B.Sc., Electrical Engineering – Electronics, Tehran Polytechnic, Tehran

WORK EXPERIENCE

University of Southern California, Los Angeles, CA — 1/09 – Present
Associate Professor of Engineering Practice

- Teaching undergraduate/graduate courses in Computer/Electrical Engineering: EE590: Directed Research, EE250: Distributed Systems and Internet of Things, EE599: Special Topics – Software Design and Optimization for Electrical Engineers, EE595: Software Design and Optimization, EE580: System Verification, EE577A/B: VLSI System Design I/II, EE477: MOS VLSI Design, EE209: Foundations of Digital System Design, EE109: Introduction to Embedded Systems, EE101: Logic Design, EE450: Computer Networks, EE454: Introduction to System-on-Chip, EE357: Basic Organization of Computer Systems, EE355: Software Design for Electrical Engineers, EE352: Computer Organization and Architecture
- Advising directed research (EE590) students, currently on the topics of machine learning, verification, hardware acceleration, low power design and optimization, signal integrity analysis and optimization, green technology design, MOS VLSI/CAD, smart grid, near/sub-threshold CMOS, memory design, neuromorphic computing
- Supervising graduate students during their internship who are registered for ENGR596
- A member of the CENG Ph.D. screening exam committee: designing the written exams (for Computer Networks, EE450) and oral exams (for CAD/VLSI courses EE477L, EE577A/EE658/EE680)
- Designing the placements exams for EE450 (Computer Networks)
- Writing recommendation letters for undergraduate/graduate USC students for their industrial and academic applications, and also helping them with their resume and interview preparation
- Reviewer for IEEE Trans. on Computer Aided Design (TCAD), IEEE Trans. on Very Large Scale Integration (TVLSI), Journal of Lower Power Electronics (JOLPE), and Journal of Circuits, Systems and Signal Processing, Design and Test
- Reviewer for different conferences, including Design Automation Conf., International Conference on Computer Aided Design, and Design Automation and Test in Europe, International Symposium on Low Power Electronic and Design

Vervecode Inc., South Pasadena, CA 2/16 – Present
Founder and President
- Providing consulting and testifying expert services.
- Exploring the endless possibilities in the areas of computer science, engineering, and mathematics.

Quandary Peak Research, Beverly Hills, CA 2/15 – 8/18
Senior Research Scientist
- Working as a consulting expert on many cases related to operating systems, power management, firmware, computer architecture, wearable technologies, memory interfaces, security, GPS tracking, image processing, face recognition, SoC chips, LTE, etc.
- Providing software analysis
- Providing witness testimony

Magma Design Automation, San Jose, CA 5/06 – 1/09
Senior Member of Technical Staff
- Was involved in various projects in the Signal Integrity and Timer groups, such as multi-model multi corner timing analysis, on-chip variation consideration, as well as crosstalk delay and slew correlation issues
- Was also involved in Current Source Model (CSM)-based timing tool development and also the main person to develop the first generation of CSM noise tool in Magma. (Tcl, C++, Hspice, Purifty)

Magma Design Automation, San Jose, CA 5/04 – 8/04
R&D Design Engineer Intern
- Designed and developed new crosstalk-aware gate delay modeling techniques (Perl, C, Matlab, Hspice)
- Designed and developed methodologies to enhance the accuracy of Magma's static and statistical static timing & crosstalk noise analysis tools (Tcl, C++, Hspice)

Lucent Technologies & Bell Labs Innovations, Holmdel, NJ 6/03 – 8/03
Design Engineer (Intern) in Test Group
- Developed an IEEE P1500 (SECT - Standard for Embedded Core Test) Wrapper with parallel access for Design for Testability (DFT) verification & System-on-Chip (SoC) testing (VHDL). Evaluated IEEE1532 standard and compared it with 1149.1-based programming methods

TECHNICAL SKILLS

The following are based on my research and industrial experiences, some of which also appear in my publications and/or incorporated into the courses I teach at USC:
- Design and optimization of algorithms
- Various machine learning and deep learning algorithms and packages
- Software analysis: C/C++, Java, Perl, Python, Verilog, VHDL, SystemVerilog, SystemC, Assembly, etc.
- Software licensing, database management, live streaming
- SoC (System-on-Chip), NoC (Network-on-Chip), many-core, datacenters, server farms, IoT (Internet of Things) modeling and optimization
- Cloud computing, mobile systems
- Power (dynamic/leakage), Signal Integrity, power delivery networks, thermal analysis, cooling systems
- Memory technologies: DDR2/DDR3/DDR4 DRAM, SRAM, Flash, memristors
- Wearable technologies
- Safety, security, hardware trojans
- Interfaces including PCIe, AXI, UART, Ethernet, HDMI, I2C, and RS232
- Communications networks protocols: routing algorithms, multiplexing and channelization, including OSPF, LTE, 802.3/5/11, Bluetooth Low Energy (BLE), socket programming for client-server protocols,
- VLSI/FPGA/ASIC (spec to GDSII), CAD/EDA flows, 2D and 3D IC fabrication issues
- System verification, UVM, assertions, Formal Verification/FPV, FPGA prototyping, and AI-aware techniques
- IC technologies: CMOS, FinFETs, GAAs, superconducting/SFQ logic, memristors

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.