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Ewertz et al.

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[54] **COMPUTER SYSTEM WITH A PAGED NON-VOLATILE MEMORY**

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Related U.S. Application Data

[63] Continuation of Ser. No. 137,376, Oct. 14, 1993, Pat. No. 5,371,876, which is a continuation of Ser. No. 698,318, May 10, 1991, abandoned.

[51] **Int. Cl.**[6] **G06F 12/02**

[52] **U.S. Cl.** **395/430**; 395/479; 395/413; 395/419; 364/DIG. 1

[58] **Field of Search** ..... 364/200 MS File, 364/900 MS File; 395/400, 425

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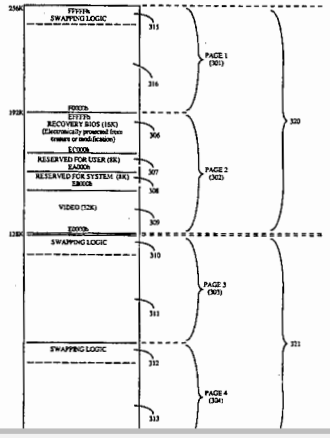
[57] **ABSTRACT**

A computer system wherein a paging technique is used to expand the useable non-volatile memory capacity beyond a fixed address space limitation. The computer system of the preferred embodiment includes a flash memory component for storing non-volatile code and data including a system BIOS in the upper 128K of memory. The useful BIOS memory space is effectively increased while maintaining the address boundary of the upper 128K region. The address space of the non-volatile memory device is logically separated into distinct pages of memory (Pages 1–4). Using the apparatus and techniques of the present invention, Page 1, Page 3 and Page 4 may be individually swapped into the address space originally occupied by Page 1 (the swappable page area). In the preferred embodiment, Page 2 is held static and thus is not used as a swap area. Each of the swappable pages, Page 1, Page 3, and Page 4, contain processing logic called swapping logic used during the swapping or paging operation. The swapping logic operates in conjunction with paging hardware to effect the swapping of pages into the swappable page area. The high order processor address lines are input by a page decoder. The page decoder is used to modify the address actually presented to the non-volatile memory device. A page register provides a means by which the processor may select a page in non-volatile memory. In an alternative embodiment of the present invention, several different forms of configuration or identification information may be stored in a page of non-volatile memory.

14 Claims, 11 Drawing Sheets



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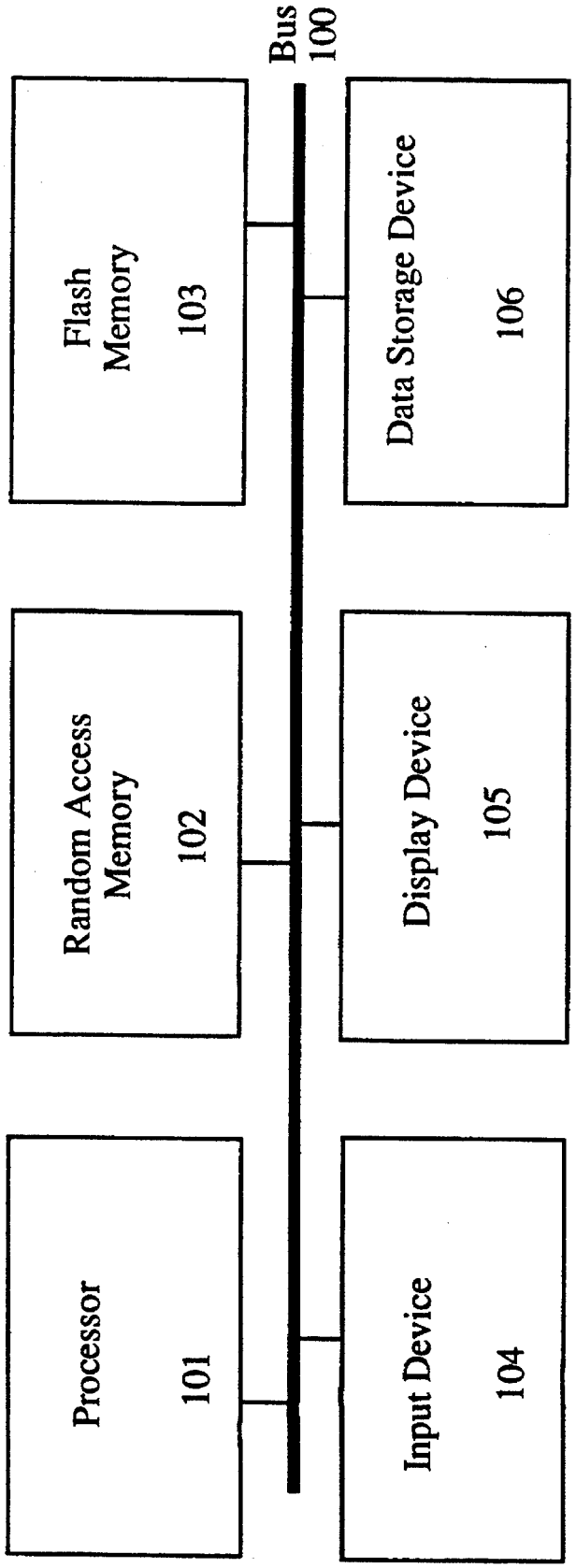

Figure 1

FIGURE 2

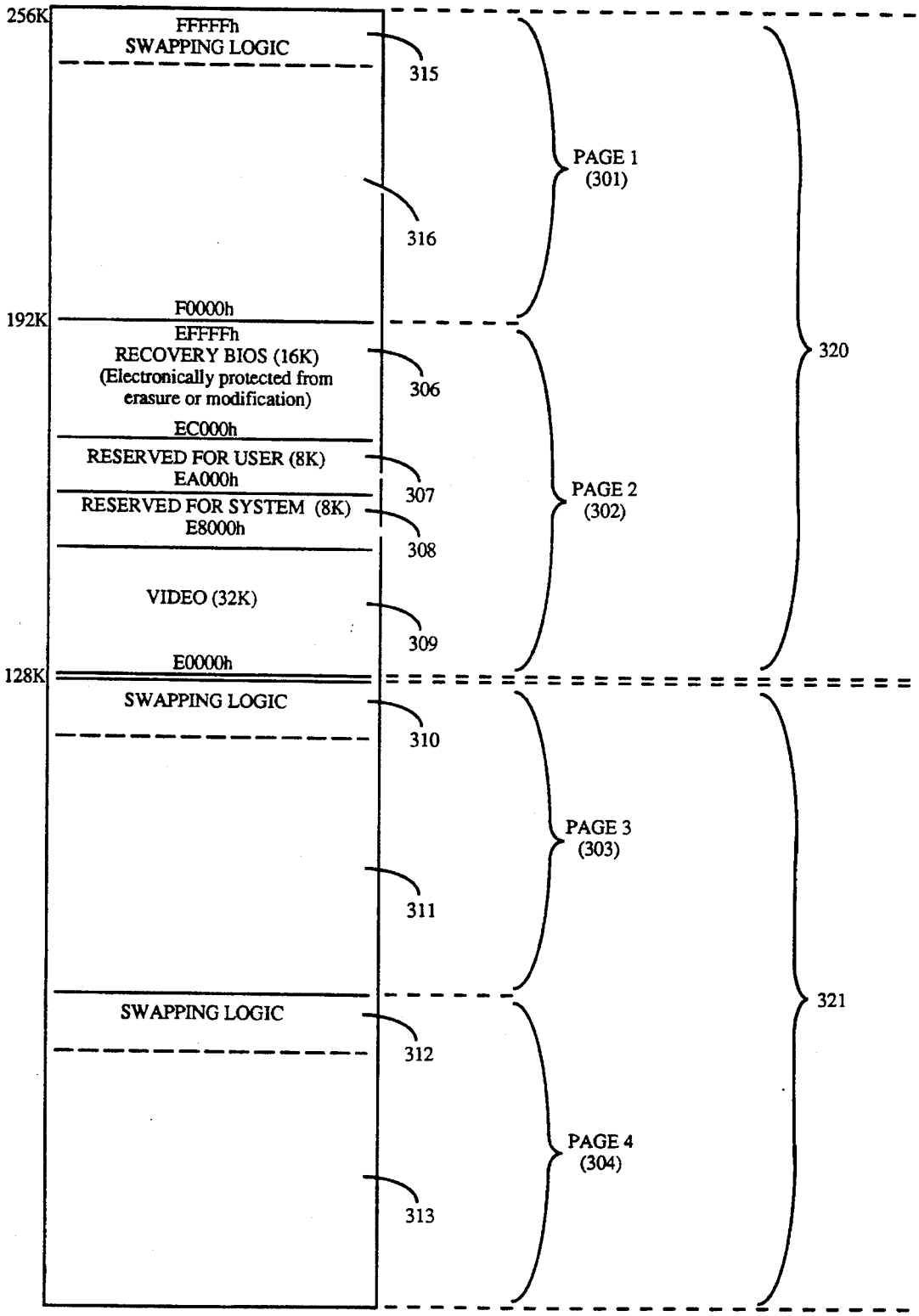

FIGURE 3A

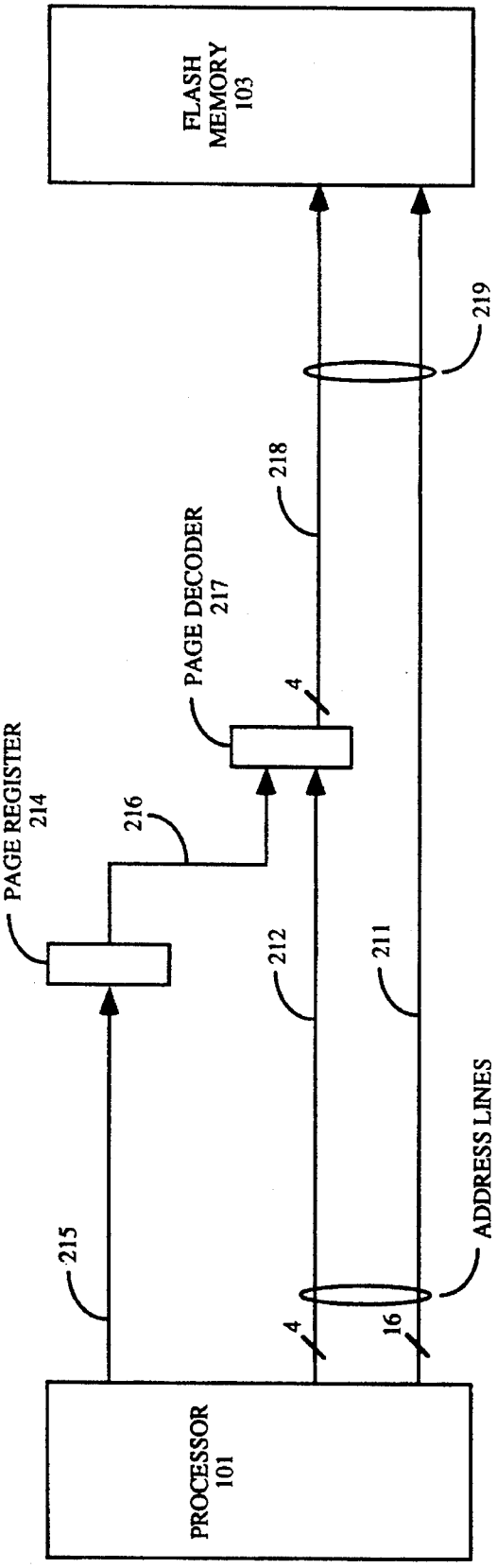

FIGURE 3B

PAGE	PROCESSOR ADDRESS	NON-VOLATILE MEMORY ADDRESS
1	F0000h - FFFFFh (64K)	F0000h - FFFFFh (64K)
2 (STATIC)	E0000h - EFFFFh (64K)	E0000h - EFFFFh (64K)
3	F0000h - FFFFFh (64K)	OTHER ADDRESS RANGE (i.e. D0000h - DFFFFh)
4	F0000h - FFFFFh (64K)	OTHER ADDRESS RANGE (i.e. C0000h - CFFFFh)
N/A	E0000h - EFFFFh (64K)	E0000h - EFFFFh (64K)
N/A	00000h - DFFFFh (64K)	00000h - DFFFFh (64K)

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