



**enCoRe USB™ CY7C63722/23**  
**PRELIMINARY**  
**CY7C63742/43**

---

---

---

**CY7C63722/23**  
**CY7C63742/43**  
**enCoRe™ USB**  
**Combination Low-Speed USB & PS/2**  
**Peripheral Controller**



**TABLE OF CONTENTS**

1.0 FEATURES ..... 5

2.0 FUNCTIONAL OVERVIEW ..... 6

2.1 enCoRe USB - The New USB Standard ..... 6

3.0 LOGIC BLOCK DIAGRAM ..... 7

4.0 PIN CONFIGURATIONS ..... 7

5.0 PIN ASSIGNMENTS ..... 7

6.0 PROGRAMMING MODEL ..... 8

6.1 Program Counter (PC) ..... 8

6.2 8-bit Accumulator (A) ..... 8

6.3 8-bit Index Register (X) ..... 8

6.4 8-bit Program Stack Pointer (PSP) ..... 8

6.5 8-bit Data Stack Pointer (DSP) ..... 8

6.6 Address Modes ..... 9

    6.6.1 Data ..... 9

    6.6.2 Direct ..... 9

    6.6.3 Indexed ..... 9

7.0 INSTRUCTION SET SUMMARY ..... 10

8.0 MEMORY ORGANIZATION ..... 11

8.1 Program Memory Organization ..... 11

8.2 Data Memory Organization ..... 12

8.3 I/O Register Summary ..... 13

9.0 CLOCKING ..... 14

9.1 Internal / External Oscillator Operation ..... 15

9.2 External Oscillator ..... 15

10.0 RESET ..... 15

10.1 Low Voltage Reset (LVR) ..... 16

10.2 Brown Out Reset (BOR) ..... 16

10.3 Watch Dog Reset (WDR) ..... 16

11.0 SUSPEND MODE ..... 16

11.1 Clocking Mode on Wake-up from Suspend ..... 17

11.2 Wake-up Timer ..... 17

12.0 GENERAL PURPOSE I/O PORTS ..... 18

12.1 Auxiliary Input Port ..... 20

13.0 USB SERIAL INTERFACE ENGINE (SIE) ..... 20

13.1 USB Enumeration ..... 21

13.2 USB Port Status and Control ..... 21

14.0 USB DEVICE ..... 22

14.1 USB Address Register ..... 22

14.2 USB Control Endpoint ..... 22

14.3 USB Non-Control Endpoints (2) ..... 23

14.4 USB Endpoint Counter Registers ..... 23

15.0 USB REGULATOR OUTPUT ..... 24

**TABLE OF CONTENTS (continued)**

<b>16.0 PS/2 OPERATION .....</b>	<b>24</b>
<b>17.0 SERIAL PERIPHERAL INTERFACE (SPI) .....</b>	<b>25</b>
17.1 Operation as an SPI Master .....	26
17.2 Master SCK Selection .....	26
17.3 Operation as an SPI Slave .....	27
17.4 SPI Status and Control .....	27
17.5 SPI Interrupt .....	28
17.6 SPI modes for GPIO pins .....	28
<b>18.0 12-BIT FREE-RUNNING TIMER .....</b>	<b>29</b>
<b>19.0 TIMER CAPTURE REGISTERS .....</b>	<b>30</b>
<b>20.0 PROCESSOR STATUS AND CONTROL REGISTER .....</b>	<b>32</b>
<b>21.0 INTERRUPTS .....</b>	<b>33</b>
21.1 Interrupt Vectors .....	34
21.2 Interrupt Latency .....	35
21.3 Interrupt Sources .....	35
21.3.1 USB Bus Reset or PS/2 Activity .....	35
21.3.2 Free Running Timer Interrupts .....	35
21.3.3 USB Endpoint Interrupts .....	35
21.3.4 SPI Interrupt .....	35
21.3.5 Capture Timer Interrupts .....	35
21.3.6 GPIO Interrupt .....	35
21.3.7 Wake-up Interrupt .....	37
<b>22.0 USB MODE TABLES .....</b>	<b>37</b>
<b>23.0 ABSOLUTE MAXIMUM RATINGS .....</b>	<b>40</b>
<b>24.0 DC CHARACTERISTICS .....</b>	<b>41</b>
<b>25.0 SWITCHING CHARACTERISTICS .....</b>	<b>42</b>
<b>26.0 ORDERING INFORMATION .....</b>	<b>47</b>
<b>27.0 PACKAGE DIAGRAMS .....</b>	<b>47</b>

**LIST OF FIGURES**

Figure 8-1. Program Memory Space with Interrupt Vector Table .....	11
Figure 9-1. Clock Oscillator On-chip Circuit .....	14
Figure 9-2. Clock Configuration Register (Address 0xF8) .....	14
Figure 10-1. Watch Dog Reset (WDR) .....	16
Figure 12-1. Block Diagram of GPIO Port (one pin shown) .....	18
Figure 12-2. Port 0 Data (Address 0x00) .....	19
Figure 12-3. Port 1 Data (Address 0x01) .....	19
Figure 12-4. GPIO Port 0 Mode0 Register (Address 0x0A) .....	19
Figure 12-5. GPIO Port 0 Mode1 Register (Address 0x0B) .....	20
Figure 12-6. GPIO Port 1 Mode0 Register (Address 0x0C) .....	20
Figure 12-7. GPIO Port 1 Mode1 Register (Address 0x0D) .....	20
Figure 12-8. Port 2 Data Register (Address 0x02) .....	20
Figure 13-1. USB Status and Control Register (Address 0x1F) .....	21
Figure 14-1. USB Device Address Register (Address 0x10) .....	22
Figure 14-2. USB EP0 Mode Register (Address 0x12) .....	22

**LIST OF FIGURES** (continued)

Figure 14-3. USB Endpoint EP1, EP2 Mode Registers (Addresses 0x14, 0x16) .....	23
Figure 14-4. USB Device Counter Registers (Addresses 0x11h, 0x13h, 0x15) .....	23
Figure 16-1. Diagram of USB - PS/2 System Connections .....	25
Figure 17-1. SPI Block Diagram .....	26
Figure 17-2. SPI Data Register (Address 0x60) .....	26
Figure 17-3. SPI Control Register (Address 0x61) .....	27
Figure 17-4. SPI Data Timing .....	28
Figure 18-1. Timer LSB Register (Address 0x24) .....	29
Figure 18-2. Timer MSB Register (Address 0x25) .....	29
Figure 18-3. Timer Block Diagram .....	29
Figure 19-1. Capture Timers Block Diagram .....	30
Figure 19-2. Capture Timer A-Rising, Data Register (Address 0x40) .....	31
Figure 19-3. Capture Timer A-Falling, Data Register (Address 0x41) .....	31
Figure 19-4. Capture Timer B-Rising, Data Register (Address 0x42) .....	31
Figure 19-5. Capture Timer B-Falling, Data Register (Address 0x43) .....	31
Figure 19-6. Capture Timers Configuration Register (Address 0x44) .....	31
Figure 19-7. Capture Timers Status Register (Address 0x45) .....	31
Figure 20-1. Processor Status and Control Register (Address 0xFF) .....	32
Figure 21-1. Global Interrupt Enable Register 0x20h (read/write) .....	33
Figure 21-2. USB End Point Interrupt Enable Register (Address 0x21) .....	33
Figure 21-3. Interrupt Controller Logic Block Diagram .....	34
Figure 21-4. Port 0 Interrupt Enable Register (Address 0x04) .....	36
Figure 21-5. Port 1 Interrupt Enable Register (Address 0x05) .....	36
Figure 21-6. Port 0 Interrupt Polarity Register (Address 0x06) .....	36
Figure 21-7. Port 1 Interrupt Polarity Register (Address 0x07) .....	36
Figure 21-8. GPIO Interrupt Diagram .....	36
Figure 25-1. Clock Timing .....	43
Figure 25-2. USB Data Signal Timing .....	43
Figure 25-3. Receiver Jitter Tolerance .....	44
Figure 25-4. Differential to EOP Transition Skew and EOP Width .....	44
Figure 25-5. Differential Data Jitter .....	44
Figure 25-7. SPI Slave Timing, CPHA=0 .....	45
Figure 25-6. SPI Master Timing, CPHA=0 .....	45
Figure 25-8. SPI Master Timing, CPHA=1 .....	46
Figure 25-9. SPI Slave Timing, CPHA=1 .....	46

**LIST OF TABLES**

Table 8-1. I/O Register Summary .....	13
Table 11-1. Wake-up Timer Adjust Settings .....	18
Table 12-1. Ports 0 and 1 Output Control Truth Table .....	19
Table 13-1. Control Modes to Force D+/D- Outputs .....	22
Table 17-1. SPI Control Register Definitions .....	27
Table 17-2. SPI Pin Assignments .....	28
Table 19-1. Capture Timer Prescaler Settings (Step size and range for FCLK = 6 MHz) .....	32
Table 21-1. Interrupt Vector Assignments .....	34
Table 22-1. USB Register Mode Encoding .....	37
Table 22-2. Decode table for Table 22-3: "Details of Modes for Differing Traffic Conditions" ...	38
Table 22-3. Details of Modes for Differing Traffic Conditions .....	39



## 1.0 Features

- enCoRe™ USB - enhanced Component Reduction
  - Internal oscillator eliminates the need for an external crystal or resonator
  - Interface can auto-configure to operate as PS/2 or USB without the need for external components to switch between modes (no GPIO pins needed to manage dual mode capability)
  - Internal 3.3V regulator for USB pull-up resistor
  - Configurable GPIO for real-world interface without external components
- Flexible, cost-effective solution for applications that combine PS/2 and low-speed USB, such as mice, gamepads, joysticks, and many others.
- USB Specification Compliance
  - Conforms to USB Specification, Version 1.1
  - Conforms to USB HID Specification, Version 1.1
  - Supports 1 Low-Speed USB device address and 3 data endpoints
  - Integrated USB transceiver
  - 3.3V regulated output for USB pull-up resistor
- 8-bit RISC microcontroller
  - Harvard architecture
  - 6-MHz external ceramic resonator or internal clock mode
  - 12-MHz internal CPU clock
  - Internal memory
  - 256 bytes of RAM
  - 6 Kbytes of EPROM (CY7C63722, CY7C63742)
  - 8 Kbytes of EPROM (CY7C63723, CY7C63743)
  - Interface can auto-configure to operate as PS/2 or USB
  - No external components for switching between PS/2 and USB modes
  - No GPIO pins needed to manage dual mode capability
- I/O ports
  - Up to 16 versatile General Purpose I/O (GPIO) pins, individually configurable
  - High current drive on any GPIO pin: 50 mA/pin current sink
  - Each GPIO pin supports high-impedance inputs, internal pull-ups, open drain outputs or traditional CMOS outputs
  - Maskable interrupts on all I/O pins
- SPI serial communication block
  - Master or slave operation
  - 2 Mbit/s transfers
- Four 8-bit Input Capture registers
  - Two registers each for two input pins
  - Capture timer setting with 5 pre-scaler settings
  - Separate registers for rising and falling edge capture
  - Simplifies interface to RF inputs for wireless applications
- Internal low-power wake-up timer during suspend mode
  - Periodic wake-up with no external components
- Optional 6-MHz internal oscillator mode
  - Allows fast start-up from suspend mode
- Watch dog timer (WDT)
- Low Voltage Reset at 3.75V
- Internal brown-out reset for suspend mode
- Improved output drivers to reduce EMI
- Operating voltage from 4.0V to 5.5VDC

# Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

## Real-Time Litigation Alerts



Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

## Advanced Docket Research



With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

## Analytics At Your Fingertips



Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

## API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

## LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

## FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

## E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.