

(12) **United States Patent**  
**Nguyen**

(10) **Patent No.:** **US 6,425,054 B1**  
(45) **Date of Patent:** **Jul. 23, 2002**

- (54) **MULTIPROCESSOR OPERATION IN A MULTIMEDIA SIGNAL PROCESSOR**
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- (\* ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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- (21) Appl. No.: **09/685,982**
- (22) Filed: **Oct. 10, 2000**

**Related U.S. Application Data**

- (63) Continuation of application No. 08/697,102, filed on Aug. 19, 1996, now abandoned.
- (51) **Int. Cl.**<sup>7</sup> ..... **G06F 12/08; G06F 13/00**
- (52) **U.S. Cl.** ..... **711/117; 711/118**
- (58) **Field of Search** ..... **711/117, 118, 711/130, 140, 147, 149; 712/1-9, 24, 29, 32-35; 345/501-506, 514-522; 710/131, 132**

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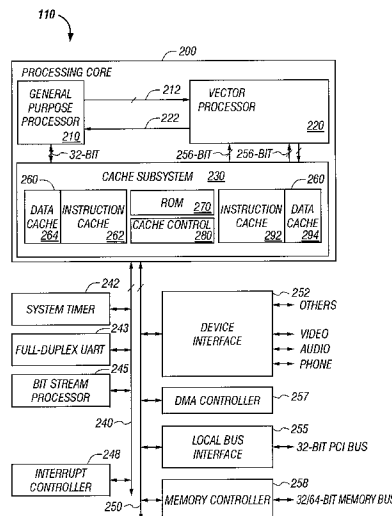
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(57) **ABSTRACT**

To achieve high performance at low cost, an integrated digital signal processor uses an architecture which includes both a general purpose processor and a vector processor. The integrated digital signal processor also includes a cache subsystem, a first bus and a second bus. The cache subsystem provides caching and data routing for the processors and buses. Multiple simultaneous communication paths can be used in the cache subsystem for the processors and buses. Furthermore, simultaneous reads and writes are supported to a cache memory in the cache subsystem.

**10 Claims, 8 Drawing Sheets**



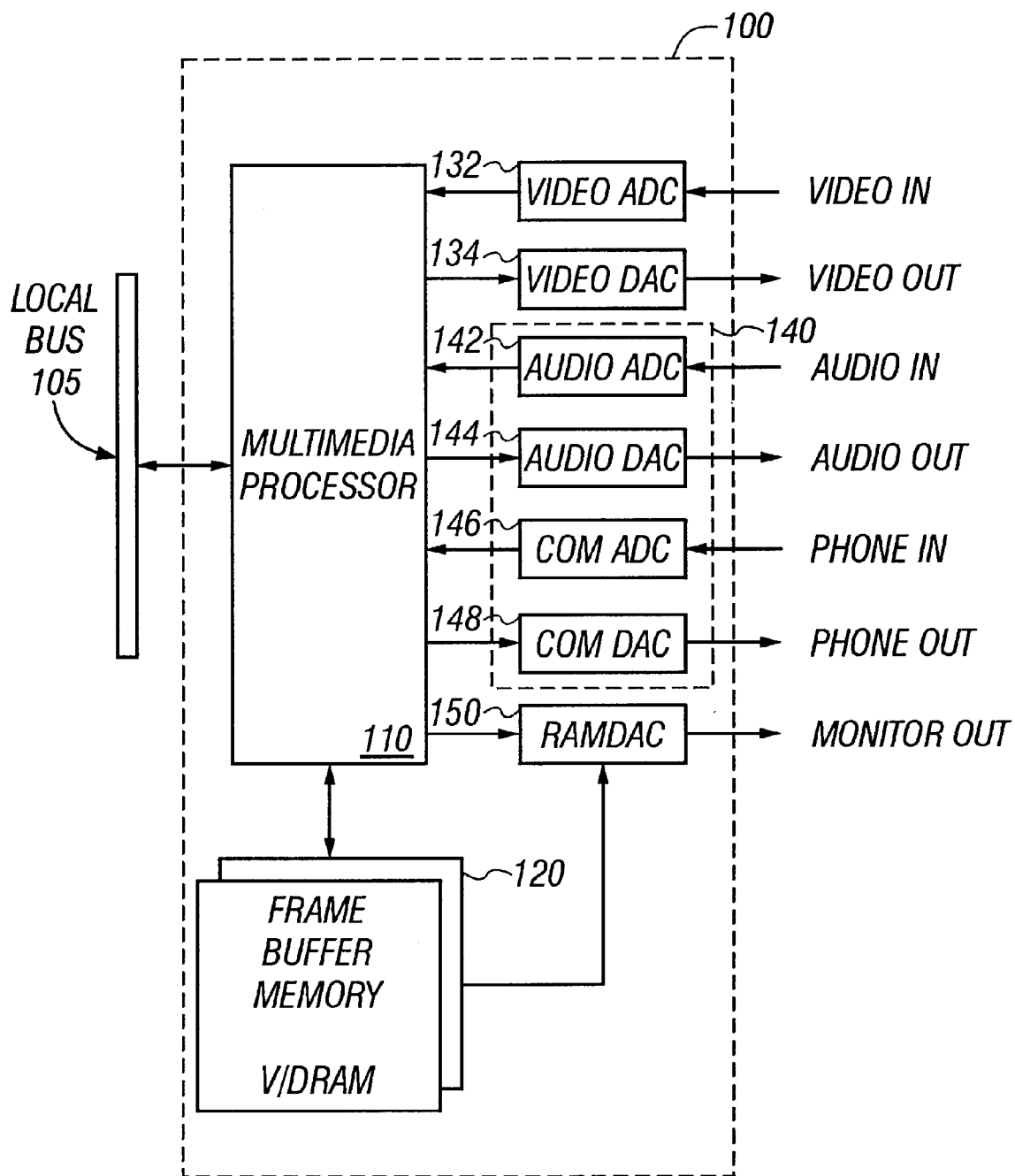


FIG. 1

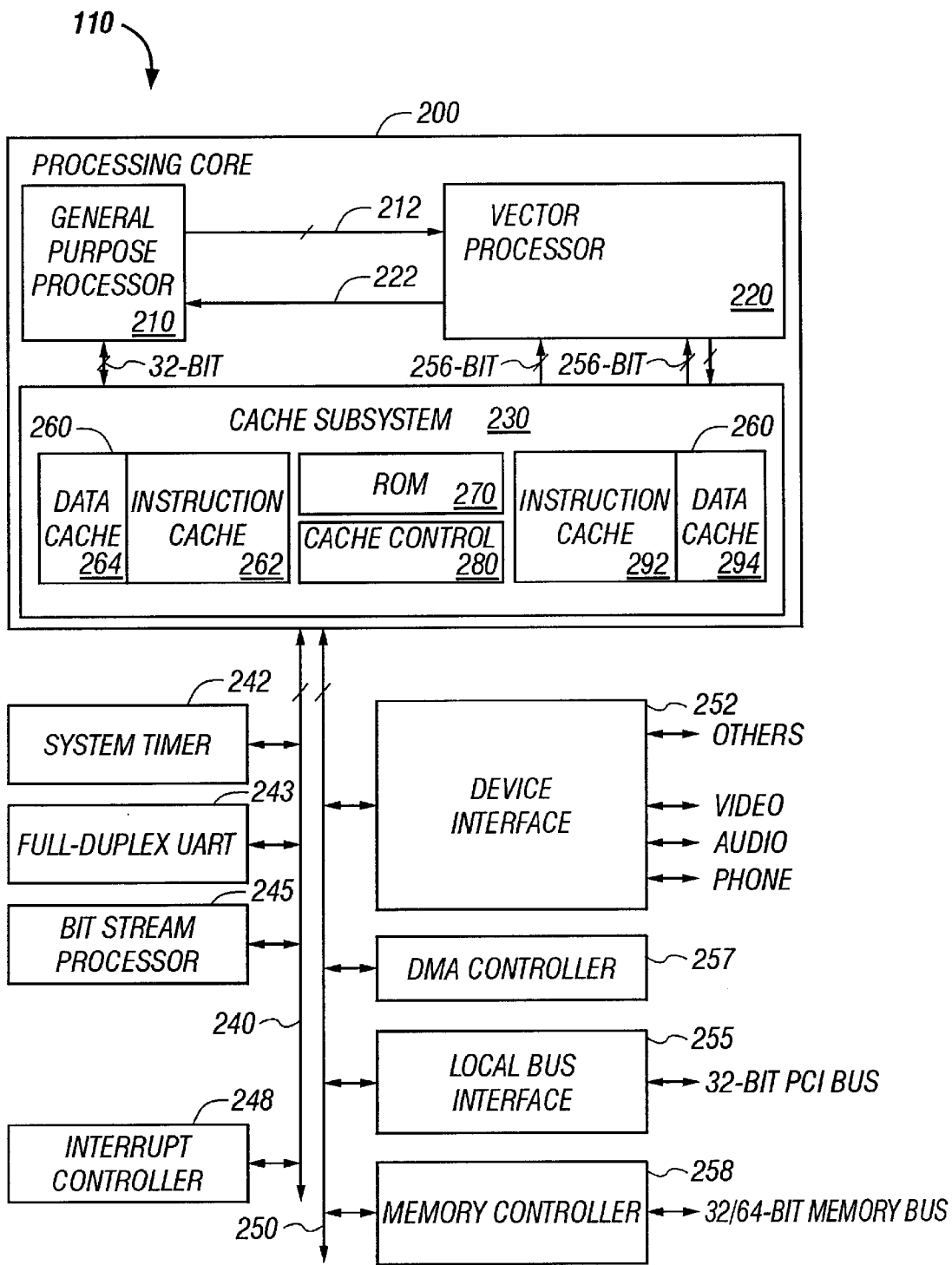


FIG. 2

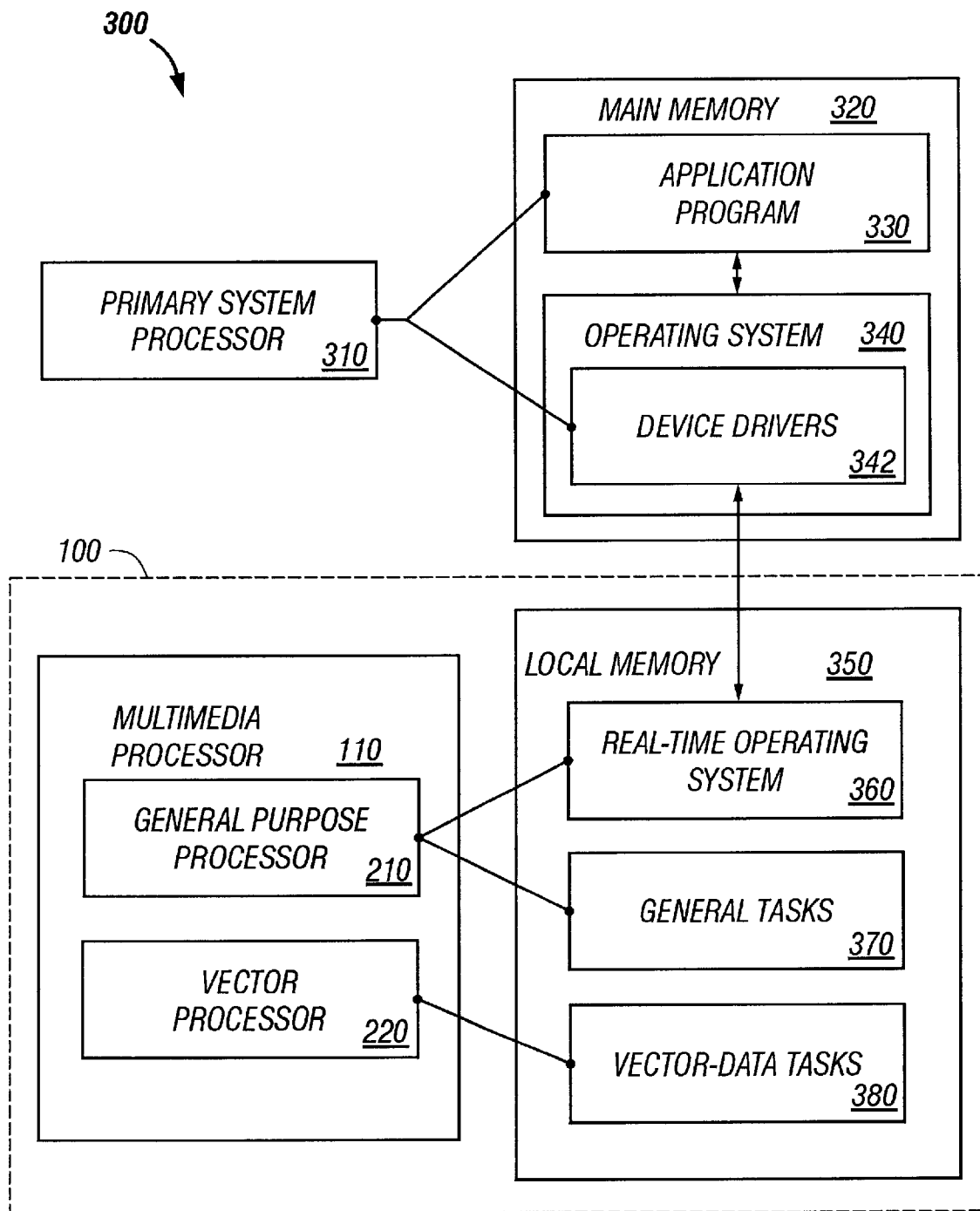


FIG. 3

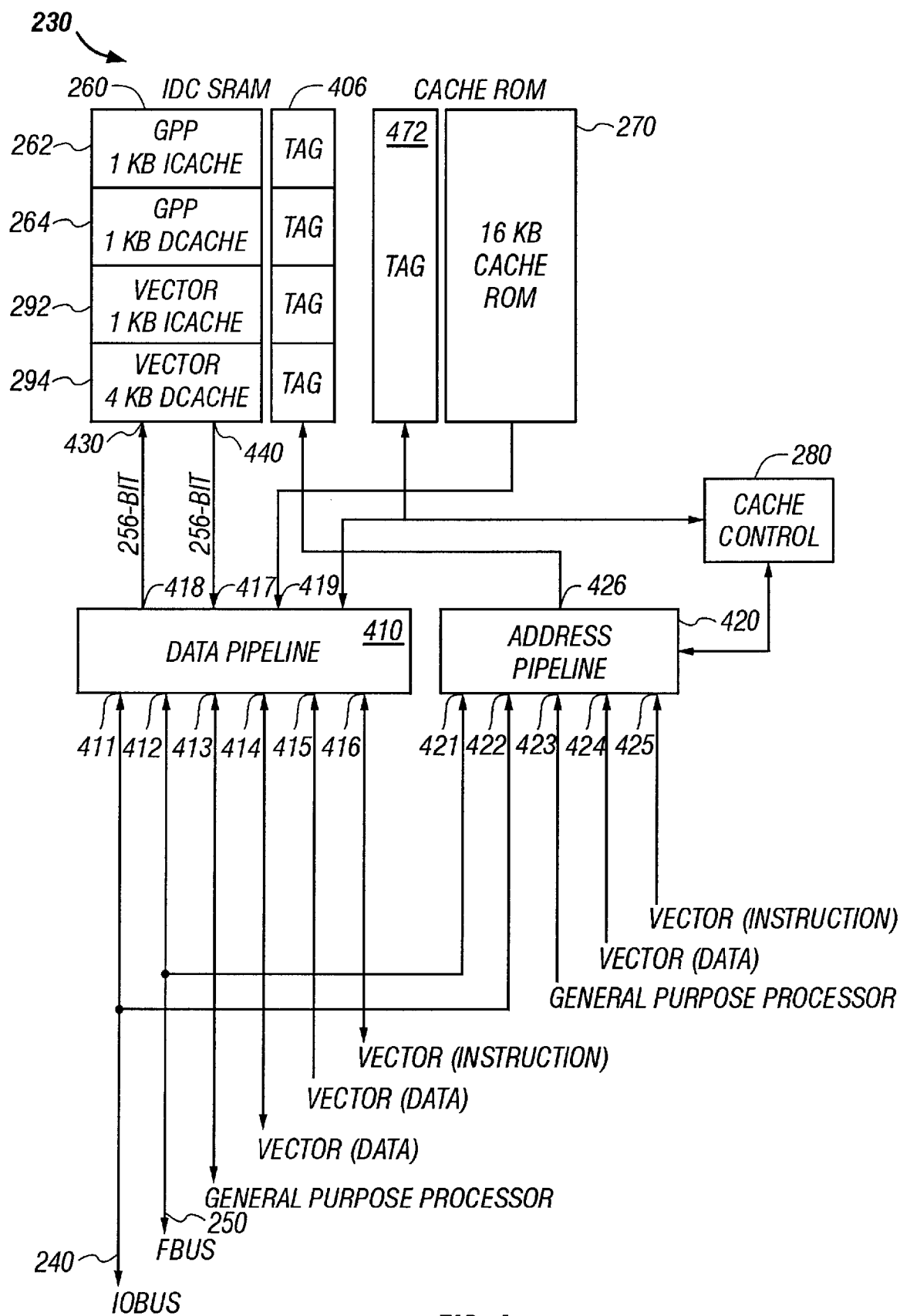


FIG. 4

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