



(12) **United States Patent**
Reeves

(10) **Patent No.:** **US 6,226,755 B1**
(45) **Date of Patent:** **May 1, 2001**

- (54) **APPARATUS AND METHOD FOR ENHANCING DATA TRANSFER TO OR FROM A SDRAM SYSTEM**
- (75) Inventor: **Earl C. Reeves**, Tomball, TX (US)
- (73) Assignee: **Compaq Computer Corp.**, Houston, TX (US)
- (*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.
- (21) Appl. No.: **09/236,871**
- (22) Filed: **Jan. 26, 1999**
- (51) **Int. Cl.⁷** **G06F 1/04**
- (52) **U.S. Cl.** **713/400; 713/600**
- (58) **Field of Search** **713/400, 500, 713/600; 711/105, 106, 167**

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* cited by examiner

Primary Examiner—Dennis M. Butler
(74) *Attorney, Agent, or Firm*—Kevin L. Daffer; Conley, Rose & Tayon

(57) **ABSTRACT**

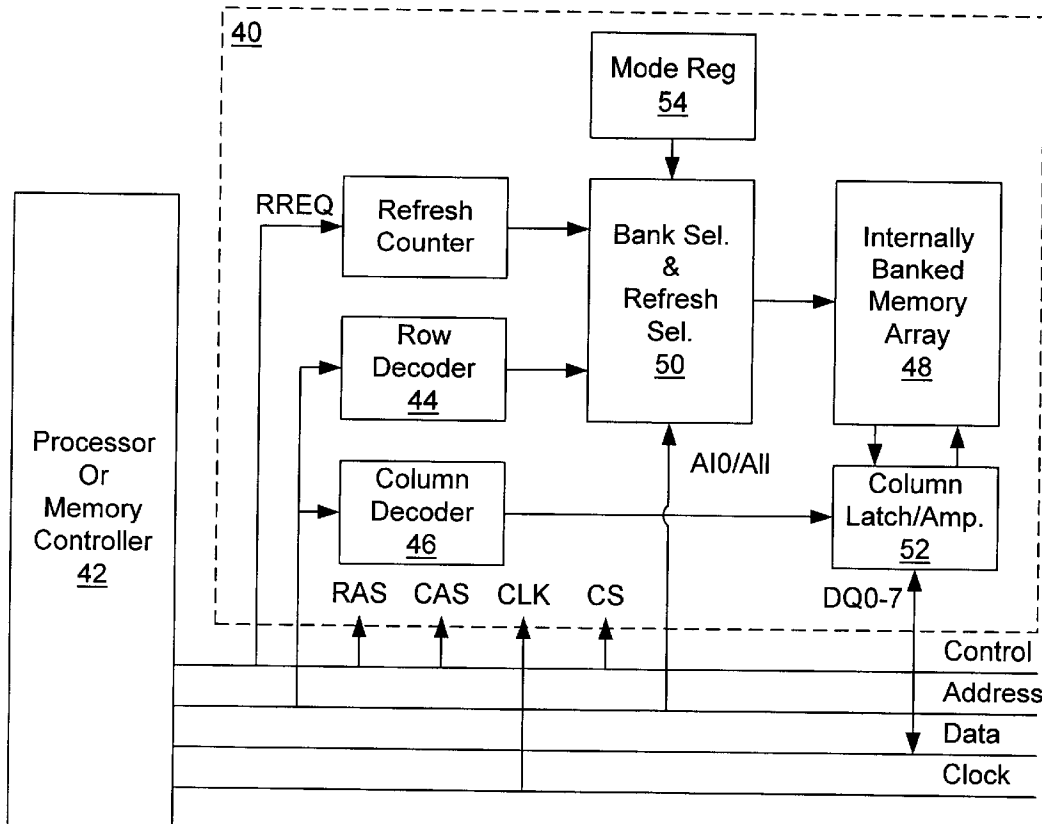
A computer system, bus interface unit employing a memory controller, and method are presented for optimizing the bandwidth data, address, and control transfer rates across a memory bus coupled to an SDRAM system. The SDRAM system is partitioned such that one partition will undergo pre-charge or refresh in the interim between times in which another partition (or a pair of partitions) initiate a burst read. The burst read cycles coincide with an initial column address of the burst, and are spaced a number of cycles equal to the burst length. Proper spacing of the initial column address, or read request, relative to a non-read requested partition ensures data read from the activated partition will be placed on the memory data bus in seamless fashion. That is, there are no non-data transfers occurring between data burst cycles, even though refresh or pre-charge operations are performed on a non-read partition. Careful placement of the hidden refresh cycles encountered by one partition relative to read cycles on other partitions ensures the data flow resulting therefrom will be optimized to sustain peak bandwidth on a synchronous DRAM memory bus.

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20 Claims, 4 Drawing Sheets



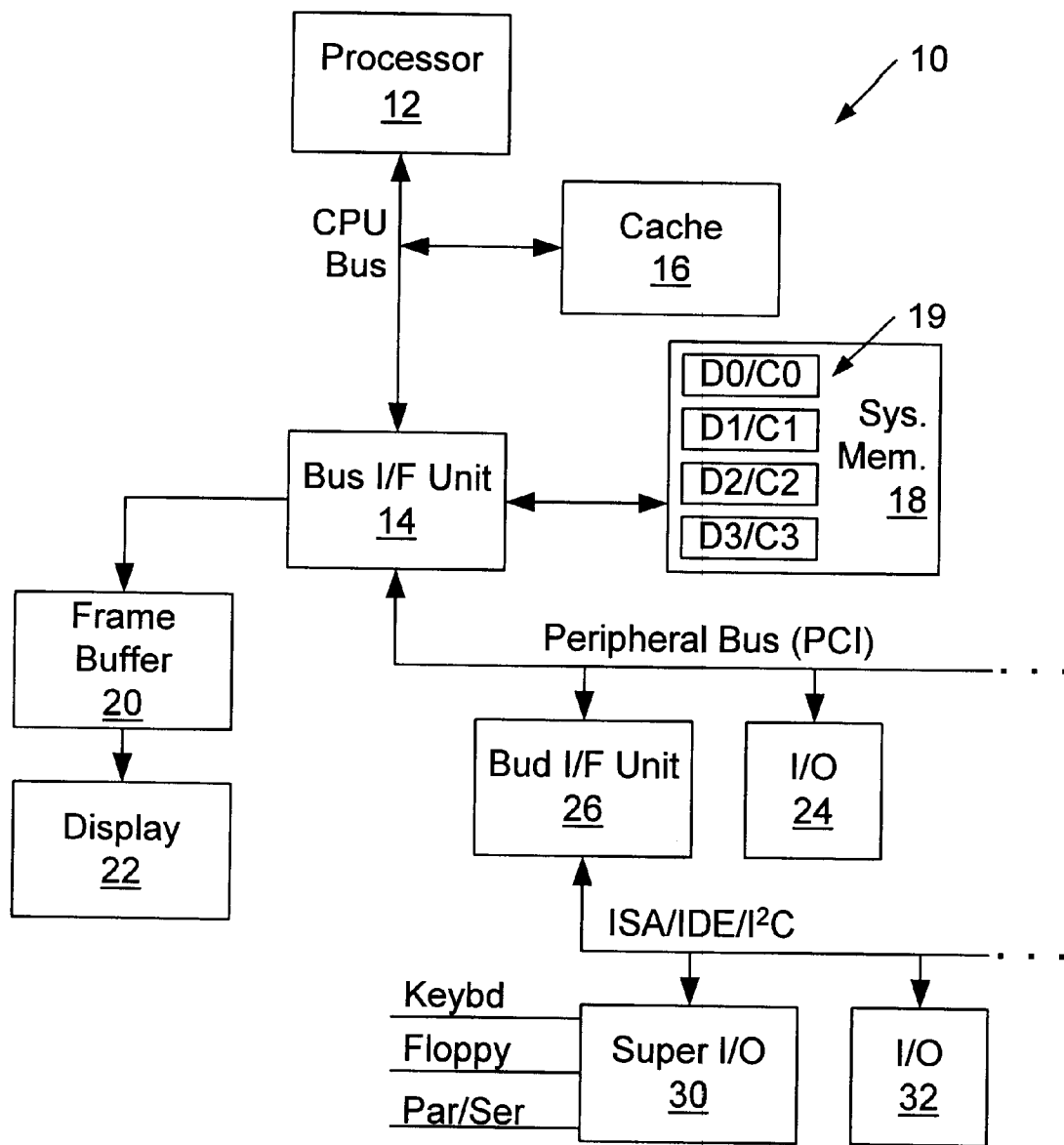


FIG. 1

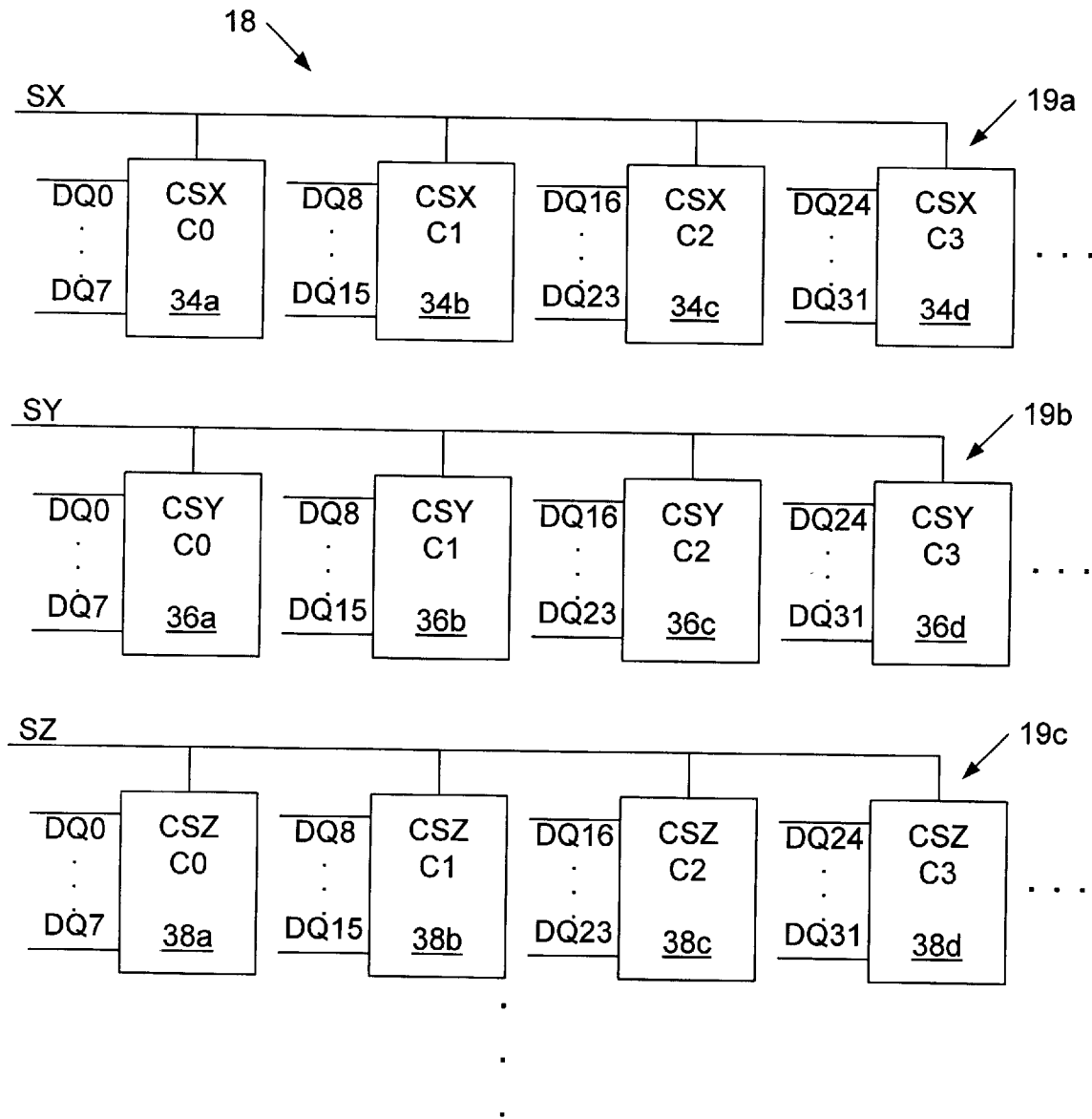


FIG. 2

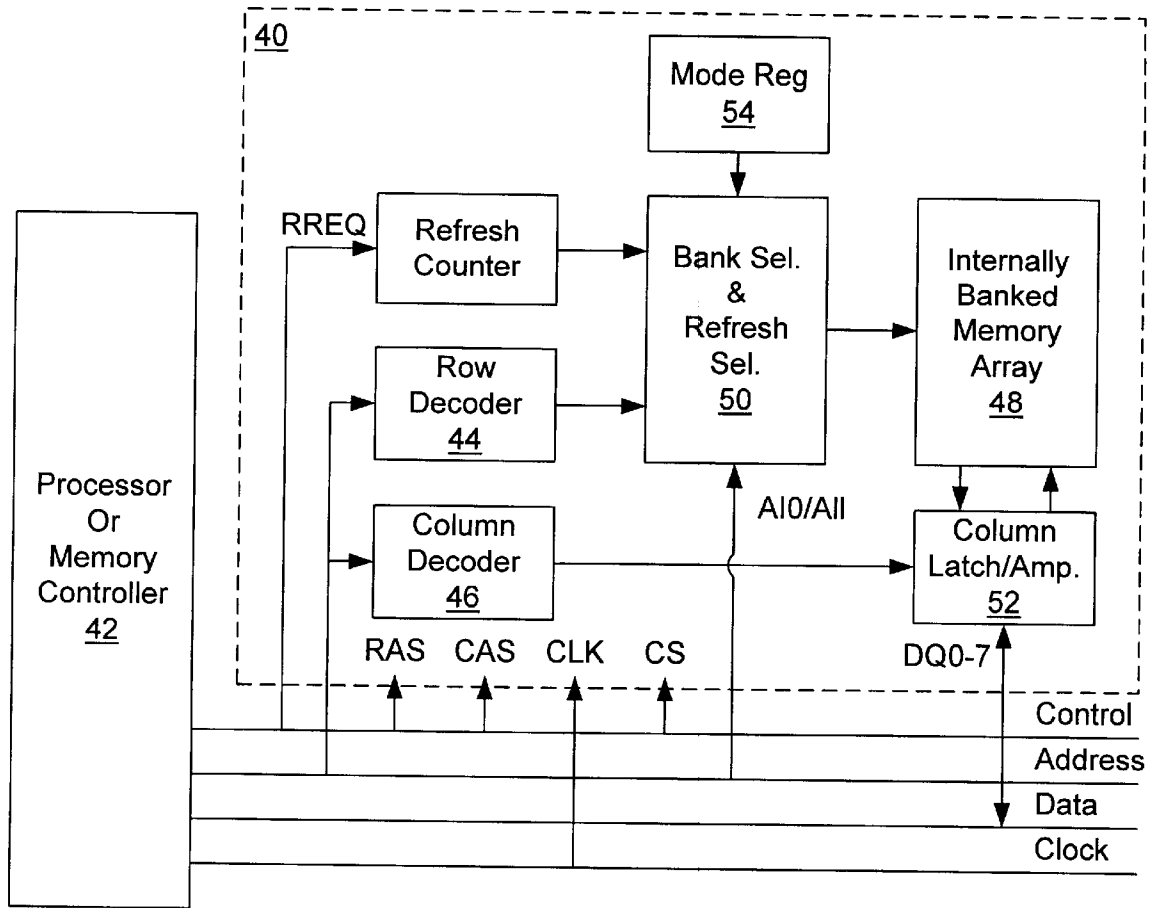


FIG.3

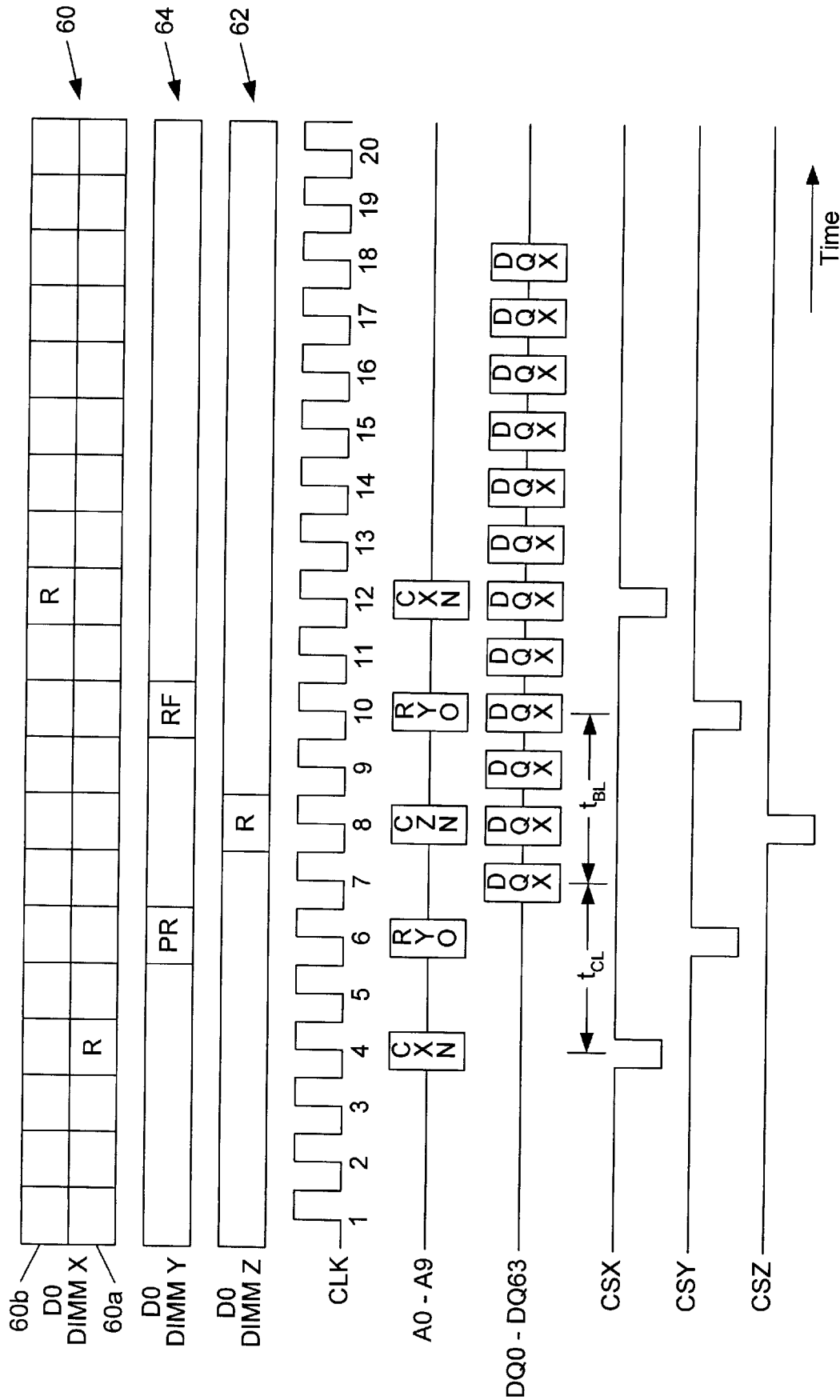


FIG.4

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