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(12) **United States Patent**  
**Fujioka et al.**

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(54) **SEMICONDUCTOR INTEGRATED CIRCUIT MEMORY**

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(75) Inventors: **Shinya Fujioka; Masao Taguchi; Yasuharu Sato; Takaaki Suzuki; Tadao Aikawa; Yasuou Matsuzaki; Toshiya Uchida**, all of Kawasaki (JP)

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(73) Assignee: **Fujitsu Limited**, Kawasaki (JP)

International Publication No. WO 98/19248, published May 7, 1998.

(\* ) Notice: Under 35 U.S.C. 154(b), the term of this patent shall be extended for 0 days.

\* cited by examiner

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*Primary Examiner*—Richard Elms  
*Assistant Examiner*—Hien Nguyen

(22) Filed: **Jun. 28, 1999**

(74) *Attorney, Agent, or Firm*—Arent Fox Kitner Plotkin & Kahn PLLC

(30) **Foreign Application Priority Data**

(57) **ABSTRACT**

Jun. 30, 1998 (JP) ..... 10-185097

(51) **Int. Cl.**<sup>7</sup> ..... **G11C 8/00**

(52) **U.S. Cl.** ..... **365/233; 365/230.03; 365/238.5**

(58) **Field of Search** ..... **365/233, 220, 365/203, 238.5, 221, 239, 230.03**

A semiconductor memory includes memory cell blocks, a burst-length information generating circuit which generates burst-length information based on a burst length, and a block enable circuit which receives the burst-length information. The block enable circuit selectively enables one of the memory cell blocks when the burst length is equal to or shorter than a predetermined burst length and selectively enables a plurality of memory cell blocks based on the burst length when the burst length is longer than the predetermined burst length. Data are read from the above-mentioned one or plurality of memory cell blocks.

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**16 Claims, 20 Drawing Sheets**

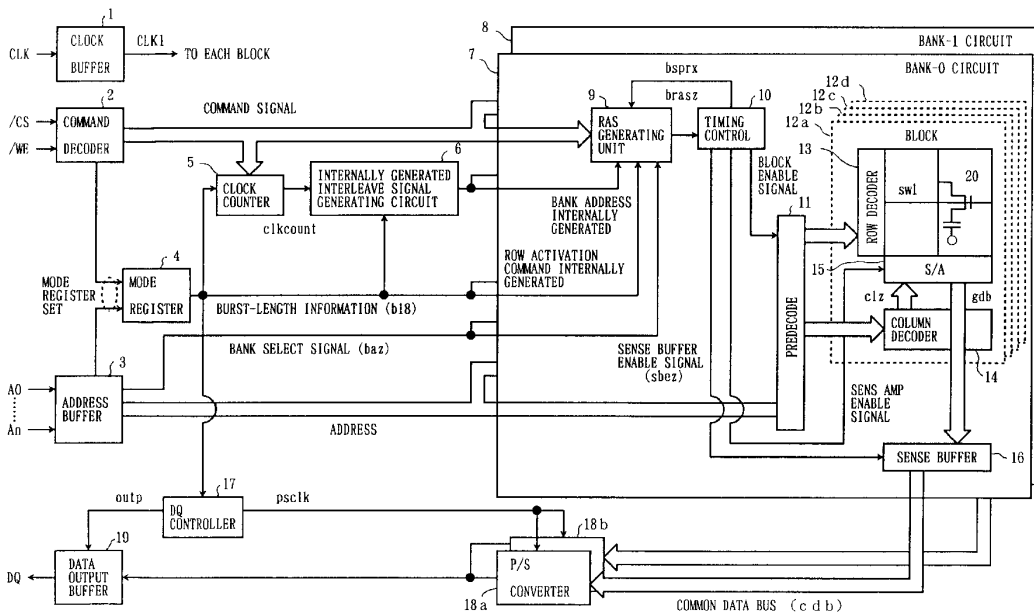
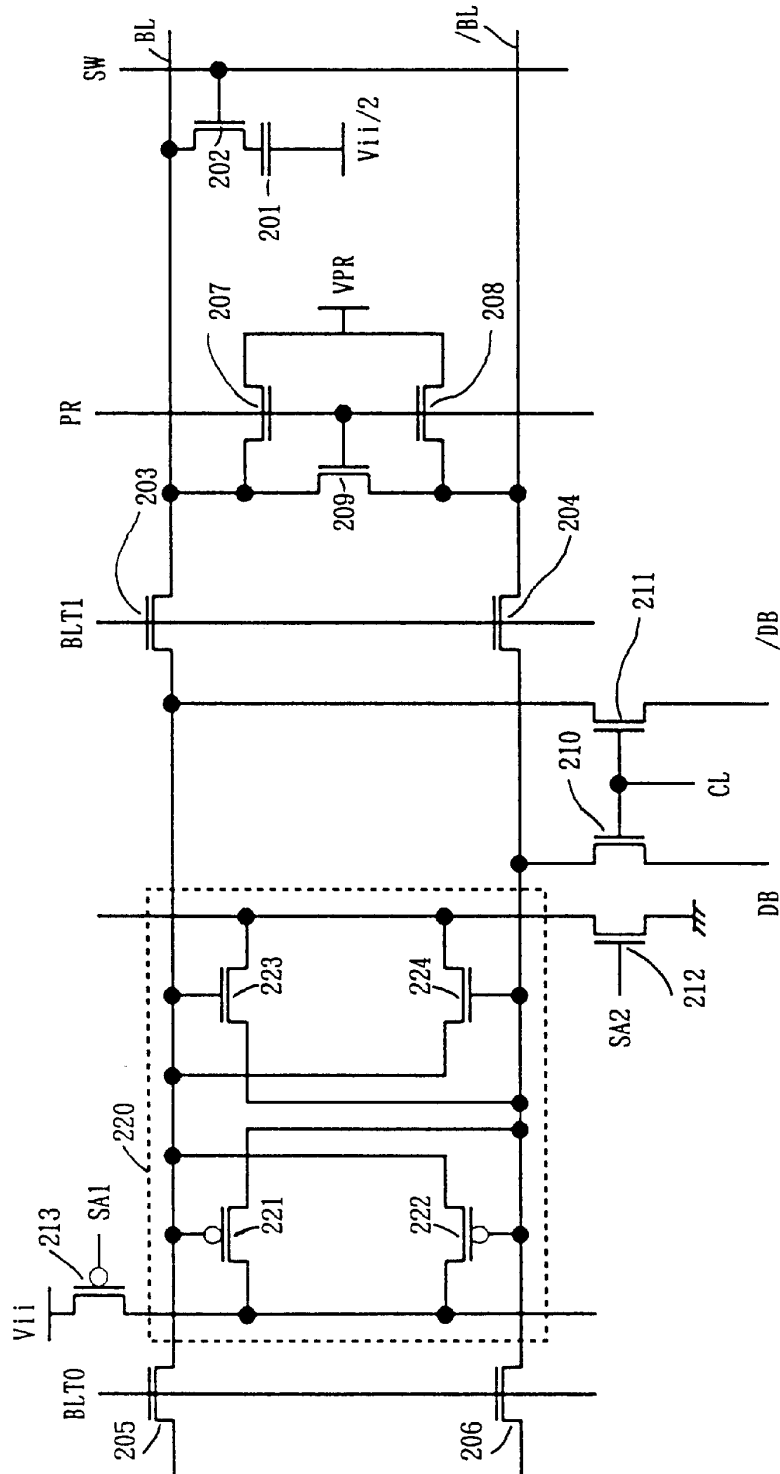


FIG. 1

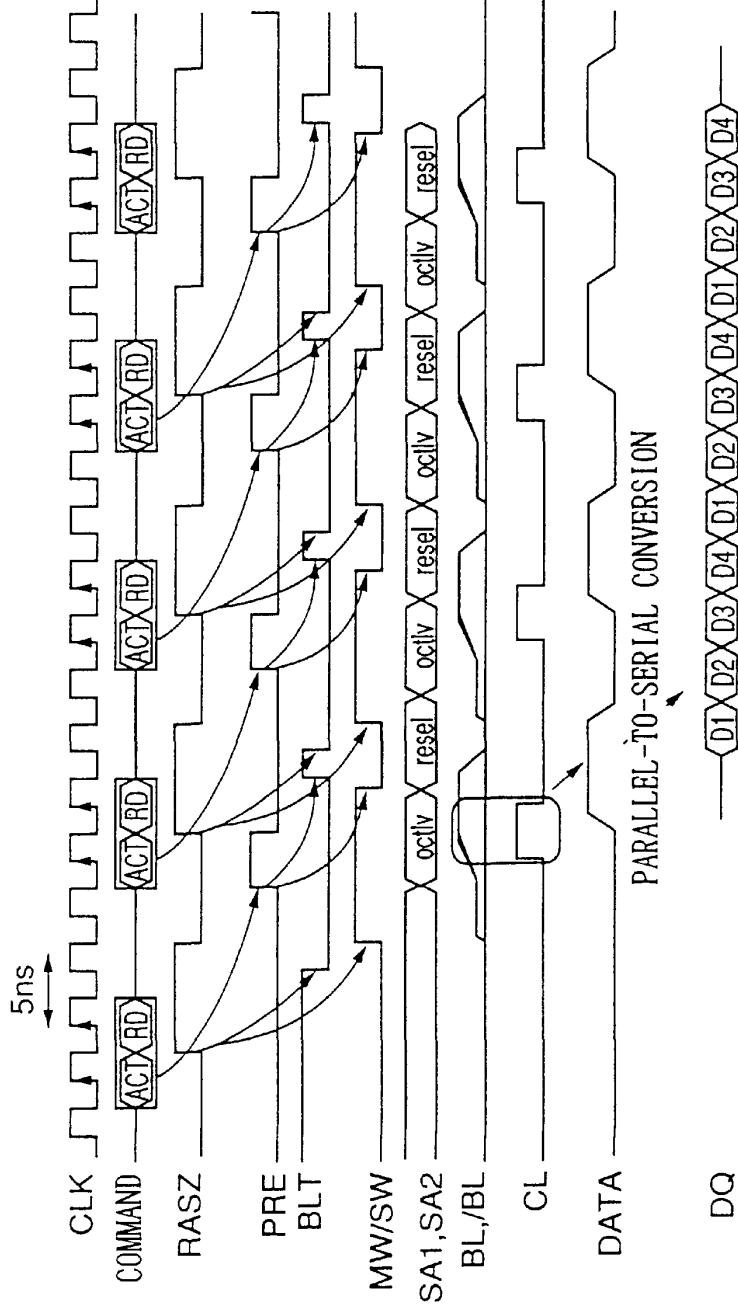
PRIOR ART





# FIG. 3

PRIOR ART



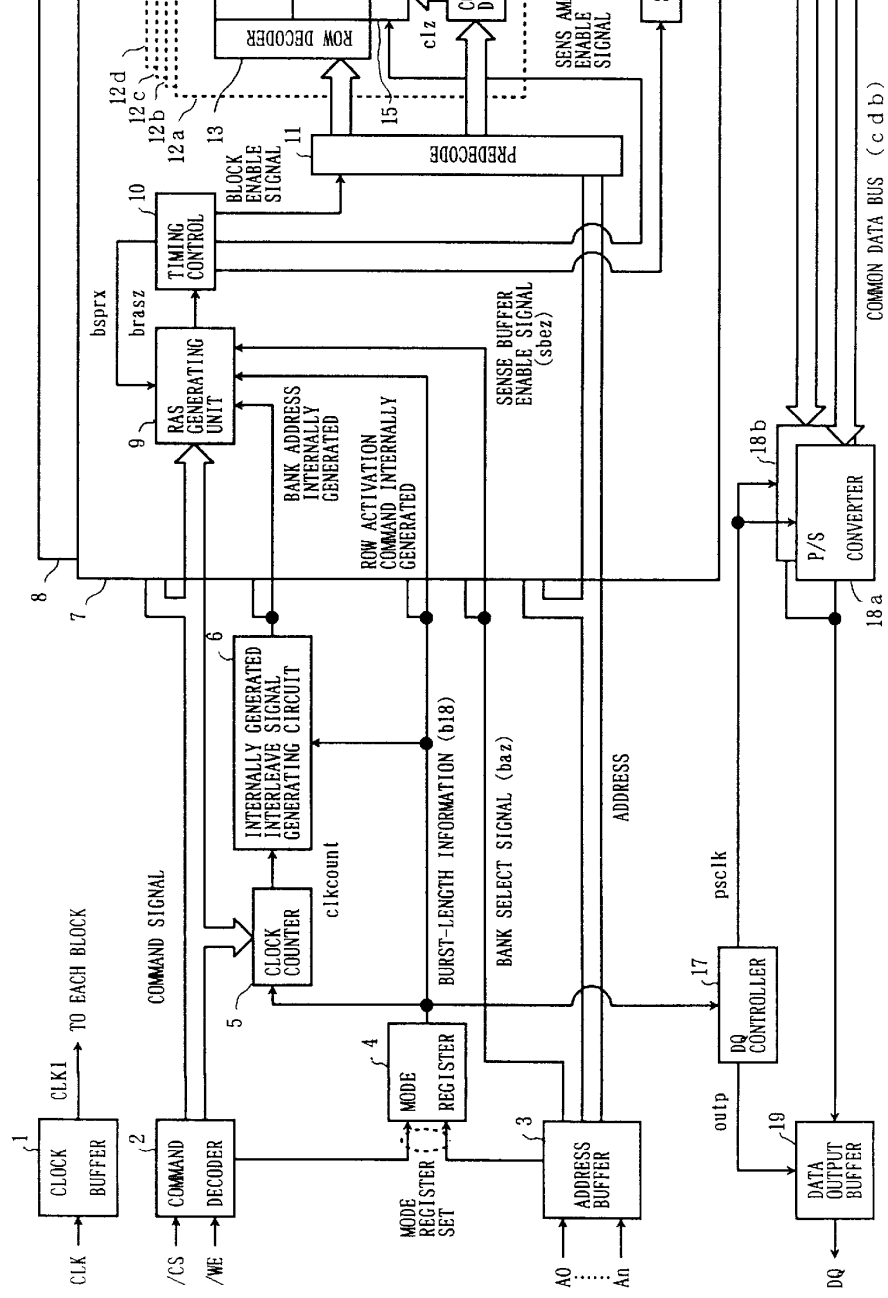


FIG. 4

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