JC542 U.S. PTO 09/504344 02/14/00

Class	Subclass	ISSUE CLASSIFICATION
711	104	

PATENT NUMBER

6651134

6651134

U.S. UTILITY Patent Application

O.I.P.E.	PATENT DATE
SCANNED RW AA Q.A. he	NOV 18 2003

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/504344		~~365~~	104	~~2824~~ 2824	Chan

APPLICANTS: Cathal Phelan

TITLE: Fixed burst memories

PTO-2040 12/99

ISSUING CLASSIFICATION

ORIGINAL CLASS	ORIGINAL SUBCLASS	CROSS REFERENCE(S) CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					
711	104	711	105	167	169			
INTERNATIONAL CLASSIFICATION		710	35					
C06F 12/00		365	233	238.5				

☐ Continued on Issue Slip Inside File Jacket

☐ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
	53	7	5A, 5B	21	1

☐ The term of this patent subsequent to _____ (date) has been disclaimed.

☐ The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____

☐ The terminal ____months of this patent have been disclaimed.

Medhi Namazi (Assistant Examiner) 6-12-03 (Date)

Donald Sparks (Primary Examiner) Supervisory Patent Examiner Technology Center 2100 6-13-03 (Date)

Dale Shaw (Legal Instruments Examiner) 6/24/03 (Date)

NOTICE OF ALLOWANCE MAILED: 6/16/03

ISSUE FEE

Amount Due	Date Paid
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ISSUE BATCH NUMBER

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PATENT APPLICATION

09504344

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PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
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01 FC:101 690.00 OP

PTO-1556
(5/87)

*U.S. GPO: 1999-459-082/19144

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SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/504,344	02/14/2000 RULE _	~~365~~ 711	~~2824~~ 2187	0325.000309

APPLICANTS
Cathal G. Phelan, Mountain View, CA ;

** CONTINUING DATA ********** none m.e

** FOREIGN APPLICATIONS ********** m.e

**IF REQUIRED, FOREIGN FILING LICENSE GRANTED **
** 05/02/2000

Foreign Priority claimed	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ yes ☑ no	CA	5	17	3
35 USC 119 (a-d) conditions met: ☐ yes ☑ no ☐ Met after Allowance				
Verified and Acknowledged: Examiner's Signature Initials				

ADDRESS
021363

TITLE Memory Device with Fixed Length Non-Interruptable Burst
~~Fixed burst memories~~

FILING FEE RECEIVED	FEES: Authority has been given in Paper
690	No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:

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02-15-00

A

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Utility Patent Application Transmittal
(Only for new non-provisional applications Under 37 CFR 1.53(b))

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D. C. 20231

Case Docket No. 0325.00030
Date: February 14, 2000

Sir:

Transmitted herewith for filing is a patent application of:

Inventor(s): Cathal G. Phelan

For: FIXED BURST MEMORIES

Enclosed are:

1. X Specification (13 pages); Claims (4 pages); Abstract (1 page)

2. X 5 sheets of formal drawings.

3. X Oath or Declaration Total Pages 2
   a. X Newly executed (original or copy)
   b. ___ Copy from a prior application (37 CFR 1.63(d)) (for continuation/divisional with Item 5 completed)
   c. ___ Copy of Revocation of Previous Power

4. ___ Incorporation By Reference (usable if Item 3b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Item 3b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

5. ___ If a Continuing Application, check appropriate box and supply the requisite information below and in a preliminary amendment:

___ Continuation _____ Divisional _____ Continuation-in-part (CIP) of prior application no.: _____

6. X An assignment to CYPRESS SEMICONDUCTOR CORP. along with PTO form 1595.

7. ___ A PTO Form 1449 with a copy of the references not previously cited.

8. X Return Receipt Postcard

9. ___ Other:

The filing fee has been calculated as shown below:

	No. Filed	No. Extra	Fee	Amount
Basic Fee	--	--	--	$690.00
Total Claims	17	0	x $ 18.00	$ 0.00
Indep. Claims	3	0	x $ 78.00	$ 0.00
Mult. Dep. Claims			$260.00	$ 0.00

SUB-TOTAL $690.00

__ SMALL ENTITY STATUS (divide SUB-TOTAL by two) ..... $____

X Assignment Recordal Fee ($40.00) ..... $ 40.00

TOTAL $730.00

X A check in the amount of $730.00 to cover the filing fee is enclosed.

X The Commissioner is hereby authorized to charge any fees under 37 CFR 1.16 and 1.17 which may be required by this paper or associated with this filing to Deposit Account No. 50-0541. A duplicate copy of this sheet is enclosed.

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CERTIFICATE OF EXPRESS MAILING

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By: Mary Donna Berkley
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Respectfully submitted,

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Attorney Docket No.: 0325.00309

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CD99073

Sub a1

FIXED BURST MEMORIES

Field of the Invention

The present invention relates to memory devices generally and, more particularly, to a memory device that transfers a fixed number of words of data with each access.

Background of the Invention

A synchronous Static Random Access Memory (SRAM) can provide data from multiple address locations using a single address. Accessing multiple locations in response to a single address is called a burst mode access. A memory device that provides a burst mode can reduce activity on the address and control buses. The burst mode of a conventional synchronous SRAM can be started and stopped in response to a control signal.

A conventional Dynamic Random Access Memory (DRAM) preserves data during periodic absences of power by implementing a memory cell as a capacitor and an access transistor. Since the charge on the capacitor will slowly leak away, the cells need to be "refreshed" once every few milliseconds. Depending on the frequency of accesses, a conventional DRAM can need an interrupt to

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perform data refreshes. Using a DRAM in a burst application is difficult because of the need to refresh. Completely hiding refresh cycles (e.g., refreshing data without the need for interrupts) in a DRAM cannot happen with conventional memory devices due to architecture choices that have been made. Data word bursts can be interrupted while in progress since conventional architectures support both burst and single access modes. Conventional DRAM access takes about 10ns to get data, but nearly 20ns to complete writeback and equalization. The addition of another 20ns for a refresh results in a total access of 40ns.

Since the data burst transfers of conventional memories can be interrupted and single accesses made, the amount of time that the data, address and control busses are not in use can vary. The variability of bus availability complicates the design of systems with shared data, address and control busses.

It would be desirable to have a memory device that has a fixed burst length.

Summary of the Invention

The present invention concerns an integrated circuit comprising a memory and a logic circuit. The memory may comprise

a plurality of storage elements each configured to read and write data in response to an internal address signal. The logic circuit may be configured to generate a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals. The generation of the predetermined number of internal address signals may be non-interruptible.

The objects, features and advantages of the present invention include providing a fixed burst memory that may (i) give network customers who typically burst large data lengths the ability to set a fixed burst length that suits particular needs; (ii) have non-interruptible bursts; (iii) free up the address bus and control bus for a number of cycles; (iv) provide programmability for setting the burst length by using DC levels [Vss or Vcc] on external pins; (v) hide required DRAM refreshes inside a known fixed burst length of data words; and/or (vi) operate at higher frequencies without needing interrupts to perform refreshes of data.

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Brief Description of the Drawings

These and other objects, features and advantages of the present invention will be apparent from the following detailed description and the appended claims and drawings in which:

FIG. 1 is a block diagram illustrating a preferred embodiment of the present invention;

FIG. 2 is a detailed block diagram illustrating a circuit 102 of FIG. 1;

FIG. 3 is a detailed block diagram of a circuit 102' illustrating an alternative embodiment of the circuit 102 of FIG. 1;

FIG. 4 is a flow diagram illustrating an example burst address sequence;

FIGS. 5A and 5B are diagrams illustrating example operations of a 4 word (FIG. 5A) and an 8 word (FIG. 5B) fixed burst access in accordance with the present invention; and

FIG. 6 is a diagram illustrating an example operation where a burst length may be long enough to include a writeback and a refresh cycle.

Detailed Description of the Preferred Embodiments

Referring to FIG. 1, a block diagram of a circuit 100 is shown in accordance with a preferred embodiment of the present invention. The circuit 100 may be implemented, in one example, as a fixed burst memory. The circuit 100 may be configured to transfer a fixed number of words of data with each access (e.g., read or write). A number of words transferred as a group is called a burst. The circuit 100 generally comprises a circuit 102 and a memory array (or circuit) 104. The circuit 102 may be implemented, in one example, as a burst address counter/register. The memory array 104 may be implemented, in one example, as a static random access memory (SRAM), a dynamic random access memory (DRAM), or other appropriate memory to meet the design criteria of a particular implementation.

The circuit 102 may have an input 106 that may receive a signal (e.g., ADDR_EXT), an input 108 that may receive a signal (e.g., LOAD), an input 110 that may receive a signal (e.g., CLK), an input 112 that may receive a signal (e.g., ADV), and an input 114 that may receive a signal (e.g., BURST). The circuit 102 may have an output 116 that may present a signal (e.g., ADDR_INT) to an input 118 of the memory 104. The memory 104 may have an input 120

that may receive a signal (e.g., R/Wb), an input 122 that may receive a signal (e.g., DATA_IN) and an output 122 that may present a signal (e.g., DATA_OUT). The various signals are generally "on" (e.g., a digital HIGH, or 1) or "off" (e.g., a digital LOW, or 0). However, the particular polarities of the on (e.g., asserted) and off (e.g., de-asserted) states of the signals may be adjusted (e.g., reversed) accordingly to meet the design criteria of a particular implementation.

The signal ADDR_EXT may be, in one example, an external address signal. The signal ADDR_EXT may be n-bits wide, where n is an integer. The signal CLK may be a clock signal. The signal R/Wb may be a control signal that may be in a first state or a second state. When the signal R/Wb is in the first state, the circuit 100 will generally read data from the memory circuit 104 for presentation as the signal DATA_OUT. When the signal R/Wb is in the second state, the circuit 100 will generally store data received as the signal DATA_IN.

The signal LOAD may be, in one example, an address load control signal. The circuit 100 may be configured to load an initial address, presented by the signal ADDR_EXT, in response to the signal LOAD. The initial address may determine the initial

location where data transfers to and from the memory 104 will generally begin.

The signal ADV may be, in one example, used as a control signal. The circuit 100 may be configured to transfer a fixed number of words to or from the memory 104 in response to the signals ADV, CLK and R/Wb. When the signal ADV is asserted, the circuit 100 will generally begin transferring a predetermined number of words. The transfer is generally non-interruptible. In one example, the signal ADV may initiate the generation of a number of addresses for presentation as the signal ADDR_INT.

The signals ADV and LOAD may be, in one example, a single signal (e.g., ADV/LDb). The signal ADV/LDb may be a control signal that may be in a first state or a second state. When the signal ADV/LDb is in the first state, the circuit 102 will generally load an address presented by the signal ADDR_EXT as an initial address. When the signal ADV/LDb is in the second state, the circuit 102 may be configured to generate the signal ADDR_INT as a fixed number of addresses in response to the signal CLK. The signal ADDR_INT may be, in one example, an internal address signal. The signal ADDR_INT may be n-bits wide. Once the circuit 102 has started generating the fixed number of addresses, the circuit 102 will

generally not stop until the fixed number of addresses has been generated (e.g., a non-interruptible burst).

The signal BURST may be, in one example, a configuration signal for programming the fixed number of addresses that the circuit 102 may generate in response to the signals CLK and ADV/LDb. The signal BURST may be generated, in one example, by (i) using bond options, (ii) voltage levels applied to external pins, or (iii) other appropriate signal generation means.

When the memory 104 is implemented as a DRAM, the circuit 100 may be configured to hide required DRAM refreshes (e.g., refreshes may occur without affecting external environment) inside a known fixed burst length of data words. The fixed burst length may allow the circuit 100 to operate at higher frequencies than a conventional DRAM without needing interrupts to perform refreshes of data. In one example, the fixed burst length may be four or eight words. However, the burst length may be set to whatever length is necessary to meet the design criteria of a particular application. For example, the burst length may be programmed, in one example, to allow both writeback and refresh to occur within a single access. The fixed burst length may be set, in one example,

longer or shorter depending upon a frequency or technology to be used.

The circuit 100 may be configured to provide a fixed burst length that may suit the requirements of network customers who typically burst large data lengths. By providing a fixed burst length, the circuit 100 may allow shared usage of data, address and control busses. A fixed length non-interruptible burst generally frees up the address bus and control bus for a known number of cycles. The address and control busses may be shared by a number of memory devices. The circuit 100 may provide a more reliable and /or accurate burst than is possible with multiple chips.

Referring to FIG. 2, a detailed block diagram illustrating implementation of the circuit 102 is shown. The circuit 102 may comprise an address counter register 126 and a burst counter 128. The address counter register 126 generally receives the signals ADDR_EXT, LOAD, and CLK. The address counter register 126 may be configured to present the signal ADDR_INT. The signal ADV and the signal BURST may be presented to a burst counter 128. The signal CLK may be presented at an input 130 of the burst counter 128. The burst counter 128 may have an output 132 that may present a signal (e.g., BURST_CLK) at an input 134 of the circuit

126. An initial address may be loaded into the address counter register 126 by presenting the initial address in the signal ADDR_EXT and asserting the signal LOAD. The circuit 126 may be configured to increment an address in response to the signal BURST_CLK. When the signal ADV is asserted, the burst counter 128 will generally present the signal BURST_CLK in response to the signal CLK. The signal BURST_CLK generally contains a number of pulses that has been programmed by the signal BURST.

Referring to FIG. 3, a detailed block diagram illustrating an alternative embodiment of the circuit 102 is shown. The circuit 102' may comprise a latch 134, a multiplexer 136 and a counter 138. The signals ADDR_EXT, LOAD and CLK may be presented to the latch 134. The latch 134 may have an output 140 that may present a portion (e.g., m bits, where m is an integer smaller than n) of the signal ADDR_EXT as a portion of the signal ADDR_INT, an output 142 that may present a second portion (e.g., k bits, where k is an integer smaller than n) of the signal ADDR_EXT to a first input of the multiplexer 136, and an output 144 that may present the second portion of the signal ADDR_EXT to an input 146 of the counter 138.

The signals ADV, CLK and BURST may be presented to inputs of the counter 138. The counter 138 may be configured to generate a number of addresses in response to the signals CLK, BURST and ADV. The number of addresses generated by the counter 138 may be programmed by the signal BURST.

The signal BURST may be presented to a control input of the multiplexer 136. The multiplexer 136 may select between a number of signals from the latch 134 and a number of signals from the counter 138 to be presented as a second portion of the signal ADDR_INT in response to the signal BURST.

Referring to FIG. 4, a flow diagram illustrating an example burst address sequence is shown. When the signal ADV is asserted, the circuit 100 will generally generate a number of address signals, for example, N where N is an integer. The address signals may be generated, in one example, on a rising edge of the signal CLK. The address signals will generally continue to be generated until the Nth address signal is generated.

Referring to FIGS. 5A and 5B, timing diagrams illustrating example operations for a four word (FIG. 5A) and an eight word (FIG. 5B) fixed burst memory in accordance with the present invention are shown. The timing diagrams generally

illustrate externally measurable signals for four and eight word fixed burst read/write architectures. In general, an operation (e.g., read or write) of the circuit 100 begins with loading an initial address (e.g., portions 150, 154, and 158 of FIG. 5A; portions 150', 154', and 158' of FIG. 5B). Starting with the initial address, a fixed number of words are generally transferred (e.g., line DQ of FIGS. 5A and 5B). During the transfer of the fixed number of words, the address and control buses (e.g., ADDR, CE, R/W, etc.) are generally available to other devices (e.g., portions 152, 156, and 160 of FIG. 5A; portions 152', 156', and 160' of FIG. 5B). In one example, the control and address bus activity may be one-fourth (FIG. 5A) or one-eighth (FIG. 5B) the data bus activity (e.g., compare line ADDR with line DQ of FIGS. 5A and 5B). The reduced bus activity may be an effect of the architecture. The data bus may be, in one example, active nearly 100% of the time (e.g., line DQ of FIGS. 5A and 5B) In one example, there may be no inefficiencies switching from read to write to read etcetera (e.g., see labels under line DQ of FIGS. 5A and 5B).

Referring to FIG. 6, a timing diagram illustrating a fixed burst length long enough to hide a writeback and a refresh cycle is shown. Internally the action being performed may

completely hide DRAM refresh activity inside nominal external activities. A portion 162 illustrates that refresh activity (e.g., writeback, read for refresh, and writeback for refresh) may be completed within the time of the burst transfer. When a fixed burst long enough to completely hide refresh activity is provided, there may be no penalty for using DRAM instead of SRAM for the memory 104.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

CLAIMS

1. An integrated circuit comprising:

a memory comprising a plurality of storage elements each configured to read and write data in response to an internal address signal; and

a logic circuit configured to generate a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

2. The integrated circuit according to claim 1, wherein said predetermine number of internal address signals is determined by a fixed burst length.

3. The integrated circuit according to claim 1, wherein said predetermined number of internal address signals is 4.

4. The integrated circuit according to claim 1, wherein said predetermined number of internal address signals is 8.

5. The integrated circuit according to claim 2, wherein said fixed burst length is programmable.

6. The integrated circuit according to claim 5, wherein said fixed burst length is programmed by bond options.

7. The integrated circuit according to claim 5, wherein said fixed burst length is programmed by voltage levels on external pins.

8. The integrated circuit according to claim 1, wherein said memory comprises a static random access memory.

9. The integrated circuit according to claim 1, wherein said memory comprises a dynamic random access memory.

10. The integrated circuit according to claim 9, wherein said predetermined number of internal address signals is chosen to provide time for writeback and refresh cycles.

11. The integrated circuit according to claim 1, wherein said predetermined number of internal address signals is chosen to meet predetermined criteria for sharing address and control busses.

12. An integrated circuit comprising:

means for reading and writing data in response to an internal address signal; and

means for generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

13. A method of providing a fixed burst length data transfer comprising the steps of:

reading from and writing data to a memory in response to an internal address signal; and

generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) a control signal, wherein said generation

of said predetermined number of internal address signals is non-interruptible.

14. The method according to claim 13, further comprising the step of programming said predetermined number.

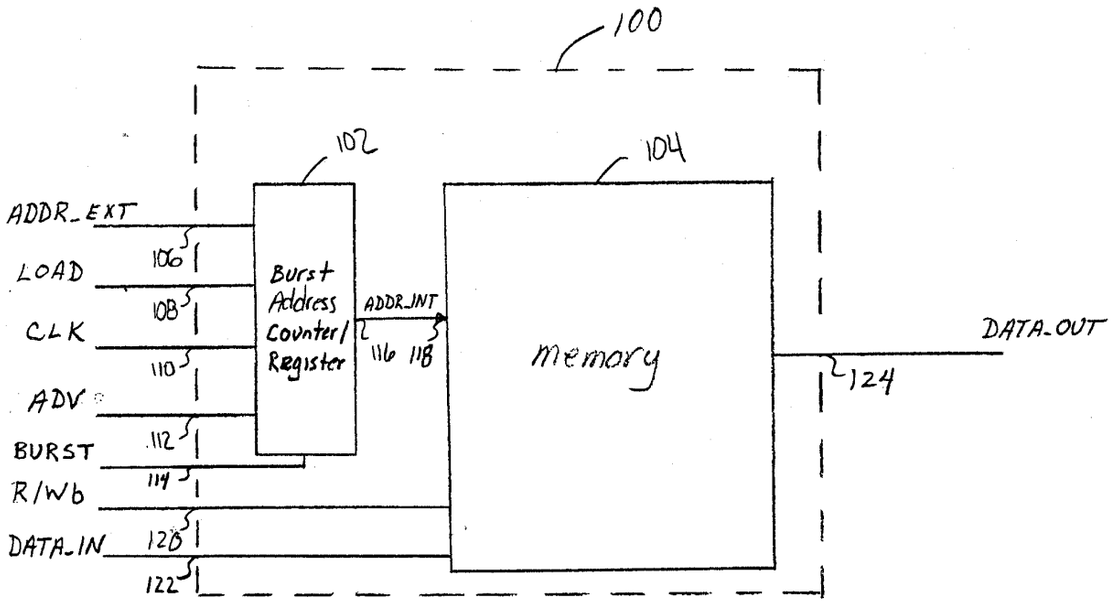
15. The method according to claim 14, wherein said programming step is performed using bond options.

16. The method according to claim 14, wherein said programming step is performed using voltage levels.

17. The method according to claim 13, further comprising the step of selecting said predetermined number to provide time for writeback and refresh cycles.

ABSTRACT OF THE DISCLOSURE

An integrated circuit comprising a memory and a logic circuit. The memory may comprise a plurality of storage elements each configured to read and write data in response to an internal address signal. The logic circuit may be configured to generate a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals. The generation of the predetermined number of internal address signals may be non-interruptible.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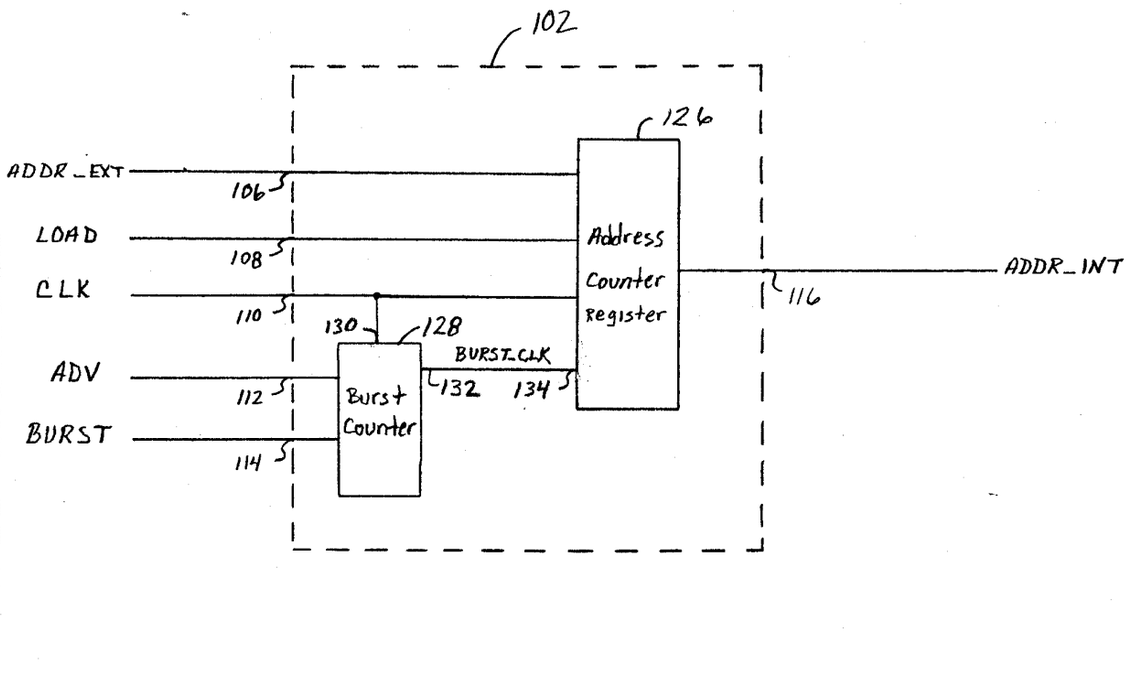
102
104
ADDR_EXT
LOAD
CLK
ADV
BURST
R/Wb
DATA_IN
106
108
110
112
114
120
122
Burst Address Counter/ Register
ADDR_INT
116
118
memory
DATA_OUT
124

FIG. 1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126
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106
LOAD
108
CLK
110
ADV
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130
128
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132
134
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Counter
Register
Burst
Counter
116
ADDR_INT

FIG. 2

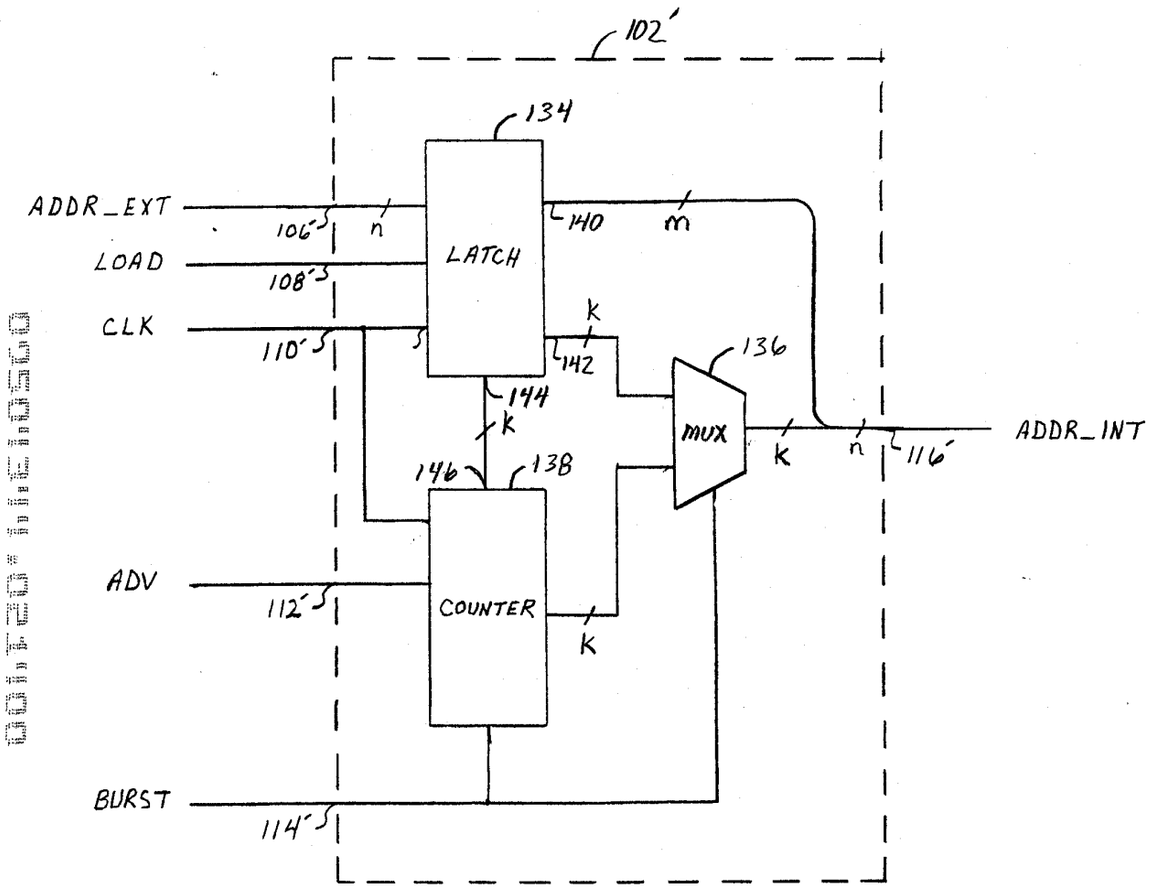

102'
134
ADDR_EXT
106'
n
LATCH
140
m
LOAD
108'
CLK
110'
k
142
136
144
k
MUX
k
n
116'
ADDR_INT
146
138
ADV
112'
COUNTER
k
BURST
114'

FIG.3

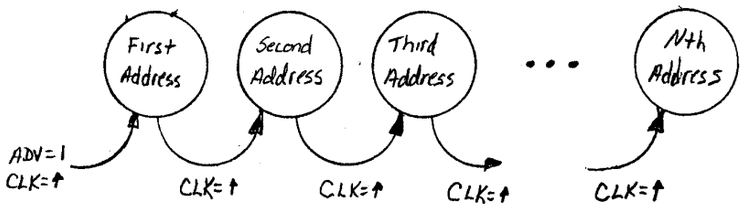

First Address
Second Address
Third Address
Nth Address
ADV=1
CLK=↑
CLK=↑
CLK=↑
CLK=↑
CLK=↑

FIG. 4

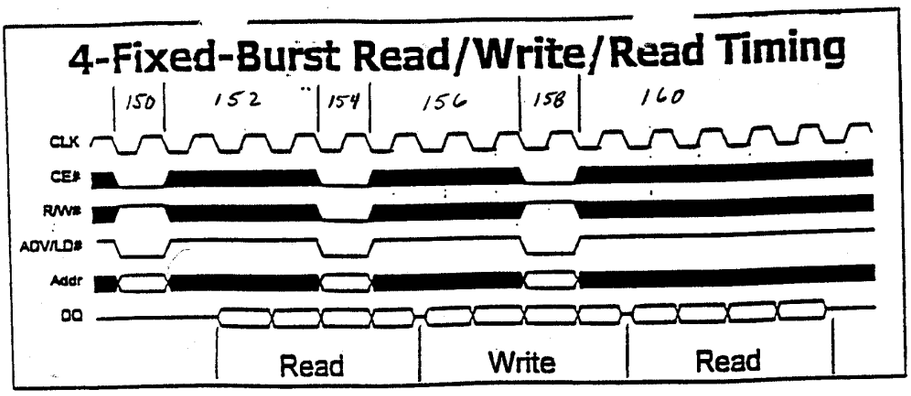


FIG. 5A

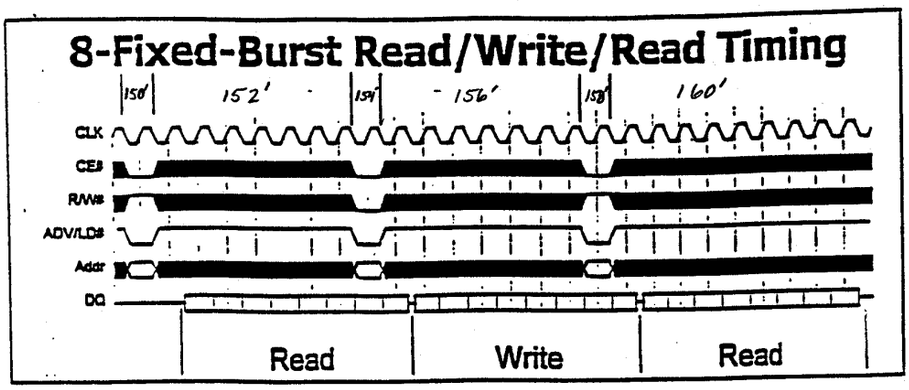


FIG. 5B

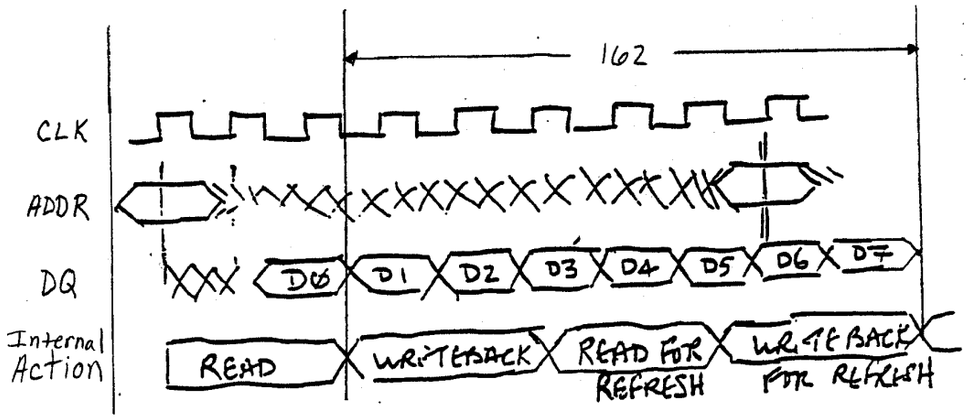


FIG. 6

PRINT OF DRAWINGS
AS ORIGINALLY FILED

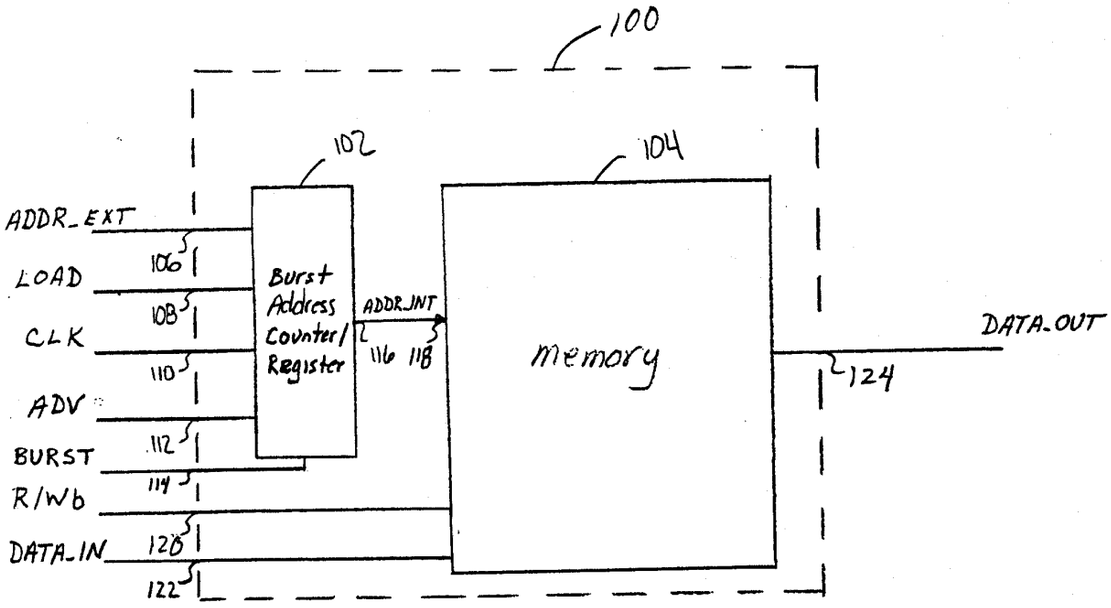


FIG. 1

PRINT OF DRAWINGS
AS ORIGINALLY FILED

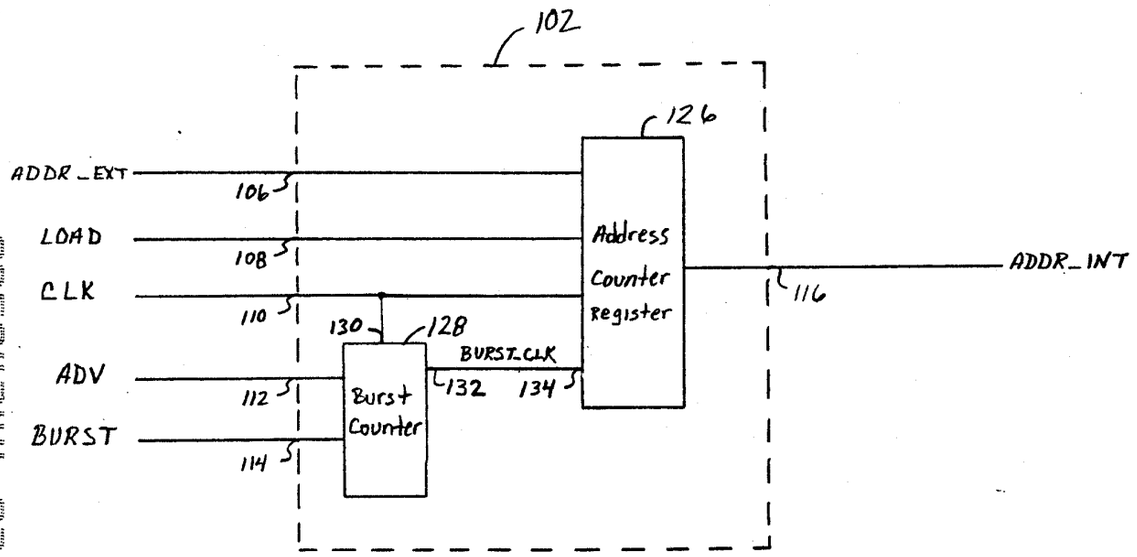


FIG. 2

PRINT OF DRAWINGS
AS ORIGINALLY FILF

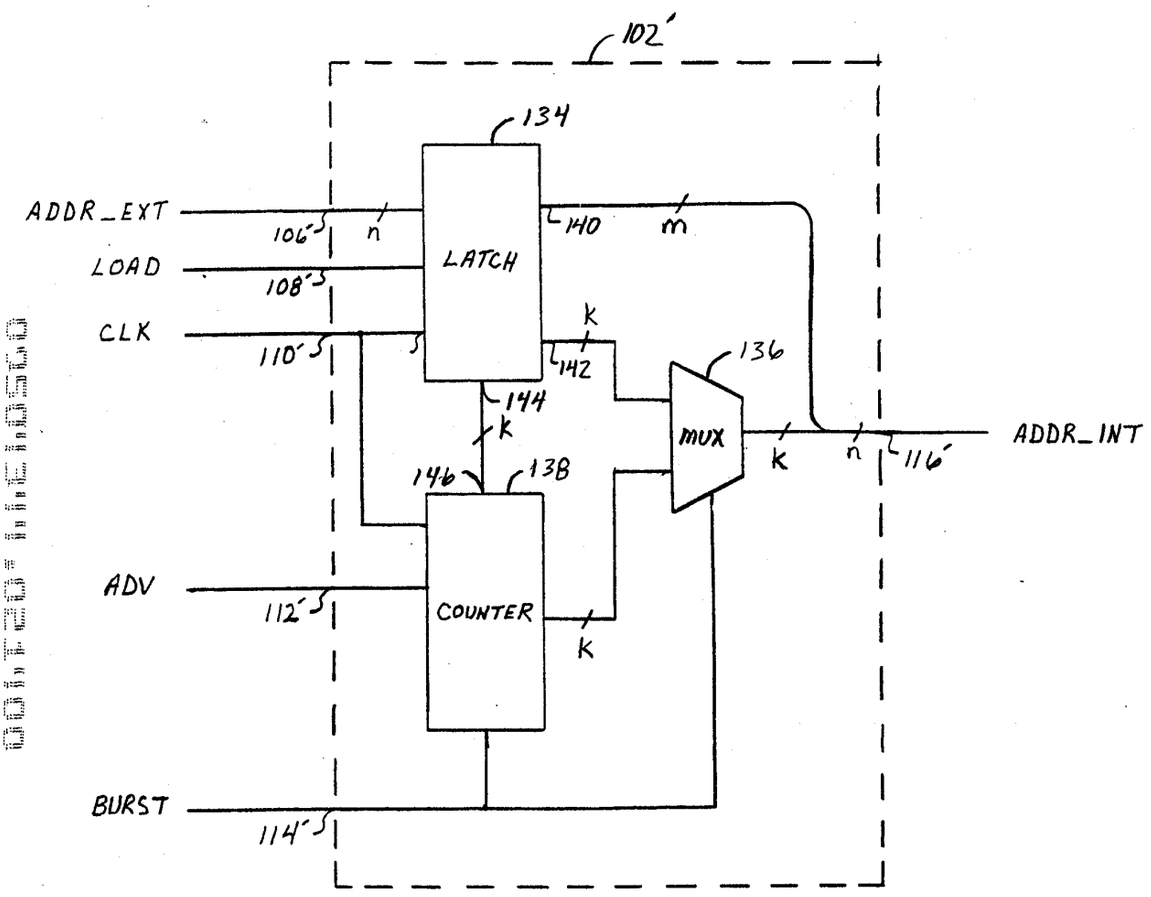


FIG.3

PRINT OF DRAWINGS
AS ORIGINALLY FILF

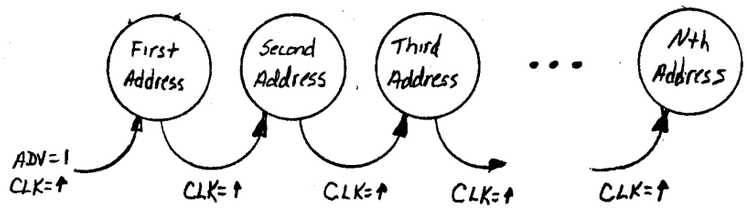


FIG. 4

PRINT OF DRAWINGS
AS ORIGINALLY FILF

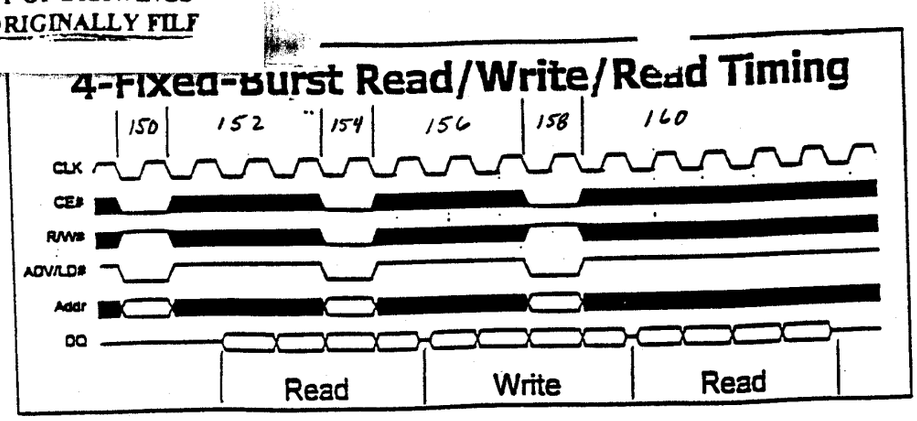


FIG. 5A

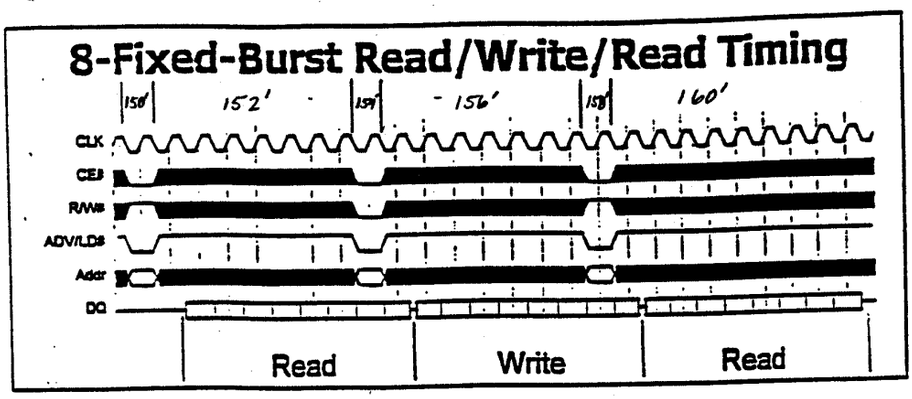


FIG. 5B

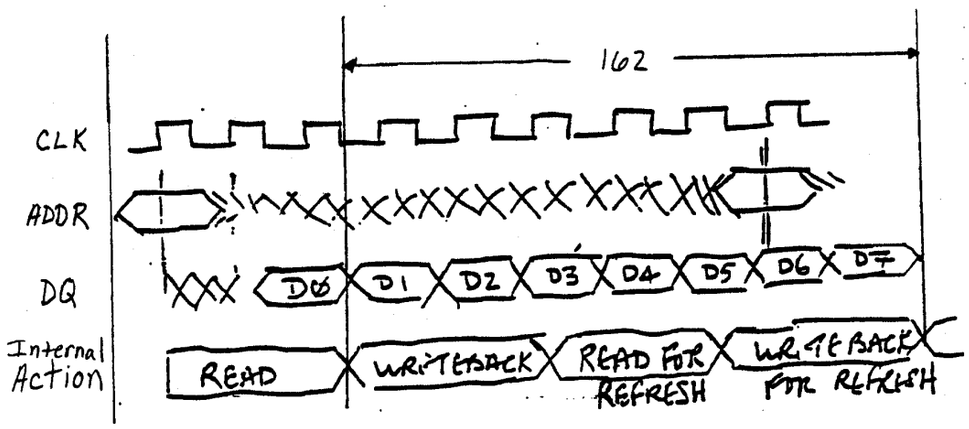


FIG. 6

Docket No. 0325.00309

DECLARATION, POWER OF ATTORNEY AND PETITION

I, the undersigned inventor, hereby declare that:

My residence, post office address and citizenship are given next to my name;

I believe that I am the first, original and sole inventor of the subject matter claimed in the application for patent entitled "**HIDDEN DRAM REFRESH IN FIXED BURST MEMORIES**", which:

_X_ is submitted herewith;

___ was filed on _____ as Application Serial No. _____ and amended on _____;

I have reviewed and understand the contents of the above-identified application for patent (hereinafter, "this application"), including the claims;

I acknowledge the duty under Title 37, Code of Federal Regulations, Section 1.56, to disclose to the United States Patent and Trademark Office information known to be material to the patentability of this application. I also acknowledge that information is material to patentability when it is not cumulative to information already provided to the United States Patent and Trademark Office and when it either

> compels, by itself or in combination with other information, a conclusion that a claim is unpatentable under the preponderance of evidence standard, giving each term in the claim its broadest reasonable construction consistent with the application, and before any consideration is given to evidence which may be submitted to establish a contrary conclusion of patentability, or
>
> refutes or is inconsistent with a position taken in either (i) asserting an argument of patentability, or (ii) opposing an argument of unpatentability relied on by the United States Patent and Trademark Office;

I hereby claim the priority benefit under Title 35, Section 119(e), of the following United States provisional patent applications:

Application No.	Filing Date

I hereby claim the priority benefit under Title 35, Section 120, of the following United States patent applications:

Serial No.	Filing Date	Status

Docket No. 0325.00309 Page 2 of 2

I hereby claim the priority benefit under Title 35, Section 365(c), of the following PCT International patent applications designating the United States:

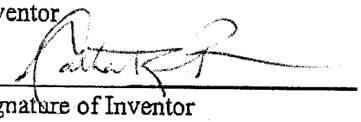
Application No.	Filing Date

Where the subject matter of the claims of this application is not disclosed in the United States or PCT priority patent applications identified above, I acknowledge the duty to disclose information known to be material to the patentability of this application that became available between the filing dates of this application and of the priority United States or PCT patent applications.

I hereby appoint as my attorneys with full power of substitution to prosecute this application and conduct all business in the United States Patent and Trademark Office associated with this application: Customer No. 021363.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.

Cathal G. Phelan
Inventor



Signature of Inventor

2/11/00
Date

Post Office Address:
394 Mountain View Ave.
Mountain View, CA 94041

Citizen of: Ireland
Residence: 394 Mountain View Ave.
Mountain View, CA 94041

GP2824 #2

Attorney's Docket No. 0325.00309 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Cathal G. Phelan		
Serial No.:	09/504,344	Art Unit:	2824
Filed:	February 14, 2000	Examiner:	
For:	FIXED BURST MEMORIES		

Assistant Commissioner For Patents
Washington, D.C. 20231

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT WITHIN THREE MONTHS OF FILING OR BEFORE MAILING OF FIRST OFFICE ACTION (37 CFR 1.97(b))

NOTE: "An information disclosure statement shall be considered by the Office if filed: (1) within three months of the filing date of a national application; (2) within three months of the date of entry of the national stage as set forth in § 1.491 in an international application; or (3) before the mailing date of a first Office action on the merits, whichever event occurs last." 37 CFR 1.97(b).

IDENTIFICATION OF TIME OF FILING THE ACCOMPANYING INFORMATION DISCLOSURE STATEMENT

The information disclosure statement submitted herewith is being filed within three months of the filing date of the application or date of entry into the national stage of an international application before the mailing date of a first Office action on the merits, whichever event occurs last. 37 CFR 1.97(b).

CHRISTOPHER P. MAIORANA, P.C.

Christopher P. Maiorana
Registration No. 42,829
24025 Greater Mack, Suite 200
St. Clair Shores, MI 48080
(810) 498-0670
Dated: May 8, 2000

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on May 8, 2000.

By: Mary Donna Berkley
Mary Donna Berkley

Sheet 1 of 1

Form PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO. 0325.00309	SERIAL NO. 09/504,344
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	APPLICANT: Cathal G. Phelan	
	FILING DATE February 14, 2000	GROUP ~~2824~~ 2187

OIPE MAY 11 2000 PATENT & TRADEMARK OFFICE

RECEIVED JUN 26 2000 TECH CENTER 2700

U.S. PATENT DOCUMENTS

Examiner Initial	Document No.	Date	Name	Class	Sub-Class	Filing Date

FOREIGN PATENT DOCUMENTS

	Document No.	Date	Country	Class	Sub-Class	Transl. Yes	Transl. No

OTHER DOCUMENTS (Incl. Author, Title, Date, Pertinent Pages, etc.)

AN	Understanding Burst Modes in Synchronous SRAMs, Cypress Semiconductor Corp., June 30, 1999.

Examiner	Date Considered 9/25/01

Examiner: Initial if references considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/504,344	02/14/00	PHELAN C	0325.000309

021363
CHRISTOPHER P. MAIORANA, P.C.
24025 GREATER MACK
SUITE 200
ST. CLAIR SHORES MI 48080

TM02/1002

EXAMINER	
NAMAZI,M	
ART UNIT	PAPER NUMBER
2187	3

DATE MAILED: 10/02/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95)
*U.S. GPO: 2000-473-000/44602

1- File Copy

Office Action Summary

Application No.	Applicant(s)
09/504,344	Phelan
Examiner	**Art Unit**
Mehdi Namazi	2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *three* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Feb 14, 2000*

2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-17* is/are pending in the applica

4a) Of the above, claim(s) _____ is/are withdrawn from considera

5) ☐ Claim(s) _____ is/are allowed.

6) ☐ Claim(s) _____ is/are rejected.

7) ☒ Claim(s) *1-17* is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 2

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

1. Claims 1-17 are presented for examination. This office action is in response to the application filed 02/14/2000.

In the Title

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. It appears --A memory device that transfers a fixed number of words of data with non-interruptible burst-- or other similar language(see claim 1, specification, pages 1 and 9, e.g.). The loss in brevity of title is more than offset by the gain in its informative value in indexing, classifying, searching, etc. See MPEP 606 and 606.01.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 6 and 15 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in

the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As per claims 6 and 15, the specification does not provide support for limitation such as *bond options*.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

6. Claims 1-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Yip et al.(YIP)(U.S.Patent No. 6,289,138).

As per claims 1 and 12-13 Yip teaches an integrated circuit comprising: a memory comprising a plurality of storage elements each configured to read and write data in response to an internal address signal(fig. 144B, element 230); and a logic circuit configured to generate a predetermined number of said internal address signals in response to (I) an external address signal(fig. 144A, "ext_addr"), (ii) a clock signal(inherent) and

(iii) one or more control signals(col. 2, lines 15-20), wherein said generation of said predetermined number of internal address signals is non-interruptible(col. 115, lines 60-64).

As per claims 2, Yip teaches wherein said predetermine number of internal address signals is determined by a fixed burst length(col. 115, lines 62-63).

As per claims 3-4 and 14, Yip teaches wherein said predetermined number of internal address signals are 4 or 8(col. 115, lines 62-63 teaches preset number of words, which means preset numbers of internal signals).

As per claim 5, Yip teaches wherein said fixed burst length is programmable(col. 109, lines 35-43).

As per claims 6 and 15, Yip teaches wherein said fixed burst length is programmed by bond options(col. 109, lines 35-43).

As per claims 7 and 16, Yip teaches wherein said fixed burst length is programmed by voltage levels on external pins(it is inherent to have voltage levels for each burst).

As per claim 8, Yip teaches wherein said memory comprises a static random access memory(fig. 1, element 230).

As per claim 9, Yip teaches wherein said memory comprises a dynamic random access memory(fig. 146, element 1910).

As per claims 10 and 17, Yip teaches wherein said predetermined number of internal address signals is chosen to provide time for writeback and refresh cycles(it is inherent to have time included for writeback and refresh cycle during each burst).

As per claim 11, Yip teaches wherein said predetermined number of internal address signals is chosen to meet predetermined criteria for sharing address and control busses(col. 115, lines 62-63).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 5,651,138(Le et al.) Teaches data processor with controlled burst memory accesses and method therefor.

U.S. Patent 5,805,928(Lee) Teaches burst length detection circuit for detecting a burst end time point and generating a burst mode signal without using a conventional burst length detection counter.

U.S. Patent 5,936,975(Okamura) Teaches semiconductor memory device with switching circuit for controlling internal addresses in parallel test.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mehdi Namazi whose telephone number is (703) 306-2758. The examiner can normally be reached on Monday-Thursday from 7:00 to 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do Hyun yoo, can be reached on (703) 308-4908.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-9600.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 746-7239 (for formal communications intended for entry)

Or:

(703) 746-7240 (for informal or draft communications, please label PROPOSED or DRAFT)

Hand-delivered responses should be brought to Crystal Park 2,

2121 Crystal Drive,

Arlington, VA., Sixth Floor (Receptionist).

M. Namazi
October 1, 2001

DO HYUN YOO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

FORM PTO-892 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	SERIAL NO.	GROUP ART UNIT	ATTACHMENT TO PAPER NO.	
NOTICE OF REFERENCES CITED	09/504,344	2187		3
	APPLICANT(S) Phelan			

U.S. PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	A	5,651,138	7/1997	Le et al.	711	154	
	B	5,805,928	9/1998	Lee	710	35	
	C	5,936,975	8/1999	Okamura	714	719	
	D	6,289,138	9/2001	Yip et al.	382	307	
	E	6,085,261	7/2000	McIntyre, Jr. et al.	710	35	
	F						
	G						
	H						
	I						
	J						
	K						

FOREIGN PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS
	L						
	M						
	N						
	O						
	P						
	Q						

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

	R	
	S	
	T	
	U	

EXAMINER	DATE	
Mehdi Namazi	September 27, 2001	Form892ccs2106b

* A copy of this reference is not being furnished with this office action.
(See Manual of Patent Examining Procedure, section 707.05(a).)

Form PTO 948 (Rev. 8-98) U.S. DEPARTMENT OF COMMERCE - Patent and Trademark Office Application No. 09/504344

NOTICE OF DRAFTSPERSON'S PATENT DRAWING REVIEW

The drawing(s) filed (insert date) 2/14/00 are:

A. ☐ approved by the Draftsperson under 37 CFR 1.84 or 1.152.

B. ☒ objected to by the Draftsperson under 37 CFR 1.84 or 1.152 for the reasons indicated below. The Examiner will require submission of new, corrected drawings when necessary. Corrected drawing must be sumitted according to the instructions on the back of this notice.

1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings: Black ink. Color.
   - ____ Color drawings are not acceptable until petition is granted. Fig(s) ____
   - ____ Pencil and non black ink not permitted. Fig(s) ____
2. PHOTOGRAPHS. 37 CFR 1.84 (b)
   - ____ 1 full-tone set is required. Fig(s) ____
   - ____ Photographs not properly mounted (must use brystol board or photographic double-weight paper). Fig(s) ____
   - ____ Poor quality (half-tone). Fig(s) ____
3. TYPE OF PAPER. 37 CFR 1.84(e)
   - ____ Paper not flexible, strong, white, and durable. Fig(s) ____
   - ____ Erasures, alterations, overwritings, interlineations, folds, copy machine marks not accepted. Fig(s) ____
   - ____ Mylar, velum paper is not acceptable (too thin). Fig(s) ____
4. SIZE OF PAPER. 37 CFR 1.84(f): Acceptable sizes:
   - ____ 21.0 cm by 29.7 cm (DIN size A4)
   - ____ 21.6 cm by 27.9 cm (8 1/2 x 11 inches)
   - ____ All drawing sheets not the same size. Sheet(s) ____
   - ____ Drawings sheets not an acceptable size. Fig(s) ____
5. MARGINS. 37 CFR 1.84(g): Acceptable margins:

   Top 2.5 cm Left 2.5cm Right 1.5 cm Bottom 1.0 cm
   SIZE: A4 Size

   Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm
   SIZE: 8 1/2 x 11

   Margins not acceptable. Fig(s) 2, 3, 5A
   - ☒ Top (T) ☒ Left (L)
   - ____ Right (R) ____ Bottom (B)
6. VIEWS. 37 CFR 1.84(h)

   REMINDER: Specification may require revision to correspond to drawing changes.

   Partial views. 37 CFR 1.84(h)(2)
   - ____ Brackets needed to show figure as one entity. Fig(s) ____
   - ____ Views not labeled separately or properly. Fig(s) ____
   - ____ Enlarged view not labeled separetely or properly. Fig(s) ____
7. SECTIONAL VIEWS. 37 CFR 1.84 (h)(3)
   - ____ Hatching not indicated for sectional portions of an object. Fig(s) ____
   - ____ Sectional designation should be noted with Arabic or Roman numbers. Fig(s) ____
8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)
   - ____ Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned so that the top becomes the right side, except for graphs. Fig(s) ____
9. SCALE. 37 CFR 1.84(k)
   - ____ Scale not large enough to show mechanism without crowding when drawing is reduced in size to two-thirds in reproduction. Fig(s) ____
10. CHARACTER OF LINES, NUMBERS, & LETTERS. 37 CFR 1.84(i)
    - ☒ Lines, numbers & letters not uniformly thick and well defined, clean, durable, and black (poor line quality). Fig(s) 1-6
11. SHADING. 37 CFR 1.84(m)
    - ____ Solid black areas pale. Fig(s) ____
    - ____ Solid black shading not permitted. Fig(s) ____
    - ____ Shade lines, pale, rough and blurred. Fig(s) ____
12. NUMBERS, LETTERS, & REFERENCE CHARACTERS. 37 CFR 1.84(p)
    - ____ Numbers and reference characters not plain and legible. Fig(s) ____
    - ____ Figure legends are poor. Fig(s) ____
    - ____ Numbers and reference characters not oriented in the same direction as the view. 37 CFR 1.84(p)(1) Fig(s) ____
    - ____ English alphabet not used. 37 CFR 1.84(p)(2) Figs ____
    - ☒ Numbers, letters and reference characters must be at least .32 cm (1/8 inch) in height. 37 CFR 1.84(p)(3) Fig(s) 1-6
13. LEAD LINES. 37 CFR 1.84(q)
    - ____ Lead lines cross each other. Fig(s) ____
    - ____ Lead lines missing. Fig(s) ____
14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.84(t)
    - ____ Sheets not numbered consecutively, and in Arabic numerals beginning with number 1. Sheet(s) ____
15. NUMBERING OF VIEWS. 37 CFR 1.84(u)
    - ____ Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig(s) ____
16. CORRECTIONS. 37 CFR 1.84(w)
    - ____ Corrections not made from prior PTO-948 dated ____
17. DESIGN DRAWINGS. 37 CFR 1.152
    - ____ Surface shading shown not appropriate. Fig(s) ____
    - ____ Solid black shading not used for color contrast. Fig(s) ____

COMMENTS

REVIEWER B.D DATE 9/27/01 TELEPHONE NO. ____

ATTACHMENT TO PAPER NO. 3

Attachment for PTO-948 (Rev. 03/01, or earlier)
6/18/01

The below text replaces the pre-printed text under the heading, "Information on How to Effect Drawing Changes," on the back of the PTO-948 (Rev. 03/01, or earlier) form.

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

1. Correction of Informalities -- 37 CFR 1.85

New corrected drawings must be filed with the changes incorporated therein. Identifying indicia, if provided, should include the title of the invention, inventor's name, and application number, or docket number (if any) if an application number has not been assigned to the application. If this information is provided, it must be placed on the front of each sheet and centered within the top margin. If corrected drawings are required in a Notice of Allowability (PTOL-37), the new drawings **MUST** be filed within the **THREE MONTH** shortened statutory period set for reply in the Notice of Allowability. Extensions of time may NOT be obtained under the provisions of 37 CFR 1.136(a) or (b) for filing the corrected drawings after the mailing of a Notice of Allowability. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

2. Corrections other than Informalities Noted by Draftsperson on form PTO-948.

All changes to the drawings, other than informalities noted by the Draftsperson, **MUST** be made in the same manner as above except that, normally, a highlighted (preferably red ink) sketch of the changes to be incorporated into the new drawings **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes.

Timing of Corrections

Applicant is required to submit the drawing corrections within the time period set in the attached Office communication. See 37 CFR 1.85(a).

Failure to take corrective action within the set period will result in **ABANDONMENT** of the application.

06/01/01

COPY OF PAPERS ORIGINALLY FILED

Attorn Docket: 0325.003

IN RE APPLICATION OF: Cathal G. Phelan

SERIAL NO: 09/504,344

TITLE: FIXED BURST MEMORIES

FILED: February 14, 2000

EXAMINER: Namzai, M.

ART UNIT: 2187

RESPONSE TRANSMITTAL AND EXTENSION OF TIME REQUEST (IF REQUIRED)

#4 Ext of time 2-26-02 DC

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Sir:

Enclosed please find an amendment, copies of three patents and a postcard along with the fee calculation below:

FEE CALCULATION FOR ENCLOSED AND EXTENSION REQUEST (IF ANY)

	Claims Remaining	Highest No. Previous	Extra	Rate	Additional Fee
Total Claims	20 minus	20 =	0	x $ 18.00	$ 0.00
Independent Claims	3 minus	3 =	0	x $ 84.00	$ 0.00
Multiple Dependent Claim First Added				+ $280.00	$ 0.00

TOTAL IF NOT SMALL ENTITY .. $0.00

[ ] SMALL ENTITY STATUS - If applicable, divide by 2 ..... $0.00
[ ] Verified statement enclosed, if not previously filed.

[X] Applicant also requests a one month extension of time for response to the outstanding Office Action. The fee is $110.00

[ ] Fee set forth in 37 C.F.R. 1.17 (p) for Information Disclosure under 37 C.F.R. 1.97 (c) $0.00

TOTAL FEE $110.00

The Commissioner is hereby authorized to charge any overpayment or underpayment of the above fee associated with this Communication to Deposit Account No. 50-0541. A duplicate copy of this sheet is attached.

CHRISTOPHER P. MAIORANA, P.C.

24025 Greater Mack, Suite 200
St. Clair Shores, Michigan 48080
(586) 498-0670

By: _____
Christopher P. Maiorana
Registration No.: 42,829

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on February 4, 2002.

By: Mary Donna Berkley
Mary Donna Berkley

02/21/2002 BNGUYEN1 00000033 09504344
01 FC:115 110.00 OP

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#5/a amdt 2-26-02 OC

Application of: Cathal G. Phelan

Serial No.: 09/504,344

Title: FIXED BURST MEMORIES

Filed: February 14, 2000

Attorney Docket No.: 0325.00309

Examiner: Namzai, M.

Art Unit: 2187

In Response To: Office Action mailed October 2, 2001

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on February 4, 2002.

By: Mary Donna Berkley
Mary Donna Berkley

AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action mailed October 2, 2001 please amend the above-identified application as follows:

IN THE SPECIFICATION

Please replace the title with the following:

1a'

MEMORY DEVICE WITH FIXED LENGTH NON-INTERRUPTIBLE BURST

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please replace the title with the following:

[FIXED BURST MEMORIES] MEMORY DEVICE WITH FIXED LENGTH NON-INTERRUPTIBLE BURST

IN THE CLAIMS

Please amend the claims as follows:

1. (AMENDED) A circuit comprising:

a memory comprising a plurality of storage elements each configured to read and write data in response to an internal address signal; and

a logic circuit configured to generate a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

2. (AMENDED) The circuit according to claim 1, wherein said predetermined number of internal address signals is determined by a fixed burst length.

3. (AMENDED) The circuit according to claim 1, wherein said predetermined number of internal address signals is at least 4.

4. (AMENDED) The circuit according to claim 1, wherein said predetermined number of internal address signals is 8.

5. (AMENDED) The circuit according to claim 2, wherein said fixed burst length is programmable.

6. (AMENDED) The circuit according to claim 5, wherein said fixed burst length is programmed by bond options.

7. (AMENDED) The circuit according to claim 5, wherein said fixed burst length is programmed by voltage levels on external pins.

8. (AMENDED) The circuit according to claim 1, wherein said memory comprises a static random access memory.

9. (AMENDED) The circuit according to claim 1, wherein said memory comprises a dynamic random access memory.

10. (AMENDED) The circuit according to claim 9, wherein said predetermined number of internal address signals is chosen to provide time for at least one writeback or refresh cycle.

11. (AMENDED) The circuit according to claim 1, wherein said predetermined number of internal address signals is chosen to meet predetermined criteria for sharing address and control busses.

12. (AMENDED) A circuit comprising:

means for reading data from and writing data to a plurality of storage elements in response to a plurality of internal address signals; and

means for generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

13. (AMENDED) A method of providing a fixed burst length data transfer comprising the steps of:

accessing a memory in response to a plurality of internal address signals; and

generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) a control signal, wherein said generation of said predetermined number of internal address signals is non-interruptible.

14. The method according to claim 13, further comprising the step of programming said predetermined number.

15. The method according to claim 14, wherein said programming step is performed using bond options.

16. The method according to claim 14, wherein said programming step is performed using voltage levels.

17. (AMENDED) The method according to claim 13, further comprising the step of selecting said predetermined number to provide time for at least one writeback or refresh cycle.

Please add the following new claims:

18. (NEW) The circuit according to claim 1, wherein said logic circuit comprises a counter configured to generate said predetermined number of internal address signals.

19. (NEW) The circuit according to claim 1, wherein said external address signal comprises an initial address for data transfers to an from said memory.

20. (NEW) A memory device according to claim 1, wherein said circuit is an integrated circuit.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (AMENDED) [An integrated] A circuit comprising:

a memory comprising a plurality of storage elements each configured to read and write data in response to an internal address signal; and

a logic circuit configured to generate a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

2. (AMENDED) The [integrated] circuit according to claim 1, wherein said [predetermine] predetermined number of internal address signals is determined by a fixed burst length.

3. (AMENDED) The [integrated] circuit according to claim 1, wherein said predetermined number of internal address signals is at least 4.

4. (AMENDED) The [integrated] circuit according to claim 1, wherein said predetermined number of internal address signals is 8.

5. (AMENDED) The [integrated] circuit according to claim 2, wherein said fixed burst length is programmable.

6. (AMENDED) The [integrated] circuit according to claim 5, wherein said fixed burst length is programmed by bond options.

7. (AMENDED) The [integrated] circuit according to claim 5, wherein said fixed burst length is programmed by voltage levels on external pins.

8. (AMENDED) The [integrated] circuit according to claim 1, wherein said memory comprises a static random access memory.

9. (AMENDED) The [integrated] circuit according to claim 1, wherein said memory comprises a dynamic random access memory.

10. (AMENDED) The [integrated] circuit according to claim 9, wherein said predetermined number of internal address signals is chosen to provide time for at least one writeback [and] or refresh [cycles] cycle.

11. (AMENDED) The [integrated] circuit according to claim 1, wherein said predetermined number of internal address signals is chosen to meet predetermined criteria for sharing address and control busses.

12. (AMENDED) [An integrated] A circuit comprising:

means for reading data from and writing data to a plurality of storage elements in response to [an] a plurality of internal address [signal] signals; and

means for generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

13. (AMENDED) A method of providing a fixed burst length data transfer comprising the steps of:

[reading from and writing data to] accessing a memory in response to [an] a plurality of internal address [signal] signals; and

generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) a control signal, wherein said generation

of said predetermined number of internal address signals is non-interruptible.

17. (AMENDED) The method according to claim 13, further comprising the step of selecting said predetermined number to provide time for at least one writeback [and] or refresh [cycles] cycle.

18. (NEW) The circuit according to claim 1, wherein said logic circuit comprises a counter configured to generate said predetermined number of internal address signals.

19. (NEW) The circuit according to claim 1, wherein said external address signal comprises an initial address for data transfers to an from said memory.

20. (NEW) A memory device according to claim 1, wherein said circuit is an integrated circuit.

R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns an integrated circuit comprising a memory and a logic circuit. The memory may comprise a plurality of storage elements each configured to read and write data in response to an internal address signal. The logic circuit may be configured to generate a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals. The generation of the predetermined number of internal address signals is non-interruptible.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims and new claims 18-20 may be found in the drawings (e.g., FIGS. 1-6) and the specification (e.g., page 5, lines 2-14 and page 6, line 19 thru page 8, line 2) as originally filed. As such, no new matter has been added.

OBJECTION TO THE TITLE

The objection to the title has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claims 6 and 15 under 35 U.S.C. §112, second paragraph, is respectfully traversed and should be withdrawn.

Support for claims 6 and 15 may be found on page 8, lines 3-8 of the specification. Furthermore, bond options are well known in the art and, therefore, one skilled in the art would understand how to make and/or use bond options. Copies of U.S. patents 6,188,636 (issued February 13, 2001), 5,900,021 (issued May 4, 1999) and 5,360,992 (issued November 1, 1994) from the USPTO web site (www.uspto.gov) are attached as evidence of bond options being well known in the art.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-17 under 35 U.S.C. §102(e) as being anticipated by Yip et al. '138 (hereinafter Yip) is respectfully traversed and should be withdrawn.

Yip discloses a general image processor (Title). The image processor includes a raster image coprocessor with a cache memory (elements 224 and 230 of FIG. 1 of Yip) connected to an external DRAM (element 1910 of FIG. 146 of Yip) via a local memory controller and an external interface (see FIG. 2). Accesses to the cache 230 and the external DRAM 1910 are interruptible (see column

54, lines 42-47, column 115, lines 26-29 and lines 52-55 and column 116, lines 20-22 of Yip).

In contrast, the present invention provides a logic circuit configured to generate a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, where **the generation of the predetermined number of internal address signals is non-interruptible**. Assuming, *arguendo*, that the cache 230 of Yip is similar to the presently claimed memory (as suggested by the Office Action in the last paragraph on page 3 and for which Applicants' representative does not necessarily agree), Yip does not disclose or suggest the generation of a predetermined number of internal address signals that is non-interruptible, as presently claimed. As such, the present invention is fully patentable over the cited reference and the rejection should be withdrawn.

In particular, during an access of the cache 230, Yip teaches that when a cache miss occurs the cache access is stalled until all the values needed are read from an external memory and stored in the cache (column 54, lines 42-47 of Yip). Since the access to the cache 230 can be stalled and writing of updated data to the cache must be accommodated, it follows that the generation of addresses for accessing the cache 230 is interruptible. Yip

teaches a cache access that can be stalled. Yip fails to disclose or suggest the generation of a predetermined number of internal address signals that is **non-interruptible**, as presently claimed. As such, the present invention is fully patentable over the cited reference and the rejection should be withdrawn.

Furthermore, assuming, *arguendo*, that the external DRAM 1910 of Yip is similar to the presently claimed memory (as suggested by the Office Action on page 4, lines 20-21 and for which Applicants' representative does not necessarily agree), Yip still does not disclose or suggest the generation of a predetermined number of internal address signals that is non-interruptible, as presently claimed. As such, the present invention is fully patentable over the cited reference and the rejection should be withdrawn.

Specifically, Yip teaches that a write burst to the DRAM 1910 can be interrupted when there is a cycle request from a higher priority port (column 115, lines 26-29 of Yip). Similarly, Yip teaches that a read burst will be terminated when a higher priority DRAM request is received (column 115, lines 52-55 of Yip). Since Yip teaches that a burst can be interrupted, Yip fails to disclose or suggest the generation of a predetermined number of internal address signals that is non-interruptible, as presently claimed.

As such, the present invention is fully patentable over the cited reference and the rejection should be withdrawn.

Despite the suggestion of the Office Action on page 4, lines 1-3, Yip does not disclose or suggest generating a predetermined number of internal address signals that is **non-interruptible**, as presently claimed. Restricting rearbitration for the DRAM 1910 so that an interruptible burst is not interrupted until a preset number of data words have been transferred (see column 115, lines 60-64 of Yip) is not the same as generating a predetermined number of internal address signals that is **non-interruptible**, as presently claimed. Therefore, Yip does not disclose or suggest generating a predetermined number of internal address signals that is **non-interruptible**, as presently claimed. As such, the present invention is fully patentable over the cited reference and the rejection should be withdrawn.

New claims 18-20 depend directly from independent claim 1, which is believed to be allowable, and, therefore, are fully patentable over the cited reference.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.

Christopher P. Maiorana
Registration No. 42,829
24025 Greater Mack, Suite 200
St. Clair Shores, MI 48080
(586) 498-0670

Dated: February 4, 2002

Docket No.: 0325.00309

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/504,344	02/14/2000	Cathal G. Phelan	0325.000309	7771

21363 7590 04/25/2002

CHRISTOPHER P. MAIORANA, P.C.
24025 GREATER MACK
SUITE 200
ST. CLAIR SHORES, MI 48080

EXAMINER	
NAMAZI, MEHDI	
ART UNIT	**PAPER NUMBER**
2187	6

DATE MAILED: 04/25/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

Office Action Summary	Application No. 09/504,344	Applicant(s) Phelan
	Examiner Mehdi Namazi	Art Unit 2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *three* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Feb 14, 2002*

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-20* is/are pending in the applica

4a) Of the above, claim(s) _____ is/are withdrawn from considera

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-20* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☐ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

1. This office action is in response to the amendment filed February 14, 2002 (Amendment A).

2. Claims 1-17 are presented for further examination in view of the foregoing amendments and remarks. Claims 1-13, and 17 have been amended. No claim has been canceled. New claims 18-20 have been added. Therefore, claims 1-20 are pending.

Response to Arguments

3. Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

4. Claim 19 is objected to because of the following informalities:

As per claim 19, line 3, replace "an" with --and--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims ~~1-17~~ 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Cowles(U.S.Patent No. 5,729,504).

As per claims 1 and 12-13 Cowles teaches a circuit comprising: a memory comprising a plurality of storage elements each configured to read and write data in response to an internal address signal(fig. 1, element 12); and a logic circuit configured to generate a predetermined number of said internal address signals in response to (I) an external address signal (col. 2, lines 20-21), (ii) a clock signal(col. 9, lines 59-61) and (iii) one or more control signals(fig. 1, element 38, produce control signal), wherein said generation of said predetermined number of internal address signals is non-interruptible(col. 8, lines 18-22).

As per claims 2, Cowles teaches wherein said predetermine number of internal address signals is determined by a fixed burst length(col. 5, lines 47-53).

As per claims 3-4 and 14, Cowles teaches wherein said predetermined number of internal address signals are 4 or 8(fig. 2, shows various burst length of 2, 4, and 8).

As per claim 5, Cowles teaches wherein said fixed burst length is programmable(col. 5, lines 31-34).

As per claims 6 and 15, Cowles teaches wherein said fixed burst length is programmed by bond options(it is well known in the art to include multiple modes of operation selected by bond options).

As per claims 7 and 16, Cowles teaches wherein said fixed burst length is programmed by voltage levels on external pins(it is inherent to have voltage levels for each burst).

As per claim 8, Cowles teaches wherein said memory comprises a static random access memory(fig. 1, element 12).

As per claim 9, Cowles teaches wherein said memory comprises a dynamic random access memory(fig. 1, element 12).

As per claims 10 and 17, Cowles teaches wherein said predetermined number of internal address signals is chosen to provide time for at least one writeback or refresh cycle(it is

inherent to have time included for writeback and refresh cycle during each burst).

As per claim 11, Cowles teaches wherein the predetermined number of internal address signals is chosen to meet predetermined criteria for sharing address and control busses (col. 8, lines 18-22).

As per claim 18, Cowles teaches wherein the logic circuit comprises a counter configured to generate the predetermined number of internal address signals(fig. 1, element 26).

As per claim 19, Cowles teaches wherein the external address signal comprises an initial address for data transfers to and from the memory(col. 2, lines 21-22).

As per claim 20, Cowles teaches wherein the circuit is an integrated circuit(abstract).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent (5,966,724)(Ryan) Teaches synchronous memory device with dual page and burst mode operations.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mehdi

Namazi whose telephone number is (703) 306-2758. The examiner can normally be reached on Monday-Thursday from 7:00 to 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do Hyun yoo, can be reached on (703) 308-4908.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-9600.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 746-7239 (for formal communications intended for entry)

Or:

(703) 746-7240 (for informal or draft communications, please label PROPOSED or DRAFT)

Hand-delivered responses should be brought to Crystal Park 2, 2121 Crystal Drive,

Arlington, VA., Sixth Floor (Receptionist).

M. Namazi
April 21, 2002

DO HYUN YOO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

FORM PTO-892 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	SERIAL NO. 09/504,344	GROUP ART UNIT 2187	ATTACHMENT TO PAPER NO.	6
NOTICE OF REFERENCES CITED	APPLICANT(S) Phelan			

U.S. PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	A	5,729,504	3/1998	Cowles	365	236	
	B	5,966,724	10/1999	Ryan	711	105	
	C						
	D						
	E						
	F						
	G						
	H						
	I						
	J						
	K						

FOREIGN PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS
	L						
	M						
	N						
	O						
	P						
	Q						

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

	R	
	S	
	T	
	U	

EXAMINER	DATE	
Mehdi Namazi	April 21, 2002	Form892ccs2106b

* A copy of this reference is not being furnished with this office action.
(See Manual of Patent Examining Procedure, section 707.05(a).)

7/16
SR
7-23-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Cathal G. Phelan
Serial No.:	09/504,344
Title:	MEMORY DEVICE WITH FIXED LENGTH NON-INTERRUPTIBLE BURST
Filed:	February 14, 2000
Attorney Docket No.:	0325.00309
Examiner:	Namazi, M.
Art Unit:	2187
In Response To:	Office Action mailed April 25, 2002

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on June 26, 2002 .

By: Mary Donna Berkley
Mary Donna Berkley

AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action mailed April 25, 2002 please amend the above-identified application as follows:

IN THE CLAIMS

Please amend the claims as follows:

1. (AMENDED) A circuit comprising:

Sub C1

a memory comprising a plurality of storage elements each configured to read and write data in response to an internal address signal; and

a logic circuit configured to generate a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

2. (AMENDED) The circuit according to claim 1, wherein said predetermined number of internal address signals is determined by a fixed burst length.

3. (AMENDED) The circuit according to claim 1, wherein said predetermined number of internal address signals is at least 4.

4. (AMENDED) The circuit according to claim 1, wherein said predetermined number of internal address signals is 8.

5. (AMENDED) The circuit according to claim 2, wherein said fixed burst length is programmable.

6. (AMENDED) The circuit according to claim 5, wherein said fixed burst length is programmed by bond options.

7. (AMENDED) The circuit according to claim 5, wherein said fixed burst length is programmed by voltage levels on external pins.

8. (AMENDED) The circuit according to claim 1, wherein said memory comprises a static random access memory.

9. (AMENDED) The circuit according to claim 1, wherein said memory comprises a dynamic random access memory.

10. (AMENDED) The circuit according to claim 9, wherein said predetermined number of internal address signals is chosen to provide time for at least one writeback or refresh cycle.

11. (AMENDED) The circuit according to claim 1, wherein said predetermined number of internal address signals is chosen to meet predetermined criteria for sharing address and control busses.

12. (AMENDED) A circuit comprising:

means for reading data from and writing data to a plurality of storage elements in response to a plurality of internal address signals; and

means for generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

13. (AMENDED) A method of providing a fixed burst length data transfer comprising the steps of:

accessing a memory in response to a plurality of internal address signals; and

generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) a control signal, wherein said generation of said predetermined number of internal address signals is non-interruptible.

14. The method according to claim 13, further comprising the step of programming said predetermined number.

15. The method according to claim 14, wherein said programming step is performed using bond options.

16. The method according to claim 14, wherein said programming step is performed using voltage levels.

17. (AMENDED) The method according to claim 13, further comprising the step of selecting said predetermined number to provide time for at least one writeback or refresh cycle.

18. The circuit according to claim 1, wherein said logic circuit comprises a counter configured to generate said predetermined number of internal address signals.

19. (AMENDED) The circuit according to claim 1, wherein said external address signal comprises an initial address for data transfers to and from said memory.

20. A memory device according to claim 1, wherein said circuit is an integrated circuit.

Please add the following new claim:

21. (NEW) The circuit according to claim 1, further comprising an address and control bus configured to present said external address signal and said one or more control signals, wherein said bus is freed up during the generation of said predetermined number of internal address signals.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

19. (AMENDED) The circuit according to claim 1, wherein said external address signal comprises an initial address for data transfers to [an] and from said memory.

21. (NEW) The circuit according to claim 1, further comprising an address and control bus configured to present said external address signal and said one or more control signals, wherein said bus is freed up during the generation of said predetermined number of internal address signals.

R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns an integrated circuit comprising a memory and a logic circuit. The memory may comprise a plurality of storage elements each configured to read and write data in response to an internal address signal. The logic circuit may be configured to generate a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals. The generation of the predetermined number of internal address signals is non-interruptible.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims can be found in the drawing as originally filed, for example, FIGS. 5A, 5B and 6, and in the specification as originally filed, for example, on page 9, lines 3-11. As such, no new matter has been added.

OBJECTION TO THE CLAIMS

The objection to claim 19 has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-20 under 35 U.S.C. §102(b) as being anticipated by Cowles is respectfully traversed and should be withdrawn.

Cowles is directed to a continuous burst EDO memory device (Title). Cowles does not disclose or suggest generating a predetermined number of internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, where the generation of the predetermined number of internal address signals is **non-interruptible**, as presently claimed.

In contrast, the present invention (claim 1) provides a circuit comprising a memory comprising a plurality of storage elements each configured to read and write data in response to an internal address signal and a logic circuit configured to generate a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals. The generation of the predetermined number of internal address signals is **non-interruptible**. Claims 12 and 13 recite similar limitations.

Assuming, *arguendo*, that the memory array 12 of Cowles is similar to the presently claimed memory (as suggested by the Office Action in section no. 6, on page 3 and for which Applicants'

representative does not necessarily agree), Cowles does not disclose or suggest the generation of a predetermined number of internal address signals that is non-interruptible, as presently claimed. As such, the present invention is fully patentable over the cited reference and the rejection should be withdrawn.

In particular, Cowles teaches that a continuous burst read operation can be **terminated** "merely" by a low to high transition of the write enable signal WE* prior to a falling edge of the CAS* signal (column 8, lines 32-36 of Cowles). Since the burst read operation can be **terminated**, it follows that the generation of addresses for accessing the memory array of Cowles is **interruptible**. Cowles teaches a burst read access that can be terminated. Cowles fails to disclose or suggest the generation of a predetermined number of internal address signals that is **non-interruptible**, as presently claimed. As such, the present invention is fully patentable over the cited reference and the rejection should be withdrawn.

Furthermore, Cowles teaches that a low to high transition of the WE* signal within a burst write access to the memory array 112 will **terminate** the burst access, preventing further writes from occurring (column 7, lines 36-38 of Cowles). Likewise, a high to low transition of the WE* signal within a burst read access will **terminate** the burst read access (column 7, lines 38-41 of Cowles).

Similarly, Cowles teaches that control circuitry can **terminate** a data burst based upon the states of signals CAS*, RAS* and WE* (column 7, lines 50-61 of Cowles). Since Cowles teaches that a burst can be terminated, Cowles fails to disclose or suggest the generation of a predetermined number of internal address signals that is **non-interruptible**, as presently claimed. As such, the present invention is fully patentable over the cited reference and the rejection should be withdrawn.

Despite the suggestion of the Office Action on page 3, paragraph no. 6, Cowles does not disclose or suggest generating a predetermined number of internal address signals that is **non-interruptible**, as presently claimed. Therefore, Cowles does not disclose or suggest each and every element of the presently pending claims, arranged as in the presently pending claims. As such, the present invention is fully patentable over the cited reference and the rejection should be withdrawn.

New claim 21 depends directly from claim 1, which is believed to be fully patentable over the cited reference, and, therefore, is also believed to be fully patentable over the cited reference.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.

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Dated: June 26, 2002

Docket No.: 0325.00309

GP 2187

COPY OF PAPERS ORIGINALLY FILED

Attorney Docket: 0325.00309

IN RE APPLICATION OF: Cathal G. Phelan

SERIAL NO.: 09/504,344

TITLE: FIXED BURST MEMORIES

FILED: February 14, 2000

EXAMINER: Namzai, M.

ART UNIT: 2187

RESPONSE TRANSMITTAL AND EXTENSION OF TIME REQUEST (IF REQUIRED)

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Sir:

Enclosed please find an amendment and a postcard along with the fee calculation below:

FEE CALCULATION FOR ENCLOSED AND EXTENSION REQUEST (IF ANY)

	Claims Remaining	Highest No. Previous	Extra Rate	Additional Fee
Total Claims	21 minus	20 =	0 x $ 18.00	$ 18.00
Independent Claims	3 minus	3 =	0 x $ 84.00	$ 0.00
Multiple Dependent Claim First Added			+ $280.00	$ 0.00

TOTAL IF NOT SMALL ENTITY . . $0.00

[ ] SMALL ENTITY STATUS - If applicable, divide by 2 . . . . . $0.00
[ ] Verified statement enclosed, if not previously filed.

[ ] Applicant also requests a _____ month extension of time for response to the outstanding Office Action. The fee is $0.00

[ ] Fee set forth in 37 C.F.R. 1.17 (p) for Information Disclosure under 37 C.F.R. 1.97 (c) $0.00

TOTAL FEE $18.00

The Commissioner is hereby authorized to charge any overpayment or underpayment of the above fee associated with this Communication to Deposit Account No. 50-0541. A duplicate copy of this sheet is attached.

CHRISTOPHER P. MAIORANA, P.C.

By: Robert M. Miller
Robert M. Miller
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24025 Greater Mack, Suite 200
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I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on June 26, 2002.

By: Mary Donna Berkley
Mary Donna Berkley

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Washington, D.C. 20231
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/504,344	02/14/2000	Cathal G. Phelan	0325.000309	7771

21363 7590 10/22/2002

CHRISTOPHER P. MAIORANA, P.C.
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EXAMINER	
NAMAZI, MEHDI	
ART UNIT	**PAPER NUMBER**
2188	8

DATE MAILED: 10/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

Office Action Summary	Application No. 09/504,344	Applicant(s) Phelan
	Examiner Mehdi Namazi	Art Unit 2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *three* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jul 9, 2002*.

2a) ☒ This action is **FINAL.** 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-21* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☒ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *02/14/00* is/are a) ☐ accepted or b) ☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. This office action is in response to the amendment filed June 9, 2002. Applicant's amendment and arguments have been considered with results that follow.

Claims

2. Claims 1-20 have been presented in this application for examination. Claim 19 has been amended. Claim 21 has been added. No claim have been canceled. Therefore, claims 1-21 remain pending in the application.

Response to Arguments

3. Applicant's arguments filed on June 9, 2002 have been fully considered. With regard to claims 1, 12 and 13 the applicant's arguments is not persuasive.

Examiner is agree with applicant's arguments on pages 9-11 with regard to termination of continuous burst (col. 8, lines 32-36 or col. 7, lines 36-38, or col. 7, lines 38-41). However, I should point out this fact that the termination is with regard to continuous burst and not with a row burst which represents a fixed burst length with no interruption. Cowles provides a solution for avoiding termination of row burst, "To avoid a

premature termination of a burst, RSA* cannot transition high until after the column associated with each row has been latched". (col. 8, lines 63-65)

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "address and control bus" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

5. The amendment filed on June 9, 2002 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

as per claim 21, line 2, "an address and control bus" is not supported by specification. Page 9, lines 8 of specification teaches two separate address bus and control bus.

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 21 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As per claim 21, line 2, "an address and control bus" is not supported by specification.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Cowles(U.S.Patent No. 5,729,504).

As per claims 1 and 12-13 Cowles teaches a circuit comprising: a memory comprising a plurality of storage elements each configured to read and write data in response to an internal address signal(fig. 4, element 112); and a logic circuit configured to generate a predetermined number of said internal address signals in response to (I) an external address signal (col. 2, lines 20-21), (ii) a clock signal(col. 9, lines 59-61) and (iii) one or more control signals(fig. 4, element 138, produce control signal), wherein said generation of said predetermined number of internal address signals is non-interruptible(col. 8, lines 18-22).

As per claims 2, Cowles teaches wherein said predetermine number of internal address signals is determined by a fixed burst length(col. 5, lines 47-53).

As per claims 3-4 and 14, Cowles teaches wherein said predetermined number of internal address signals are 4 or 8(fig. 2, shows various burst length of 2, 4, and 8).

As per claim 5, Cowles teaches wherein said fixed burst length is programmable(col. 5, lines 31-34).

As per claims 6 and 15, Cowles teaches wherein said fixed burst length is programmed by bond options(it is well known in the art to include multiple modes of operation selected by bond options).

As per claims 7 and 16, Cowles teaches wherein said fixed burst length is programmed by voltage levels on external pins(it is inherent to have voltage levels for each burst).

As per claim 8, Cowles teaches wherein said memory comprises a static random access memory(fig. 4, element 112).

As per claim 9, Cowles teaches wherein said memory comprises a dynamic random access memory(fig. 4, element 112).

As per claims 10 and 17, Cowles teaches wherein said predetermined number of internal address signals is chosen to provide time for at least one writeback or refresh cycle(col. 8,

lines 33-36, lines 63-65)(Cowles teaches that continuous burst between rows are intruptable but row or fixed burst are not).

As per claim 11, Cowles teaches wherein the predetermined number of internal address signals is chosen to meet predetermined criteria for sharing address and control busses (col. 8, lines 18-22).

As per claim 18, Cowles teaches wherein the logic circuit comprises a counter configured to generate the predetermined number of internal address signals(fig. 4, element 126).

As per claim 19, Cowles teaches wherein the external address signal comprises an initial address for data transfers to and from the memory(col. 2, lines 21-22).

As per claim 20, Cowles teaches wherein the circuit is an integrated circuit(abstract).

As per claim 21, Cowles teaches an address and control bus configured to present the external address signal and the one or more control signals, wherein the bus is freed up during the generation of the predetermined number of internal address signal(fig. 5)(col. 6, lines 47-50).

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mehdi Namazi whose telephone number is (703) 306-2758. The examiner can normally be reached on Monday-Thursday from 7:00 to 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do Hyun yoo, can be reached on (703) 308-4908.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-9600.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 746-7239 (for formal communications intended for entry)

Or:

(703) 746-7240 (for informal or draft communications, please label PROPOSED or DRAFT)

Hand-delivered responses should be brought to Crystal Park 2,

2121 Crystal Drive,

Arlington, VA., Sixth Floor (Receptionist).

M. Namazi
October 18, 2002

Reginald G. Bragdon
REGINALD G. BRAGDON
PRIMARY EXAMINER

Official

P/C C. Barnes 12/18/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Cathal G. Phelan
Serial No.:	09/504,344
Title:	MEMORY DEVICE WITH FIXED LENGTH NON-INTERRUPTIBLE BURST
Filed:	February 14, 2000
Attorney Docket No.:	0325.00309
Examiner:	Namazi, M.
Art Unit:	2187
In Response To:	Office Action mailed October 22, 2002

O.K to enter 6-12-03

CERTIFICATE OF FACSIMILE

The undersigned hereby certifies that the foregoing documents were sent via facsimile to the following: Assistant Commissioner for Patents, Washington, D.C. 20231, Examiner M. Namazi at (703) 746-7238 on December 16, 2002.

By: Mary Donna Berkley
Mary Donna Berkley

AMENDMENT AFTER FINAL

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action mailed October 22, 2002 please amend the above-identified application as follows:

IN THE CLAIMS

Please amend the claims as follows:

1. (AMENDED) A circuit comprising:

a memory comprising a plurality of storage elements each configured to read and write data in response to an internal address signal; and

a logic circuit configured to generate a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

C1

2. (AMENDED) The circuit according to claim 1, wherein said predetermined number of internal address signals is determined by a fixed burst length.

3. (AMENDED) The circuit according to claim 1, wherein said predetermined number of internal address signals is at least 4.

4. (AMENDED) The circuit according to claim 1, wherein said predetermined number of internal address signals is 8.

5. (AMENDED) The circuit according to claim 2, wherein said fixed burst length is programmable.

16

6. (AMENDED) The circuit according to claim 5, wherein said fixed burst length is programmed by bond options.

7. (AMENDED) The circuit according to claim 5, wherein said fixed burst length is programmed by voltage levels on external pins.

8. (AMENDED) The circuit according to claim 1, wherein said memory comprises a static random access memory.

C1

9. (AMENDED) The circuit according to claim 1, wherein said memory comprises a dynamic random access memory.

10. (AMENDED) The circuit according to claim 9, wherein said predetermined number of internal address signals is chosen to provide time for at least one writeback or refresh cycle.

11. (AMENDED) The circuit according to claim 1, wherein said predetermined number of internal address signals is chosen to meet predetermined criteria for sharing address and control busses.

17

16. (AMENDED) A circuit comprising:

means for reading data from and writing data to a plurality of storage elements in response to a plurality of internal address signals; and

means for generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

C1

17. (AMENDED) A method of providing a fixed burst length data transfer comprising the steps of:

accessing a memory in response to a plurality of internal address signals; and

generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) a control signal, wherein said generation of said predetermined number of internal address signals is non-interruptible.

18. The method according to claim 17, further comprising the step of programming said predetermined number.

18

C

19 ~~18~~. The method according to claim 18 ~~14~~, wherein said programming step is performed using bond options.

20 ~~16~~. The method according to claim 18 ~~14~~, wherein said programming step is performed using voltage levels.

21 ~~17~~. (AMENDED) The method according to claim 17 ~~13~~, further comprising the step of selecting said predetermined number to provide time for at least one writeback or refresh cycle.

C1

12 ~~16~~. The circuit according to claim 1, wherein said logic circuit comprises a counter configured to generate said predetermined number of internal address signals.

13 ~~19~~. (AMENDED) The circuit according to claim 1, wherein said external address signal comprises an initial address for data transfers to and from said memory.

14 ~~20~~. A memory device according to claim 1, wherein said circuit is an integrated circuit.

15 ~~21~~. (AMENDED) The circuit according to claim 1, further comprising address and control busses configured to present said

19 C

C1 external address signal and said one or more control signals, wherein said busses are freed up during the generation of said predetermined number of internal address signals.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

21. (AMENDED) The circuit according to claim 1, further comprising [an] address and control [bus] <u>busses</u> configured to present said external address signal and said one or more control signals, wherein said [bus is] <u>busses are</u> freed up during the generation of said predetermined number of internal address signals.

REMARKS

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns an integrated circuit comprising a memory and a logic circuit. The memory may comprise a plurality of storage elements each configured to read and write data in response to an internal address signal. The logic circuit may be configured to generate a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals. The generation of the predetermined number of internal address signals is non-interruptible.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendment to claim 21 can be found in the drawings as originally filed, for example, FIGS. 1-3, 5A and 5B, and in the specification as originally filed, for example, on page 9, lines 5-10; and page 12, lines 7-15. As such, no new matter has been added.

Furthermore, the present amendment does not raise new issues. The amendment to claim 21 merely changes the grammatically singular "address and control bus" (which Applicant's representatives believe is supported by the specification) to the

grammatically plural "address and control busses." The Examiner has already considered this issue (see page 4, first paragraph of the Office Action dated October 22, 2002). Therefore, the present amendment raises no new issues, and should be entered and considered.

Claim 21 has been amended. Claims 1-21 remain active in the present application.

OBJECTION TO THE DRAWINGS

The objection to the drawings has been obviated by appropriate amendment and should be withdrawn.

OBJECTION TO THE CLAIMS

The objection to claim 21 has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The objection to claim 21 under 35 U.S.C. § 112, first paragraph, has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-21 under 35 U.S.C. §102(b) as being anticipated by Cowles is respectfully traversed.

Cowles is directed to a continuous burst EDO memory device (Title). The invention disclosed by Cowles improves upon a conventional burst "extended data out" (or "BEDO") memory architecture. Despite the statements to the contrary in the Office Action dated October 22, 2002 (hereinafter "the Office Action"), Cowles does not disclose or suggest generating a predetermined number of internal address signals **non-interruptibly**, as presently claimed. Instead, Cowles teaches that the improvement disclosed therein relates to an ability to access a second row of memory while bursting data out of a first row (a so-called "continuous BEDO," or "CBEDO" architecture; see, e.g., FIG. 5 and col. 2, ll. 15-18, 44-48 and 55-61; col. 6, ll. 17-29; col. 7, ll. 55-64; col. 8, ll. 26-33 and 60-63; and col. 9, ll. 4-11, 21-23 and 47-52 of Cowles). This ability to access a second row of memory while bursting data out of first row has little or nothing to do with whether a "burst" can be interrupted. In fact, each of the various burst accesses disclosed by Cowles <u>can</u> be interrupted. Consequently, it appears that any generation of internal addresses performed by the various memory architectures of Cowles can also be interrupted (see, e.g., the detailed discussion below and FIG. 4;

col. 5, l. 61 through col. 6, l. 9; and col. 8, ll. 37-48 of Cowles).

In contrast, the present claim 1 recites a circuit comprising a memory comprising a plurality of storage elements each configured to read and write data in response to an internal address signal and a logic circuit configured to generate **non-interruptibly** a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals. Claims 12 and 13 recite similar limitations. Therefore, Cowles neither discloses nor suggests the presently claimed invention.

The Office Action appears to draw a distinction between a "continuous burst" and a "row burst" as they relate to interruptibility (see, e.g., the paragraph bridging pages 2-3 of the Office Action, which appears to suggest that a continuous burst can be terminated or interrupted, while a row burst cannot). However, Cowles draws such a distinction for only one of three conditions under which a burst can be prematurely terminated or interrupted. In fact, Cowles discloses that a BEDO access can be interrupted under any of the three conditions, whereas a CBEDO access can be interrupted under only two of the three conditions. The passage relied upon in the Office Action to support the distinction between a "continuous burst" and a "row burst" is

actually directed to a difference between BEDO and CBEDO memories that affects only one of the three BEDO termination conditions; see the detailed discussion below. As a result, both the "continuous burst" and "row burst" modes disclosed by Cowles are interruptible.

For example, with regard to BEDO memories, Cowles states that:

> "The time at which data will be valid at the outputs of the burst EDO DRAM is dependent only on the timing of the CAS* signal **provided that OE* is maintained low, and WE* remains high.**" (Col. 4, ll. 8-11 of Cowles; emphasis added.)

Furthermore, with regard to BEDO memories, Cowles also states that:

> "Once the memory device begins to output data in a burst read cycle, the output drivers 34 will continue to drive the data lines without tri-stating the data outputs during CAS* high intervals **dependent on the state of the output enable 42 and write enable 36 (OE* and WE*) control lines**, thus allowing additional time for the system to latch the output data." (Col. 3, l. 65-col. 4, l. 4 of Cowles; emphasis added.)

> "The control circuit[r]y determines when a current data burst should be terminated **based upon the state of RAS* 14, CAS* 24 and WE* 36.**" (Col. 4, ll. 63-65 of Cowles; emphasis added.)

> "**The level of the WE* signal must remain high** for read and low for write burst accesses **throughout the burst access**. A low to high transition within a burst write access will terminate the burst access, preventing further writes from occurring. A high to low transition on WE* within a burst read access will likewise terminate the burst read access and will place the data output 10 in a high impedance state." (Col. 5, ll. 4-10 of Cowles; emphasis added.)

> **"Both RAS* and CAS* going high during a burst access will also terminate the burst access cycle** placing the data drivers in a high impedance output state, and resetting the burst length counter." (Col. 5, ll. 25-28 of Cowles; emphasis added.)

Thus, in BEDO memories, Cowles teaches that there are three conditions that will terminate a BEDO access:

1. WE* transitioning, either from low to high or from high to low;
2. RAS* and CAS* going high; or
3. OE* going high (although, arguably, the state of OE* may have little, if anything, to do with generating a predetermined number of internal addresses).

The improvement to BEDO memories disclosed by Cowles and discussed above is directed to minimizing the impact of condition #2 above when accessing a different row. If we assume *arguendo* that the OE* signal disclosed by Cowles has little, if anything, to do with generation of internal addresses, there remains one condition (WE* transitioning) under which the CBEDO memory of Cowles will terminate a burst access, and thus, interrupt the generation of internal addresses, contrary to the present claims.

With regard to CBEDO memories, Cowles states that:

> "The time at which data will be valid at the outputs of the burst EDO DRAM is dependent only on the timing of the CAS* signal **provided that OE* is maintained low, and WE* remains high.**" (Col. 6, ll. 63-66 of Cowles [emphasis added]; note the similarities to col. 4, ll. 8-11 of Cowles, cited above.)

> "Once the memory device begins to output data in a burst read cycle, the output drivers 134 will continue to drive the data lines without tri-stating the data outputs during CAS* high intervals **dependent on the state of the output enable and write enable (OE* and WE*) control lines**, thus allowing additional time for the system to latch the output data." (Col. 7, ll. 53-59 of Cowles [emphasis added]; note the similarities to col. 3, l. 65-col. 4, l. 4 of Cowles, cited above.)
>
> "The control circuit[r]y determines when a current data burst should be terminated **based upon the state of RAS* 114, CAS* 124 and WE* 136.**" (Col. 7, ll. 52-54 of Cowles [emphasis added]; note the similarities [including the typographical error] to col. 4, ll. 63-65 of Cowles, cited above.)
>
> "**The level of the WE* signal must remain high** for read and low for write burst accesses **throughout the burst access.** A low to high transition within a burst write access will terminate the burst access, preventing further writes from occurring. A high to low transition on WE* within a burst read access will likewise terminate the burst read access and will place the data output 110 in a high impedance state." (Col. 7, ll. 34-41 of Cowles [emphasis added]; note the similarities to col. 5, ll. 4-10 of Cowles, cited above.)

Thus, in CBEDO memories, Cowles teaches that at least two of the three conditions above that terminate a BEDO access (WE* transitioning and OE* going high) will also terminate a CBEDO access. Cowles is quite clear in this teaching with regard to WE* transitions:

> "In a CBEDO operation, **control circuitry 138** does not terminate a burst operation when CAS* and RAS* go high, but **looks to WE* for an indication that a burst operation is to be terminated.**" (Col. 7, ll. 57-61 of Cowles; emphasis added.)

> "To terminate a continuous burst read operation, **the WE* signal merely has to transition high** prior to a falling edge of the CAS* signal." (Col. 8, ll. 33-36 of Cowles; emphasis added.)

Therefore, even if we assume for the sake of argument that OE* does not affect the generation of internal addresses, there is still one condition under which the memories of Cowles will interrupt (or prematurely terminate) an access: WE* transitioning. Cowles rather explicitly teaches how such a premature termination can take place.

For example, in FIG. 4 of Cowles, the access at "COLn" is prematurely terminated when WE* transitions from low to high, causing the "COLp" address to be latched and data from the "COLp" address to be read out (see, e.g., the "ADDR," "WE" and "DQ" waveforms in FIG. 4 and the corresponding description at col. 5, l. 61-col. 6, l. 9 of Cowles). Cowles correlates the read and write operations of the BEDO memory of FIG. 3 and the CBEDO memory of FIG. 5; i.e., in both memories, the next falling edge of CAS* after the WE* signal transitions low latches a new column address for a burst write operation (see, e.g., col. 8, ll. 37-48 of Cowles). One of ordinary skill in the art would understand that the next falling edge of CAS* after the WE* signal transitions high latches a new column address for a burst read operation. Thus, this

passage further substantiates the interruptibility of both the BEDO and CBEDO memories of Cowles.

Thus, it appears that Cowles consistently discloses at least one condition under which the generation of internal addresses can be interrupted, contrary to the **non-interruptible** internal address generation presently claimed.

As noted in the Office Action, Cowles discloses that:

> "To avoid a premature termination of a burst, RAS* cannot transition high until after the last column associated with each row has been latched." (Col. 8, ll. 63-65 of Cowles.)

However, as discussed above, this statement refers to reducing the impact of burst termination condition #2 above (see, e.g., col. 8, l. 65-col. 9, l. 15 of Cowles), a condition that also terminates a burst access in the BEDO memory of Cowles. More to the point of the present claims, Cowles discloses that:

> "Transitions of the WE* signal may be locked out during critical timing periods *within an access cycle* in order to reduce the possibility of triggering a false write cycle. After the critical timing period, *the state of WE* will determine whether a burst access continues*, is initiated, or is terminated." (Col. 5, ll. 11-16 and col. 7, ll. 42-47 of Cowles; emphasis added.)

These statements in Cowles apply to both the BEDO and CBEDO memory architectures (consistent with the WE*-initiated interrupt shown in FIG. 4 applying to both BEDO and CBEDO memories). However, as the plain language of the passage

indicates, locking out transitions of the WE* signal during "critical timing periods" does not necessarily prevent termination or interruption of a burst access. Otherwise, how could the state of WE* determine whether a burst access continues? If the access was not interruptible, the state of WE* would only determine whether the next burst access is a read access or a write access; it could not determine whether the ongoing burst access continues or not.

Furthermore, Cowles provides very little guidance as to what the "critical timing periods" might be. Cowles teaches that RAS* must remain high for a minimum of about 100 ns in a BEDO memory (col. 6, ll. 18-29 of Cowles). However, other than to refer to a specified minimum time period relating to the RAS signal (see col. 8, ll. 60-63), Cowles is largely silent as to what the "critical timing periods" are for a CBEDO memory. From these indications, one of ordinary skill in the art could only surmise that "critical timing periods within an access cycle" means something considerably less than an entire access cycle. Thus, it is entirely possible, if not likely, that a burst access can be interrupted during an access cycle by a WE* transition outside the "critical timing period." Consequently, the disclosure that WE* transitions "may be locked out during critical timing periods

within an access cycle" does not mean that burst accesses in a BEDO and/or CBEDO memory are non-interruptible, as presently claimed.

Since Cowles teaches that a burst can be terminated during a read or write access, whether in BEDO or CBEDO mode, Cowles fails to disclose or suggest the **non-interruptible** generation of a predetermined number of internal address signals, as presently claimed. As such, Cowles does not disclose or suggest each and every element of the presently pending claims, arranged as in the presently pending claims. Therefore, Cowles does not anticipate the present claims, and the rejection should be withdrawn.

CONCLUSION

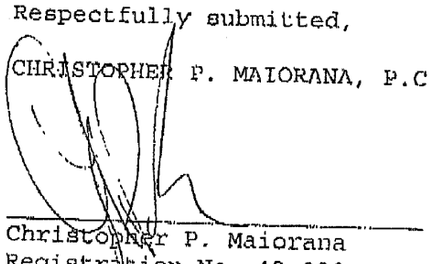
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



Christopher P. Maiorana
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Dated: December 16, 2002

Docket No.: 0325.00309

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PATENTS, TRADEMARKS
& COPYRIGHTS

FACSIMILE MESSAGE

TO: Examiner M. Namazi

COMPANY: U.S. Patent and Trademark Office

RE: Serial No.: 09/504,344 - Filed: February 14, 2000

FILE NO.: 0325.00309

FAX NO.: (703) 746-7238

FROM: Christopher P. Maiorana, Esq.

DATE: December 16, 2002 TIME: _____

TOTAL NUMBER OF PAGES 20 *(including cover sheet)*

If you do not receive any of these pages, please telephone us at (586) 498-0670 or telefax us at (586) 498-0673.

COMMENTS:

Enclosed is the following:

Amendment After Final (19 pages).

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PATENTS, TRADEMARKS
& COPYRIGHTS

December 16, 2002

Meredith McKenzie, Esq.
Manager of Intellectual Property
Cypress Semiconductor Corp.
3901 North First Street, Building 2
San Jose, CA 95134-1599

Re: United States Patent Application Entitled:
FIXED BURST MEMORIES
Cypress Reference No.: CD99073
Our Reference No.: 0325.00309

Dear Meredith:

Enclosed is a copy of the Amendment After Final and accompanying documents that were filed today, via facsimile, with the United States Patent and Trademark Office for the above-identified patent application.

Please call me if you have any questions.

Very truly yours,

CHRISTOPHER P. MAIORANA, P.C.

Christopher P. Maiorana

CPM/mdb
Enclosure
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FN

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/504,344	02/14/2000	Cathal G. Phelan	0325.000309	7771

21363 7590 01/10/2003

CHRISTOPHER P. MAIORANA, P.C.
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EXAMINER	
NAMAZI, MEHDI	
ART UNIT	**PAPER NUMBER**
2188	10

DATE MAILED: 01/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

FN

Advisory Action

Application No.	Applicant(s)
09/504,344	Phelan
Examiner	**Art Unit**
Mehdi Namazi	2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED *Dec 16, 2002* FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid the abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

THE PERIOD FOR REPLY [check only a) or b)]

a) ☒ The period for reply expires *three* months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☐ The proposed amendment(s) will not be entered because:

(a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);

(b) ☐ they raise the issue of new matter (see NOTE below);

(c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

(d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: _____

3. ☐ Applicant's reply has overcome the following rejection(s):

4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☒ The a) ☐ affidavit, b) ☐ exhibit, or c) ☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because:
See attached paper.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☒ For purposes of Appeal, the proposed amendment(s) a) ☐ will not be entered or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: _____

Claim(s) objected to: _____

Claim(s) rejected: *1-21*

Claim(s) withdrawn from consideration: _____

8. ☐ The proposed drawing correction filed on _____ is a) ☐ approved or b) ☐ disapproved by the Examiner.

9. ☐ Note the attached Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

10. ☐ Other:

Reginald G. Bragdon
REGINALD G. BRAGDON
PRIMARY EXAMINER

The examiner respectfully disagree with applicant's argument. Broadly interpreting the claim language, applicant's invention teaches "the fixed burst length may allow the circuit 100 to operate at higher frequencies then a conventional DRAM without needing interrupts to preform refreshes of data."(specification , page 8, lines 12-15). Cowles clearly teaches a continuous (non-interruptible) stream while new rows of the memory are accessed(abstract). In fact Cowles does not interrupt any signal **during refreshing of data**.

P/1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit:	2188
Examiner:	Namazi, M.
Applicant:	Cathal G. Phelan
Serial No:	09/504,344
Filing Date:	February 14, 2000
For:	MEMORY DEVICE WITH FIXED LENGTH NON-INTERRUPT BURST

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on January 22, 2003 .

By: Mary Donna Berkley
Mary Donna Berkley

NOTICE OF APPEAL

Patent and Trademark Board of Appeals and Interferences
Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

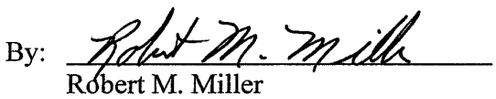
The Applicant of the above-captioned patent application hereby appeals to the Board of Patent Appeals and Interferences from the decision dated October 22, 2002 of the Examiner finally rejecting Claims 1-21.

The payment for the appeal fee is enclosed herewith.

01/30/2003 EWILLIAM 00000008 09504344
01 FC:1401 320.00 OP

If Applicant has not requested a sufficient extension and/or has not paid a sufficient fee for this matter, and/or for the extension necessary to prevent the abandonment of this application, please consider this as a request for an extension for the required time period and/or authorization to charge our Deposit Account No. 50-0541 for any fee which may be due.

Respectfully submitted,

By: 

Robert M. Miller
Reg. No. 42,892
CHRISTOPHER P. MAIORANA, P.C.
24025 Greater Mack, Suite 200
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(586) 498-0670

Date: January 22, 2003

Attorney Docket No.: 0325.00309

Our Docket No.: 0325.00309

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Applicant	Cathal G. Phelan		
Application No.:	09/504,344	Examiner:	Namazi, M.
Filed:	February 14, 2000	Art Group:	2188
For:	MEMORY DEVICE WITH FIXED LENGTH NON-INTERRUPTIBLE BURST		

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on March 24, 2003 .

By: Mary Donna Berkley
Mary Donna Berkley

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MAR 3 1 2003
Technology Center 2100

APPEAL BRIEF

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Appellants submit, in triplicate, the following Appeal Brief pursuant to 37 C.F.R. §1.192 for consideration by the Board of Patent Appeals and Interferences. Appellants also submit herewith a PTO-2038 Form in the amount of $320.00 to cover the cost of filing the opening brief as required by 37 C.F.R. §1.17(c). Please charge any additional fees or credit any overpayment to our Deposit Account Number 50-0541.

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01 FC:1402 320.00 OP

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GROUP 2100

Docket Number:0325.00309
Application No.: 09/504,344

TABLE OF CONTENTS

[1] U.S. Patent No. 5, 729,504.

I. REAL PARTY IN INTEREST

The real party in interest is the Assignee, Cypress Semiconductor Corporation.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the Appellant, the Appellant's legal representative, or the Assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-21 are pending and remain rejected. The Appellant hereby appeals the rejection of claims 1-21. A copy of the currently pending claims is included in the Appendix.

IV. STATUS OF AMENDMENTS

Appellant is appealing a final Office Action issued by the Examiner on October 22, 2002. On December 16, 2002, Appellant filed an Amendment After Final. An Advisory Action dated January 10, 2003 entered the amendment and maintained the rejection. Appellant filed a Notice of Appeal on January 22, 2003. The Notice of Appeal was received by the B.P.A.I. on January 28, 2003.

V. SUMMARY OF INVENTION

In one embodiment, the present invention concerns a circuit (100) comprising a memory (104) and a logic circuit(102). The memory may comprise a plurality of storage elements each configured to read and write data in response to an internal address signal (ADDR_INT). The logic circuit may be configured to generate a predetermined number of the internal address signals in response to (i) an external address signal (ADDR_EXT), (ii) a clock signal (CLK) and (iii) one or more control signals (LOAD, ADV, BURST). The generation of the predetermined number of internal address signals is non-interruptible[2].

In another embodiment, the present invention concerns a circuit (100) comprising (a) means for reading data from and writing data to a plurality of storage elements in response to a plurality of internal address signals (104) and (b) means for generating a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals (102). The generation of the predetermined number of internal address signals is non-interruptible.[3]

In yet another embodiment, the present invention concerns a method of providing a fixed burst length data transfer (see the signal DQ in FIGS. 5A, 5B and 6) comprising the steps of (A) accessing a memory in response to a plurality of internal address signals and (B) generating a predetermined number of the internal address signals in response to (i) an external address signal

---

[2] See FIG. 4 and page11, lines 11-17 of the specification.

[3] *Id.*

(ADDR), (ii) a clock signal (CLK) and (iii) a control signal (ADV), where the generation of the predetermined number of internal address signals is non-interruptible.[4]

VI. ISSUE

The issue is whether claims 1-21 are patentable under 35 U.S.C. §102(b) over Cowles.[5]

VII. GROUPING OF CLAIMS

Appellant contends that the claims of the present invention do not stand or fall together. In particular, the following groups of claims are separately patentable:

Group 1: Claims 1, 2-5, 8, 9, and 18-20 stand together.

Group 2: Claim 6 stands alone.

Group 3: Claim 7 stands alone.

Group 4: Claim 10 stands alone.

Group 5: Claim 11 stands alone.

Group 6: Claim 12 stands alone.

Group 7: Claim 13, 14 and 16 stand together.

Group 8: Claim 15 stands alone.

Group 9: Claim 17 stands alone.

Group 10: Claim 21 stands alone.

---

[4] See FIG. 4 and page11, lines 11-17 of the specification.

[5] U.S. Patent No. 5,729,504.

The claim(s) in each group is(are) separately patentable from the claim(s) in any other groups. During prosecution, each independent and dependent claim is considered to be separately patentable over every other claim.[6] As such, each of the above groups is considered to be separately patentable over every other group.[7]

In particular, groups 1-5 concern a circuit, group 6 concerns a means plus function and groups 7-10 concern a method. Since the means plus function claim of group 6 and the method claims of groups 7-10 do not necessarily encompass all the structure comprising the circuit of the claims of any of the groups 1-5, groups 1-5 are separately patentable with respect to groups 6-10. Detailed reasons why the groups are patentable over the cited references are provided in the Arguments below.

Group 2 is separately patentable over group 1 due to the added structure of group 2. In particular, the recitation in claim 6 that the fixed burst length is programmed by bond options provides claim 6 of group 2 with structure not recited the independent claim 1 of group 1. Therefore, the dependent claim 2 in group 2 may be found patentable over the cited reference even if the independent claim 1 in group 1 is not. As such, group 2 is separately patentable as compared to group 1. Detailed reasons why claim 2 is separately distinguishable over the cited reference is provided in the Arguments below.

---

[6] See, e.g., *Rowe v. Dror*, 42 USPQ2d 1550, 1552 (Fed. Cir. 1997), *Preemption Devices, Inc. v. Minnesota Mining and Manufacturing Company*, 221 USPQ 841, 843 (Fed. Cir. 1984), and *Jones v. Hardy*, 727 F.2d 1524, 1528, 220 USPQ 1021, 1024 (Fed. Cir. 1984) (It is well established that each claim in a patent constitutes a separate invention.).

[7] Manual of Patent Examining Procedure (M.P.E.P.), Eighth Edition, August, 2001, §1206.

Group 3 is separately patentable over groups 1 and 2 due to the added structure of group 3. In particular, the recitation in claim 7 that the fixed burst length is programmed by voltage levels at external pins provides claim 7 of group 3 with structure not recited the independent claim 1 of group 1 or the dependent claim 6 of group 2. Therefore, the dependent claim 7 in group 3 may be found patentable over the cited reference even if the independent claim 1 in group 1 and the dependent claim 6 in group 2 are not. As such, group 3 is separately patentable as compared to groups 1 and 2. Detailed reasons why claim 7 is separately distinguishable over the cited reference is provided in the Arguments below.

Group 4 is separately patentable over groups 1-3 due to the added structure of group 4. In particular, the recitation in claim 10 that the predetermined number of internal address signals is chosen to provide time for at least one writeback or refresh cycle provides claim 10 of group 4 with structure not recited the independent claim 1 of group 1 or the dependent claims 6 and 7 of groups 2 and 3. Therefore, the dependent claim 10 in group 4 may be found patentable over the cited reference even if the independent claim 1 in group 1 and the dependent claims 6 and 7 in groups 2 and 3 are not. As such, group 4 is separately patentable as compared to groups 1, 2 and 3. Detailed reasons why claim 10 is separately distinguishable over the cited reference is provided in the Arguments below.

Group 5 is separately patentable over groups 1-4 due to the added structure of group 5. In particular, the recitation in claim 11 that the predetermined number of internal address signals is chosen to meet predetermined criteria for sharing address and control busses provides claim 11 of group 5 with structure not recited the independent claim 1 of group 1 or the dependent claims 6, 7 and 10 of groups 2-4. Therefore, the dependent claim 11 in group 5may be found patentable over

the cited reference even if the independent claim 1 in group 1 and the dependent claims 6, 7 and 10 in groups 2-4 are not. As such, group 5 is separately patentable as compared to groups 1-4. Detailed reasons why claim 11 is separately distinguishable over the cited reference is provided in the Arguments below.

The means plus function of group 6 is separately patentable over the circuit of groups 1-5 and/or the method of groups 7-10 because group 6 includes the means to perform the claimed functions. In particular, independent claim 12 in group 6 provides means for generating a predetermined number of the internal address signals where the generation of the predetermined number of internal address signals is non-interruptible not necessarily provided for in groups 1-5 and 7-10. References to the specific means plus the respective specific functions in claim 12 provide separately distinguishable limitations over the cited reference. Therefore, claim 12 may be found patentable over the cited reference even if groups 1-5 and 7-10 are not. As such, group 6 is separately patentable as compared to groups 1-5 and 7-10. Detailed reasons why claim 12 is separately distinguishable over the cited reference is provided in the Arguments below.

The method of group 7 is separately patentable over the apparatus of groups 1-5 and/or the means plus function of group 6 because group 7 involves process steps and/or specific circuit elements not necessarily in groups 1-6. In particular, independent claim 13 in group 7 provides the step of generating a predetermined number of the internal address signals where the generation of the predetermined number of internal address signals is non-interruptible. Independent claim 1 in group 1, dependent claims 6, 7, 10, and 11 in groups 2-5, and/or independent claim 12 in group 6 recite structure not necessarily provided for in group 7. Therefore, claims 1, 6, 7, 10, 11 and 12 in groups 1-6 may be found patentable over the cited reference even if claim 14 in group 7

is not. As such, group 7 is separately patentable as compared to groups 1-6. Detailed reasons why claim 14 is separately distinguishable over the cited reference is provided in the Arguments below.

Group 8 is separately patentable over group 7 due to the added step of group 8. In particular, claim 15 includes the step of programming the fixed burst length using bond options not provided for by the independent claim 13 in group 7. Therefore, the dependent claim 15 in group 8 may be found patentable over the cited reference even if the independent claim 13 in group 7 is not. As such, group 8 is separately patentable as compared to group 7. Detailed reasons why claim 15 is separately distinguishable over the cited reference is provided in the Arguments below.

Group 9 is separately patentable over group 7 due to the added step of group 9. In particular, claim 17 which includes the step of selecting the predetermined number to provide time for at least one writeback or refresh cycle. Independent claim 1 in group 1, dependent claims 6, 7, 10, and 11 in groups 2-5, and/or independent claim 12 in group 6 recite structure not necessarily provided for in group 9. Therefore, claims 1, 6, 7, 10, 11 and 12 in groups 1-6 may be found patentable over the cited reference even if claim 17 in group 9 is not. As such, group 9 is separately patentable as compared to groups 1-7. Detailed reasons why claim 17 is separately distinguishable over the cited reference is provided in the Arguments below.

Group 10 is separately patentable over group 1 due to the added structure of group 10. In particular, the recitation in claim 21 of address and control busses configured to present the external address signal and the one or more control signals, where the busses are freed up during the generation of the predetermined number of internal address signals provides claim 21 of group 10 with structure not recited the independent claim 1 of group 1. Therefore, the dependent claim 21 in group 10 may be found patentable over the cited reference even if the independent claim 1 in group

1 is not. As such, group 10 is separately patentable as compared to group 1. Detailed reasons why claim 21 is separately distinguishable over the cited reference is provided in the Arguments below.

VIII. ARGUMENTS

A. Selected groupings of the claims are each patentable over Cowles

35 U.S.C. § 102

As set forth in the Final Office Action,[8] claims 1-21 are rejected under 35 U.S.C. § 102(b) as anticipated by Cowles.[9]

The Federal Circuit has stated that "[a]nticipation requires the presence in a single prior art reference disclosure of **each and every element** of the claimed invention, **arranged as in the claim**."[10] The Federal circuit has added that the anticipation determination is viewed from one of ordinary skill in the art: "There must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention."[11] As explained herein below, because Cowles does not disclose or suggest each and every element of the presently pending claims, arranged as in the claims, Cowles does not anticipate the presently claimed invention.

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[8] Page 5, paragraph no. 9 of the Final Office Action mailed October 22, 2002.

[9] U.S. Patent No. 5,729,504.

[10] *Brown v. 3M*, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) citing *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383, 58 USPQ2d 1286, 1291 (Fed. Cir. 2001); *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991) (Emphasis added by Appellant.).

[11] *Scripps Clinic & Research Found. V. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991).

1. Group 1 (claims 1, 2-5, 8, 9 and 18-20) is fully patentable over Cowles.

The presently pending claim 1 provides a circuit comprising a memory and a logic circuit. The memory comprises a plurality of storage elements each configured to read and write data in response to an internal address signal. The logic circuit is configured to generate a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals. The generation of the predetermined number of internal address signals is non-interruptible.

Cowles does not disclose or suggest each and every element of the presently pending claim 1, arranged as in claim 1. Specifically, Cowles does not disclose or suggest the non-interruptible generation of the predetermined number of address signals as presently claimed. Cowles is directed to a continuous burst EDO memory device.[12] The Examiner admits that a continuous burst of Cowles is interruptible.[13] Specifically, the Examiner states that he agrees with Appellant's arguments with regard to termination of a continuous burst.[14] In particular, the Examiner admits that the interruptibility of a continuous burst is supported by the following passages in Cowles:[15]

> **To terminate** a continuous burst read operation, **the WE* signal merely has to transition high** prior to a falling edge of the CAS* signal. (Column 8, lines 33-36 of Cowles; emphasis added).

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[12]Title of Cowles.

[13] See page 2, paragraph no. 3, lines 4-6 of the Office Action mailed October 22, 2002.

[14] *Id.*

[15] *Id.*

> The level of the WE* signal must remain high for read and low for write burst accesses throughout the burst access. **A low to high transition within a burst write access will terminate the burst access**, preventing further writes from occurring. **A high to low transition on WE* within a burst read access will likewise terminate the burst read access** and will place the data output 110 in a high impedance state. (Column 7, lines 34-41 of Cowles; emphasis added).

However, the Examiner urges that while a "continuous burst" can be terminated, a "row burst" represents a fixed burst length with no interruption.[16] Despite the position taken by the Examiner, Cowles does not appear to draw such a distinction between bursts. Specifically, with regard to a burst from a BEDO memory, Cowles states:

> Once the memory device begins to output data in a burst read cycle, the output drivers 34 will continue to drive the data lines without tri-stating the data outputs during CAS* high intervals **dependent on the state of the output enable 42 and write enable 36 (OE* and WE*) control lines**, thus allowing additional time for the system to latch the output data. (Column 3, line 65 through column 4, line 4 of Cowles; emphasis added).
>
> The control circuit[r]y determines when a current data burst should be terminated **based upon the state of RAS* 14, CAS* 24 and WE* 36**. (Column 4, lines 63-65 of Cowles; emphasis added).
>
> **The level of the WE* signal must remain high for read and low for write burst accesses throughout the burst access**. A low to high transition within a burst write access will terminate the burst access, preventing further writes from occurring. A high to low transition on WE* within a burst read access will likewise terminate the burst read access and will place the data output 10 in a high impedance state. (Column 5, lines 4-10 of Cowles; emphasis added).
>
> **Both RAS* and CAS* going high during a burst access will also terminate the burst access cycle** placing the data drivers in a high

[16] See page 2, paragraph no. 3, lines 6-9 of the Office Action mailed October 22, 2002, which appears to suggest that a continuous burst can be terminated or interrupted, while a row burst cannot.

impedance output state, and resetting the burst length counter. (Column 5, lines 25-28 of Cowles; emphasis added).

Thus, in BEDO memories, Cowles clearly teaches that there are three conditions that will terminate (i.e., interrupt) a burst access:

1. WE* transitioning, either from low to high or from high to low;

2. RAS* and CAS* going high; or

3. OE* going high.[17]

Cowles is quite clear that WE* transitions will terminate both a row burst and a continuous burst access. In particular, Cowles states:

> The control circuit[r]y determines when a current data burst should be terminated based upon the states of RAS* 114, CAS* 124 and WE* 136. In the standard BEDO operation described above, **control circuitry 138 terminated a data burst when WE* transitioned during a burst**, or when both CAS* and RAS* transitioned high. In a CBEDO operation, **control circuitry 138** does not terminate a burst operation when CAS* and RAS* go high, but **looks to WE* for an indication that a burst operation is to be terminated**. (Column 7, lines 52-61 of Cowles; emphasis added).

> **To terminate** a continuous burst read operation, **the WE* signal merely has to transition high** prior to a falling edge of the CAS* signal. (Col. 8, ll. 33-36 of Cowles; emphasis added).

Therefore, since Cowles states that a transition of the signal WE* during a burst can terminate the burst in both the standard BEDO operation and in the continuous BEDO (CBEDO) operation, Cowles explicitly teaches that a premature termination of a row burst can take place.

FIG. 4 of Cowles further evidences that row bursts are interruptible. Specifically, FIG. 4 illustrates a burst access starting at column address "COLn" is terminated (i.e., interrupted)

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[17] However, the state of OE*, arguably, may have little, if anything, to do with generating a predetermined number of internal addresses.

when the signal WE* transitions from low to high.[18] Furthermore, Cowles shows addressing sequences for burst lengths of 2, 4, and 8 cycles.[19] However, FIG. 4 of Cowles illustrates a burst access starting at the column address "COLp" is interrupted after only three cycles by the signal RAS* rising.[20] With regard to the operations illustrated in FIG. 4, Cowles further states:

> It will be appreciated that the read and write operations performed on a single memory row of the memory of FIG. 5 are identical to the operation of the memory of FIG. 1 as shown in FIG. 3. That is, after completing a burst read, the WE* signal transitions low and the next falling edge of CAS* latches a new column address for a burst write operation. **Likewise, the timing diagram of FIG. 4 depicting burst write access cycles followed by burst read cycles can be replicated with the memory of the present invention.** As such, BEDO memory devices can be replaced with CBEDO memory devices without effecting the operation of the memory support system. It will further be appreciated by those skilled in the art that the memory device of FIG. 5 can operate with burst lengths of 2, 4, 8, or full row cycles. (Column 8, lines 37-50 of Cowles; emphasis added).

Therefore, despite the position taken by the Examiner,[21] Cowles does not disclose or suggest generating a predetermined number of internal address signals, where the generation of the predetermined number of internal address signals is non-interruptible, as presently claimed.

Furthermore, contrary to the position taken by the Examiner,[22] merely because Cowles teaches that a premature termination of a burst may be avoided, it does not necessarily (or

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[18] See column 6, lines 1-6 of Cowles.

[19] See FIG. 2, column 4, lines 14-18 and column 8, lines 48-50 of Cowles.

[20] See FIG. 4 and column 6, lines 6-9 of Cowles).

[21] See page 2, paragraph no. 3, lines 6-9 of the Office Action mailed October 22, 2002.

[22] See page 2, last two lines through page 3, line 3 of the Office Action mailed October 22, 2002.

logically) follow that the burst is non-interruptible, as presently claimed. Specifically, Cowles recites that:

> To avoid a premature termination of a burst, RAS* cannot transition high until after the last column associated with each row has been latched. (Column 8, lines 63-65 of Cowles).

However, the sentence cited by the Examiner only pertains to termination of a burst in response to a transition of the signal RAS*. The passage is silent with respect to the signal WE*. As discussed above, Cowles discloses that a transition of the signal WE* during a burst can terminate the burst in both the standard BEDO operation and in the continuous BEDO (CBEDO) operation. In particular, Cowles states:

> The control circuit[r]y determines when a current data burst should be terminated based upon the states of RAS* 114, CAS* 124 and WE* 136. In the standard BEDO operation described above, **control circuitry 138 terminated a data burst when WE* transitioned during a burst**, or when both CAS* and RAS* transitioned high. In a CBEDO operation, **control circuitry 138** does not terminate a burst operation when CAS* and RAS* go high, but **looks to WE* for an indication that a burst operation is to be terminated**. (Column 7, lines 52-61 of Cowles; emphasis added).

> **To terminate** a continuous burst read operation, **the WE* signal merely has to transition high** prior to a falling edge of the CAS* signal. (Col. 8, ll. 33-36 of Cowles; emphasis added).

Cowles expressly states that the method of operation of the memory device includes (i) receiving a signal on a write enable input and (ii) terminating the step of outputting data in response to the signal.[23] Furthermore, the fact that Cowles addresses a way to **avoid** a premature termination of a burst due to the signal RAS* is acknowledgment that the burst **can** be prematurely terminated (i.e.,interrupted). Therefore, the burst is not non-interruptible, as presently claimed.

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[23] See column 11, lines 37-41 and column 12, lines 36-40 of Cowles.

Because Cowles teaches that a burst can be terminated by at least a transition of a write enable signal WE* during a read or write access, whether in a BEDO or a CBEDO operating mode, Cowles fails to disclose or suggest the **non-interruptible** generation of a predetermined number of internal address signals, as presently claimed. Therefore, Cowles does not disclose or suggest each and every element of the presently pending claim 1, arranged as in the presently pending claim 1. As such, the presently pending claim 1 is fully patentable over the cited reference[24] and the rejection should be reversed.

2. Group 2 (claim 6) is fully patentable over Cowles

Claim 6 depends indirectly from claim 1 and, therefore, includes the limitations of claim 1. Consequently, the arguments presented in support of the patentability of claim 1 are hereby incorporated by reference in support of claim 6. Claim 6 further recites that a fixed burst length is programmed by bond options.

Cowles does not disclose or suggest each and every element of the presently pending claim 6. Specifically, Cowles is silent regarding programming a fixed burst length by bond options.[25] In particular, the Office Action fails to point to any specific language or figure in Cowles that is considered to disclose or suggest a fixed burst length is **programmed by bond options**, as

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[24] *Brown v. 3M*, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) citing *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383, 58 USPQ2d 1286, 1291 (Fed. Cir. 2001); *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991). *Scripps Clinic & Research Found. V. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991).

[25] Appellant's representative has downloaded an electric version of the Cowles reference and performed a search for the words "bond" and "bond option", with no such occurrences.

presently claimed.[26] Furthermore, the position taken in the Office Action that "it is well known in the art to include multiple modes of operation selected by bond options"[27] does not adequately address the deficiencies of Cowles to support the rejection under 35 U.S.C. § 102. In particular, the Federal Circuit has stated:

> To serve as anticipation, when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and it would be so recognized by persons of ordinary skill.[28]

Even assuming, *arguendo*, it is well known in the art to include multiple modes of operation selected by bond options as urged by the Examiner,[29] the Examiner failed to present any evidence that a person of ordinary skill would recognize bond options for programming a burst length are necessarily present in Cowles. Inherency requires certainty of results, not mere possibility.[30] Therefore, because Cowles does not disclose or suggest each and every element of the presently pending claim 6, arranged as in the present claim 6, the Examiner failed to meet the

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[26] See page 6, lines 9-12 of the Office Action mailed October 22, 2002.

[27] See page 6, lines 9-12 of the Office Action mailed October 22, 2002.

[28] Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 20 USPQ 2d 1746, 1749 (Fed. Cir. 1991) (citations omitted) See also In re Sun, 31 USPQ 2d 1451, 1453 (Fed. Cir. 1993) (unpublished) ("under section 102(b), anticipation requires that the prior art reference disclose either expressly or under the principles of inherency, every limitation of the claim").

[29] See page 6, lines 9-12 of the Office Action mailed October 22, 2002.

[30] See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). See also, In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981).

Office's burden of factually establishing a *prima facie* case of anticipation.[31] As such, the presently pending claim 6 is fully patentable over the cited reference and the rejection should be reversed.

3. Group 3 (claim 7) is fully patentable over Cowles

Claim 7 depends indirectly from claim 1 and, therefore, includes the limitations of claim 1. Consequently, the arguments presented in support of the patentability of claim 1 are hereby incorporated by reference in support of claim 7. Claim 7 further recites that a fixed burst length is programmed by voltage levels on external pins.

Cowles does not disclose or suggest each and every element of the presently pending claim 7. Specifically, Cowles is silent regarding programming a fixed burst length by **voltage levels on external pins**.[32] In particular, the Examiner failed to point to any specific language or figure in Cowles that is considered to disclose or suggest a fixed burst length is **programmed by voltage levels on external pins**, as presently claimed.[33] Furthermore, the conclusory statement in the Office Action that "it is inherent to have voltage levels for each burst"[34] does not adequately address why

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[31] *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). (Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim). *In re* Skinner, 2 USPQ2d 1788, 1788-89 (B.P.A.I. 1986) ("[i]t is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office"). *See also Ex parte* Natale, 11 USPQ2d 1222, 1226 (B.P.A.I. 1989).

[32] Appellant's representative has downloaded an electronic version of the Cowles reference and performed a search for the words "bond" and "bond option", with no such occurrences.

[33] See page 6, lines 9-12 of the Office Action mailed October 22, 2002.

[34] See page 6, lines 9-12 of the Office Action mailed October 22, 2002.

a person of ordinary skill would recognize **programming a fixed burst length by voltage levels on external pins** as being **necessarily** present in Cowles. In particular,

> To serve as anticipation, when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and it would be so recognized by persons of ordinary skill.[35]

The Examiner has presented no evidence to support such a position.[36] Inherency requires certainty of results, not mere possibility.[37]

Thus, the Examiner failed to factually establish that Cowles discloses or suggests each and every element of the presently pending claim 7, arranged as in the present claim 7.[38] Therefore, the Examiner has not met the Office's burden of factually establishing a *prima facie* case of anticipation.[39] As such, claim 7 is fully patentable over Cowles and the rejection should be reversed.

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[35] Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 20 USPQ 2d 1746, 1749 (Fed. Cir. 1991) (citations omitted) See also In re Sun, 31 USPQ 2d 1451, 1453 (Fed. Cir. 1993) (unpublished) ("under section 102(b), anticipation requires that the prior art reference disclose either expressly or under the principles of inherency, every limitation of the claim").

[36] See page 6, lines 13-15 of the Office Action.

[37] See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). See also, In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981).

[38] *Brown v. 3M*, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) citing *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383, 58 USPQ2d 1286, 1291 (Fed. Cir. 2001); *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991).

[39] *In re* Skinner, 2 USPQ2d 1788, 1788-89 (B.P.A.I. 1986). *See also Ex parte* Natale, 11 USPQ2d 1222, 1226 (B.P.A.I. 1989) ("[i]t is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office").

4. Group 4 (claim 10) is fully patentable over Cowles

Claim 10 depends indirectly from claim 1 and, therefore, includes the limitations of claim 1. Consequently, the arguments presented in support of the patentability of claim 1 are hereby incorporated by reference in support of claim 10. Claim 10 further recites that the predetermined number of internal address signals is chosen to provide time for at least one writeback or refresh cycle.[40]

Cowles does not disclose or suggest each and every element of the presently pending claim 10. Specifically, Cowles is silent regarding choosing the predetermined number of internal address signals to provide time for at least one writeback or refresh cycle.[41] In particular, the lines of Cowles cited by the Examiner in support of the rejection do not address choosing the predetermined number of internal address signals to provide time for at least one writeback or refresh cycle, as presently claimed.[42] The Federal Circuit has stated:

> To serve as anticipation, when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and it would be so recognized by persons of ordinary skill.[43]

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[40] See page 3, paragraph no. 12 of the final Office Action dated May 24, 2002.

[41] Appellant's representative has downloaded an electric version of the Cowles reference and performed a search for the words "writeback" and "refresh", with no such occurrences.

[42] See page 6, line 20 through page 7, line 2 of the Office Action mailed October 22, 2002.

[43] Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 20 USPQ 2d 1746, 1749 (Fed. Cir. 1991) (citations omitted) See also In re Sun, 31 USPQ 2d 1451, 1453 (Fed. Cir. 1993) (unpublished) ("under section 102(b), anticipation requires that the prior art reference disclose either expressly or under the principles of inherency, every limitation of the claim").

The Examiner failed to present any evidence that a person of ordinary skill would recognize that Cowles necessarily chooses a burst length to provide time for at least one writeback or refresh cycle.[44] Inherency requires certainty of results, not mere possibility.[45] Therefore, because Cowles does not disclose or suggest each and every element of the presently pending claim 10, arranged as in the present claim 10, the Examiner failed to meet the Office's burden of factually establishing a *prima facie* case of anticipation.[46] As such, the presently pending claim 10 is fully patentable over the cited reference and the rejection should be reversed.

5. Group 5 (claim 11) is fully patentable over Cowles

Claim 11 depends directly from claim 1 and, therefore, includes the limitations of claim 1. Consequently, the arguments presented in support of the patentability of claim 1 are hereby incorporated by reference in support of claim 11. Claim 11 further recites that the predetermined number of internal address signals is chosen to meet predetermined criteria for sharing address and control busses.

Cowles does not disclose or suggest each and every element of the presently pending claim 11. Specifically, Cowles is silent regarding choosing the predetermined number of internal

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[44] See page 6, line 20 through page 7, line 2 of the Office Action mailed October 22, 2002.

[45] See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). See also, In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981).

[46] *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). (Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim). *In re* Skinner, 2 USPQ2d 1788, 1788-89 (B.P.A.I. 1986) ("[i]t is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office"). *See also Ex parte* Natale, 11 USPQ2d 1222, 1226 (B.P.A.I. 1989).

address signals to meet predetermined criteria for sharing address and control busses.[47] In particular, the lines of Cowles cited by the Examiner in support of the rejection do not address choosing the predetermined number of internal address signals to meet predetermined criteria for sharing address and control busses, as presently claimed.[48] The Federal Circuit has stated:

> To serve as anticipation, when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and it would be so recognized by persons of ordinary skill.[49]

The Examiner failed to present any evidence that a person of ordinary skill would recognize that Cowles necessarily chooses a burst length to meet predetermined criteria for sharing address and control busses.[50] Inherency requires certainty of results, not mere possibility.[51] Therefore, because Cowles does not disclose or suggest each and every element of the presently pending claim 11, arranged as in the present claim 11, the Examiner failed to meet the Office's

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[47] Appellant's representative has downloaded an electric version of the Cowles reference and performed a search for the words "free," "freed up," "share" and "sharing", with no such occurrences.

[48] See page 7, lines 3-6 of the Office Action mailed October 22, 2002.

[49] Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 20 USPQ 2d 1746, 1749 (Fed. Cir. 1991) (citations omitted) See also In re Sun, 31 USPQ 2d 1451, 1453 (Fed. Cir. 1993) (unpublished) ("under section 102(b), anticipation requires that the prior art reference disclose either expressly or under the principles of inherency, every limitation of the claim").

[50] See page 7, lines 3-6 of the Office Action mailed October 22, 2002.

[51] See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). See also, In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981).

burden of factually establishing a *prima facie* case of anticipation.[52] As such, the presently pending claim 11 is fully patentable over the cited reference and the rejection should be reversed.

6. Group 6 (claim 12) is fully patentable over Cowles

The presently pending claim 12 provides (a) means for reading data from and writing data to a plurality of storage elements in response to a plurality of internal address signals and (b) means for generating a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, where the generation of the predefermined number of internal address signals is non-interruptible.

Cowles does not disclose or suggest each and every element of the presently pending claim 12, arranged as in claim 12. Specifically, Cowles does not disclose or suggest the non-interruptible generation of the predetermined number of address signals, as presently claimed. Cowles is directed to a continuous burst EDO memory device.[53] The Examiner admits that a continuous burst of Cowles is interruptible.[54] Specifically, the Examiner states that he agrees with Appellant's arguments with regard to termination of a continuous burst.[55] In particular, the

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[52] *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). (Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim). *In re* Skinner, 2 USPQ2d 1788, 1788-89 (B.P.A.I. 1986) ("[i]t is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office"). *See also Ex parte* Natale, 11 USPQ2d 1222, 1226 (B.P.A.I. 1989).

[53] Title of Cowles.

[54] See page 2, paragraph no. 3, lines 4-6 of the Office Action mailed October 22, 2002.

[55] *Id.*

Examiner admits that the interruptibility of a continuous burst is supported by the following passages in Cowles:[56]

> **To terminate** a continuous burst read operation, **the WE* signal merely has to transition high** prior to a falling edge of the CAS* signal. (Column 8, lines 33-36 of Cowles; emphasis added).
>
> The level of the WE* signal must remain high for read and low for write burst accesses throughout the burst access. **A low to high transition within a burst write access will terminate the burst access**, preventing further writes from occurring. **A high to low transition on WE* within a burst read access will likewise terminate the burst read access** and will place the data output 110 in a high impedance state. (Column 7, lines 34-41 of Cowles; emphasis added).

However, the Examiner urges that while a "continuous burst" can be terminated, a "row burst" represents a fixed burst length with no interruption.[57] Despite the position taken by the Examiner, Cowles does not appear to draw such a distinction between bursts. Specifically, with regard to a burst from a BEDO memory, Cowles states:

> Once the memory device begins to output data in a burst read cycle, the output drivers 34 will continue to drive the data lines without tri-stating the data outputs during CAS* high intervals **dependent on the state of the output enable 42 and write enable 36 (OE* and WE*) control lines**, thus allowing additional time for the system to latch the output data. (Column 3, line 65 through column 4, line 4 of Cowles; emphasis added).
>
> The control circuit[r]y determines when a current data burst should be terminated **based upon the state of RAS* 14, CAS* 24 and WE* 36**. (Column 4, lines 63-65 of Cowles; emphasis added).

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[56] *Id.*

[57] See page 2, paragraph no. 3, lines 6-9 of the Office Action mailed October 22, 2002, which appears to suggest that a continuous burst can be terminated or interrupted, while a row burst cannot.

> **The level of the WE* signal must remain high for read and low for write burst accesses throughout the burst access.** A low to high transition within a burst write access will terminate the burst access, preventing further writes from occurring. A high to low transition on WE* within a burst read access will likewise terminate the burst read access and will place the data output 10 in a high impedance state. (Column 5, lines 4-10 of Cowles; emphasis added).
>
> **Both RAS* and CAS* going high during a burst access will also terminate the burst access cycle** placing the data drivers in a high impedance output state, and resetting the burst length counter. (Column 5, lines 25-28 of Cowles; emphasis added).

Thus, in BEDO memories, Cowles clearly teaches that there are three conditions that will terminate (i.e., interrupt) a burst access:

1. WE* transitioning, either from low to high or from high to low;
2. RAS* and CAS* going high; or
3. OE* going high.[58]

Cowles is quite clear that WE* transitions will terminate both a row burst and a continuous burst access. In particular, Cowles states:

> The control circuit[r]y determines when a current data burst should be terminated based upon the states of RAS* 114, CAS* 124 and WE* 136. In the standard BEDO operation described above, **control circuitry 138 terminated a data burst when WE* transitioned during a burst**, or when both CAS* and RAS* transitioned high. In a CBEDO operation, **control circuitry 138** does not terminate a burst operation when CAS* and RAS* go high, but **looks to WE* for an indication that a burst operation is to be terminated**. (Column 7, lines 52-61 of Cowles; emphasis added).
>
> **To terminate** a continuous burst read operation, **the WE* signal merely has to transition high** prior to a falling edge of the CAS* signal. (Col. 8, ll. 33-36 of Cowles; emphasis added).

[58] However, the state of OE*, arguably, may have little, if anything, to do with generating a predetermined number of internal addresses.

Therefore, since Cowles states that a transition of the signal WE* during a burst can terminate the burst in both the standard BEDO operation and in the continuous BEDO (CBEDO) operation, Cowles explicitly teaches that a premature termination of a row burst can take place.

FIG. 4 of Cowles further evidences that row bursts are interruptible. Specifically, FIG. 4 illustrates a burst access starting at column address "COLn" is terminated (i.e., interrupted) when the signal WE* transitions from low to high.[59] Furthermore, Cowles shows addressing sequences for burst lengths of 2, 4, and 8 cycles.[60] However, FIG. 4 of Cowles illustrates a burst access starting at the column address "COLp" is interrupted after only three cycles by the signal RAS* rising.[61] With regard to the operations illustrated in FIG. 4, Cowles further states:

> It will be appreciated that the read and write operations performed on a single memory row of the memory of FIG. 5 are identical to the operation of the memory of FIG. 1 as shown in FIG. 3. That is, after completing a burst read, the WE* signal transitions low and the next falling edge of CAS* latches a new column address for a burst write operation. **Likewise, the timing diagram of FIG. 4 depicting burst write access cycles followed by burst read cycles can be replicated with the memory of the present invention.** As such, BEDO memory devices can be replaced with CBEDO memory devices without effecting the operation of the memory support system. It will further be appreciated by those skilled in the art that the memory device of FIG. 5 can operate with burst lengths of 2, 4, 8, or full row cycles. (Column 8, lines 37-50 of Cowles; emphasis added).

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[59] See column 6, lines 1-6 of Cowles.

[60] See FIG. 2, column 4, lines 14-18 and column 8, lines 48-50 of Cowles.

[61] See FIG. 4 and column 6, lines 6-9 of Cowles.

Therefore, despite the position taken by the Examiner,[62] Cowles does not disclose or suggest generating a predetermined number of internal address signals, where the generation of the predetermined number of internal address signals is non-interruptible, as presently claimed.

Furthermore, contrary to the position taken by the Examiner,[63] merely because Cowles teaches that a premature termination of a burst may be avoided, it does not necessarily (or logically) follow that the burst is non-interruptible, as presently claimed. Specifically, Cowles recites that:

> To avoid a premature termination of a burst, RAS* cannot transition high until after the last column associated with each row has been latched. (Column 8, lines 63-65 of Cowles).

However, the sentence cited by the Examiner only pertains to termination of a burst in response to a transition of the signal RAS*. The passage is silent with respect to the signal WE*. As discussed above, Cowles discloses that a transition of the signal WE* during a burst can terminate the burst in both the standard BEDO operation and in the continuous BEDO (CBEDO) operation. In particular, Cowles states:

> The control circuit[r]y determines when a current data burst should be terminated based upon the states of RAS* 114, CAS* 124 and WE* 136. In the standard BEDO operation described above, **control circuitry 138 terminated a data burst when WE* transitioned during a burst**, or when both CAS* and RAS* transitioned high. In a CBEDO operation, **control circuitry 138** does not terminate a burst operation when CAS* and RAS* go high, but **looks to WE* for an indication that a burst operation is to be terminated**. (Column 7, lines 52-61 of Cowles; emphasis added).

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[62] See page 2, paragraph no. 3, lines 6-9 of the Office Action mailed October 22, 2002.

[63] See page 2, last two lines through page 3, line 3 of the Office Action mailed October 22, 2002.

> **To terminate** a continuous burst read operation, **the WE* signal merely has to transition high** prior to a falling edge of the CAS* signal. (Col. 8, ll. 33-36 of Cowles; emphasis added).

Cowles expressly states that the method of operation of the memory device includes (i) receiving a signal on a write enable input and (ii) terminating the step of outputting data in response to the signal.[64] Furthermore, the fact that Cowles addresses a way to **avoid** a premature termination of a burst due to the signal RAS* is acknowledgment that the burst **can** be prematurely terminated (i.e.,interrupted). Therefore, the burst is not non-interruptible, as presently claimed.

Because Cowles teaches that a burst can be terminated by at least a transition of a write enable signal WE* during a read or write access, whether in a BEDO or a CBEDO operating mode, Cowles fails to disclose or suggest the **non-interruptible** generation of a predetermined number of internal address signals, as presently claimed. Therefore, Cowles does not disclose or suggest each and every element of the presently pending claim 12, arranged as in the presently pending claim 12. As such, the presently pending claim 12 is fully patentable over the cited reference[65] and the rejection should be reversed.

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[64] See column 11, lines 37-41 and column 12, lines 36-40 of Cowles.

[65] *Brown v. 3M*, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) citing *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383, 58 USPQ2d 1286, 1291 (Fed. Cir. 2001); *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991). *Scripps Clinic & Research Found. V. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991).

7. Group 7 (claims 13, 14 and 16) is fully patentable over Cowles

The presently pending claim 13 provides the steps of (a) accessing a memory in response to a plurality of internal address signals and (b) generating a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, where the generation of the predetermined number of internal address signals is non-interruptible.

Cowles does not disclose or suggest each and every element of the presently pending claim 13, arranged as in claim 13. Specifically, Cowles does not disclose or suggest the non-interruptible generation of the predetermined number of address signals as presently claimed. Cowles is directed to a continuous burst EDO memory device.[66] The Examiner admits that a continuous burst of Cowles is interruptible.[67] Specifically, the Examiner states that he agrees with Appellant's arguments with regard to termination of a continuous burst.[68] In particular, the Examiner admits that the interruptibility of a continuous burst is supported by the following passages in Cowles:[69]

> **To terminate** a continuous burst read operation, **the WE* signal merely has to transition high** prior to a falling edge of the CAS* signal. (Column 8, lines 33-36 of Cowles; emphasis added).
>
> The level of the WE* signal must remain high for read and low for write burst accesses throughout the burst access. **A low to high transition within a burst write access will terminate the burst**

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[66] Title of Cowles.

[67] See page 2, paragraph no. 3, lines 4-6 of the Office Action mailed October 22, 2002.

[68] *Id.*

[69] *Id.*

> **access**, preventing further writes from occurring. **A high to low transition on WE* within a burst read access will likewise terminate the burst read access** and will place the data output 110 in a high impedance state. (Column 7, lines 34-41 of Cowles; emphasis added).

However, the Examiner urges that while a "continuous burst" can be terminated, a "row burst" represents a fixed burst length with no interruption.[70] Despite the position taken by the Examiner, Cowles does not appear to draw such a distinction between bursts. Specifically, with regard to a burst from a BEDO memory, Cowles states:

> Once the memory device begins to output data in a burst read cycle, the output drivers 34 will continue to drive the data lines without tri-stating the data outputs during CAS* high intervals **dependent on the state of the output enable 42 and write enable 36 (OE* and WE*) control lines**, thus allowing additional time for the system to latch the output data. (Column 3, line 65 through column 4, line 4 of Cowles; emphasis added).
>
> The control circuit[r]y determines when a current data burst should be terminated **based upon the state of RAS* 14, CAS* 24 and WE* 36**. (Column 4, lines 63-65 of Cowles; emphasis added).
>
> **The level of the WE* signal must remain high for read and low for write burst accesses throughout the burst access**. A low to high transition within a burst write access will terminate the burst access, preventing further writes from occurring. A high to low transition on WE* within a burst read access will likewise terminate the burst read access and will place the data output 10 in a high impedance state. (Column 5, lines 4-10 of Cowles; emphasis added).
>
> **Both RAS* and CAS* going high during a burst access will also terminate the burst access cycle** placing the data drivers in a high impedance output state, and resetting the burst length counter. (Column 5, lines 25-28 of Cowles; emphasis added).

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[70] See page 2, paragraph no. 3, lines 6-9 of the Office Action mailed October 22, 2002, which appears to suggest that a continuous burst can be terminated or interrupted, while a row burst cannot.

Thus, in BEDO memories, Cowles clearly teaches that there are three conditions that will terminate (i.e., interrupt) a burst access:

1. WE* transitioning, either from low to high or from high to low;

2. RAS* and CAS* going high; or

3. OE* going high.[71]

Cowles is quite clear that WE* transitions will terminate both a row burst and a continuous burst access. In particular, Cowles states:

> The control circuit[r]y determines when a current data burst should be terminated based upon the states of RAS* 114, CAS* 124 and WE* 136. In the standard BEDO operation described above, **control circuitry 138 terminated a data burst when WE* transitioned during a burst**, or when both CAS* and RAS* transitioned high. In a CBEDO operation, **control circuitry 138** does not terminate a burst operation when CAS* and RAS* go high, but **looks to WE* for an indication that a burst operation is to be terminated**. (Column 7, lines 52-61 of Cowles; emphasis added).

> **To terminate** a continuous burst read operation, **the WE* signal merely has to transition high** prior to a falling edge of the CAS* signal. (Col. 8, ll. 33-36 of Cowles; emphasis added).

Therefore, since Cowles states that a transition of the signal WE* during a burst can terminate the burst in both the standard BEDO operation and in the continuous BEDO (CBEDO) operation, Cowles explicitly teaches that a premature termination of a row burst can take place.

FIG. 4 of Cowles further evidences that row bursts are interruptible. Specifically, FIG. 4 illustrates a burst access starting at column address "COLn" is terminated (i.e., interrupted)

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[71] However, the state of OE*, arguably, may have little, if anything, to do with generating a predetermined number of internal addresses.

when the signal WE* transitions from low to high.[72] Furthermore, Cowles shows addressing sequences for burst lengths of 2, 4, and 8 cycles.[73] However, FIG. 4 of Cowles illustrates a burst access starting at the column address "COLp" is interrupted after only three cycles by the signal RAS* rising.[74] With regard to the operations illustrated in FIG. 4, Cowles further states:

> It will be appreciated that the read and write operations performed on a single memory row of the memory of FIG. 5 are identical to the operation of the memory of FIG. 1 as shown in FIG. 3. That is, after completing a burst read, the WE* signal transitions low and the next falling edge of CAS* latches a new column address for a burst write operation. **Likewise, the timing diagram of FIG. 4 depicting burst write access cycles followed by burst read cycles can be replicated with the memory of the present invention.** As such, BEDO memory devices can be replaced with CBEDO memory devices without effecting the operation of the memory support system. It will further be appreciated by those skilled in the art that the memory device of FIG. 5 can operate with burst lengths of 2, 4, 8, or full row cycles. (Column 8, lines 37-50 of Cowles; emphasis added).

Therefore, despite the position taken by the Examiner,[75] Cowles does not disclose or suggest generating a predetermined number of internal address signals, where the generation of the predetermined number of internal address signals is non-interruptible, as presently claimed.

Furthermore, contrary to the position taken by the Examiner,[76] merely because Cowles teaches that a premature termination of a burst may be avoided, it does not necessarily (or

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[72] See column 6, lines 1-6 of Cowles.

[73] See FIG. 2, column 4, lines 14-18 and column 8, lines 48-50 of Cowles.

[74] See FIG. 4 and column 6, lines 6-9 of Cowles.

[75] See page 2, paragraph no. 3, lines 6-9 of the Office Action mailed October 22, 2002.

[76] See page 2, last two lines through page 3, line 3 of the Office Action mailed October 22, 2002.

logically) follow that the burst is non-interruptible, as presently claimed. Specifically, Cowles recites that:

> To avoid a premature termination of a burst, RAS* cannot transition high until after the last column associated with each row has been latched. (Column 8, lines 63-65 of Cowles).

However, the sentence cited by the Examiner only pertains to termination of a burst in response to a transition of the signal RAS*. The passage is silent with respect to the signal WE*. As discussed above, Cowles discloses that a transition of the signal WE* during a burst can terminate the burst in both the standard BEDO operation and in the continuous BEDO (CBEDO) operation. In particular, Cowles states:

> The control circuit[r]y determines when a current data burst should be terminated based upon the states of RAS* 114, CAS* 124 and WE* 136. In the standard BEDO operation described above, **control circuitry 138 terminated a data burst when WE* transitioned during a burst**, or when both CAS* and RAS* transitioned high. In a CBEDO operation, **control circuitry 138** does not terminate a burst operation when CAS* and RAS* go high, but **looks to WE* for an indication that a burst operation is to be terminated**. (Column 7, lines 52-61 of Cowles; emphasis added).
>
> **To terminate** a continuous burst read operation, **the WE* signal merely has to transition high** prior to a falling edge of the CAS* signal. (Col. 8, ll. 33-36 of Cowles; emphasis added).

Cowles expressly states that the method of operation of the memory device includes (i) receiving a signal on a write enable input and (ii) terminating the step of outputting data in response to the signal.[77] Furthermore, the fact that Cowles addresses a way to **avoid** a premature termination of a burst due to the signal RAS* is acknowledgment that the burst **can** be prematurely terminated (i.e.,interrupted). Therefore, the burst is not non-interruptible, as presently claimed.

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[77] See column 11, lines 37-41 and column 12, lines 36-40 of Cowles.

Because Cowles teaches that a burst can be terminated by at least a transition of a write enable signal WE* during a read or write access, whether in a BEDO or a CBEDO operating mode, Cowles fails to disclose or suggest the **non-interruptible** generation of a predetermined number of internal address signals, as presently claimed. Therefore, Cowles does not disclose or suggest each and every element of the presently pending claim 13, arranged as in the presently pending claim 13. As such, the claims of Group 7 are fully patentable over the cited reference[78] and the rejection should be reversed.

8. Group 8 (claim 15) is fully patentable over Cowles

Claim 15 depends indirectly from claim 13 and, therefore, includes the limitations of claim 13. Consequently, the arguments presented in support of the patentability of claim 13 are hereby incorporated by reference in support of claim 15. Claim 15 further recites that a programming step is performed using bond options.

Cowles does not disclose or suggest each and every element of the presently pending claim 6. Specifically, Cowles is silent regarding bond options.[79] In particular, the Office Action fails to point to any specific language or figure in Cowles that is considered to disclose or suggest

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[78] *Brown v. 3M*, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) citing *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383, 58 USPQ2d 1286, 1291 (Fed. Cir. 2001); *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991). *Scripps Clinic & Research Found. V. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991).

[79] Appellant's representative has downloaded an electric version of the Cowles reference and performed a search for the words "bond" and "bond option", with no such occurrences.

a programming step **performed using bond options**, as presently claimed.[80] Furthermore, the position taken in the Office Action that "it is well known in the art to include multiple modes of operation selected by bond options"[81] does not adequately address the deficiencies of Cowles to support the rejection under 35 U.S.C. § 102. In particular, the Federal Circuit has stated:

> To serve as anticipation, when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is **necessarily present** in the thing described in the reference, and it would be so recognized by persons of ordinary skill.[82]

Even assuming, *arguendo*, it is well known in the art to include multiple modes of operation selected by bond options as urged by the Examiner,[83] the Examiner failed to present any evidence that a person of ordinary skill would recognize a programming step performed **using bond options**, as necessarily present in Cowles. Inherency requires certainty of results, not mere possibility.[84] Therefore, because Cowles does not disclose or suggest each and every element of the presently pending claim 15, arranged as in the present claim 15, the Examiner has not met the

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[80] See page 6, lines 9-12 of the Office Action mailed October 22, 2002.

[81] See page 6, lines 9-12 of the Office Action mailed October 22, 2002.

[82] Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 20 USPQ 2d 1746, 1749 (Fed. Cir. 1991) (citations omitted, emphasis added) See also In re Sun, 31 USPQ 2d 1451, 1453 (Fed. Cir. 1993) (unpublished) ("under section 102(b), anticipation requires that the prior art reference disclose either expressly or under the principles of inherency, every limitation of the claim").

[83] See page 6, lines 9-12 of the Office Action mailed October 22, 2002.

[84] See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). See also, In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981).

Office's burden of factually establishing a *prima facie* case of anticipation.[85] As such, the presently pending claim 15 is fully patentable over Cowles and the rejection should be reversed.

9. Group 9 (claim 17) is fully patentable over Cowles

Claim 17 depends directly from claim 13 and, therefore, includes the limitations of claim 13. Consequently, the arguments presented in support of the patentability of claim 13 are hereby incorporated by reference in support of claim 17. Claim 17 further recites the step of selecting the predetermined number of internal address signals to provide time for at least one writeback or refresh cycle.[86]

Cowles does not disclose or suggest each and every element of the presently pending claim 17. Specifically, Cowles is silent regarding selecting the predetermined number of internal address signals **to provide time for at least one writeback or refresh cycle**, as presently claimed.[87] In particular, the lines of Cowles cited by the Examiner in support of the rejection do not address selecting the predetermined number of internal address signals **to provide time for at least one writeback or refresh cycle**, as presently claimed.[88] The Federal Circuit has stated:

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[85] *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). (Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim). *In re* Skinner, 2 USPQ2d 1788, 1788-89 (B.P.A.I. 1986)("[i]t is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office"). *See also Ex parte* Natale, 11 USPQ2d 1222, 1226 (B.P.A.I. 1989) .

[86] See page 3, paragraph no. 12 of the final Office Action dated May 24, 2002.

[87] Appellant's representative has downloaded an electric version of the Cowles reference and performed a search for the words "writeback" and "refresh", with no such occurrences.

[88] See page 6, line 20 through page 7, line 2 of the Office Action mailed October 22, 2002.

> To serve as anticipation, when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and it would be so recognized by persons of ordinary skill.[89]

The Examiner failed to present any evidence that a person of ordinary skill would recognize that selecting a burst length to provide time for at least one writeback or refresh cycle is necessarily present in Cowles.[90] Specifically, the sections of Cowles cited by the Examiner in support of the rejection of claim 17 provide:

> To terminate a continuous burst read operation, the WE* signal merely has to transition high prior to a falling edge of the CAS* signal.
>
> ***
>
> To avoid a premature termination of a burst, RAS* cannot transition high until after the last column associated with each row has been latched.[91]

The portions of Cowles cited by the Examiner are silent regarding selecting the predetermined number of internal address signals to provide time for at least one writeback or refresh cycle, as presently claimed. Furthermore, the Examiner provided no line of reasoning why the passages were considered to make clear that the missing descriptive matter was necessarily present in the memory

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[89] Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 20 USPQ 2d 1746, 1749 (Fed. Cir. 1991) (citations omitted) See also In re Sun, 31 USPQ 2d 1451, 1453 (Fed. Cir. 1993) (unpublished) ("under section 102(b), anticipation requires that the prior art reference disclose either expressly or under the principles of inherency, every limitation of the claim").

[90] See page 6, line 20 through page 7, line 2 of the Office Action mailed October 22, 2002.

[91] See page 6, line 20 through page 7, line 2 of the Office Action mailed October 22, 2002 (citing column 8, lines 33-36 and 63-65 of Cowles).

device of Cowles. Inherency requires certainty of results, not mere possibility.[92] Therefore, because Cowles does not disclose or suggest each and every element of the presently pending claim 17, arranged as in the present claim 17, the Examiner failed to meet the Office's burden of factually establishing a *prima facie* case of anticipation.[93] As such, the presently pending claim 17 is fully patentable over the cited reference and the rejection should be reversed.

10. Group 10 (claim 21) is fully patentable over Cowles

Claim 21 depends directly from claim 1 and, therefore, includes the limitations of claim 1. Consequently, the arguments presented in support of the patentability of claim 1 are hereby incorporated by reference in support of claim 21. Claim 21 further recites that the circuit further comprises address and control busses configured to present the external address signal and one or more control signals, where the busses are **freed up during the generation of the predetermined number of internal address signals**.

Cowles does not disclose or suggest each and every element of the presently pending claim 21, arranged as in the presently pending claim 21. Specifically, Cowles is silent regarding address and control busses configured to present the external address signal and one or more control signals, where the busses are **freed up during the generation of the predetermined number of**

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[92] See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). See also, In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981).

[93] *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). (Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim). *In re* Skinner, 2 USPQ2d 1788, 1788-89 (B.P.A.I. 1986)("[i]t is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office"). *See also Ex parte* Natale, 11 USPQ2d 1222, 1226 (B.P.A.I. 1989).

internal address signals, as presently claimed.[94] In particular, the lines of Cowles cited by the Examiner in support of the rejection do not address address and control busses configured to present the external address signal and one or more control signals, where the busses are **freed up during the generation of the predetermined number of internal address signals**, as presently claimed.[95] Furthermore, the Federal Circuit has stated:

> To serve as anticipation, when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and it would be so recognized by persons of ordinary skill.[96]

The Examiner failed to present any evidence that a person of ordinary skill would recognize that Cowles necessarily presents address and control busses configured to present the external address signal and one or more control signals, where the busses are **freed up during the generation of the predetermined number of internal address signals**, as presently claimed.[97] Inherency requires certainty of results, not mere possibility.[98] Therefore, because Cowles does not

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[94] Appellant's representative has downloaded an electric version of the Cowles reference and performed a search for the words "free," "freed up," "share" and "sharing", with no such occurrences.

[95] See page 7, lines 15-19 of the Office Action mailed October 22, 2002.

[96] Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 20 USPQ 2d 1746, 1749 (Fed. Cir. 1991) (citations omitted) See also In re Sun, 31 USPQ 2d 1451, 1453 (Fed. Cir. 1993) (unpublished) ("under section 102(b), anticipation requires that the prior art reference disclose either expressly or under the principles of inherency, every limitation of the claim").

[97] See page 7, lines 15-19 of the Office Action mailed October 22, 2002.

[98] See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). See also, In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981).

disclose or suggest each and every element of the presently pending claim 21, arranged as in the present claim 21, the Examiner failed to meet the Office's burden of factually establishing a *prima facie* case of anticipation.[99] As such, the presently pending claim 21 is fully patentable over the cited reference and the rejection should be reversed.

B. CONCLUSION

Cowles does not disclose or suggest a logic circuit configured to generate a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, where the generation of the predetermined number of internal address signals is **non-interruptible**, as presently claimed. Hence, the Examiner has clearly erred with respect to the patentability of the claimed invention. It is respectfully requested that the Board overturn the Examiner's rejection of all pending claims, and hold that the

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[99] *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). (Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim). *In re* Skinner, 2 USPQ2d 1788, 1788-89 (B.P.A.I. 1986) ("[i]t is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office"). *See also Ex parte* Natale, 11 USPQ2d 1222, 1226 (B.P.A.I. 1989).

claims are not rendered anticipated or obvious by the cited reference. However, should the Board find the arguments herein in support of independent claims 1, 12 and/or 13 unpersuasive, the Board is respectfully requested to carefully consider the arguments set forth above in support of each of the independently patentable groups.

Respectfully submitted,

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Dated: March 24, 2003

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IX. APPENDIX

CLAIMS IN CURRENT FORM

1. (AMENDED) A circuit comprising:

a memory comprising a plurality of storage elements each configured to read and write data in response to an internal address signal; and

a logic circuit configured to generate a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

2. (AMENDED) The circuit according to claim 1, wherein said predetermined number of internal address signals is determined by a fixed burst length.

3. (AMENDED) The circuit according to claim 1, wherein said predetermined number of internal address signals is at least 4.

4. (AMENDED) The circuit according to claim 1, wherein said predetermined number of internal address signals is 8.

5. (AMENDED) The circuit according to claim 2, wherein said fixed burst length is programmable.

6. (AMENDED) The circuit according to claim 5, wherein said fixed burst length is programmed by bond options.

7. (AMENDED) The circuit according to claim 5, wherein said fixed burst length is programmed by voltage levels on external pins.

8. (AMENDED) The circuit according to claim 1, wherein said memory comprises a static random access memory.

9. (AMENDED) The circuit according to claim 1, wherein said memory comprises a dynamic random access memory.

10. (AMENDED) The circuit according to claim 9, wherein said predetermined number of internal address signals is chosen to provide time for at least one writeback or refresh cycle.

11. (AMENDED) The circuit according to claim 1, wherein said predetermined number of internal address signals is chosen to meet predetermined criteria for sharing address and control busses.

12. (AMENDED) A circuit comprising:

means for reading data from and writing data to a plurality of storage elements in response to a plurality of internal address signals; and

means for generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

13. (AMENDED) A method of providing a fixed burst length data transfer comprising the steps of:

accessing a memory in response to a plurality of internal address signals; and

generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) a control signal, wherein said generation

of said predetermined number of internal address signals is non-interruptible.

14. The method according to claim 13, further comprising the step of programming said predetermined number.

15. The method according to claim 14, wherein said programming step is performed using bond options.

16. The method according to claim 14, wherein said programming step is performed using voltage levels.

17. (AMENDED) The method according to claim 13, further comprising the step of selecting said predetermined number to provide time for at least one writeback or refresh cycle.

18. The circuit according to claim 1, wherein said logic circuit comprises a counter configured to generate said predetermined number of internal address signals.

19. (AMENDED) The circuit according to claim 1, wherein said external address signal comprises an initial address for data transfers to and from said memory.

20. A memory device according to claim 1, wherein said circuit is an integrated circuit.

21. (AMENDED) The circuit according to claim 1, further comprising address and control busses configured to present said external address signal and said one or more control signals, wherein said busses are freed up during the generation of said predetermined number of internal address signals.

#12

Attorney Docket: 0325.00309

IN RE APPLICATION OF:	Cathal G. Phelan	**RESPONSE TRANSMITTAL AND EXTENSION OF TIME REQUEST (IF REQUIRED)**
SERIAL NO.:	09/504,344	
TITLE:	FIXED BURST MEMORIES	
FILED:	February 14, 2000	
EXAMINER:	Namzai, M.	
ART UNIT:	2187	

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Sir:

Enclosed please find an appeal brief and a postcard along with the fee calculation below:

FEE CALCULATION FOR ENCLOSED AND EXTENSION REQUEST (IF ANY)

	Claims Remaining	Highest No. Previous	Extra Rate	Additional Fee
Total Claims	21 minus	21 =	0 x $ 18.00	$ 0.00
Independent Claims	3 minus	3 =	0 x $ 84.00	$ 0.00
Multiple Dependent Claim First Added			+ $280.00	$ 0.00

TOTAL IF NOT SMALL ENTITY .. $0.00

[ ] SMALL ENTITY STATUS - If applicable, divide by 2 ..... $0.00
[ ] Verified statement enclosed, if not previously filed.

[ ] Applicant also requests a _____ month extension of time for response to the outstanding Office Action. The fee is $0.00

[X] Fee set forth for Appeal Brief $320.00

TOTAL FEE $320.00

The Commissioner is hereby authorized to charge any overpayment or underpayment of the above fee associated with this Communication to Deposit Account No. 50-0541. A duplicate copy of this sheet is attached.

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Robert M. Miller
Registration No.: 42,892

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on March 24, 2003.

By: Mary Donna Berkley
Mary Donna Berkley

Notice of Allowability	Application No.	Applicant(s)	
	09/504,344	PHELAN, CATHAL G.	
	Examiner	Art Unit	
	Mehdi Namazi	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *03/28/2003*.
2. ☒ The allowed claim(s) is/are *1-21*.
3. ☐ The drawings filed on _____ are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.
5. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
   (a) ☐ The translation of the foreign language provisional application has been received.
6. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE**

7. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

8. ☒ CORRECTED DRAWINGS must be submitted.
   (a) ☒ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☒ to Paper No. *3*.
   (b) ☐ including changes required by the proposed drawing correction filed _____, which has been approved by the Examiner.
   (c) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No. _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet.

9. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1☐ Notice of References Cited (PTO-892)
2☐ Notice of Informal Patent Application (PTO-152)
3☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
4☐ Interview Summary (PTO-413), Paper No.____ .
5☐ Information Disclosure Statements (PTO-1449), Paper No. ____.
6☐ Examiner's Amendment/Comment
7☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
8☒ Examiner's Statement of Reasons for Allowance
9☐ Other .

DETAILED ACTION

Drawings

1. The application having been allowed, formal drawings are required in response to this Office Action.

Allowable Subject Matter

2. The following is an examiner's statement of reasons for allowance: the prior art discloses an integrated circuit memory device which can operate at high data speeds. The integrated circuit memory can output data of a "fixed burst length" in a continuous stream while rows of the memory are accessed. However, to terminate a continuous burst read operation, the WE signal merely has to transition high prior to a falling edge of the CAS signal(see, for example, Cowles). thus prior art of record does not teach or fairly suggest the non-interruptible generation of a predetermined number of internal address signals. Accordingly, the invention as claimed is not seen to be anticipated or made obvious, within the meaning of 35 U.S.C. 103, by the prior art of record.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to

avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mehdi Namazi whose telephone number is (703) 306-2758. The examiner can normally be reached on Monday-Friday from 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks, can be reached on (703) 308-1756. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-9600.

M. Namazi
June 13, 2003

Donald A. Sparks
Supervisory Patent Examiner
TC 2100

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

021363 7590 06/16/2003

CHRISTOPHER P. MAIORANA, P.C.
24025 GREATER MACK
SUITE 200
ST. CLAIR SHORES, MI 48080

EXAMINER	
NAMAZI, MEHDI	
ART UNIT	**CLASS-SUBCLASS**
2188	711-104000

DATE MAILED: 06/16/2003

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/504,344	02/14/2000	Cathal G. Phelan	0325.000309	7771

TITLE OF INVENTION: MEMORY DEVICE WITH FIXED LENGTH NON-INTERRUPTIBLE BURST

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1300	$0	$1300	09/16/2003

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status is changed, pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above and notify the United States Patent and Trademark Office of the change in status, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check the box below and enclose the PUBLICATION FEE and 1/2 the ISSUE FEE shown above.

☐ Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (REV. 05-03) Approved for use through 04/30/2004.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
Alexandria, Virginia 22313-1450
Fax (703)746-4000

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

021363 7590 06/16/2003

CHRISTOPHER P. MAIORANA, P.C.
24025 GREATER MACK
SUITE 200
ST. CLAIR SHORES, MI 48080

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above, or being facsimile transmitted to the USPTO, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/504,344	02/14/2000	Cathal G. Phelan	0325.000309	7771

TITLE OF INVENTION: MEMORY DEVICE WITH FIXED LENGTH NON-INTERRUPTIBLE BURST

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1300	$0	$1300	09/16/2003

EXAMINER	ART UNIT	CLASS-SUBCLASS
NAMAZI, MEHDI	2188	711-104000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the USPTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) ❑ individual ❑ corporation or other private group entity ❑ government

4a. The following fee(s) are enclosed:

❑ Issue Fee

❑ Publication Fee

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s):

❑ A check in the amount of the fee(s) is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Commissioner is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

Commissioner for Patents is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

(Authorized Signature) (Date)

NOTE; The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMIT THIS FORM WITH FEE(S)

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/504,344	02/14/2000	Cathal G. Phelan	0325.000309	7771

021363 7590 06/16/2003

CHRISTOPHER P. MAIORANA, P.C.
24025 GREATER MACK
SUITE 200
ST. CLAIR SHORES, MI 48080
UNITED STATES

EXAMINER	
NAMAZI, MEHDI	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 06/16/2003

Determination of Patent Term Extension under 35 U.S.C. 154 (b)
(application filed after June 7, 1995 but prior to May 29, 2000)

The patent term extension is 0 days. Any patent to issue from the above identified application will include an indication of the 0 day extension on the front page.

If a continued prosecution application (CPA) was filed in the above-identified application, the filing date that determines patent term extension is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) system. (http://pair.uspto.gov)

Any questions regarding the patent term extension or adjustment determination should be directed to the Office of Patent Legal Administration at (703)305-1383.

PTOL-85 (REV. 05-03) Approved for use through 04/30/2004.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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021363 7590 06/16/2003

CHRISTOPHER P. MAIORANA, P.C.
24025 GREATER MACK
SUITE 200
ST. CLAIR SHORES, MI 48080
UNITED STATES

EXAMINER	
NAMAZI, MEHDI	
ART UNIT	**PAPER NUMBER**
2188	13

DATE MAILED: 06/16/2003

Notice of Fee Increase on January 1, 2003

If a reply to a "Notice of Allowance and Fee(s) Due" is filed in the Office on or after January 1, 2003, then the amount due will be higher than that set forth in the "Notice of Allowance and Fee(s) Due" since there will be an increase in fees effective on January 1, 2003. See Revision of Patent and Trademark Fees for Fiscal Year 2003; Final Rule, 67 Fed. Reg. 70847, 70849 (November 27, 2002).

The current fee schedule is accessible from: http://www.uspto.gov/main/howtofees.htm.

If the issue fee paid is the amount shown on the "Notice of Allowance and Fee(s) Due," but not the correct amount in view of the fee increase, a "Notice to Pay Balance of Issue Fee" will be mailed to applicant. In order to avoid processing delays associated with mailing of a "Notice to Pay Balance of Issue Fee," if the response to the Notice of Allowance and Fee(s) due form is to be filed on or after January 1, 2003 (or mailed with a certificate of mailing on or after January 1, 2003), the issue fee paid should be the fee that is required at the time the fee is paid. If the issue fee was previously paid, and the response to the "Notice of Allowance and Fee(s) Due" includes a request to apply a previously-paid issue fee to the issue fee now due, then the difference between the issue fee amount at the time the response is filed and the previously paid issue fee should be paid. See Manual of Patent Examining Procedure, Section 1308.01 (Eighth Edition, August 2001).

Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

PTOL-85 (REV. 05-03) Approved for use through 04/30/2004.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#14 MC

Group Art Unit:	2188
Examiner:	Namazi, M.
Applicants:	Cathal G. Phelan
Serial No:	09/504,344
Filing Date:	February 14, 2000
For:	MEMORY DEVICE WITH FIXED LENGTH NON-INTERRUPTIBLE BURST

DRAWING TRANSMITTAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Notice of Allowance mailed June 16, 2003 indicating that formal drawings are due, enclosed are three (3) sheets of formal drawings.

Respectfully submitted,

By: _____
Christopher P. Maiorana
Registration No. 42,829
CHRISTOPHER P. MAIORANA, P.C.
24025 Greater Mack, Suite 200
St. Clair Shores, Michigan 48080
(586) 498-0670

Date: September 15, 2003

Attorney Docket No.: 0325.00309

CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service via First Class Mail in an envelope with sufficient postage and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on September 15, 2003.

By: Mary Donna Berkley
Mary Donna Berkley

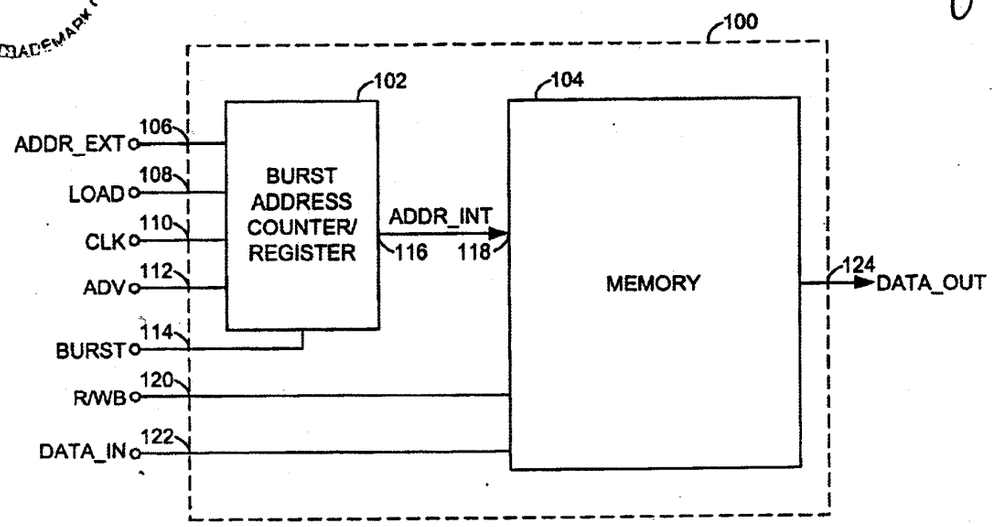

FIG. 1

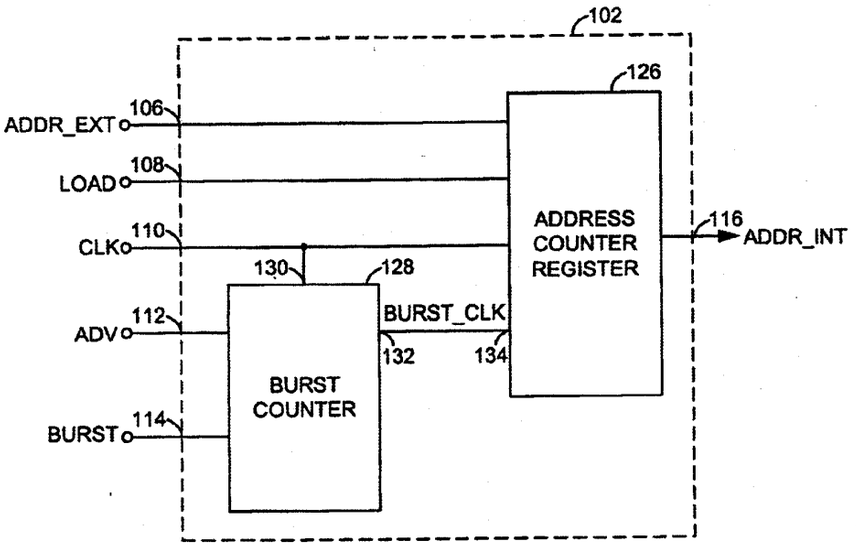

FIG. 2

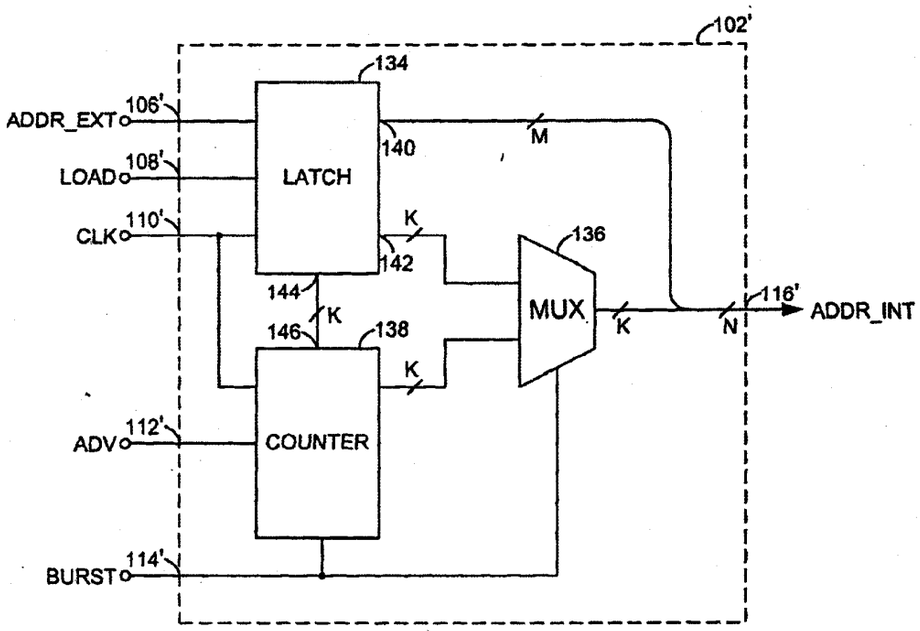

FIG. 3

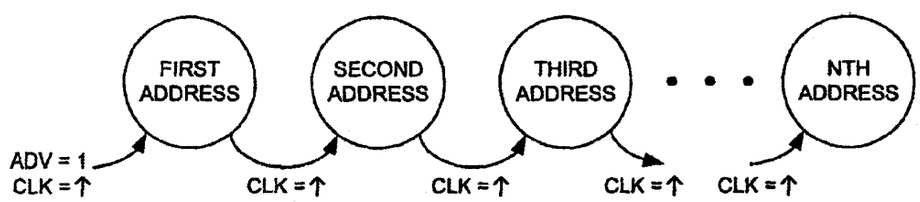

FIG. 4

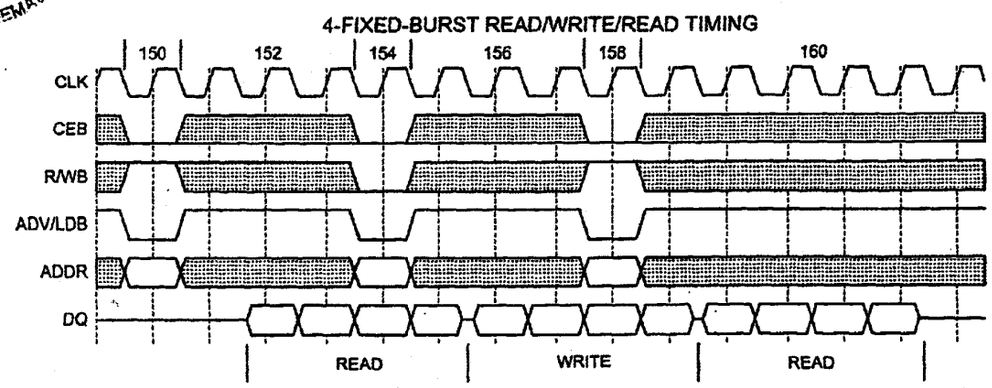

FIG. 5A

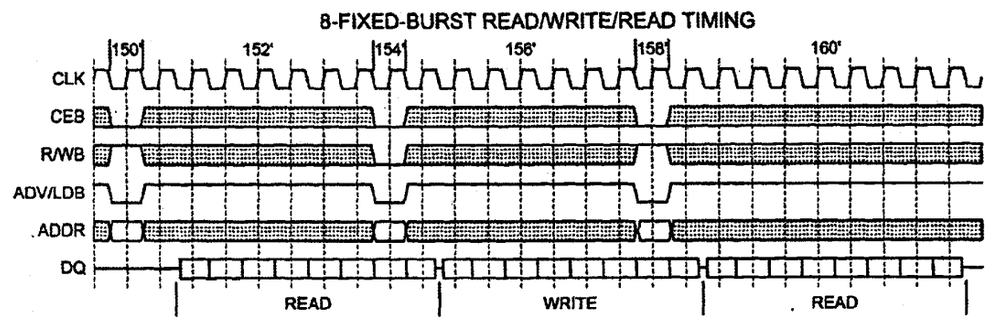

FIG. 5B

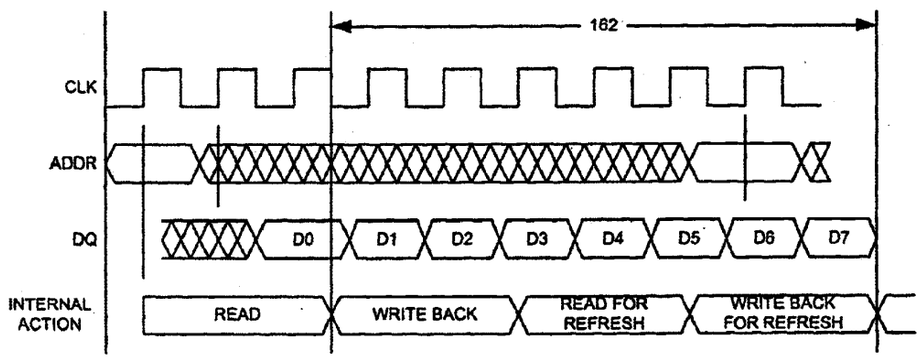

FIG. 6

OIPE SC103 SEP 17 2003 PATENT & TRADEMARK OFFICE

B

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
Alexandria, Virginia 22313-1450
Fax (703)746-4000

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

021363 7590 06/16/2003

CHRISTOPHER P. MAIORANA, P.C.
24025 GREATER MACK
SUITE 200
ST. CLAIR SHORES, MI 48080

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above, or being facsimile transmitted to the USPTO, on the date indicated below.

Mary Donna Berkley	(Depositor's name)
Mary Donna Berkley	(Signature)
September 15, 2003	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/504,344	02/14/2000	Cathal G. Phelan	0325.000309	7771

TITLE OF INVENTION: MEMORY DEVICE WITH FIXED LENGTH NON-INTERRUPTIBLE BURST

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1300	$0	$1300	09/16/2003

EXAMINER	ART UNIT	CLASS-SUBCLASS
NAMAZI, MEHDI	2188	711-104000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Christopher P. Maiorana, P.C.
2 Robert M. Miller
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the USPTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Cypress Semiconductor Corp. San Jose, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) ☐ individual ☒ corporation or other private group entity ☐ government

4a. The following fee(s) are enclosed:

☒ Issue Fee
☐ Publication Fee
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):

☐ A check in the amount of the fee(s) is enclosed.
☒ Payment by credit card. Form PTO-2038 is attached. Deduct fee from Deposit Account
☒ The Commissioner is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 50-0541 (enclose an extra copy of this form).

Commissioner for Patents is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

(Authorized Signature) (Date) 09/15/03

Christopher P. Maiorana (42,829)

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

09/504,344 09/23/2003 TLUONG 00000004 500541
01 FC:1501 1300.00 DA

TRANSMIT THIS FORM WITH FEE(S)

PATENT APPLICATION FEE DETERMINATION RECORD
Effective December 29, 1999

Application or Docket Number: 09/504344

CLAIMS AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA
BASIC FEE		
TOTAL CLAIMS	17 minus 20=	*
INDEPENDENT CLAIMS	3 minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT		

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
	345.00	OR		690.00
X$ 9=		OR	X$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL		OR	TOTAL	690

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 20	Minus	** 20	= 1
Independent	* 3	Minus	*** 3	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 21	Minus	** 20	= 1
Independent	* 3	Minus	*** 3	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	18.00
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

ISSUE SLIP STAPLE AREA (for additional cross references)

POSITION	INITIALS	ID NO.	DATE
FEE DETERMINATION	SM		2/23/02
O.I.P.E. CLASSIFIER		16	3300
FORMALITY REVIEW			
RESPONSE FORMALITY REVIEW			
	DMN	64830	5.2

INDEX OF CLAIMS

✔ ..... Rejected
= ..... Allowed
— (Through numeral)... Canceled
÷ ..... Restricted
N ..... Non-elected
I ..... Interference
A ..... Appeal
O ..... Objected

Claim Final	Claim Original	Date 9/27/01	Date 9/21/01	Date 10/18/02	Date 6/12/03
1	1	✔	✔	✔	=
2	2				=
3	3				=
4	4				=
5	5				=
6	6				=
7	7				=
8	8				=
9	9				=
10	10				=
11	11				=
16	12				=
17	13				=
18	14				=
19	15				=
20	16				=
21	17	✔			=
12	18				=
13	19				=
14	20		✔		=
15	21			✔	=
	22				
	23				
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Claim Final	Claim Original	Date
	51	
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Claim Final	Claim Original	Date
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	150	

If more than 150 claims or 10 actions
staple additional sheet here

(LEFT INSIDE)

MULTIPLE DEPENDENT CLAIM FEE CALCULATION SHEET
(FOR USE WITH FORM PTO-875)

SERIAL NO. | FILING DATE

APPLICANT(S)

CLAIMS

	AS FILED		AFTER 1st AMENDMENT		AFTER 2nd AMENDMENT	
	IND.	DEP.	IND.	DEP.	IND.	DEP.
1	1					
2		1				
3		1				
4		1				
5		1				
6		1				
7		1				
8		1				
9		1				
10		1				
11		1				
12	1					
13	1					
14		1				
15		1				
16		1				
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49						
50						
TOTAL IND.	3					
TOTAL DEP.	14					
TOTAL	17					

	IND.	DEP.	IND.	DEP.	IND.	DEP.
51						
52						
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100						
TOTAL IND.						
TOTAL DEP.						
TOTAL						

SEARCHED

Class	Sub.	Date	Exmr.
711	104-105	~~9/26/01~~	M.N
	169		
	167		
365	233		
	238.5		
710	35	9/26/01	M.N
U.P date search		4-19-02	M.N
U.P date search		10-18-02	M.N
U.P date search		6-12-03	M.N

INTERFERENCE SEARCHED

Class	Sub.	Date	Exmr.
711	104		
	105		
	169		
	167		
365	233		
	238.5		
710	35		

SEARCH NOTES
(INCLUDING SEARCH STRATEGY)

	Date	Exmr.
Clm Cas3ge	9-25-01	M.N
Reginald Bragdon	9-26-01	M.N
EAST	9-26-01	M.N
Clm Cas3ge	4-19-02	M.N
EAST	4-19-02	M.N
Reginald Bragdon	10-18-02	M.N
Clm Cas3ge	6-13-03	M.N
EAST	6-13-03	M.N

(RIGHT OUTSIDE)