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Phelan

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- (54) **MEMORY DEVICE WITH FIXED LENGTH NON INTERRUPTIBLE BURST**
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- (52) **U.S. Cl.** 711/104; 711/105; 711/167; 711/169; 710/35; 365/233; 365/238.5
- (58) **Field of Search** 711/104-105, 169, 711/167; 365/233, 238.5; 710/35
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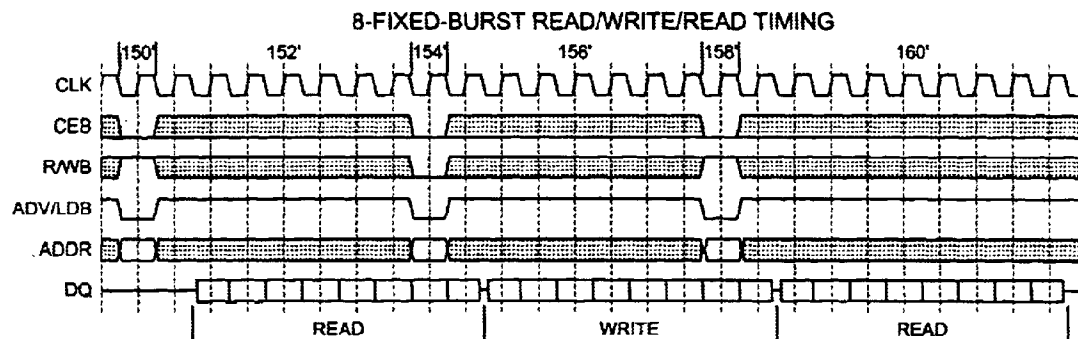
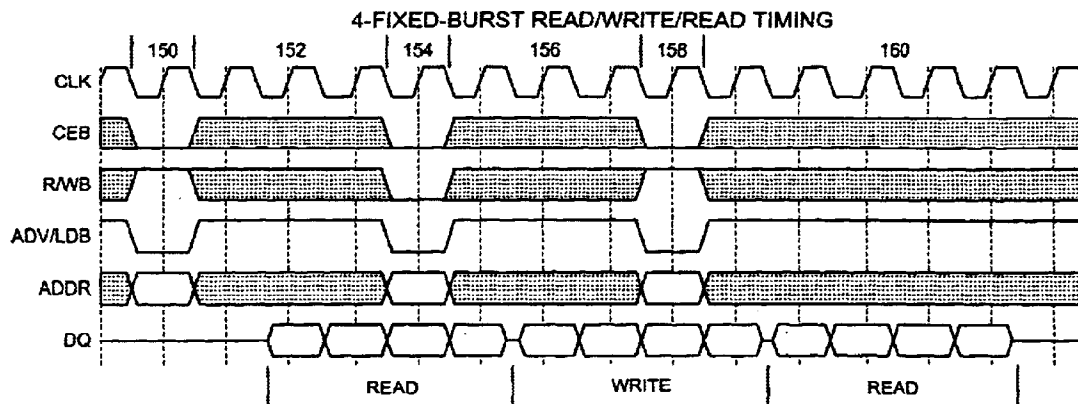
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(57) **ABSTRACT**

An integrated circuit comprising a memory and a logic circuit. The memory may comprise a plurality of storage elements each configured to read and write data in response to an internal address signal. The logic circuit may be configured to generate a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals. The generation of the predetermined number of internal address signals may be non-interruptible.

21 Claims, 3 Drawing Sheets



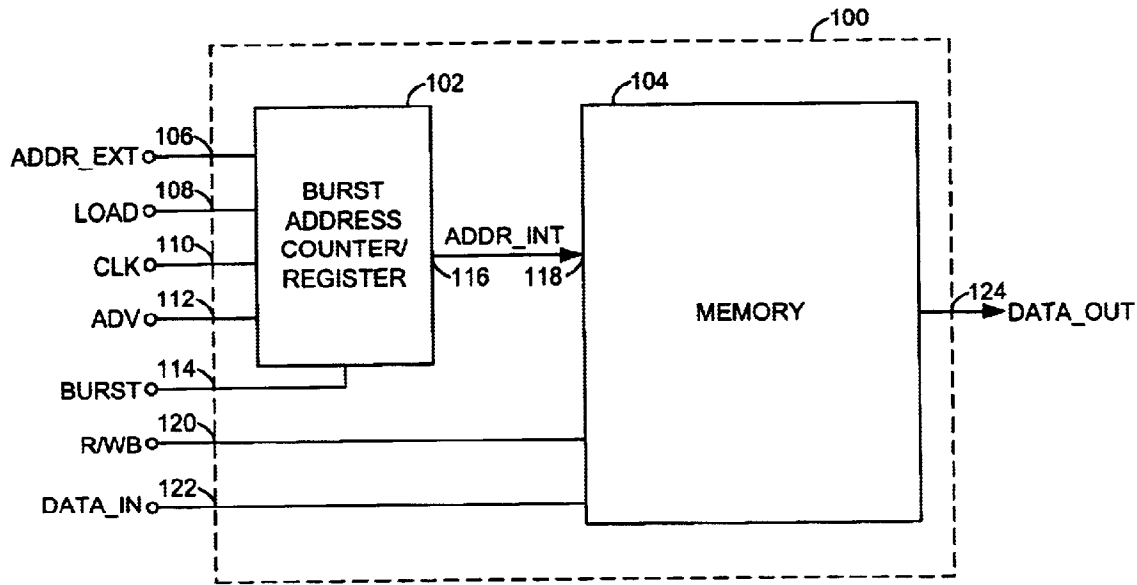


FIG. 1

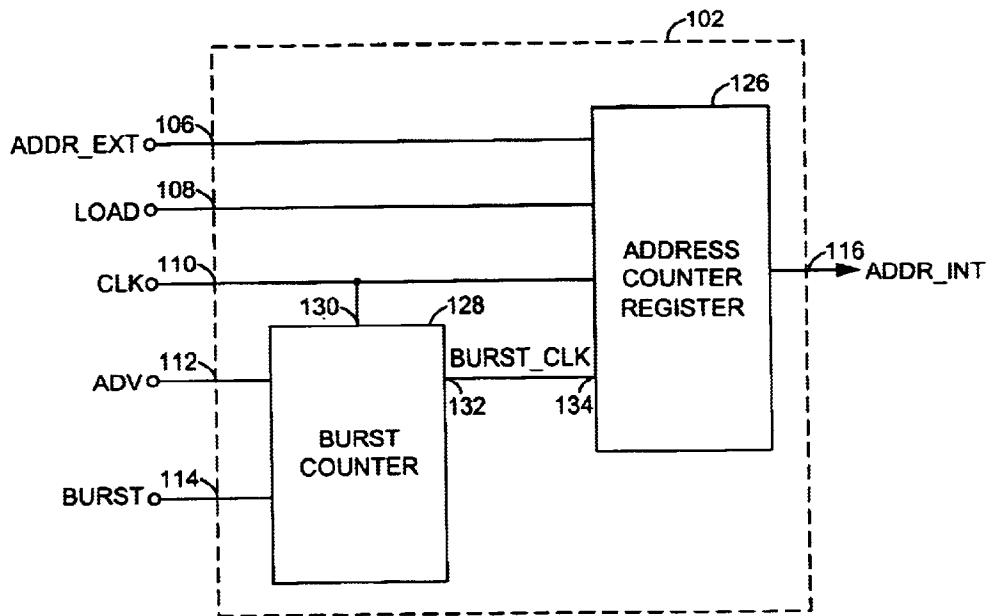


FIG. 2

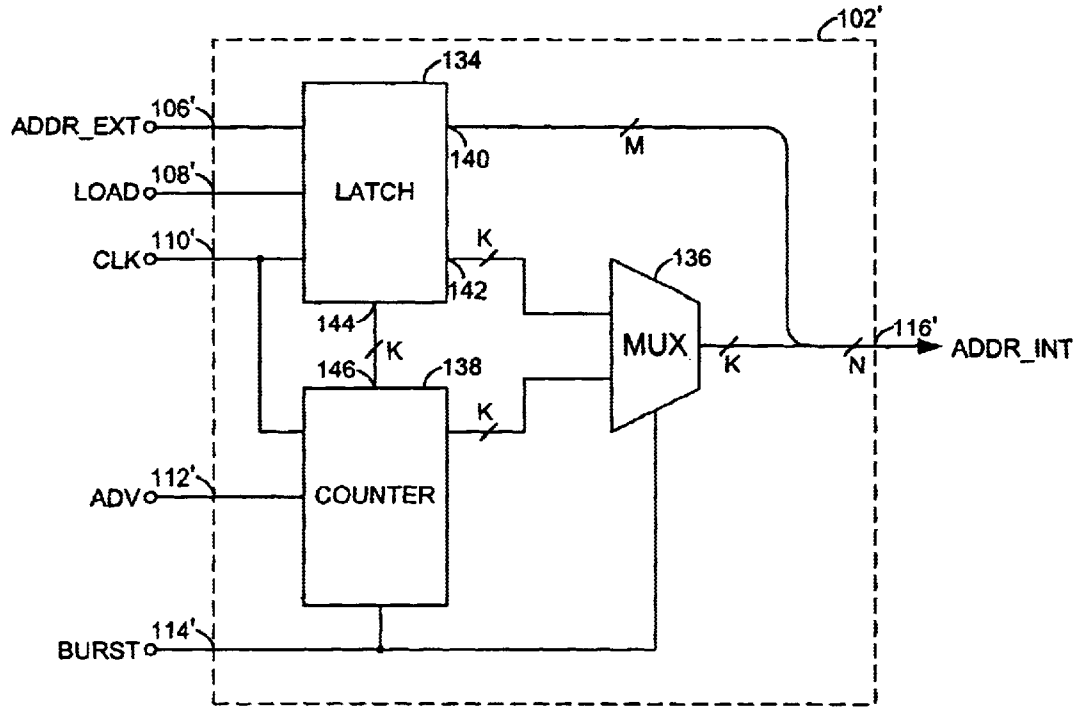


FIG. 3

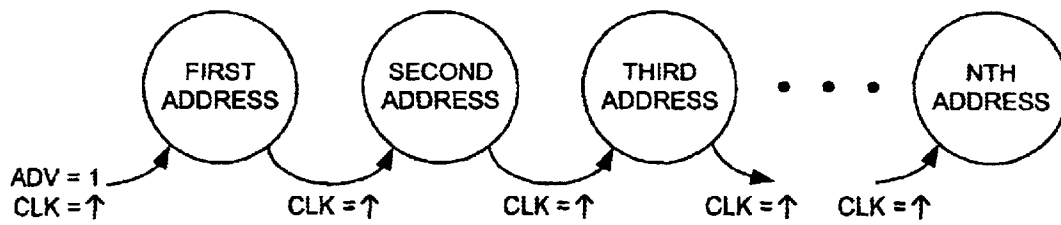


FIG. 4

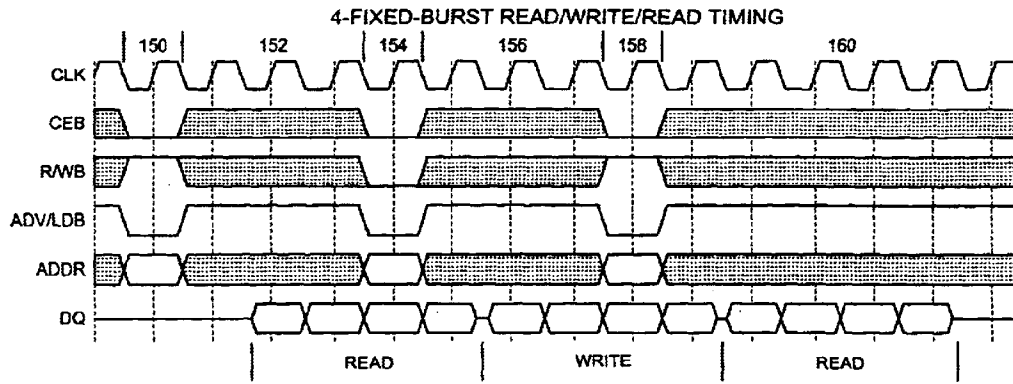


FIG. 5A

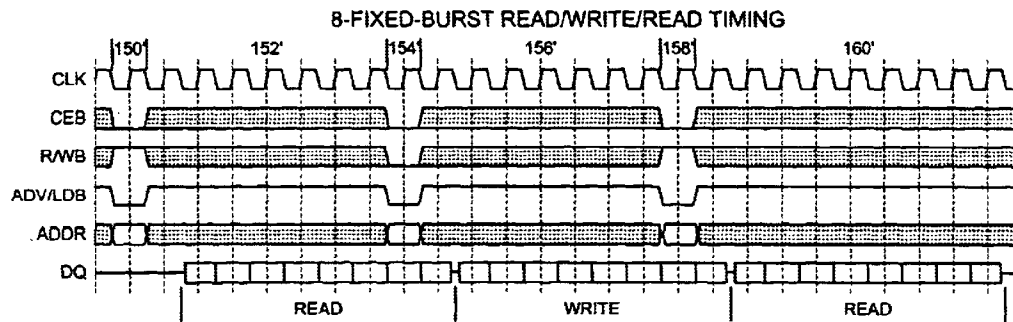


FIG. 5B

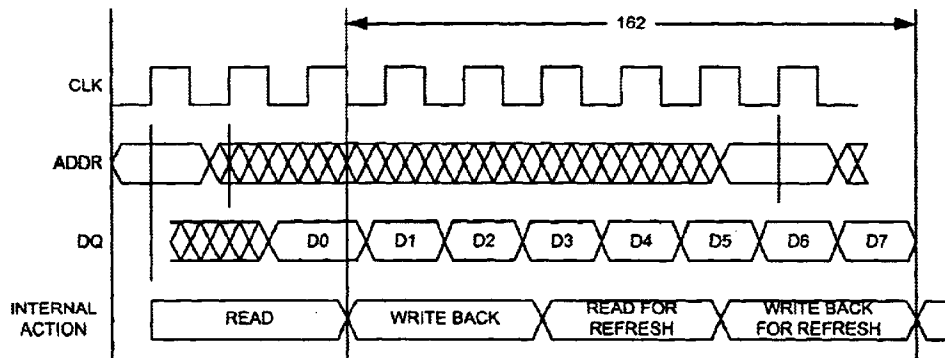


FIG. 6

MEMORY DEVICE WITH FIXED LENGTH NON INTERRUPTIBLE BURST

FIELD OF THE INVENTION

The present invention relates to memory devices generally and, more particularly, to a memory device that transfers a fixed number of words of data with each access.

BACKGROUND OF THE INVENTION

A synchronous Static Random Access Memory (SRAM) can provide data from multiple address locations using a single address. Accessing multiple locations in response to a single address is called a burst mode access. A memory device that provides a burst mode can reduce activity on the address and control buses. The burst mode of a conventional synchronous SRAM can be started and stopped in response to a control signal.

A conventional Dynamic Random Access Memory (DRAM) preserves data during periodic absences of power by implementing a memory cell as a capacitor and an access transistor. Since the charge on the capacitor will slowly leak away, the cells need to be "refreshed" once every few milliseconds. Depending on the frequency of accesses, a conventional DRAM can need an interrupt to perform data refreshes. Using a DRAM in a burst application is difficult because of the need to refresh. Completely hiding refresh cycles (e.g., refreshing data without the need for interrupts) in a DRAM cannot happen with conventional memory devices due to architecture choices that have been made. Data word bursts can be interrupted while in progress since conventional architectures support both burst and single access modes. Conventional DRAM access takes about 10 ns to get data, but nearly 20 ns to complete writeback and equalization. The addition of another 20 ns for a refresh results in a total access of 40 ns.

Since the data burst transfers of conventional memories can be interrupted and single accesses made, the amount of time that the data, address and control busses are not in use can vary. The variability of bus availability complicates the design of systems with shared data, address and control busses.

It would be desirable to have a memory device that has a fixed burst length.

SUMMARY OF THE INVENTION

The present invention concerns an integrated circuit comprising a memory and a logic circuit. The memory may comprise a plurality of storage elements each configured to read and write data in response to an internal address signal. The logic circuit may be configured to generate a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals. The generation of the predetermined number of internal address signals may be non-interruptible.

The objects, features and advantages of the present invention include providing a fixed burst memory that may (i) give network customers who typically burst large data lengths the ability to set a fixed burst length that suits particular needs; (ii) have non-interruptible bursts; (iii) free up the address bus and control bus for a number of cycles; (iv) provide programmability for setting the burst length by using DC levels [Vss or Vcc] on external pins; (v) hide required DRAM refreshes inside a known fixed burst length of data words; and/or (vi) operate at higher frequencies without needing interrupts to perform refreshes of data.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects, features and advantages of the present invention will be apparent from the following detailed description and the appended claims and drawings in which:

FIG. 1 is a block diagram illustrating a preferred embodiment of the present invention;

FIG. 2 is a detailed block diagram illustrating a circuit 102 of FIG. 1;

FIG. 3 is a detailed block diagram of a circuit 102' illustrating an alternative embodiment of the circuit 102 of FIG. 1;

FIG. 4 is a flow diagram illustrating an example burst address sequence;

FIGS. 5A and 5B are diagrams illustrating example operations of a 4 word (FIG. 5A) and an 8 word (FIG. 5B) fixed burst access in accordance with the present invention; and

FIG. 6 is a diagram illustrating an example operation where a burst length may be long enough to include a writeback and a refresh cycle.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. 1, a block diagram of a circuit 100 is shown in accordance with a preferred embodiment of the present invention. The circuit 100 may be implemented, in one example, as a fixed burst memory. The circuit 100 may be configured to transfer a fixed number of words of data with each access (e.g., read or write). A number of words transferred as a group is called a burst. The circuit 100 generally comprises a circuit 102 and a memory array (or circuit) 104. The circuit 102 may be implemented, in one example, as a burst address counter/register. The memory array 104 may be implemented, in one example, as a static random access memory (SRAM), a dynamic random access memory (DRAM), or other appropriate memory to meet the design criteria of a particular implementation.

The circuit 102 may have an input 106 that may receive a signal (e.g., ADDR_EXT), an input 108 that may receive a signal (e.g., LOAD), an input 110 that may receive a signal (e.g., CLK), an input 112 that may receive a signal (e.g., ADV), and an input 114 that may receive a signal (e.g., BURST). The circuit 102 may have an output 116 that may present a signal (e.g., ADDR_INT) to an input 118 of the memory 104. The memory 104 may have an input 120 that may receive a signal (e.g., R/Wb), an input 122 that may receive a signal (e.g., DATA_IN) and an output 122 that may present a signal (e.g., DATA_OUT). The various signals are generally "on" (e.g., a digital HIGH, or 1) or "off" (e.g., a digital LOW, or 0). However, the particular polarities of the on (e.g., asserted) and off (e.g., de-asserted) states of the signals may be adjusted (e.g., reversed) accordingly to meet the design criteria of a particular implementation.

The signal ADDR_EXT may be, in one example, an external address signal. The signal ADDR_EXT may be n-bits wide, where n is an integer. The signal CLK may be a clock signal. The signal R/Wb may be a control signal that may be in a first state or a second state. When the signal R/Wb is in the first state, the circuit 100 will generally read data from the memory circuit 104 for presentation as the signal DATA_OUT. When the signal R/Wb is in the second state, the circuit 100 will generally store data received as the signal DATA_IN.

The signal LOAD may be, in one example, an address load control signal. The circuit 100 may be configured to

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