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## Professional Profile

Dr. Souri's expertise is in microelectronics and computing systems. His professional activities involve advising industrial and legal clients as well as government entities on science and technology matters addressing issues related to intellectual property, product reliability, and failure analysis. He has led complex investigations involving electronics, computer communications, and software controls for safety-critical applications in the medical device, automotive, aviation and process controls industries.

Dr. Souri's experience in the area of microelectronics systems includes technical investigations into computer memories, device physics, integrated circuit (IC) fabrication processes, and esoteric semiconductor material systems for solid-state lighting. He also has broad experience with power electronic devices, circuit protection, IC packaging, and printed circuit board assemblies and display technologies as used in various industries including consumer appliances.

In computing systems, Dr. Souri has worked extensively with embedded controls systems for automotive applications, computer hard disk drives and for drug delivery and implantable devices. He also has expertise in telephony, secure mobile and Internet communications, microprocessor architectures particularly for mobile computing and has analyzed audio/video/image processing software and developed digital asset delivery technologies.

Dr. Souri received his Ph.D. in Electrical Engineering at Stanford University on 3-Dimensional integration of ICs and has taught several courses on IC fabrication, optical fiber communications, TCP/IP networking, and communications protocols and implementation of systems on 3-D chips. He also read Engineering Science at Balliol College, Oxford, where he specialized in photoreflectance microscopy of semiconductor materials. His current research interests include: cloud computing, information security and privacy; financial portfolio optimization, and trading algorithms and software.

## Academic Credentials & Professional Honors

Ph.D., Electrical Engineering, Stanford University, 2003

M.S., Electrical Engineering, Stanford University, 1994

M.A., University of Oxford, UK, 2007

B.A., Engineering Science, University of Oxford, UK, *honors*, 1992



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## Prior Experience

Founder, Merenga Inc., 2000-2002

Co-Founder and Engineering Manager, arcadiaOne, Inc., 1999-2000

Research Engineer, Circuit Protection Division, Raychem, 1996-1997

Research Scientist, Corporate Research & Development, Raychem, 1994-1996

## Professional Affiliations

Institution of Engineering and Technology — IET (member)

Institute of Electrical and Electronic Engineers (senior member)

Oxford University Society (life member)

Oxford Union (member)

## Patents

Patent 6,188,556: Two-Terminal Transistor PTC Circuit Protection Devices, WO0024126, 2001 (with C. McCoy, H. Duffy, A. Cogan, and R. Bommakant).

Patent 6,181,541: Transistor-PTC Circuit Protection Devices, WO0024105, 2001 (with H. Duffy, A. Cogan, M. Munch, and N. Nickols).

Patent 6,153,948: Electronic Circuits with Wide Dynamic Range of On/Off Delay Time, WO001249, 2000 (with A. Cogan).

Patent 5,569,495: Method of Making Varistor Chip with Etching to Remove Damaged Surfaces, CA2220931, EP0826225, WO963978, JP11505375T, 1996 (with A. Evans, T. Tsukada, and R. Dupon).

## Publications

D'Andrade B, Kattamis AZ, Murphy PF, McNulty J, Souri S. Arcing enabled by tin whiskers. IEEE: Reliability Society 2010 Annual Technical Report, 2010.

Fu J, Souri S, Harris J. Temperature and humidity dependent reliability analysis of RGB LED chip. Proceedings, ISTFA 2006: Discretes, Passives, MEMS, and Optoelectronics, pp. 137-141, 2006.

Saraswat K, Kapur P, Souri S. Performance limitations of metal interconnects and possible alternatives. 203rd Meeting of the Electrochemical Society, Paris, France, April 2003.

Saraswat K, Kapur P, Chandra G, Chiang T-Y, Souri S. Scaling induced performance limitations of metal interconnects. IEEE ISSCC Microprocessor Design Workshop, San Francisco, CA, February 2002.

Chiang T, Souri S, Chui C, Saraswat K. Thermal analysis of heterogeneous 3-D ICs with various integration scenarios. IEEE IEDM, December 2001.

Banerjee K, Souri S, Kapur P, Saraswat K. 3-D Heterogeneous ICs: A technology for the next decade and beyond. 5th IEEE Workshop on Signal Propagation on Interconnects, Venice, Italy, May 2001.



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Banerjee K, Souri S, Kapur P, Saraswat K. 3-D ICs: A novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration. Proceedings, IEEE: Special Issue on Interconnections, Vol. 89, No. 5, pp. 602-633, May 2001.

Davis J, Venkatesan R, Kaloyeros A, Bylansky M, Souri S, Banerjee K, Saraswat K, Rahman A, Reif R, Meindl J. Integration limits on Gigascale Integration (GSI) in the 21st Century. Proceedings, IEEE: Special Issue of Limits to Semiconductor Technology, Vol. 89, No. 3, pp. 3-05-324, March 2001.

Saraswat K, Banerjee K, Joshi A, Kalvade P, Kapur P, Souri S. 3-D ICs: Motivation, performance analysis and technology. Proceedings, 26th European Solid-State Circuits Conference (ESSCIRC), Stockholm, Sweden, September 19-21, 2000.

Souri S, Banerjee K, Mehrotra A, Saraswat KC. Multiple Si layer ICs: Motivation, performance analysis, and design implications. 37th ACM Design Automation Conference (DAC), pp. 213-220, Los Angeles, CA, June 5-9, 2000.

Saraswat K, Banerjee K, Joshi A, Kalavade P, Souri S, Subramanian V. 3-D ICs with multiple Si Layers: Performance analysis, and technology. 5th International Symposium on Low and High Dielectric Constant Materials: Materials Science, Processing, and Reliability Issues, 197th Meeting of the Electrochemical Society, Toronto, Canada, May 14-19, 2000.

Saraswat K, Souri S, Subramanian V, Joshi A, Wang A. Novel 3-D structures. Proceedings, IEEE International SOI Conference, pp. 54-55, 1999.

Subramanian V, Toita M, Ibrahim N, Souri S, Saraswat K. Low-leakage germanium-seeded laterally-crystallized single-grain 100nm TFTs for vertical integration applications. IEEE Electron Device Letters, Vol. 20, pp. 341-343, 1999.

Souri S, Saraswat K. Interconnect performance modeling for 3D integrated circuits with multiple Si layers. IEEE International Interconnect Technology Conference, pp. 24-26, 1999.

Haskell B, Souri S, Helfand M. Varistor behavior at twin boundaries in ZnO. Journal of the American Ceramic Society, Vol. 82, No. 8, August 1999.

Chu A, Souri S, Melfand M, Kinsman K, Dupon R. Superior electrical performance of Raychem ZnO Varistor through advanced processing. Proceedings, 1st Asian Meeting on Ferroelectricty, Xian, China, October 5-8, 1995.

**Book Chapters**

Souri S, Chiang T, Kapur P, Banerjee K, Saraswat KC. 3-D ICs deep submicron interconnect performance modeling and analysis. In: Interconnect Technology and Design for Gigascale Integration. Davis J and Meindl J (eds), Kluwer Academic Publishers, October 2003.

**Speaker Engagements**

Souri S. 3-Dimensional ICs interconnect architecture, technology and performance analysis. Oral Defense, Stanford University, 2003.

Souri S. 3-D ICs with multiple Si Layers: performance analysis and technology. Solid State Technology and Devices Seminar, Microlab, UC Berkeley, 2001.

Souri S. 3D ICs: Performance, analysis and technology. Integrated Circuits and Technology Seminar, Stanford University, 2001.



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Souri S. Photoreflectance microscopy of semiconductor materials. Raychem Corporation, CR&D, Menlo Park, CA, 1994.



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