United States Patent [19]

Guthrie et al.

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[54] **ENHANCED DUAL SPEED BUS COMPUTER SYSTEM**

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[51] Int. Cl.^{6} **G06F 13/42**; G06F 13/00; G06F 1/12

[52] U.S. Cl. **710/60**; 710/100; 713/501

[58] Field of Search 395/280, 307–309, 395/880, 849; 710/60, 29, 62, 33, 104, 100, 127–129; 709/233; 713/501, 551

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Primary Examiner—Gopal C. Ray
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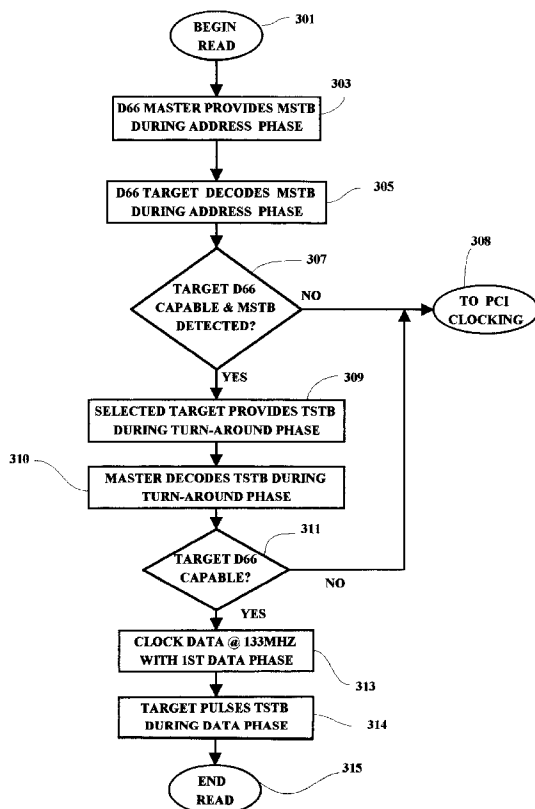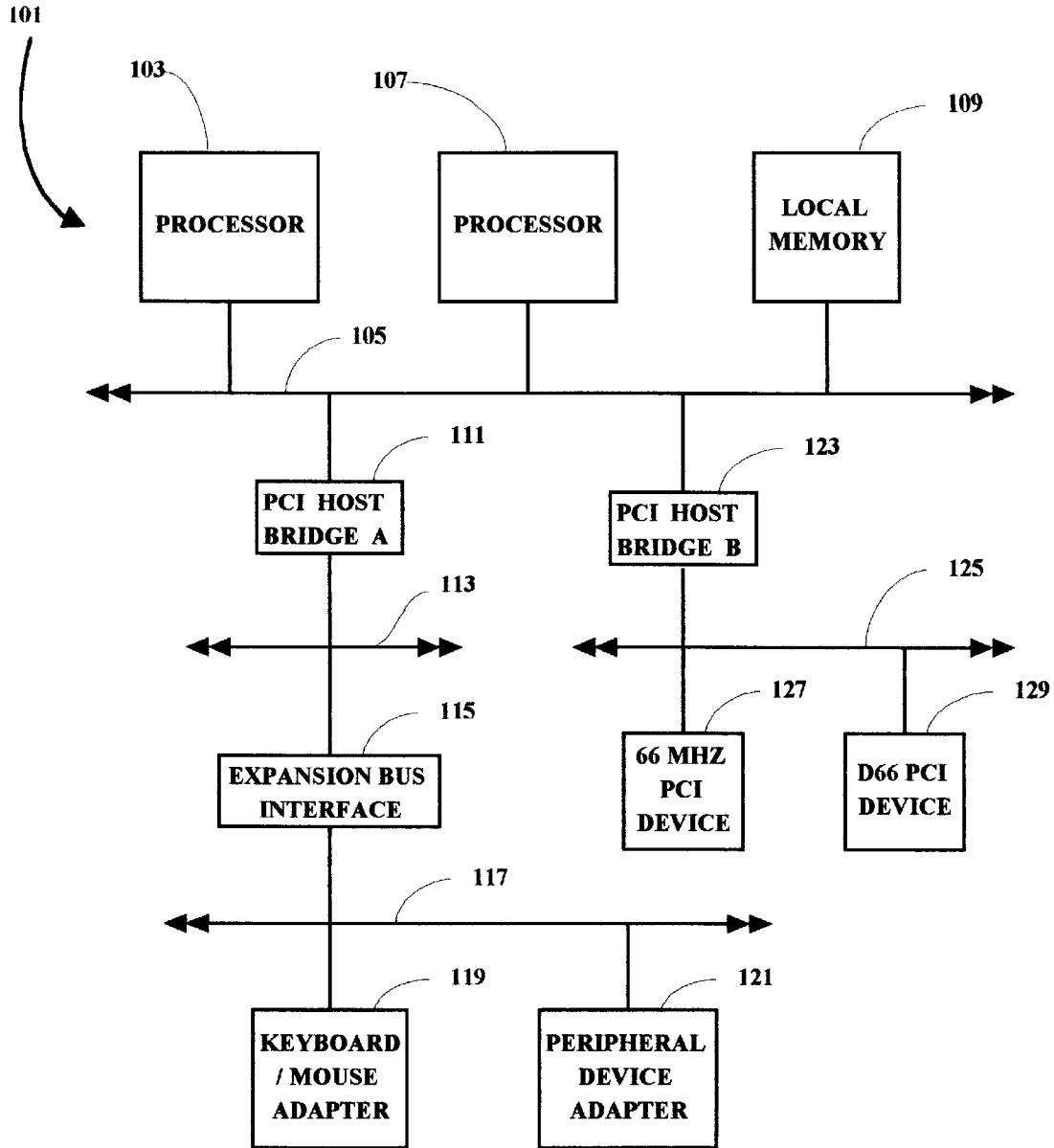
[57] **ABSTRACT**

A methodology and implementing system **101** are provided in which a PCI bus is enhanced to operate at a plurality of data transfer speeds, including for example, 133 MHz in order to accommodate subsystem boards operating at higher frequencies, while at the same time allowing normal 66 MHz PCI clocking for devices designed to operate at the lower 66 MHz standard PCI speed. Master strobe MSTB **303**, **403** and target strobe TSTB signals **309**, **411** are generated in a handshaking methodology to determine if a master data transaction requesting device and a target data transaction device are designed to operate at the higher data transfer frequency. Higher frequency capable devices or boards are run at the increased frequency when both the requesting master and the selected target devices request the higher transfer rate, and standard devices or boards are run at the lower standard PCI frequency, while both master and target devices are coupled to and run from the same multi-speed PCI bus **125**.

15 Claims, 4 Drawing Sheets

FIG. 1

FIG. 2A

FIG. 2B

(BEGIN READ) — 301

↓

D66 MASTER PROVIDES MSTB DURING ADDRESS PHASE — 303

↓

D66 TARGET DECODES MSTB DURING ADDRESS PHASE — 305

↓

TARGET D66 CAPABLE & MSTB DETECTED? — 307

— NO → (TO PCI CLOCKING) — 308

↓ YES

SELECTED TARGET PROVIDES TSTB DURING TURN-AROUND PHASE — 309

↓

310 — **MASTER DECODES TSTB DURING TURN-AROUND PHASE**

↓

TARGET D66 CAPABLE? — 311

— NO →

↓ YES

CLOCK DATA @ 133MHZ WITH 1ST DATA PHASE — 313

↓

TARGET PULSES TSTB DURING DATA PHASE — 314

↓

(END READ) — 315

FIG. 3

FIG. 4

DOCKET ALARM
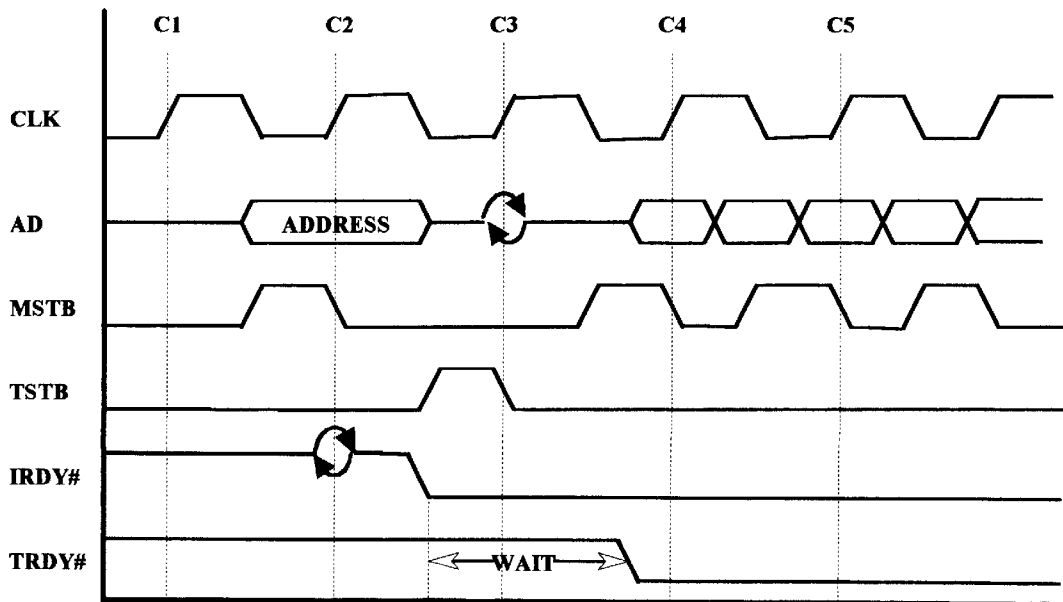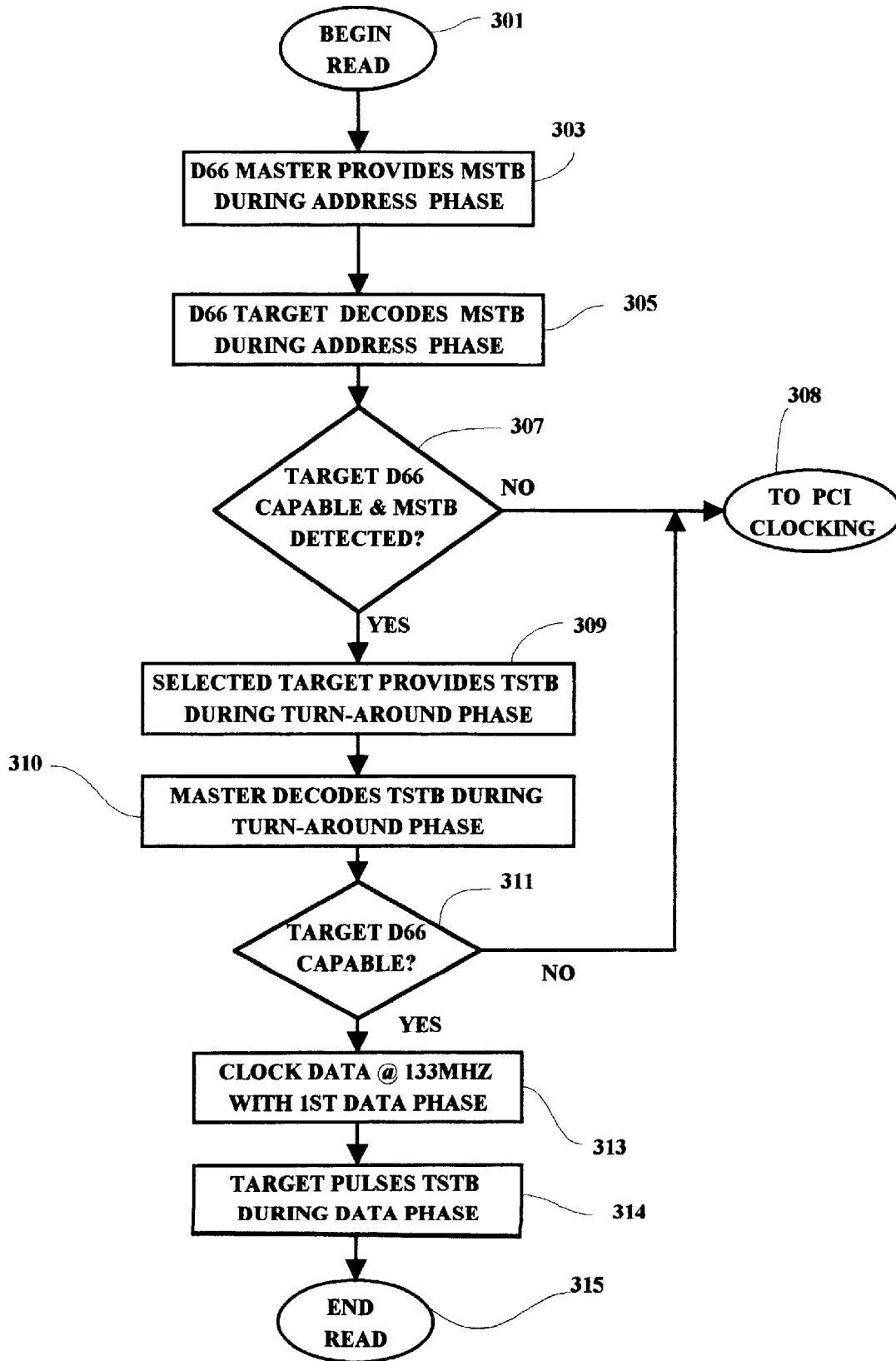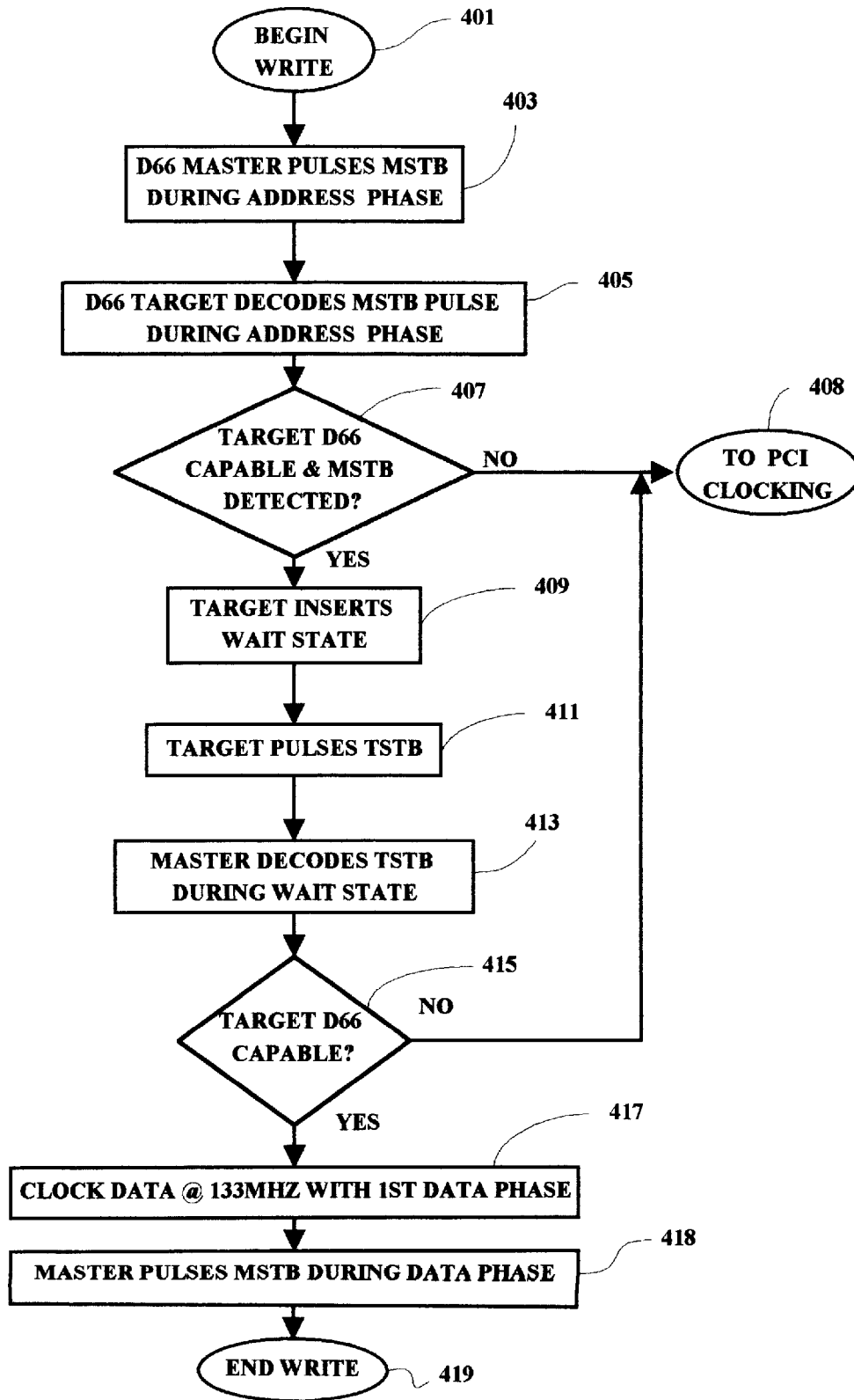
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