



United States Patent [19]

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Bland et al.

[45] Date of Patent: **Sep. 17, 1996**

[54] **BRIDGE BETWEEN TWO BUSES OF A COMPUTER SYSTEM THAT DETERMINES THE LOCATION OF MEMORY OR ACCESSES FROM BUS MASTERS ON ONE OF THE BUSES**

5,446,869 8/1995 Padgett et al. 395/500

OTHER PUBLICATIONS

"82420/82430 PCIset ISA and EISA Bridges", Intel, Dec. 1993, pp. 15-19.

"Peripheral Component Interconnect", Revision I.O. Specification, Dec. 1992, Section 3.6.1.

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[57] ABSTRACT

A bridge is provided between an industry standard architecture (ISA) bus and a peripheral controller interconnect (PCI) bus and performs memory cycles on both buses simultaneously when a master on the ISA bus initiates a memory transfer. Data is steered between the ISA and PCI buses when a slave on the PCI bus claims the memory address within a predetermined time period after the memory cycle is initiated on the PCI bus. The ISA bus is isolated from the PCI bus when no slave on the PCI bus claims the memory address. This allows the memory cycle to be completed on the ISA bus, and the memory cycle on the PCI bus is terminated.

[21] Appl. No.: **351,192**

[22] Filed: **Nov. 30, 1994**

[51] Int. Cl.⁶ **G06F 13/00**

[52] U.S. Cl. **395/308; 395/306**

[58] Field of Search 395/306, 308; 370/85.13

[56] References Cited

U.S. PATENT DOCUMENTS

- 5,191,653 3/1993 Banks et al. 395/885
- 5,191,657 3/1993 Ludwig et al. 395/306

18 Claims, 4 Drawing Sheets

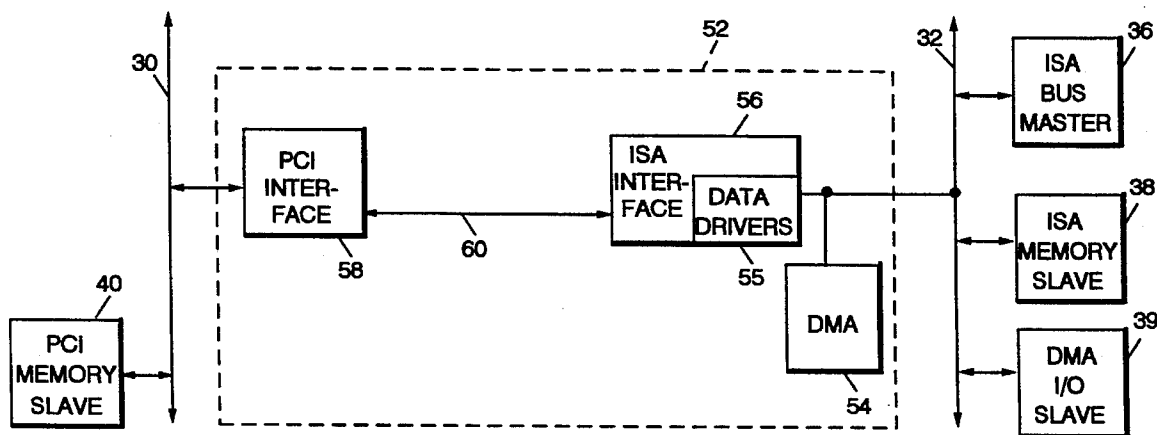
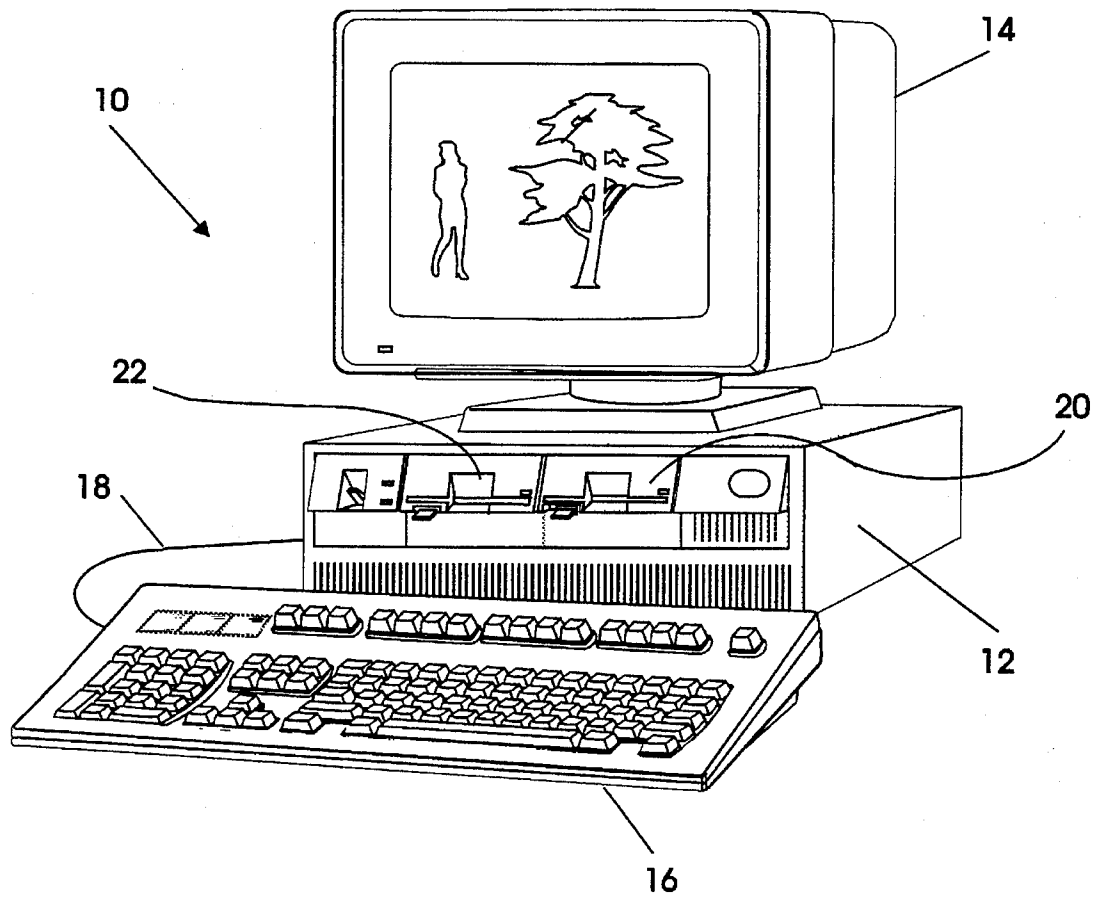


FIG. 1



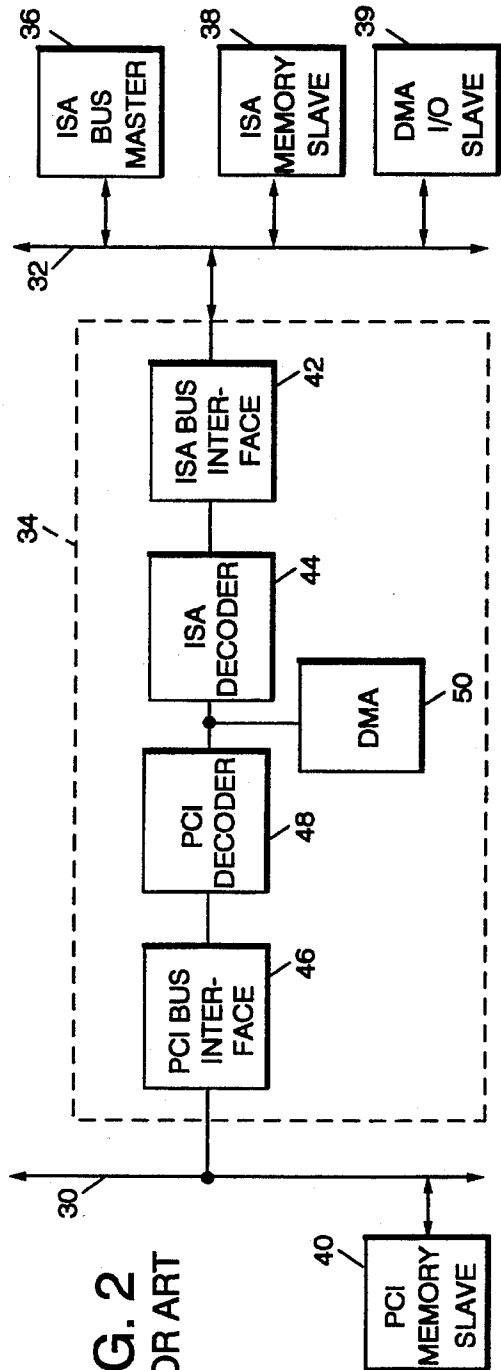


FIG. 2
PRIOR ART

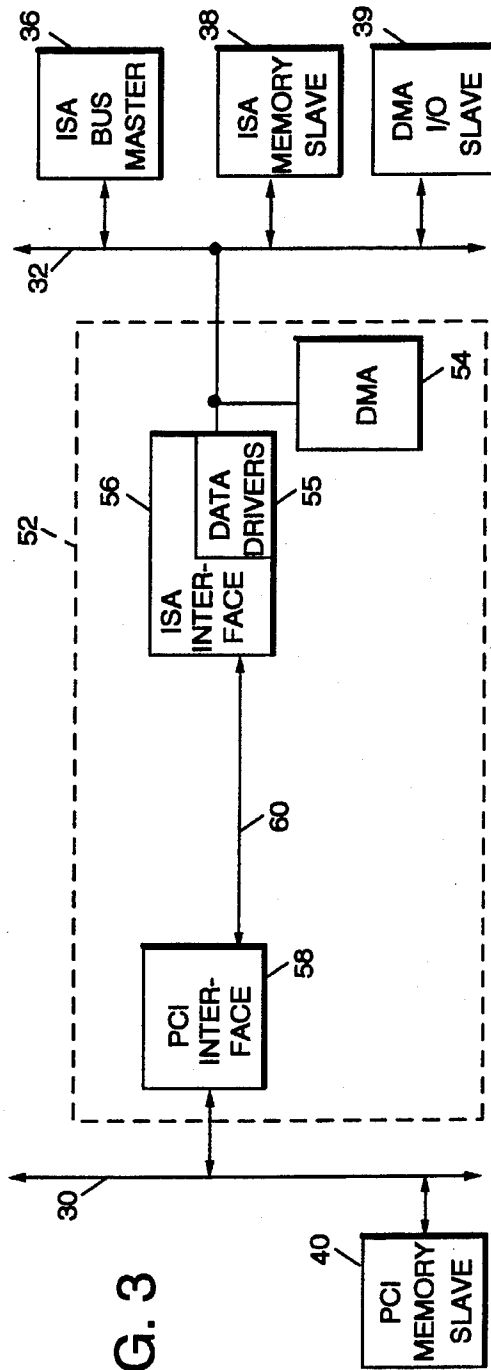


FIG. 3

FIG. 4

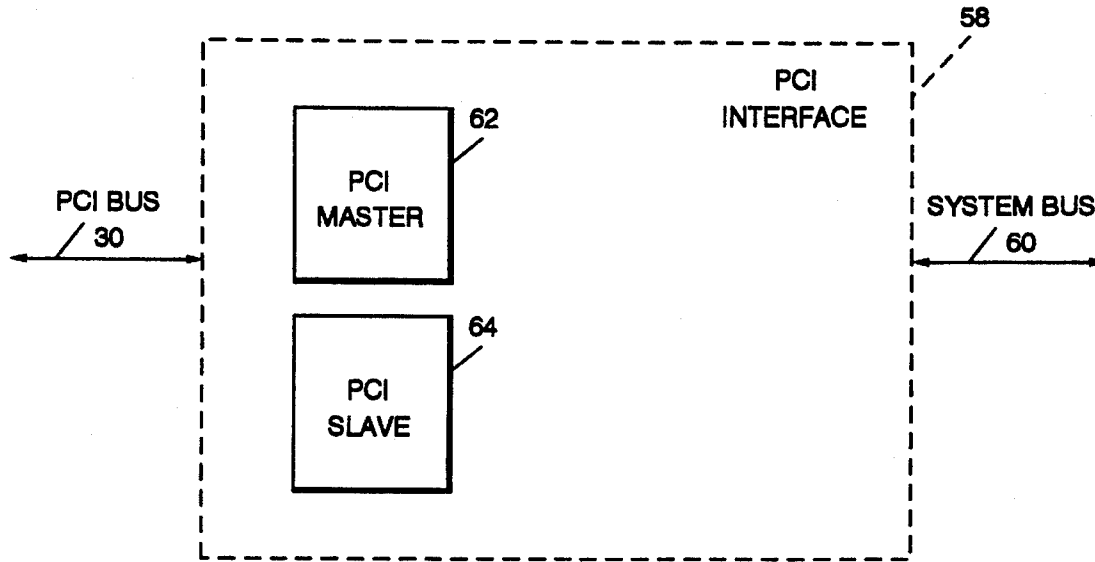
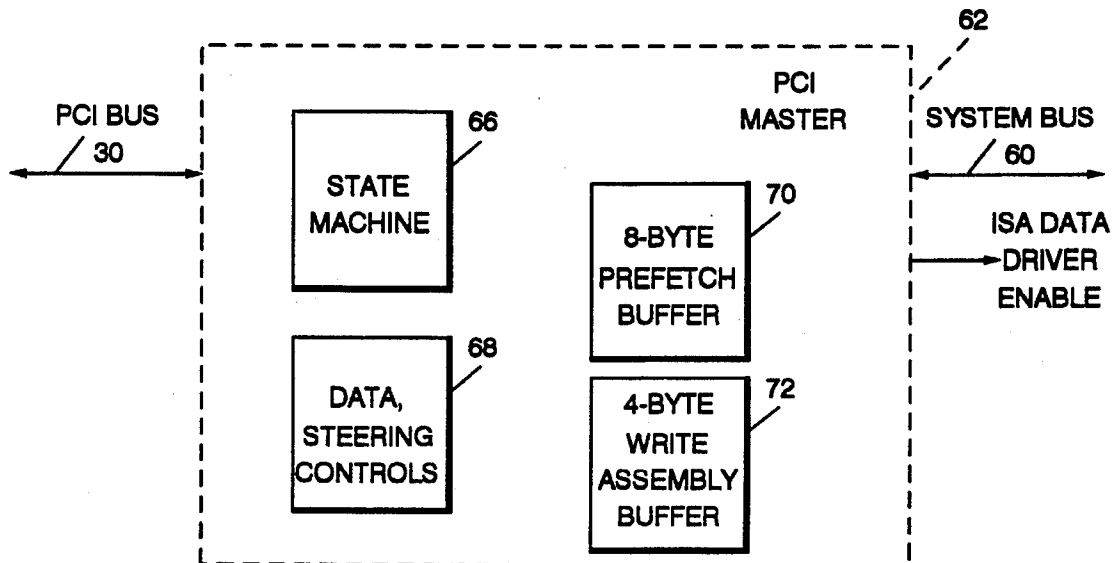


FIG. 5



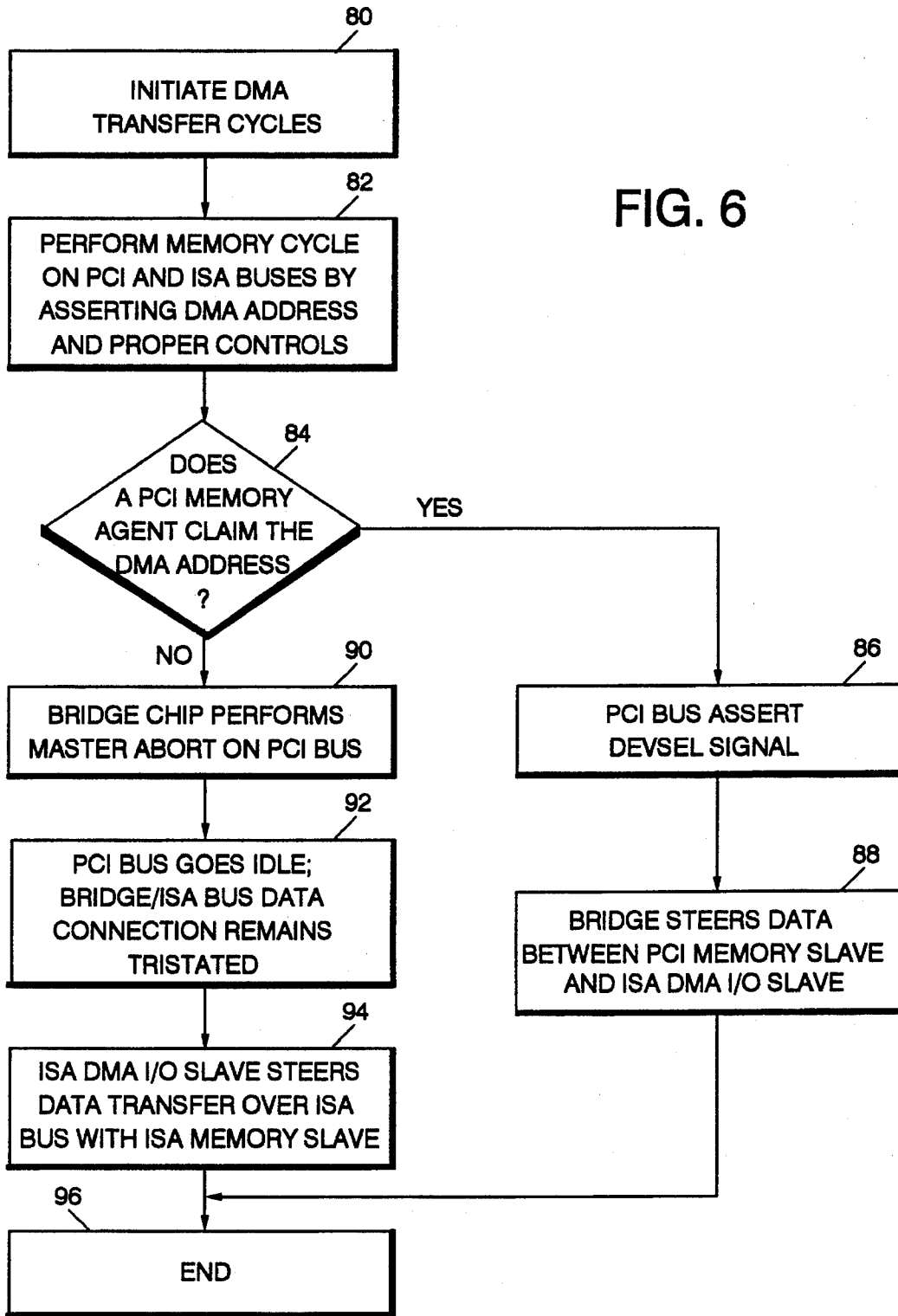


FIG. 6

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