# United States Patent [19]

## Bland et al.

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[45] **Date of Patent:** Sep. 17, 1996

[54] **BRIDGE BETWEEN TWO BUSES OF A COMPUTER SYSTEM THAT DETERMINES THE LOCATION OF MEMORY OR ACCESSES FROM BUS MASTERS ON ONE OF THE BUSES**

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[21] Appl. No.: **351,192**

[22] Filed: **Nov. 30, 1994**

[51] **Int. Cl.**$^6$ ...................................................... **G06F 13/00**

[52] **U.S. Cl.** ............................................. **395/308**; 395/306

[58] **Field of Search** ..................................... 395/306, 308; 370/85.13

[56] **References Cited**

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[57] **ABSTRACT**

A bridge is provided between an industry standard architecture (ISA) bus and a peripheral controller interconnect (PCI) bus and performs memory cycles on both buses simultaneously when a master on the ISA bus initiates a memory transfer. Data is steered between the ISA and PCI buses when a slave on the PCI bus claims the memory address within a predetermined time period after the memory cycle is initiated on the PCI bus. The ISA bus is isolated from the PCI bus when no slave on the PCI bus claims the memory address. This allows the memory cycle to be completed on the ISA bus, and the memory cycle on the PCI bus is terminated.
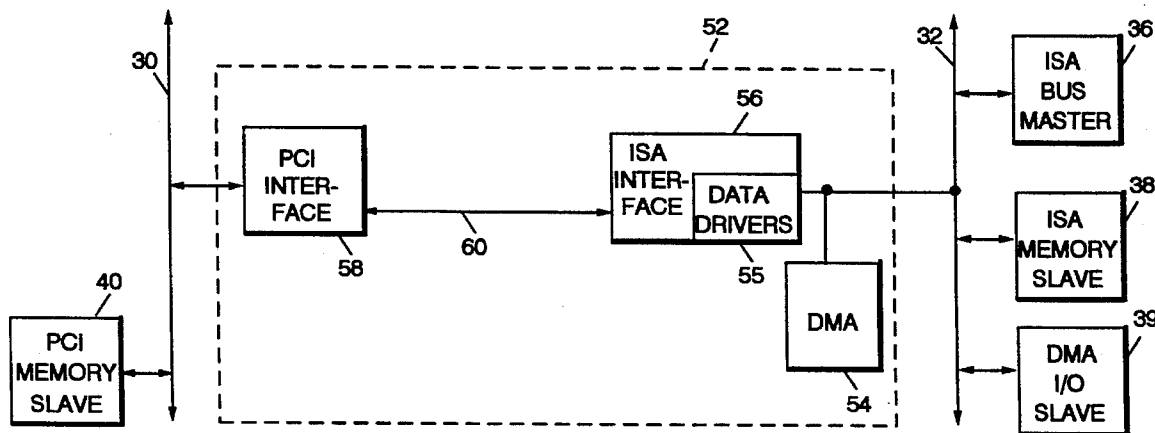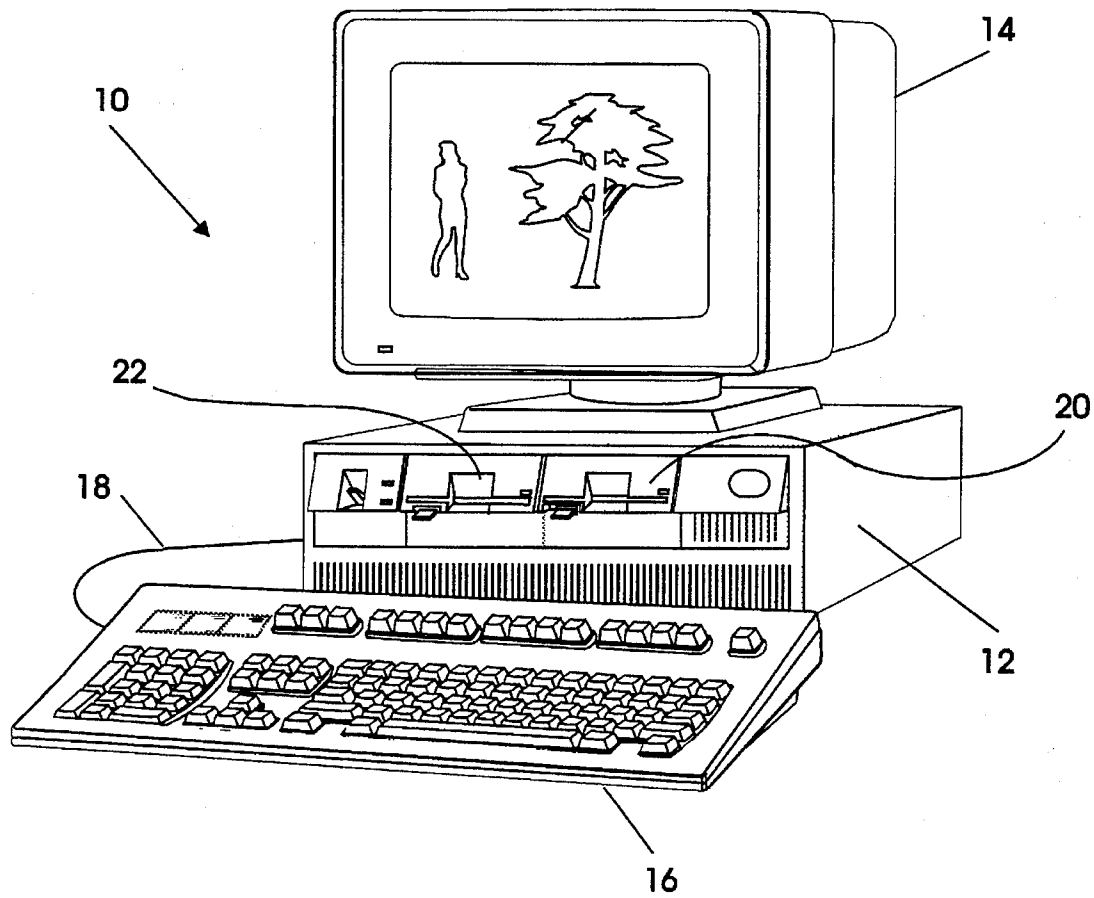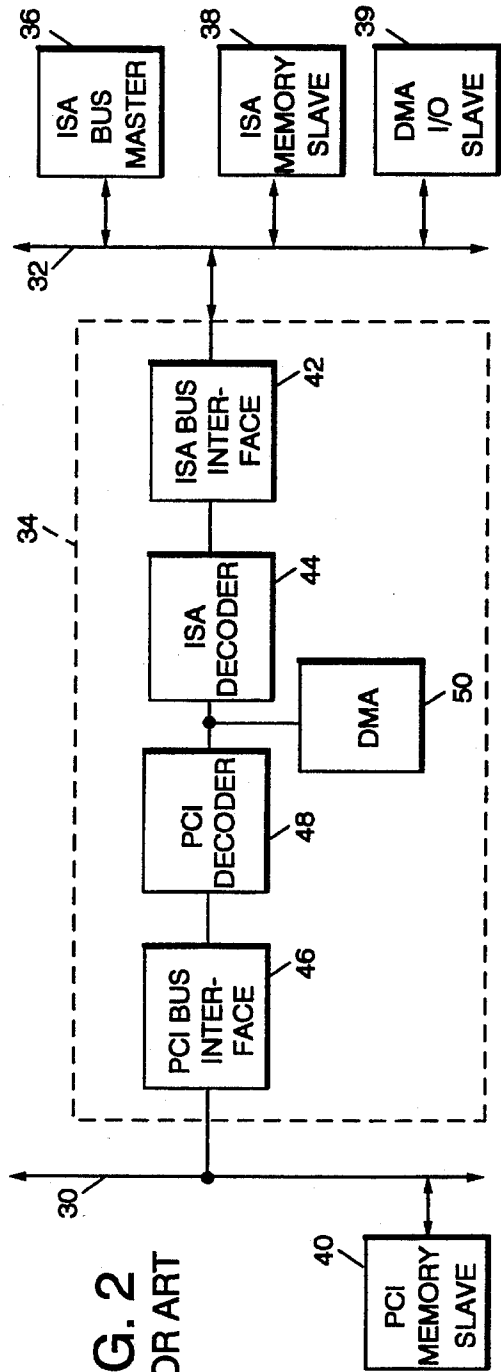
**18 Claims, 4 Drawing Sheets**
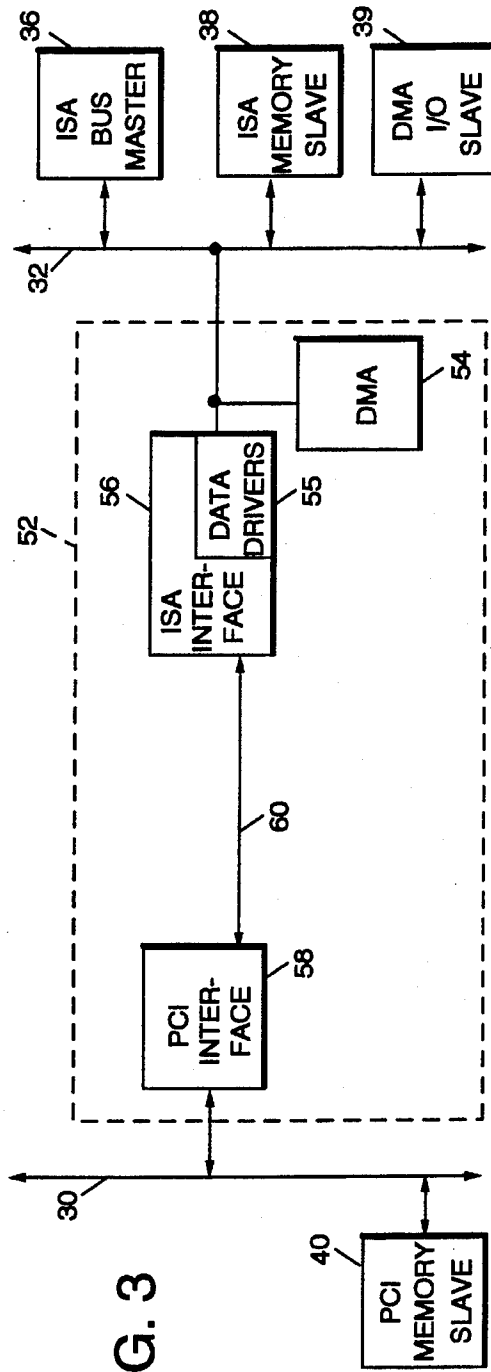
## FIG. 1

FIG. 2
PRIOR ART

FIG. 3

# FIG. 4

PCI INTERFACE   58

PCI BUS / 30

PCI MASTER   62

PCI SLAVE   64

SYSTEM BUS / 60

# FIG. 5

PCI MASTER   62

PCI BUS / 30

STATE MACHINE   66

DATA, STEERING CONTROLS   68

8-BYTE PREFETCH BUFFER   70

4-BYTE WRITE ASSEMBLY BUFFER   72

SYSTEM BUS / 60

ISA DATA DRIVER ENABLE

FIG. 6

```
                    ┌─────────────────────┐ 80
                    │    INITIATE DMA     │
                    │  TRANSFER CYCLES    │
                    └─────────────────────┘
                              │
                              ▼
                 ┌──────────────────────────┐ 82
                 │  PERFORM MEMORY CYCLE    │
                 │  ON PCI AND ISA BUSES BY │
                 │  ASSERTING DMA ADDRESS   │
                 │  AND PROPER CONTROLS     │
                 └──────────────────────────┘
                              │
                              ▼
                        ╱─────────╲ 84
                       ╱   DOES    ╲
                      ╱ A PCI MEMORY╲      YES
                      ╲ AGENT CLAIM THE╱──────────────┐
                       ╲DMA ADDRESS ╱                 │
                        ╲    ?     ╱                   │
                         ╲───────╱                    │
                         │ NO                          │
                         ▼                             ▼
         ┌──────────────────────┐ 90      ┌──────────────────────┐ 86
         │  BRIDGE CHIP PERFORMS │        │   PCI BUS ASSERT     │
         │ MASTER ABORT ON PCI BUS│       │   DEVSEL SIGNAL      │
         └──────────────────────┘        └──────────────────────┘
                    │                                │
                    ▼                                ▼
         ┌──────────────────────┐ 92      ┌──────────────────────┐ 88
         │  PCI BUS GOES IDLE;  │         │  BRIDGE STEERS DATA  │
         │ BRIDGE/ISA BUS DATA  │         │BETWEEN PCI MEMORY SLAVE│
         │ CONNECTION REMAINS   │         │ AND ISA DMA I/O SLAVE │
         │     TRISTATED        │         └──────────────────────┘
         └──────────────────────┘                    │
                    │                                 │
                    ▼                                 │
         ┌──────────────────────┐ 94                 │
         │ ISA DMA I/O SLAVE STEERS│                 │
         │ DATA TRANSFER OVER ISA │                  │
         │ BUS WITH ISA MEMORY SLAVE│                │
         └──────────────────────┘                    │
                    │                                 │
                    ▼◄────────────────────────────────┘
         ┌──────────────────────┐ 96
         │        END           │
         └──────────────────────┘
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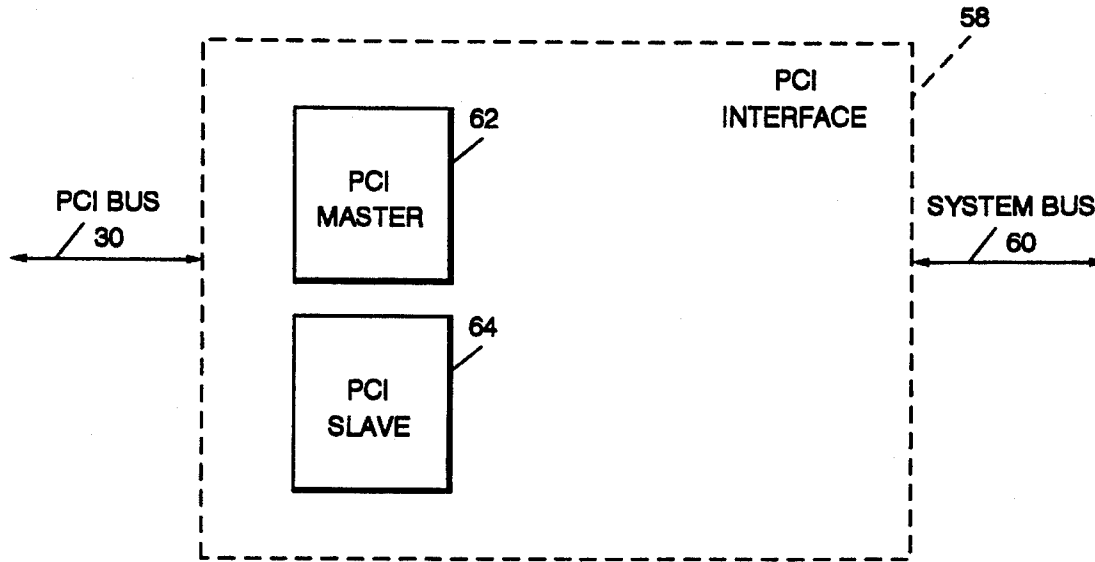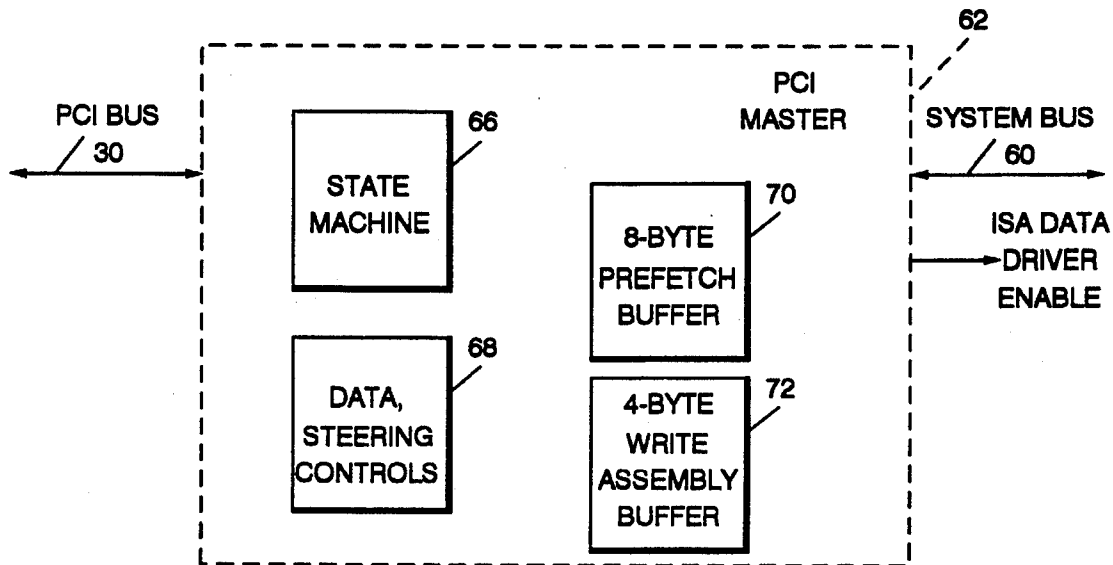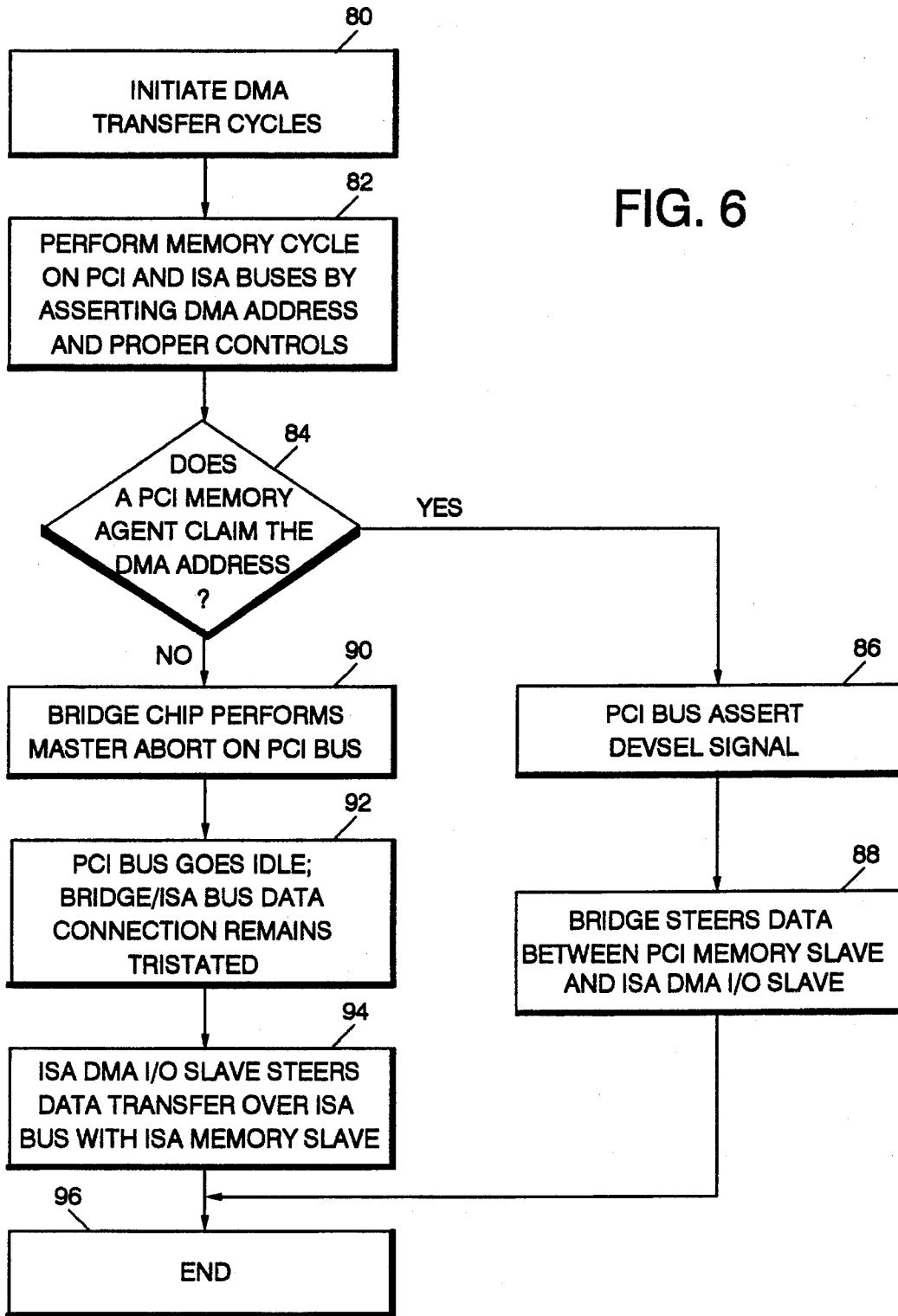
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