



United States Patent [19]

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Lysinger

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[54] **MULTIPLE ACCESS MEMORY DEVICE**

5,526,320 6/1996 Zagar et al. 365/233.5

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[21] Appl. No.: **775,664**

[57] ABSTRACT

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A memory circuit has a plurality of data storage locations and an address associated with each data storage location. A first decoded address storage circuit stores a first decoded memory address and outputs the stored first decoded memory address. A second decoded address storage circuit stores a second decoded memory address and outputs the stored second decoded memory address. An address access circuit is coupled to the output of the first decoded address storage circuit and accesses the data storage location associated with the first decoded memory address in response to the first decoded memory address being output from the first decoded address storage circuit. A control circuit is coupled to the first decoded address storage circuit for controlling the transfer of decoded memory address information from the second decoded address storage circuit to the first decoded address storage circuit.

[51] Int. Cl.⁶ **G11C 8/00**

[52] U.S. Cl. **365/230.06; 365/189.05; 365/230.08**

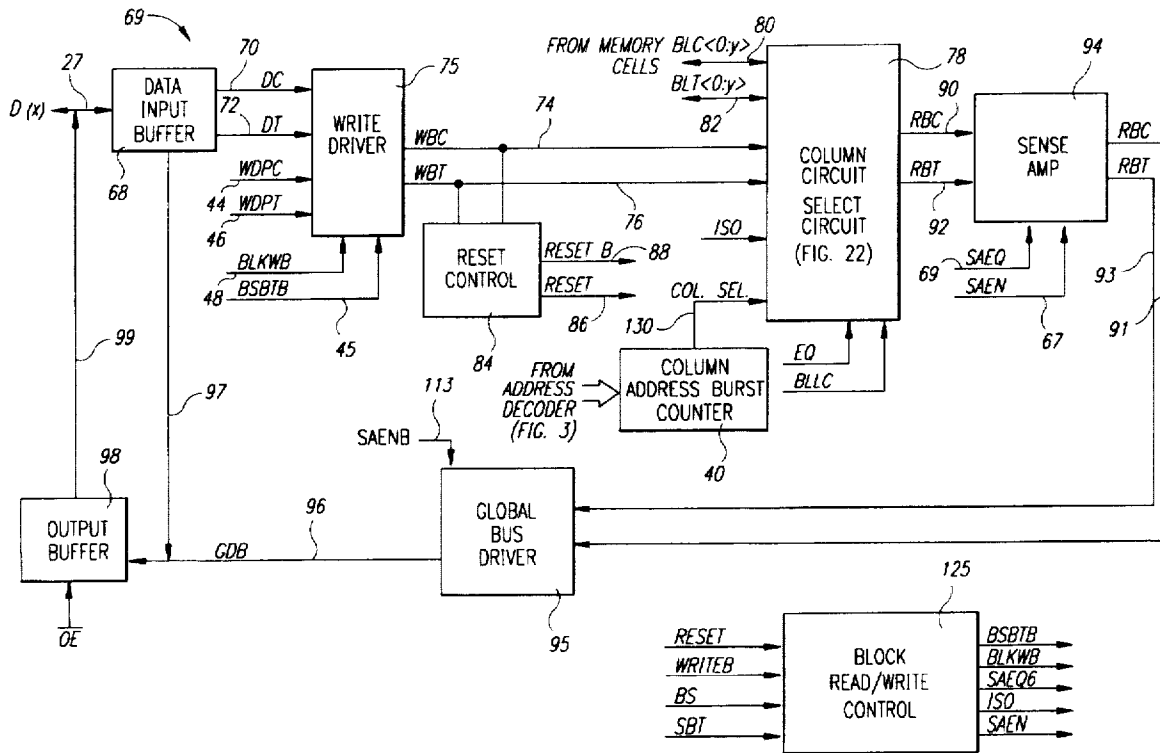
[58] Field of Search **365/230.06, 230.08, 365/189.05**

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13 Claims, 22 Drawing Sheets



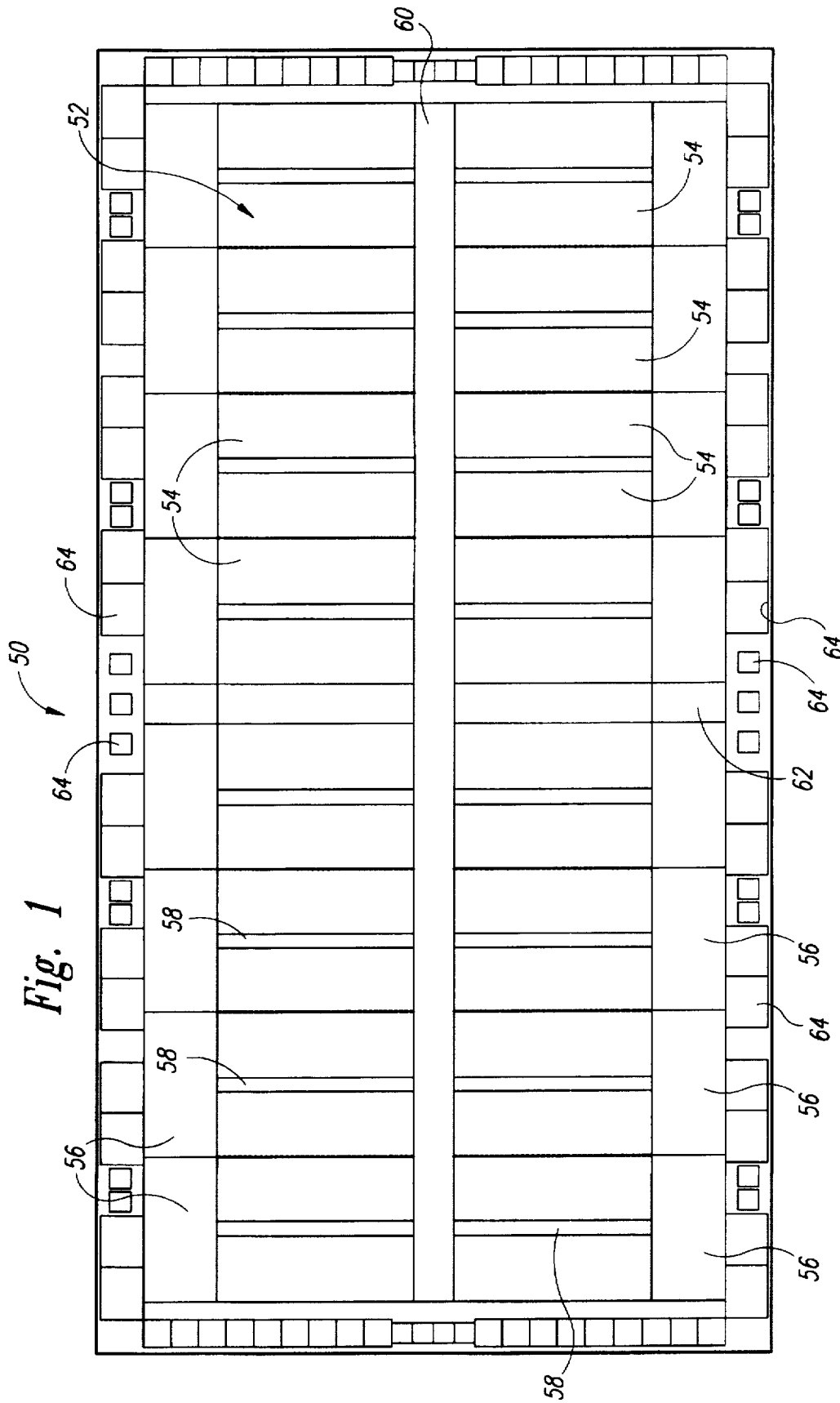


Fig. 1

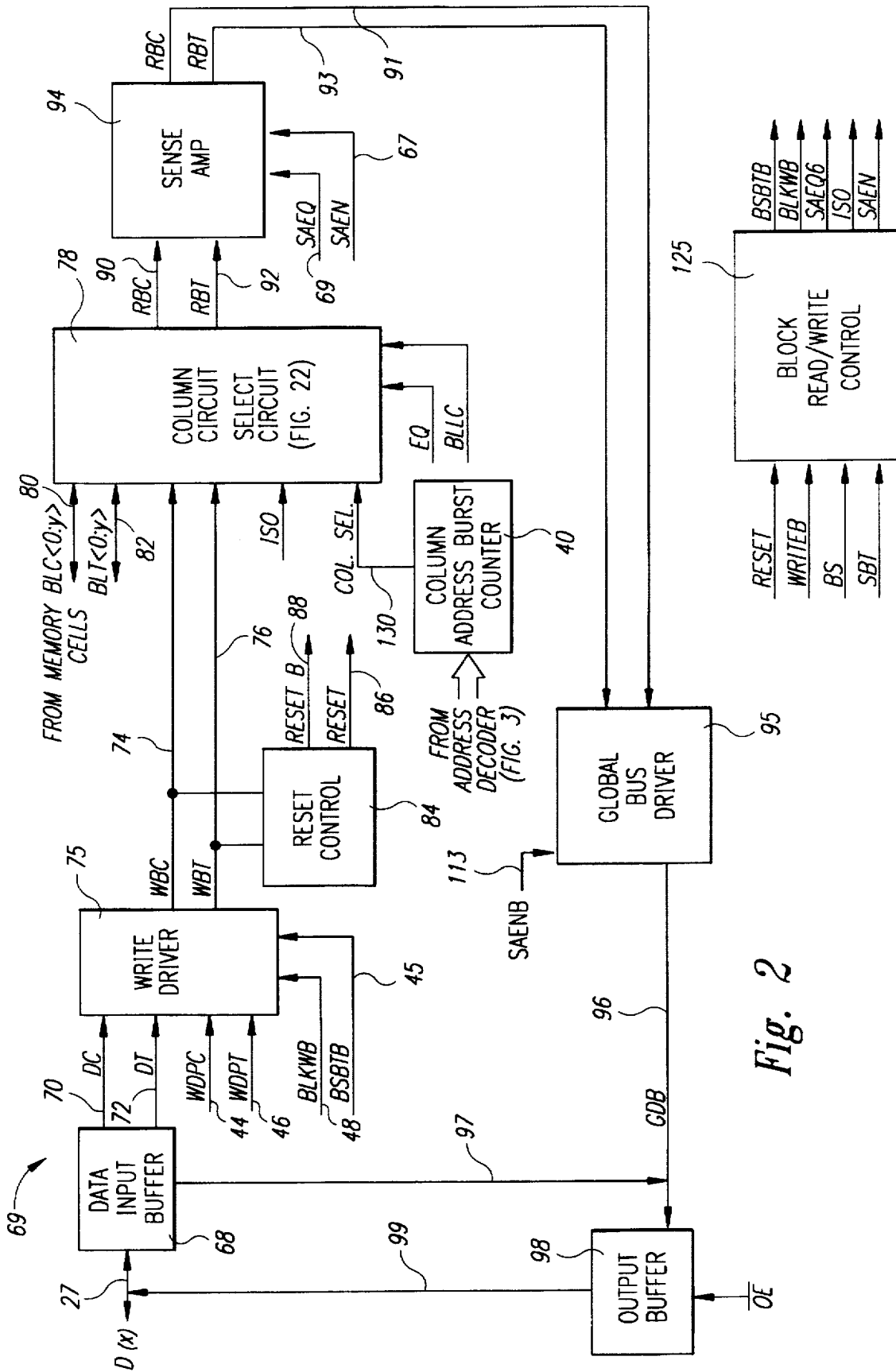


Fig. 2

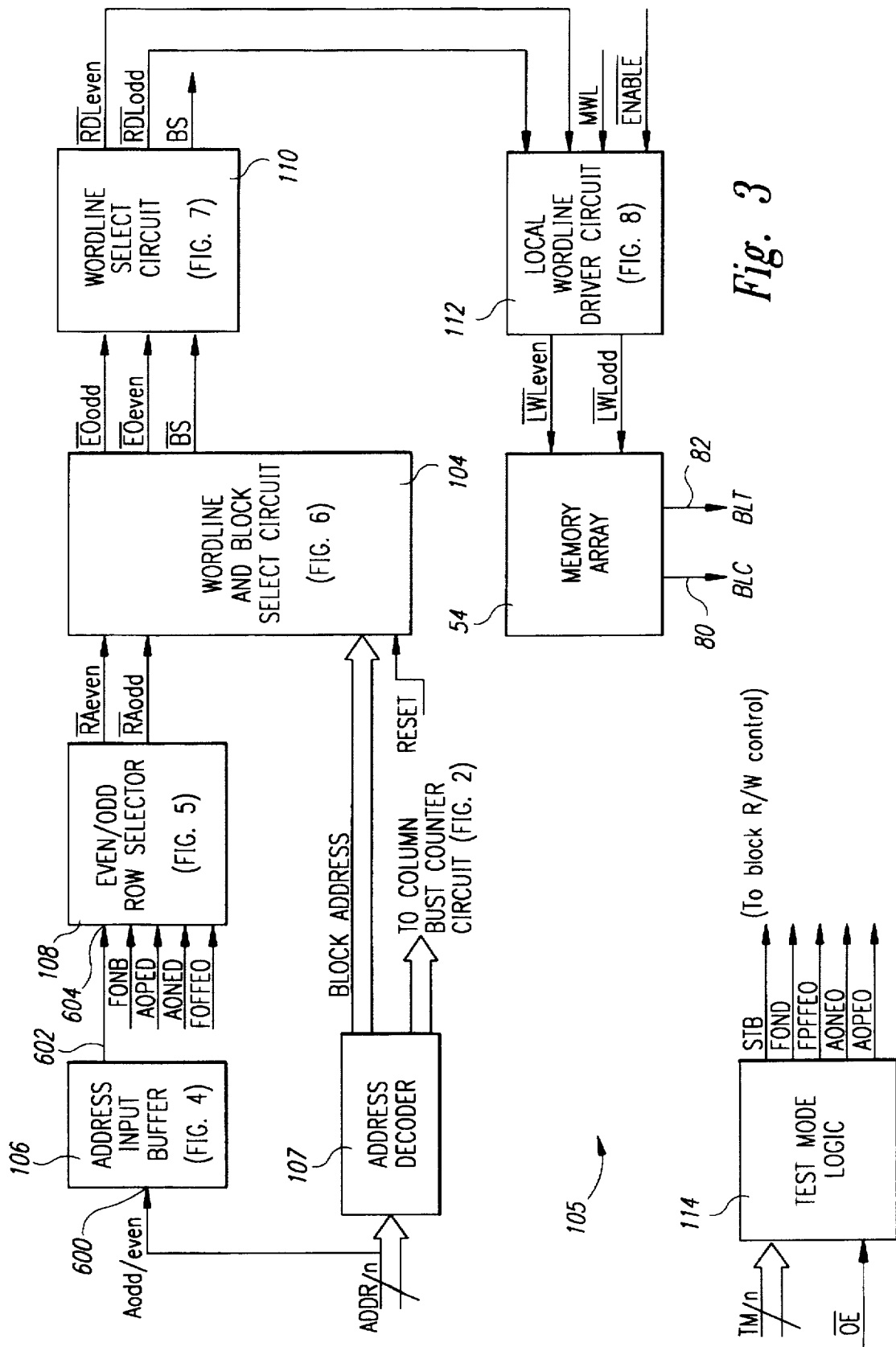


Fig. 3

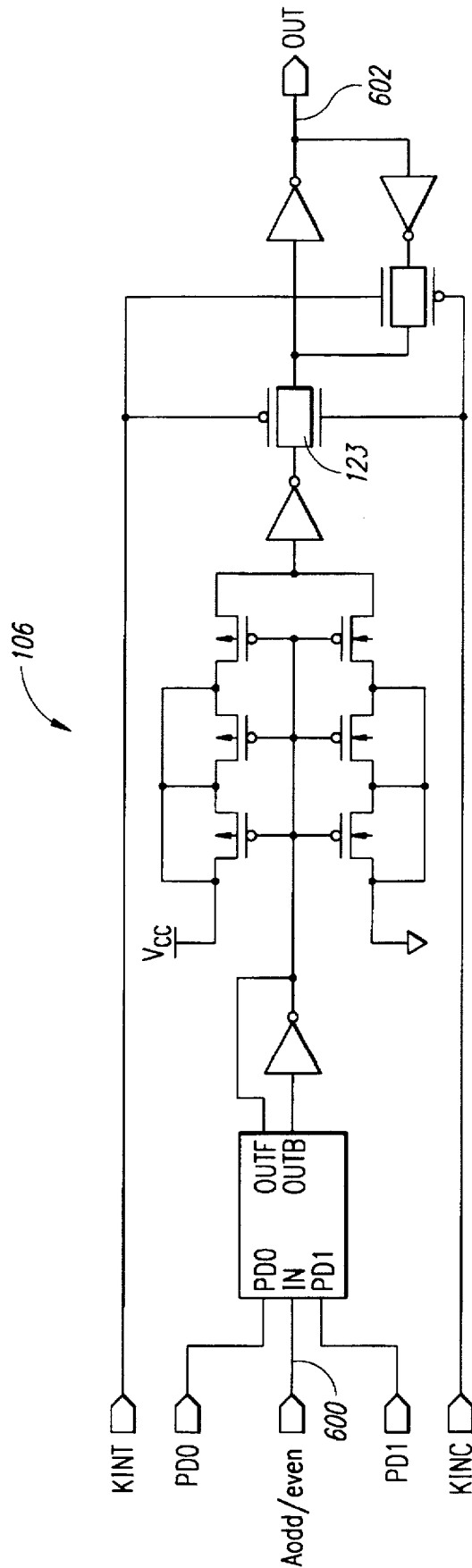


Fig. 4

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