



(12) **United States Patent**
Fujioka et al.

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(45) **Date of Patent:** **Feb. 6, 2001**

(54) **SEMICONDUCTOR INTEGRATED CIRCUIT MEMORY**

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(73) Assignee: **Fujitsu Limited**, Kawasaki (JP)

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(*) Notice: Under 35 U.S.C. 154(b), the term of this patent shall be extended for 0 days.

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(21) Appl. No.: **09/340,147**

Primary Examiner—Richard Elms
Assistant Examiner—Hien Nguyen

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(30) **Foreign Application Priority Data**

(57) **ABSTRACT**

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(51) **Int. Cl.⁷** **G11C 8/00**

(52) **U.S. Cl.** **365/233; 365/230.03; 365/238.5**

(58) **Field of Search** **365/233, 220, 365/203, 238.5, 221, 239, 230.03**

A semiconductor memory includes memory cell blocks, a burst-length information generating circuit which generates burst-length information based on a burst length, and a block enable circuit which receives the burst-length information. The block enable circuit selectively enables one of the memory cell blocks when the burst length is equal to or shorter than a predetermined burst length and selectively enables a plurality of memory cell blocks based on the burst length when the burst length is longer than the predetermined burst length. Data are read from the above-mentioned one or plurality of memory cell blocks.

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16 Claims, 20 Drawing Sheets

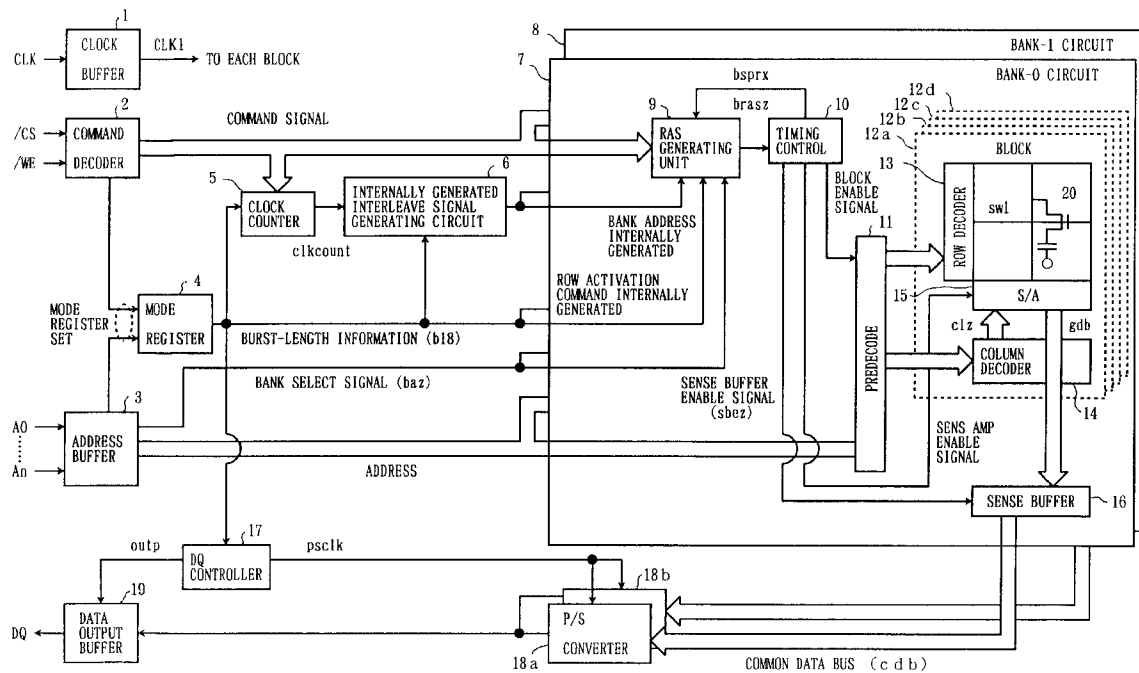


FIG. 1

PRIOR ART

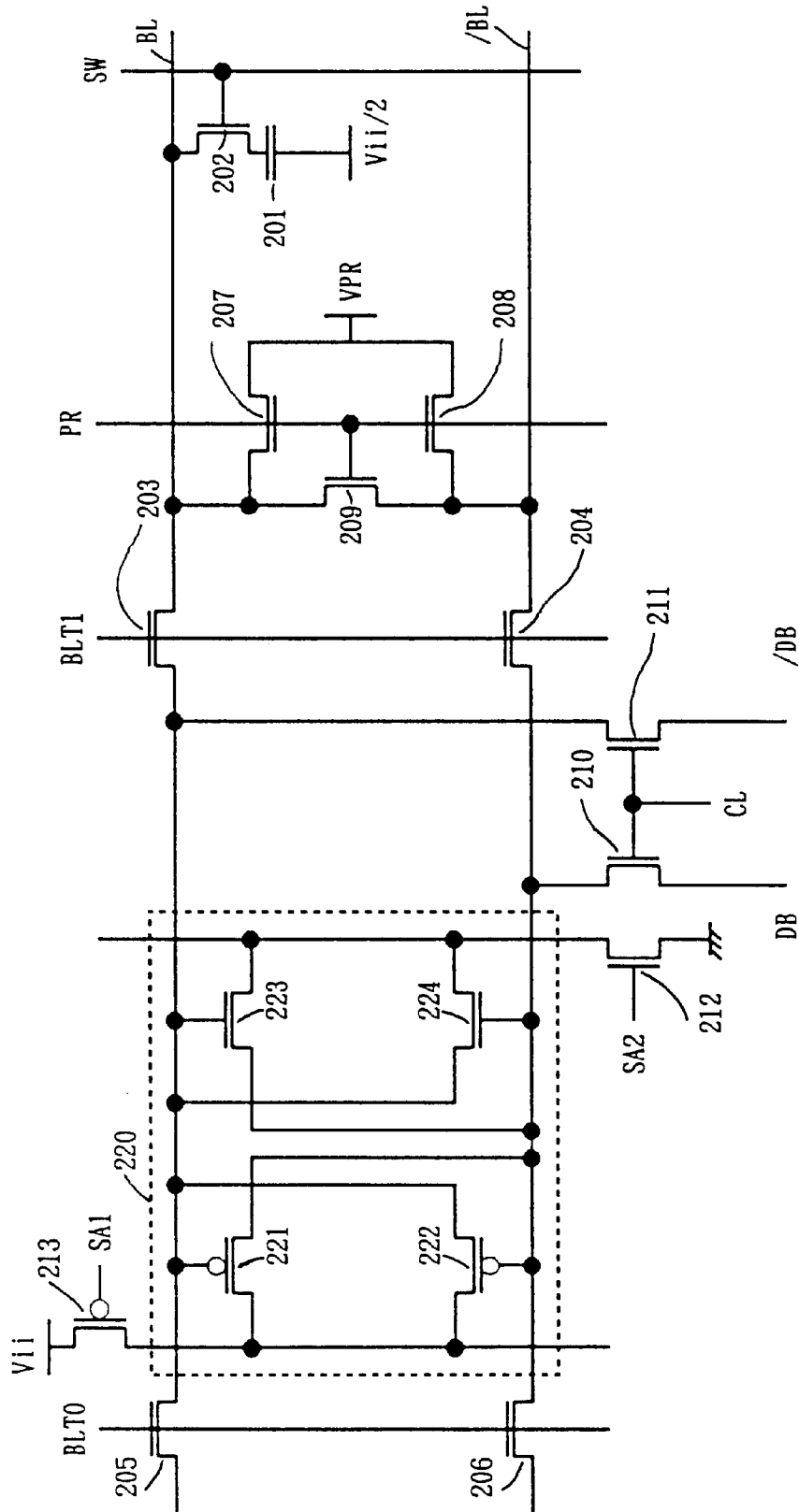


FIG. 2

PRIOR ART

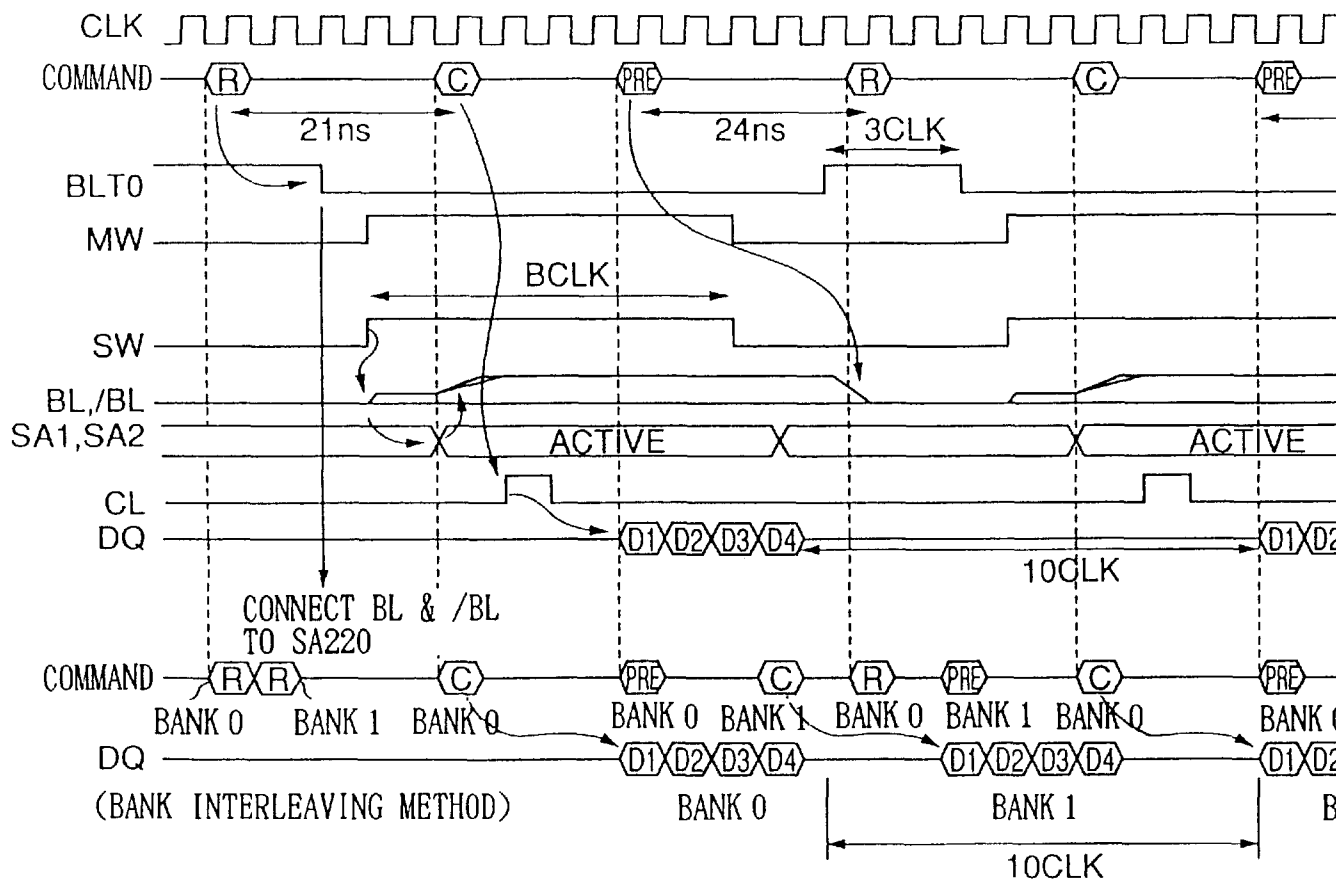


FIG. 3

PRIOR ART

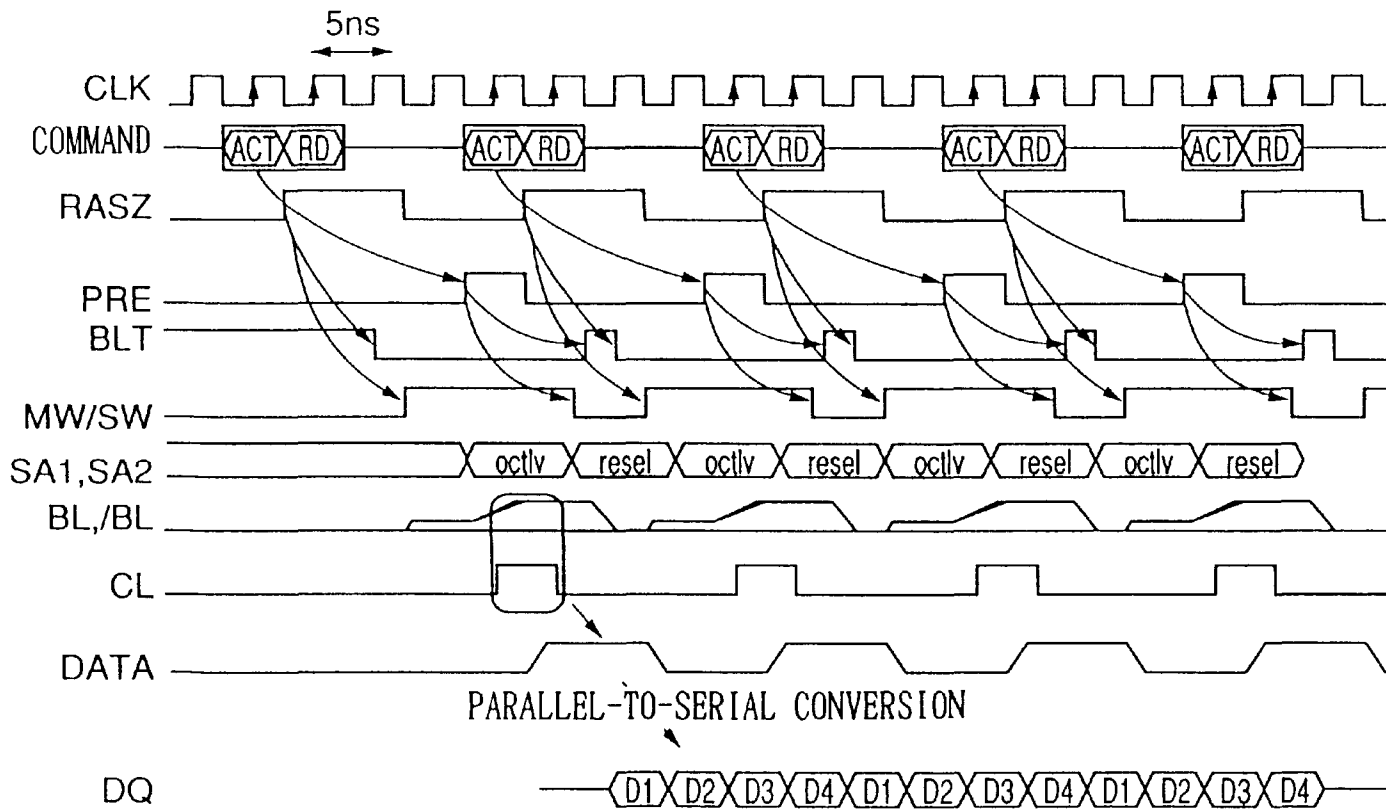
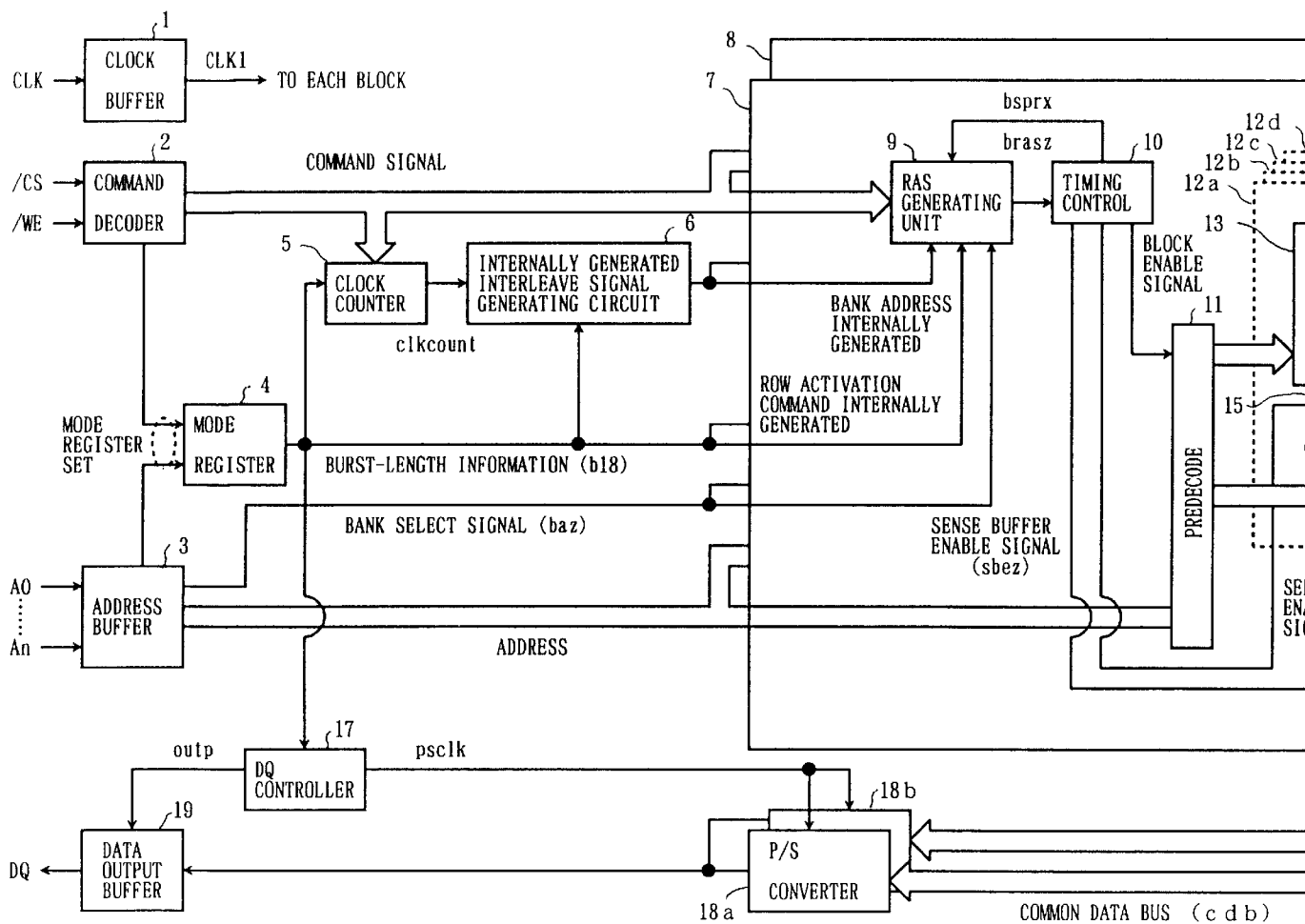


FIG. 4



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