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United States Patent [19]

Zagar

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[54] **SYNCHRONOUS NAND DRAM ARCHITECTURE**

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[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

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Related U.S. Application Data

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[51] **Int. Cl.^{6}** **G11C 8/00**
[52] **U.S. Cl.** **365/233**; 365/239; 365/230.06
[58] **Field of Search** 365/230.03, 149, 365/233, 189.04, 189.05, 239, 221, 230.06

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Primary Examiner—Joseph A. Popek
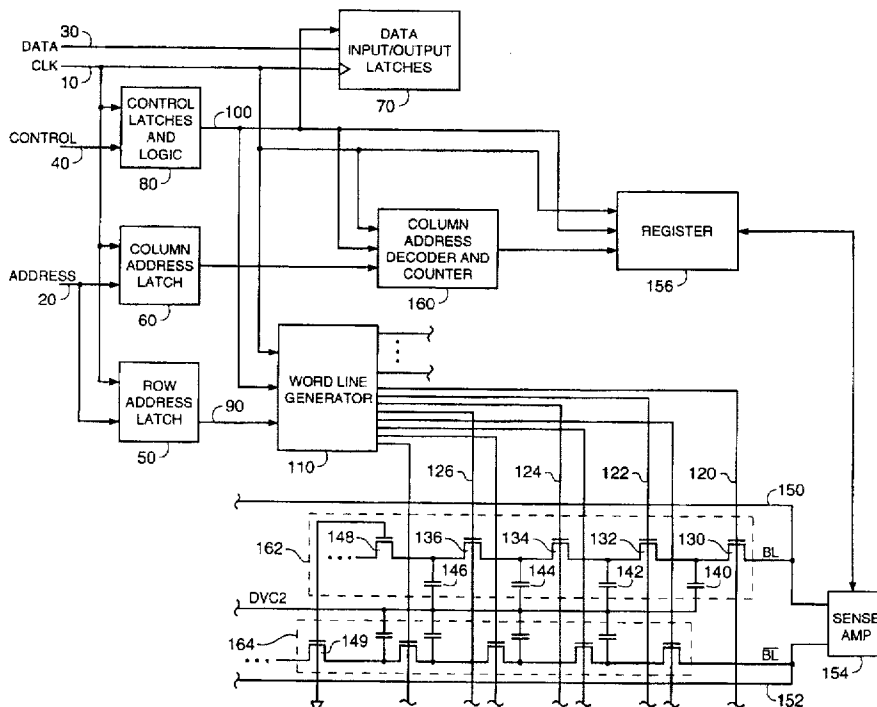*Attorney, Agent, or Firm*—Schwegman, Lundberg, Woessner & Kluth, P.A.

[57] **ABSTRACT**

An integrated circuit memory device has two banks of NAND structured memory cells and a clock input for synchronously latching control, address and data signals. Time delays of sequentially accessing and restoring memory bits in the NAND structure are masked through the use of the dual bank architecture and synchronous timing. The NAND structured memory cells provide an extremely dense memory array for a high capacity memory device. The input clock signal driving a synchronous word line generator provides a simplified high speed access to the array. A set of random access storage registers temporarily store data from the array and provide high speed page access to an entire page of data from each bank of the memory. The ability to access one bank while simultaneously opening or closing a row in the other bank allows for an unlimited number of high speed sequential data accesses.

8 Claims, 6 Drawing Sheets
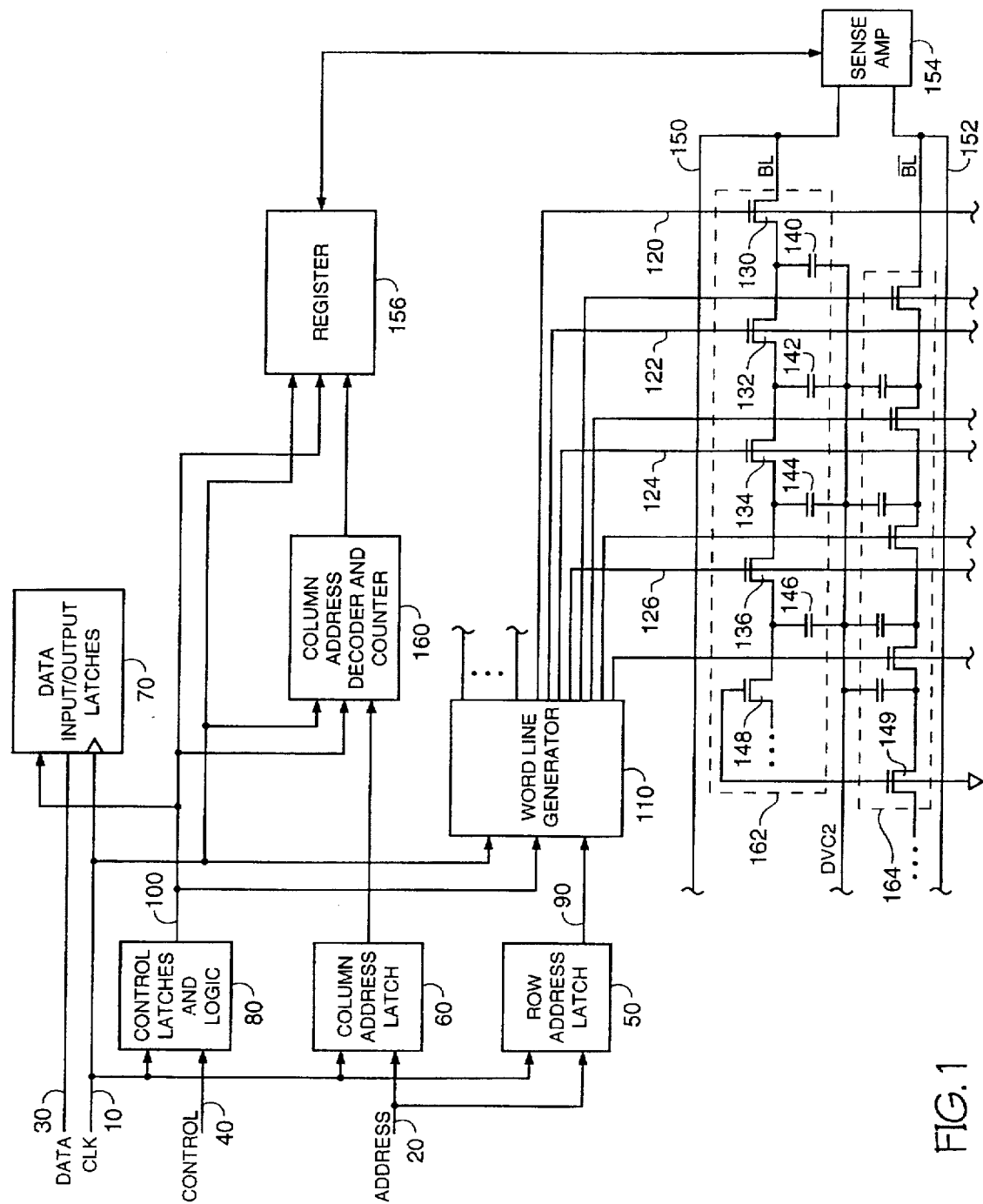
FIG. 1

FIG. 2

FIG. 3

FIG. 4

DOCKET ALARM
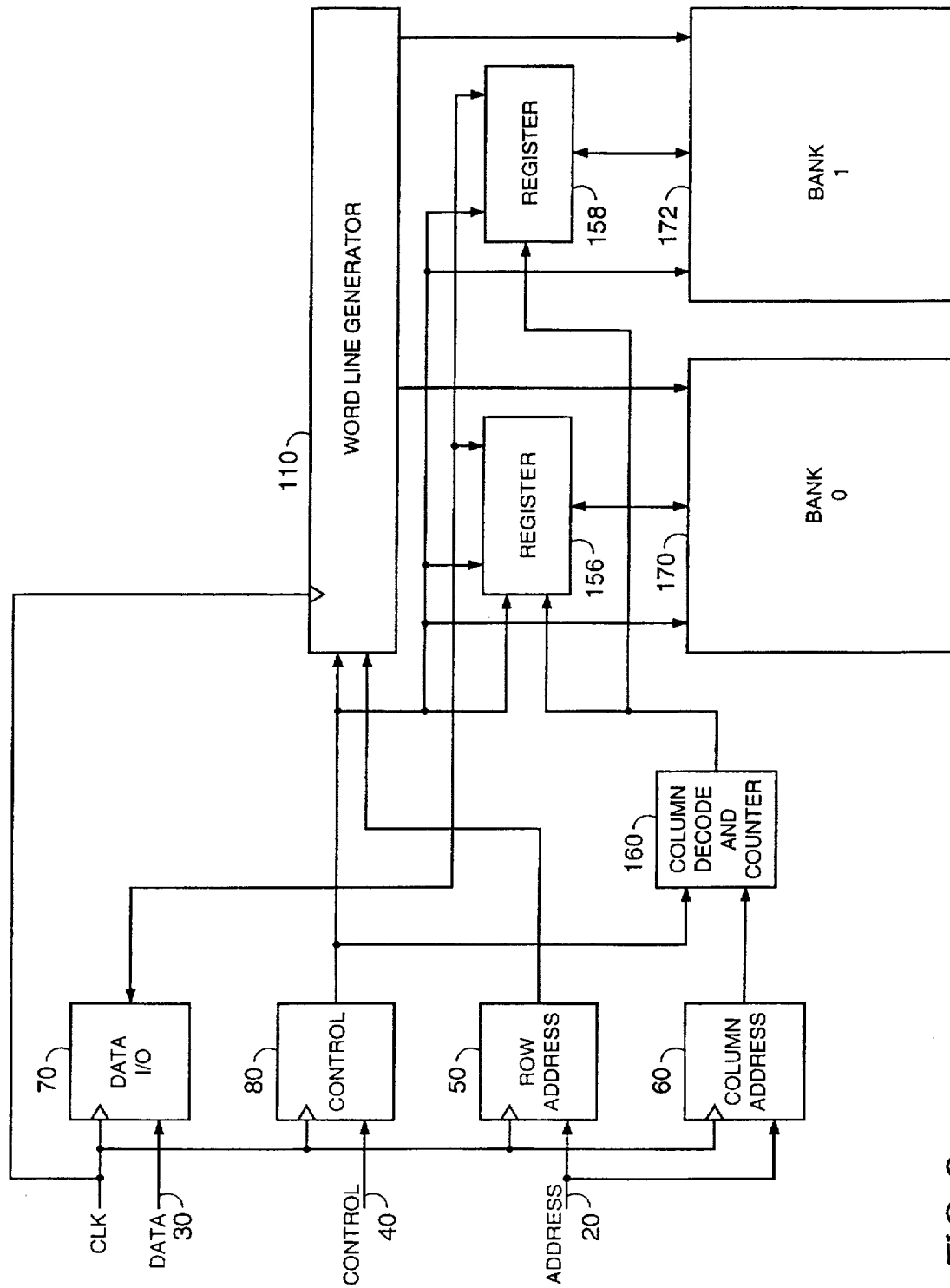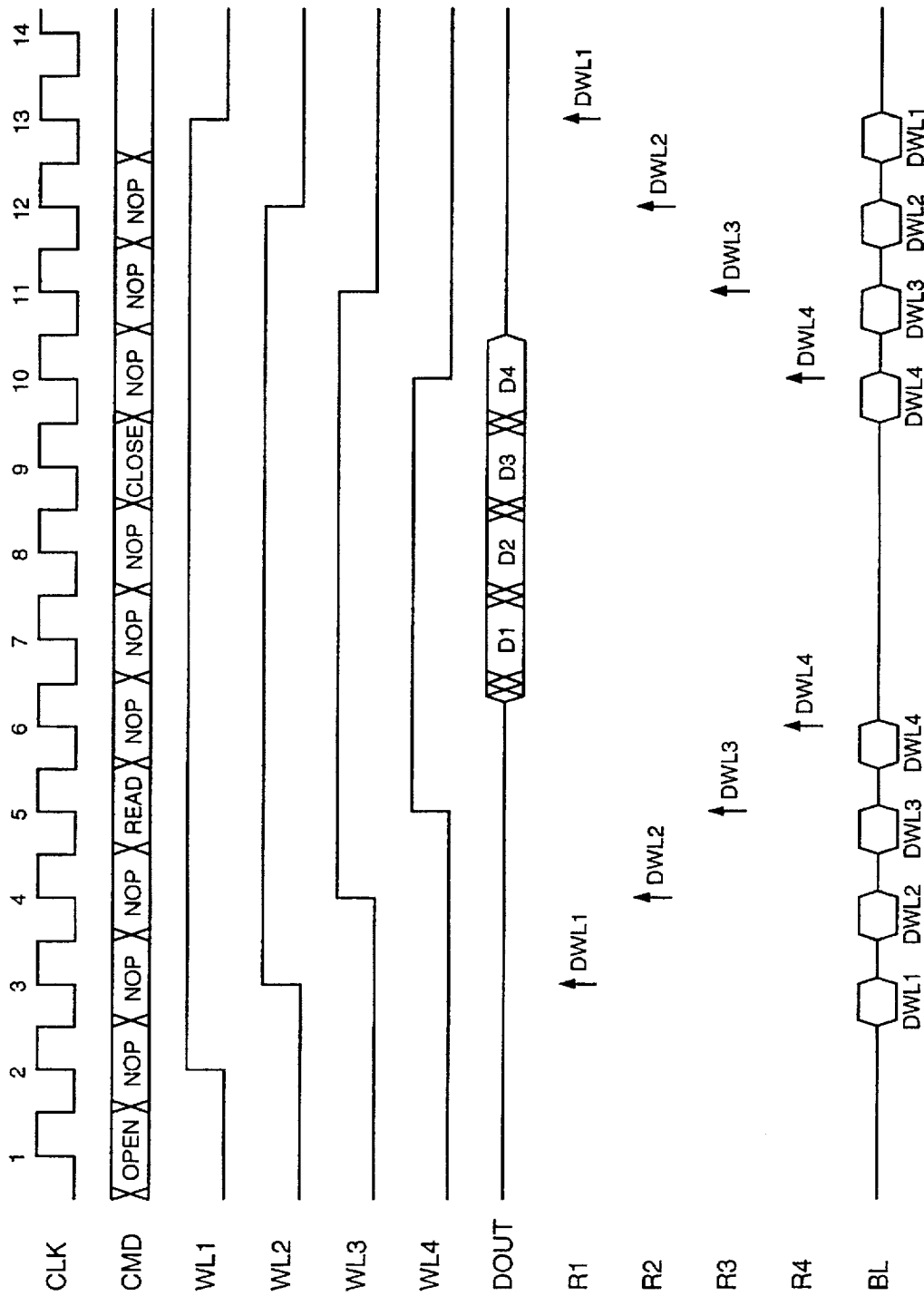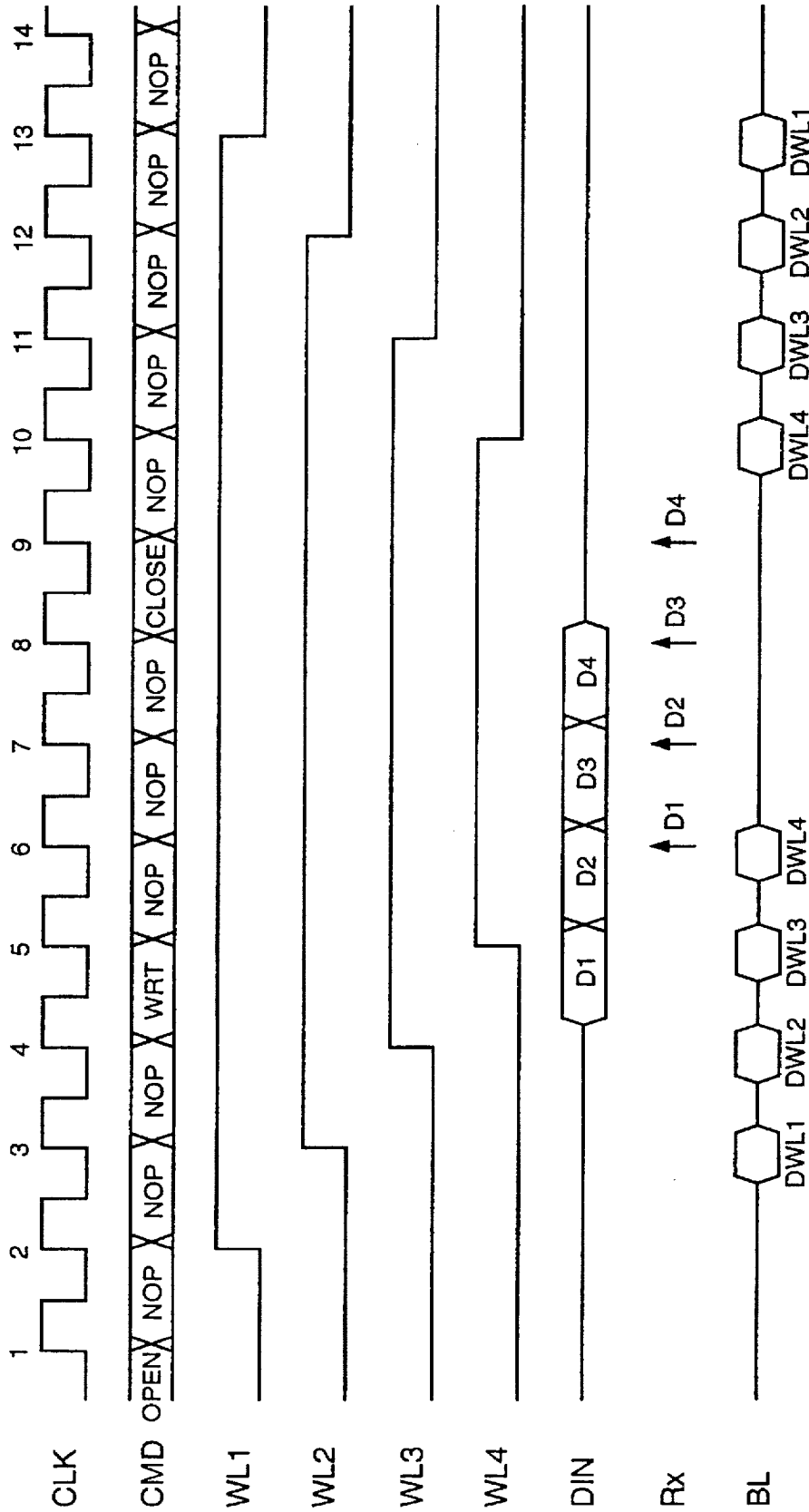
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