IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

MONTEREY RESEARCH, LLC, Plaintiff, vs. QUALCOMM INCORPORATED, QUALCOMM TECHNOLOGIES, INC., and QUALCOMM CDMA TECHNOLOGIES ASIA-PACIFIC PTE LTD., Defendants.	Civil Action No. 19-2083 (NIQA)

DEFENDANT QUALCOMM'S PROPOSED CLAIM CONSTRUCTIONS

Pursuant to the Court's Scheduling Order (Dkt. 30 at 7), Defendants Qualcomm Incorporated, Qualcomm Technologies, Inc., and Qualcomm CDMA Technologies Asia-Pacific PTE Ltd., (collectively "Qualcomm") hereby identify preliminary claim constructions for terms proposed by the parties on February 16, 2021.

Qualcomm reserves the right to modify or supplement these disclosures to facilitate agreement with Monterey, to avoid duplication of terms or phrases, or to reflect newly received information. Furthermore, Qualcomm reserves the right to modify or supplement its preliminary proposed constructions once it has had an opportunity to review Monterey's preliminary proposed constructions.

Qualcomm's list of proposed claim term as well as Qualcomm's preliminary claim constructions have been prepared in response to Monterey's November 20, 2020 Preliminary Disclosure of Asserted Claims and Infringement Contentions. To the extent that Monterey may amend its contentions, Qualcomm reserves the right to modify the list or constructions below. Qualcomm also reserves the right to modify the list or constructions in view of positions taken by Monterey in *inter partes* review proceedings. Qualcomm reserves the right to offer evidence and argument regarding the construction of any terms or elements that are identified by Monterey, or to argue for a plain meaning where it is evident that Monterey's apparent interpretation deviates from that plain meaning.

U.S. Patent Number 6,459,625

Term	Proposed Construction
"An electrical interconnection system to optimize layout of a periphery area in a memory device, comprising:" (cl. 10)	The preamble is limiting
"periphery area of a silicon substrate" (cl. 10)	"section of a flash memory device outside the core cell area"
"first metal layer lines are fabricated to be oriented to extend substantially in one direction" (cl. 10) / "second metal layer lines are fabricated to be oriented to extend substantially perpendicular to said first metal layer lines" (cl. 10) / "said third metal layer lines are fabricated to be oriented to extend substantially parallel to said first metal layer lines" (cl. 10)	Indefinite

U.S. Patent Number 6,534,805

Term	Proposed Construction
"local interconnect layer" (cl. 8, 12, 14, 16, 18, 20)	"distinct process layer that exclusively performs local interconnect functions"
"a single local interconnect layer comprising local interconnects corresponding to bitlines and a global wordline" (cl. 8, 12, 14, 16, 18, 20)	Plain and ordinary meaning, other than "local interconnect layer" construed as above
"polysilicon structure" (cl. 14, etc.)	"structure formed of polysilicon"
"first metal layer" (cl. 53, 59)	"first conductive layer above the local interconnect layer"

U.S. Patent Number 6,642,573

Term	Proposed Construction
"high k dielectric material" (cl. 1)	"dielectric material having a K of about 20 or more"
"mid k dielectric material" (cl. 1, 11)	"dielectric material having a K in the range from greater than 10 to about 20"
"composite dielectric material" (cl. 1, 9, 10, 11, 20)	"dielectric material comprising the elements of at least two other dielectric materials formed by co-deposition of its component elements, or by sequential deposition following by a treatment step"
"ONO structure" (cl. 1)	"stacked structure consisting of a bottom oxide layer, a middle nitride layer, and a top oxide layer"

U.S. Patent Number 6,651,134

Term	Construction
"non-interruptible" (cl. 1, 17)	"once initiated, cannot be stopped or terminated until the fixed number of internal addresses has been generated"
"predetermined number of said internal address signals" (cl. 1, 2, 3, 4, 17, 18)	"number of said internal address signals determined prior to receipt of the external address signal, clock signal, and one or more control signals"
"fixed burst length" (cl. 2, 5)	"burst of a length determined prior to receipt of the external address signal, clock signal, and one or more control signals"
"means for reading data from and writing data to a plurality of storage elements in response to a plurality of internal address signals" (cl. 16)	Function: "reading data from and writing data to a plurality of storage elements in response to a plurality of internal address signals" Structure: the memory array 104 depicted in Figure 1 described as "a static random access memory (SRAM) or a dynamic random access memory (DRAM), or other appropriate memory to meet the design criteria of a particular implementation, or their equivalent"
"means for generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said	Function: "generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal, and (iii) one or more control signals, wherein said generation of said

predetermined number of internal address signals is non-interruptible" (cl. 16)	predetermined number of internal address signals is non-interruptible" Structure: the "circuit 102" depicted in Figure 2 and described at 3:62-4:14, the "circuit 102'" depicted in Figure 3 and described at 4:16-40, or their equivalents.

U.S. Patent Number 6,680,516

Term	Proposed Construction
"semiconductor substrate" (cl. 5)	"supporting semiconductor material upon which or within which elements of the semiconductor device are formed"
"metallic layer" (cl. 5)	"conductive layer comprised of metal, metal alloy, or metal compound."
"etch stop layer" (cl. 5)	"first layer used to significantly slow further progress of an etch of a second layer when the etch reaches the first layer"
"via, through the insulating layer, on the substrate" (cl. 5)	"hole, through the insulating layer and exposing the substrate"

U.S. Patent Number 6,765,407

Term	Proposed Construction
"programmable digital circuit block" (cl. 1, 3, 7, 8, 10, 14, 15)	"programmable digital circuit block that cannot be programmed to perform arbitrary functions"

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