IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

MONTEREY RESEARCH, LLC,	)	
	)	
Plaintiff,	)	
	)	C.A. No. 19-cv-2149-CFC
v.	)	
	)	**JURY TRIAL DEMANDED**
ADVANCED MICRO DEVICES, INC.,	)	
	)	
Defendant.	)	
	)	

FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Monterey Research, LLC ("Monterey"), for its First Amended Complaint for Patent Infringement against Defendant Advanced Micro Devices, Inc. ("AMD"), alleges as follows:

INTRODUCTION

1. Monterey is an intellectual property and technology licensing company. Monterey's patent portfolio comprises over 2,700 active and pending patents worldwide, including approximately 2,000 active United States patents. Monterey's patent portfolio stems from technology developed by a number of leading high-technology companies, including Cypress Semiconductor Corporation, Fujitsu, NVX Corporation, and Ramtron. Those companies developed key innovations that have greatly enhanced the capabilities of computer systems, increased electronic device processing power, and reduced electronic device power consumption. Among other things, those inventions produced significant technological advances, including smaller, faster, and more efficient semiconductors and integrated circuits.

2. AMD infringes Monterey's patents by making, using, selling, offering for sale, and/or importing products (including importing products made by a patented process) throughout the United States, including within this District. AMD's customers incorporate those products into downstream

products that are made, used, sold, offered for sale, and/or imported throughout the United States, including within this District. Those downstream products include, but are not limited to, motherboards, desktop computers, servers, laptop computers, videogame consoles, and other products that include AMD semiconductor devices and integrated circuits.

3. AMD has infringed and continues to infringe Monterey's patents. AMD has thus far refused to license those patents and, instead, has continued to make, use, sell, offer to sell, and/or import Monterey's intellectual property within the United States without Monterey's permission.

NATURE OF THE CASE

4. This action arises under 35 U.S.C. § 271 for AMD's infringement of Monterey's United States Patent Nos. 6,534,805 ("the '805 patent"); 6,629,226 ("the '226 patent"); 6,651,134 ("the '134 patent"); 6,765,407 ("the '407 patent"); 6,961,807 ("the '807 patent"); and 8,373,455 ("the '455 patent") (collectively, "the Patents-in-Suit").

THE PARTIES

5. Plaintiff Monterey is a Delaware limited liability company with offices in New Jersey and California. Monterey maintains a registered agent for service in Delaware: Intertrust Corporate Services Delaware Ltd. located at 200 Bellevue Parkway, Suite 210, Wilmington, Delaware 19808.

6. Defendant AMD is a Delaware corporation with a principal place of business at 2485 Augustine Drive, Santa Clara, California 95054. AMD is a publicly traded company that may be served through its registered agent for service, The Corporation Trust Company, 1209 Orange Street, Wilmington, Delaware 19801.

JURISDICTION AND VENUE

7. This Court has jurisdiction over the subject matter of this action under 28 U.S.C. §§ 1331 and 1338(a) at least because this action arises under the patent laws of the United States, including 35 U.S.C. § 271 *et seq*.

8. Personal jurisdiction exists over AMD at least because AMD is a Delaware corporation organized under the laws of the State of Delaware. AMD also has a registered agent for service of process in Delaware. In addition, AMD has committed, aided, abetted, contributed to, and/or participated in the commission of acts of infringement giving rise to this action within the State of Delaware by, *inter alia*, directly and/or indirectly making, using, selling, offering for sale, importing products, and/or practicing methods that practice one or more claims of the Patents-in-Suit. Furthermore, AMD has transacted and conducted business in the State of Delaware and with Delaware residents by making, using, selling, offering to sell, and/or importing (including importing products made by a patented process) products and instrumentalities that practice one or more claims of the Patents-in-Suit. Among other things, AMD, directly and/or through intermediaries, uses, sells, ships, distributes, imports into, offers for sale, and/or advertises or otherwise promotes its products throughout the United States, including in the State of Delaware. *See, e.g.*, www.amd.com/en. At least for those reasons, AMD has the requisite minimum contacts within the forum such that the exercise of jurisdiction over AMD would not offend traditional notions of fair play and substantial justice.

9. Venue is proper in this Court pursuant to 28 U.S.C. §§ 1391(b) and (c) and 1400(b). AMD resides in this district and has committed acts of infringement in this district. AMD has committed acts of infringement in this district by, among other things, selling and offering for sale in this district (and elsewhere) infringing products made, used, developed, tested, and otherwise practiced by AMD. Venue is further proper based on the facts alleged in the preceding paragraphs, which Monterey incorporates by reference as if fully set forth herein.

THE PATENTS-IN-SUIT

10. Monterey incorporates by reference the preceding paragraphs as if fully set forth herein.

A. U.S. Patent No. 6,534,805

11. The ’805 patent, titled “SRAM Cell Design,” was duly and properly issued by the United States Patent and Trademark Office (“USPTO”) on March 18, 2003. On October 14, 2014, the USPTO issued an Ex Parte Reexamination Certificate for the ’805 patent, which confirmed the patentability of the ’805 patent. A true and correct copy of the ’805 patent and the Ex Parte Reexamination Certificate for the ’805 patent is attached hereto as Exhibit A.

12. Monterey is the owner and assignee of the ’805 patent; owns all right, title, and interest in the ’805 patent; and holds the right to sue and recover damages for infringement thereof, including past infringement.

B. U.S. Patent No. 6,629,226

13. The ’226 patent, titled “FIFO Read Interface Protocol,” was duly and properly issued by the USPTO on September 30, 2003. A true and correct copy of the ’226 patent is attached hereto as Exhibit B.

14. Monterey is the owner and assignee of the ’226 patent; owns all right, title, and interest in the ’226 patent; and holds the right to sue and recover damages for infringement thereof, including past infringement.

C. U.S. Patent No. 6,651,134

15. The ’134 patent, titled “Memory Device with Fixed Length Non Interruptible Burst,” was duly and properly issued by the USPTO on November 18, 2003. A true and correct copy of the ’134 patent is attached hereto as Exhibit C.

16. Monterey is the owner and assignee of the ’134 patent; owns all right, title, and interest in the ’134 patent; and holds the right to sue and recover damages for infringement thereof, including past infringement.

D. U.S. Patent No. 6,765,407

17. The ’407 patent, titled “Digital Configurable Macro Architecture,” was duly and properly issued by the USPTO on July 20, 2004. A true and correct copy of the ’407 patent is attached hereto as Exhibit D.

18. Monterey is the owner and assignee of the ’407 patent; owns all right, title, and interest in the ’407 patent; and holds the right to sue and recover damages for infringement thereof, including past infringement.

E. U.S. Patent No. 6,961,807

19. The ’807 patent, titled “Device, System and Method for an Integrated Circuit Adaptable for Use in Computing Systems of Differing Memory Requirements,” was duly and properly issued by the USPTO on November 1, 2005. A true and correct copy of the ’807 patent is attached hereto as Exhibit E.

20. Monterey is the owner and assignee of the ’807 patent; owns all right, title, and interest in the ’807 patent; and holds the right to sue and recover damages for infringement thereof, including past infringement.

F. U.S. Patent No. 8,373,455

21. The ’455 patent, titled “Output Buffer Circuit,” was duly and properly issued by the USPTO on February 12, 2013. A true and correct copy of the ’455 patent is attached hereto as Exhibit F.

22. Monterey is the owner and assignee of the ’455 patent; owns all right, title, and interest in the ’455 patent; and holds the right to sue and recover damages for infringement thereof, including past infringement.

FACTUAL BACKGROUND

23. Monterey incorporates by reference the preceding paragraphs as if fully set forth herein.

24. The Patents-in-Suit stem from the research and design of innovative and proprietary technology developed by leading high-technology companies, including Cypress Semiconductor Corporation ("Cypress"). Cypress is an American multinational company and pioneer of cutting-edge semiconductor technology. Founded in 1982, Cypress has made substantial investments in researching, developing, and manufacturing high-quality semiconductor devices, integrated circuits, and products containing the same.

25. The Patents-in-Suit are directed to inventive technology relating to semiconductor devices, integrated circuits, and/or products containing the same.

26. Defendant AMD works closely with its customers, OEMs, foundry suppliers, distributors, and/or other third parties to make, use, sell, offer to sell, and/or import semiconductor devices, integrated circuits, and/or products containing the same. Among other things, AMD optimizes its manufacturing process for its customers and optimizes its products for integration into downstream products. AMD's affirmative acts in furtherance of the manufacture, use, sale, offer to sell, and importation of its products in and/or into the United States include, but are not limited to, any one or combination of: (i) designing specifications for manufacture of its products; (ii) collaborating on, encouraging, and/or funding the development of processes for the manufacture of its products; (iii) soliciting and/or sourcing the manufacture of its products; (iv) licensing, developing, and/or transferring technology and know-how to enable the manufacture of its products; (v) enabling and encouraging the use, sale, or importation of its products in the United States; and (vi) advertising its products and/or downstream products incorporating them in the United States.

27. AMD also provides marketing and/or technical support services for its products from its facilities in the United States. For example, AMD maintains a website that advertises its products, including identifying the applications for which they can be used and providing specifications for its

products. *See, e.g.*, www.amd.com/en. AMD's publicly-available website also contains user manuals, product documentation, and other materials related to its products. *See, e.g.*, www.amd.com/en. For example, AMD's website contains a knowledge base, software help center, support forum, technical documents, and downloadable graphics drivers. *See, e.g.*, www.amd.com/en.

AMD'S PRE-SUIT KNOWLEDGE OF MONTEREY'S PATENTS AND CHARGE OF INFRINGEMENT

28. Monterey notified AMD that it infringes the '805, '134, '807, and '455 patents on September 24, 2018.

29. AMD was placed on notice of the '407 patent for purposes of 35 U.S.C. § 287(a) as of January 26, 2018, when Monterey sent a notice letter to AMD informing them of the patent and identifying covered AMD products.

COUNT ONE
INFRINGEMENT OF THE '805 PATENT

30. Monterey incorporates by reference the preceding paragraphs as if fully set forth herein.

31. Monterey is the assignee and lawful owner of all right, title, and interest in and to the '805 patent.

32. The '805 patent is valid and enforceable.

33. The '805 patent is generally directed to static random access memory ("SRAM") cell design, particularly to optimizing SRAM cell design using a simpler geometric layout.

34. As semiconductor structure size continued to shrink with time, one exemplary issue with the prior art of the '805 patent was increased difficulties in manufacturing. Specifically, the then-existing memory cells contained complex geometric designs which required numerous processing steps and larger cell sizes. Generally, more processing steps lead to increased

manufacturing costs and reduced profits.

35. The ’805 patent teaches, among other things, an improved memory cell layout which allows the features to be arranged in such a way as to minimize cell size. For example, the single local interconnect layer of the ’805 patent allows for a thinner product and fewer processing steps.

36. AMD products use SRAM with a six-transistor (“6T”) and/or eight-transistor (“8T”) cell design. AMD’s 6T and 8T SRAM contain a single local interconnect layer. This has resulted in, among other things, AMD’s ability to decrease the size of its SRAM area and to decrease the number of manufacturing steps.

37. AMD has directly infringed, and continues to directly infringe, one or more claims of the ’805 patent under 35 U.S.C. § 271(a), either literally and/or under the doctrine of equivalents, by, among other things, making, using, selling, offering to sell, and/or importing in or into the United States without authorization products covered by one or more claims of the ’805 patent, including, but not limited to, all AMD devices incorporating SRAM with a 6T and/or 8T cell design, such as the A8-3800 semiconductor device and other products in the A-Series, Pro A-Series, Ryzen, Ryzen Pro, Athlon, Epyc, FX, E-Series, Opteron, Phenom, Sempron, and the Turion product families; and all other semiconductor devices, integrated circuits, and products with similar infringing technology (“the Accused ’805 Products”).

38. As one non-limiting example, AMD infringes claim 8 of the ’805 patent. For example, the A8-3800 semiconductor device contains:

a. a memory cell (e.g., SRAM cell of the A8-3800) comprising a plurality of substantially oblong active regions (e.g., N-type and/or P-type diffusion areas of the A8-3800) formed in a semiconductor substrate and arranged substantially in parallel with one another, and a plurality of substantially oblong local interconnects (e.g., structures formed at the polysilicon layer

on top of the substrate of the A8-3800) above said substrate that extend only partially across the memory cell and are arranged substantially in parallel with one another and substantially perpendicular to said active regions; and

b. a single local interconnect layer (e.g., metal 1 ("M1") layer of the A8-3800) comprising local interconnects (e.g., structures formed at the M1 layer of the A8-3800) corresponding to bitlines (e.g., those formed at the metal 2 ("M2") layer of the A8-3800) and a global word-line (e.g., those formed at the metal 3 ("M3") layer of the A8-3800).

39. Claim 8 of the '805 patent applies to each Accused '805 Product at least because each of those products contain the same or similar structures as the AMD A8-3800.

40. Monterey has complied with the requirements of 35 U.S.C. § 287(a) at least because Monterey provided AMD with written notice of its infringement as discussed above.

41. AMD was on notice of the '805 patent under 35 U.S.C. § 287(a) at least as early as September 24, 2018.

42. AMD, knowing its products infringe the '805 patent and with the specific intent for others to infringe the '805 patent, has induced infringement of, and continues to induce infringement of, one or more claims of the '805 patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, by, among other things, actively inducing others, including its customers, to make, use, sell, offer to sell, and/or import in or into the United States without authorization the Accused '805 Products, as well as products containing the same. AMD knowingly and intentionally instructs its customers, OEMs, foundry suppliers, distributors, and/or third parties to infringe at least through user manuals, product documentation, and other materials, such as those located on AMD's website at www.amd.com/en. For example, AMD provides data sheets, programmer references, design guides, revision guides, diagrams, white papers, and software instructing customers on uses

of AMD's products that infringe the '805 patent. *See, e.g.*, https://www.amd.com/en/support/tech-docs: https://www.amd.com/system/files/TechDocs/53738_PDS_Athlon.pdf. Additional non-limiting examples include the materials found on AMD's websites at www.amd.com/en/processors/athlon-and-a-series and www.amd.com/en/products/specifications/processors/.

43. AMD has contributed to the infringement of, and continues to contribute to the infringement of, one or more claims of the '805 patent under 35 U.S.C. § 271(c), either literally and/or under the doctrine of equivalents, by, among other things, selling, offering to sell, and/or importing in or into the United States the Accused '805 Products, which constitute a material part of the invention of the '805 patent, knowing the Accused '805 Products to be especially made or especially adapted for use in an infringement of such patent, and not a staple article or commodity of commerce suitable for substantial noninfringing use. *See, e.g.*, https://www.amd.com/en/support/tech-docs: https://www.amd.com/system/files/TechDocs/53738_PDS_Athlon.pdf.

44. Monterey has sustained and is entitled to recover damages as a result of AMD's infringement.

45. AMD's infringement of the '805 patent has been knowing, deliberate, and willful, beginning at least as early as November 15, 2019, the date Monterey filed the first complaint in this action and therefore at least the date by which AMD knew of the '805 patent and that its conduct constituted and resulted in infringement of the '805 patent. AMD nonetheless has committed—and continues to commit—acts of direct and indirect infringement despite knowing that its actions constituted infringement of the valid and enforceable '805 patent, despite a risk of infringement that was known or so obvious that it should have been known to AMD, and/or even though AMD otherwise knew or should have known that its actions constituted an unjustifiably high risk of

infringement of that valid and enforceable patent. AMD's conduct in light of these circumstances is egregious. AMD's knowing, deliberate, and willful infringement of the '805 patent entitles Monterey to increased damages under 35 U.S.C. § 284 and to attorney fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

COUNT TWO
INFRINGEMENT OF THE '226 PATENT

46. Monterey incorporates by reference the preceding paragraphs as if fully set forth herein.

47. Monterey is the assignee and lawful owner of all right, title, and interest in and to the '226 patent.

48. The '226 patent is valid and enforceable.

49. The '226 patent is generally directed to a method and/or architecture for implementing a multiqueue memory read interface, and more particularly, to a method and/or architecture for implementing a multiqueue read interface protocol for eliminating synchronizing problems for configuration dependent latencies where the protocol may be capable of handling variable size packets.

50. The '226 patent explains that in prior multiqueue memories (e.g., first-in-first-out ("FIFO") memory), a signal, e.g., ADDRESS, was a queue address configured to determine a queue number of the multiqueue memory. The signals, e.g., READ_CLOCK and READ_EN, could control the timing of the presentation of the data signal, e.g., DATA. Because of particular architectures and specifications of particular devices, the latency between enabling a queue address signal, e.g., ADDRESS, and presenting a data signal, e.g., DATA, could differ depending on the particular configuration. Configuration information needed to be written into an external read device. The only event reference available to the external read device was an end of packet or a start of packet, e.g.,

EOP or SOP. In such an environment, the read device was required to monitor this event to generate the queue address signal, e.g., ADDRESS, in a sufficient number of cycles ahead of the read.

51. These prior multiqueue memory systems had the disadvantage of requiring a fixed packet size. A circuit could be required to generate the queue address, e.g., ADDRESS, a certain number of cycles before the end of packet occurs. The particular number of cycles may be the same as the minimum latency requirement. For certain configurations, there was a specific latency between the queue address signal, e.g., ADDRESS, and presenting the signal, e.g., DATA. If the packet size varied randomly, such as when the size of the packet was less than the number of cycles of latency, a read of one or more unwanted packets occurred. Additionally, it may have been difficult for the read device to synchronize the queue address signal, e.g., ADDRESS, with the data received from the memory (e.g., FIFO). Therefore, the read device needed to be configured with enough logic to respond to the different latencies. Such a configuration required extra overhead for the read device.

52. The ’226 patent teaches, among other things, an interface coupled to a multiqueue storage device and configured to interface the multiqueue storage device with one or more handshaking signals. The multiqueue storage device and the interface may be configured to transfer variable size data packets. Such a system provided numerous benefits, including but not limited to: (i) eliminating synchronizing problems with configuration dependent latencies; (ii) being capable of handling variable size packets; (iii) allowing back-to-back reads of variable size packets; and (iv) exchanging address and data between an external read device and a multiqueue storage device.

53. AMD products use a multiqueue storage device, such as an NVM Express (“NVME”) compliant memory. NVME compliant memory can be found in, among other products, the AMD Pro SSG. AMD products use multiqueue storage devices that are compliant with the NVME Base Specification standard and similar versions of the NVME standard that incorporate the innovations

of the ’226 patent’s multiqueue memory read interface. AMD’s multiqueue storage device further interfaces with handshaking signals, and allows back-to-back reads of variable size data packets.

54. AMD has directly infringed, and continues to directly infringe, one or more claims of the ’226 patent under 35 U.S.C. § 271(a), either literally and/or under the doctrine of equivalents, by, among other things, making, using, selling, offering to sell, and/or importing in or into the United States without authorization products covered by one or more claims of the ’226 patent, including, but not limited to, products supporting NVME or with NVME compliant memory, such as the Radeon Pro SSG semiconductor device and other products in the Radeon Pro, Epyc and Ryzen product families; other AMD semiconductor devices, integrated circuits, and products built to utilize NVME compliant memory; and all other semiconductor devices, integrated circuits, and products using a similar multiqueue memory read interface (“the Accused ’226 Products”).

55. As one non-limiting example, AMD infringes claim 18 of the ’226 patent. For example, the Radeon Pro SSG semiconductor device contains: An interface coupled to a multiqueue storage device (e.g., multiqueue memory of the Radeon Pro SSG) and configured to interface said multiqueue storage device with one or more handshaking signals (e.g., data link packets and/or command set of the Radeon Pro SSG), wherein said multiqueue storage device and said interface are configured to allow back-to-back reads of variable size data packets (e.g., via sequential read requests and/or burst read requests, and/or a Scatter Gather List of the Radeon Pro SSG).

56. Claim 18 of the ’226 patent applies to each Accused ’226 Product at least because each of those products contain infringing NVME compliant memory; and/or contain a multiqueue storage device with similar infringing functionality.

57. Monterey has complied with the requirements of 35 U.S.C. § 287(a) at least because Monterey provided AMD with written notice of its infringement.

58. AMD was on notice of the ’226 patent at least as early as November 15, 2019, the date Monterey filed the first complaint in this action.

59. AMD, knowing its products infringe the ’226 patent and with the specific intent for others to infringe the ’226 patent, has induced infringement of, and continues to induce infringement of, one or more claims of the ’226 patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, by, among other things, actively inducing others, including its customers, to make, use, sell, offer to sell, and/or import (including import products made by a patented process) in or into the United States without authorization the Accused ’226 Products, as well as products containing the same. AMD knowingly and intentionally instructs its customers, OEMs, foundry suppliers, distributors, and/or other third parties to infringe at least through user manuals, product documentation, and other materials, such as those located on AMD’s website at www.amd.com/en. For example, AMD provides data sheets, programmer references, design guides, revision guides, diagrams, white papers, and software instructing customers on uses of AMD’s products that infringe the ’226 patent. *See, e.g.*, https://www.amd.com/en/support/tech-docs: https://www.amd.com/system/files/TechDocs/56245-PUB.pdf. Additional non-limiting examples include the materials found on AMD’s websites at www.amd.com/en/chipsets/str40 and www.amd.com/en/chipsets/x570.

60. AMD has contributed to the infringement of, and continues to contribute to the infringement of, one or more claims of the ’226 patent under 35 U.S.C. § 271(c), either literally and/or under the doctrine of equivalents, by, among other things, selling, offering to sell, and/or importing in or into the United States the Accused ’226 Products, which constitute a material part of the invention of the ’226 patent, knowing the Accused ’226 Products to be especially made or especially adapted for use in an infringement of such patent, and not a staple article or commodity of commerce

suitable for substantial noninfringing use. *See, e.g.*, https://www.amd.com/en/support/tech-docs: https://www.amd.com/system/files/TechDocs/56245-PUB.pdf.

61. Monterey has sustained and is entitled to recover damages as a result of AMD's infringement.

62. AMD's infringement of the '226 patent has been knowing, deliberate, and willful, beginning at least as early as November 15, 2019, the date Monterey filed the first complaint in this action and therefore at least the date by which AMD knew of the '226 patent and knew that its conduct constituted and resulted in infringement of the '226 patent. AMD nonetheless has committed—and continues to commit—acts of direct and indirect infringement despite knowing that its actions constituted infringement of the valid and enforceable '226 patent, despite a risk of infringement that was known or so obvious that it should have been known to AMD, and/or even though AMD otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. AMD's conduct in light of these circumstances is egregious. AMD's knowing, deliberate, and willful infringement of the '226 patent entitles Monterey to increased damages under 35 U.S.C. § 284 and to attorney fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

COUNT THREE
INFRINGEMENT OF THE '134 PATENT

63. Monterey incorporates by reference the preceding paragraphs as if fully set forth herein.

64. Monterey is the assignee and lawful owner of all right, title, and interest in and to the '134 patent.

65. The '134 patent is valid and enforceable.

66. The '134 patent generally concerns memory devices, and is more specifically related

to non-interruptible burst read and write access features, as described in JEDEC standard JESD212 GDDR5 SGRAM and similar versions of the JEDEC GDDRx standards.

67. The ’134 patent provides a faster and more efficient way for burst read and write access over conventional DRAM devices existing when the patent was filed in early 2000. Prior to the ’134 patent, DRAM memory devices had a burst mode that had the possibility of needing to continually perform interrupts to perform data refreshes.

68. The ’134 patent teaches, among other things, a fixed burst memory that can have non-interruptible bursts, hide required DRAM refreshes inside a known fixed burst length, free up the address and control busses for multiple cycles, and operate at higher frequencies without needing interrupts to perform refreshes of data.

69. AMD products use memory devices that are compliant with the JESD212 GDDR5 SGRAM standard and similar versions of the JEDEC GDDRx standards that incorporate the innovations of the ’134 patent’s non-interruptible fixed burst length.

70. AMD has directly infringed, and continues to directly infringe, one or more claims of the ’134 patent under 35 U.S.C. § 271(a), either literally and/or under the doctrine of equivalents, by, among other things, making, using, selling, offering to sell, and/or importing in or into the United States without authorization products covered by one or more claims of the ’134 patent, including, but not limited to, products that comply with the JEDEC standards JESD212 GDDR5 SGRAM and similar versions of the JEDEC GDDRx standards that use non-interruptible burst read or write operations, such as the Radeon RX 580 graphics card and other products in the Radeon, Radeon Pro, Embedded Radeon, Mobility Platforms, Instinct, FireStream, and the FirePro product families; the Neo and Liverpool graphics processors; other AMD semiconductor devices, integrated circuits, and products that are compliant with the JESD212 GDDR5 SGRAM standard or similar versions; and all

other semiconductor devices, integrated circuits, and products with similar infringing technology ("the Accused '134 Products").

71. As one non-limiting example, AMD infringes claim 1 of the '134 patent since the AMD Radeon RX 580 semiconductor device contains DDR3 SGRAM memory controllers that operate in conformance with JEDEC's DDR3 SGRAM standard. For example, the AMD Radeon RX 580 contains a circuit comprising:

a. a memory comprising a plurality of storage elements (e.g., banks of storage elements of the Radeon RX 580);

b. each configured to read and write data in response to an internal address signal (e.g., stored bits of memory bank addressed and defined by internal addresses of the Radeon RX 580);

c. a logic circuit configured to generate a predetermined number of said internal address signals (e.g., generating addresses based on bank addresses, row addresses, and column addresses of the Radeon RX 580) in response to an external address signal (e.g., read and/or write signals of the Radeon RX 580), a clock signal (e.g., clock signal of the Radeon RX 580), and one or more control signals (e.g., control signal of the Radeon RX 580);

d. wherein said generation of said predetermined number of internal address signals is non-interruptible (e.g., burst reads or writes cannot be terminated or interrupted in the Radeon RX 580).

72. Claim 1 of the '134 patent applies to each Accused '134 Product at least because each of those products either complies with the same JEDEC JESD212 GDDR5 SGRAM standard, or similar versions of the JEDEC standard, which result in infringing features (e.g., non-interruptible burst oriented read or write operations of the Accused '134 Products) found in the JESD212 GDDR5

SGRAM standard.

73. Monterey has complied with the requirements of 35 U.S.C. § 287(a) at least because Monterey provided AMD with written notice of its infringement as discussed above.

74. AMD was on notice of the ’134 patent under 35 U.S.C. § 287(a) at least as early as September 24, 2018.

75. AMD, knowing its products infringe the ’134 patent and with the specific intent for others to infringe the ’134 patent, has induced infringement of, and continues to induce infringement of, one or more claims of the ’134 patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, by, among other things, actively inducing others, including its customers, to make, use, sell, offer to sell, and/or import in or into the United States without authorization the Accused ’134 Products, as well as products containing the same. AMD knowingly and intentionally instructs its customers, OEMs, foundry suppliers, distributors, and/or other third parties to infringe at least through user manuals, product documentation, and other materials, such as those located on AMD’s website at www.amd.com/en. For example, AMD provides data sheets, programmer references, design guides, revision guides, diagrams, white papers, and software instructing customers on uses of AMD’s products that infringe the ’134 patent. *See, e.g.*, https://www.amd.com/en/support/tech-docs and https://www.amd.com/en/support/graphics/radeon-500-series/radeon-rx-500-series/radeon-rx-580. Additional non-limiting examples include the materials found on AMD’s website at www.amd.com/en/products/graphics/radeon-rx-580#product-specs.

76. AMD has contributed to the infringement of, and continues to contribute to the infringement of, one or more claims of the ’134 patent under 35 U.S.C. § 271(c), either literally and/or under the doctrine of equivalents, by, among other things, selling, offering to sell, and/or importing

in or into the United States the Accused '134 Products, which constitute a material part of the invention of the '134 patent, knowing the Accused '134 Products to be especially made or especially adapted for use in an infringement of such patent, and not a staple article or commodity of commerce suitable for substantial noninfringing use. *See, e.g.*, https://www.amd.com/en/support/tech-docs and https://www.amd.com/en/support/graphics/radeon-500-series/radeon-rx-500-series/radeon-rx-580.

77. Monterey has sustained and is entitled to recover damages as a result of AMD's infringement.

78. AMD's infringement of the '134 patent has been knowing, deliberate, and willful, beginning at least as early as November 15, 2019, the date Monterey filed the first complaint in this action and therefore at least the date by which AMD knew of the '134 patent and knew that its conduct constituted and resulted in infringement of the '134 patent. AMD nonetheless has committed—and continues to commit—acts of direct and indirect infringement despite knowing that its actions constituted infringement of the valid and enforceable '134 patent, despite a risk of infringement that was known or so obvious that it should have been known to AMD, and/or even though AMD otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. AMD's conduct in light of these circumstances is egregious. AMD's knowing, deliberate, and willful infringement of the '134 patent entitles Monterey to increased damages under 35 U.S.C. § 284 and to attorney fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

COUNT FOUR
INFRINGEMENT OF THE '407 PATENT

79. Monterey incorporates by reference the preceding paragraphs as if fully set forth herein.

80. Monterey is the assignee and lawful owner of all right, title, and interest in and to the

’407 patent.

81. The ’407 patent is valid and enforceable.

82. The ’407 patent is generally directed to programmable digital circuit architecture, and particularly to programmable digital devices which are configurable to perform any one of various digital functions, by changing the contents of a register.

83. The ’407 patent explains that microcontrollers or controllers have been utilized in various applications for many years. Microcontrollers are frequently found in, for example: appliances, computers and computer equipment, automobiles, environmental control, aerospace, and thousands of other uses. Prior to the ’407 patent, field programmable gate arrays (“FPGA”) were utilized in several microcontroller applications. FPGAs are highly inefficient with respect to chip area, increasing their cost. Moreover, FPGAs need to have their look-up tables re-programmed in order to enable them to implement a new digital function, which is a time consuming task. FPGAs are not ideally suited for microcontroller applications, since, for example, microcontroller applications are very cost-sensitive. A FPGA is not able to realize the number of digital functions that are demanded by certain microcontroller applications within these strict cost constraints.

84. The ’407 patent teaches, among other things, a programmable digital circuit block that can be programmed to perform a variety of predetermined digital functions upon being configured with a single register write operation. This solution allows the configuration of the programmable digital circuit block to be determined by a small number of configuration registers, providing much flexibility. In particular, the configuration of the programmable digital circuit block is fast and easy since changes in configuration are accomplished by changing the contents of the configuration registers, whereas the contents are generally a small number of configuration data bits.

85. AMD products use an array of programmable digital circuit blocks, such as Zen or

Family 17h cores. For example, the Zen or Family 17h core can be found in a number of different AMD Zen microarchitecture based products, as it functions as a processing core of the AMD Zen microarchitecture based processor. The Zen or Family 17h core is programmable to perform a variety of predetermined digital functions by changing the contents of a register.

86. AMD has directly infringed, and continues to directly infringe, one or more claims of the ’407 patent under 35 U.S.C. § 271(a), either literally and/or under the doctrine of equivalents, by, among other things, making, using, selling, offering to sell, and/or importing in or into the United States without authorization products covered by one or more claims of the ’407 patent, including, but not limited to, products with multiple cores utilizing the AMD64 instruction set, such as the Ryzen 3 1200 semiconductor device and other products in the Ryzen, Ryzen Pro, Athlon, Epyc, A-Series, Pro A-Series, FX, E-Series, Opteron, Phenom, Sempron, and the Turion product families; other multicore AMD semiconductor devices, integrated circuits, and products built to utilize the AMD64 instruction set; and all other semiconductor devices, integrated circuits, and products using a similar instruction set (“the Accused ’407 Products”).

87. As one non-limiting example, AMD infringes claim 8 of the ’407 patent. For example, the Ryzen 3 semiconductor device contains:

a. an array of programmable digital circuit block (e.g., Zen or Family 17H cores of the Ryzen 3);

b. where each programmable digital circuit block is configurable to perform a predetermined digital function (e.g., operating a secure virtual machine of the Ryzen 3);

c. upon being configured with a single register write operation (e.g., writing the EFER register of the Ryzen 3).

88. Claim 8 of the ’407 patent applies to each Accused ’407 Product at least because each

of those products contain infringing Zen, Family 17h, or newer cores; and/or contain AMD64 instruction set based cores containing similar infringing functionality.

89. Monterey has complied with the requirements of 35 U.S.C. § 287(a) at least because Monterey provided AMD with written notice of its infringement as discussed above.

90. AMD was on notice of the '407 patent under 35 U.S.C. § 287(a) at least as early as January 26, 2018.

91. AMD, knowing its products infringe the '407 patent and with the specific intent for others to infringe the '407 patent, has induced infringement of, and continues to induce infringement of, one or more claims of the '407 patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, by, among other things, actively inducing others, including its customers, to make, use, sell, offer to sell, and/or import (including import products made by a patented process) in or into the United States without authorization the Accused '407 Products, as well as products containing the same. AMD knowingly and intentionally instructs its customers, OEMs, foundry suppliers, distributors, and/or other third parties to infringe at least through user manuals, product documentation, and other materials, such as those located on AMD's website at www.amd.com/en. For example, AMD provides data sheets, programmer references, design guides, revision guides, diagrams, white papers, and software instructing customers on uses of AMD's products that infringe the '407 patent. *See, e.g.*, https://www.amd.com/en/support/tech-docs: https://www.amd.com/system/files/TechDocs/AMD%20Ryzen%20Processor%20and%20AMD%20Ryzen%20Master%20Overclocking%20Users%20Guide.pdf. Additional non-limiting examples include the materials found on AMD's websites at www.amd.com/en/technologies/zen-core and www.amd.com/system/files/TechDocs/24593.pdf .

92. AMD has contributed to the infringement of, and continues to contribute to the

infringement of, one or more claims of the ’407 patent under 35 U.S.C. § 271(c), either literally and/or under the doctrine of equivalents, by, among other things, selling, offering to sell, and/or importing in or into the United States the Accused ’407 Products, which constitute a material part of the invention of the ’407 patent, knowing the Accused ’407 Products to be especially made or especially adapted for use in an infringement of such patent, and not a staple article or commodity of commerce suitable for substantial noninfringing use. *See, e.g.*, https://www.amd.com/en/support/tech-docs: https://www.amd.com/system/files/TechDocs/AMD%20Ryzen%20Processor%20and%20AMD%20Ryzen%20Master%20Overclocking%20Users%20Guide.pdf.

93. Monterey has sustained and is entitled to recover damages as a result of AMD’s infringement.

94. AMD’s infringement of the ’407 patent has been knowing, deliberate, and willful, beginning at least as early as November 15, 2019, the date Monterey filed the first complaint in this action and therefore at least the date by which AMD knew of the ’407 patent and knew that its conduct constituted and resulted in infringement of the ’407 patent. AMD nonetheless has committed—and continues to commit—acts of direct and indirect infringement despite knowing that its actions constituted infringement of the valid and enforceable ’407 patent, despite a risk of infringement that was known or so obvious that it should have been known to AMD, and/or even though AMD otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. AMD’s conduct in light of these circumstances is egregious. AMD’s knowing, deliberate, and willful infringement of the ’407 patent entitles Monterey to increased damages under 35 U.S.C. § 284 and to attorney fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

COUNT FIVE
INFRINGEMENT OF THE ’807 PATENT

95. Monterey incorporates by reference the preceding paragraphs as if fully set forth herein.

96. Monterey is the assignee and lawful owner of all right, title, and interest in and to the ’807 patent.

97. The ’807 patent is valid and enforceable.

98. The ’807 patent is generally directed to integrated circuits and associated memory systems.

99. The ’807 patent explains that in the design of an integrated circuit incorporating a microprocessor, microcontroller, or other logic, it is often difficult to determine the appropriate amount of on-chip memory to incorporate on the die in order to suit the many applications that the integrated circuit may serve.

100. For example, a large amount of on-chip static memory (e.g., RAM) provided the benefit of fast program execution but had a disadvantage in that the large on-chip RAM required an initial program loading operation from an off-chip non-volatile memory (e.g., Flash ROM), which could have the program content stored therein. The use of such a non-volatile memory might add additional costs to the overall system that utilizes the integrated circuit, in part because the integrated circuit packages and corresponding pin counts might be quite large. For example, the interface between the external Flash ROM and the integrated circuit might include a parallel interface having 30 or more pins, which increased the complexity, size, and cost of use of such a system. While the cost and size of such an arrangement might be acceptable in the design of large, complex systems, the cost and size of such an arrangement might be unacceptable if the integrated circuit is to be used in a simple, low-cost system.

101. Alternatively, a large amount of non-volatile memory incorporated on-chip with the

integrated circuit had the advantage of relatively low costs when compared with an arrangement that uses on-chip RAM/external Flash ROM. However, such an arrangement had the disadvantage of relatively slower program execution when compared with on-chip RAM/external Flash ROM, which might be unacceptable for use in a large, complex system.

102. The ’807 patent teaches, among other things, a microprocessor, a cache controller, and a multipurpose memory, wherein the multipurpose memory has a first operating mode for dynamically storing as a cache memory portions of a program obtained from a first external memory device for execution by the microprocessor under control of the cache controller, and the multipurpose memory has a second operating mode for storing an entire program obtained from a second external memory device to be run by the microprocessor. A system designer can choose whether to configure the system using the integrated circuit coupled with the first external memory device, or the integrated circuit coupled with the second external memory device. Beneficially, this allows for an architecture for an integrated circuit die that may be utilized with large, complex systems using external memory or with small, low-cost systems.

103. AMD products use a multipurpose memory. AMD’s Radeon processors, for example, contain a multipurpose memory, such as the high bandwidth cache. This has resulted in, among other things, AMD’s ability to provide an architecture for an integrated circuit die that may be utilized with large, complex systems using external memory or with small, low-cost systems.

104. AMD has directly infringed, and continues to directly infringe, one or more claims of the ’807 patent under 35 U.S.C. § 271(a), either literally and/or under the doctrine of equivalents, by, among other things, making, using, selling, offering to sell, and/or importing in or into the United States without authorization products covered by one or more claims of the ’807 patent, including, but not limited to, products with a high bandwidth cache, such as the Radeon Pro SSG semiconductor

device and other products in the Radeon Pro, Radeon RX, Radeon Instinct, and the Vega10 product family; other AMD semiconductor devices, integrated circuits, and products with the Vega10 architecture and/or a high bandwidth cache; and all other semiconductor devices, integrated circuits, and products with a similar multipurpose memory architecture ("the Accused '807 Products").

105. As one non-limiting example, AMD infringes claim 1 of the '807 patent. For example, the Radeon Pro SSG semiconductor device contains an integrated circuit device comprising:

a. a microprocessor (e.g., processor of the Radeon Pro SSG);

b. a multipurpose memory (e.g., high bandwidth cache of the Radeon Pro SSG) coupled with the microprocessor;

c. a cache controller (e.g., high bandwidth cache controller of the Radeon Pro SSG);

d. a first memory port (e.g., PCIe port of the Radeon Pro SSG) for coupling a first external memory device (e.g., system memory of the Radeon Pro SSG) with said cache controller; and

e. a second memory port (e.g., PCIe port of the Radeon Pro SSG) for coupling a second external memory device (e.g., NVME memory and/or Pro SSG storage of the Radeon Pro SSG) with said multipurpose memory;

f. wherein the multipurpose memory has a first operating mode (e.g., first cache mode of the Radeon Pro SSG) for dynamically storing as a cache memory portions of a program obtained from the first external memory device for execution by the microprocessor under control of the cache controller, and the multipurpose memory has a second operating mode (e.g., second cache mode of the Radeon Pro SSG) for storing an entire program obtained from the second external memory device to be run by the microprocessor.

106. Claim 1 of the ’807 patent applies to each Accused ’807 Product at least because each of those products contain infringing high bandwidth cache; and/or contain similar infringing features.

107. Monterey has complied with the requirements of 35 U.S.C. § 287(a) at least because Monterey provided AMD with written notice of its infringement as discussed above.

108. AMD was on notice of the ’807 patent under 35 U.S.C. § 287(a) at least as early as September 24, 2018.

109. AMD, knowing its products infringe the ’807 patent and with the specific intent for others to infringe the ’807 patent, has induced infringement of, and continues to induce infringement of, one or more claims of the ’807 patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, by, among other things, actively inducing others, including its customers, to make, use, sell, offer to sell, and/or import (including import products made by a patented process) in or into the United States without authorization the Accused ’807 Products, as well as products containing the same. AMD knowingly and intentionally instructs its customers, OEMs, foundry suppliers, distributors, and/or other third parties to infringe at least through user manuals, product documentation, and other materials, such as those located on AMD’s website at www.amd.com/en. For example, AMD provides data sheets, programmer references, design guides, revision guides, diagrams, white papers, and software instructing customers on uses of AMD’s products that infringe the ’807 patent. *See, e.g.*, https://www.amd.com/en/support/tech-docs and https://www.amd.com/en/support/professional-graphics/radeon-pro/radeon-pro-series/radeon-pro-ssg. Additional non-limiting examples include the materials found on AMD’s website at www.amd.com/en/products/professional-graphics/radeon-pro-ssg.

110. AMD has contributed to the infringement of, and continues to contribute to the infringement of, one or more claims of the ’807 patent under 35 U.S.C. § 271(c), either literally and/or

under the doctrine of equivalents, by, among other things, selling, offering to sell, and/or importing in or into the United States the Accused '807 Products, which constitute a material part of the invention of the '807 patent, knowing the Accused '807 Products to be especially made or especially adapted for use in an infringement of such patent, and not a staple article or commodity of commerce suitable for substantial noninfringing use. *See, e.g.*, https://www.amd.com/en/support/tech-docs and https://www.amd.com/en/support/professional-graphics/radeon-pro/radeon-pro-series/radeon-pro-ssg.

111. Monterey has sustained and is entitled to recover damages as a result of AMD's infringement.

112. AMD's infringement of the '807 patent has been knowing, deliberate, and willful, beginning at least as early as November 15, 2019, the date Monterey filed the first complaint in this action and therefore at least the date by which AMD knew of the '807 patent and knew that its conduct constituted and resulted in infringement of the '807 patent. AMD nonetheless has committed—and continues to commit—acts of direct and indirect infringement despite knowing that its actions constituted infringement of the valid and enforceable '807 patent, despite a risk of infringement that was known or so obvious that it should have been known to AMD, and/or even though AMD otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. AMD's conduct in light of these circumstances is egregious. AMD's knowing, deliberate, and willful infringement of the '807 patent entitles Monterey to increased damages under 35 U.S.C. § 284 and to attorney fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

COUNT SIX
INFRINGEMENT OF THE '455 PATENT

113. Monterey incorporates by reference the preceding paragraphs as if fully set forth

herein.

114. Monterey is the assignee and lawful owner of all right, title, and interest in and to the ’455 patent.

115. The ’455 patent is valid and enforceable.

116. The ’455 patent is directed to output buffers, and particularly to single ended output buffers.

117. The ’455 patent explains that in an integrated circuit, output buffers are often used at output pins to transfer signals to the signal lines. The transmission of information across the signal lines can be subject to various problems such as impedance mismatch, signal reflection, or irregular output waveform. Typically, output buffers must meet specifications dictated by applications, such as maintaining a smooth and robust output waveform.

118. Prior to the ’455 patent, output buffers had limited flexibility in meeting variations arising from different applications. While the drive strength of an earlier output buffer could be increased by adding additional driver devices in parallel, doing so may only just have met a minimum output impedance necessary to reduce signal reflections on a transmission line driven by the buffer.

119. Another disadvantage of earlier output buffers was that they could be sensitive to operating conditions. While an earlier output buffer could be tuned to meet worst case load conditions, if an actual output transmission line was less than such worst case, it could be difficult to meet driving requirements, such as rise time and fall time—particularly across uncontrollable variations in manufacturing process, differing operating voltages, and/or temperatures.

120. The ’455 patent teaches, among other things, an output driver comprising a first driver transistor, a first switch element coupled between a first driver control node and a first power supply node, and a selectable current source coupled between the first driver control node and a second

power supply node, wherein the selectable current source includes a plurality of selectable current legs. This solution describes output driver circuits that can, among other things, vary drive strength according to supply voltage conditions and/or provide programmable drive strength. As a result, the output buffer can, among other things, meet performance requirements over a range of operating voltages. Further, programmability of drive strength can also, among other things, enable the output buffer to be configured to provide a desired signal profile despite variations in transmission line load.

121. As an additional exemplary feature, an output buffer can include output driver transistors that can be enabled in response to current sources sinking or sourcing a current that can vary according to supply voltage and/or are programmable. Beneficially, among other things, this allows drive strength of such devices can be varied without increasing or decreasing the number of driver devices.

122. AMD products use an output driver. AMD's Ryzen processors, for example, contain an output driver circuit, such as the output driver and/or pre-driver in the DDR IO circuitry. This has resulted in, among other things, AMD's ability to provide a desired signal profile despite variations in transmission line load.

123. AMD has directly infringed, and continues to directly infringe, one or more claims of the '455 patent under 35 U.S.C. § 271(a), either literally and/or under the doctrine of equivalents, by, among other things, making, using, selling, offering to sell, and/or importing in or into the United States without authorization products covered by one or more claims of the '455 patent, including, but not limited to, products with an output driver and/or pre-driver in the DDR IO circuitry, such as the Ryzen 7 1700 semiconductor device and other products in the Ryzen product family; other AMD semiconductor devices, integrated circuits, and products with an output driver and/or pre-driver; and all other semiconductor devices, integrated circuits, and products with similar infringing technology

("the Accused '455 Products").

124. As one non-limiting example, AMD infringes claim 7 of the '455 patent. For example, the Ryzen 7 semiconductor device contains an output driver circuit comprising:

a. a first driver transistor that provides a low impedance path to an output node (e.g., output of the output driver and/or pre-driver of the Ryzen 7) in response to a voltage at a first driver control node (e.g., gate of a transistor of the Ryzen 7);

b. a first switch element (e.g., transistor switch of the Ryzen 7) coupled between the first driver control node and a first power supply node (e.g., first power supply of the Ryzen 7); and

c. a selectable current source (e.g., selectable transistor current source of the Ryzen 7) coupled between the first driver control node and a second power supply node (e.g., second power supply of the Ryzen 7), the selectable current source generating a drive current that varies in response to a drive select value,

d. wherein the selectable current source includes a plurality of selectable current legs (e.g., transistor current legs of the Ryzen 7), each connected to a current control node and enabled to provide a current to the current control node in response to a corresponding drive control signal (e.g., control signal of the Ryzen 7).

125. Claim 7 of the '455 patent applies to each Accused '455 Product at least because each of those products contain infringing output drivers and/or pre-drivers; and/or contain circuits with similar infringing functionality.

126. Monterey has complied with the requirements of 35 U.S.C. § 287(a) at least because Monterey provided AMD with written notice of its infringement as discussed above.

127. AMD was on notice of the '455 patent under 35 U.S.C. § 287(a) at least as early as

September 24, 2018.

128. AMD, knowing its products infringe the ’455 patent and with the specific intent for others to infringe the ’455 patent, has induced infringement of, and continues to induce infringement of, one or more claims of the ’455 patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, by, among other things, actively inducing others, including its customers, to make, use, sell, offer to sell, and/or import (including import products made by a patented process) in or into the United States without authorization the Accused ’455 Products, as well as products containing the same. AMD knowingly and intentionally instructs its customers, OEMs, foundry suppliers, distributors, and/or other third parties to infringe at least through user manuals, product documentation, and other materials, such as those located on AMD’s website at www.amd.com/en. For example, AMD provides data sheets, programmer references, design guides, revision guides, diagrams, white papers, and software instructing customers on uses of AMD’s products that infringe the ’455 patent. *See, e.g.*, https://www.amd.com/en/support/tech-docs: https://www.amd.com/system/files/TechDocs/AMD%20Ryzen%20Processor%20and%20AMD%20Ryzen%20Master%20Overclocking%20Users%20Guide.pdf. Additional non-limiting examples include the materials found on AMD’s websites at www.amd.com/en/ryzen-7 and www.amd.com/en/products/cpu/amd-ryzen-7-1700.

129. AMD has contributed to the infringement of, and continues to contribute to the infringement of, one or more claims of the ’455 patent under 35 U.S.C. § 271(c), either literally and/or under the doctrine of equivalents, by, among other things, selling, offering to sell, and/or importing in or into the United States the Accused ’455 Products, which constitute a material part of the invention of the ’455 patent, knowing the Accused ’455 Products to be especially made or especially adapted for use in an infringement of such patent, and not a staple article or commodity of commerce

suitable for substantial noninfringing use. *See, e.g.*, https://www.amd.com/en/support/tech-docs: https://www.amd.com/system/files/TechDocs/AMD%20Ryzen%20Processor%20and%20AMD%20Ryzen%20Master%20Overclocking%20Users%20Guide.pdf.

130. Monterey has sustained and is entitled to recover damages as a result of AMD's infringement.

131. AMD's infringement of the '455 patent has been knowing, deliberate, and willful, beginning at least as early as November 15, 2019, the date Monterey filed the first complaint in this action and therefore at least the date by which AMD knew of the '455 patent and knew that its conduct constituted and resulted in infringement of the '455 patent. AMD nonetheless has committed—and continues to commit—acts of direct and indirect infringement despite knowing that its actions constituted infringement of the valid and enforceable '455 patent, despite a risk of infringement that was known or so obvious that it should have been known to AMD, and/or even though AMD otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. AMD's conduct in light of these circumstances is egregious. AMD's knowing, deliberate, and willful infringement of the '455 patent entitles Monterey to increased damages under 35 U.S.C. § 284 and to attorney fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

RELIEF REQUESTED

Wherefore, Monterey respectfully requests that this Court enter judgment against AMD as follows:

A. that AMD has infringed each of the Patents-in-Suit;

B. that AMD's infringement of each of the Patents-in-Suit is and has been willful;

C. that Monterey be awarded damages adequate to compensate it for the patent infringement that has occurred, together with pre-judgment interest, post-judgment interest, and costs;

D. that Monterey be awarded an accounting and additional damages for any infringing sales not presented at trial;

E. that Monterey be awarded all other damages permitted by 35 U.S.C. § 284, including without limitation increased damages up to three times the amount of compensatory damages found;

F. that this is an exceptional case and that Monterey be awarded its costs and reasonable attorneys' fees incurred in this action as provided by 35 U.S.C. § 285;

G. that AMD as well as its officers, directors, agents, employees, representatives, attorneys, and all others acting in privity or in concert with them, its subsidiaries, divisions, successors and assigns be permanently enjoined from further infringement of each of the Patents-in-Suit;

H. that, in the event a permanent injunction preventing further infringement of each of the Patents-in-Suit is not granted, Monterey be awarded a compulsory ongoing licensing fee for any such further infringement; and

I. such other relief as this Court deems just and proper.

DEMAND FOR JURY TRIAL

Monterey hereby demands trial by jury on all claims and issues so triable.

Respectfully submitted,

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Dated: February 5, 2020

EXHIBIT A

US006534805B1

(12) **United States Patent**
Jin

(10) **Patent No.: US 6,534,805 B1**
(45) **Date of Patent: Mar. 18, 2003**

(54) **SRAM CELL DESIGN**

(75) Inventor: **Bo Jin**, Campbell, CA (US)

(73) Assignee: **Cypress Semiconductor Corp.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/829,510**

(22) Filed: **Apr. 9, 2001**

(51) **Int. Cl.**[7] **H01L 27/10**; H01L 21/84

(52) **U.S. Cl.** **257/206**; 257/211; 257/369; 438/153

(58) **Field of Search** 257/204, 206, 257/211, 369, 390, 393; 438/152, 153, 238

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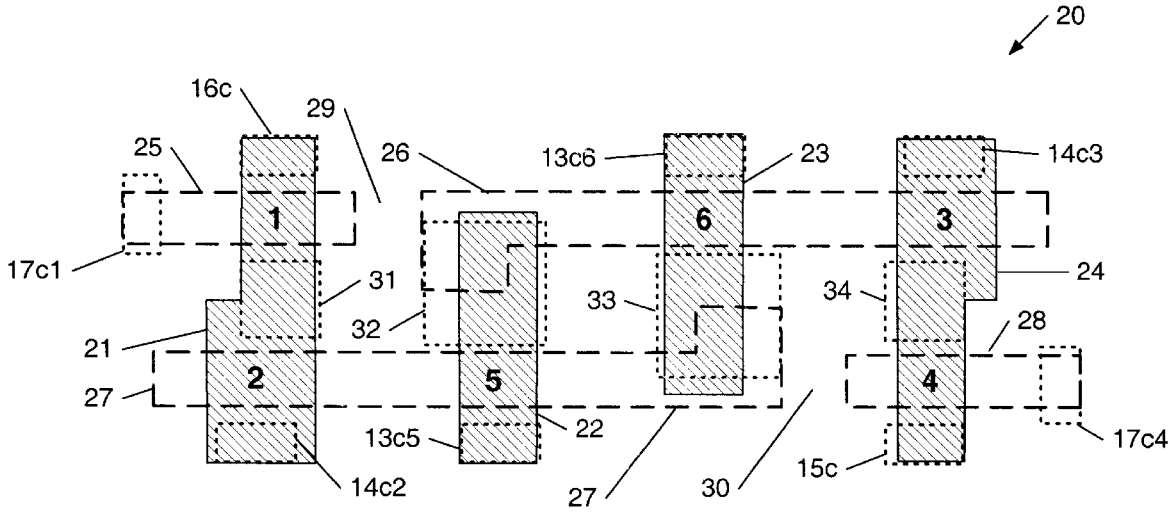
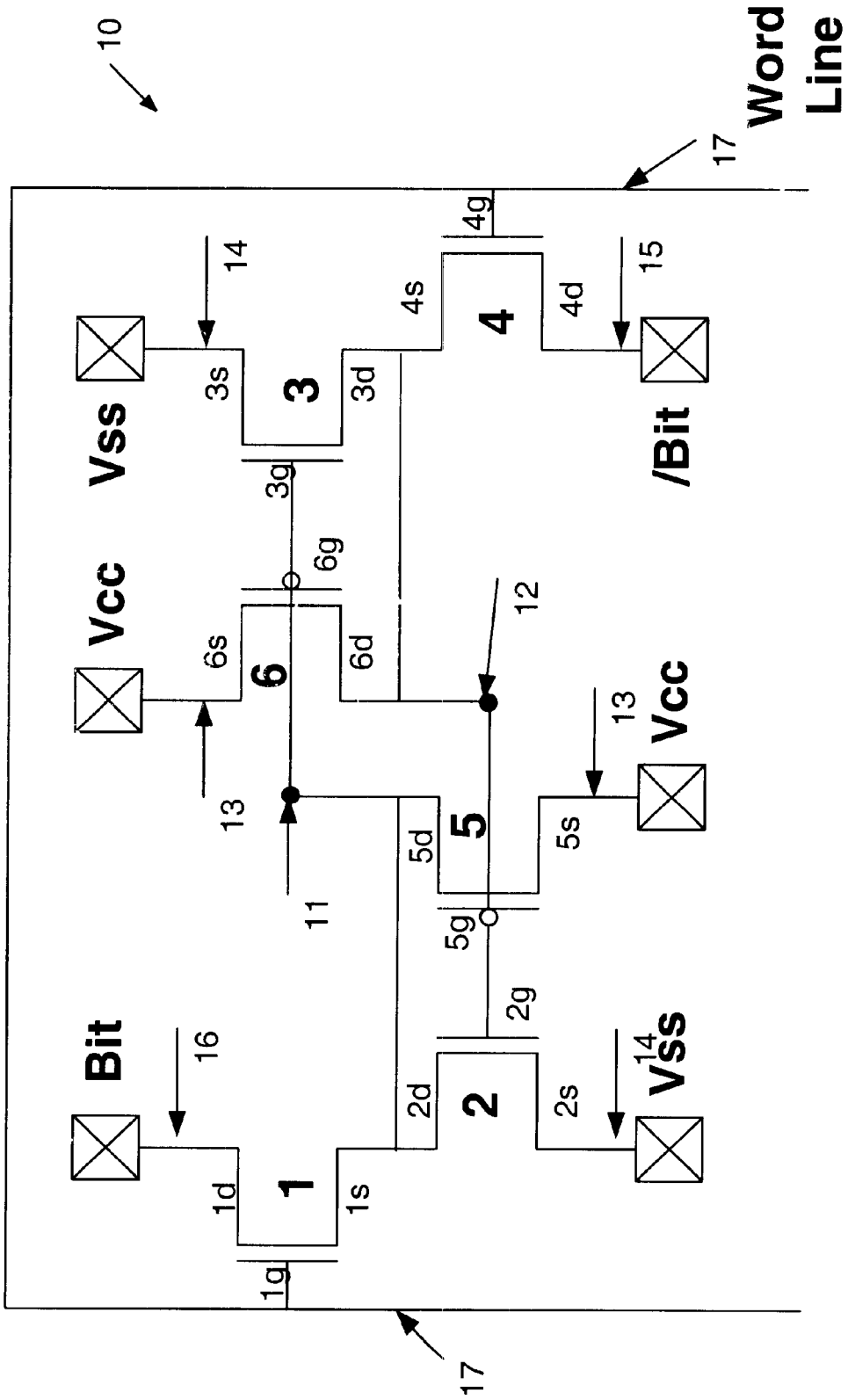
Primary Examiner—Mary Wilczewski
Assistant Examiner—Toniae M. Thomas
(74) *Attorney, Agent, or Firm*—Kevin L. Daffer; Conley, Rose & Tayon P.C.

(57) **ABSTRACT**

An embodiment of a memory cell includes a series of four substantially oblong parallel active regions, arranged side-by-side such that the inner active regions of the series include source/drain regions for p-channel transistors, and the outer active regions include source/drain regions for n-channel transistors. Another embodiment of the memory cell includes six transistors having gates substantially parallel to one another, where three of the gates are arranged along a first axis and the other three gates are arranged along a second axis parallel to the first axis. In another embodiment, the memory cell may include substantially oblong active regions arranged substantially in parallel with one another, with substantially oblong local interconnects arranged above and substantially perpendicular to the active regions. A method for fabricating a memory cell may include forming substantially oblong active regions within a semiconductor substrate, and forming substantially oblong local interconnects above and perpendicular to the active regions.

10 Claims, 3 Drawing Sheets

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6s
6
6d
13
Vcc
13
5d
5
5s
11
5g
2g
Bit
16
14
Vss
2d
2
2s
1d
1
1s
1g
17

FIG. 1

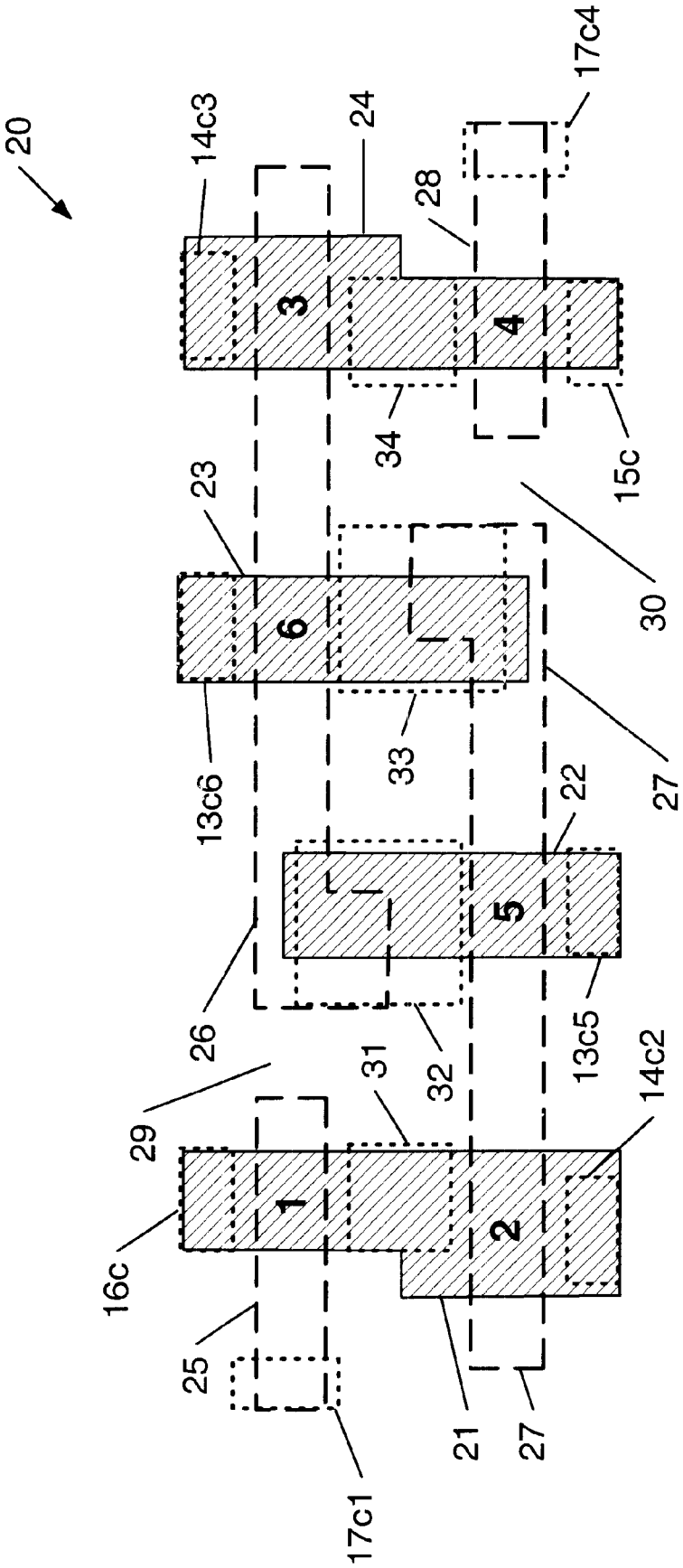
20
14c3
24
17c4
28
3
4
34
15c
23
30
6
13c6
33
27
22
5
26
13c5
32
31
14c2
29
1
2
16c
25
21
27
17c1

FIG. 2

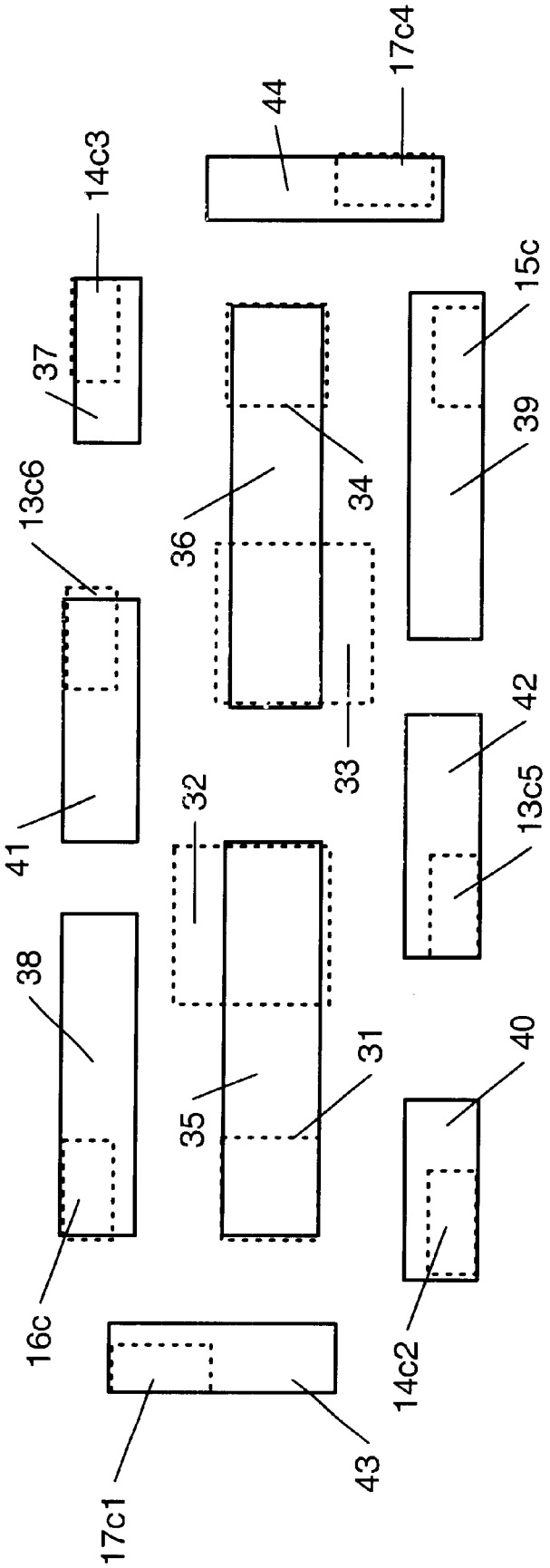
17c4
44
14c3
37
15c
39
34
36
13c6
33
42
13c5
32
41
38
31
35
40
16c
14c2
43
17c1

FIG. 3

SRAM CELL DESIGN

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to semiconductor memory device fabrication, and more particularly to an improved Static Random Access Memory (SRAM) cell design and method of manufacture.

2. Description of the Related Art

The proliferation of computers and other microprocessor-based devices has contributed to an increasing demand for semiconductor memory. Microprocessors are present not only in computers, but in a diverse range of products including automobiles, cellular telephones and kitchen appliances. A conventional microprocessor executes a sequence of instructions and processes information. Frequently, both the instructions and the information reside in semiconductor memory. Therefore, an increased requirement for memory has accompanied the microprocessor boom.

There are various types of semiconductor memory, including Read Only Memory (ROM) and Random Access Memory (RAM). ROM is typically used where instructions or data must not be modified, while RAM is used to store instructions or data which must not only be read, but modified. ROM is a form of non-volatile storage—i.e., the information stored in ROM persists even after power is removed from the memory. On the other hand, RAM storage is generally volatile, and must remain powered-up in order to preserve its contents.

A conventional semiconductor memory device stores information digitally, in the form of bits (i.e., binary digits). The memory is typically organized as a matrix of memory cells, each of which is capable of storing one bit. The cells of the memory matrix are accessed by wordlines and bitlines. Wordlines are typically associated with the rows of the memory matrix, and bitlines with the columns. Raising a wordline activates a given row; the bitlines are then used to read from or write to the corresponding cells in the currently active row. Memory cells are typically capable of assuming one of two voltage states (commonly described as "on" or "off"). Information is stored in the memory by setting each cell in the appropriate logic state. For example, to store a bit having the value 1 in a particular cell, one would set the state of that cell to "on;" similarly, a 0 would be stored by setting the cell to the "off" state. (Obviously, the association of "on" with 1 and "off" with 0 is arbitrary, and could be reversed.)

The two major types of semiconductor RAM, Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM), differ in the manner by which their cells represent the state of a bit. In an SRAM, each memory cell includes transistor-based circuitry that implements a bistable latch. A bistable latch relies on transistor gain and positive (i.e. reinforcing) feedback to guarantee that it can only assume one of two states—"on" or "off." The latch is stable in either state (hence, the term "bistable"). It can be induced to change from one state to the other only through the application of an external stimulus; left undisturbed, it will remain in its original state indefinitely. This is just the sort of operation required for a memory circuit, since once a bit value has been written to the memory cell, it will be retained until it is deliberately changed.

In contrast to the SRAM, the memory cells of a DRAM employ a capacitor to store the "on"/"off" voltage state

representing the bit. A transistor-based buffer drives the capacitor. The buffer quickly charges or discharges the capacitor to change the state of the memory cell, and is then disconnected. Ideally, the capacitor then holds the charge placed on it by the buffer and retains the stored voltage level.

DRAMs have at least two drawbacks compared to SRAMs. The first of these is that leakage currents within the semiconductor memory are unavoidable, and act to limit the length of time the memory cell capacitors can hold their charge. Consequently, DRAMs typically require a periodic refresh cycle to restore sagging capacitor voltage levels. Otherwise, the capacitive memory cells would not maintain their contents. Secondly, changing the state of a DRAM memory cell requires charging or discharging the cell capacitor. The time required to do this depends on the amount of current the transistor-based buffer can source or sink, but generally cannot be done as quickly as a bistable latch can change state. Therefore, DRAMs are typically slower than SRAMs. DRAMs offset these disadvantages by offering higher memory cell densities, since the capacitive memory cells are intrinsically smaller than the transistor-based cells of an SRAM.

As microprocessors have become more sophisticated, greater capacity and speed are demanded from the associated memory. SRAMs are widely used in applications where speed is of primary importance, such as cache memory supporting the Central Processing Unit (CPU) in a personal computer. Like most semiconductor devices, SRAMs are fabricated en masse on semiconductor wafers.

Fabrication of a metal-oxide-semiconductor (MOS) integrated circuit involves numerous processing steps. A gate dielectric, typically formed from silicon dioxide ("oxide"), is formed on a semiconductor substrate which is doped with either n-type or p-type impurities. Conductive regions and layers of the device may be isolated from one another by an interlevel dielectric. For each MOS field effect transistor (MOSFET) being formed, a gate conductor is formed over the gate dielectric, and dopant impurities are introduced into the substrate to form a source and drain. Frequently, the integrated circuit will employ a conducting layer to provide a local interconnect function as well. A pervasive trend in modern integrated circuit manufacture is to produce transistors that are as fast as possible and thus have feature sizes as small as possible. Many modern day processes employ features, such as gate conductors and interconnects, which have less than 1.0 μm critical dimension. As feature size decreases, the sizes of the resulting transistor and the interconnect between transistors also decrease. Fabrication of smaller transistors allows more transistors to be placed on a single monolithic substrate, thereby allowing relatively large circuit systems to be incorporated on a single, relatively small die area.

However, integrated circuits become increasingly difficult to manufacture as their dimensions are reduced. Integrated circuits with complex geometries may be particularly difficult to manufacture as dimensions are reduced. Consequently, integrated circuit designs without complex geometries are preferable. Further, reducing the number of steps in an integrated circuit's manufacturing process flow is desired. Reducing the number of processing steps often results in higher profits. Clearly, it would be desirable to have an improved circuit design and method of manufacture to facilitate fabrication of smaller and faster SRAMS.

SUMMARY OF THE INVENTION

The problems outlined above may be addressed by an improved circuit design and method of fabrication disclosed

herein for an integrated circuit, specifically a semiconductor memory device. In the embodiments considered herein, the semiconductor memory device is a static random access memory (SRAM) device, but it is believed that principles disclosed herein are applicable to other types of integrated circuits as well. For example, any device requiring local interconnection of multiple active regions and gates may be suitable.

A memory cell is disclosed herein including a series of four substantially oblong parallel active regions. The active regions are arranged such that the inner active regions comprise source/drain regions for p-channel transistors, while the outer active regions comprise source/drain regions for n-channel transistors. Substantially oblong polysilicon structures may be arranged above and substantially perpendicular to the active regions. Substantially oblong local interconnects may also be arranged above and substantially perpendicular to the active regions. Each active region may include source/drain regions for no more than two transistors. Source/drain contacts to the source/drain regions of the transistors may include at least one shared contact, such that the shared contact is connected to a polysilicon structure as well as an inner source/drain region. A shared contact may be connected to a source/drain contact using a local interconnect. In an embodiment, the local interconnect is dielectrically spaced above the substrate. In an alternate embodiment, the local interconnect may have an upper surface substantially commensurate with the upper surface of at least one respective contact.

A memory cell including six transistors with gates that are substantially parallel to one another is also disclosed. Three of the gates are arranged along a first axis, and the other three are arranged along a second axis parallel to the first axis. Two of the gates along an axis may be arranged within a single polysilicon structure. Of these two, one may be a gate for a p-channel transistor and the other may be a gate for an n-channel transistor. The third gate along an axis may be arranged within another polysilicon structure. This second polysilicon structure may be electrically coupled to a respective local wordline. Each of the two local wordlines may be electrically coupled to a global wordline, which in an embodiment comprises metal. Also included in the memory cell may be a shared contact arranged between the axes and in contact with a source/drain region of a p-channel transistor along one axis and a polysilicon structure along the other axis. In an embodiment, the memory cell may also include an active region substantially perpendicular to the axes and electrically coupled to a bitline where the bitline extends across the entire length of the memory cell. The bitline may be substantially parallel to the active region, and the length of the bitline may be less than a third of the width of the cell.

In an embodiment, a memory cell is disclosed having substantially oblong active regions arranged substantially in parallel with one another within a semiconductor substrate. The memory cell also has multiple local interconnects arranged above and substantially perpendicular to the active regions, where the interconnects are also substantially oblong and in parallel with one another. In an embodiment, the memory cell may also include substantially square local interconnects such that all interconnects are either substantially oblong or substantially square. In an embodiment, the memory cell may also include a shared contact that is electrically coupled to an active region and a polysilicon structure abutting said active region.

Also disclosed herein is a method of fabricating a memory cell including forming substantially oblong active regions arranged substantially in parallel with one another within a semiconductor substrate. The method also includes forming substantially oblong local interconnects arranged above the semiconductor substrate where the interconnects are substantially in parallel with one another and substantially perpendicular to the active regions. In an embodiment, forming the local interconnects may include etching a trench through a dielectric material and depositing a conductive material into the trench. The method may include forming substantially oblong polysilicon structures arranged above the semiconductor substrate where the polysilicon structures are substantially in parallel with one another and substantially perpendicular to the active regions. Forming the polysilicon structures may include forming an access polysilicon structure for each of two access transistor gates within the memory cell, where the access polysilicon structures do not extend across the entire memory cell. In an embodiment, forming the memory cell may include forming a global wordline, where the wordline is dielectrically spaced above the active regions and where the wordline is electrically coupled to the access polysilicon structures.

The improved circuit design and method of fabrication disclosed herein may provide numerous advantages. This circuit design may be improved because the memory cell layout may allow the features to be arranged in such a way as to minimize cell size. Another advantage of the improved circuit design is the substantially parallel features that reduce manufacturing complexities, particularly in photolithography. As a result of the substantially parallel layout, reducing feature sizes to increase device speeds and/or to minimize memory cell size may be facilitated. In addition, the substantially parallel layout may change the aspect ratio of the memory cell such that the bitlines may be reduced in length, thus advantageously decreasing bitline resistivity and increasing memory cell performance. Furthermore, this circuit design may be improved because of the symmetrical the layout design, which may improve noise margins. Yet another advantage of the improved circuit design is the elimination of polysilicon wordlines that traverse the entirety of the memory cell. Elimination of such polysilicon wordlines may minimize cell size by reducing the density of features required on the polysilicon layer of the cell. Reducing the amount of polysilicon in the wordlines may also result in increased use of a metal layer to perform the wordline function, thus advantageously decreasing wordline resistivity and increasing memory cell performance. A further advantage of the improved circuit design is that the improved polysilicon layer may partially perform local interconnecting functions. Therefore, the subsequent local interconnect layer may be greatly simplified and the local interconnects may also be arranged substantially in parallel. The improved layout may further enable the use of a trench local interconnect layer, thus reducing the number of processing steps.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the accompanying drawings in which:

FIG. **1** shows the transistor configuration of an embodiment of an improved SRAM memory cell;

FIG. **2** represents a layout of the active regions and polysilicon structures for the embodiment of FIG. **1**; and

FIG. **3** represents a layout of the local interconnect for the regions and structures shown in FIG. **2**.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the appended claims.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

A circuit diagram for an improved double wordline SRAM memory cell is shown in FIG. **1**. Generally stated, SRAM memory cells may be formed by interconnecting two CMOS inverters together so that the input of a first inverter is tied to the output of a second inverter and vice versa to form a positive feedback orientation. Such configuration of two inverters is commonly referred to as a bi-stable latch as described above. The inverters include transistors commonly referred to as latch transistors. In the embodiment of FIG. **1**, transistors **2** and **5** form the first inverter, transistors **3** and **6** form the second inverter, the node representing the input of the first inverter is labeled **12**, and the node representing the input of the second inverter is labeled **11**. Thus, the memory cell **10** comprises four latch transistors **2**, **3**, **5**, and **6** and two access transistors **1** and **4**, each of which has a drain, source and gate. The latch transistors **2**, **3**, **5**, and **6** include a pair of n-channel pull-down transistors **2** and **3** and a pair of p-channel load transistors **5** and **6**.

The inverters are connected as follows to form the bi-stable latch of FIG. **1**. A drain **2***d* of pull-down transistor **2** is coupled to a drain **5***d* of load transistor **5** at node **11** and a drain **3***d* of a pull-down transistor **3** is coupled to a drain **6***d* of load transistor **6** at node **12**. These nodes **11** and **12** store opposite logic states (i.e., one is a logic "1" while the other is a logic "0"). Sources **5**s and **6**s of transistors **5** and **6** are coupled to a common power line **13** (hereinafter referred to as a "Vcc line") while sources **2***s* and **3***s* of pull-down transistors **2** and **3** are coupled to a common ground line **14** (hereinafter referred to as a "Vss line"). Gates **2***g* and **5***g* of transistors **2** and **5** are coupled together and connected to the node **12** and gates **3***g* and **6***g* of transistors **3** and **6** are coupled together and connected to node **11**.

Such interconnections create positive feedback, which allows the memory cell to store data as either a "high" or "low" input (i.e., a logic "1" or "0"). Data is stored in these memory cells during a "write cycle" and that data is subsequently read during a "read" cycle. The n-channel access transistors **1** and **4** are coupled to the memory cell **10** to allow communication between the cell **10** and an external device through a pair of complementary bitlines **15** and **16**. With respect to the access transistors **1** and **4**, each source **1***s* and **4***s* is coupled to nodes **11** and **12**, respectively. A drain **1***d* of access transistor **1** is coupled to a bitline **16**, referred to as "Bit," which operates as a data line to read data from and write data into the memory cell **10**. A drain **4***d* of a second access transistor **4** is similarly coupled to a complementary bitline **15** called "/Bit," In addition, both gates **1***g* and **4***g* are coupled to wordline **17**.

Applying a positive voltage to the wordline **17** turns on both access transistors **1** and **4**, thus accessing memory cell **10**. This allows one of the two bitlines **15** and **16** to sense the contents of the memory cell **10** based on the voltage at either node **11** or **12**. For example, if node **11** is at a high (Vcc) voltage and node **12** is at the ground potential (Vss), when the wordline **17** is brought to a high voltage, the pull-down transistor **3** and the access transistor **4** are both turned on and will thus pull the bitline "/Bit" **15** down toward the ground potential Vss. Moreover, the load transistor **5** and the access transistor **1** are also tuned on; thus the bitline "Bit" **16** will be pulled up towards the Vcc potential. Thus the state of the cell **10** (either "1" or "0") can be determined by sensing the difference in potential between the bitlines **15** and **16**.

Conversely, writing a "1" or a "0" into the cell **10** can be accomplished by forcing the bitline **15** or the bitline **16** to either Vcc or Vss and then raising the wordline **17**. The potential placed on either the bitline "/Bit" **15** or the bitline "Bit" **16** will then be transferred to the node **11** or **12**, respectively, forcing the cell **10** into either a corresponding "**1**" state or a "**0**" state.

Shown in FIG. **2** is an embodiment of a layout **20** that may be used to form in silicon the memory cell **10** represented in FIG. **1**. (Elements appearing in more than one figure retain the same item numbers throughout the figures.) FIG. **2** presents a top-down view of an exemplary memory cell layout **20**. Layout **20** illustrates the active regions, isolation regions, polysilicon structures, and contact structures that may be used to form the typical metal oxide semiconductor (MOS) transistors, NMOS and PMOS, used in a typical CMOS SRAM. In the embodiment of FIG. **2**, NMOS transistors **1**–**4** are formed within active regions **21** and **24**, and PMOS transistors **5** and **6** are formed within active regions **22** and **23**. The active regions are formed within a semiconductor substrate. The semiconductor substrate may preferably be a silicon substrate doped n-type and p-type in the vicinity of the p-channel transistors and the n-channel transistors, respectively. More specifically, the semiconductor substrate may include n-type and p-type well regions formed in a monocrystalline silicon substrate, or in an epitaxial silicon layer grown on a monocrystalline silicon substrate.

Active regions, i.e., areas where active transistors are to be formed, are labeled **21**–**24** and are arranged side-by-side and substantially parallel to each other. Diffusion regions are also to be formed within the active regions **21**–**24**. For example, diffusion regions may be lightly doped drain regions and heavily doped source/drain regions formed in active regions adjacent to the transistor gate structures. Dielectric isolation regions such as **29** and **30** separate active regions from one another. Isolation regions may be formed by a number of techniques such as shallow trench isolation (STI), recessed oxide isolation (ROI), or local oxidation of silicon (LOCOS). Isolation regions may therefore be field oxide regions, which serve to isolate separate active regions on the semiconductor layer from one another.

In the embodiment of FIG. **2**, NMOS active regions **21** and **24** are utilized for the formation of two transistors each, a pass transistor and a latch transistor. Polysilicon structures **25** and **27** are arranged above active region **21** to form gates of pass transistor **1** and latch transistor **2**, respectively. Similarly, above active region **24**, polysilicon structures **28** and **26** are arranged to form gates of pass transistor **4** and latch transistor **3**, respectively. Consequently, active regions **21** and **24** each have two gate conductors arranged above them. In this embodiment, no active region has more than two gate conductors arranged above it, and therefore no active region forms more than two transistors.

In the embodiment of FIG. **2**, the active regions are substantially oblong, and in some cases may be substantially rectangular as well. For example, PMOS active regions,

such as active regions **22** or **23** shown in FIG. **2**, may have a length that is substantially constant across the width of the region, as well as a width that is substantially constant along the length of the region. However, if an NMOS active region is forming an access transistor and a latch transistor, it may have some variation in width although the length may be substantially constant across the width of the region. For example, active regions **21** and **24** as shown in FIG. **2** are each forming access transistors **1** and **4**, respectively, and latch transistors **2** and **3**, respectively. By design, access transistors frequently have widths that are smaller than those of adjacent latch transistors. The active region is thus designed to ensure the stability of the SRAM. This design feature is commonly referred to as the "beta ratio." A beta ratio is defined as the width of the latch transistor divided by the width of the pass transistor. To ensure circuit stability, the beta ratio should be >1. In an embodiment, the beta ratio is approximately 1.5. Therefore, in an embodiment, the width of the access transistor is approximately ⅔ the width of the latch transistor. Consequently, an NMOS active region may be considered to be substantially oblong if the length of the region is substantially constant and if the width of the region varies by approximately ⅓ or less along the length of the region. Further, an NMOS active region may be considered to be substantially oblong if the length of the region is substantially constant and the width of the region by design varies only with the respective widths of the access and latch transistors. In an embodiment, "substantially oblong" may refer to any region or structure having a length that is greater than or equal to approximately three times its maximum width. Active regions as described above are oblong with respect to, for example, the markedly "L-shaped" regions formed in layouts for which two transistors are arranged at right angles to each other.

Each transistor includes a gate electrode formed above an active region, arranged between a pair of source/drain regions, and separated from the substrate by a relatively thin dielectric. In a preferred embodiment, gate electrodes are arranged within polysilicon structures **25–28** to form transistors **1–6** as shown in FIG. **2**. The polysilicon may be deposited by, for example, using chemical vapor deposition (CVD) of silicon from a silane source. However, the gate electrodes may comprise any suitable conductive material such as polysilicon, aluminum, or copper. Therefore structures **25–28** are not limited to polysilicon. For example, the gate electrodes may include multiple layers of material, such as a doped polysilicon and a silicide. A silicide may be formed from a polysilicon layer upon which a layer of refractory metal such as cobalt or titanium has been formed. Upon heating the refractory metal, a reaction between the polysilicon and the cobalt or titanium may result in the formation of a silicide such as cobalt silicide or titanium silicide. In an embodiment, the width of the gate electrode (or channel length of the transistor) may be approximately 0.12 microns, but may also be larger or smaller depending on the transistor that is being formed.

Many SRAMs are single wordline cells, meaning that there is only one local wordline arranged within each cell. It therefore follows that a double wordline cell has two local wordlines arranged within each cell. The two local wordlines are coupled either within the cell or outside the cell. Frequently, single wordline cells and double wordline cells have some similarities. Both cells may have wordlines that are polysilicon and that extend continuously from one side of the cell to the other. However, the embodiment of FIG. **2** presents a split double wordline cell. That is, the local wordlines of the embodiment of FIG. **2** do not extend continuously from one side of the memory cell to the other. For example, polysilicon structures **25** and **28** each comprise local wordlines and each couples to global wordline **17** (not shown). However, neither polysilicon structure extends continuously from one side of the memory cell to the other. Thus, polysilicon structures **25** and **28** are coupled together and to global wordline **17** outside of cell layout **20**. Polysilicon structures **25** and **28** are coupled such that they rise and fall in potential together.

The split double wordline of the embodiment of FIG. **2** may allow the memory cell size to be reduced while also improving memory cell performance. Each wordline-coupled polysilicon structure **25** and **28** may be electrically coupled to a polysilicon structure arranged within an immediately adjacent cell. However, an entire row of memory cells would not be coupled together by one or two continuous polysilicon wordlines as is frequently found in SRAM circuits. For example, a continuous conductive wordline is frequently formed when the gate electrodes are formed. Because this type of continuous wordline is eliminated in the embodiment of FIG. **2**, the density of the features required by the polysilicon layer of the memory cell is reduced. Consequently, the die size required to accommodate the polysilicon layer may be reduced, and the layout of the remaining polysilicon features may be improved to provide a more manufacturable memory cell. Further, the performance of the memory cell may be improved, as memory cell addressing times may no longer be limited by the resistivity of continuous polysilicon wordlines. As noted above, split local wordline polysilicon structures **25** and **28** are each electrically coupled to the global wordline **17**. Except for those areas where global wordline **17** is electrically coupled to polysilicon structures **25** and **28**, global wordline **17** may be a metal dielectrically spaced from the polysilicon structures.

Conductive regions and layers of the memory cell may be isolated from one another by dielectrics. Examples of dielectrics may include silicon dioxide (SiO_2), tetraethylorthosilicate glass (TEOS), silicon nitride (Si_xN_y), silicon oxynitride ($SiO_xN_y(H_z)$), and silicon dioxide/silicon nitride/silicon dioxide (ONO). The dielectrics may be grown or may be deposited by physical deposition such as sputtering or by a variety of chemical deposition methods and chemistries such as chemical vapor deposition. Additionally, the dielectrics may be undoped or may be doped, for example with boron, phosphorus, boron and phosphorus, or fluorine, to form a doped dielectric layer such as borophosphosilicate glass (BPSG), phosphosilicate glass (PSG), and fluorinated silicate glass (FSG).

The coupling of global wordline **17** to the gates of access transistors **1** and **4** may require the use of contacts **17*c*1** and **17*c*4**, respectively, as shown in FIG. **2**. At various stages in the fabrication of semiconductor devices, it may be necessary to form openings in a dielectric layer to allow for contact to underlying regions or layers. Generally, an opening through a dielectric exposing a diffusion region or an opening through a dielectric layer between polysilicon and an interconnect or first metal layer is called a "contact opening" or a "contact hole." If the opening is substantially oblong, it may be referred to as a "trench." An opening in other dielectric layers such as an opening through an intermetal dielectric layer is commonly referred to as a "via." For purposes of this disclosure, henceforth "contact opening" may be used to refer to a contact opening and/or a via. Similarly, "trench" may be used to refer to any substantially oblong contact opening and/or via. A contact opening or trench may expose a diffusion region within the silicon

substrate such as a source or drain, or may expose some other layer or structure such as an underlying metallization layer, a local interconnect layer, or a gate structure. Conductive contact structures may be formed above the source/drain regions, and interconnects may overlie the contact structures and may connect neighboring contact structures. These contact structures to diffusion regions may be isolated from an adjacent gate structure by a dielectric spacer. The dielectric spacer may also isolate the gate from the diffusion region.

Contacts **17***c***1** and **17***c***4** could be used to electrically couple polysilicon structures **25** and **28**, respectively, to a dielectrically spaced global wordline **17**. Because global wordline **17** is dielectrically spaced, it may be metal. Metal global wordlines have significantly lower resistivity than the polysilicon global wordlines or the silicided global wordlines used in some memory cells. For example, the Rs of polysilicon is approximately 50 ohms/square and the Rs of silicide is approximately 20 ohms/square. However, metals have Rs values that are significantly smaller, for example, less than approximately 0.2 ohms/square. Consequently, metal global wordlines have significantly lower resistivities than polysilicon or silicide global wordlines. Therefore, metal global wordlines may be much longer than global wordlines of polysilicon or silicide, yet still have lower resistivities. As such, metal global wordlines may significantly reduce memory cell addressing times.

For example, in the embodiment of FIG. **2**, the cell aspect ratio is approximately 1:3.5. An aspect ratio as used herein generally describes the ratio between the height and width of a semiconductor feature. In the case of the cell aspect ratio, the ratio is taken between the height of the memory cell and the width of the memory cell. That is, the memory cell of the embodiment of FIG. **2** has a width (along the wordline direction) that is approximately 3.5 times its height (along the bitline direction). Further, the global wordline traversing the memory cell of the embodiment of FIG. **2** is longer than, for example, a global wordline of a memory cell with an equivalent area and an aspect ratio of 1:1. However, despite being longer, the metal global wordline of the cell of FIG. **2** would have a lower resistance than a polysilicon or silicide global wordline of a memory cell with a 1:1 aspect ratio due to the much lower metal Rs value. Further, the bitline traversing the memory cell of the embodiment of FIG. **2** would be shorter than the bitline of a cell with an equivalent area and an aspect ratio of 1:1. Consequently, the embodiment of FIG. **2** may provide significantly faster memory cell addressing times.

A double wordline may advantageously simplify cell layout by allowing all transistor gates to be arranged substantially parallel to one another. Such arrangement may eliminate active regions that are arranged one perpendicular to another and/or continuous active regions that have 90 degree "knees." Furthermore, double wordlines may also eliminate similar arrangement of the polysilicon structures. Thus, the double wordlines may facilitate the use of substantially oblong features for the active regions and the polysilicon structures. That is, the active regions may be arranged substantially parallel to one another, and the polysilicon structures may also be arranged substantially parallel to one another. Such arrangement may facilitate the future reduction of critical dimensions(CDs) for these layers since eliminating complicated geometries aids manufacturability for the photolithography process, as discussed above.

If active regions are arranged such that complex geometries are eliminated, it follows that the isolation regions are also arranged such that complex geometries are eliminated. Elimination of complex geometries may also reduce manufacturing complexities for other manufacturing processes. For example, a shallow trench isolation process ("STI") is more robust with the elimination of complex geometries. Shallow trench isolation is primarily used for isolating active regions, and is rapidly replacing local oxidation of silicon, or LOCOS, isolation structures. STI processes do not exhibit the lateral extension of oxide into the active region of the device, known as the "bird's beak", that is common with LOCOS processes. In contrast to a LOCOS process, the STI process involves patterning the semiconductor substrate, etching shallow trenches into the substrate, filling the trenches with dielectric, and removing the dielectric from the substrate so that the remaining dielectric has an upper surface approximately commensurate with the upper surface of the semiconductor substrate. That is, the STI process results in an essentially planar upper surface. Thus, STI processes further enable the reduction of CDs for polysilicon structures. For example, photolithography processes require substantially planar upper surfaces to pattern sub-micron features due to the very small depth of focus. Thus, STI processes may enable production of smaller, and therefore faster, transistors. However, the STI process is also more robust if the geometry is not complex. As geometries continue to shrink, the STI geometry also shrinks thus making the required patterning, etching, and dielectric fill more difficult. If the STI geometry is complex, the required processing may be much more difficult. Thus, simplified STI geometries are preferred.

Turning now to FIG. **2**, bitline "Bit" **16** is coupled to the drain of transistor **1** by contact **16***c*, while bitline "/Bit" **15** is coupled to the drain of transistor **4** by contact **15***c*. The sources of transistors **2** and **3** are coupled to Vss by contacts **14***c***2** and **14***c***3**, respectively, while the sources of transistors **5** and **6** are coupled to Vcc by contact **13***c***5** and **13***c***6**, respectively. Bitlines **15** and **16**, Vcc **13**, and Vss **14** are also dielectrically spaced from the polysilicon structures. The bitlines, Vss, and Vcc may be contacted to each memory cell using what is commonly referred to as the first metal layer. The "first metal layer" refers to the first conductive layer above the local interconnect layer, and may be a misnomer in those cases where the local interconnect layer utilizes a metal.

Contact regions **31**–**34** as shown in FIG. **2** may be used for the local interconnections of gates and drains as described in the discussion of FIG. **1** above. Many types of contacts may be used; e.g., self-aligned contacts (SAC) or shared contacts may be used. Further, contacts may be substantially rectangular or substantially square. For example, SAC may be substantially square. Contacts **31** and **34** represent openings in the dielectric that expose portions of active regions **21** and **24**, respectively. In particular, contact **31** allows for a contact to the source of transistor **1** and the drain of transistor **2** and contact **34** allows for contact to the source of transistor **4** and the drain of transistor **3**. Contacts **32** and **33** represent openings in the dielectric, which expose portions of active regions **22** and **23**, respectively, as well as exposing portions of polysilicon structures **26** and **27**, respectively. As such, contacts **32** and **33** are shared contacts. That is, contacts **32** and **33** allow for contact not only to diffusion regions, but also to polysilicon structures. For example, as shown in FIG. **2**, contact **32** allows for a contact to the drain of transistor **5**, but it also allows for a contact to the gates of transistors **3** and **6** via polysilicon structure **26**. Polysilicon structure **26** is connected to the gates of transistors **3** and **6** as discussed above, and contact **32** allows for a contact to polysilicon structure **26**. In particular, contact **32** allows for a contact to

a portion of polysilicon structure **26** which may be wider than the remainder of polysilicon structure **26**. Although polysilicon structure **26** has a wider portion, it is nonetheless considered to be substantially oblong. A polysilicon structure may be considered to be substantially oblong if the length of the polysilicon structure is greater than about three times the width of the polysilicon structure. Furthermore, a polysilicon structure may be considered to be substantially oblong despite having a substantially wider region if the wider region solely accommodates a contact region. Similarly, contact **33** is a shared contact which allows for contact to the drain of transistor **6** as well as polysilicon structure **27** and hence gates of transistors **2** and **5**. Consequently, shared contacts **32** and **33** reduce the number of contacts needed by the subsequent local interconnect. Shared contacts such as **32** and **33** may be substantially rectangular.

Local interconnections are generally used for short runs relative to much longer metal conductors used for global connections. Thus, the term "local interconnect" may refer to the function of connecting features within a circuit, or it may refer to a distinct process layer that exclusively performs such short connections. Therefore, a process layer may perform local interconnecting functions, yet not be termed a "local interconnect layer." That is, a polysilicon layer may partially provide local interconnect in addition to providing transistor gates. The polysilicon layer may be configured such that multiple gates are connected, thus forming a local interconnect.

For example, polysilicon structures **26** and **27** provide local interconnect because they each form multiple gates. Polysilicon structure **26** is arranged above active region **23** and active region **24** to form gates of PMOS latch transistor **6** and NMOS latch transistor **3**, respectively. Polysilicon structure **27** is arranged above active region **21** and active region **22** to form gates of NMOS latch transistor **2** and PMOS latch transistor **5**, respectively. Therefore, polysilicon structures **26** and **27** each include two gates. Thus, polysilicon structures **26** and **27** may each perform a local interconnecting function because they each connect two separate gate conductors together. As a result, the subsequent local interconnect layer of the embodiment of FIG. **2** may be simplified because polysilicon structures **26** and **27** are performing a local interconnecting function that is frequently provided by a local interconnect layer. As will be discussed in more detail below, the embodiment of FIG. **2** utilizes an improved, simplified local interconnect layer layout as a result of the local interconnecting function provided by polysilicon structures **26** and **27**.

FIG. **3** illustrates a local interconnect layer which may be used in conjunction with the layout shown in FIG. **2**. Contacts **31–34** may be formed through a dielectric material arranged above the topography of the features shown in FIG. **2**. The dielectric material is preferably deposited using physical vapor deposition (PVD), chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), low pressure chemical vapor deposition (LPCVD), or spin on deposition techniques. In the vapor depositions, a silane or TEOS source, for example, may be used to produce the dielectric. In the spin on depositions, a liquid material of, for example, silicon (i.e., silicates, siloxanes, or silsesquioxanes) or TEOS may be spin-on deposited and subsequently cured. The dielectric material preferably has a thickness of approximately 6000–8000 angstroms, but other thicknesses may be suitable depending on the particular process used. Contacts **31–34** are also shown in FIG. **2**. In the completed circuit, contacts **31** and **32** are connected to local interconnect region **35** which electrically connects the source of transistor **1** to the drains of transistors **2** and **5** and the gates of transistors **3** and **6** as shown in FIGS. **1** and **2**. Thus, local interconnect region **35** completes the connections necessary to form node **11** as illustrated in FIG. **1**. Similarly, local interconnect region **36** and contacts **33** and **34** will complete the connections necessary to form node **12** as illustrated in FIG. **1**. It can be seen from FIG. **3** that local interconnect structures **35** and **36** are substantially rectangular and require connection to the structures of the previous layers in only two areas. This is an improvement over local interconnect structures which require multi-limbed, non-oblong interconnect structures and three connections to the structures of previous layers. The local interconnect of the embodiment of FIG. **3** is simplified as a result of the interconnect provided by the polysilicon structures **26** and **27**.

In one embodiment of the local interconnect, the dielectric material is arranged upon the topography and planarized using, for example, chemical mechanical polishing, or "CMP." The dielectric is then etched to form contact openings **31–34**. Next, an adhesion or "glue" layer may be formed by blanket depositing an adhesion material onto the sidewalls and bottom of openings **31–34**. Suitable adhesion materials include titanium (Ti), titanium-tungsten (TiW), titanium nitride (TiN), or tungsten silicides (WSi_x). Adhesion layers may be used in those cases where conductive materials may adhere poorly to the dielectric material. Adhesion layers may be used, for example, to compensate for poor adhesion characteristics of tungsten and some tungsten alloys to silicon dioxide dielectric films. After an adhesion layer has been formed, a conductive material layer may then be deposited. In the case where tungsten, "W," is the conductive material deposited, this step is referred to as W plug. However, any suitable conducting material may be applied in a manner appropriate to the material. Next, the contact plugs are planarized such that they are substantially commensurate to an uppermost surface of the dielectric material. This planarization step may be accomplished via CMP. Next, an additional conducting layer is deposited. This conducting layer is commonly referred to as the local interconnect layer. The local interconnect layer may be made from a material having higher resistivity than the metals or conducting materials used for global interconnects. Suitable local interconnect materials may include polysilicon, doped polysilicon, refractory metal, silicide, or combinations of these. The local interconnect layer is subsequently patterned and etched, thus completing an embodiment of a local interconnect process flow.

In another local interconnect embodiment, the dielectric material is also arranged upon the topography and planarized. However, the dielectric is then etched to form trench openings that will suffice not only as contacts, but also as the local interconnects themselves. That is, a single trench etched through the dielectric opens up contact regions **31** and **32** as well as interconnect region **35** as shown in FIG. **3**. Similarly, an additional trench may be etched into the dielectric for contact regions **33** and **34** as well as interconnect region **36**. Other openings in the dielectric, such as Vss contact opening **14*c*3**, may be also etched into the dielectric at this time. Next, an adhesion layer may be formed by blanket depositing an adhesion material onto the sidewalls and bottom of the trenches and contact openings. After the adhesion layer has been formed, a conductive material layer may then be deposited. This conductive material is planarized such that the uppermost surfaces of the trenches and contacts are substantially commensurate to an uppermost

surface of the dielectric material. Again, this planarization step may be accomplished via CMP. At this point, the local interconnect layer process for the preferred embodiment is complete. Consequently, multiple processing steps are eliminated as compared to the above-described formation of local interconnects dielectrically spaced above the substrate. In particular, eliminated are the deposition of an additional conductive layer, the patterning of the additional conductive layer, and the etching of the additional conductive layer.

Returning to FIG. **3**, in addition to local interconnect structures **35** and **36** and their respective contacts, other interconnect structures of interest are shown. Interconnect structures **38** and **39** correspond to bitlines "Bit" and "/Bit" and contacts **16***c* and **15***c*, respectively. It is noted that the contacts shown correspond to those shown in FIG. **2**. Similarly, interconnect structures **37** and **40** correspond to Vss and contacts **14***c***3** and **14***c***2**, respectively, while interconnect structures **41** and **42** correspond to Vcc and contacts **13***c***6** and **13***c***5**, respectively. Following the interconnect layer, dielectric material may be arranged upon the interconnect layer, and contacts may subsequently be formed through this dielectric material. Another conducting layer, typically some type of metal, may be formed above the dielectric material and patterned and etched. This metal layer may be referred to as a first metal layer. Frequently, this metal layer contacts the bitlines, Vcc, and Vss globally across several memory cells. Yet another dielectric material may be arranged upon this first metal layer, and upon the dielectric material may be deposited a second metal layer. This second metal layer may be used as a global wordline. For example, interconnect structures **43** and **44** correspond to global wordline **17** and contacts **17***c***1** and **17***c***4**.

It will be appreciated to those skilled in the art having the benefit of this disclosure that the embodiments described are believed applicable to semiconductor memories. Furthermore, although illustrated with reference to SRAMs, the system and method disclosed herein may be adapted to other types of memory devices. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense as to possibly numerous architectures, circuitry, and methodologies which fall within the spirit and scope of the present invention.

What is claimed is:

1. A memory cell comprising a series of four substantially oblong active regions formed within a semiconductor substrate and arranged side-by-side with long axes substantially parallel, wherein each of the inner active regions of the series comprises a pair of source/drain regions for a respective p-channel transistor, and each of the outer active regions of the series comprises a pair of source/drain regions for a respective n-channel transistor.

2. The memory cell as recited in claim **1**, further comprising a plurality of substantially oblong polysilicon structures arranged above and substantially perpendicular to the active regions.

3. The memory cell as recited in claim **1**, wherein each active region comprises source/drain regions for no more than two transistors.

4. The memory cell as recited in claim **2**, further comprising source/drain contacts to the source/drain regions of transistors, wherein at least one of the source/drain contacts comprises a shared contact to one of the inner active regions and one of the polysilicon structures.

5. The memory cell as recited in claim **4**, further comprising a series of substantially oblong local interconnects arranged substantially perpendicular to the active regions, wherein the shared contact is connected to another of the source/drain contacts by one of the local interconnects.

6. The memory cell as recited in claim **5**, wherein the local interconnects are dielectrically spaced above the semiconductor substrate.

7. The memory cell as recited in claim **5**, wherein the local interconnects have an upper surface that is substantially coplanar with an upper surface of the source/drain contacts.

8. A memory cell comprising a plurality of substantially oblong active regions formed in a semiconductor substrate and arranged substantially in parallel with one another, and a plurality of substantially oblong local interconnects above said substrate that extend only partially across the memory cell and are arranged substantially in parallel with one another and substantially perpendicular to said active regions.

9. The memory cell as recited in **8**, further comprising substantially square local interconnects above said substrate, wherein all local interconnects within the cell are either substantially oblong or substantially square.

10. The memory cell as recited in claim **8**, further comprising a shared contact to one of the active regions and a polysilicon structure, wherein the polysilicon structure is arranged substantially perpendicular to said active region and a portion of the polysilicon structure abuts a portion of said active region.

* * * * *

US006534805C1

(12) **EX PARTE REEXAMINATION CERTIFICATE** (10327th)

United States Patent

Jin

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(54) **SRAM CELL DESIGN**

(75) Inventor: **Bo Jin**, Campbell, CA (US)

(73) Assignee: **Cypress Semiconductor Corporation**, San Jose, CA (US)

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(52) **U.S. Cl.**
USPC **257/206**; 257/211; 257/369; 438/153

(58) **Field of Classification Search**
None
See application file for complete search history.

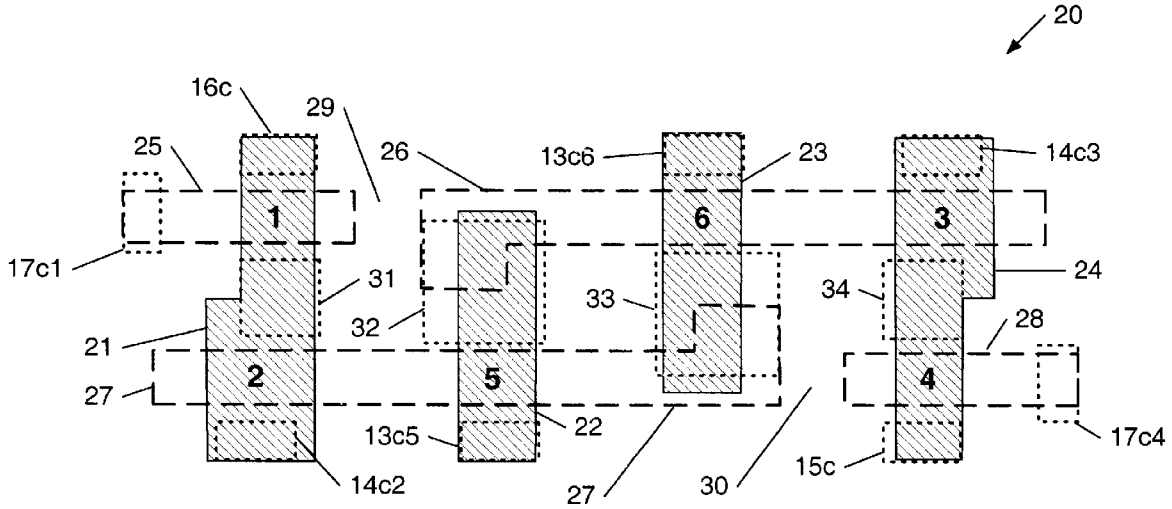
(56) **References Cited**

To view the complete listing of prior art documents cited during the proceeding for Reexamination Control Number 90/011,833, please refer to the USPTO's public Patent Application Information Retrieval (PAIR) system under the Display References tab.

Primary Examiner — Leonardo Andujar

(57) **ABSTRACT**

An embodiment of a memory cell includes a series of four substantially oblong parallel active regions, arranged side-by-side such that the inner active regions of the series include source/drain regions for p-channel transistors, and the outer active regions include source/drain regions for n-channel transistors. Another embodiment of the memory cell includes six transistors having gates substantially parallel to one another, where three of the gates are arranged along a first axis and the other three gates are arranged along a second axis parallel to the first axis. In another embodiment, the memory cell may include substantially oblong active regions arranged substantially in parallel with one another, with substantially oblong local interconnects arranged above and substantially perpendicular to the active regions. A method for fabricating a memory cell may include forming substantially oblong active regions within a semiconductor substrate, and forming substantially oblong local interconnects above and perpendicular to the active regions.



EX PARTE REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

THE PATENT IS HEREBY AMENDED AS INDICATED BELOW.

Matter enclosed in heavy brackets [ ] appeared in the patent, but has been deleted and is no longer a part of the patent; matter printed in italics indicates additions made to the patent.

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

Claims **1-6** are cancelled.

Claim **8** is determined to be patentable as amended.

Claims **9-10**, dependent on an amended claim, are determined to be patentable.

New claims **11-61** are added and determined to be patentable.

Claim **7** was not reexamined.

8. A memory cell comprising a plurality of substantially oblong active regions formed in a semiconductor substrate and arranged substantially in parallel with one another, and a plurality of substantially oblong local interconnects above said substrate that extend only partially across the memory cell and are arranged substantially in parallel with one another and substantially perpendicular to said active regions*; and*

a single local interconnect layer comprising local interconnects corresponding to bitlines and a global wordline.

11. The memory cell of claim 8, wherein each local interconnect of the single local interconnect layer is substantially oblong.

12. The memory cell of claim 8, the single local interconnect layer comprising local interconnects corresponding to common power and common ground.

13. The memory cell of claim 12, wherein each local interconnect of the single local interconnect layer is substantially oblong.

14. The memory cell of claim 8, comprising:

a first contact to one of the substantially oblong active regions;

a shared contact to another one of the substantially oblong active regions and a polysilicon structure;

a first substantially oblong local interconnect that connects the first contact and the shared contact,

wherein the single local interconnect layer comprises the first substantially oblong local interconnect.

15. The memory cell of claim 8, comprising:

a first contact to one of the substantially oblong active regions;

a shared contact to another one of the substantially oblong active regions and a polysilicon structure;

a first substantially oblong local interconnect that connects the first contact and the shared contact,

wherein the first substantially oblong local interconnect is formed from a trench opening as a contact to one of the substantially oblong active regions.

16. A memory cell, comprising:

a series of four substantially oblong active regions formed within a semiconductor substrate and arranged side-by-side with long axes substantially parallel,

wherein each inner active region of the series comprises a pair of source/drain regions for a respective p-channel transistor, and

wherein each outer active region of the series comprises a pair of source/drain regions for a respective n-channel transistor; and

a single local interconnect layer comprising local interconnects corresponding to bitlines and a global wordline.

17. The memory cell of claim 16, wherein each local interconnect of the single local interconnect layer is substantially oblong.

18. The memory cell of claim 16, the single local interconnect layer comprising local interconnects corresponding to common power and common ground.

19. The memory cell of claim 18, wherein each local interconnect of the single local interconnect layer is substantially oblong.

20. The memory cell of claim 16, comprising:

a first contact to one of the outer active regions;

a shared contact to one of the inner active regions and a polysilicon structure;

a first substantially oblong local interconnect that connects the first contact and the shared contact,

wherein the single local interconnect layer comprises the first substantially oblong local interconnect.

21. The memory cell of claim 16, comprising:

a first contact to one of the outer active regions;

a shared contact to one of the inner active regions and a polysilicon structure;

a first substantially oblong local interconnect that connects the first contact and the shared contact,

wherein the first substantially oblong local interconnect is formed from a trench opening as a contact to one of the active regions.

22. The memory cell of claim 16, comprising:

a plurality of substantially oblong polysilicon structures arranged above and substantially perpendicular to the active regions.

23. The memory cell of claim 16, comprising:

source/drain contacts to the source/drain regions of transistors,

wherein at least one of the source/drain contacts comprises a shared contact to one of the inner active regions and one of the polysilicon structures.

24. The memory cell of claim 23, comprising:

a series of substantially oblong local interconnects arranged substantially perpendicular to the active regions,

wherein the shared contact is connected to another of the source/drain contacts by one of the substantially oblong local interconnects.

25. The memory cell of claim 24, wherein the substantially oblong local interconnects are dielectrically spaced above the semiconductor substrate.

26. The memory cell of claim 24, wherein the substantially oblong local interconnects have an upper surface that is substantially coplanar with an upper surface of the source/drain contacts.

27. A memory cell, comprising:

a series of four substantially oblong active regions formed within a semiconductor substrate and arranged side-by-side with long axes substantially parallel,

wherein each inner active region of the series comprises a pair of source/drain regions for a respective p-channel transistor, and

wherein each outer active region of the series comprises a pair of source/drain regions for a respective n-channel transistor;

a first contact to one of the outer active regions;

a shared contact to both a polysilicon structure and to one of the inner active regions; and

a substantially oblong local interconnect that connects the first contact and the shared contact,

wherein the substantially oblong local interconnect overlaps both the polysilicon structure and said one of the inner active regions.

28. The memory cell of claim 27, wherein the substantially oblong local interconnect is dielectrically spaced above the semiconductor substrate.

29. A memory cell, comprising:

a series of four substantially oblong active regions formed within a semiconductor substrate and arranged side-by-side with long axes substantially parallel,

wherein each inner active region of the series comprises a pair of source/drain regions for a respective p-channel transistor, and

wherein each outer active region of the series comprises a pair of source/drain regions for a respective n-channel transistor;

a first contact to one of the outer active regions;

source/drain contacts to the source/drain regions of transistors, wherein at least one of the source/drain contacts comprises a shared contact to both a polysilicon structure and to one of the inner active regions; and

a substantially oblong local interconnect that connects the first contact and the shared contact,

wherein the substantially oblong local interconnect overlaps both the polysilicon structure and said one of the inner active regions, and

wherein the substantially oblong local interconnect has an upper surface that is substantially coplanar with an upper surface of the source/drain contacts.

30. A memory cell, comprising:

a plurality of substantially oblong active regions formed in a semiconductor substrate and arranged substantially in parallel with one another;

a plurality of substantially oblong local interconnects above said substrate that extend partially across the memory cell and are arranged substantially in parallel with one another and substantially perpendicular to the active regions;

a first contact to one of the active regions;

a shared contact to both a polysilicon structure and to another one of the active regions; and

a substantially oblong local interconnect that connects the first contact and the shared contact,

wherein the substantially oblong local interconnect overlaps both the polysilicon structure and said another one of the active regions.

31. The memory cell of claim 30, comprising:

substantially square local interconnects above the substrate,

wherein local interconnects within the cell are one of substantially oblong and substantially square.

32. The memory cell of claim 30,

wherein the polysilicon structure is arranged substantially perpendicular to said another one of the active regions, and

wherein a portion of the polysilicon structure abuts a portion of the said another one of the active regions.

33. A memory cell, comprising:

a series of four substantially oblong active regions formed within a semiconductor substrate and arranged side-by-side with long axes substantially parallel,

wherein each inner active region of the series comprises a pair of source/drain regions for a respective p-channel transistor,

wherein each outer active region of the series comprises a pair of source/drain regions for a respective n-channel transistor, and

wherein a width varies along a length of each of the active regions.

34. The memory cell of claim 33, wherein the length varies along the width of each of the active regions.

35. The memory cell of claim 33, comprising:

a plurality of substantially oblong polysilicon structures arranged above and substantially perpendicular to the active regions.

36. The memory cell of claim 35, comprising:

source/drain contacts to the source/drain regions of transistors,

wherein at least one of the source/drain contacts comprises a shared contact to one of the inner active regions and one of the polysilicon structures.

37. The memory cell of claim 36, comprising:

a series of substantially oblong local interconnects arranged substantially perpendicular to the active regions,

wherein the shared contact is connected to another of the source/drain contacts by one of the local interconnects.

38. The memory cell of claim 37, wherein the local interconnects are dielectrically spaced above the semiconductor substrate.

39. The memory cell of claim 37, wherein the substantially oblong local interconnects have an upper surface that is substantially coplanar with an upper surface of the source/drain contacts.

40. A memory cell, comprising:

a series of four substantially oblong active regions formed within a semiconductor substrate and arranged side-by-side with long axes substantially parallel,

wherein each inner active region of the arrangement comprises a pair of source/drain regions for a respective p-channel transistor,

wherein each outer active region of the arrangement comprises a pair of source/drain regions for a respective n-channel transistor, and

wherein a width varies along at least a portion of a length and the length varies along at least a portion of the width of each of the four substantially oblong active regions.

41. The memory cell of claim 40, comprising:

a plurality of substantially oblong polysilicon structures arranged above and substantially perpendicular to the active regions.

42. The memory cell of claim 41, comprising:

source/drain contacts to the source/drain regions of transistors,

wherein at least one of the source/drain contacts comprises a shared contact to one of the inner active regions and one of the polysilicon structures.

43. The memory cell of claim 42, comprising:

a series of substantially oblong local interconnects arranged substantially perpendicular to the active regions,

wherein the shared contact is connected to another of the source/drain contacts by one of the local interconnects.

44. The memory cell of claim 43, wherein the local interconnects are dielectrically spaced above the semiconductor substrate.

45. The memory cell of claim 43, wherein the substantially oblong local interconnects have an upper surface that is substantially coplanar with an upper surface of the source/drain contacts.

46. A memory cell, comprising

a series of four substantially oblong active regions formed in a semiconductor substrate and arranged substantially in parallel with one another,

wherein a width varies along a length of each of the active regions; and

a plurality of substantially oblong local interconnects that above the substrate and extend partially across the memory cell and are arranged substantially in parallel with one another and substantially perpendicular to the active regions.

47. The memory cell of claim 46, wherein the length varies along the width of each of the active regions.

48. The memory cell of claim 46, comprising:

substantially square local interconnects above the substrate,

wherein all local interconnects within the cell are either substantially oblong or substantially square.

49. The memory cell of claim 46, comprising:

a shared contact to one of the active regions and a polysilicon structure,

wherein the polysilicon structure is arranged substantially perpendicular to the active region, and

wherein a portion of the polysilicon structure abuts a portion of the active region.

50. A memory cell, comprising:

a series of four substantially oblong active regions formed in a semiconductor substrate and arranged substantially in parallel with one another,

wherein a width varies along at least a portion of a length and the length varies along at least a portion of the width of each of the plurality of active regions; and

a plurality of substantially oblong local interconnects above the substrate that extend partially across the memory cell and are arranged substantially in parallel with one another and substantially perpendicular to the active regions.

51. The memory cell of claim 50, comprising:

substantially square local interconnects above the substrate,

wherein local interconnects within the cell are one of substantially oblong and substantially square.

52. The memory cell of claim 50, comprising:

a shared contact to one of the active regions and a polysilicon structure,

wherein the polysilicon structure is arranged substantially perpendicular to the active region, and

wherein a portion of the polysilicon structure abuts a portion of the active region.

53. A memory cell, comprising:

a series of four substantially oblong active regions formed within a semiconductor substrate and arranged side-by-side with long axes substantially parallel,

wherein each inner active region of the series comprises a pair of source/drain regions for a respective p-channel transistor, and

wherein each outer active region of the series comprises a pair of source/drain regions for a respective n-channel transistor;

a first metal layer above the semiconductor substrate,

wherein the first metal layer contacts bitlines, common power, and common ground globally across a plurality of memory cells; and

a second metal layer above the first metal layer,

wherein the second metal layer is configured as a global wordline.

54. The memory cell of claim 53, comprising:

a plurality of substantially oblong polysilicon structures arranged above and substantially perpendicular to the active regions.

55. The memory cell of claim 54, comprising:

source/drain contacts to the source/drain regions of transistors,

wherein at least one of the source/drain contacts comprises a shared contact to one of the inner active regions and one of the polysilicon structures.

56. The memory cell of claim 55, comprising:

a series of substantially oblong local interconnects arranged substantially perpendicular to the active regions,

wherein the shared contact is connected to another of the source/drain contacts by one of the local interconnects.

57. The memory cell of claim 56, wherein the local interconnects are dielectrically spaced above the semiconductor substrate.

58. The memory cell of claim 56, wherein the substantially oblong local interconnects have an upper surface that is substantially coplanar with an upper surface of the source/drain contacts.

59. A memory cell, comprising:

a plurality of substantially oblong active regions formed in a semiconductor substrate and arranged substantially in parallel with one another;

a plurality of substantially oblong local interconnects above the substrate and extending partially across the memory cell and are arranged substantially in parallel with one another and substantially perpendicular to the active regions;

a first metal layer above the semiconductor substrate,

wherein the first metal layer contacts bitlines, common power, and common ground globally across a plurality of memory cells; and

a second metal layer above the first metal layer,

wherein the second metal layer is configured as a global wordline.

60. The memory cell of claim 59, comprising:

substantially square local interconnects above the substrate,

wherein local interconnects within the cell are one of substantially oblong and substantially square.

61. The memory cell of claim 59, comprising:

a shared contact to one of the active regions and a polysilicon structure,

wherein the polysilicon structure is arranged substantially perpendicular to the active region, and

wherein a portion of the polysilicon structure abuts a portion of the active region.

* * * * *

EXHIBIT B

US006629226B1

(12) **United States Patent**
Paul et al.

(10) **Patent No.: US 6,629,226 B1**
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(54) **FIFO READ INTERFACE PROTOCOL**

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(52) **U.S. Cl.** **711/169**
(58) **Field of Search** 711/154, 169, 711/170; 710/52

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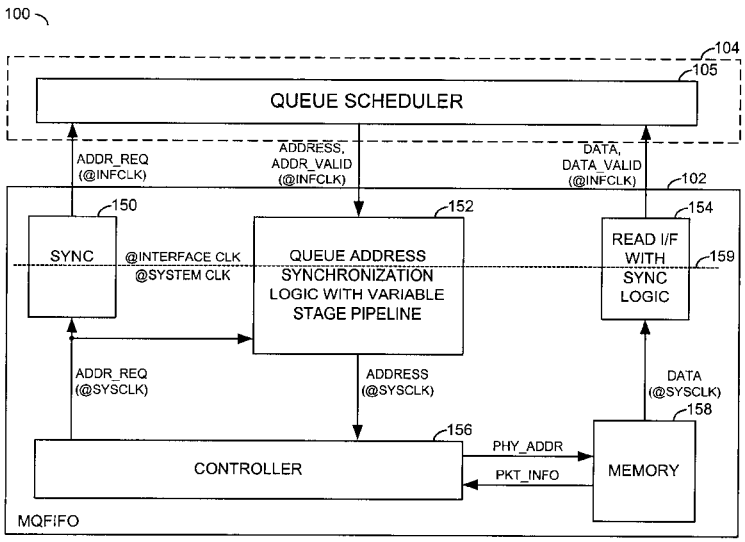
(57) **ABSTRACT**

An interface coupled to a multiqueue storage device and configured to interface the multiqueue storage device with one or more handshaking signals. The multiqueue storage device and the interface may be configured to transfer variable size data packets.

19 Claims, 4 Drawing Sheets



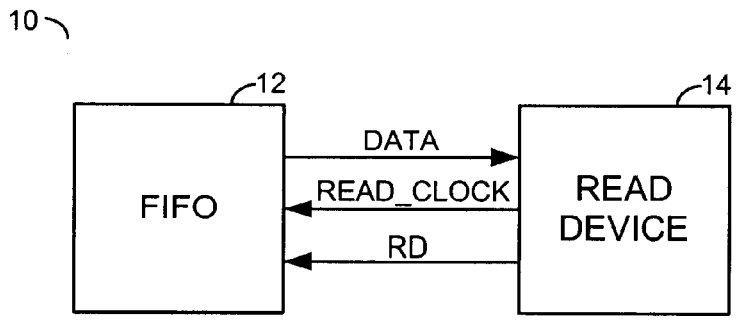


FIG. 1

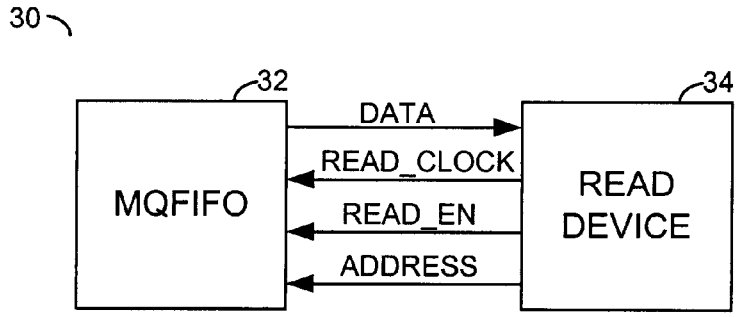


FIG. 2

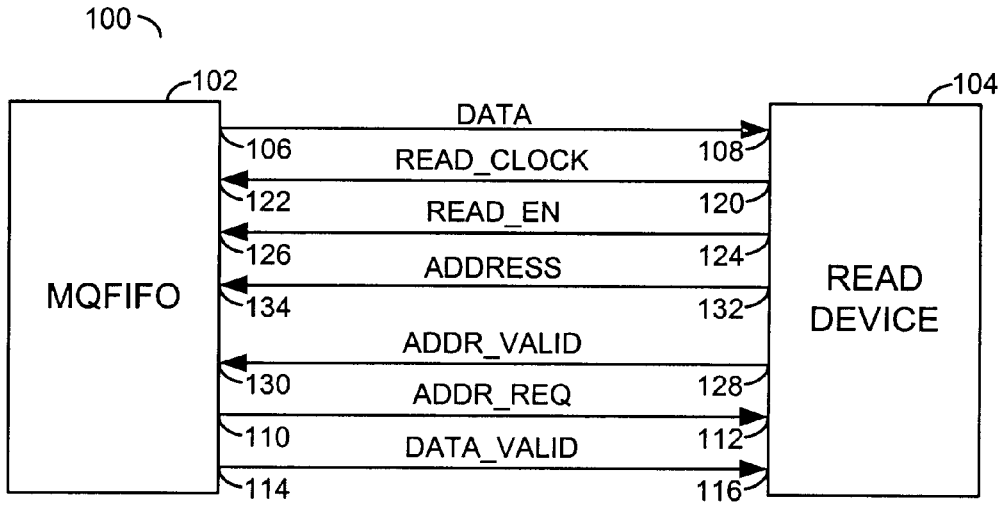


FIG. 3

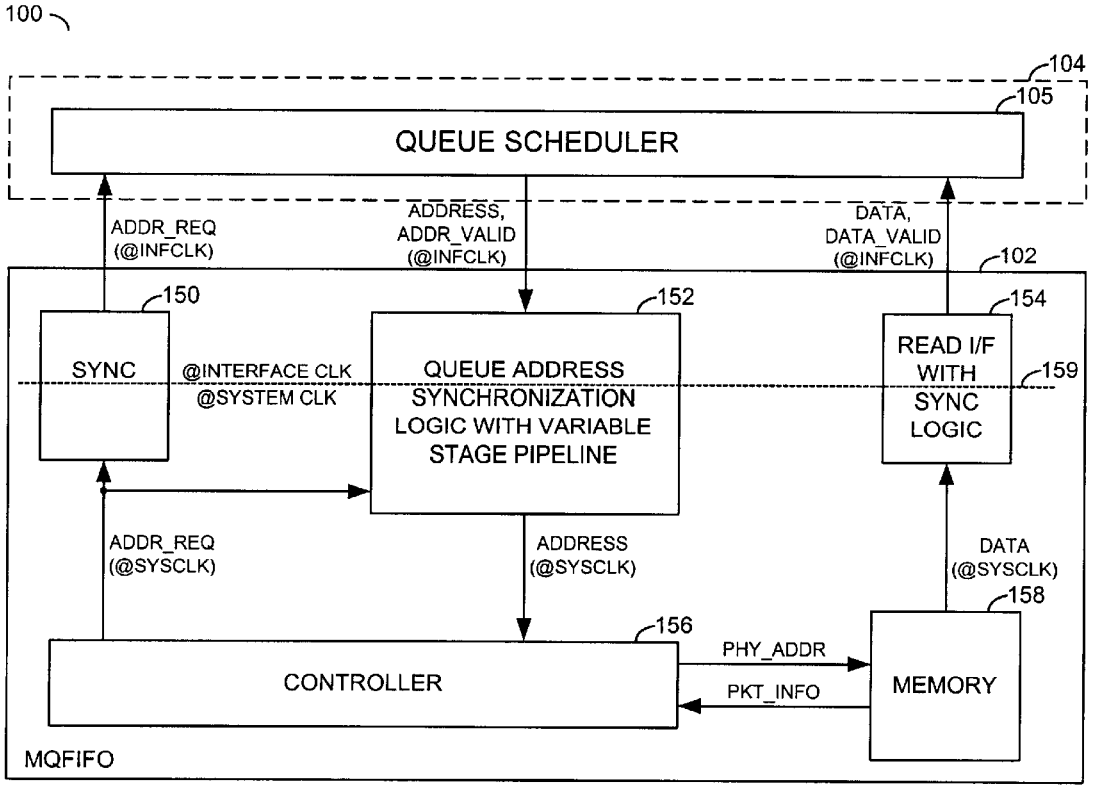

100
104
105
QUEUE SCHEDULER
ADDR_REQ (@INFCLK)
ADDRESS, ADDR_VALID (@INFCLK)
DATA, DATA_VALID (@INFCLK)
102
150
152
154
SYNC
@INTERFACE CLK
@SYSTEM CLK
QUEUE ADDRESS SYNCHRONIZATION LOGIC WITH VARIABLE STAGE PIPELINE
READ I/F WITH SYNC LOGIC
159
ADDR_REQ (@SYSCLK)
ADDRESS (@SYSCLK)
DATA (@SYSCLK)
158
156
PHY_ADDR
PKT_INFO
CONTROLLER
MEMORY
MQFIFO

FIG. 4

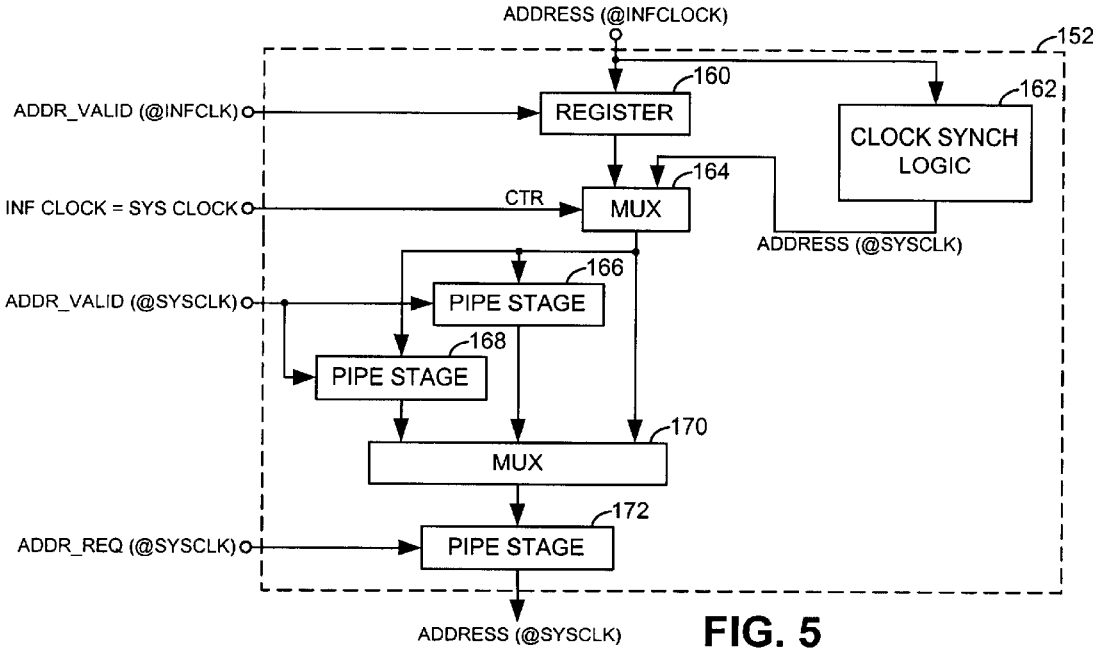

ADDRESS (@INFCLOCK)
152
160
162
ADDR_VALID (@INFCLK)
REGISTER
CLOCK SYNCH LOGIC
164
INF CLOCK = SYS CLOCK
CTR
MUX
ADDRESS (@SYSCLK)
166
ADDR_VALID (@SYSCLK)
PIPE STAGE
168
PIPE STAGE
170
MUX
172
ADDR_REQ (@SYSCLK)
PIPE STAGE
ADDRESS (@SYSCLK)

FIG. 5

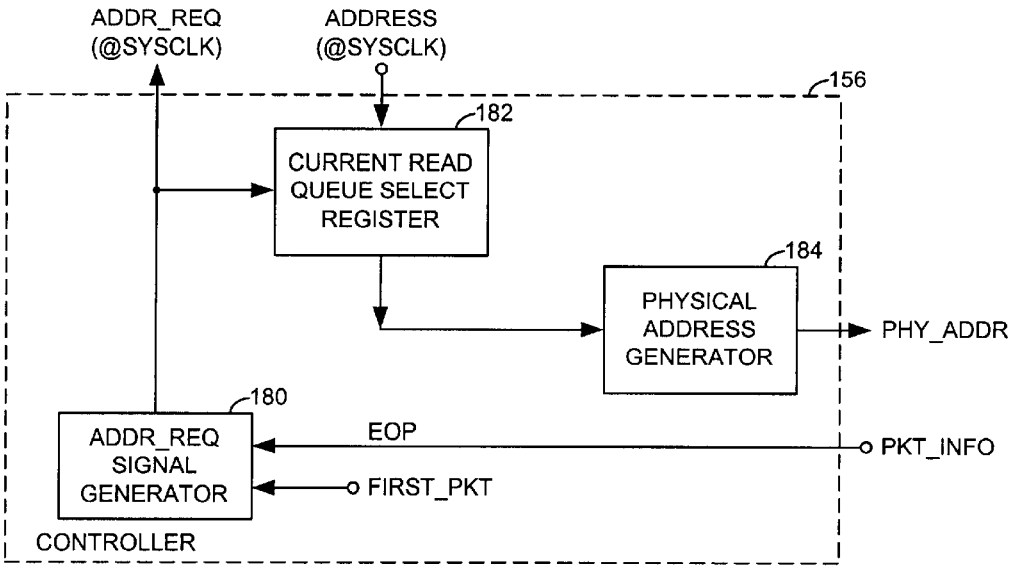

ADDR_REQ
(@SYSCLK)
ADDRESS
(@SYSCLK)
156
182
CURRENT READ
QUEUE SELECT
REGISTER
184
PHYSICAL
ADDRESS
GENERATOR
PHY_ADDR
180
ADDR_REQ
SIGNAL
GENERATOR
EOP
PKT_INFO
FIRST_PKT
CONTROLLER

FIG. 6

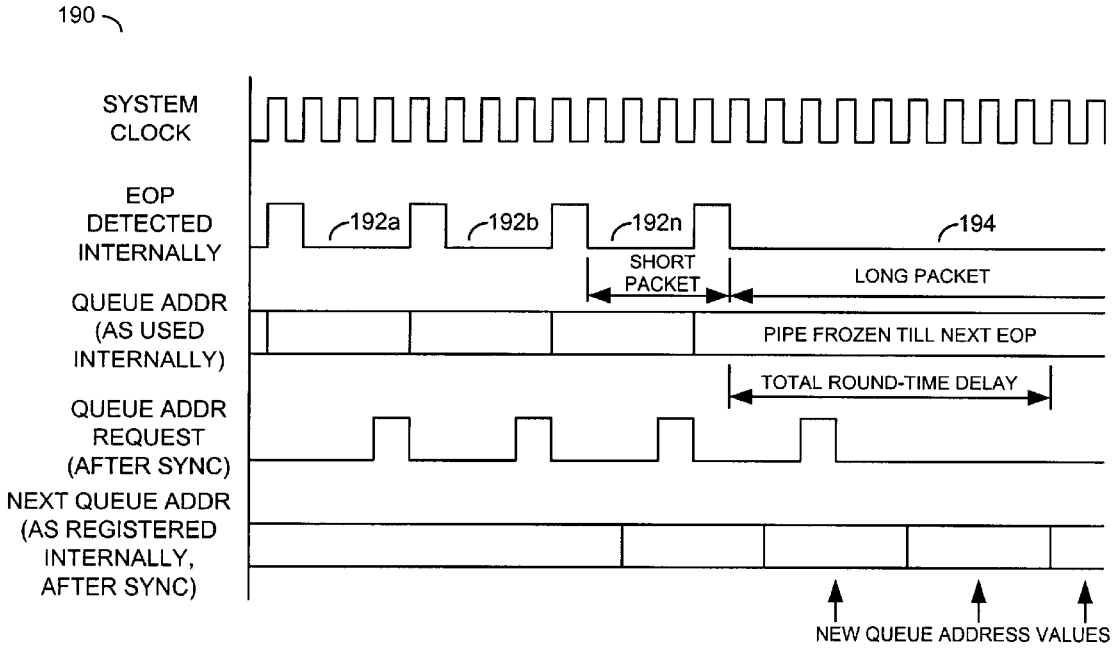

190
SYSTEM
CLOCK
EOP
DETECTED
INTERNALLY
192a
192b
192n
194
SHORT
PACKET
LONG PACKET
QUEUE ADDR
(AS USED
INTERNALLY)
PIPE FROZEN TILL NEXT EOP
TOTAL ROUND-TIME DELAY
QUEUE ADDR
REQUEST
(AFTER SYNC)
NEXT QUEUE ADDR
(AS REGISTERED
INTERNALLY,
AFTER SYNC)
NEW QUEUE ADDRESS VALUES

FIG. 7

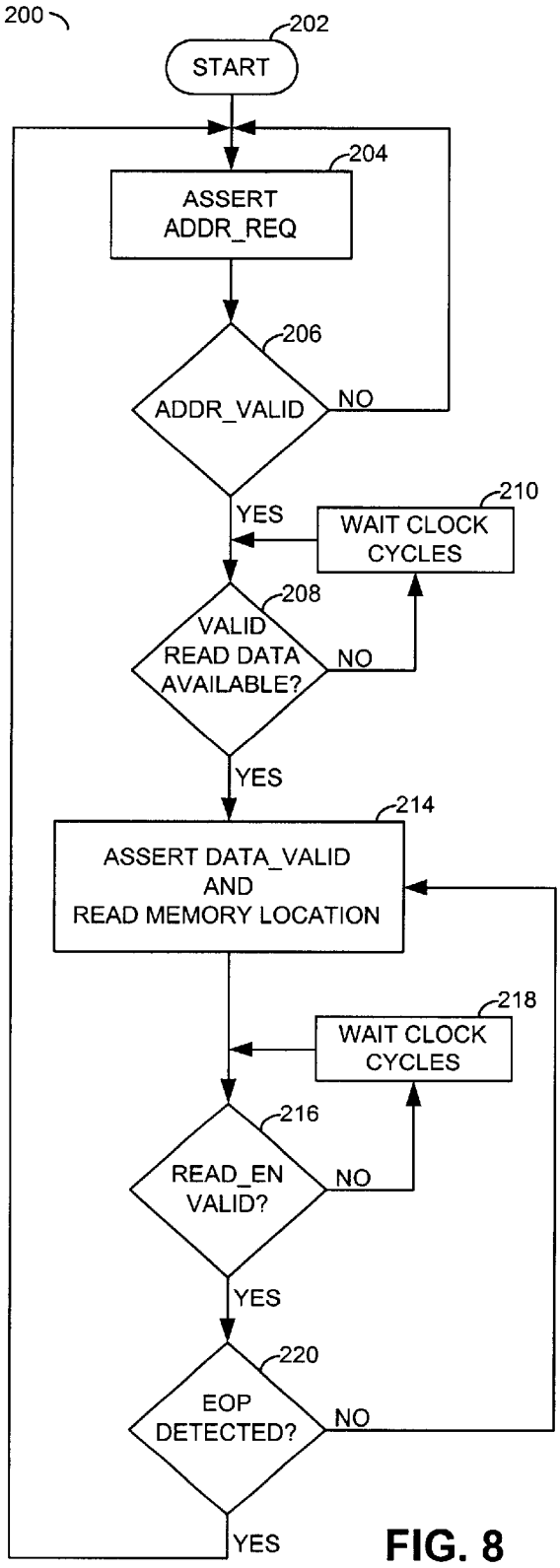

200
202
START
204
ASSERT ADDR_REQ
206
ADDR_VALID
NO
YES
210
WAIT CLOCK CYCLES
208
VALID READ DATA AVAILABLE?
NO
YES
214
ASSERT DATA_VALID AND READ MEMORY LOCATION
218
WAIT CLOCK CYCLES
216
READ_EN VALID?
NO
YES
220
EOP DETECTED?
NO
YES

FIG. 8

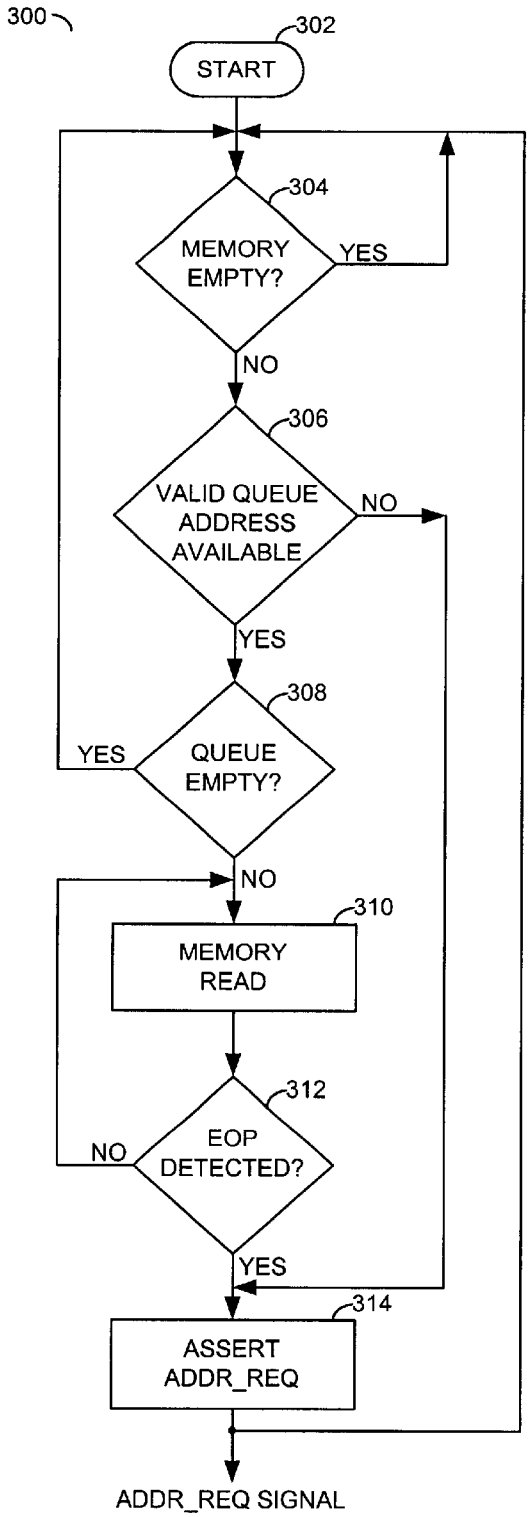

300
302
START
304
MEMORY EMPTY?
YES
NO
306
VALID QUEUE ADDRESS AVAILABLE
NO
YES
308
QUEUE EMPTY?
YES
NO
310
MEMORY READ
312
EOP DETECTED?
NO
YES
314
ASSERT ADDR_REQ
ADDR_REQ SIGNAL

FIG. 9

FIFO READ INTERFACE PROTOCOL

CROSS REFERENCE TO RELATED APPLICATIONS

The present application may relate to co-pending application Ser. No. 09/714,441, filed Nov. 16, 2000, Ser. No. 09/732,686, filed Dec. 8, 2000, Ser. No. 09/732,687, filed Sep. 8, 2000, Ser. No. 09/676,704, filed Sep. 29, 2000, Ser. No. 09/676,171, filed Sep. 29, 2000, Ser. No. 09/676,706, filed Sep. 29, 2000, Ser. No. 09/676,705, filed Sep. 29, 2000, Ser. No. 09/676,170, filed Sep. 29, 2000 and Ser. No. 09/676,169, filed Sep. 29, 2000, which are each hereby incorporated by reference in their entirety.

FIELD OF THE INVENTION

The present invention relates to a method and/or architecture for implementing a multiqueue first-in-first-out (FIFO) memory read interface generally and, more particularly, to a method and/or architecture for implementing a multiqueue FIFO read interface protocol for eliminating synchronizing problems for configuration dependent latencies where the protocol may be capable of handling variable size packets.

The present invention may also relate to a method and/or architecture for variable stage pipeline system generally and, more particularly, to a method and/or architecture for implementing an event driven variable stage pipeline system for handling variable size blocks that may have a minimum block size less than total round-time delay.

BACKGROUND OF THE INVENTION

Referring to FIG. **1**, a diagram illustrating a conventional circuit **10** for exchanging data between a first-in-first-out (FIFO) device **12** and a read device **14** is shown. A read signal RD is presented from the read device **14** to the FIFO **12**. After a fixed number of latency cycles, the signal DATA is presented to the read device **14**. The signals READ_CLOCK and RD control the timing of the presentation of the data signal DATA.

Referring to FIG. **2**, a diagram illustrating a conventional system **30** for exchanging data between a multiqueue FIFO **32** and a read device **34** is shown. The signal ADDRESS is a queue address configured to determine a queue number of the multiqueue FIFO **32**. The signals READ_CLOCK and READ_EN control the timing of the presentation of the data signal DATA.

The read signal RD in FIG. **1** is replaced by the read enable signal READ_EN in FIG. **2**. The signal READ_EN controls whether to continue or to stop a particular read. The queue address signal ADDRESS is an additional signal not present in FIG. **1**. Since there are multiple queues in the FIFO **32**, a read occurs from the particular queue that is addressed by the signal ADDRESS.

Because of particular architectures (e.g., the cited co-pending applications) and specifications of particular devices, the latency between enabling the queue address signal ADDRESS and presenting the signal DATA can differ depending on the particular configuration. The configuration information needs to be written into the external read device **34**. The only event reference available to the external read device **34** is an end of packet or a start of packet (EOP/SOP). In such an environment, the read device **34** is required to monitor this event to generate the queue address signal ADDRESS in a sufficient number of cycles ahead of the read.

The circuit **30** has the disadvantage of requiring a fixed packet size. The circuit **30** can be required to generate the queue address ADDRESS a certain number of cycles before the EOP occurs. The particular number of cycles is the same as the minimum latency requirement. For certain configurations, there is a specific latency between the queue address signal ADDRESS and presenting the signal DATA. If the packet size varies randomly, such as when the size of the packet is less than the number of cycles of latency, a read of one or more unwanted packets occurs. The circuit **30** additionally requires a pipeline memory (within the multiqueue **32**) to handle variable sized packets in an asynchronous configuration.

It may also be difficult for the read device **34** to synchronize the queue address signal ADDRESS with the data received from the FIFO **32**. Therefore, the read device **34** needs to be configured with enough logic to respond to the different latencies. Such a configuration requires extra overhead for the read device **34**.

Handling of slow read clock speeds is also difficult within the circuit **30**. The read operation occurs at one clock and the internal logic operates at another clock, such as the system clock (e.g., the cited co-pending applications). This requires the queue address signal ADDRESS and the read enable signal READ_EN to be synchronized before other processing can be executed. The data read also needs to be synchronized. As a result, there is an uncertainty of 1–2 clock cycles resulting in the latency. This makes the synchronization between the queue address signal ADDRESS and the data read extremely difficult.

SUMMARY OF THE INVENTION

One aspect of the present invention concerns an interface coupled to a multiqueue storage device and configured to interface the multiqueue storage device with one or more handshaking signals. The multiqueue storage device and the interface may be configured to transfer variable size data packets.

Another aspect of the present invention concerns an apparatus configured to interface a first clock speed of a multiqueue storage device and a second clock speed of an interface. The apparatus may be configured to control a flow of variable size data packets.

The objects, features and advantages of the present invention include providing a method and/or architecture for implementing a multiqueue FIFO read interface protocol that may (i) eliminate synchronizing problems with configuration dependent latencies; (ii) be capable of handling variable size packets; (iii) allow back-to-back reads of variable size packets; (iv) exchange address and data between an external read device and a multiqueue storage device; (v) generate an address request for an external device from the storage device; (vi) generate a valid queue address in response to the address request; (vii) provide data in response to the valid queue address; (viii) provide a single clock domain or a dual clock domain between a multiqueue storage device and a read interface device; (ix) vary a latency between an address request and an address validate; (x) provide an event driven variable stage pipeline system; and/or (xi) handle variable size packets with a minimum packet size less than a total round-time delay.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects, features and advantages of the present invention will be apparent from the following detailed description and the appended claims and drawings in which:

FIG. **1** is a block diagram of a conventional interface between a FIFO and a read device;

FIG. **2** is a block diagram of a conventional interface between a multiqueue FIFO and a read device;

FIG. **3** is a block diagram of a preferred embodiment of the present invention;

FIG. **4** is a block diagram of a preferred embodiment of the present invention;

FIG. **5** is a detailed block diagram of a logic circuit of FIG. **4**;

FIG. **6** is a detailed block diagram of a controller circuit of FIG. **4**;

FIG. **7** is a timing diagram illustrating an operation of the present invention;

FIG. **8** is a flow diagram illustrating an operation of the present invention; and

FIG. **9** is a flow diagram illustrating an operation of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. **3**, a block diagram of a system (or circuit) **100** is shown in accordance with a preferred embodiment of the present invention. The system **100** generally comprises a storage device **102** and a read device **104**. The storage device **102** is generally implemented as a FIFO. In one example, the read device **104** may be implemented as an external read interface device (e.g., implemented externally from the FIFO **102**). The FIFO **102** may be implemented as a single port device or a multiport device. The FIFO **102** may be implemented, in one example, as a multiqueue FIFO. However, other appropriate type storage devices may be implemented accordingly to meet the design criteria of a particular implementation.

The FIFO **102** may have an output **106** that presents a signal (e.g., DATA) to an input **108** of the read device **104**, an output **110** that presents a signal (e.g., ADDR_REQ) to an input **112** of the read device **104** and an output **114** that presents a signal (e.g., DATA_VALID) to an input **116** of the read device **104**. The read device **104** may have an output **120** that presents a signal (e.g., READ_CLOCK) to an input **122** of the FIFO **102**, an output **124** that presents a signal (e.g., READ_EN) to an input **126** of the FIFO **102**, an output **128** that presents a signal (e.g., ADDR_VALID) to an input **130** of the FIFO **102** and an output **132** that presents a signal (e.g., ADDRESS) to an input **134** of the FIFO **102**. The signal READ_CLOCK may be implemented as a read clock signal. The signal READ_EN may be implemented as a read enable signal. The signal ADDRESS may be implemented as a queue address signal. The signal ADDR_VALID may be implemented as a valid address indication signal. The signal ADDR_REQ may be implemented as an address request signal. The signal DATA_VALID may be implemented as a data validation signal. In one example, the various signals of the present invention may be implemented as handshaking signals. Specifically, the signals ADDR_VALID, ADDR_REG and DATA_VALID may allow for variable size data packets and asynchronous operation.

The read device **104** may read various size packets from the multiqueue FIFO **102**. The circuit **100** may accommodate different latency requirements between receiving the signal ADDRESS and presenting the signal DATA, depending on a particular configuration. The read device **104** may have to account for timing considerations of the system **100**. The circuit **100** may illustrate an exchange of data (via variable size data packets) between the FIFO **102** and the read device **104**.

The circuit **100** generally implements a handshaking protocol to transfer data. For example, the signal ADDR_REQ may request a next queue address. The signal ADDR_VALID may then be asserted to indicate that the queue address ADDRESS is valid in the current cycle. The signal DATA_VALID may then be asserted to indicate that the read data DATA is valid. Additionally, the read enable signal READ_EN may be modified, in order to indicate whether or not the read device **104** has space to continue with the read. Thus, the signal READ_EN may provide a "pause" feature of the circuit **100**. The read enable signal READ_EN may allow the read device **104** to efficiently control reading of data from the multiqueue FIFO **102**.

The read device **104** may generate the queue address signal ADDRESS and the queue address valid signal ADDR_VALID it response to the queue address request signal ADDR_REQ. The queue address valid signal ADDR_VALID may be required for a case when the read device **104** may not be ready with a computation of a next queue address. Internal logic of the FIFO **102** (to be described in connection with FIGS. **4–6**) may register the queue address signal ADDRESS at a certain time when the signal ADDR_VALID is valid. The signal DATA_VALID generally allows the read device **104** to know when to start and/or stop reading the data. The signal DATA_VALID may be implemented to synchronize the queue address ADDRESS with the signal DATA. Thus, the read data valid signal DATA_VALID is generally asserted when the signal DATA is presented.

The circuit **100** may allow accessing of variable size packets, where the minimum packet size may be less than a total round-time delay between a queue address request (e.g., the signal ADDR_REQ) and a queue address (e.g., the signal ADDRESS). One purpose of the circuit **100** may be to control the flow of queue addresses in order to read variable size packets in a two clock environment. For example, the read device **104** may be clocked by a different clock (e.g., an interface clock) than a system clock (e.g., a system clock of the circuit **100**).

Referring to FIG. **4**, a detailed block diagram of the circuit **100** is shown. FIG. **4** may illustrate a flow of information of the circuit **100**. The read device **104** may comprise a queue scheduler (or read control device) **105**. A maximum delay for the queue scheduler **105** may be 4 cycles, since a minimum packet size of the circuit **100** may be 4 cycles. The maximum delay (4 cycles) may allow the queue scheduler logic **105** to be simplistic. For example, the queue scheduler logic **105** may not require a previous queue address request to be stored.

The multiqueue FIFO **102** generally comprises a block (or circuit) **150**, a block (or circuit) **152**, a block (or circuit) **154**, a block (or circuit) **156** and a block (or circuit) **158**. The circuit **150** may be implemented as a synchronization circuit. The circuit **152** may be implemented as an address circuit. The circuit **152** may provide queue addresses to the circuit **100**. The circuit **152** may comprise synchronization logic that may provide a variable stage pipeline memory (to be discussed in connection with FIG. **5**). The circuit **154** may be implemented as a read interface circuit. The circuit **154** may comprise synchronization logic. The circuit **156** may be implemented as a controller circuit (to be discussed further in connection with FIG. **6**). The circuit **158** may be implemented as a memory circuit that may comprise a number of memory cells.

A dotted line **159** may illustrate a division between components operating at an interface clock (generally

referred to as a signal with the suffix "(@INFCLK)") and components operating at a system clock (generally referred to as signals with the suffix "(@SYSCLK)"). The controller **156** may present the signal ADDR_REQ(@SYSCLK) to the circuit **150** as well as to the circuit **152**. The circuit **150** generally presents the signal ADDR_REQ(@INFCLK) to the circuit **104**. The circuit **150** generally synchronizes the system clock domain and the interface clock domain for the signal ADDR_REQ(@INFCLK).

The circuit **152** generally presents the signal ADDRESS (@SYSCLK) to the controller **156**. The controller **156** generally presents a signal (e.g., PHY_ADDR) to the memory **158** in response to the signal ADDRESS (@SYSCLK). The memory **158** generally presents a signal (e.g., PKT_INFO) to the controller **156** and data (e.g., the signal DATA(@SYSCLK)) to the read interface **154**, while operating in the system clock domain. The interface **154** generally synchronizes the clock domain of read data to the interface clock domain as shown by the signals DATA (@INFCLK) and DATA(@SYSCLK).

Because of different latencies and variable size packets, the read device **104** may require stringent timing. The queue scheduler **105** may have difficulty predicting an appropriate time to (i) generate the signal ADDRESS and (ii) synchronize the read data DATA with the queue address signal ADDRESS. The FIFO **102** generally implements the controller **156** to control reading and writing in such cases. As a result, the circuit **100** may read data packets in all such cases.

Referring to FIG. **5**, a more detailed diagram of the queue address circuit **152** is shown. FIG. **5** illustrates a flow of the queue address ADDRESS within the address circuit **152**, in response to a queue address request (e.g., the signal ADDR_REQ) and subsequent data flow. Additionally, the circuit **152** of FIG. **5** may illustrate an example implementation of event driven variable stage pipelining of the queue address ADDRESS. The queue address circuit **152** generally comprises a register **160**, a clock synchronization logic block (or circuit) **162**, a multiplexer **164**, a pipeline stage **166**, a pipeline stage **168**, a multiplexer **170** and a pipeline stage **172**. The register **160** and the logic circuit **162** generally receive the signal ADDRESS(@INFCLK). The register **160** may also receive the signal ADDR_VALID(@INFCLK). The multiplexer **164** may receive a signal from the register **160** and the signal ADDRESS(@SYSCLK) from the logic circuit **162**.

The multiplexer **164** may present a signal to the pipeline stage **166**, the pipeline stage **168** and the multiplexer **170**, in response to a control signal (e.g., CTR) received at an input **165**. The signal CTR is generally in an asserted stage when the interface clock is equivalent to the system clock. The pipeline stage **166** and the pipeline stage **168** may receive the signal ADDR_VALID(@SYSCLK). The pipeline stage **166** and the pipeline stage **168** are generally clocked by the signal ADDR_VALID(@SYSCLK). The multiplexer **170** generally presents a signal from either the pipeline stage **166**, the pipeline stage **168** or the multiplexer **164** to the pipeline stage **172**. The pipeline stage **172** is generally clocked by the signal ADDR_REQ(@SYSCLK). The pipeline stage **172** may then present the signal ADDRESS (@SYSCLK).

A detailed description of the flow of the queue address synchronization logic **152** will now be described. The queue address ADDRESS, if valid as indicated by the signal ADDR_VALID, is synchronized with respect to the system clock (e.g., at the clock synchronous logic block **162**), before the queue address ADDRESS is registered (e.g., at the register **160**). The queue address ADDRESS may then be passed through a variable stage pipeline (via the multiplexer **164**, the multiplexer **170**, the pipeline stage **166** and the pipeline stage **168** and then read on the occurrence of a particular event (e.g., a transition of the signal ADDR_REQ (@SYSCLK)). The pipeline stages **166** and **168** may be written to when the queue address ADDRESS is valid via the signal ADDR_VALID. The pipeline stage **172** may be written to when the signal ADDR_REQ(@SYSCLK) is valid (e.g., when the controller **156** is ready to take a next address value). Additional pipeline stages may be added if the queue address information (e.g., the signal ADDRESS and the signal ADDR_VALID) need to be further processed before passing the queue address ADDRESS to the controller **156** for physical address computation.

A required pipeline depth of the circuit **152** (via the pipeline stages **166**, **168** and/or **172**) may be calculated as follows:

if "T" represents the total cycle time between an internal event (e.g., the queue address request signal ADDR_REQ before synchronization and the time when the queue address ADDRESS is available after synchronization) and "P" is the minimum size of the packet in terms of cycles, then the required pipeline depth is given by the following equation:

$$T/P \leqq \text{Pipeline Depth.}$$

So, the pipeline depth may indicate how many queue addresses need to be stored in order to provide back-to-back reads of variable size packets. For example, if the value T (total cycle time) is 11 system clock cycles and the value P (minimum packet size allowed) is 4 cycles, a maximum of 3 (e.g., 11/4) stages of pipelining may be required. The value T may include a round-time synchronization delay and a maximum time taken by the queue scheduler **105** to generate and send the queue address ADDRESS in response to the address request signal ADDR_REQ. The pipeline stages **166**, **168** and/or **172** may be variable to allow bypassing of the pipeline stages when not required, reducing latency on the address path.

The clock synchronization logic **162** may be bypassed (via the signal CTR) when the interface and system clocks are similar in phase and frequency. The synchronized queue select address (e.g., the signal ADDRESS(@SYSCLK)) is passed either directly to the pipeline stage **172**, or through the pipeline stage **166** if the pipeline stage **172** still contains a valid address, or through the pipeline stage **168**, if the pipeline stage **166** is full. The address ADDRESS (@SYSCLK) is then read when the controller **156** is ready to read the next packet in response to the signal ADDR_REQ(@SYSCLK). The queue address ADDRESS is typically read when the end of a previous packet read is detected, or the first packet has to be read (to be described in connection with FIG. **6**).

Referring to FIG. **6**, block diagram showing an implementation of the controller **156** involving generation of the physical address PHY_ADDR and address request ADDR_REQ generation is shown. The controller **156** generally comprises a generator block (or circuit) **180**, a register block (or circuit) **182** and a generator block (or circuit) **184**. The queue address ADDRESS is registered at the register **182** to prevent the address ADDRESS from changing while reading a current packet. The address ADDRESS is generally then sent to the address generator **184** which computes a physical address (e.g., the signal PHY_ADDR) for reading the packet from the memory **158**. The signal ADDR_

REQ is also computed based on end of packet information (e.g., EOP), or if a packet (e.g., FIRST_PKT) needs to be transferred. The packet FIRST_PKT may be internally generated.

The queue address request signal ADDR_REQ is generally internally generated on an occurrence of an event. In one example, the event may be an early detection of an end of packet (via the signal EOP) while reading from the internal memory or when the first packet transfer needs to occur (via the signal FIRST_PKT). The event may trigger a request for the next queue address. The signal ADDR_REQ may be synchronized with respect to a read clock (e.g., the interface clock INFCLK) and presented to the queue scheduler **105**. The queue scheduler **105** may require a predetermined number of cycles to return an address (e.g., the queue address ADDRESS). For example, synchronization may take 1–4 cycles after detecting the synchronized request signal (e.g., the signal ADDR_REQ).

Referring to FIG. **7**, a timing diagram **190** illustrating requirements of internal pipelining of queue addresses, in order to have back-to-back reads of variable size packets is shown. The timing diagram **190** may illustrate example timings demonstrating why the pipelining stages **166**, **168** and/or **172** are required to store extra queue select addresses. The timing diagram **140** may illustrate a case where a sequence of smaller sized packets **192***a*–**192***n* (4 cycles as in the diagram) is followed by a long packet **194**. In such a case, the internal pipeline may be frozen after processing the last small packet **192***n*. The last few small packets may result in a similar sequence of the next queue addresses. Because of a larger round-time delay (due to synchronization, and delay due to address validation), the new queue addresses need to be stored. The stored queue addresses may be used at an end of the long packet **194**. If the long packet **194** ended after the second new queue address has arrived (as indicated in the timing diagram **190**), storage of 2 new queue select addresses instead of 3 queue addresses may be required with respect to the timing diagram **190**.

Referring to FIG. **8**, a flow diagram of a method (or process) **200** illustrating the interaction of the various signals of the circuit **100** is shown. The process **200** generally has a state **202**, a state **204**, a decision state **206**, a decision state **208**, a state **210**, a state **212**, a state **214**, a decision state **216**, a state **218** and a decision state **220**. The state **202** generally begins the process **200**. Next, the state **204** asserts the signal ADDR_REQ. The decision state **206** then determines if the signal ADDR_VALID is active (e.g., ON, or a digital "1"). If the signal ADDR_VALID is not active (e.g., OFF, or a digital "0"), the process **200** returns to the state **204**. If the signal ADDR_VALID is active, the process **200** continues to the decision state **208**. If the decision state **208** determines that valid read data is not available, the state **210** waits until valid read data is available and returns to the state **208**. If the state **208** determines that valid read data is available, the state **214** asserts (e.g., turns on) the signal DATA_VALID and initiates a read of a memory location. Next, if the state **216** determines that the signal READ_EN is not valid (e.g., enabled), the state **218** waits one or more clock cycles and returns to the state **216**. If the state **216** determines that the signal READ_EN is valid, the state **220** then determines if an end of packet is detected. If an end of packet is not detected, the process **200** returns to the state **214**. If an end of packet is detected, the process **200** returns to the state **204**.

The queue address signal ADDRESS is registered to be a valid transfer only if the request for next queue address has been activated and the queue address valid signal ADDR_VALID is also activated at the time the address is supposed to have been received. The queue address signal ADDRESS passes through internal pipeline stages before the data is read out from the memory **158**. When data is detected as valid data, the read data valid signal DATA_VALID is activated to indicate that the data on the read data bus is valid. The memory read of the packet continues, until an end of packet is detected. When an end of packet EOP is detected, the next address request is generated, and the process **200** continues. A pause may be implemented by deactivating the signal READ_EN (e.g., the memory read may be paused while the signal READ_EN is deactivated).

Referring to FIG. **9**, a method (or process) **300** for generation of next queue address request signal ADDR_REQ is shown. The method **300** generally comprises a start state **302**, a decision state **304**, a decision state **306**, a decision state **308**, a state **310**, a decision state **312** and a state **314**. The state **302** generally starts the method **300**. The state **304** determines if the memory **158** is empty, and if so, the method **300** returns to the state **304**. In one example, one or more clock cycles may pass before the state **304** checks the status of the memory **158**. The particular number of clock cycles may be adjusted accordingly to meet the design criteria of a particular implementation. In one example, the number of clock cycles may be programmed. In such an example, if the state **304** determines that the memory **158** is empty, the process **300** would first retreat to the state **302** before reducing the status of the memory **158**.

If the decision state **304** determines that the memory is not empty, the state **306** then determines if a valid queue address is available. If a valid queue address is not available, the method **300** moves to the state **314** where the signal ADDR_REQ is asserted. If a valid queue address is available, the decision state **308** determines if the queue is empty. If the queue is empty, the method **300** returns to the state **304**. If the queue is not empty, the state **310** reads from the memory **158**. Next, the decision state **312** determines if an end of packet is detected. If an end of packet is not detected, the method **300** returns to the state **310** and waits until the end of packet EOP is detected. If an end of packet is detected, the state **314** asserts the signal ADDR_REQ.

The start state **302** begins when the memory **158** is non-empty. The queue address is registered depending on the status of the signal ADDR_VALID. If the signal ADDR_VALID is not valid and the memory **158** is non-empty, the queue address request signal ADDR_REQ continues to be generated until a queue address value is registered. The loop in the state **304** may also help in initiating the address request signal ADDR_REQ. The signal ADDR_REQ may be generated first when the packet FIRST_PKT is ready to be read. The address starts the packet read from the memory **158**. If the queue is found to be empty, the process restarts, and no packet read takes place. When an end of packet occurs, the next queue address request is generated and the process restarts again.

The present invention may provide a method for exchanging address and data signals between the external read device **104** and the multiqueue storage element **102**. The multiqueue storage element **102** is generally responsible for generating an address request that may be presented to the external read device **104**. The external read device **104** may generate a valid queue address (e.g., the signal ADDR_VALID) in response to an address request (e.g., the signal ADDR_REQ). The multiqueue storage device **102** may then provide valid data (e.g., the signal DATA_VALID and the signal DATA), in response to the valid queue address. The multiqueue storage element **102** and the read device **104**

may be in a single clock domain or different clock domains. Data exchange between the multiqueue storage device **102** and the read interface **104** may be of variable packet sizes. The latency between the address request signal ADDR_REQ and the address valid signal ADDR_VALID may be varied. The latency between the address valid signal ADDR_VALID and the data valid signal DATA_VALID may be varied. The present invention may allow back-to-back reads of variable size data packets. Additionally, the present invention may provide a logic for controlling the flow of information in a two clock system having variable size data packet handling capacity.

The present invention may handle any data packet size, without losing bandwidth. For example, latency of the circuit **100** may vary due to a particular configuration (e.g., read clock, if it is not same as system clock or when width/depth expansion is supported). However, the queue scheduler **105** may not be responsible for generating the queue addresses according to the particular configuration. Therefore, the read device **104** (e.g., the queue scheduler **105**) may not need to be informed of the configuration of the multiqueue FIFO **102**. Thus, slower read clocks may be used. Although there may be an uncertainty with the latency of the circuit **100** when the read interface clock INFCLK is a slower clock, the read device **104** may synchronize the signal DATA with the queue address ADDRESS with the read data valid signal DATA_VALID.

The function performed by the flow diagrams of FIGS. **8–9** may be implemented using a conventional general purpose digital computer programmed according to the teachings of the present specification, as will be apparent to those skilled in the relevant art(s). Appropriate software coding can readily be prepared by skilled programmers based on the teachings of the present disclosure, as will also be apparent to those skilled in the relevant art(s).

The present invention may also be implemented by the preparation of ASICs, FPGAs, or by interconnecting an appropriate network of conventional component circuits, as is described herein, modifications of which will be readily apparent to those skilled in the art(s).

The present invention thus may also include a computer product which may be a storage medium including instructions which can be used to program a computer to perform a process in accordance with the present invention. The storage medium can include, but is not limited to, any type of disk including floppy disk, optical disk, CD-ROM, and magneto-optical disks, ROMs, RAMs, EPROMs, EEPROMs, Flash memory, magnetic or optical cards, or any type of media suitable for storing electronic instructions.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. An interface coupled to a multiqueue storage device and configured to interface said multiqueue storage device with one or more handshaking signals, wherein said multiqueue storage device and said interface are configured to transfer variable size data packets and said multiqueue storage device is configured to generate an address request signal.

2. The interface according to claim **1**, wherein said multiqueue storage device and said interface are configured to allow back-to-back reads of said variable size data packets.

3. The interface according to claim **1**, wherein said interface is configured to generate a valid queue address signal in response to said address request signal.

4. The interface according to claim **3**, wherein said multiqueue storage device generates data in response to said valid queue address signal.

5. The interface according to claim **1**, wherein said multiqueue storage device and said interface operate in a single clock domain.

6. The interface according to claim **1**, wherein said multiqueue storage device and said interface operate in a plurality of clock domains.

7. The interface according to claim **1**, wherein a first latency between a first at least one of said one or more handshaking signals is varied.

8. The interface according to claim **7**, wherein a second latency between a second at least one of said one or more handshaking signals is varied.

9. The interface according to claim **1**, wherein said one or more handshaking signals comprise one or more of:

said address request signal;

an address valid signal; and

a data valid signal.

10. The interface according to claim **1**, wherein said interface comprises an external read interface and said multiqueue storage device comprises a multiqueue first-in-first-out (FIFO) memory device.

11. An interface comprising:

means for interfacing a multiqueue storage device; and

means for interfacing with one or more handshaking signals, wherein said multiqueue storage device and said interface are configured to allow back-to-back reads of variable size data packets.

12. A method for providing a read protocol, comprising the steps of:

(A) interfacing a multiqueue storage device; and

(B) interfacing with one or more handshaking signals, wherein said multiqueue storage device and said interface are configured to allow back-to-back reads of variable size data packets.

13. The method according to claim **12**, wherein said interface comprises an external read interface and said multiqueue storage device comprises a multiqueue first-in-first-out (FIFO) memory device.

14. The method according to claim **12**, wherein step (B) further comprises:

generating an address request signal.

15. The method according to claim **14**, wherein step (A) further comprises:

generating a valid data signal in response to a valid queue address signal.

16. The method according to claim **13**, further comprising the step of:

operating in a single clock domain or a plurality of clock domains.

17. The method according to claim **12**, further comprising the step of:

providing a varying latency between at least one of said one or more handshaking signals.

18. An interface coupled to a multiqueue storage device and configured to interface said multiqueue storage device with one or more handshaking signals, wherein said multiqueue storage device and said interface are configured to allow back-to-back reads of variable size data packets.

19. A method for providing a read protocol, comprising the steps of:

(A) interfacing with a multiqueue storage device; and

(B) interfacing with one or more handshaking signals and generating an address request signal, wherein said multiqueue storage device and said interfacing are configured to allow variable size data packets.

* * * * *

EXHIBIT C

US006651134B1

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Phelan

(10) **Patent No.: US 6,651,134 B1**
(45) **Date of Patent: Nov. 18, 2003**

(54) **MEMORY DEVICE WITH FIXED LENGTH NON INTERRUPTIBLE BURST**

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(73) Assignee: **Cypress Semiconductor Corp.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/504,344**

(22) Filed: **Feb. 14, 2000**

(51) **Int. Cl.**[7] **C06F 12/00**

(52) **U.S. Cl.** **711/104**; 711/105; 711/167; 711/169; 710/35; 365/233; 365/238.5

(58) **Field of Search** 711/104–105, 169, 711/167; 365/233, 238.5; 710/35

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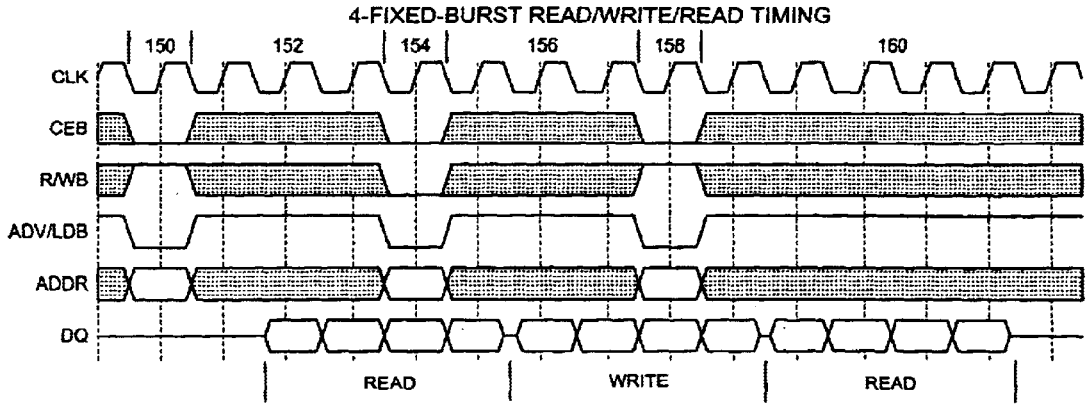
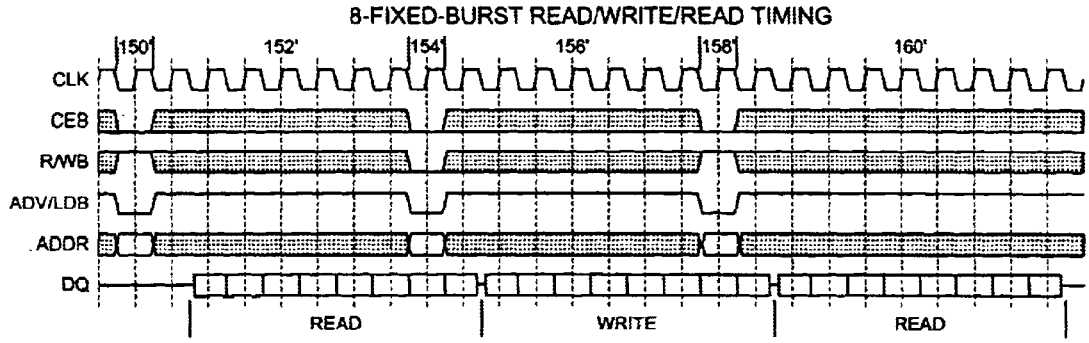
Primary Examiner—Donald Sparks
Assistant Examiner—Medhi Namazi
(74) *Attorney, Agent, or Firm*—Christopher P. Maiorana, P.C.; Robert M. Miller

(57) **ABSTRACT**

An integrated circuit comprising a memory and a logic circuit. The memory may comprise a plurality of storage elements each configured to read and write data in response to an internal address signal. The logic circuit may be configured to generate a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals. The generation of the predetermined number of internal address signals may be non-interruptible.

21 Claims, 3 Drawing Sheets





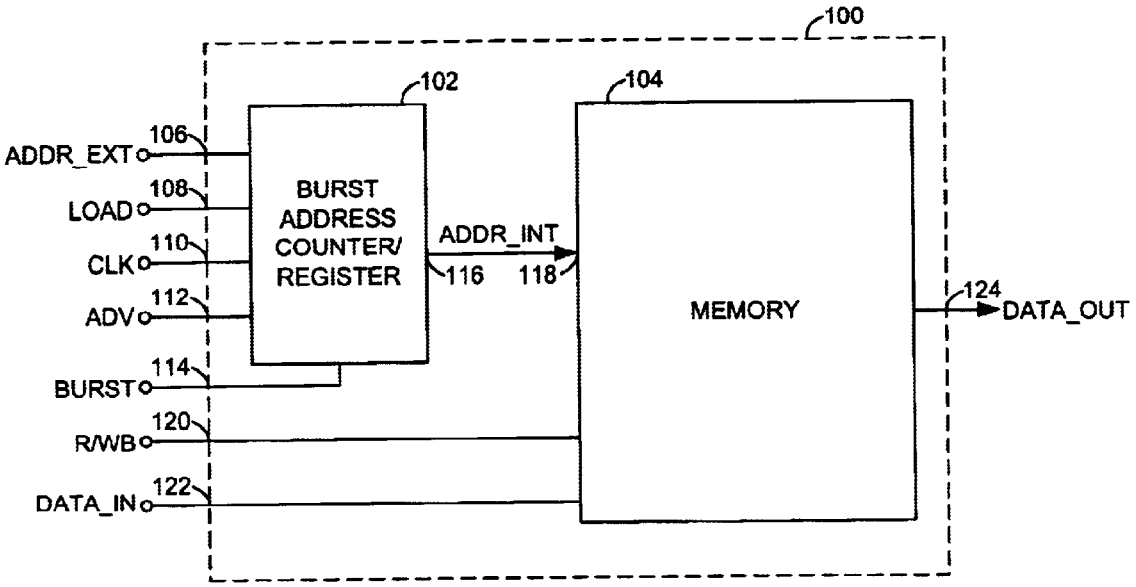

100
102
104
ADDR_EXT
106
LOAD
108
CLK
110
ADV
112
BURST
114
R/WB
120
DATA_IN
122
BURST ADDRESS COUNTER/ REGISTER
ADDR_INT
116
118
MEMORY
124
DATA_OUT

FIG. 1

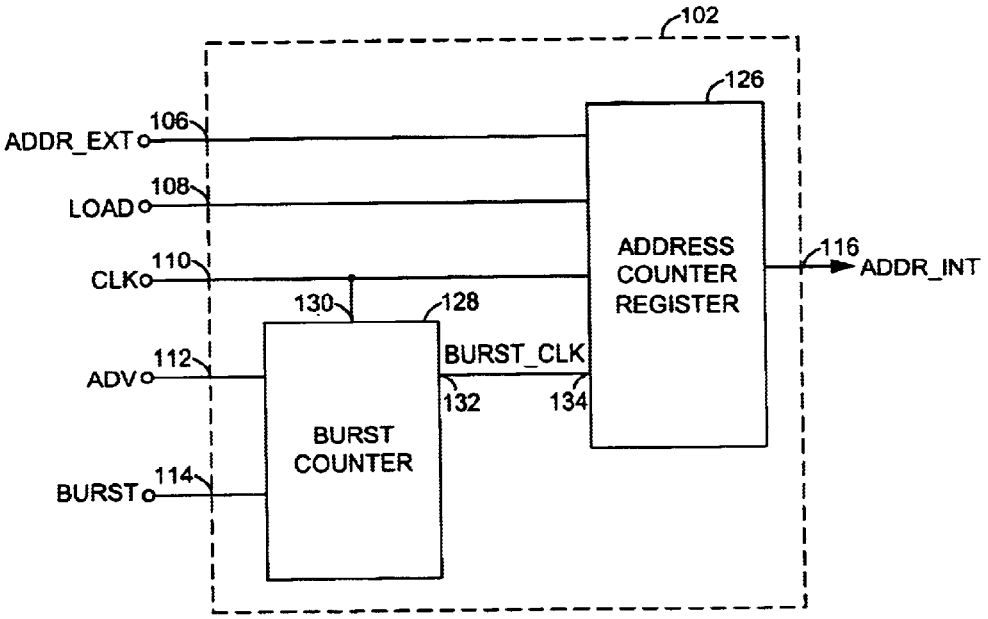

102
126
ADDR_EXT
106
LOAD
108
CLK
110
ADV
112
BURST
114
130
128
BURST_CLK
132
134
BURST COUNTER
ADDRESS COUNTER REGISTER
116
ADDR_INT

FIG. 2

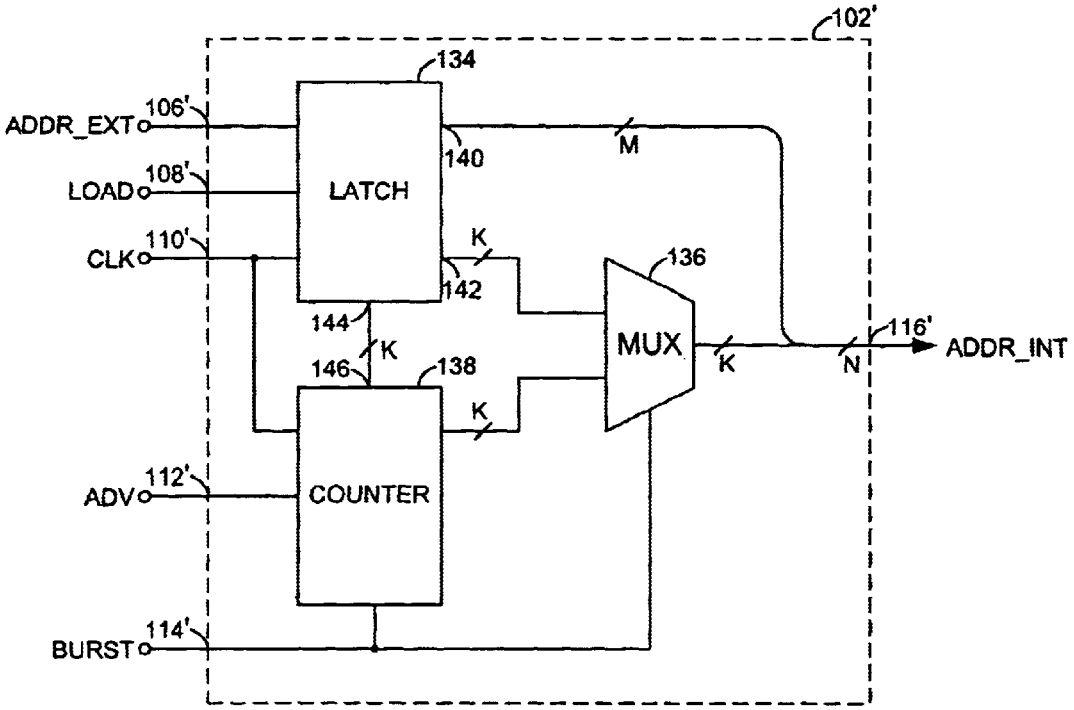

102'
134
ADDR_EXT
106'
LOAD
108'
CLK
110'
LATCH
140
M
K
142
136
144
K
146
138
MUX
K
N
116'
ADDR_INT
K
ADV
112'
COUNTER
BURST
114'

FIG. 3

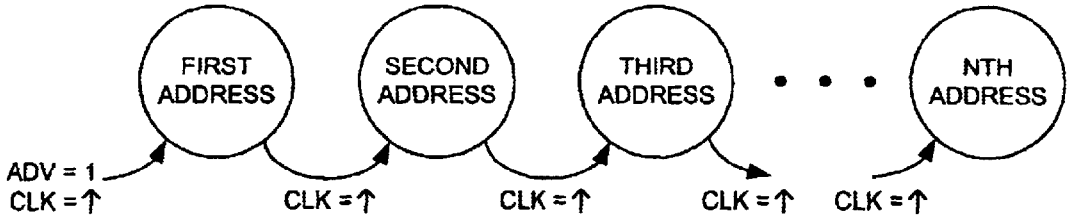

FIRST ADDRESS
SECOND ADDRESS
THIRD ADDRESS
NTH ADDRESS
ADV = 1
CLK = ↑
CLK = ↑
CLK = ↑
CLK = ↑
CLK = ↑

FIG. 4

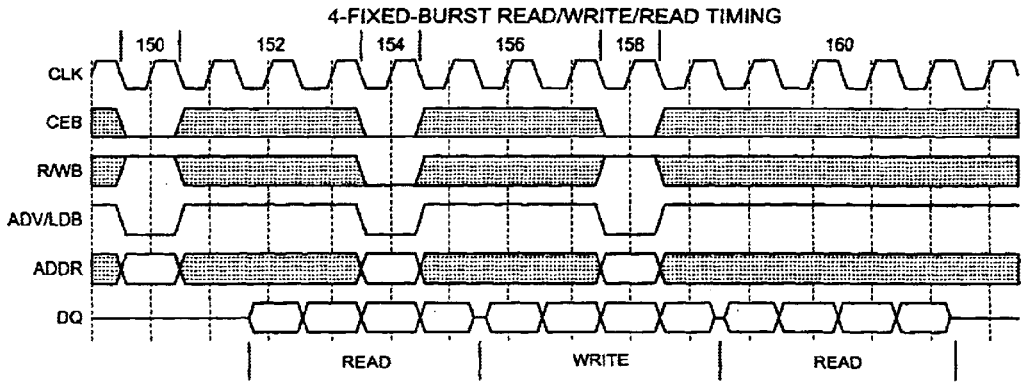


FIG. 5A

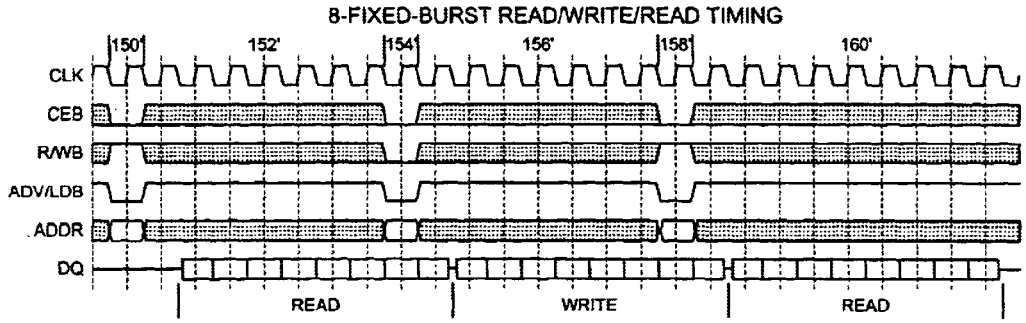


FIG. 5B

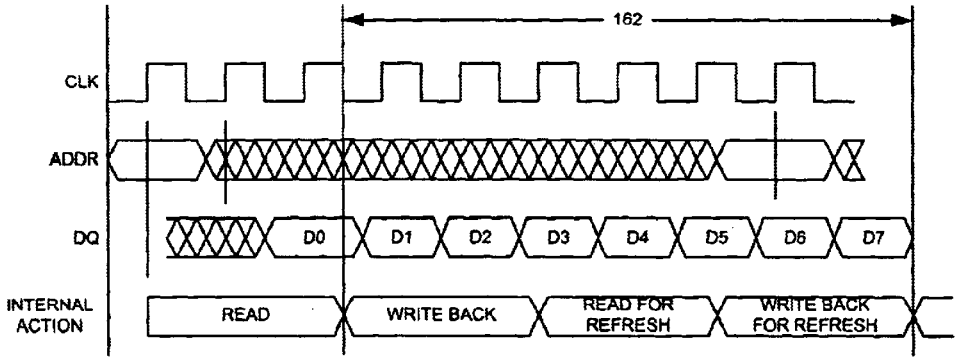


FIG. 6

MEMORY DEVICE WITH FIXED LENGTH NON INTERRUPTIBLE BURST

FIELD OF THE INVENTION

The present invention relates to memory devices generally and, more particularly, to a memory device that transfers a fixed number of words of data with each access.

BACKGROUND OF THE INVENTION

A synchronous Static Random Access Memory (SRAM) can provide data from multiple address locations using a single address. Accessing multiple locations in response to a single address is called a burst mode access. A memory device that provides a burst mode can reduce activity on the address and control buses. The burst mode of a conventional synchronous SRAM can be started and stopped in response to a control signal.

A conventional Dynamic Random Access Memory (DRAM) preserves data during periodic absences of power by implementing a memory cell as a capacitor and an access transistor. Since the charge on the capacitor will slowly leak away, the cells need to be "refreshed" once every few milliseconds. Depending on the frequency of accesses, a conventional DRAM can need an interrupt to perform data refreshes. Using a DRAM in a burst application is difficult because of the need to refresh. Completely hiding refresh cycles (e.g., refreshing data without the need for interrupts) in a DRAM cannot happen with conventional memory devices due to architecture choices that have been made. Data word bursts can be interrupted while in progress since conventional architectures support both burst and single access modes. Conventional DRAM access takes about 10 ns to get data, but nearly 20 ns to complete writeback and equalization. The addition of another 20 ns for a refresh results in a total access of 40 ns.

Since the data burst transfers of conventional memories can be interrupted and single accesses made, the amount of time that the data, address and control busses are not in use can vary. The variability of bus availability complicates the design of systems with shared data, address and control busses.

It would be desirable to have a memory device that has a fixed burst length.

SUMMARY OF THE INVENTION

The present invention concerns an integrated circuit comprising a memory and a logic circuit. The memory may comprise a plurality of storage elements each configured to read and write data in response to an internal address signal. The logic circuit may be configured to generate a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals. The generation of the predetermined number of internal address signals may be non-interruptible.

The objects, features and advantages of the present invention include providing a fixed burst memory that may (i) give network customers who typically burst large data lengths the ability to set a fixed burst length that suits particular needs; (ii) have non-interruptible bursts; (iii) free up the address bus and control bus for a number of cycles; (iv) provide programmability for setting the burst length by using DC levels [Vss or Vcc] on external pins; (v) hide required DRAM refreshes inside a known fixed burst length of data words; and/or (vi) operate at higher frequencies without needing interrupts to perform refreshes of data.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects, features and advantages of the present invention will be apparent from the following detailed description and the appended claims and drawings in which:

FIG. **1** is a block diagram illustrating a preferred embodiment of the present invention;

FIG. **2** is a detailed block diagram illustrating a circuit **102** of FIG. **1**;

FIG. **3** is a detailed block diagram of a circuit **102'** illustrating an alternative embodiment of the circuit **102** of FIG. **1**;

FIG. **4** is a flow diagram illustrating an example burst address sequence;

FIGS. **5**A and **5**B are diagrams illustrating example operations of a 4 word (FIG. **5**A) and an 8 word (FIG. **5**B) fixed burst access in accordance with the present invention; and

FIG. **6** is a diagram illustrating an example operation where a burst length may be long enough to include a writeback and a refresh cycle.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. **1**, a block diagram of a circuit **100** is shown in accordance with a preferred embodiment of the present invention. The circuit **100** may be implemented, in one example, as a fixed burst memory. The circuit **100** may be configured to transfer a fixed number of words of data with each access (e.g., read or write). A number of words transferred as a group is called a burst. The circuit **100** generally comprises a circuit **102** and a memory array (or circuit) **104**. The circuit **102** may be implemented, in one example, as a burst address counter/register. The memory array **104** may be implemented, in one example, as a static random access memory (SRAM), a dynamic random access memory (DRAM), or other appropriate memory to meet the design criteria of a particular implementation.

The circuit **102** may have an input **106** that may receive a signal (e.g., ADDR_EXT), an input **108** that may receive a signal (e.g., LOAD), an input **110** that may receive a signal (e.g., CLK), an input **112** that may receive a signal (e.g., ADV), and an input **114** that may receive a signal (e.g., BURST). The circuit **102** may have an output **116** that may present a signal (e.g., ADDR_INT) to an input **118** of the memory **104**. The memory **104** may have an input **120** that may receive a signal (e.g., R/Wb), an input **122** that may receive a signal (e.g., DATA_IN) and an output **122** that may present a signal (e.g., DATA_OUT). The various signals are generally "on" (e.g., a digital HIGH, or 1) or "off" (e.g., a digital LOW, or 0). However, the particular polarities of the on (e.g., asserted) and off (e.g., de-asserted) states of the signals may be adjusted (e.g., reversed) accordingly to meet the design criteria of a particular implementation.

The signal ADDR_EXT may be, in one example, an external address signal. The signal ADDR_EXT may be n-bits wide, where n is an integer. The signal CLK may be a clock signal. The signal R/Wb may be a control signal that may be in a first state or a second state. When the signal R/Wb is in the first state, the circuit **100** will generally read data from the memory circuit **104** for presentation as the signal DATA_OUT. When the signal R/Wb is in the second state, the circuit **100** will generally store data received as the signal DATA_IN.

The signal LOAD may be, in one example, an address load control signal. The circuit **100** may be configured to

load an initial address, presented by the signal ADDR_EXT, in response to the signal LOAD. The initial address may determine the initial location where data transfers to and from the memory **104** will generally begin.

The signal ADV may be, in one example, used as a control signal. The circuit **100** may be configured to transfer a fixed number of words to or from the memory **104** in response to the signals ADV, CLK and R/Wb. When the signal ADV is asserted, the circuit **100** will generally begin transferring a predetermined number of words. The transfer is generally non-interruptible. In one example, the signal ADV may initiate the generation of a number of addresses for presentation as the signal ADDR_INT.

The signals ADV and LOAD may be, in one example, a single signal (e.g., ADV/LDb). The signal ADV/LDb may be a control signal that may be in a first state or a second state. When the signal ADV/LDb is in the first state, the circuit **102** will generally load an address presented by the signal ADDR_EXT as an initial address. When the signal ADV/LDb is in the second state, the circuit **102** may be configured to generate the signal ADDR_INT as a fixed number of addresses in response to the signal CLK. The signal ADDR_INT may be, in one example, an internal address signal. The signal ADDR_INT may be n-bits wide. Once the circuit **102** has started generating the fixed number of addresses, the circuit **102** will generally not stop until the fixed number of addresses has been generated (e.g., a non-interruptible burst).

The signal BURST may be, in one example, a configuration signal for programming the fixed number of addresses that the circuit **102** may generate in response to the signals CLK and ADV/LDb. The signal BURST may be generated, in one example, by (i) using bond options, (ii) voltage levels applied to external pins, or (iii) other appropriate signal generation means.

When the memory **104** is implemented as a DRAM, the circuit **100** may be configured to hide required DRAM refreshes (e.g., refreshes may occur without affecting external environment) inside a known fixed burst length of data words. The fixed burst length may allow the circuit **100** to operate at higher frequencies than a conventional DRAM without needing interrupts to perform refreshes of data. In one example, the fixed burst length may be four or eight words. However, the burst length may be set to whatever length is necessary to meet the design criteria of a particular application. For example, the burst length may be programmed, in one example, to allow both writeback and refresh to occur within a single access. The fixed burst-.length may be set, in one example, longer or shorter depending upon a frequency or technology to be used.

The circuit **100** may be configured to provide a fixed burst length that may suit the requirements of network customers who typically burst large data lengths. By providing a fixed burst length, the circuit **100** may allow shared usage of data, address and control busses. A fixed length non-interruptible burst generally frees up the address bus and control bus for a known number of cycles. The address and control busses may be shared by a number of memory devices. The circuit **100** may provide a more reliable and/or accurate burst than is possible with multiple chips.

Referring to FIG. **2**, a detailed block diagram illustrating implementation of the circuit **102** is shown. The circuit **102** may comprise an address counter register **126** and a burst counter **128**. The address counter register **126** generally receives the signals ADDR_EXT, LOAD, and CLK. The address counter register **126** may be configured to present the signal ADDR_INT. The signal ADV and the signal BURST may be presented to a burst counter **128**. The signal CLK may be presented at an input **130** of the burst counter **128**. The burst counter **128** may have an output **132** that may present a signal (e.g., BURST_CLK) at an input **134** of the circuit **126**. An initial address may be loaded into the address counter register **126** by presenting the initial address in the signal ADDR_EXT and asserting the signal LOAD. The circuit **126** may be configured to increment an address in response to the signal BURST_CLK. When the signal ADV is asserted, the burst counter **128** will generally present the signal BURST_CLK in response to the signal CLK. The signal BURST_CLK generally contains a number of pulses that has been programmed by the signal BURST.

Referring to FIG. **3**, a detailed block diagram illustrating an alternative embodiment of the circuit **102** is shown. The circuit **102'** may comprise a latch **134**, a multiplexer **136** and a counter **138**. The signals ADDR_EXT, LOAD and CLK may be presented to the latch **134**. The latch **134** may have an output **140** that may present a portion (e.g., m bits, where m is an integer smaller than n) of the signal ADDR_EXT as a portion of the signal ADDR_INT, an output **142** that may present a second portion (e.g., k bits, where k is an integer smaller than n) of the signal ADDR_EXT to a first input of the multiplexer **136**, and an output **144** that may present the second portion of the signal ADDR_EXT to an input **146** of the counter **138**.

The signals ADV, CLK and BURST may be presented to inputs of the counter **138**. The counter **138** may be configured to generate a number of addresses in response to the signals CLK, BURST and ADV. The number of addresses generated by the counter **138** may be programmed by the signal BURST.

The signal BURST may be presented to a control input of the multiplexer **136**. The multiplexer **136** may select between a number of signals from the latch **134** and a number of signals from the counter **138** to be presented as a second portion of the signal ADDR_INT in response to the signal BURST.

Referring to FIG. **4**, a flow diagram illustrating an example burst address sequence is shown. When the signal ADV is asserted, the circuit **100** will generally generate a number of address signals, for example, N where N is an integer. The address signals may be generated, in one example, on a rising edge of the signal CLK. The address signals will generally continue to be generated until the Nth address signal is generated.

Referring to FIGS. **5**A and **5**B, timing diagrams illustrating example operations for a four word (FIG. **5**A) and an eight word (FIG. **5**B) fixed burst memory in accordance with the present invention are shown. The timing diagrams generally illustrate externally measurable signals for four and eight word fixed burst read/write architectures. In general, an operation (e.g., read or write) of the circuit **100** begins with loading an initial address (e.g., portions **150**, **154**, and **158** of FIG. **5**A; portions **150'**, **154'**, and **158'** of FIG. **5**B). Starting with the initial address, a fixed number of words are generally transferred (e.g., line DQ of FIGS. **5**A and **5**B). During the transfer of the fixed number of words, the address and control buses (e.g., ADDR, CE, R/W, etc.) are generally available to other devices (e.g., portions **152**, **156**, and **160** of FIG. **5**A; portions **152'**, **156'**, and **160'** of FIG. **5**B). In one example, the control and address bus activity may be one-fourth (FIG. **5**A) or one-eighth (FIG. **5**B) the data bus activity (e.g., compare line ADDR with line DQ of FIGS. **5**A and **5**B). The reduced bus activity may be an effect of the

architecture. The data bus may be, in one example, active nearly 100% of the time (e.g., line DQ of FIGS. **5**A and **5**B) In one example, there may be no inefficiencies switching from read to write to read etcetera (e.g., see labels under line DQ of FIGS. **5**A and **5**B).

Referring to FIG. **6**, a timing diagram illustrating a fixed burst length long enough to hide a writeback and a refresh cycle is shown. Internally the action being performed may completely hide DRAM refresh activity inside nominal external activities. A portion **162** illustrates that refresh activity (e.g., writeback, read for refresh, and writeback for refresh) may be completed within the time of the burst transfer. When a fixed burst long enough to completely hide refresh activity is provided, there may be no penalty for using DRAM instead of SRAM for the memory **104**.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. A circuit comprising:

a memory comprising a plurality of storage elements each configured to read and write data in response to an internal address signal; and

a logic circuit configured to generate a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

2. The circuit according to claim **1**, wherein said predetermined number of internal address signals is determined by a fixed burst length.

3. The circuit according to claim **1**, wherein said predetermined number of internal address signals is at least 4.

4. The circuit according to claim **1**, wherein said predetermined number of internal address signals is 8.

5. The circuit according to claim **2**, wherein said fixed burst length is programmable.

6. The circuit according to claim **5**, wherein said fixed burst length is programmed by bond options.

7. The circuit according to claim **5**, wherein said fixed burst length is programmed by voltage levels on external pins.

8. The circuit according to claim **1**, wherein said memory comprises a static random access memory.

9. The circuit according to claim **1**, wherein said memory comprises a dynamic random access memory.

10. The circuit according to claim **9**, wherein said predetermined number of internal address signals is chosen to provide time for at least one writeback or refresh cycle.

11. The circuit according to claim **1**, wherein said predetermined number of internal address signals is chosen to meet predetermined criteria for sharing address and control busses.

12. The circuit according to claim **1**, wherein said logic circuit comprises a counter configured to generate said predetermined number of internal address signals.

13. The circuit according to claim **1**, wherein said external address signal comprises an initial address for data transfers to and from said memory.

14. A memory device according to claim **1**, wherein said circuit is an integrated circuit.

15. The circuit according to claim **1**, further comprising address and control busses configured to present said external address signal and said one or more control signals, wherein said busses are freed up during the generation of said predetermined number of internal address signals.

16. A circuit comprising:

means for reading data from and writing data to a plurality of storage elements in response to a plurality of internal address signals; and

means for generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

17. A method of providing a fixed burst length data transfer comprising the steps of:

accessing a memory in response to a plurality of internal address signals; and

generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) a control signal, wherein said generation of said predetermined number of internal address signals is non-interruptible.

18. The method according to claim **17**, further comprising the step of programming said predetermined number.

19. The method according to claim **18**, wherein said programming step is performed using bond options.

20. The method according to claim **18**, wherein said programming step is performed using voltage levels.

21. The method according to claim **17**, further comprising the step of selecting said predetermined number to provide time for at least one writeback or refresh cycle.

* * * * *

EXHIBIT D

US006765407B1

(12) **United States Patent**
Snyder

(10) **Patent No.: US 6,765,407 B1**
(45) **Date of Patent: Jul. 20, 2004**

(54) **DIGITAL CONFIGURABLE MACRO ARCHITECTURE**

(75) Inventor: **Warren Snyder**, Snohomish, WA (US)

(73) Assignee: **Cypress Semiconductor Corporation**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/272,231**

(22) Filed: **Oct. 15, 2002**

Related U.S. Application Data

(63) Continuation of application No. 09/909,045, filed on Jul. 18, 2001, now Pat. No. 6,507,214.
(60) Provisional application No. 60/243,708, filed on Oct. 26, 2000.

(51) **Int. Cl.**[7] **H03K 7/38**
(52) **U.S. Cl.** **326/38**; 326/40; 326/37
(58) **Field of Search** 326/37–41

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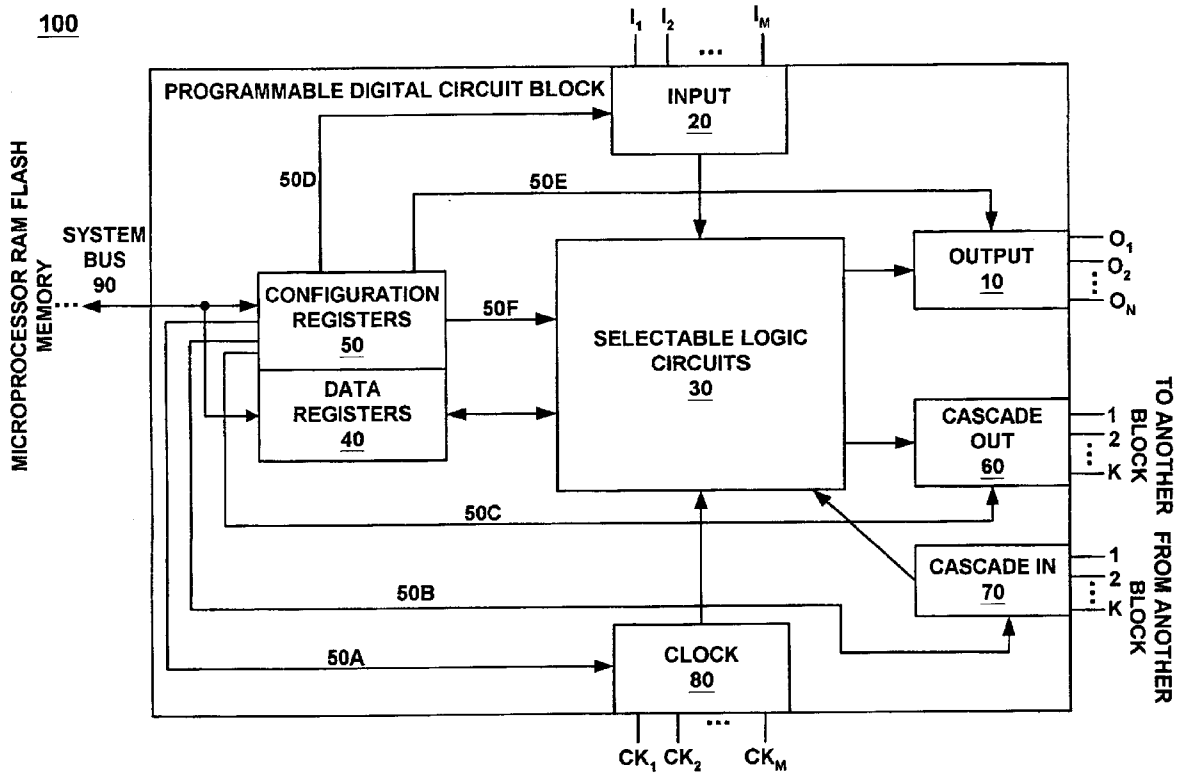
Primary Examiner—Vibol Tan
(74) *Attorney, Agent, or Firm*—Wagner, Murabito & Hao LLP

(57) **ABSTRACT**

A new digital configurable macro architecture is described. The digital configurable macro architecture is well suited for microcontroller or controller designs. In particular, the foundation of the digital configurable macro architecture is a programmable digital circuit block. In an embodiment, programmable digital circuit blocks are 8-bit circuit modules that can be programmed to perform any one of a variety of predetermined digital functions by changing the contents of a few registers therein, unlike a FPGA which is a generic device that can be programmed to perform any arbitrary digital function. Specifically, the circuit components of the programmable digital circuit block are designed for reuse in several of the predetermined digital functions such that to minimize the size of the programmable digital circuit block.

20 Claims, 9 Drawing Sheets



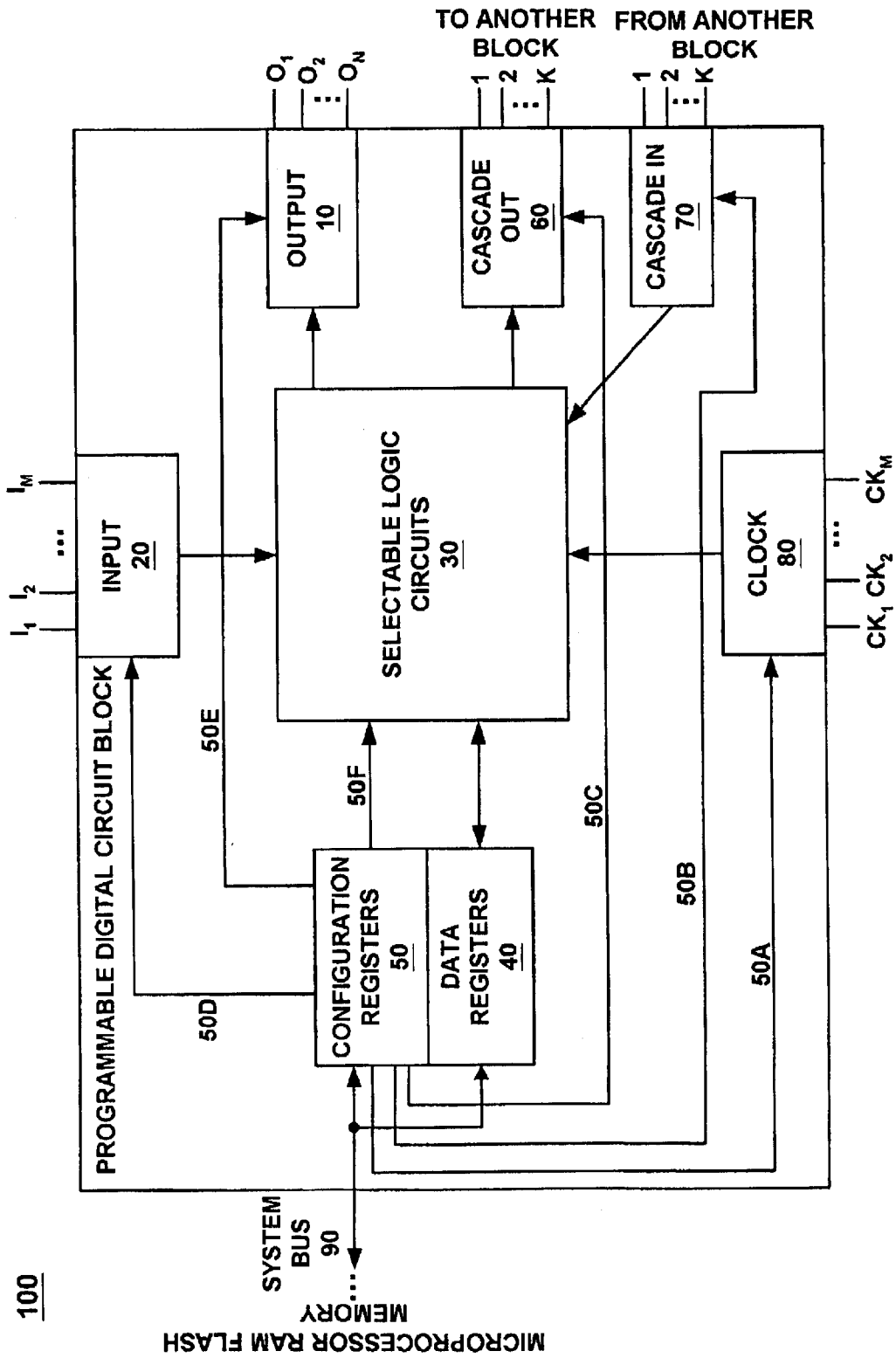

100
MICROPROCESSOR RAM FLASH MEMORY
SYSTEM BUS 90
PROGRAMMABLE DIGITAL CIRCUIT BLOCK
INPUT 20
I_1 I_2 ... I_M
OUTPUT 10
O_1 O_2 ... O_N
CASCADE OUT 60
TO ANOTHER BLOCK
1 2 ... K
CASCADE IN 70
FROM ANOTHER BLOCK
1 2 ... K
SELECTABLE LOGIC CIRCUITS 30
CLOCK 80
CK_1 CK_2 ... CK_M
CONFIGURATION REGISTERS 50
DATA REGISTERS 40
50A
50B
50C
50D
50E
50F

FIGURE 1

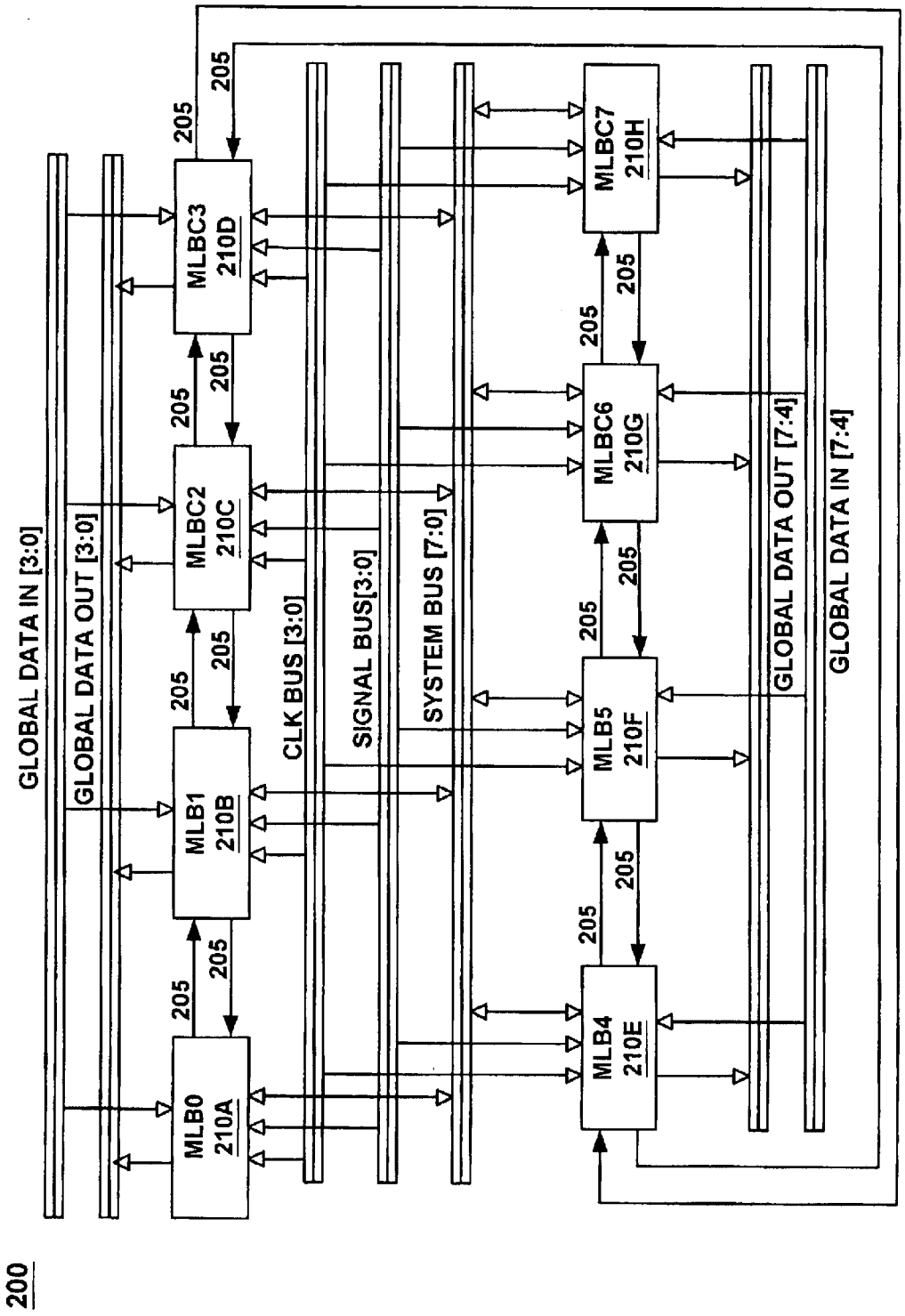

200
GLOBAL DATA IN [3:0]
GLOBAL DATA OUT [3:0]
MLB0 210A
MLB1 210B
MLBC2 210C
MLBC3 210D
MLB4 210E
MLB5 210F
MLBC6 210G
MLBC7 210H
205
CLK BUS [3:0]
SIGNAL BUS[3:0]
SYSTEM BUS [7:0]
GLOBAL DATA OUT [7:4]
GLOBAL DATA IN [7:4]

FIGURE 2

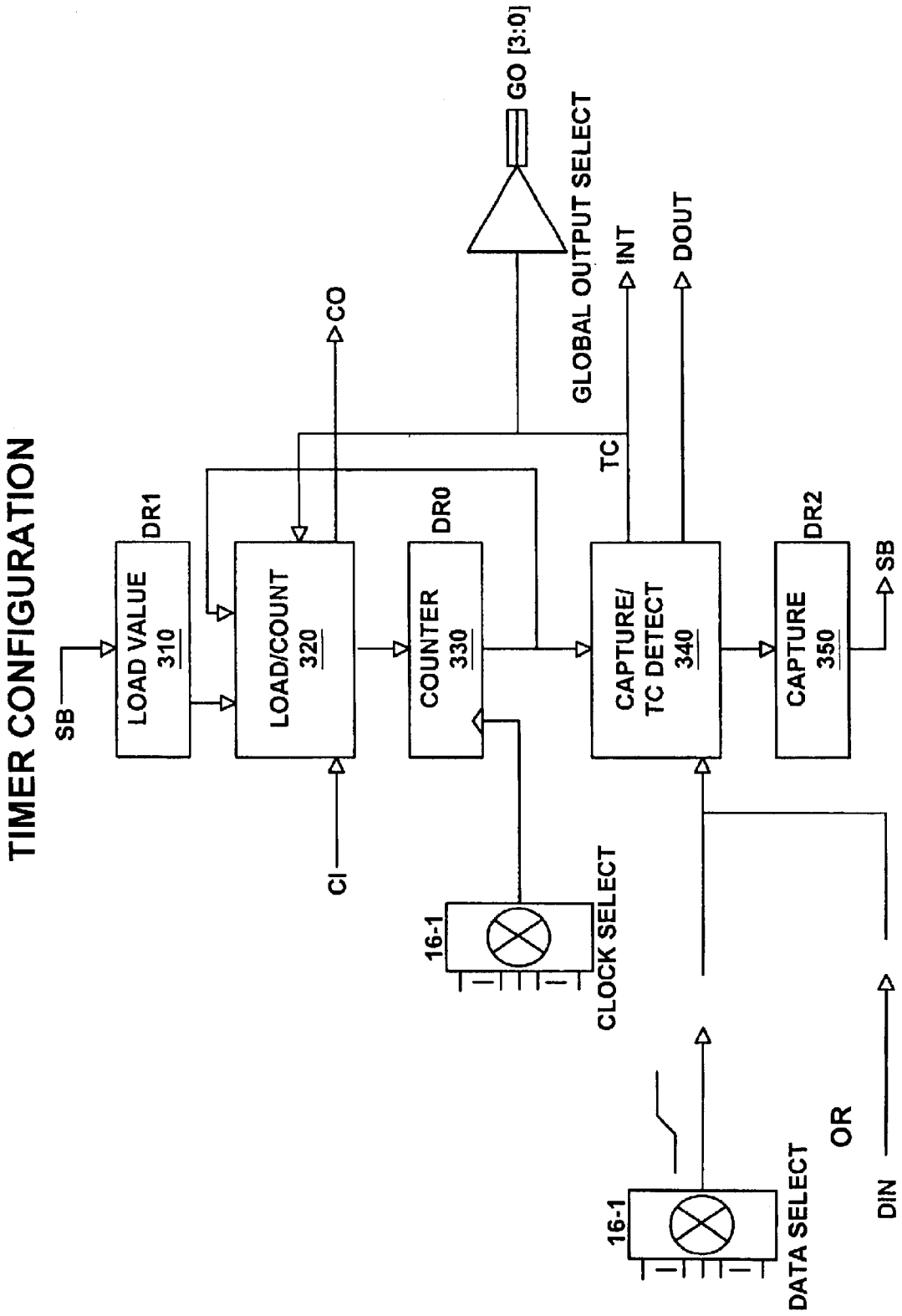

TIMER CONFIGURATION
SB
LOAD VALUE
310
DR1
LOAD/COUNT
320
CI
CO
COUNTER
330
DR0
16-1
CLOCK SELECT
GO [3:0]
GLOBAL OUTPUT SELECT
TC
INT
CAPTURE/
TC DETECT
340
DOUT
16-1
DATA SELECT
OR
DIN
CAPTURE
350
DR2
SB

FIGURE 3

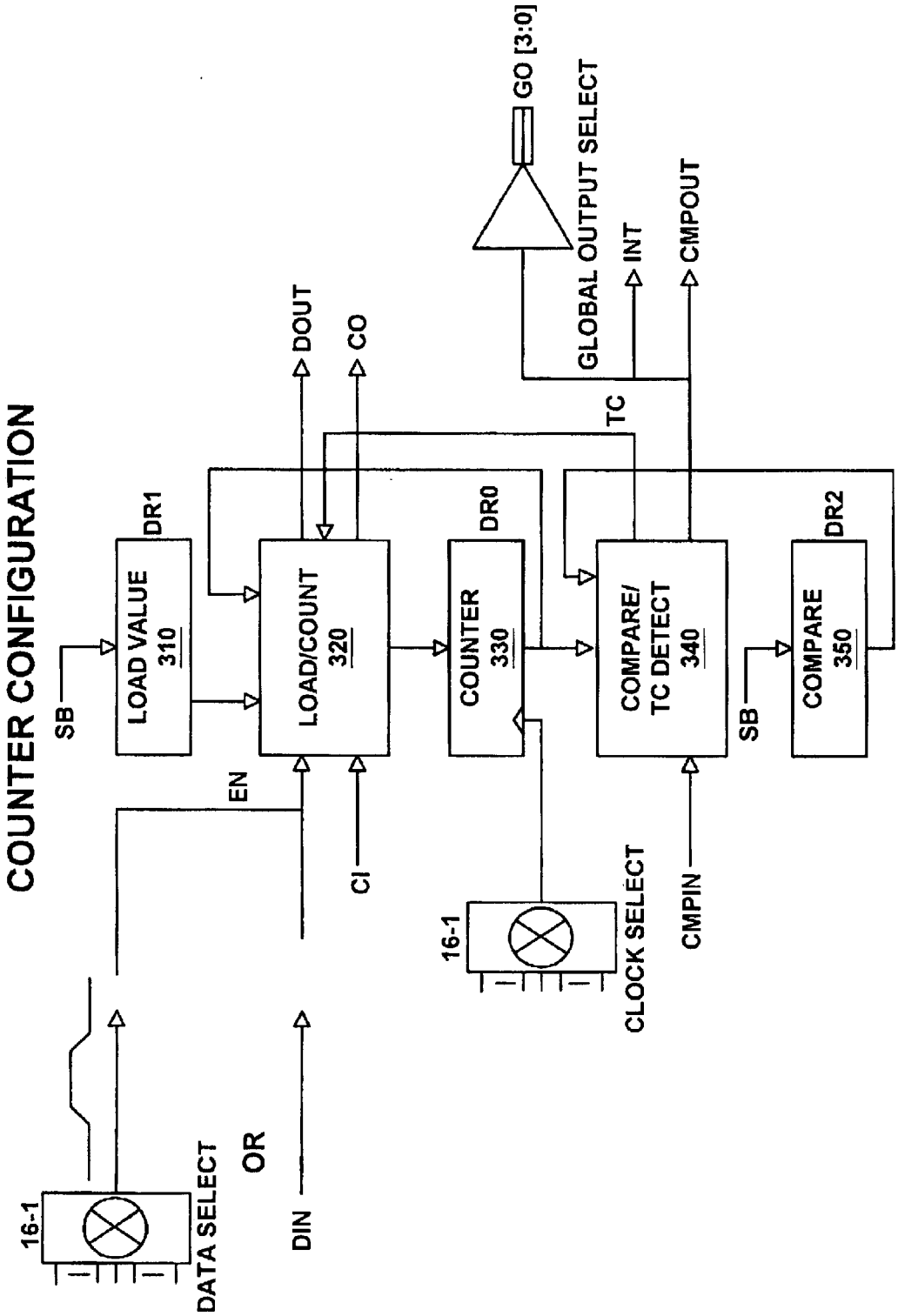

COUNTER CONFIGURATION
SB
LOAD VALUE 310
DR1
LOAD/COUNT 320
DOUT
CO
EN
CI
COUNTER 330
DR0
COMPARE/ TC DETECT 340
TC
GLOBAL OUTPUT SELECT
GO [3:0]
INT
CMPOUT
CLOCK SELECT
16-1
CMPIN
SB
COMPARE 350
DR2
16-1
DATA SELECT
OR
DIN

FIGURE 4

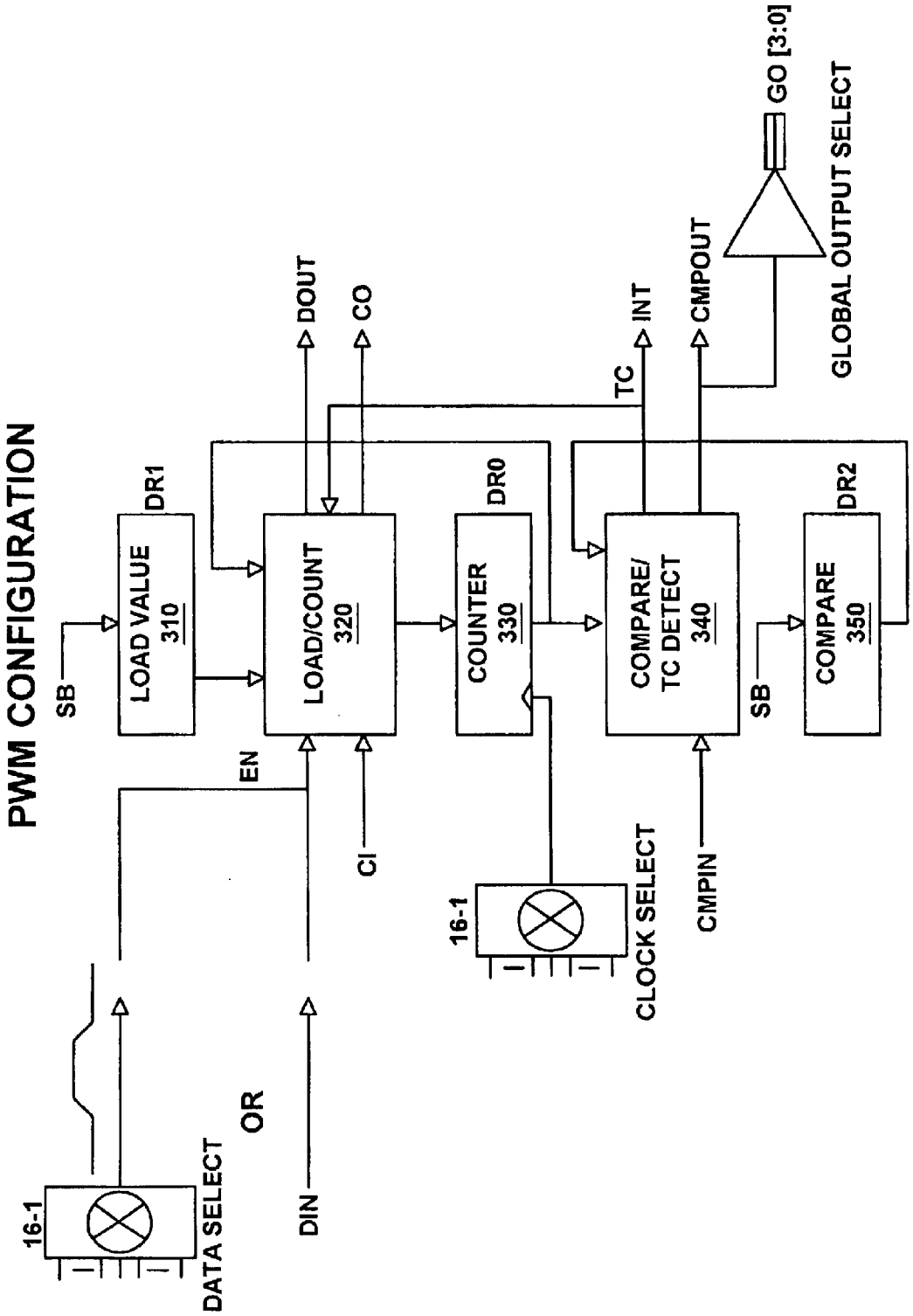

PWM CONFIGURATION
SB
LOAD VALUE 310
DR1
LOAD/COUNT 320
DOUT
CO
EN
CI
COUNTER 330
DR0
16-1
CLOCK SELECT
COMPARE/ TC DETECT 340
TC
INT
CMPOUT
CMPIN
SB
COMPARE 350
DR2
GO [3:0]
GLOBAL OUTPUT SELECT
16-1
DATA SELECT
OR
DIN

FIGURE 5

TX UART CONFIGURATION

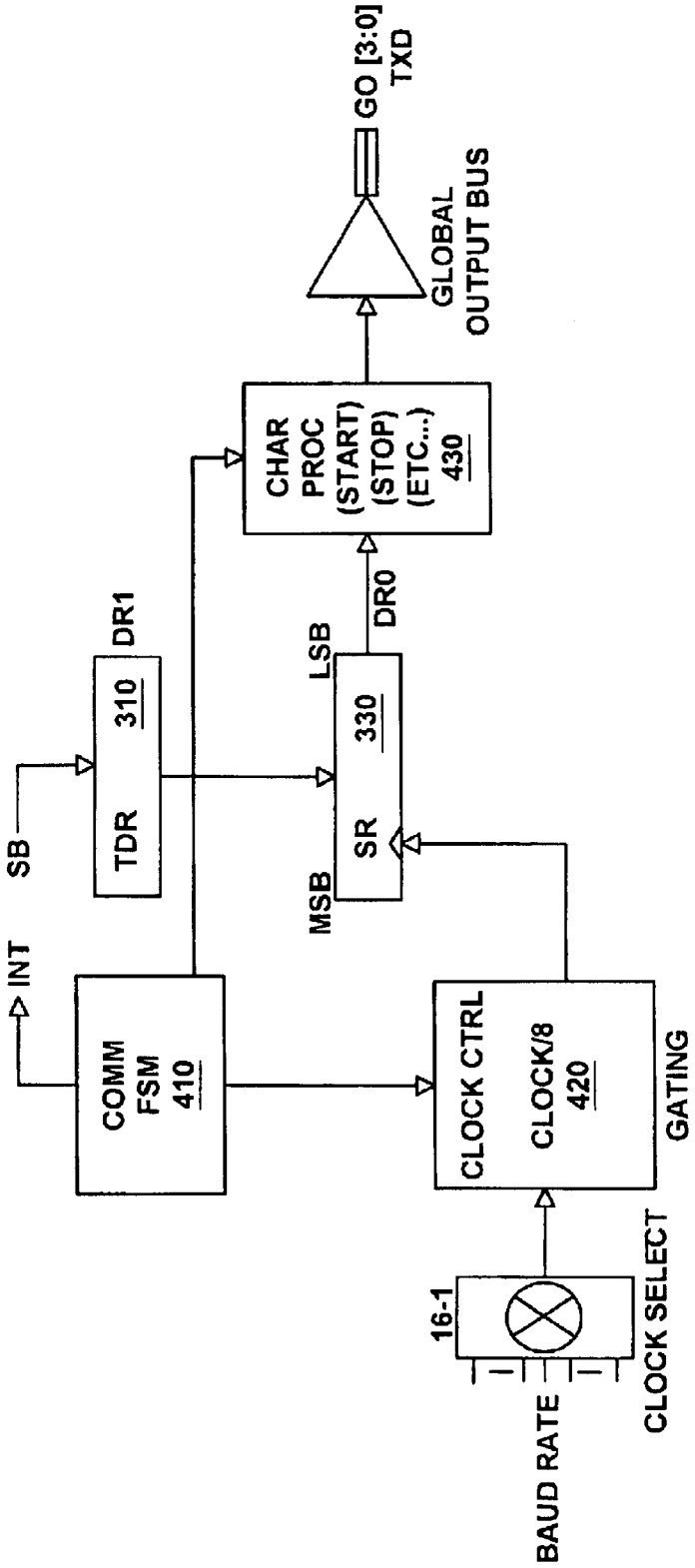


FIGURE 6

RX UART CONFIGURATION

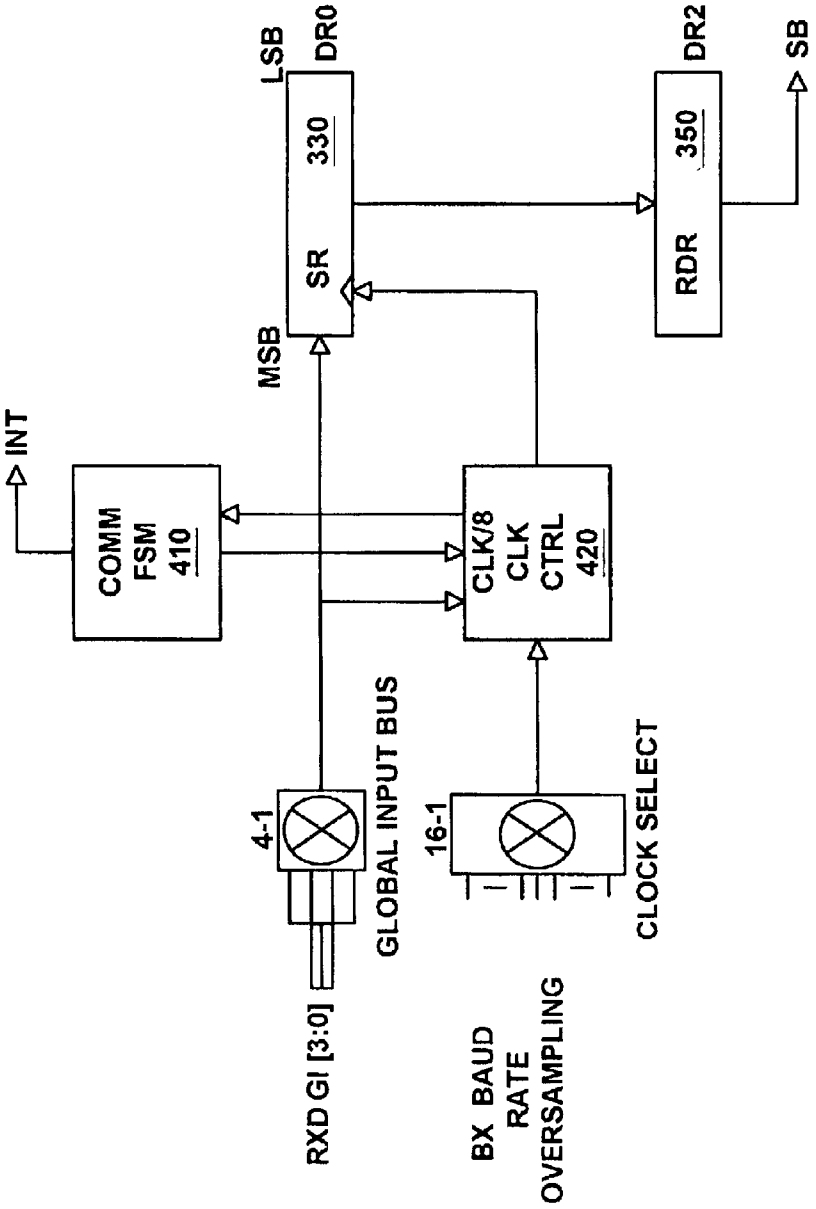


FIGURE 7

SPI MASTER CONFIGURATION

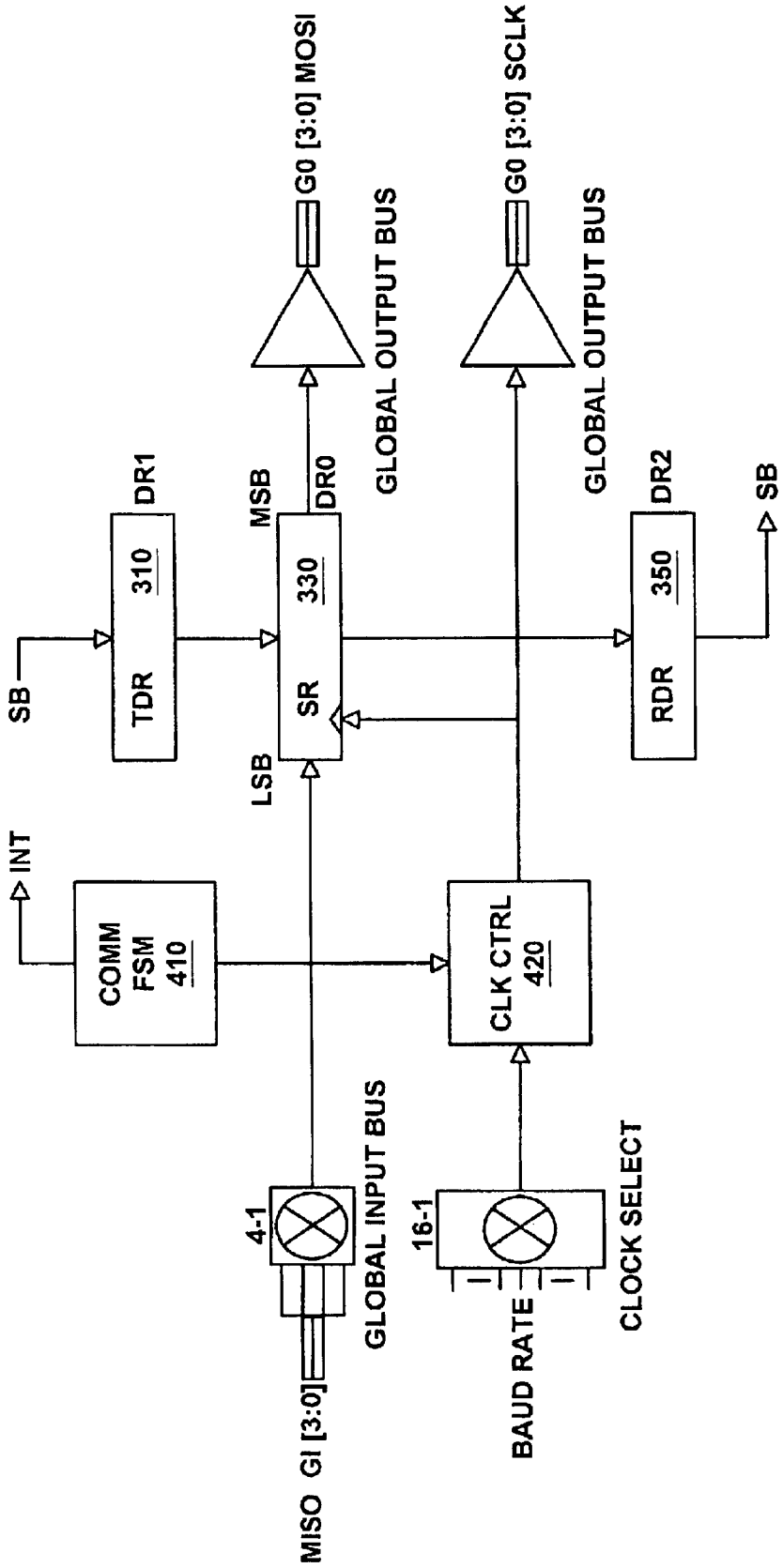


FIGURE 8

SPI SLAVE CONFIGURATION

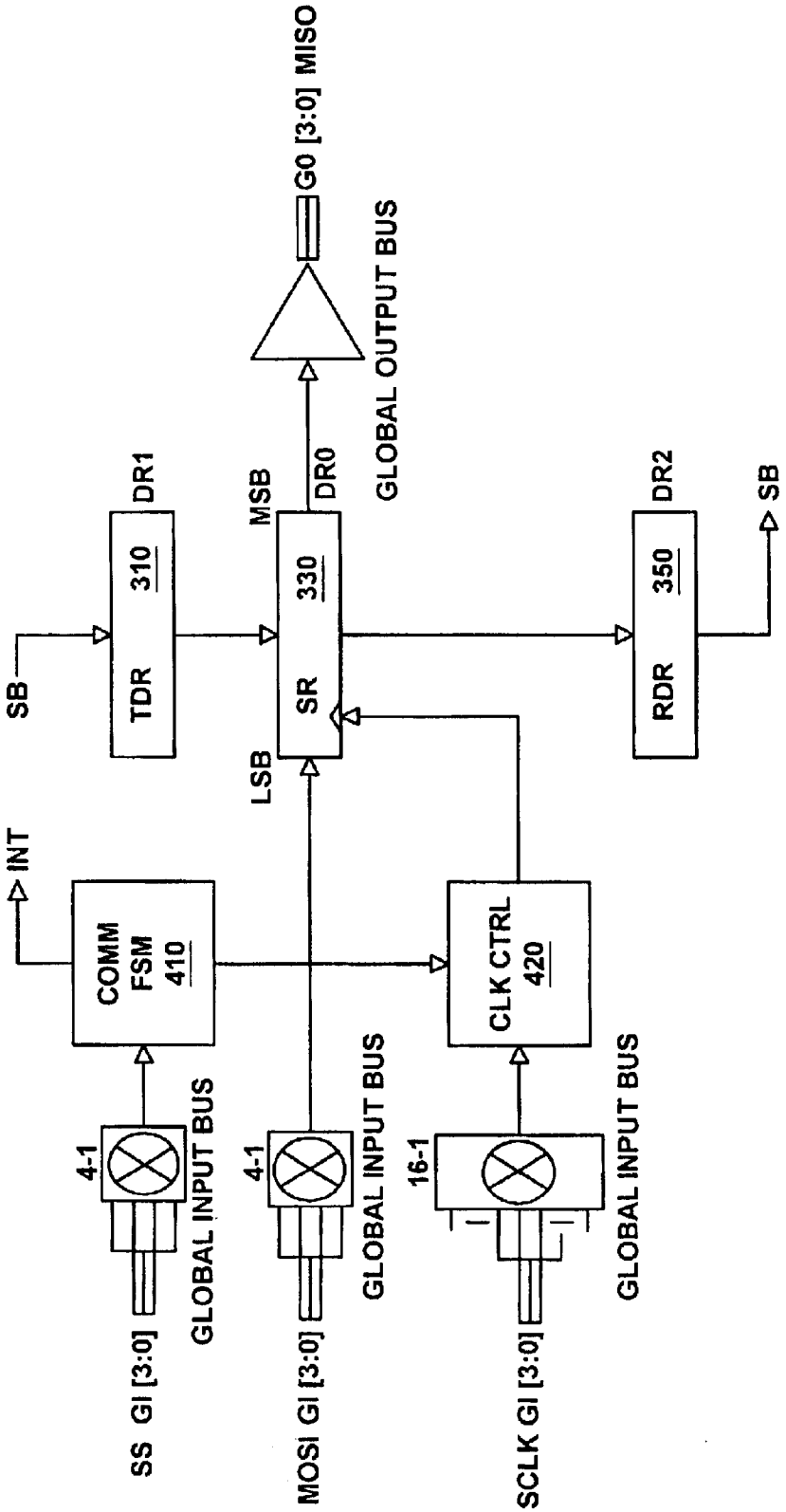


FIGURE 9

DIGITAL CONFIGURABLE MACRO ARCHITECTURE

RELATED U.S. APPLICATION

This patent application is a continuation of application Ser. No. 09/909,045, filed Jul. 18, 2001, now U.S. Pat. No. 6,507,214, entitled "DIGITAL CONFIGURABLE MACRO ARCHITECTURE", by Snyder, which claims priority to the copending provisional patent application, Serial No. 60/243,708, entitled "Advanced Programmable Microcontroller Device," with filing date Oct. 26, 2000, and assigned to the assignee of the present application, which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to programmable digital circuits. More particularly, the present invention relates to the field of programmable digital circuits which are dynamically configurable to any one of various digital functions by changing the contents of configuration registers.

2. Related Art

Microcontrollers or controllers have been utilized in various applications for many years. Primarily, microcontrollers are used in control-oriented applications that are interrupt-driven, sensing and controlling external events. Microcontrollers are frequently found in: appliances (e.g., microwave oven, refrigerator, television, VCR, stereo), computers and computer equipment (e.g., laser printers, modems, disk drives), automobiles (e.g., engine control, diagnostics, climate control), environmental control (e.g., greenhouse, factory, home), aerospace, and thousands of other uses.

The Field Programmable Gate Array (FPGA) has become very popular in recent years, even being utilized in several microcontroller applications. One reason for its popularity is the shortage in design cycle time that may be achieved by using programmable devices. Typically, FPGAs offer the highest logic capacity. FPGAs can be programmed to realize different digital functions. In particular, many FPGAs have programmable look-up tables to realize different digital functions. Typically, a FPGA contains from a few to tens of thousands of programmable logic blocks and an even greater number of flip-flops, each programmable logic block having a look-up table, multiplexors, and flip-flops. Most FPGAs do not provide 100% interconnect between programmable logic blocks.

However, FPGAs are highly inefficient with respect to chip area, increasing their cost. Typically, less than half of the logic resources in the FPGA are used to realize a digital function. Moreover, FPGAs need to have their look-up tables re-programmed in order to enable them to implement a new digital function, which is a time consuming task.

FPGAs are not ideally suited for microcontroller applications. Microcontroller applications are very cost-sensitive. A FPGA is not able to realize the number of digital functions that are demanded by today's microcontroller applications within these strict cost constraints.

SUMMARY OF THE INVENTION

A new digital configurable macro architecture is described. The digital configurable macro architecture is

well suited for microcontroller or controller designs. In particular, the foundation of the digital configurable macro architecture is a programmable digital circuit block. In an embodiment, programmable digital circuit blocks are 8-bit circuit modules that can be programmed to perform any one of a variety of predetermined digital functions by changing the contents of a few registers therein, unlike a FPGA which is a generic device that can be programmed to perform any arbitrary digital function. Specifically, the circuit components of the programmable digital circuit block are designed for reuse in several of the predetermined digital functions such that to minimize the size of the programmable digital circuit block. The programmable digital circuit blocks can be configured, for example, as timers, counters, serial communication ports, cyclic redundancy generators/checkers (CRC), or pseudo random sequence generators (PRS). The user selects the digital function that is needed and configures the programmable digital circuit block accordingly.

The programmable digital circuit blocks can be configured to coupled in series or in parallel to handle more complex digital functions. For example, a 24-bit timer can be designed by coupling three 8-bit programmable digital circuit blocks that have been individually configured as 8-bit timers. Additionally, a first programmable digital circuit block that is configured as a CRC generator can feed a second programmable digital circuit block that is configured as a serial output communication port.

More importantly, the configuration of the programmable digital circuit block is determined by its small number of configuration registers. This provides much flexibility. In particular, the configuration of the programmable digital circuit block is fast and easy since changes in configuration are accomplished by changing the contents of the configuration registers, whereas the contents are generally a small number of configuration data bits. Thus, the programmable digital circuit block is dynamically configurable from one predetermined digital function to another predetermined digital function for real-time processing.

These and other advantages of the present invention will no doubt become apparent to those of ordinary skill in the art after having read the following detailed description of the preferred embodiments which are illustrated in the drawing figures.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the present invention.

FIG. **1** illustrates a programmable digital circuit block in accordance with an embodiment of the present invention.

FIG. **2** illustrates a block diagram of an exemplary programmable digital device having a plurality of programmable digital circuit blocks in accordance with an embodiment of the present invention.

FIG. **3** illustrates a block diagram of a timer configuration of a programmable digital circuit block in accordance with an embodiment of the present invention.

FIG. **4** illustrates a block diagram of a counter configuration of a programmable digital circuit block in accordance with an embodiment of the present invention.

FIG. **5** illustrates a block diagram of a pulse width modulator (PWM) configuration of a programmable digital circuit block in accordance with an embodiment of the present invention.

FIG. **6** illustrates a block diagram of a UART transmitter configuration of a programmable digital circuit block in accordance with an embodiment of the present invention.

FIG. **7** illustrates a block diagram of a UART receiver configuration of a programmable digital circuit block in accordance with an embodiment of the present invention.

FIG. **8** illustrates a block diagram of a SPI Master configuration of a programmable digital circuit block in accordance with an embodiment of the present invention.

FIG. **9** illustrates a block diagram of a SPI Slave configuration of a programmable digital circuit block in accordance with an embodiment of the present invention.

The drawings referred to in this description should not be understood as being drawn to scale except if specifically noted.

DETAILED DESCRIPTION OF THE INVENTION

Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be recognized by one of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

FIG. **1** illustrates a programmable digital circuit block **100** in accordance with an embodiment of the present invention. The programmable digital circuit block **100** is the foundation of a new digital configurable macro architecture of the present invention. The digital configurable macro architecture is well suited for microcontroller or controller designs.

The design of the programmable digital circuit block **100** in the digital configurable macro architecture was developed after examining and studying conventional microcontrollers to determine the types of digital functions that were implemented within various conventional microcontrollers. It was discovered that there were not very many different types of digital functions demanded in microcontroller applications. Furthermore, it was determined that these different types of digital functions had many circuit components in common. Moreover, it was determined that the digital functions were generally implemented as 8-bit or multiples of 8-bits because their length was generally based on the length of standard buses. This led to the development of the programmable digital circuit blocks **100**, the building block of the digital configurable macro architecture.

In an embodiment, the programmable digital circuit block **100** is an 8-bit circuit module that can be programmed to perform any one of a variety of predetermined digital functions (which are useful in microcontroller applications) by changing the contents of a few configuration registers **50** therein, unlike a FPGA which is a generic device that can be programmed to perform any arbitrary digital function. Specifically, the circuit components of the programmable digital circuit block **100** are designed for reuse in several of the predetermined digital functions such that to minimize the size of the programmable digital circuit block **100**. Hence, the programmable digital circuit block **100** is highly efficient in terms of die area. In an embodiment, the programmable digital circuit block **100** can be configured as a timer, a counter, a pulse width modulator (PWM), a cyclic redundancy generator/checker (CRC), a pseudo random sequence generator (PRS), a dead zone delay, a UART (universal asynchronous receiver-transmitter) transmitter, a UART (universal asynchronous receiver-transmitter) receiver, a SPI (serial peripheral interface) Master, or a SPI (serial peripheral interface) Slave.

In another embodiment, the programmable digital circuit block **100** can be configured as a timer, a counter, a pulse width modulator (PWM), a cyclic redundancy generator/checker (CRC), a pseudo random sequence generator (PRS), or a dead zone delay, whereas the digital communication functions (e.g., UART and SPI) are eliminated to further reduce the size of the programmable digital circuit block **100**. In particular, the user selects the digital function that is needed and configures the programmable digital circuit block **100** accordingly. It should be understood that the programmable digital circuit block **100** can be designed to implement other digital functions.

A design can have an array of programmable digital circuit blocks **100** which can be configured to coupled together in series or in parallel to handle more complex digital functions or to increase precision. For example, a 24-bit timer can be designed by coupling three 8-bit programmable digital circuit blocks **100** that have been individually configured as 8-bit timers. Similarly, the 8-bit timer can be extended to 16- or 32-bit digital functions by coupling multiple programmable digital circuit blocks **100** together. Additionally, a first programmable digital circuit block that is configured as a CRC generator can feed a second programmable digital circuit block that is configured as a serial output communication port, reducing device programming and increasing performance.

More importantly, the configuration of the programmable digital circuit block **100** is determined by its configuration registers **50**. The programmable digital circuit block **100** generally has one or more configuration registers **50**. This provides much flexibility. In particular, the configuration of the programmable digital circuit block **100** is fast and easy to configure and re-configure since changes in configuration are accomplished by changing the contents of the configuration registers **50**, whereas the contents are generally a small number of configuration data bits. Thus, the programmable digital circuit block **100** is dynamically configurable from one predetermined digital function to another prede-

termined digital function for real-time processing. In contrast, FPGAs need to have their look-up tables re-programmed in order to have them implement a new digital function, a time-consuming task that is not done in real-time processing.

Referring to FIG. **1**, in an embodiment the programmable digital circuit block **100** includes one or more configuration registers **50**, one or more data registers **40**, a plurality of selectable logic circuits **30**, one or more configurable inputs **20**, one or more configurable outputs **10**, one or more cascade outputs **60**, one or more cascade inputs **70**, a clock input **80**, and a system input **90**. It should be understood that the programmable digital circuit block **100** can have other designs Including lengths other than 8-bits.

The configuration registers **50** are programmed via the system bus **90**. Any device, such as a microprocessor using data stored in a RAM or flash memory, can program (or write to) the configuration registers. The configuration registers **50** receive and store a plurality of configuration data corresponding to any one of the plurality of predetermined digital function described above. The programmed configuration registers **50** configure the programmable digital circuit block **100** to perform any one of the predetermined digital functions based on the configuration data. Moreover, the configuration registers **50** can be dynamically programmed with the configuration data for real-time processing. In addition, the configuration data includes (1) bits for indicating one of the predetermined digital functions and configuring the selectable logic circuits **30**, (2) bits for configuring and selecting the configurable inputs **20** and the configurable outputs **10** and the clock input **80**, (3) bits for indicating the mode of the predetermined digital function (e.g., parity, no parity, etc.), (4) bits for indicating the length of the predetermine digital function if several programmable digital circuit block **100** are coupled together (e.g., 8-bit, 16-bit, 24-bit, etc.), and (5) bits for indicating and configuring the interface between adjacent programmable digital circuit blocks **100** that are coupled together (e.g., configuring and selecting the cascade inputs **70** and the cascade outputs **60** for serial or parallel interfacing).

In general, the number of bits in the configuration data is sufficiently small to enable the configuration registers **50** to be programmed on-the-fly so that the programmable digital circuit block **100** can be dynamically configured and interfaced. Thus, the programmable digital circuit blocks **100** can be configured as a timer for a first length of time, re-configured as a counter for a second length of time, re-configured as a PWM for a third length of time, and so on, for real-time processing. For example, it is possible for a single register write to configure the programmable digital circuit block **100** from a timer to a PWM or to a counter or to a CRC generator or etc.

The connections **50**A–**50**F between the configuration registers **50** and other components of the programmable digital circuit block **100** enable the configuration registers **50** to properly configure the programmable digital circuit block **100** to any one of the predetermined digital functions and to properly interface the programmable digital circuit block **100** with other programmable digital circuit blocks in series or in parallel.

Continuing with FIG. **1**, the selectable logic circuits **30** are tailored such that they have a minimum set of circuit resources that can be programmed by the configuration registers **50** to implement any one of a variety of predetermined digital functions, unlike the FPGA where a substantial amount of circuit resources may remain unused. In particular, the design and structure of the selectable logic circuits **30** are dependent on the predetermined digital functions such that to minimize the size of the programmable digital circuit block **100**. The fixed number of digital functions for the programmable digital circuit block **100** substantially influences the design of the programmable digital circuit block **100**, providing cost savings and improving performance. The configuration registers **50** configure and select any of the selectable logic circuits **30** to perform one of the predetermined digital functions based on the configuration data. More importantly, the selectable logic circuits **30** are reused in several of the predetermined digital functions as will be illustrated below, ensuring the size efficiency of the programmable digital circuit block **100**. In an embodiment, the selectable logic circuits **30** include a plurality of logic gates.

Moreover, the selectable logic circuits **30** realize any one of the variety of predetermined digital functions by using the data registers **40** to receive data, load data, capture data, etc. Thus, the data registers **40** are also reused in several of the predetermined digital functions as will be illustrated below.

Again referencing FIG. **1**, the cascade outputs **60** and the cascade inputs **70** are selected and configured according to the configuration data. The cascade outputs **60** allow the programmable digital circuit block **100** to output signals for directly interfacing with adjacent or neighboring programmable digital circuit blocks. The cascade inputs **70** allow the adjacent or neighboring programmable digital circuit blocks to send signals that directly interface and are received by the programmable digital circuit block **100**. Specifically, the cascade outputs **60** and the cascade inputs **70** enable multiple programmable digital circuit blocks to seamlessly interface to. handle more complex digital functions or to increase precision as described above (e.g., 32-bit timer, CRC generator and SPI Master, 24-bit counter, etc.).

FIG. **2** illustrates a block diagram of an exemplary programmable digital device **200** having a plurality of programmable digital circuit blocks **210**A–**210**H in accordance with an embodiment of the present invention. The plurality of programmable digital circuit blocks **210**A–**210**H includes a first group and a second group. The first group includes the programmable digital circuit blocks **210**A–**210**B and **210**E–**210**F. Moreover, each programmable digital circuit block of the first group can be configured as a timer, a counter, a pulse width modulator (PWM), a cyclic redundancy generator/checker (CRC), a pseudo random sequence generator (PRS), or a dead zone delay. The second group includes the programmable digital circuit blocks **210**C–**210**D and **210**G–**210**H. Moreover, each programmable digital circuit block of the second group can be configured as a timer, a counter, a pulse width modulator (PWM), a cyclic redundancy generatbr/checker (CRC), a pseudo random sequence generator (PRS), a dead zone delay, a UART (universal asynchronous receiver-transmitter) transmitter, a UART (universal asynchronous receiver-transmitter) receiver, a SPI (serial peripheral interface) Master, or a SPI (serial peripheral interface) Slave.

As illustrated in FIG. **2**, adjacent or neighboring programmable digital circuit blocks are interfaced via cascade lines **205** (input or output) as described above. The cascade lines **205** enable the programmable digital circuit blocks **210**A–**210**H to seamlessly interface to handle more complex digital functions or to increase precision. For example, a 32-bit counter can be designed by coupling four 8-bit programmable digital circuit blocks that have been individually configured as 8-bit counters. Similarly, the 8-bit counter can be extended to 16- or 24-bit digital functions by coupling multiple programmable digital circuit blocks together. Additionally, a first programmable digital circuit block that is configured as a CRC generator can feed a second programmable digital circuit block that is configured as a serial output communication port, reducing device programming and increasing performance.

Moreover, the exemplary programmable digital device **200** includes a signal bus for digitized analog signals, a clock bus, a system bus for programming the programmable digital circuit blocks **210**A–**210**H, and a plurality of global data buses for transmitting data to/from the programmable digital circuit blocks **210**A–**210**H.

FIG. **3** illustrates a block diagram of a timer configuration of a programmable digital circuit block in accordance with an embodiment of the present invention. FIG. **4** illustrates a block diagram of a counter configuration of a programmable digital circuit block in accordance with an embodiment of the present invention. FIG. **5** illustrates a block diagram of a pulse width modulator (PWM) configuration of a programmable digital circuit block in accordance with an embodiment of the present invention.

As illustrated in FIGS. **3**–**5**, the selectable logic circuits **320** and **340** are reused for the timer, counter, and PWM configurations. Moreover, the first data register **310**, the second data register **330**, and the third data register **350** of the programmable digital circuit block are reused for the timer, counter, and PWM configurations. In essence, the configuration data loaded onto the configuration registers determines how the data registers **310**, **330**, and **350** are to be used, what operation is to be performed on the data by the selectable logic circuits **320** and **340**, where the input data is selected from (e.g., system bus (SB), signal bus, global bus, etc.), where the output data is transmitted, what clock signal is to be used, what are the cascade inputs (e.g., DIN, Cl, etc.) from other programmable digital circuit blocks, what are the cascade outputs (e.g., DOUT, CO, etc.) to other programmable digital circuit blocks, when to generate an interrupt (INT), and what is the data flow within the programmable digital circuit block so that the programmable digital circuit block can properly perform any one of the predetermined digital functions.

FIG. **6** illustrates a block diagram of a UART transmitter configuration of a programmable digital circuit block in accordance with an embodiment of the present invention. FIG. **7** illustrates a block diagram of a UART receiver configuration of a programmable digital circuit block in accordance with an embodiment of the present invention. FIG. **8** illustrates a block diagram of a SPI Master configuration of a programmable digital circuit block in accordance with an embodiment of the present invention. FIG. **9** illustrates a block diagram of a SPI Slave configuration of a programmable digital circuit block in accordance with an embodiment of the present invention.

As illustrated in FIGS. **6**–**9**, the selectable logic circuits **410** and **420** are reused for the UART transmitter, the UART receiver, the SPI Master, and the SPI Slave configurations. Moreover, the first data register **310**, the second data register **330**, and the third data register **350** of the programmable digital circuit block are reused in several of the UART transmitter, the UART receiver, the SPI Master, and the SPI Slave configurations. However, the selectable logic circuit **430** is used in the UART transmitter configuration of FIG. **6** since the UART protocol requires that particular protocol bits (e.g., start bits, stop bits, etc.) to be generated by the UART transmitter.

FIGS. **3**–**9** illustrate that the programmable digital circuit block can be configured fast and easily. Furthermore, FIGS. **3**–**9** illustrate that the programmable digital circuit block is highly efficient in terms of die area.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents.

What is claimed is:

1. A programmable digital device comprising:

a programmable digital circuit block that is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation.

2. The programmable digital device as recited in claim **1** wherein said programmable digital circuit block is configurable into a serial arrangement.

3. The programmable digital device as recited in claim **1** wherein said programmable digital circuit block is configurable into a parallel arrangement.

4. The programmable digital device as recited in claim **1** wherein said predetermined digital functions include a timer, a counter, a pulse width modulator (PWM), a cyclic redundancy generator/checker (CRC), a pseudo random sequence generator (PRS), a dead zone delay, a UART transmitter, a UART receiver, a SPI Master, and a SPI Slave.

5. The programmable digital device as recited in claim **1** wherein said predetermined digital functions include a timer, a counter, a pulse width modulator (PWM), a cyclic redundancy generator/checker (CRC), a pseudo random sequence generator (PRS), and a dead zone delay.

6. The programmable digital device as recited in claim **1** wherein said predetermined digital functions are 8-bit predetermined digital functions.

7. The programmable digital device as recited in claim **1** wherein said programmable digital circuit block further comprises:

a configuration register for receiving and storing a plurality of configuration data corresponding to any of said plurality of predetermined digital functions; and

a plurality of selectable logic circuits which perform any of said plurality of predetermined digital functions, wherein said predetermined digital functions determine size and arrangement of said selectable logic circuits.

8. A programmable digital device comprising:

an array of programmable digital circuit blocks, each programmable digital circuit block is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation.

9. The programmable digital device as recited in claim **8** wherein each programmable digital circuit block is configurable into a serial arrangement.

10. The programmable digital device as recited in claim **8** wherein each programmable digital circuit block is configurable into a parallel arrangement.

11. The programmable digital device as recited in claim **8** wherein said predetermined digital functions include a timer, a counter, a pulse width modulator (PWM), a cyclic redundancy generator/checker (CRC), a pseudo random sequence generator (PRS), a dead zone delay, a UART transmitter, a UART receiver, a SPI Master, and a SPI Slave.

12. The programmable digital device as recited in claim **8** wherein said predetermined digital functions include a timer, a counter, a pulse width modulator (PWM), a cyclic redundancy generator/checker (CRC), a pseudo random sequence generator (PRS), and a dead zone delay.

13. The programmable digital device as recited in claim **8** wherein said predetermined digital functions are 8-bit predetermined digital functions.

14. The programmable digital device as recited in claim **8** wherein each programmable digital circuit block further comprises:

a configuration register for receiving and storing a plurality of configuration data corresponding to any of said plurality of predetermined digital functions; and

a plurality of selectable logic circuits which perform any of said plurality of predetermined digital functions, wherein said predetermined digital functions determine size and arrangement of said selectable logic circuits.

15. A method of configuring a programmable digital circuit block, comprising:

selecting one a plurality of predetermined digital functions;

performing a single register write operation to provide to said programmable digital circuit block a plurality of configuration data corresponding to said selected one of said predetermined digital functions; and

configuring said programmable digital circuit block using said configuration data.

16. The method as recited in claim **15** wherein said configuring includes configuring said programmable digital circuit block into a serial arrangement.

17. The method as recited in claim **15** wherein said configuring includes configuring said programmable digital circuit block into a parallel arrangement.

18. The method as recited in claim **15** wherein said predetermined digital functions include a timer, a counter, a pulse width modulator (PWM) a cyclic redundancy generator/checker (CRC), a pseudo random sequence generator (PRS), a dead zone delay, a UART transmitter, a UART receiver, a SPI Master, and a SPI Slave.

19. The method as recited in claim **15** wherein said predetermined digital functions include a timer, a counter, a pulse width modulator (PWM), a cyclic redundancy generator/checker (CRC), a pseudo random sequence generator (PRS), and a dead zone delay.

20. The method as recited in claim **15** wherein said predetermined digital functions are 8-bit predetermined digital functions.

* * * * *

EXHIBIT E

US006961807B1

(12) **United States Patent**
Hauck

(10) **Patent No.: US 6,961,807 B1**
(45) **Date of Patent: Nov. 1, 2005**

(54) **DEVICE, SYSTEM AND METHOD FOR AN INTEGRATED CIRCUIT ADAPTABLE FOR USE IN COMPUTING SYSTEMS OF DIFFERING MEMORY REQUIREMENTS**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 196 days.

(21) Appl. No.: **10/229,432**

(22) Filed: **Aug. 27, 2002**

(51) **Int. Cl.**[7] **G06F 12/00**

(52) **U.S. Cl.** **711/103**; 711/100; 711/149; 711/154

(58) **Field of Search** 711/100, 102, 711/103, 118, 131, 149, 154, 170; 710/36; 365/63

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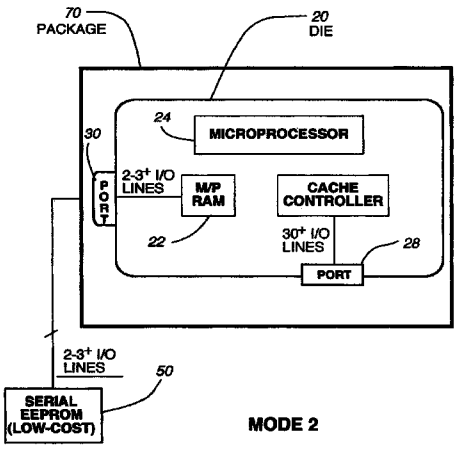
Primary Examiner—Tuan V. Thai
(74) *Attorney, Agent, or Firm*—Dorsey & Whitney LLP

(57) **ABSTRACT**

An integrated circuit device, and associated system and method, including a microprocessor, a multipurpose memory coupled with the microprocessor, a cache controller, and a first and second memory port. In one example, the first memory port is provided for coupling a first external memory device with the cache controller, and the second memory port is provided for coupling a second external memory device with the multipurpose memory. In one example, the first memory port may be adapted to be coupled with a Flash ROM, and the second memory port may be adapted to be coupled with an EEPROM. In this manner, the integrated circuit device may be utilized in different systems that have differing memory requirements.

17 Claims, 5 Drawing Sheets



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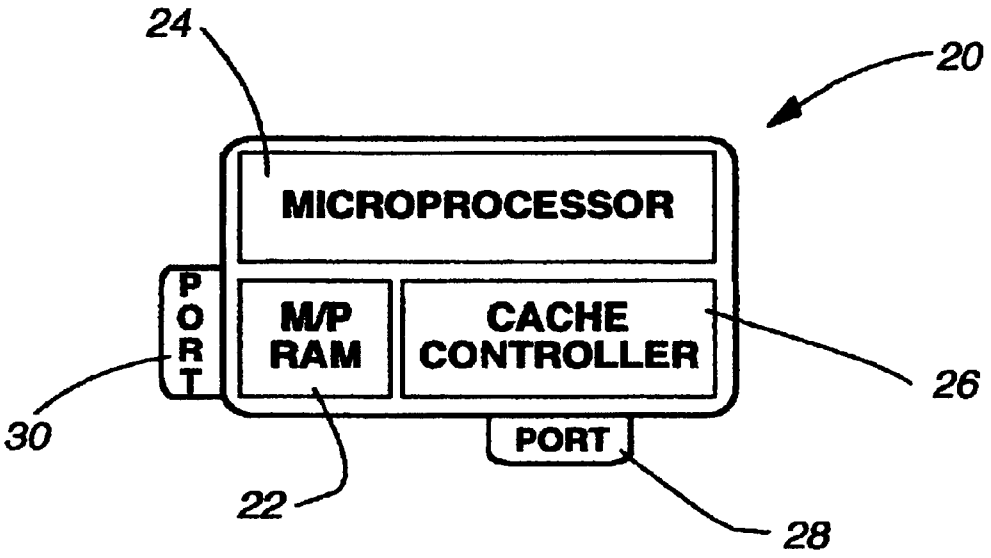
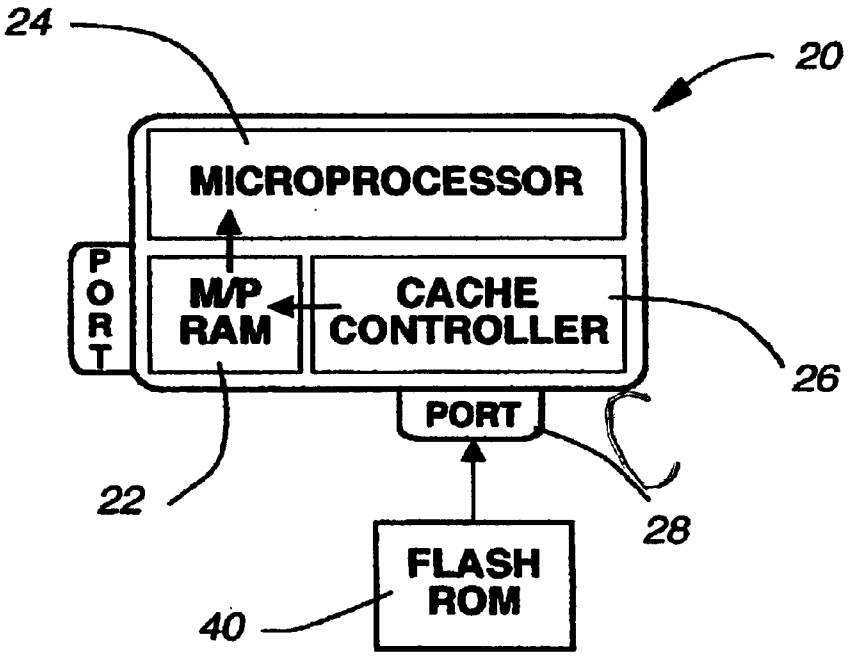
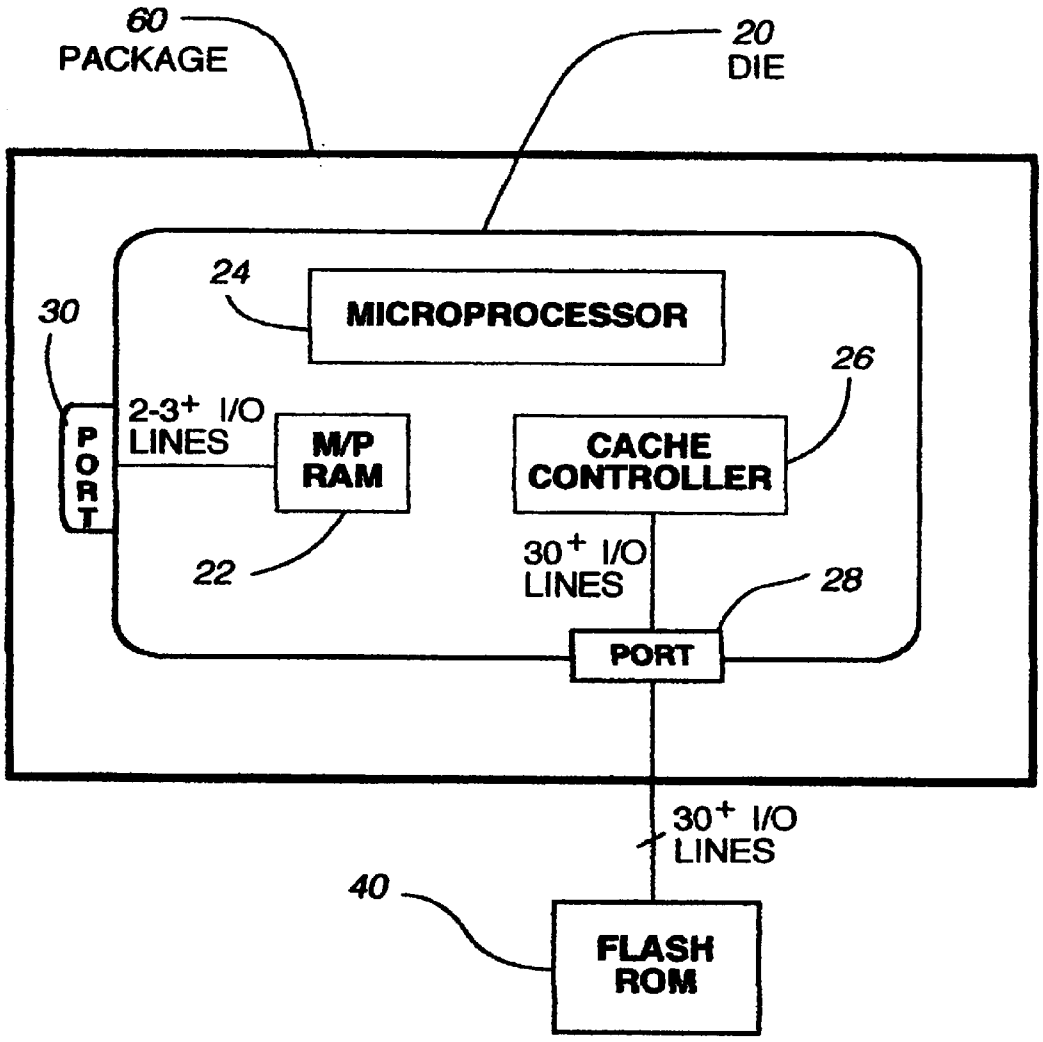


Fig. 1



MODE 1

Fig. 2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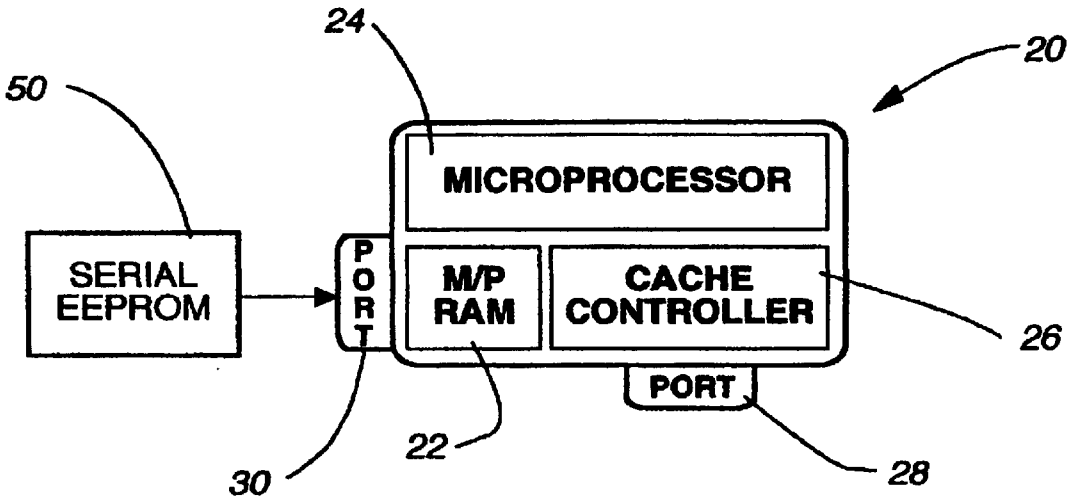
PACKAGE
20
DIE
24
MICROPROCESSOR
30
26
PORT
2-3+ I/O
LINES
M/P
RAM
CACHE
CONTROLLER
22
30+ I/O
LINES
28
PORT
30+ I/O
LINES
40
FLASH
ROM

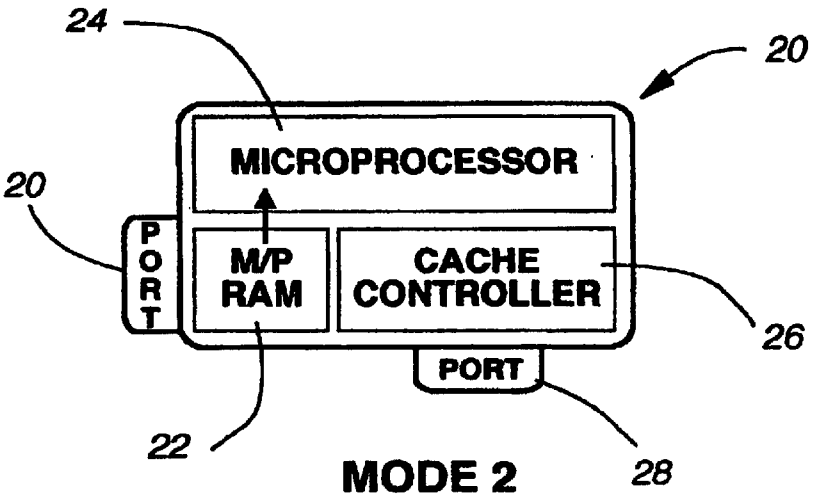
MODE 1

Fig. 3



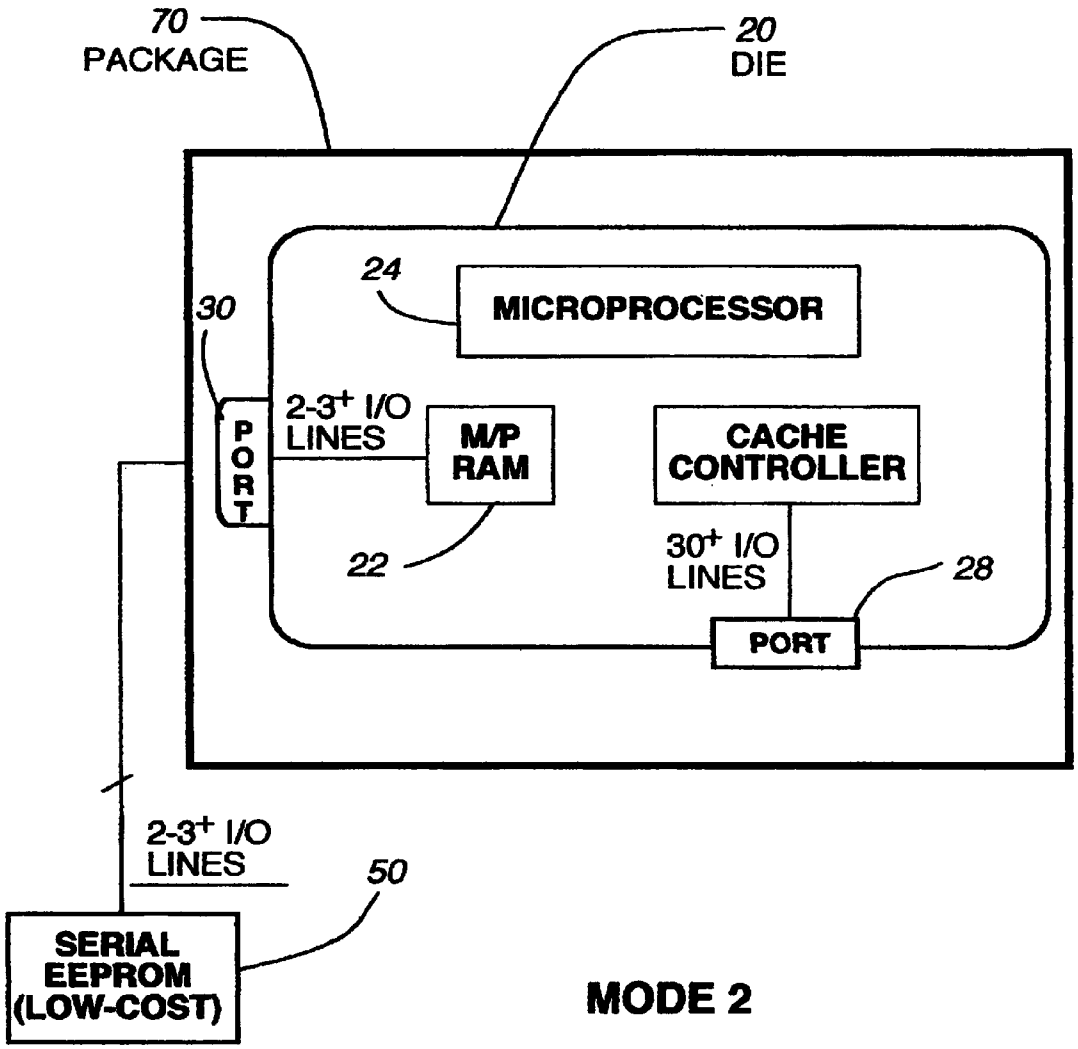
MODE 2

Fig. 4A (BOOT)



MODE 2

Fig. 4B (RUN)


70
PACKAGE
20
DIE
24
MICROPROCESSOR
30
PORT
2-3+ I/O
LINES
M/P
RAM
CACHE
CONTROLLER
22
30+ I/O
LINES
28
PORT
2-3+ I/O
LINES
50
SERIAL
EEPROM
(LOW-COST)

MODE 2

Fig. 5

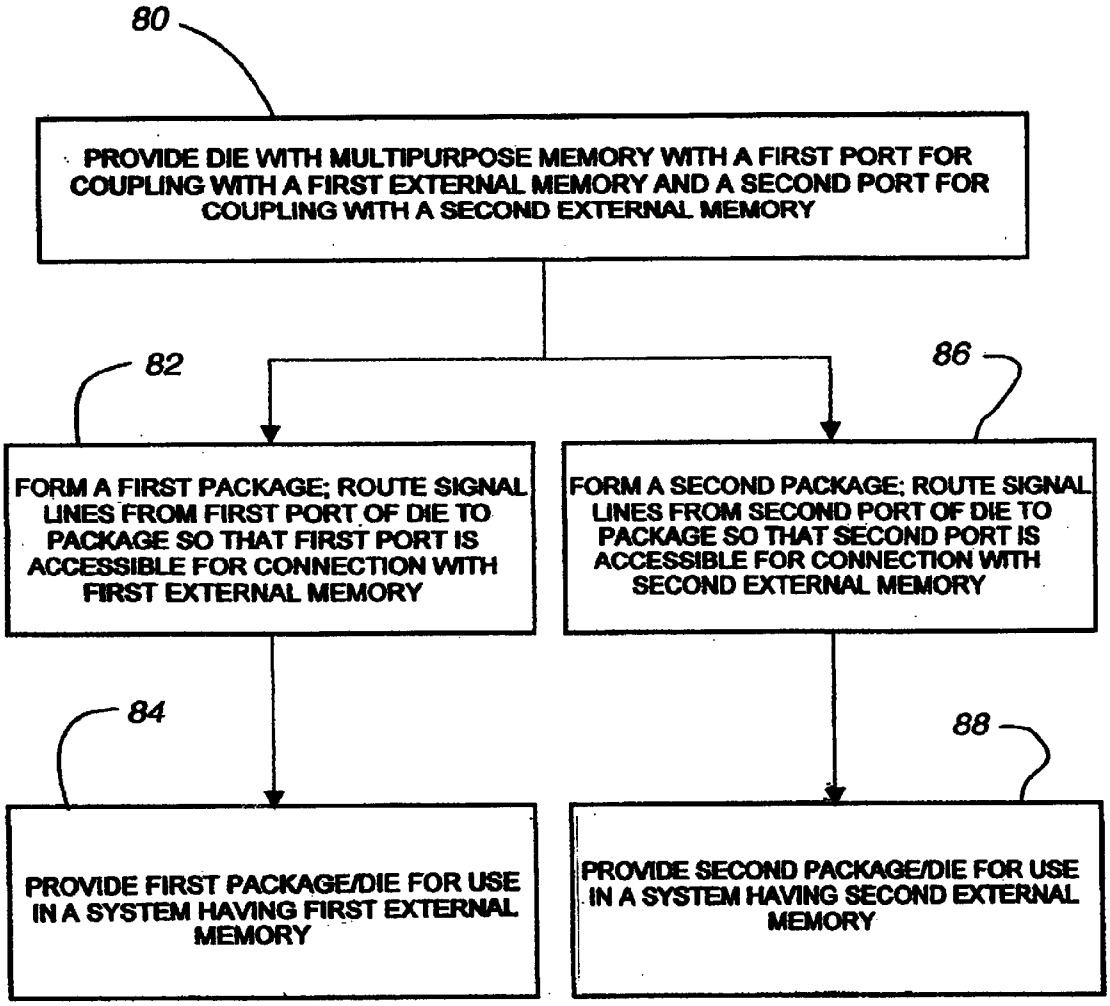

80
PROVIDE DIE WITH MULTIPURPOSE MEMORY WITH A FIRST PORT FOR COUPLING WITH A FIRST EXTERNAL MEMORY AND A SECOND PORT FOR COUPLING WITH A SECOND EXTERNAL MEMORY
82
86
FORM A FIRST PACKAGE; ROUTE SIGNAL LINES FROM FIRST PORT OF DIE TO PACKAGE SO THAT FIRST PORT IS ACCESSIBLE FOR CONNECTION WITH FIRST EXTERNAL MEMORY
FORM A SECOND PACKAGE; ROUTE SIGNAL LINES FROM SECOND PORT OF DIE TO PACKAGE SO THAT SECOND PORT IS ACCESSIBLE FOR CONNECTION WITH SECOND EXTERNAL MEMORY
84
88
PROVIDE FIRST PACKAGE/DIE FOR USE IN A SYSTEM HAVING FIRST EXTERNAL MEMORY
PROVIDE SECOND PACKAGE/DIE FOR USE IN A SYSTEM HAVING SECOND EXTERNAL MEMORY

Fig. 6

DEVICE, SYSTEM AND METHOD FOR AN INTEGRATED CIRCUIT ADAPTABLE FOR USE IN COMPUTING SYSTEMS OF DIFFERING MEMORY REQUIREMENTS

TECHNICAL FIELD

This application relates, in general, to integrated circuits and associated memory systems.

BACKGROUND

Computer chips, such as microprocessors or microcontrollers, are made of a die and a package. The die has an integrated circuit thereon which may include various circuits such as the microprocessor, memory, power circuits, logic circuit, interface circuits, etc. From the die, signal lines are connected to signal lines of the package. The package has pins or other conductors extending from the package which are used to connect the signal lines of the package to other circuits on a printed circuit board.

In the design of an integrated circuit incorporating a microprocessor, microcontroller, or other logic, it is often difficult to determine the appropriate amount of on-chip memory to incorporate on the die in order to suit the many applications that the integrated circuit may serve. For instance, a large amount of on-chip static memory (i.e., RAM) provides the benefit of fast program execution but has a disadvantage in that the large on-chip RAM requires an initial program loading operation from an off-chip non-volatile memory (i.e., Flash ROM) which has the program content stored therein. The use of such a non-volatile memory may add additional costs to the overall system design which utilizes the integrated circuit, in part because the integrated circuit packages and corresponding pin counts may be quite large. For instance, the interface between the external Flash ROM and the integrated circuit may include a parallel interface having 30 or more pins, which increases the complexity, size, and cost of use of such a system. While the cost and size of such an arrangement may be acceptable in the design of large, complex systems, such as a system that uses multiple chips and large program memories, the cost and size of such an arrangement may be unacceptable if the integrated circuit is to be used in a simple, low-cost system—such as in the design of a smaller microprocessor embedded system.

Alternatively, a large amount of non-volatile memory incorporated on-chip with the integrated circuit has the advantage of relatively low costs when compared with an arrangement that uses on-chip RAM/external Flash ROM. However, such an arrangement has the disadvantage of relatively slower program execution when compared with on-chip RAM/external Flash ROM, which may be unacceptable for use in a large, complex system.

Hence, in order to accommodate the needs of large, complex systems as well as small, low-cost systems, different integrated circuits are designed, manufactured, packaged and sold. As recognized by the present inventor, what is needed is an architecture for an integrated circuit die that may be utilized with large, complex systems using external memory or with small, low-cost systems.

It is against this background that various embodiments of the present invention were developed.

SUMMARY

According to one broad aspect of one embodiment of the present invention, disclosed herein is an integrated circuit

device including a microprocessor, a multipurpose memory coupled with the microprocessor, a cache controller, and a first and second memory port. In one example, the first memory port is provided for coupling a first external memory device with the cache controller, and the second memory port is provided for coupling a second external memory device with the multipurpose memory. In one example, the first memory port may be adapted to be coupled with a Flash ROM, and the second memory port may be adapted to be coupled with an EEPROM. In this manner, the integrated circuit device may be utilized in different systems that have differing memory requirements.

In another embodiment, the multipurpose memory has a first operating mode for dynamically storing portions of a program obtained from the first external memory device, such as for execution by the microprocessor under control of the cache controller. In another example, the cache controller may be disabled, and the multipurpose memory has a second operating mode for storing an entire program obtained from the second external memory device to be run by the microprocessor. A serial peripheral interface may be provided between the second memory port and the EEPROM.

According to another broad aspect of an embodiment of the invention, disclosed herein is a system including a first external memory device and an integrated circuit. The integrated circuit includes a microprocessor, a multipurpose memory coupled with the microprocessor, a cache controller, and first and second memory ports. The first memory port is provided for coupling the first external memory device with the cache controller, and the second memory port is provided for coupling a second external memory device with the multipurpose memory. In this embodiment, the first memory device may include a Flash ROM which contains a program for execution by the microprocessor. Alternatively, the system could include a second external memory device and the integrated circuit, wherein the second external memory device is an EEPROM. Due to the architecture of the integrated circuit, a system designer would have the choice of whether to configure the system using the integrated circuit coupled with the first external memory device, or the integrated circuit coupled with the second external memory device.

According to another broad aspect of an embodiment of the invention, disclosed herein is a method for forming an integrated circuit on a die. The method includes providing a microprocessor on the die, providing a multipurpose memory on the die, providing a cache controller on the die, and providing a first and second memory port on the die. In one example, the first memory port is provided for coupling the cache controller with a first external memory device, such as a Flash ROM, and the second memory port is provided for coupling the multipurpose memory with a second external memory device, such as an EEPROM. A package may be provided for the integrated circuit such that, in one example, the first memory port of the die is coupled with a portion of the conductors of the package so that the first memory port may be connected with the first external memory device. Alternatively, the second memory port of the die may be coupled with a portion of the conductors of the package so that the second memory port may be connected with the second external memory device. In this manner, the integrated circuit may be used with different packages in different systems having differing memory requirements.

The foregoing and other features, utilities and advantages of the invention will be apparent from the following more

particular description of various embodiments of the invention as illustrated in the accompanying drawings and claims.

DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates a block diagram of an integrated circuit die having a multi-purpose memory, in accordance with one embodiment of the present invention.

FIG. **2** illustrates a block diagram of the integrated circuit die of FIG. **1** coupled with an external memory (Flash ROM), in accordance with one embodiment of the present invention.

FIG. **3** illustrates a block diagram of the integrated circuit die of FIG. **2** coupled through a package with an external memory, in accordance with one embodiment of the present invention.

FIG. **4**A illustrates a block diagram of the integrated circuit die of FIG. **1** coupled with an external memory (EEPROM) during an initialization phase, in accordance with one embodiment of the present invention.

FIG. **4**B illustrates a block diagram of the integrated circuit die of FIG. **1** coupled during normal operation, in accordance with one embodiment of the present invention.

FIG. **5** illustrates a block diagram of the integrated circuit die of FIG. **4**A coupled through a package with an external memory (EEPROM), in accordance with one embodiment of the present invention.

FIG. **6** illustrates an example of logical operations for forming and using an integrated circuit die, in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

Disclosed herein in one embodiment is an integrated circuit device, and associated system and method, which may be used with different packages so that the integrated circuit may be utilized with large, complex systems using external memory, or with small, low-cost systems. In one example, an integrated circuit device, such as an integrated circuit die, includes a multi-purpose memory which is configurable to operate in different modes depending upon the implementation or system in which the integrated circuit is used. In this manner, an integrated circuit die design may be manufactured and utilized with different systems having differing memory and performance requirements. Various embodiments of the present invention will now be described.

Referring to FIG. **1**, an integrated circuit die **20** has a multi-purpose memory **22** which is on-chip with a microprocessor **24** and cache controller **26**, in accordance with one embodiment of the present invention. The multi-purpose memory **22** can be selected to operate in at least two different modes, the particular mode selected dependant upon the final environment or system in which the die **20** will be used. In one example, the integrated circuit die **20** has a first memory port **28** which provides an interface to the cache controller **26**, and a second memory port **30** which provides an interface to the multi-purpose memory **22**. In order to use the same die in different system designs, the packaging of the die **20** may be varied, as will be discussed below.

Generally, in a first mode, the integrated circuit die **20** may be utilized with an external non-volatile memory **40** (FIG. **2**), such as Flash ROM, coupled with the first memory port **28** wherein the multi-purpose memory **22** acts as a cache memory, as shown and described with reference to FIGS. **2**–**3**. Such an implementation may be useful in complex system design where one or more microprocessors are used with a large external system memory, such as Flash ROM. In a second mode, the integrated circuit die **20** may be used with an external memory **50** (FIG. **4**A-B), such as a serial EEPROM, coupled with the second memory port **30** wherein the program instructions and/or other persistent information stored on the external memory **50** are loaded into the multi-purpose memory **22** during an initialization phase for execution, as shown and described with reference to FIGS. **4**–**5**. Hence, the integrated circuit die **20** may be employed in different applications having differing memory architectures, depending upon the particular needs of the overall system in which the integrated circuit **20** will be used.

As shown in FIG. **1**, the integrated circuit die **20** may also have a microprocessor **24** and a cache controller **26**. The microprocessor **24**, which may be a microcontroller or programmable logic, may include a central processing unit and related circuits and logic for implementing various computational functions, and may support a RISC (reduced instruction set computer) or CISC (complex instruction set computer) instruction set.

The cache controller **26** of the integrated circuit die **20** of FIG. **1**, when enabled as in the first mode shown in FIGS. **2**–**3**, provides instructions and/or data from an external memory **40** (i.e., the Flash ROM) to the multi-purpose memory **22** of the die **20**. The microprocessor **24** then executes instructions from the on-chip multi-purpose memory **22**, which speeds execution and improves overall performance. The cache controller **26** may include conventional algorithms for controlling the flow of data into the multi-purpose memory **22**, in order to reduce access to the program stored in the off chip memory **40** (i.e., Flash ROM) and improve execution performance using the on-chip multi-purpose memory **22**.

Referring to FIGS. **2**–**3**, a first environment is illustrated in which the integrated circuit die **20** of FIG. **1** may be used. In this embodiment, the integrated circuit die **20** is coupled through the first memory port **28** with one or more non-volatile external memories devices **40**, such as a Flash ROM, which are provided for persistent storage of the program to be executed by the microprocessor **24**. The cache controller **26** functions as a normal cache and provides an interface to the external memory **40**, so that the integrated circuit die **20** may be used in a system design wherein external program memory **40** is utilized, such as in a multi-chip system that uses large program memories.

In this example, the multi-purpose memory **22** acts as cache memory to the microprocessor **24** for accessing program instructions externally stored in the external memory **40**. The external memory **40** may contain large programs, and the cache controller **26** loads a set of instructions (or portions of the program) into the multi-purpose memory **22** from the external memory **40**. The microprocessor **24** executes these instructions from the multi-purpose memory **22**, which provides a performance benefit of rapid availability of instructions for execution. If an instruction to be executed is not in the multi-purpose memory **22**, then the external memory **40** is accessed through the cache controller **26** so that the needed instructions are loaded into the multi-purpose memory **22**. In this sense, the contents of the multi-purpose memory **22** can change dynamically during operation under the control of the cache controller **26** as needed. As mentioned above, the cache controller **26** may implement or support one or more conventional cache management policies, depending on the particular performance needs of the system in which the integrated circuit die **20** is being used.

In order to provide the connections between the integrated circuit die **20** and the external memory system **40** for operating in the first mode, the first memory port **28** may include numerous I/O pins (i.e., 30 pins) for address and data between the external memory **40** and the die **20**/package **60**. In one example, the second memory port **30** is unused in this configuration, as shown in FIG. **3**. The configurations of FIGS. **2–3** may be generally suited for embedded microprocessor systems where the memory requirements are relatively large.

Referring to FIGS. **4–5**, a second environment is illustrated in which the integrated circuit die **20** of FIG. **1** may be used. In this embodiment, the integrated circuit die **20** is coupled through the second memory port **30** with one or more non-volatile external memories devices **50**, such as a low-cost serial EEPROM, which is provided for persistent storage of the program to be executed or data to be used by the microprocessor **24**. The serial EEPROM **50** may be, in one example, an 8 pin device which may be significantly less expensive and smaller than a Flash ROM memory device **40** of FIGS. **2–3**.

In this embodiment (shown as a second mode in FIGS. **4**A–B, **5**), the multipurpose memory **22** acts as a preloadable, non-cached program memory for the microprocessor **24**, in one example. In this embodiment, the cache controller **26** is preferably disabled. As shown in FIG. **4**A, the multi-purpose memory **22** is loaded during an initialization phase of the microprocessor **24** with the entire program to be run by the microprocessor **24**. The external memory **50** may contain the entire program to be loaded into multi-purpose memory **22** and run by the microprocessor **24**. A boot loader may be provided with the second memory interface **30** to pre-load the multi-purpose memory **22** with a program, and after the boot operation is complete, the multi-purpose memory **22** functions as an internal program memory on-chip, in one example.

Once the program is loaded into multi-purpose memory **22**, then in one example the multi-purpose memory **22** is locked so that the program contents of the multi-purpose memory **22** cannot change, and as shown in FIG. **4**B, the microprocessor **24** accesses, preferably directly, the multi-purpose memory **22** to obtain program instructions to execute. In one example, the program contents of the multi-purpose memory **22** are static and do not change dynamically during normal operations.

In order to provide the connections between the integrated circuit die **20** and the external memory **50** (i.e., EEPROM) for operating in the second mode, the second memory port **30** may include a plurality of I/O pins (i.e., 3 or 4 pins) to form a bus between the external memory **50** and the die **20**/package **70**. An example of the interface of the second memory port **30** between the multi-purpose memory **22** and an EEPROM **50** may include an serial peripheral interface (SPI), such as commercially available from Atmel, Microchip, and/or ST Microelectronics. Such an SPI interface utilizes, for example, 3 or 4 pins which permits the integrated circuit die **20** to be utilized in an overall low cost design. In one example, the integrated circuit package **70** may include 56 pins, in which a 3 wire SPI interface is made available as a portion of the package **70**.

In one example, the first memory port **28** is unused in this configuration, as shown in FIG. **5**, and the I/O pins of the first memory port **28** would preferably not be brought out from the die to the package. The configurations of FIGS. **4–5** may be generally suited for embedded microprocessor systems where the memory requirements are relatively small when compared with the configuration of FIGS. **2–3**, or in a single processor system design.

FIG. **6** illustrates an example of logical operations for forming and using an integrated circuit die, in accordance with one embodiment of the present invention. The operations of FIG. **6** can be used to provide an integrated die which may be used in either a first system design or a second system design depending on the respective memory requirements thereof.

At operation **80**, an integrated circuit die is provided with a multi-purpose memory, such as the multi-purpose memory **22** of FIG. **1**, having a first port for coupling with a first external memory and a second port for coupling with a second external memory. In one embodiment, the first port provided by operation **80** is adapted for coupling a first external memory, such as a Flash ROM, with the multi-purpose memory using a cache controller, such as the cache controller **26** shown in FIG. **1**. Further, in one example, the second port provided by operation **80** may be adapted for coupling a second external memory, such as a serial EEPROM, with the multi-purpose memory. In this manner, operation **80** provides an integrated circuit die which may be utilized with either the first external memory or the second external memory, in one example.

Operations **82–84** and **86–88** relate to utilizing the integrated circuit die formed by operation **80** in at least two different settings. The integrated circuit die may be utilized with a first package which provides access to the first port of the die for connection with a first external memory (operation **82–84**); or the integrated circuit die may be used with a second package which provides access to the second port of the die for connection with a second external memory (operations **86–88**).

At operation **82**, a first package is formed for encasing the integrated circuit die of operation **80**. The package may have a plurality of conductors thereon. The signal lines from the first port of the die are routed to a portion of the conductors of the package so that the first port is accessible for connection with the first external memory. In one example, the signal lines from the second port of the integrated circuit die are not routed to the first package, as the first package is not to be used with the second memory port. At operation **84**, the first package and die are provided for use in a system having a first external memory. Because operation **82** provided the signal lines from the first port of the die to the conductors of package, the first external memory may be coupled with the appropriate signal lines of the first package so as to couple the first external memory with the first memory port.

If the die is to be used in a system having different memory requirements than described with reference to operations **82–84** (i.e., lower costs or smaller), then operations **86–88** may be used to provide the integrated circuit in combination with a second package. In one example, a portion of the conductors of the second package devoted to the second memory port is smaller than the portion of conductors of the first package devoted to the first memory port, so that the overall size of the second package may be smaller than the first package. At operation **86**, the second package is formed for the housing and encasing the integrated circuit die. The signal lines from the second port of the die are routed to a portion of the conductors of the package so that the second memory port is accessible for connection with an external memory device, such as a serial EEPROM. At operation **86**, the second package and die are provide for use in a system having an external memory such as the second external memory described with reference to FIGS. **4**A–B, **5**.

While the operations of FIG. **6** have been described with reference to a first and second package, it is understood that the integrated circuit die provided by operation **80** may be used in a package which routes signal lines from both the first and second ports of the die to the package so that both the first and second ports of the die are accessible for connection with the first or second external memory. In one embodiment, the multi-purpose memory may be configured so that the integrated circuit die utilizes either the first external memory over the first port, or the second external memory over the second port, but preferably not both. In this example, a system designer utilizing the integrated circuit die for a particular system design would connect either a first external memory through the first memory port, or a second external memory through the second memory port.

Accordingly, it can be seen that embodiments of the present invention provide an integrated circuit die with a multi-purpose memory architecture so that the same die can be used in different system designs having differing memory requirements, such as complex designs utilizing large external memories, or simple, inexpensive designs.

While the first and second external memory devices have been described and shown as Flash ROMs and Serial EEPROMs respectively, it is understood that other types of external memory devices may be used as the first and second external memory devices. Additionally, while the first and second memory ports have been shown and described as having 30 or more lines and 2–3 lines respectively, it is understood that the first and second memory ports may have a number of signal lines which may be more or less than the number of signal lines shown and described herein.

While the methods disclosed herein have been described and shown with reference to particular operations performed in a particular order, it will be understood that these operations may be combined, sub-divided, or re-ordered to form equivalent methods without departing from the teachings of the present invention. Accordingly, unless specifically indicated herein, the order and grouping of the operations is not a limitation of the present invention.

While the invention has been particularly shown and described with reference to a preferred embodiment thereof, it will be understood by those skilled in the art that various other changes in the form and details may be made without departing from the spirit and scope of the invention.

I claim:

1. An integrated circuit device, comprising:

a microprocessor;

a multipurpose memory coupled with the microprocessor;

a cache controller;

a first memory port for coupling a first external memory device with said cache controller; and

a second memory port for coupling a second external memory device with said multipurpose memory;

wherein the multipurpose memory has a first operating mode for dynamically storing as a cache memory portions of a program obtained from the first external memory device for execution by the microprocessor under control of the cache controller, and the multipurpose memory has a second operating mode for storing an entire program obtained from the second external memory device to be run by the microprocessor.

2. The device of claim **1**, wherein the first memory port is adapted to be coupled with a Flash ROM as the first external memory device.

3. The device of claim **1**, wherein the second memory port is adapted to be coupled with an EEPROM as the second external memory device.

4. The device of claim **1**, further comprising:

a serial peripheral interface between said second memory port and said second external memory device.

5. The device of claim **1**, wherein when said first memory port is coupled with said first external memory device, said second memory port is not coupled with the second external memory device.

6. An integrated circuit device, comprising:

a microprocessor;

a multipurpose memory coupled with the microprocessor;

a cache controller;

a first memory port for coupling a first external memory device with said cache controller; and

a second memory port for coupling a second external memory device with said multipurpose memory;

wherein the multipurpose memory has a first operating mode for dynamically storing as a cache memory portions of a program obtained from the first external memory device for execution by the microprocessor under control of the cache controller, and the multipurpose memory has a second operating mode for storing an entire program obtained from the second external memory device to be run by the microprocessor; and

wherein the cache controller is disabled when the second memory port is coupled with the second external memory device.

7. A method for forming an integrated circuit on a die, comprising:

providing a microprocessor on the die;

providing a multipurpose memory on the die;

providing a cache controller on the die;

providing a first memory port for coupling the cache controller with a first external memory device;

providing a second memory port for coupling the multipurpose memory with a second external memory device;

providing the multipurpose memory with a first operating mode for dynamically storing portions of a program obtained from the first external memory device for execution by the microprocessor under control of the cache controller; and

providing the multipurpose memory with a second operating mode for storing an entire program obtained from a second external memory device to be run by the microprocessor.

8. The method of claim **7**, wherein the operation of providing a first memory port for coupling the cache controller with a first external memory device further comprises:

adapting the first memory port to be coupled with a Flash ROM as the first external memory device.

9. The method of claim **7**, wherein the operation of providing a second memory port for coupling the cache controller with a second external memory device further comprises:

adapting the second memory port to be coupled with a serial EEPROM as the second external memory device.

10. The method of claim **7**, further comprising:

providing a package for the integrated circuit, the package having a plurality of conductors; and

coupling the first memory port of the die with a portion of the conductors of the package so that the first memory port may be connected with the first external memory device.

11. The method of claim **7**, further comprising:

providing a package for the integrated circuit, the package having a plurality of conductors; and

coupling the second memory port of the die with a portion of the conductors of the package so that the second memory port may be connected with the second external memory device.

12. The method of claim **7**, further comprising:

providing the multipurpose memory with a first operating mode for dynamically storing portions of a program obtained from the first external memory device for execution by the microprocessor under control of the cache controller.

13. A system, comprising:

an external memory device; and

an integrated circuit including:

a microprocessor;

a multipurpose memory coupled with the microprocessor;

a cache controller coupled with the multipurpose memory;

a first memory port for coupling the external memory device with said cache controller; and

a second memory port for coupling a second external memory device with said multipurpose memory,

wherein said first and second memory ports are not simultaneously active to pass data to said multipurpose memory

wherein the multipurpose memory has a first operating mode for dynamically storing portions of a program obtained from the external memory device for execution by the microprocessor under control of the cache controller, and the multipurpose memory has a second operating mode for storing an entire program obtained from the second external memory device to be run by the microprocessor.

14. The system of claim **13**, wherein the external memory device is a Flash ROM.

15. The system of claim **14**, wherein the second memory port is adapted to be coupled with an EEPROM as the second external memory device.

16. The system of claim **13**, wherein the multipurpose memory has a first operating mode for dynamically storing portions of a program obtained from the external memory device for execution by the microprocessor under control of the cache controller.

17. The system of claim **13**, wherein the second memory port is a serial peripheral interface.

* * * * *

EXHIBIT F

US008373455B1

(12) **United States Patent**
McLaughlin et al.

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(45) **Date of Patent: Feb. 12, 2013**

(54) **OUTPUT BUFFER CIRCUIT**

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H03B 1/00 (2006.01)
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(52) **U.S. Cl.** **327/112**; 327/108; 327/109; 327/110; 327/111; 327/170

(58) **Field of Classification Search** 327/108–112, 327/170
See application file for complete search history.

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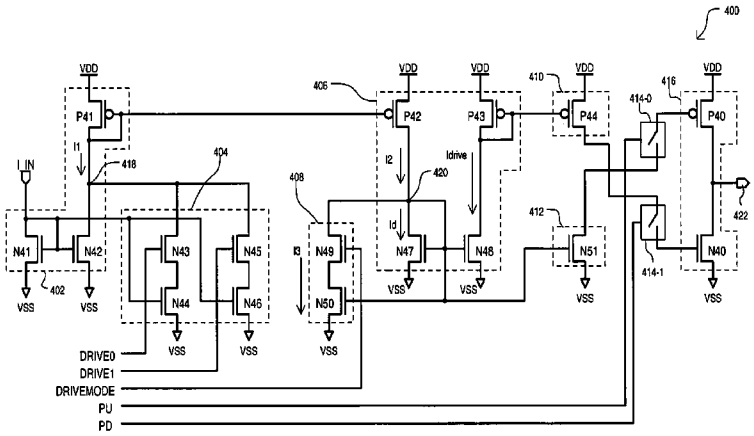
(57) **ABSTRACT**

An output driver circuit can include at least a first driver transistor having a source-drain path coupled between a first power supply node and an output node. A first variable current supply can generate a current having at least one component that is inversely proportional to a power supply voltage. A first driver switch element can be coupled in series with the first variable current supply between a gate of the at least first driver transistor and a second power supply node.

14 Claims, 4 Drawing Sheets



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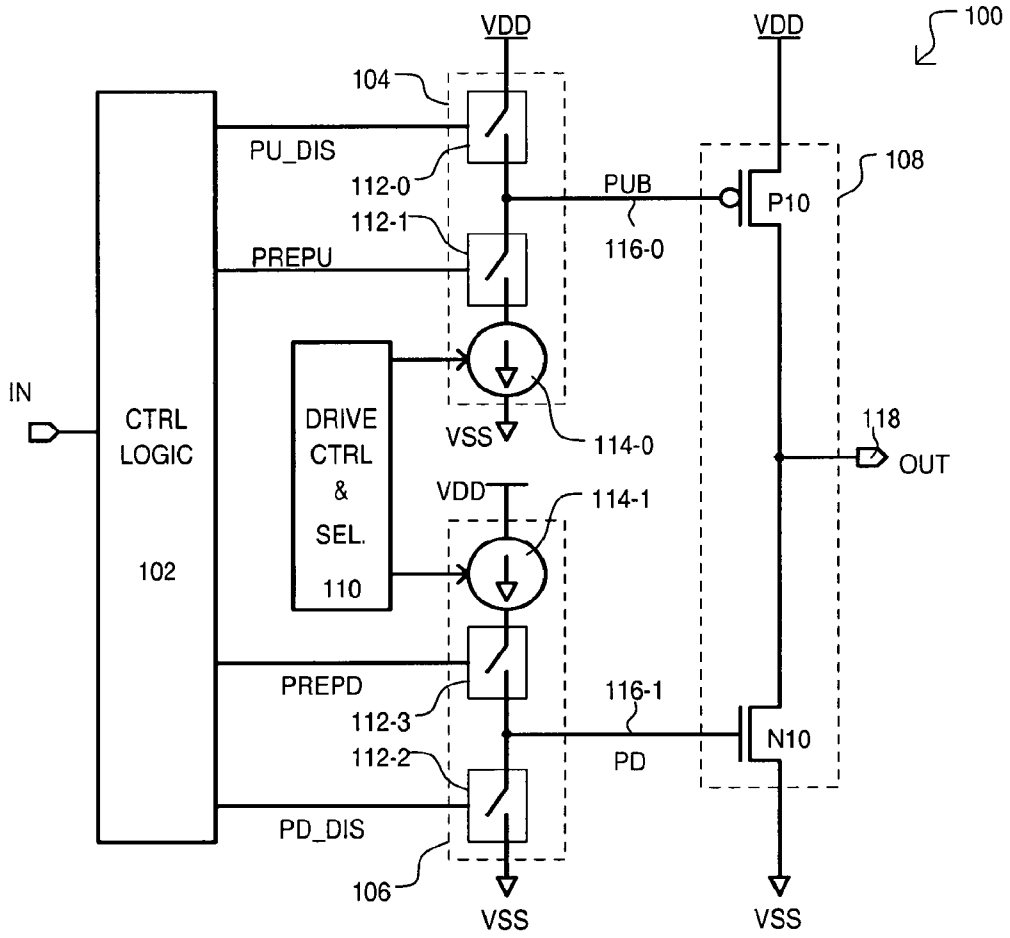
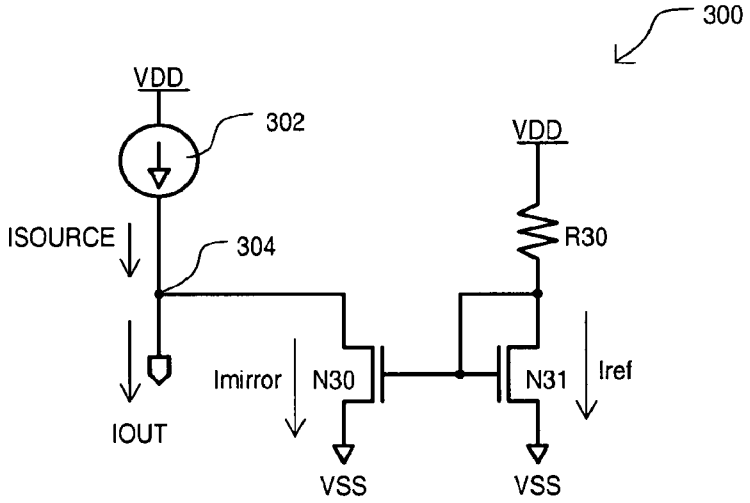

VDD
VDD
100
104
PU_DIS
112-0
112-1
PREPU
PUB
116-0
108
P10
IN
CTRL
LOGIC
102
DRIVE
CTRL
&
SEL.
110
VSS
114-0
118
OUT
VDD
114-1
PREPD
112-3
112-2
116-1
PD
N10
PD_DIS
106
VSS
VSS

FIG. 1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VDD
302
VDD
ISOURCE
304
R30
Imirror
N30
N31
Iref
IOUT
VSS
VSS

FIG. 3

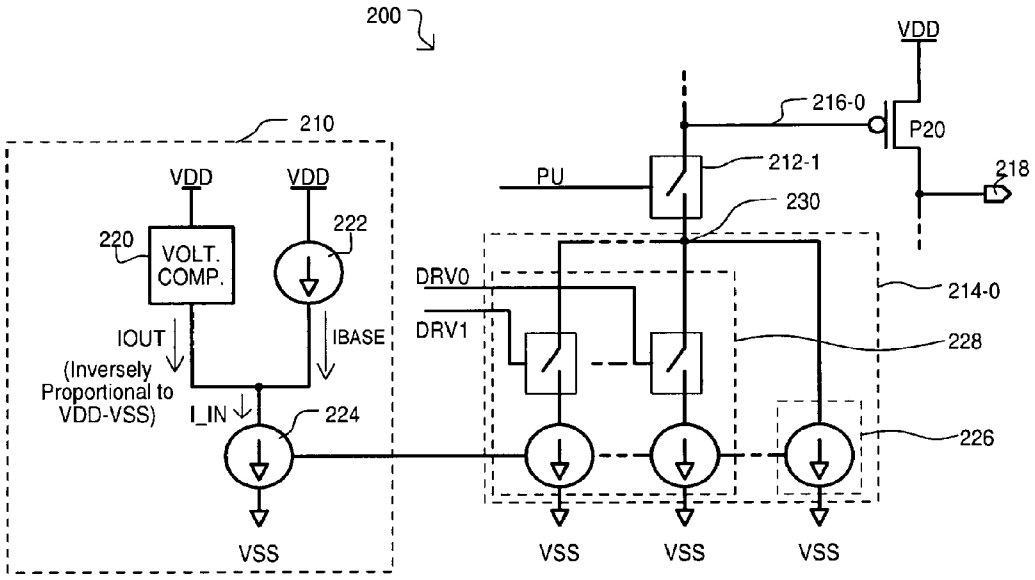
200
210
VDD
VDD
220
VOLT. COMP.
222
IOUT
(Inversely Proportional to VDD-VSS)
IBASE
I_IN
224
VSS
VDD
216-0
P20
PU
212-1
218
230
DRV0
DRV1
214-0
228
226
VSS
VSS
VSS

FIG. 2A

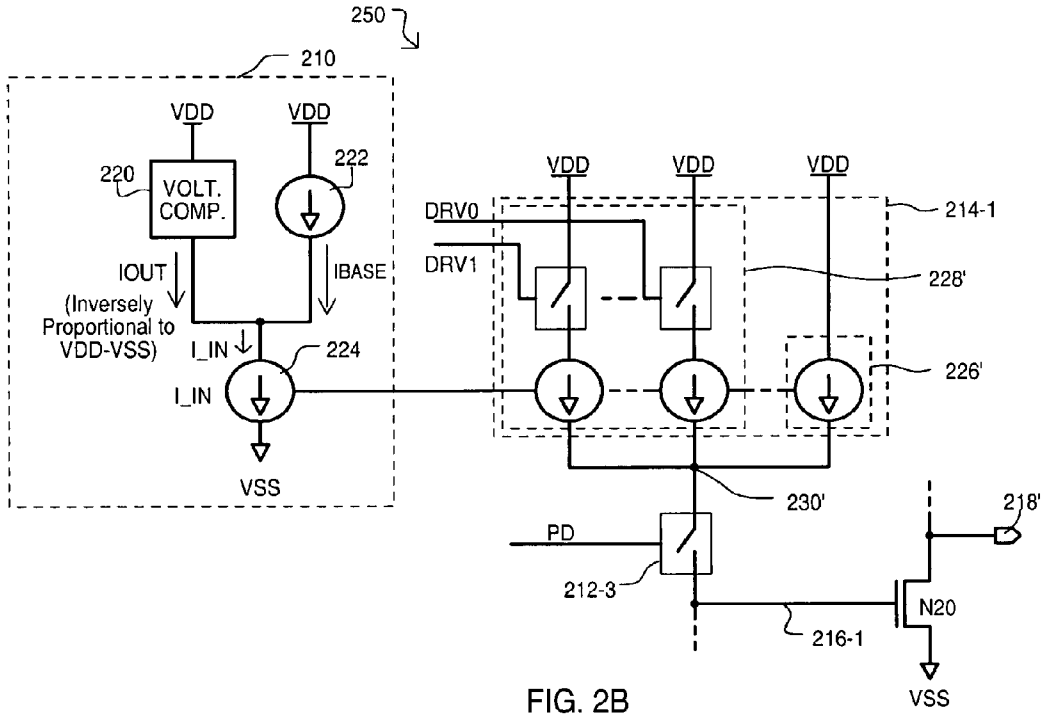
250
210
VDD
VDD
220
VOLT. COMP.
222
IOUT
(Inversely Proportional to VDD-VSS)
IBASE
I_IN
224
I_IN
VSS
VDD
VDD
VDD
DRV0
DRV1
214-1
228'
226'
230'
218'
PD
212-3
N20
216-1
VSS

FIG. 2B

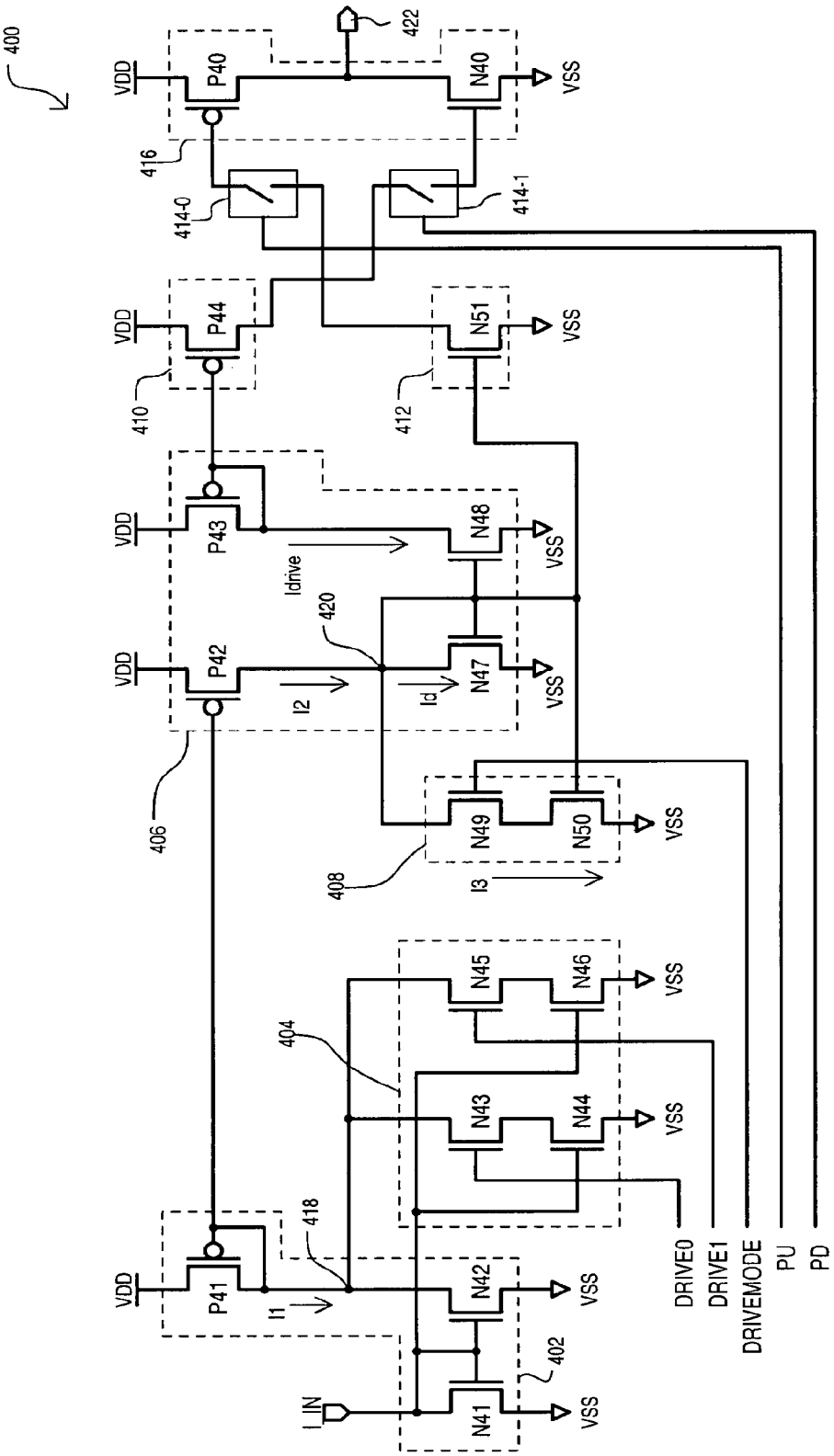
400
VDD
P40
N40
VSS
422
416
414-0
414-1
P44
N51
410
412
P43
N48
Idrive
420
P42
N47
I2
Id
406
N49
N50
408
I3
N45
N46
404
N43
N44
418
P41
I1
N42
402
I_IN
N41
DRIVE0
DRIVE1
DRIVEMODE
PU
PD

FIG. 4

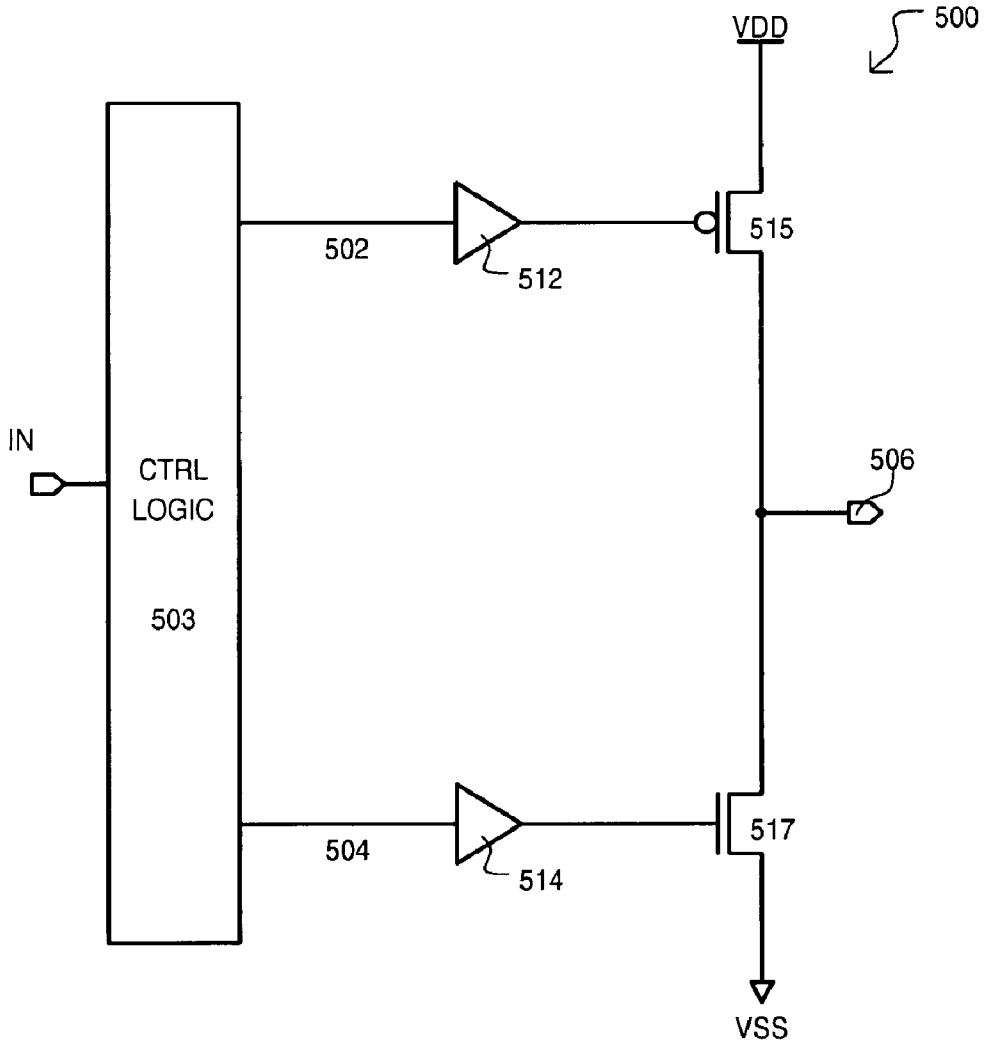

FIG. 5 (BACKGROUND ART)

OUTPUT BUFFER CIRCUIT

RELATED APPLICATIONS

This application is a continuation of U.S. Non-Provisional Application Ser. No. 11/904,901 filed Sep. 27, 2007 and claims priority to U.S. Provisional Application No. 60/847,554 filed on Sep. 27, 2006, both of which are incorporated herein by reference.

TECHNICAL FIELD

The present invention relates generally to output buffers and more particularly to single ended output buffers.

BACKGROUND OF THE INVENTION

In an integrated circuit, output buffers are often used at output pins to transfer signals to the signal lines. The transmission of information across the signal lines can be subject to various problems such as impedance mismatch, signal reflection, or irregular output waveform. Typically, output buffers must meet specifications dictated by application, such as maintaining a smooth and robust output waveform.

FIG. **5** shows a block diagram of a conventional output buffer **500** that can drive an output **506** between a high (e.g., VDD) and low (e.g., VSS) level in response to an input signal IN. The conventional output buffer **500** can include control logic **503**, a first driver **512**, a second driver **514**, a p-channel output transistor **515** and an n-channel output driver transistor **517**. In response to a logic output signal **502** from control logic **503**, first driver **512** can drive a gate of p-channel output transistor **515** between a high power supply level (e.g., VDD) to turn the transistor off, and a low power supply level (e.g., VSS) to turn the transistor on. In an opposite fashion, in response to a logic output signal **504** from control logic **503**, second driver **514** can drive a gate of n-channel output transistor **515** between a low power supply level (e.g., VSS) to turn the transistor off, and a high power supply level (e.g., VDD) to turn the transistor on. P-channel output transistor **515** and n-channel output transistor **517** can be large output driving devices and thus include relatively large gates that can present a significant capacitance to their respective drivers (**512** and **514**).

Control logic **503** can output signals to control the operation of the output buffer. For example, an output **506** can be driven high by turning on p-channel output transistor **515** and turning off n-channel output transistor **517**, or can be driven low by turning off p-channel output transistor **515** and turning on n-channel output transistor **517**. An output **506** could also be placed in a high impedance state (i.e., tristate) by turning off both output transistors (**515** and **517**).

A disadvantage of conventional output buffer **500** can be the limited flexibility in meeting variations arising from different applications. While a drive strength of a conventional output buffer **500** can be increased by adding additional driver devices in parallel, doing so may only just meet a minimum output impedance necessary to reduce signal reflections on a transmission line driven by the buffer.

Another disadvantage of conventional output buffer **500** can be sensitivity to operating conditions. While an output buffer **500** can be tuned to meet worst case load conditions, if an actual output transmission line is less than such worst case, it can be difficult to meet driving requirements, such as rise time and fall time, particularly across uncontrollable variations in manufacturing process, differing operating voltages, and/or temperatures.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block schematic diagram of a first embodiment of the present invention.

FIGS. **2**A and **2**B show one way of conceptualizing pull-up and pull-down paths according to an embodiment.

FIG. **3** is a block schematic diagram of a voltage compensation circuit that can be included in the embodiments.

FIG. **4** shows a tuning circuit according to an embodiment of the invention.

FIG. **5** shows a conventional output driver circuit.

DETAILED DESCRIPTION

Various embodiments of the present invention will now be described in detail with reference to a number of drawings. The embodiments show output driver circuits that can vary drive strength according to supply voltage conditions and/or provide programmable drive strength. As a result, an output buffer can meet performance requirements over a range of operating voltages. Further, programmability of drive strength can enable the output buffer to be configured to provide a desired signal profile despite variations in transmission line load.

Referring now to FIG. **1**, an output driver is shown in a block schematic diagram and designated by the general reference character **100**. An output buffer **100** can include control logic **102**, pull-up predriver circuit **104**, pull-down predriver circuit **106**, driver section **108**, and current control section **110**. Control logic **102** can receive an input signal IN, and in response, generate control output signals for controlling predriver circuits (**106** and **104**). In the particular example of FIG. **1**, such control output signals include a pull-up disable signal (PU_DIS), pull-up enable signal (PREPU), pull-down disable signal (PD_DIS), pull-down enable signal (PREPD).

A pull-up predriver circuit **104** can include a first switch element **112-0**, a second switch element **112-1**, and a first variable current source **114-0**. A first switch element **112-0** can provide a low or high impedance path between a high power supply node VDD and a first driver control node **116-0** in response to signal PU_DIS. A second switch element **114-0** can provide a high or low impedance path between first driver control node **116-0** and first variable current source **114-0** in response to signal PREPU. First variable current source **114-0** can provide a current that is controllable according to current control section **110**. More particularly, in response to a current control section **110**, a variable current source **114-0** can source a current from first control node **116-0** (provided switch element **112-1** is in a low impedance state) that can vary inversely with respect to a power supply voltage and/or can be programmable.

A pull-down predriver circuit **106** can include a third switch element **112-2**, a fourth switch element **112-3**, and a second variable current source **114-1**. A third switch element **112-2** can provide a low or high impedance path between a low power supply node VSS and a second driver control node **116-1** in response to signal PD_DIS. A fourth switch element **112-3** can provide a high or low impedance path between second driver control node **116-1** and second variable current source **114-0** in response to signal PREPD. Like first variable current source **114-0**, second variable current source **114-1** can provide a current controlled by current control section **110** that preferably varies inversely with respect to a power supply voltage and/or can be programmable.

A driver section **108** can include a p-channel insulated gate field effect transistor (hereinafter PFET) P**10** and an n-channel FET (NFET) N**10**. PFET P**10** can have a source-drain path connected between a high power supply node VDD and an output node **118**. A gate of PFET P**10** can be connected to first driver control node **116-0**. In such an arrangement, a rising

edge of an output signal can be generated at output node **118** by disabling first switch element **112-0** and enabling second switch element **112-1**. This can cause a potential at the gate of PFET P**10** to fall according to the current drawn by first variable current source **114-0**. This is in contrast to conventional arrangements that can drive a gate of an output PFET P**10** by switching it to a low power supply VSS. PFET P**10** can be disabled by disabling second switch element **112-1** and enabling first switch element **112-0**, thereby connecting its gate to a high power supply node VDD. By providing a strong second switch element **112-1**, large crowbar currents through output driver can be reduced or avoided as output PFET P**10** can be turned off quickly.

NFET N**10** can have a source-drain path connected between a low power supply node VSS and an output node **118**. A gate of NFET N**10** can be connected to second driver control node **116-1**. In such an arrangement, a falling edge of an output signal can be generated at output node **118** by disabling third switch element **112-2** and enabling fourth switch element **112-3**. This can cause a potential at the gate of NFET N**10** to rise according to the current supplied by second variable current source **114-1**. This is in contrast to conventional arrangements that can drive a gate of an output NFET by switching its gate to a high power supply VDD. NFET P**10** can be disabled by disabling fourth switch element **112-3** and enabling third switch element **112-2**, thereby connecting its gate to a low power supply node VSS. As the case of PFET P**10**, providing a strong fourth switch element **112-3** can reduce or eliminate large crowbar currents through driver section **108**.

In this way, an output buffer can include output driver transistors that are enabled in response to current sources sinking or sourcing a current that can vary according to supply voltage and/or are programmable. Thus, drive strength of such devices can be varied without increasing or decreasing the number of driver devices, as is done in some conventional approaches.

Referring now to FIGS. **2**A and **2**B portions of an output buffer circuit according to other embodiments are shown in block schematic diagrams. FIG. **2**A shows one way of conceptualizing a pull-up path of an output driver. FIG. **2**B shows one way of conceptualizing a pull-down path of an output driver.

Referring now to FIG. **2**A, a pull-up path is shown in a block schematic diagram and designated by the general reference character **200**. A pull-up path **200** can include sections shown in FIG. **1**, thus like sections are referred to by the same reference character but with the first digit being a "2" instead of "1". A pull-up path **200** can include current control section **210**, switch element **212-1**, variable current source **214-0**, and output driver PFET P**20**. A current control section **210** can provide a current I_IN that varies in response to a power supply voltage. In the particular example shown, a current control section **210** can include a voltage compensation circuit **220**, a base current source **222**, and current mirror source **224**. A voltage compensation circuit **220** can provide a current IOUT that varies inversely with power supply voltage. That is, as a power supply voltage increases (e.g., VDD-VSS), current IOUT decreases. Conversely, as power supply decreases, current IOUT can increase. A current IOUT can be added with a constant current IBASE provided by base current source **222**, to create a current I_IN for current mirror source **224**.

A variable current source **214-0** can include a static section **226** and a programmable section **228**. A static section **226** can include a current source that mirrors the current passing through current mirror source **224** and draws current from a current control node **230**. Thus, a current drawn by static section **226** can also vary inversely with a power supply voltage. In a similar fashion, a programmable section **228** can include one or more current sources that mirror the current passing through current mirror source **224**. Such current sources can be arranged in parallel with one another with respect to current control node **230**. However, unlike static section **226**, current sources within programmable section **228** can be switched into current control node **228** to vary that amount of current drawn at current control node **230**. In the particular example shown, signals DRV**0** and DRV**1** can control the current sources of programmable section **228**.

A switch element **212-1** can selectively connect a driver control node **216-0** to variable current source **214-0**, to thereby drive a gate of PFET P**20** low, to pull output node **218** toward VDD.

In this way, a pull-up device in an output driver can be controlled by a variable current source sinking a current with a magnitude that is both programmable and inversely related to a power supply level.

Referring now to FIG. **2**B, a pull-down path is shown in a block schematic diagram and designated by the general reference character **250**. A pull-down path **250** can include sections shown in FIG. **1**, thus like sections are referred to by the same reference character but with the first digit being a "2" instead of "1". A pull-down path **250** can include current control section **210**, switch element **212-3**, variable current source **214-1**, and output driver NFET N**20**.

A current control section **210** can provide a current I_IN in the same fashion as described with reference to FIG. **2**A.

A variable current source **214-1** can have the same general configuration as variable current source **214-0**, except that current is sourced to a common current control node **230'**.

A switch element **212-3** can selectively connect a driver control node **216-1** to variable current source **214-1**, to thereby enable NFET N**20**, and drive output node **218** toward VSS.

In this way, a pull-down device in an output driver can be controlled by a variable current source sourcing a current with a magnitude that is both programmable and inversely related to a power supply level.

FIGS. **2**A and **2**B thus show how can an output driver to be tuned for a given output transmission line by altering a current drive amount, and not the number of active drivers. Further, such a driving current can be inversely proportional to a power supply voltage and thus be capable of operating over a wide range of power supply levels.

Referring now to FIG. **3**, a voltage compensation circuit is shown in a block schematic diagram and designated by the general reference character **300**. A voltage compensation circuit **300** can correspond to that shown as **220** in FIGS. **2**A and **2**B. A voltage compensation circuit **300** can include a current mirror formed by NFETs N**30** and N**31**, a reference load R**30**, and a current source **302**. NFET N**31** can have a source connected to a low power supply node VSS, a gate connected to its drain, and a drain connected to reference load R**30**. NFET N**30** can have a source connected to a low power supply node VSS, a gate connected to the gate of N**31**, and a drain connected to a current out node **304**.

As shown in FIG. **3**, NFET N**31** can draw a current Iref. This current can be mirrored by NFET N**30** to draw a current Imirror. That is, if NFETs N**30** and N**31** are matched in size, such currents can be the same, and if NFETs N**30** and N**31** are scaled with respect to one another, such currents can vary according to their scaling factor. A current ISOURCE provided by current source **302** can be a constant current.

In the arrangement of FIG. **3**, as a power supply voltage increases, current Iref (and hence current Imirror) can increase. This can shunt current away from current out node **304**, reducing the magnitude of output current IOUT. On the other hand, as a power supply voltage decreases, current Iref (and hence current Imirror) can decrease. This can shunt less current away from current out node **304**, thus output current IOUT can increase in magnitude.

In this way a current can be provided that can be inversely proportional to a power supply voltage.

While the embodiments of FIGS. **2**A and **2**B show one way of conceptualizing the current drivers, in a preferred embodiment a common voltage compensated current can be utilized to generate a drive current for both pull-up and pull-down devices by a series of current mirrors. An example of such an arrangement is shown in FIG. **4**.

Referring to FIG. **4**, an output driver tuning circuit is shown in a schematic diagram and designated by the general reference character **400**. A tuning circuit **400** can include an input current circuit **402**, a programmable switching section **404**, a current driver section **406**, a drive strength modulator **408**, pull-down current source **410**, pull-up current source **412**, pull-up switch element **414-0**, pull-down switch element **414-1**, output driver section **416**.

An input current section **402** can include a current mirror formed by NFETs N**41** and N**42** and load PFET P**41**. NFET N**41** can have a drain that receives a voltage compensated input current I_IN. In one particular arrangement, a current I_IN can be generated by circuits like those shown as **210** in FIGS. **2**A and **2**B and/or **300** in FIG. **3**. That is, current I_IN can be inversely proportional to a supply voltage. Current I_IN can be mirrored by NFET N**42** and thus draw current at node **418**. Load PFET P**41** can be connected to node **418** in a "diode" configuration (its drain and gate connected to the node, its source connected to a high power supply node VDD).

Programmable switching section **404** can include one or more selectable legs to vary the amount of current drawn at node **418**. In the particular example of FIG. **4**, programmable switching section **404** includes two legs, one formed by series connected NFETs N**43**/N**44**, the other leg formed by series connected NFETs N**45**/N**46**. NFETs N**44** and N**45** within each leg can have gates connected to the gate of current mirror N**41**/N**42**, and thus can draw a current that mirrors input current I_IN (i.e., these currents are also supply voltage compensated). Each leg of programmable switching section **404** can be enabled by a corresponding drive select signal DRIVE**0** or DRIVE**1** .

In such an arrangement, a current I**1** drawn at node **418** can include that drawn by NFET N**42**, and any additional current draw switched in by switching section **404**. Any of NFETs N**42**, N**44** and N**46** can be scaled with respect to NFET N**41** to provide a desired programmability range.

A current driver section **406** can include mirror PFET P**42**, a drive current mirror N**47**/N**48**, and a drive PFET P**43**. PFET P**42** can be connected in a current mirror fashion to load PFET P**41**, and thus can provide a current I**2** to node **420** that mirrors I**1**. Drive current mirror N**47**/N**48** can receive a current Id from node **420**, and mirror such current to generate a current Idrive that flows from PFET P**43** to NFET N**48**.

A drive strength modulator **408** can include NFETs N**49** and N**50** arranged in series with one another between node **420** and a low power supply node **408**. In such an arrangement, when drive strength modulator is disabled (NFET N**49** off), current Idrive can essentially mirror current I**2**. In contrast, when drive strength modulator is enabled (NFET N**49** on), the scaling factor between the different legs of current driver section **406** can be changed, as NFET N**50** is added in parallel with NFET N**47**. As a result current Idrive can be reduced.

Pull-down current source **410** can include a PFET P**44** having a gate connected in a current mirror fashion to that of PFET **43**. Thus, PFET P**44** can source a current that mirrors current Idrive. Similarly, pull-up current source **412** can include an NFET N**51** having a gate connected in a current mirror fashion to a gate of NFET N**47**, and thus sink a current that mirrors current Id (and hence Idrive).

An output driver section **416** can have the same structure as that shown as **108** in FIG. **1**, and include driver PFET P**40** and driver NFET N**40**.

Pull-up switch element **414-0** can be connected between a gate of driver PFET P**40** and pull-up current source **412**. Thus, when pull-up switch element **414-0** is enabled in response to signal PU, driver PFET P**40** can drive output node **422** high based on a current Id. In a similar fashion, pull-down switch element **414-1** can be connected between a gate of driver NFET N**40** and pull-down current source **410**. Thus, when pull-down switch element **414-1** is enabled in response to signal PD, driver NFET N**40** can drive output node **422** low based on current Idrive.

Again, due to the current mirroring of tuning circuit **400** currents Id/Idrive are inversely proportional to a power supply voltage.

Output driver circuits according to the embodiments can provide for rise and fall times that can meet a same specification under varying voltage supply conditions, as a drive strength is determined by sinking or sourcing a current that varies with power supply voltage levels.

In addition or alternatively, output driver circuits according to the embodiments can provide for a selectable rise and fall time, by enabling any of multiple current sources to increase and/or decrease a current that controls the drive strength of the output buffer. As but one example, for a worst case load condition, a first number of current sources can be enabled to provide a relatively fast switching speed. For load conditions less than a worst case, fewer current sources can be enabled, thus slowing down the rise/fall times appropriately. Such load-drive matching can reduce electromagnetic interference (EMI) in systems that drive signals between various locations.

Embodiments of the present invention can be employed as output drivers for various integrated circuits. As but one particular example, such an output driver may be particularly suitable for driving an output clock signal that can control the timing of other circuits in a larger system.

Embodiments of the present invention are well suited to performing various other steps or variations of the steps recited herein, and in a sequence other than that depicted and/or described herein. In one embodiment, such a process is carried out by processors and other electrical and electronic components, e.g., executing computer readable and computer executable instructions comprising code contained in a computer usable medium.

For purposes of clarity, many of the details of the improved solution and the methods of designing and manufacturing the same that are widely known and are not relevant to the present invention have been omitted from the following description.

It should be appreciated that reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Therefore, it is emphasized and should be appreciated that two or more references to "an embodiment" or "one embodiment" or "an

alternative embodiment" in various portions of this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures or characteristics may be combined as suitable in one or more embodiments of the invention.

Similarly, it should be appreciated that in the foregoing description of exemplary embodiments of the invention, various features of the invention are sometimes grouped together in a single embodiment, figure, or description thereof for the purpose of streamlining the disclosure aiding in the understanding of one or more of the various inventive aspects.

What is claimed is:

1. An output driver circuit, comprising:

at least a first driver transistor having a source-drain path coupled between a first power supply node and an output node;

a first variable current supply that generates a current having at least one component that is inversely proportional to a power supply voltage; and

a first driver switch element coupled in series with the first variable current supply between a gate of the at least first driver transistor and a second power supply node, wherein the first driver switch and the first variable current supply are configured to control a rise time of the output driver circuit.

2. The output driver circuit of claim **1**, wherein:

the at least first driver transistor includes a p-channel insulated gate field effect transistor, the first power supply node is a high power supply node and the second power supply node is a low power supply node.

3. The output driver circuit of claim **1**, further including:

at least a second driver transistor having a source-drain path coupled between the second power supply node and the output node; and

a second variable current supply that generates a current having at least one component that is inversely proportional to the power supply voltage; and

a second driver switch element coupled in series with the second variable current supply between a gate of the at least second driver transistor and the first power supply node, wherein the second driver switch and the second variable current supply are configured to control a fall time of the output driver circuit.

4. The output driver circuit of claim **1**, wherein:

the first variable current supply comprises a supply current source that provides source current to a reference current node, and a current mirror that shunts current away from the reference current node.

5. The output driver circuit of claim **4**, wherein:

the current mirror includes an output mirror transistor having a source-drain path in series with the supply current source and in parallel with the reference current output node, a reference mirror transistor having a gate coupled to a gate of the output mirror transistor and to its drain, an impedance element coupled to the drain of the reference mirror transistor.

6. The output driver circuit of claim **1**, wherein:

the first variable current supply includes a selectable current supply circuit that includes a current mirror having a reference current leg that receives a current having at least one component that is inversely proportional to the power supply voltage, a mirror current leg coupled to a selectable drive current node that mirrors the current flowing in the reference current leg, at least one first selectable mirror leg coupled to the selectable drive current node and coupled to mirror the current flowing in the reference current leg, and a mirror switch coupled in series with the at least one selectable mirror leg that is enabled in response to a drive signal.

7. An output driver circuit, comprising:

a first driver transistor that provides a low impedance path to an output node in response to a voltage at a first driver control node;

a first switch element coupled between the first driver control node and a first power supply node; and

a selectable current source coupled between the first driver control node and a second power supply node, the selectable current source generating a drive current that varies in response to a drive select value,

wherein the selectable current source includes a plurality of selectable current legs, each connected to a current control node and enabled to provide a current to the current control node in response to a corresponding drive control signal.

8. The output driver circuit of claim **7**, wherein:

the selectable current source includes a drive current source circuit, and a first drive current switch element coupled in series with the current source circuit between the first driver control node and the second power supply node.

9. The output driver circuit of claim **7**, wherein:

the selectable current source further includes a reference current source that provides a reference current having at least one component that is inversely proportional to a power supply voltage, and each of the selectable current legs provides a current proportional to the reference current.

10. The output driver circuit of claim **7**, wherein:

the plurality of selectable current legs includes a drive current leg that provides a pre-drive current to a drive node, a drive strength modulator that selectively shunts current from the drive node in response to a drive strength control signal, and the drive current is proportional to the current at the drive node.

11. An output driver circuit, comprising:

a first driver transistor that provides a low impedance path to an output node in response to a voltage at a first driver control node;

a second driver transistor that provides a low impedance path to the output node in response to a voltage at a second driver control node; and

a first switch element coupled between the first driver control node and a first power supply node, and between the second driver control node and the first power supply node, the selectable current source generating a drive current that varies in response to a drive select value.

12. The output driver circuit of claim **11**, further including:

a second switch element coupled between the second driver control node and the second power supply node.

13. The output driver circuit of claim **7**, further including:

a control logic circuit that selectively enables the first switch element and selectable current source in response to at least one input signal.

14. The output driver circuit of claim **3**, wherein:

the second driver transistor includes an n-channel insulated gate field effect transistor, and the first power supply node is a high power supply node and the second power supply node is a low power supply node.

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