

United States Patent [19]
Cowles

[11] Patent Number: 5,729,504
[45] Date of Patent: Mar. 17, 1998

- [54] CONTINUOUS BURST EDO MEMORY DEVICE
- [75] Inventor: Timothy B. Cowles, Boise, Id.
- [73] Assignee: Micron Technology, Inc., Boise, Id.
- [21] Appl. No.: 572,487
- [22] Filed: Dec. 14, 1995
- [51] Int. Cl.⁶ G11C 8/00
- [52] U.S. Cl. 365/236; 365/238.5; 365/239; 395/496
- [58] Field of Search 365/236, 238.5, 365/239; 395/496

"4DRAM 1991", *Toshiba America Electronic Components, Inc.*, pp. A-137—A-159.

"Application Specific DRAM", *Toshiba America Electronic Components, Inc.*, C178, C-260, C 218, (1994).

"Burst DRAM Function & Pinout", *Oki Electric Ind., Co., Ltd., 2nd Presentation, Item #619*, (Sep. 1994)

(List continued on next page.)

Primary Examiner—David C. Nelms
Assistant Examiner—F. Niranjana
Attorney, Agent, or Firm—Schwegman, Lundberg, Woessner & Kluth, P.A.

[56] References Cited

U.S. PATENT DOCUMENTS

4,344,156	8/1982	Eaton et al.	365/203
4,484,308	11/1984	Lewandowski et al.	364/900
4,562,555	12/1985	Ouchi et al.	365/233
4,567,579	1/1986	Patel et al.	365/189
4,575,825	3/1986	Ozaki et al.	365/189
4,603,403	7/1986	Toda	365/189

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

19507562 9/1995 Germany .

OTHER PUBLICATIONS

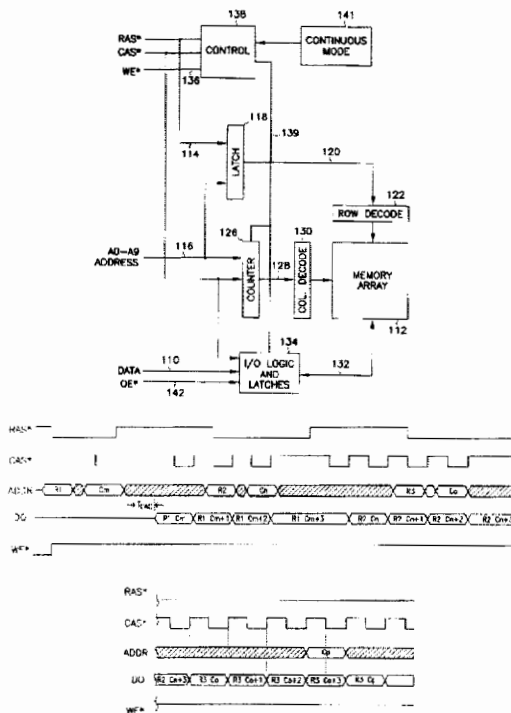
"Dram 1 Meg X 4 Dram 5Vedo Page Mode", *1995 DRAM Data Book*, pp. 1-1 thru 1-30, (Micron Technology, I).

"Rossini, Pentium, PCI-ISA, Chip Set", *Symphony Laboratories*, entire book.

[57] ABSTRACT

An integrated circuit memory device is described which can operate at high data speeds. The memory device can either store or retrieve data from the memory in a burst access operation. The burst operations latch a memory address from external address lines and internally generates additional memory addresses. The integrated circuit memory can output data in a continuous stream while new rows of the memory are accessed. A method and circuit are described for outputting a burst of data stored in a first row of the memory while accessing a second row of the memory.

20 Claims, 7 Drawing Sheets



IPR2021-00167

U.S. PATENT DOCUMENTS

4,618,947	10/1986	Tran et al.	365/230
4,649,522	3/1987	Kirsch	365/189
4,685,089	8/1987	Patel et al.	365/233
4,707,811	11/1987	Takemae et al.	365/239
4,788,667	11/1988	Nakano	365/193
4,870,622	9/1989	Aria et al.	365/230
4,875,192	10/1989	Matsumoto	365/193
5,058,066	10/1991	Yu	365/189.05
5,126,975	6/1992	Handy et al.	365/230
5,257,200	10/1993	Tobita	365/189
5,268,865	12/1993	Takasugi	365/189
5,280,594	1/1994	Young et al. .	
5,305,284	4/1994	Iwase	365/238.5
5,325,330	6/1994	Morgan	365/189.05
5,325,502	6/1994	McLaury	395/425
5,349,566	9/1994	Merritt et al.	365/233.5
5,357,469	10/1994	Sommer et al.	365/193
5,373,227	12/1994	Keeth	323/313
5,379,261	1/1995	Jones, Jr.	365/230
5,392,239	2/1995	Margulis et al.	365/189
5,410,670	4/1995	Hansen et al.	365/425
5,452,261	9/1995	Chung et al.	365/233
5,457,659	10/1995	Schaefer	365/222
5,526,320	6/1996	Zagar et al.	365/233.5

OTHER PUBLICATIONS

"Hyper Page Mode DRAM", *8029 Electronic Engineering*, 66, No. 813, Woolwich, London, GB, pp. 47-48, (Sep. 1994).

"Mosel-Vitellic V53C8257H DRAM Specification Sheet, 20 pages, Jul. 2, 1994".

"Pipelined Burst DRAM", *Toshiba, JEDEC JC 42.3 Hawaii*, (Dec. 1994).

"Samsung Synchronous DRAM", *Samsung Electronics*, pp. 1-16, (Mar. 1993).

"Synchronous DRAM 2 MEG x 8 SDRAM", *Micron Semiconductor, Inc.*, pp. 2-43 through 2-8.

Dave Bursky, "Novel I/O Options and Innovative Architectures Let DRAMs Achieve SRAM Performance; Fast DRAMS can be swapped for SRAM Caches", *Electronics Design*, vol. 41, No. 15, Cleveland, Ohio, pp. 55-67, (Jul. 22, 1993).

Shiva P. Gowni, et al., "A 9NS, 32K X 9, BICMOS TTL Synchronous Cache RAM With Burst Mode Access", *IEEE, Custom Integrated Circuits Conference*, pp. 781-786, (Mar. 3, 1992).

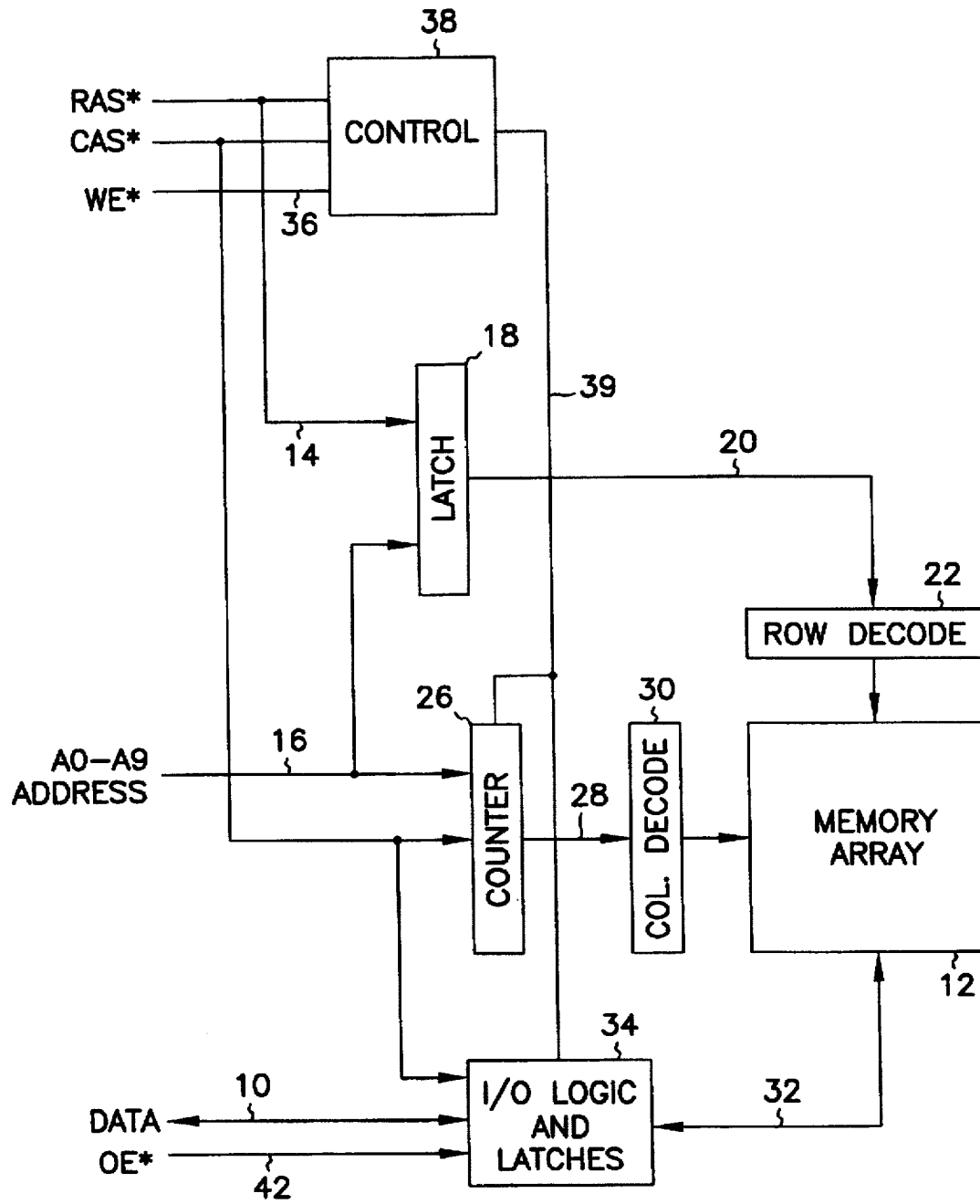


FIG. 1 (PRIOR ART)

Burst Length	Starting Column Address			Linear	Interleave
	A ₂	A ₁	A ₀		
2	V	V	0	0-1	0-1
	V	V	1	1-0	1-0
4	V	0	0	0-1-2-3	0-1-2-3
	V	0	1	1-2-3-0	1-0-3-2
	V	1	0	2-3-0-1	2-3-0-1
	V	1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

FIG. 2
(PRIOR ART)

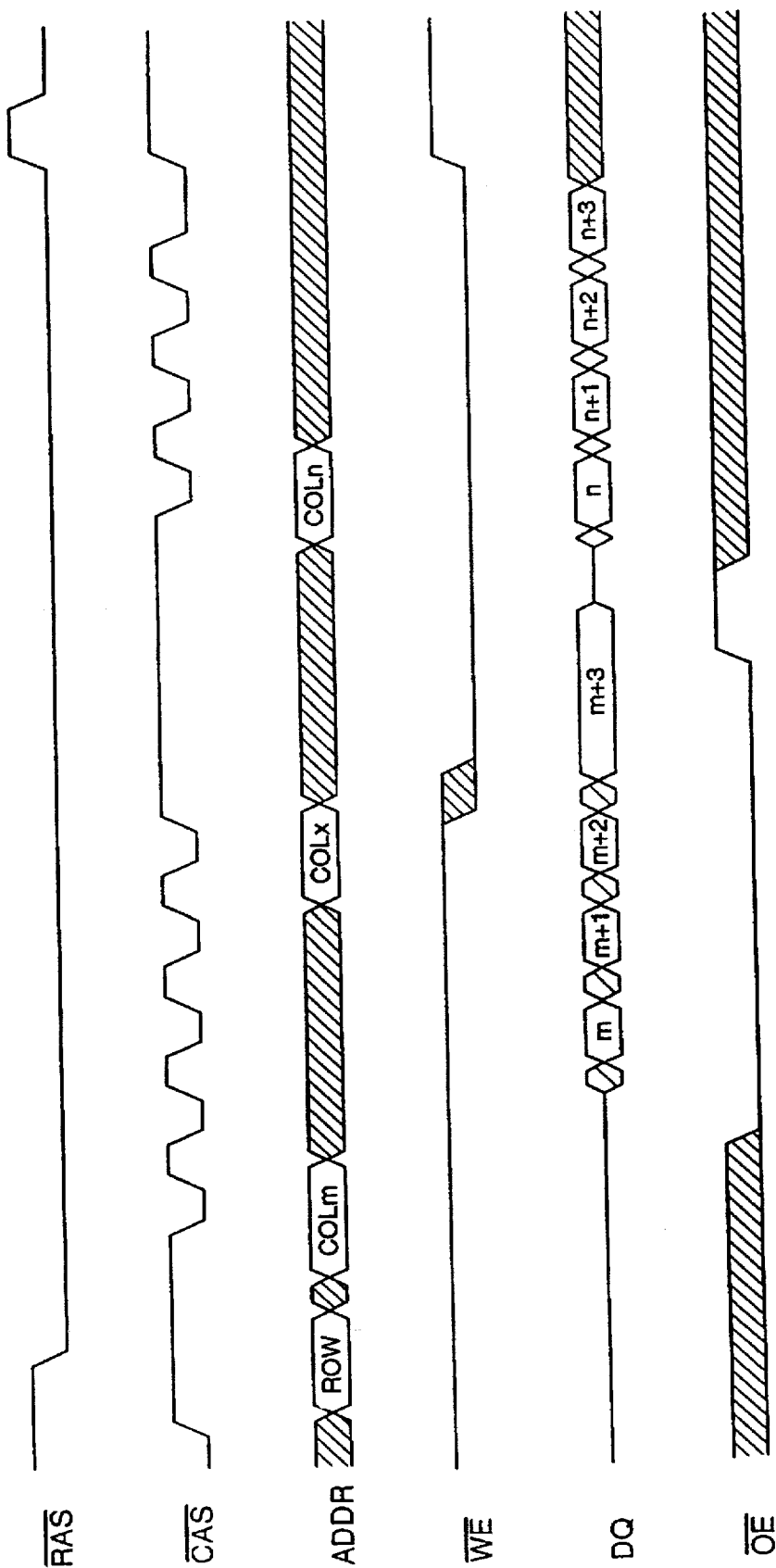


FIG. 3 (PRIOR ART)

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts



Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research



With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips



Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.