IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

MONTEREY RESEARCH, LLC, Plaintiff, vs. NANYA TECHNOLOGY CORPORATION, NANYA TECHNOLOGY CORPORATION, U.S.A., and NANYA TECHNOLOGY CORPORATION DELAWARE, Defendants.	Civil Action No. 19-2090 (NIQA)

NANYA DEFENDANTS' INITIAL PROPOSED CONSTRUCTIONS

Pursuant to the Court's Scheduling Order Governing (Dkt. 38 at 7), Defendants Nanya Technology Corporation, Nanya Technology Corporation, U.S.A., and Nanya Technology Corporation Delaware (collectively "Nanya") hereby identify preliminary claim constructions for terms identified by the parties.

Nanya reserves the right to modify or supplement these disclosures to facilitate agreement with Monterey, to avoid duplication of terms or phrases, or to reflect newly received information. Furthermore, Nanya reserves the right to modify or supplement its preliminary proposed constructions once it has had an opportunity to review Monterey's preliminary proposed constructions.

Nanya's list of preliminary proposed constructinos has been compiled in response to Monterey's November 20, 2020 Preliminary Disclosure of Asserted Claims and Infringement Contentions. To the extent that Monterey may amend its contentions, Nanya reserves the right to modify the preliminary proposed constructions below. Nanya reserves the right to offer evidence and argument regarding the construction of any terms or elements that are identified by Monterey, or to argue for a plain meaning where it is evident that Monterey's apparent interpretation deviates from that plain meaning.

U.S. Patent Number 6,363,031

“sleep signal” (cl. 1)	Signal that disables input buffers and other current sinking elements
“a Jedec-standard ‘ZZ’ signal” (cl. 3, 11, 15)	A control input received on an input pin configured according to a Jedec standard to place a Jedec-compliant device in a sleep mode.
“chip select signals” (cl. 11)	A chip enable signal presented to an input of a circuit
“automatically generating a Jedec-standard ‘ZZ’ signal” (cl. 3, 11, 15)	Generating a Jedec-standard ‘ZZ’ signal after a predetermined length of time

U.S. Patent Number 6,651,134

“non-interruptible” (cl. 1, 17)	once initiated, cannot be stopped or terminated until the fixed number of internal addresses has been generated
“predetermined number of said internal address signals” (cl. 1, 2, 3, 4, 17, 18)	number of said internal address signals determined prior to receipt of the external address signal, clock signal, and one or more control signals
“fixed burst length” (cl. 2, 5)	burst of a length determined prior to receipt of the external address signal, clock signal, and one or more control signals
“means for reading data from and writing data to a plurality of storage elements in response to a plurality of internal address signals” (cl. 16)	Function: reading data from and writing data to a plurality of storage elements in response to a plurality of internal address signals Structure: the memory array 104 depicted in Figure 1 described as “a static random access memory (SRAM) or a dynamic random access memory (DRAM), or other appropriate memory to meet

	the design criteria of a particular implementation" or their equivalent
"means for generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible" (cl. 16)	Function: generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal, and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible. Structure: the "circuit 102" depicted in Figure 2 and described at 3:62-4:14, the "circuit 102'" depicted in Figure 3 and described at 4:16-40, or their equivalents.

U.S. Patent Number 6,680,516

"semiconductor substrate" (cl. 5)	supporting semiconductor material upon which or within which elements of the semiconductor structure are formed
"metallic layer" (cl. 5)	conductive layer comprised of metal, metal alloy, or metal compound.
"etch stop layer" (cl. 5)	a first layer used to significantly slow further progress of an etch of a second layer when the etch reaches the first layer
"via, through the insulating layer, on the substrate" (cl. 5)	hole, through the insulating layer and exposing the substrate

U.S. Patent Number 6,825,526

"tunnel oxide layer" (cl. 1, 8, 15)	oxide layer with a very high probability of electron direct tunneling across it
"channel region" (cl. 1, 8, 15)	high conductivity region connecting source and drain

"said effective channel width corresponds to a height of said trench sidewalls" (cl. 1, 8, 15)	Effective channel width increases with an increase in height of a trench sidewall
"drive current" (cl. 3, 10, 17)	Current that flows between drain and source regions in a flash memory array

Dated: March 1, 2021 */s/ Peter J. Wied*

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