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United States Patent [19]

Takasugi et al.

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[54] MEMORY DEVICE PROVIDING BURST READ ACCESS AND WRITE ACCESS FROM A SINGLE ADDRESS INPUT

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Jul. 22, 1997	[JP]	Japan	9-18533 9-21247 10-13717
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[51] Int. Cl.⁶ G11C 8/00

365/233, 236

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Primary Examiner—Trong Phan Attorney, Agent, or Firm-Jones Volentine, LLP

ABSTRACT [57]

According to a first aspect of the invention, a memory device has a main memory array and a sub memory array. In a single burst, data are read from a series of columns in the main memory array, transferred from one column in the main memory array to one column in the sub memory array, read from a series of columns in the sub memory array, and written into the above-mentioned one column in the main memory array. According to a second aspect of the invention, a memory device has a memory array and separate external data input terminals and output terminals. In a single burst, data are read from a series of columns in the memory array, and written to one of the columns, preferably the last column in the series. Input of the written data is preferably simultaneous with the output of the data read from the column to which the input data are written.

82 Claims, 90 Drawing Sheets

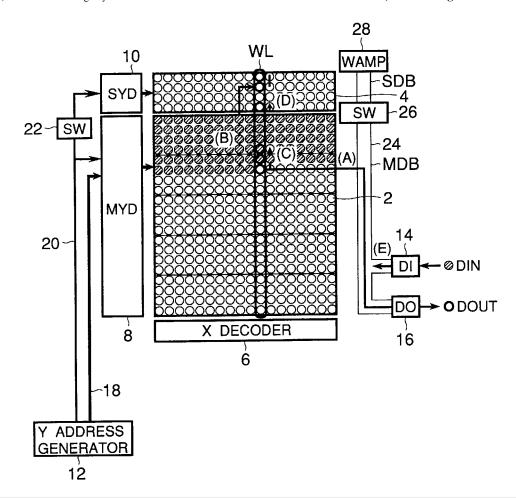




FIG.1

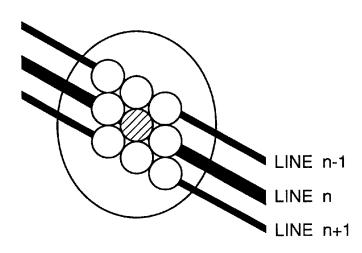


FIG.3

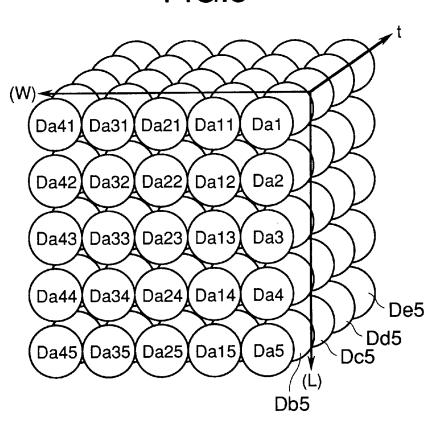
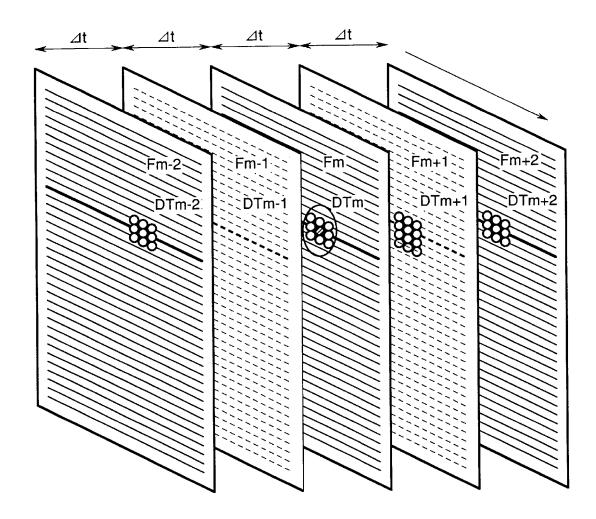


FIG.2





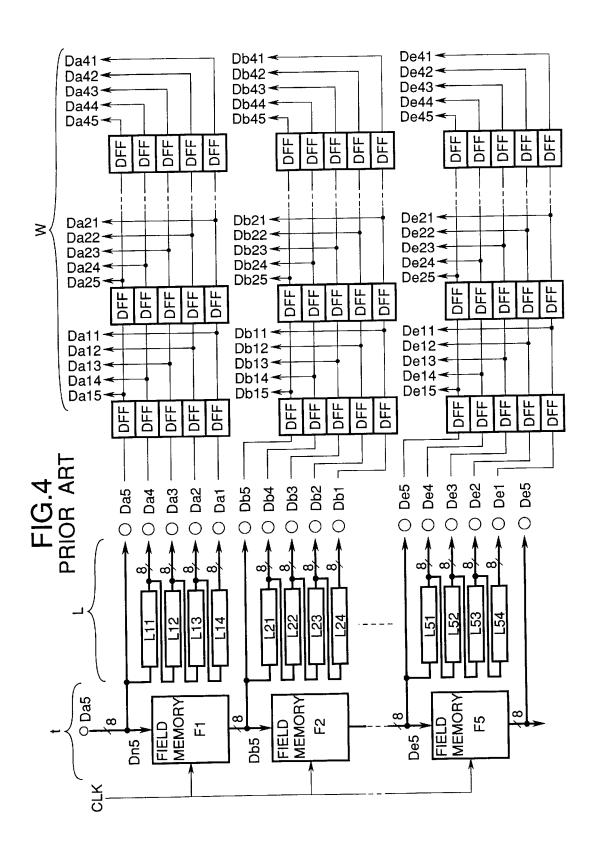




FIG.5

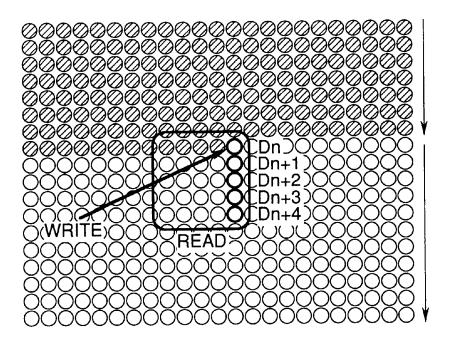
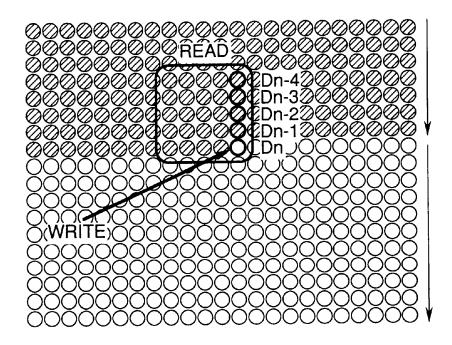


FIG.6





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