

ERIK CHMELAR, PhD, PE, MBA, JD, PMP, PMI-ACP

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I am a technology expert with over 20 years of industry experience in semiconductor electronics, including digital circuitry, programmable devices, microcontrollers, and telecommunications.

CREREDENTIALS

EDUCATION —

- **PhD, Electrical Engineering**, Stanford University, Stanford, CA
Dissertation: “Test and Diagnosis of Field-programmable Gate Arrays,” advised by E. J. McCluskey.
- **MS, Electrical Engineering**, Stanford University, Stanford, CA
- **BS, Electrical Engineering**, Michigan Technological University, Houghton, MI
- **BS, Chemical Physics**, Saginaw Valley State University, University Center, MI
- **MBA, Management**, Western Michigan University, Kalamazoo, MI
- **JD, Intellectual Property**, University of Michigan Law School, Ann Arbor, MI

LICENSES AND CERTIFICATIONS —

- **Licensed Professional Engineer (PE)**, State of Michigan
- **Certified Project Management Professional (PMP)**
- **Agile Certified Practitioner (PMI-ACP)**
- **Licensed Patent Attorney** (State Bar of Michigan, USPTO)

EXPERIENCE

Independent Consultant, Midland, MI (part time) Aug. 2007 – present

- Provide expert IP services to practicing companies and non-practicing entities (NPEs).
- Draft and prosecute patent applications, mine patent portfolios, and create infringement/use charts.
- Recent technology areas include programmable hardware, microcontrollers, and smart-card systems.

Murphy, Bilak & Homiller, PLLC., Cary, NC Jan. 2020 – Jun. 2020

Senior Associate, Patent Prosecution

- Prosecuted patent applications for industry-leading wireless and semiconductor corporations.
- Drafted approx. 100 office-action responses for complex 5G technologies.
- Analyzed ETSI 3GPP specifications for prosecution of standard essential patents (SEPs).

InterDigital Communications, Inc., Wilmington, DE Sep. 2015 – Oct. 2018

Sr. Manager, Innovation Partners

- Created patent portfolios for 5G, IoT, connected/autonomous vehicles, and augmented/virtual reality.
- Managed scientists and engineers to create over 100 new invention disclosures / patent applications.
- Forged research partnerships with commercial and academic organizations to develop patent portfolios.

Dera Industries LLC., Midland, MI May 2016 – Jul. 2017

Co-founder, Managing Member

- Developed and productized the award-winning One-Tie™ re-usable tie strap.
- Achieved \$1 million in annual sales prior to licensing the intellectual property.

Stryker Corp., Kalamazoo, MI Feb. 2012 – Mar. 2015

Sr. Principal Engineer, Advanced Development

- Supervised R&D of disruptive medical instruments and surgical technologies.
- Formalized new business opportunities, developed budgets and timelines, and staffed project teams.
- Collaborated with several top-tier universities to bring necessary expertise into the organization.
- Delivered working prototypes for biophotonic devices and boundary-constraint surgical robotics.

LSI Corp. (Broadcom), Milpitas, CA Jul. 2004 – Jan. 2012

Staff Software Engineer, Advanced Technology Development

- Conducted R&D for very large scale integrated (VLSI) and serializer-deserializer (SerDes) circuits.
- Granted approx. 20 patents for physical (PHY) interfaces, SerDes, and VLSI test architectures.
- Made cutting-edge contributions in SerDes and test that were implemented in customer designs.

Saginaw Valley State University, University Center, MI (part time)

Jan. 2009 – Jan. 2012

Adjunct Professor, Electrical and Computer Engineering

- Taught courses in digital circuits, computer architecture and organization, and data communications.

Stanford University, Stanford, CA (part time)

Sep. 2006 – Aug. 2008

Consulting Assistant Professor, Electrical Engineering

- Advised PhD students on the test and reliability of VLSI circuits.
- Taught a PhD-level course on clock and data recovery (CDR) for high-speed serial communications.

Xilinx, Inc., Los Gatos, CA (PhD. Intern, two summers)

Jun. 2002 – Sep. 2003

Product Test Engineer

- Engineered tools to detect and diagnose defects in FPGAs, which reduced diagnosis time by 75%.

Cisco Systems, Inc., San Jose, CA

Nov. 1999 – Apr. 2002

Manufacturing Engineer

- Oversaw functional testing of layer-2/3 network switches and determined root-cause failures.

SERVICE AND MENTORING

University of Michigan Law School, Ann Arbor, MI

2018

Admissions Representative

- Advised prospective law students at 30 law fairs and forums.

National Science Foundation, Western Michigan University I-Corps, Kalamazoo, MI

2015

Instructor

- Taught Lean Startup and Business Canvas fundamentals to a cohort of 30 entrepreneurs.

Accreditation Board of Engineering and Technology (ABET), Baltimore, MD

2013 – 2014

Engineering Program Evaluator

- Evaluated electrical computer engineering educational programs.

National Science Foundation, University of Michigan I-Corps, Ann Arbor, MI

2013

Industry Mentor

- Mentored teams of medical-device entrepreneurs participating in the I-Corps program.

Western Michigan University, Starting Gate Accelerator, Kalamazoo, MI

2013

Industry Mentor

- Mentored entrepreneurs participating in the university startup-accelerator program.

PROFICIENCIES

- Hardware – Verilog, VHDL, ASICs, FPGAs
- Engineering – COMSOL, ANSYS
- Legal research – Lexis, Westlaw, Innography
- Creativity – Illustrator, Photoshop, Premiere
- Software – C/C++, Objective-C, Java, MatLab
- CAD – SolidWorks, AutoCAD, Blender
- Legal Productivity – Foundation IP, Anaqua, Clio
- Foreign languages – German, Czech

List Publications by Erik Chmelar

- E. Chmelar, "Error signature analysis (ESA) receiver architecture for data communication," DesignCon, 2012.
- E. Chmelar and C. Ito, "Mostly digital SerDes (MDS): a comprehensive low power receiver architecture," DesignCon, 2012.
- I. Park, D. Lee, E. Chmelar, and E. McCluskey, "Inconsistent fails due to limited tester timing accuracy," Proc. 26th VLSI Test Symp., 2008.
- A. Al-Yamani, N. Devta-Prasanna, E. Chmelar, M. Grinchuk, and A. Gunda, "Scan test cost and power reduction through systematic scan reconfiguration," IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems, vol. 26, pp. 907–918, 2007.
- A. Al-Yamani, E. Chmelar, and M. Grinchuk, "Segmented addressable scan architecture," Proc. 23rd VLSI Test Symp., 2005.
- E. Chmelar, "Minimizing the number of test configurations for FPGAs," Int. Conf. Computer Aided Design, 2004.
- E. Chmelar, "The test and diagnosis of FPGAs," Ph.D. thesis, Stanford University, 2004.
- E. Chmelar and S. Toutounchi, "FPGA bridging fault detection and location via differential IDDQ," Proc. 22nd VLSI Test Symp., 2004.
- E. Chmelar, "Subframe multiplexing: FPGA manufacturing test time reduction," CRC TR-04-01, 2004.
- E. Chmelar, "Subframe multiplexing for FPGA manufacturing test," Proc. Int. Symp. FPGAs, 2004.
- E. Chmelar, "FPGA interconnect delay fault testing," Proc. Int. Test Conf., pp. 1239–1247, 2003.

List of US Patents by Erik Chmelar

- US6920621B1, "Methods of testing for shorts in programmable logic devices using relative quiescent current measurements," issued 2005-07-19.
- US6979142B1, "Retractable tip mechanical pencil assembly," issued 2005-12-27.
- US7093842B2, "Skateboard truck assembly," issued 2006-08-22.
- US7206983B2, "Segmented addressable scan architecture and method for implementing scan-based testing of integrated circuits," issued 2007-04-17.
- US7210083B2, "System and method for implementing postponed quasi-masking test output compression in integrated circuit," issued 2007-04-24.
- US7293312B2, "Multipurpose skateboard tool," issued 2007-11-13.
- US7328386B2, "Methods for using checksums in X-tolerant test response compaction in scan-based testing of integrated circuits," issued 2008-02-05.
- US7656339B2, "Systems and methods for analog to digital conversion," issued 2010-02-02.
- US7656340B2, "Systems and methods for pipelined analog to digital conversion," issued 2010-02-02.
- US7696915B2, "Analog-to-digital converter having reduced number of activated comparators," issued 2010-04-13.
- US7779320B2, "Low power scan shifting with random-like test patterns," issued 2010-08-17.
- US7973692B2, "Systems and methods for synchronous, retimed analog to digital conversion," issued 2011-06-07.
- US7956790B2, "Systems and methods for synchronous, retimed analog to digital conversion," issued 2011-07-05.
- US8121186B2, "Systems and methods for speculative signal equalization," issued 2012-02-21.
- US8432250B2, "Process variation based microchip identification," issued 2013-04-30.
- US8527912B2, "Digitally obtaining contours of fabricated polygons," issued 2013-09-03.
- US8615062B2, "Adaptation using error signature analysis in a communication system," issued 2013-12-24.
- US8923382B2, "Tap adaptation with a fully unrolled decision feedback equalizer," issued 2014-12-30.
- US8929497B2, "Dynamic deskew for bang-bang timing recovery in a communication system," issued 2015-01-06.

US8982941B2, "Predictive selection in a fully unrolled decision feedback equalizer," issued 2015-03-17.

US9014313B2, "Error signature analysis for data and clock recovery in a communication system," issued 2015-04-21.

US9087157B2, "Low-loss transmission line TDM communication link and system," issued 2015-07-21.

US9292644B2, "Row based analog standard cell layout design and methodology," issued 2016-03-22.

US10258706B2, "Sterilization container capable of providing an indication regarding whether or not surgical instruments sterilized in the container were properly sterilized," issued 2019-04-16.

US10604317B2, "Reusable tie strap with multiple apertures," issued 2020-03-31.

US10731698B2, "Hook device with rotatable opposing jaws," issued 2020-08-04.