IW 8035384

# THE UNITED STATES OF AMERICA

## TO ALL TO WHOM THESE PRESENTS SHALL COME:

### UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office

March 11, 2020

THIS IS TO CERTIFY THAT ANNEXED IS A TRUE COPY FROM THE RECORDS OF THIS OFFICE OF THE FILE WRAPPER AND CONTENTS OF:

**APPLICATION NUMBER:** *09/504,344*
**FILING DATE:** *February 14, 2000*
**PATENT NUMBER:** *6,651,134*
**ISSUE DATE:** *November 18, 2003*

By Authority of the

Under Secretary of Commerce for Intellectual Property
and Director of the United States Patent and Trademark Office

W. MONTGOMERY
Certifying Officer

0325.00309
CD99073

# FIXED BURST MEMORIES

## Field of the Invention

The present invention relates to memory devices generally and, more particularly, to a memory device that transfers a fixed number of words of data with each access.

## Background of the Invention

A synchronous Static Random Access Memory (SRAM) can provide data from multiple address locations using a single address. Accessing multiple locations in response to a single address is called a burst mode access. A memory device that provides a burst mode can reduce activity on the address and control buses. The burst mode of a conventional synchronous SRAM can be started and stopped in response to a control signal.

A conventional Dynamic Random Access Memory (DRAM) preserves data during periodic absences of power by implementing a memory cell as a capacitor and an access transistor. Since the charge on the capacitor will slowly leak away, the cells need to be "refreshed" once every few milliseconds. Depending on the frequency of accesses, a conventional DRAM can need an interrupt to

1

perform data refreshes. Using a DRAM in a burst application is difficult because of the need to refresh. Completely hiding refresh cycles (e.g., refreshing data without the need for interrupts) in a DRAM cannot happen with conventional memory

5    devices due to architecture choices that have been made. Data word bursts can be interrupted while in progress since conventional architectures support both burst and single access modes. Conventional DRAM access takes about 10ns to get data, but nearly 20ns to complete writeback and equalization. The addition of

10   another 20ns for a refresh results in a total access of 40ns.

Since the data burst transfers of conventional memories can be interrupted and single accesses made, the amount of time that the data, address and control busses are not in use can vary. The variability of bus availability complicates the design of

15   systems with shared data, address and control busses.

It would be desirable to have a memory device that has a fixed burst length.

## Summary of the Invention

20   The present invention concerns an integrated circuit comprising a memory and a logic circuit. The memory may comprise

2

a plurality of storage elements each configured to read and write data in response to an internal address signal. The logic circuit may be configured to generate a predetermined number of the internal address signals in response to (i) an external address

5 signal, (ii) a clock signal and (iii) one or more control signals. The generation of the predetermined number of internal address signals may be non-interruptible.

The objects, features and advantages of the present invention include providing a fixed burst memory that may (i) give

10 network customers who typically burst large data lengths the ability to set a fixed burst length that suits particular needs; (ii) have non-interruptible bursts; (iii) free up the address bus and control bus for a number of cycles; (iv) provide programmability for setting the burst length by using DC levels

15 [Vss or Vcc] on external pins; (v) hide required DRAM refreshes inside a known fixed burst length of data words; and/or (vi) operate at higher frequencies without needing interrupts to perform refreshes of data.

## Brief Description of the Drawings

These and other objects, features and advantages of the present invention will be apparent from the following detailed description and the appended claims and drawings in which:

5      FIG. 1 is a block diagram illustrating a preferred embodiment of the present invention;

FIG. 2 is a detailed block diagram illustrating a circuit 102 of FIG. 1;

FIG. 3 is a detailed block diagram of a circuit 102' illustrating an alternative embodiment of the circuit 102 of FIG. 1;

FIG. 4 is a flow diagram illustrating an example burst address sequence;

FIGS. 5A and 5B are diagrams illustrating example operations of a 4 word (FIG. 5A) and an 8 word (FIG. 5B) fixed burst access in accordance with the present invention; and

FIG. 6 is a diagram illustrating an example operation where a burst length may be long enough to include a writeback and a refresh cycle.

4

## Detailed Description of the Preferred Embodiments

Referring to FIG. 1, a block diagram of a circuit 100 is shown in accordance with a preferred embodiment of the present invention. The circuit 100 may be implemented, in one example, as a fixed burst memory. The circuit 100 may be configured to transfer a fixed number of words of data with each access (e.g., read or write). A number of words transferred as a group is called a burst. The circuit 100 generally comprises a circuit 102 and a memory array (or circuit) 104. The circuit 102 may be implemented, in one example, as a burst address counter/register. The memory array 104 may be implemented, in one example, as a static random access memory (SRAM), a dynamic random access memory (DRAM), or other appropriate memory to meet the design criteria of a particular implementation.

The circuit 102 may have an input 106 that may receive a signal (e.g., ADDR_EXT), an input 108 that may receive a signal (e.g., LOAD), an input 110 that may receive a signal (e.g., CLK), an input 112 that may receive a signal (e.g., ADV), and an input 114 that may receive a signal (e.g., BURST). The circuit 102 may have an output 116 that may present a signal (e.g., ADDR_INT) to an input 118 of the memory 104. The memory 104 may have an input 120

that may receive a signal (e.g., R/Wb), an input 122 that may receive a signal (e.g., DATA_IN) and an output 122 that may present a signal (e.g., DATA_OUT). The various signals are generally "on" (e.g., a digital HIGH, or 1) or "off" (e.g., a digital LOW, or 0).

5   However, the particular polarities of the on (e.g., asserted) and off (e.g., de-asserted) states of the signals may be adjusted (e.g., reversed) accordingly to meet the design criteria of a particular implementation.

The signal ADDR_EXT may be, in one example, an external address signal. The signal ADDR_EXT may be n-bits wide, where n is
10  an integer. The signal CLK may be a clock signal. The signal R/Wb may be a control signal that may be in a first state or a second state. When the signal R/Wb is in the first state, the circuit 100 will generally read data from the memory circuit 104 for
15  presentation as the signal DATA_OUT. When the signal R/Wb is in the second state, the circuit 100 will generally store data received as the signal DATA_IN.

The signal LOAD may be, in one example, an address load control signal. The circuit 100 may be configured to load an
20  initial address, presented by the signal ADDR_EXT, in response to the signal LOAD. The initial address may determine the initial

6

location where data transfers to and from the memory 104 will generally begin.

The signal ADV may be, in one example, used as a control signal. The circuit 100 may be configured to transfer a fixed number of words to or from the memory 104 in response to the signals ADV, CLK and R/Wb. When the signal ADV is asserted, the circuit 100 will generally begin transferring a predetermined number of words. The transfer is generally non-interruptible. In one example, the signal ADV may initiate the generation of a number of addresses for presentation as the signal ADDR_INT.

The signals ADV and LOAD may be, in one example, a single signal (e.g., ADV/LDb). The signal ADV/LDb may be a control signal that may be in a first state or a second state. When the signal ADV/LDb is in the first state, the circuit 102 will generally load an address presented by the signal ADDR_EXT as an initial address. When the signal ADV/LDb is in the second state, the circuit 102 may be configured to generate the signal ADDR_INT as a fixed number of addresses in response to the signal CLK. The signal ADDR_INT may be, in one example, an internal address signal. The signal ADDR_INT may be n-bits wide. Once the circuit 102 has started generating the fixed number of addresses, the circuit 102 will

7

generally not stop until the fixed number of addresses has been generated (e.g., a non-interruptible burst).

The signal BURST may be, in one example, a configuration signal for programming the fixed number of addresses that the circuit 102 may generate in response to the signals CLK and ADV/LDb. The signal BURST may be generated, in one example, by (i) using bond options, (ii) voltage levels applied to external pins, or (iii) other appropriate signal generation means.

When the memory 104 is implemented as a DRAM, the circuit 100 may be configured to hide required DRAM refreshes (e.g., refreshes may occur without affecting external environment) inside a known fixed burst length of data words. The fixed burst length may allow the circuit 100 to operate at higher frequencies than a conventional DRAM without needing interrupts to perform refreshes of data. In one example, the fixed burst length may be four or eight words. However, the burst length may be set to whatever length is necessary to meet the design criteria of a particular application. For example, the burst length may be programmed, in one example, to allow both writeback and refresh to occur within a single access. The fixed burst length may be set, in one example,

8

longer or shorter depending upon a frequency or technology to be used.

The circuit 100 may be configured to provide a fixed burst length that may suit the requirements of network customers who typically burst large data lengths. By providing a fixed burst length, the circuit 100 may allow shared usage of data, address and control busses. A fixed length non-interruptible burst generally frees up the address bus and control bus for a known number of cycles. The address and control busses may be shared by a number of memory devices. The circuit 100 may provide a more reliable and /or accurate burst than is possible with multiple chips.

Referring to FIG. 2, a detailed block diagram illustrating implementation of the circuit 102 is shown. The circuit 102 may comprise an address counter register 126 and a burst counter 128. The address counter register 126 generally receives the signals ADDR_EXT, LOAD, and CLK. The address counter register 126 may be configured to present the signal ADDR_INT. The signal ADV and the signal BURST may be presented to a burst counter 128. The signal CLK may be presented at an input 130 of the burst counter 128. The burst counter 128 may have an output 132 that may present a signal (e.g., BURST_CLK) at an input 134 of the circuit

9

126. An initial address may be loaded into the address counter

register 126 by presenting the initial address in the signal

ADDR_EXT and asserting the signal LOAD. The circuit 126 may be

configured to increment an address in response to the signal

5    BURST_CLK. When the signal ADV is asserted, the burst counter 128

will generally present the signal BURST_CLK in response to the

signal CLK. The signal BURST_CLK generally contains a number of

pulses that has been programmed by the signal BURST.

Referring to FIG. 3, a detailed block diagram

10   illustrating an alternative embodiment of the circuit 102 is shown.

The circuit 102' may comprise a latch 134, a multiplexer 136 and a

counter 138. The signals ADDR_EXT, LOAD and CLK may be presented

to the latch 134. The latch 134 may have an output 140 that may

present a portion (e.g., m bits, where m is an integer smaller than

15   n) of the signal ADDR_EXT as a portion of the signal ADDR_INT, an

output 142 that may present a second portion (e.g., k bits, where

k is an integer smaller than n) of the signal ADDR_EXT to a first

input of the multiplexer 136, and an output 144 that may present

the second portion of the signal ADDR_EXT to an input 146 of the

20   counter 138.

10

The signals ADV, CLK and BURST may be presented to inputs of the counter 138. The counter 138 may be configured to generate a number of addresses in response to the signals CLK, BURST and ADV. The number of addresses generated by the counter 138 may be programmed by the signal BURST.

The signal BURST may be presented to a control input of the multiplexer 136. The multiplexer 136 may select between a number of signals from the latch 134 and a number of signals from the counter 138 to be presented as a second portion of the signal ADDR_INT in response to the signal BURST.

Referring to FIG. 4, a flow diagram illustrating an example burst address sequence is shown. When the signal ADV is asserted, the circuit 100 will generally generate a number of address signals, for example, N where N is an integer. The address signals may be generated, in one example, on a rising edge of the signal CLK. The address signals will generally continue to be generated until the Nth address signal is generated.

Referring to FIGS. 5A and 5B, timing diagrams illustrating example operations for a four word (FIG. 5A) and an eight word (FIG. 5B) fixed burst memory in accordance with the present invention are shown. The timing diagrams generally

11

Subclass
Class
ISSUE CLASSIFICATION

104

711

**PATENT NUMBER**

**6651134**

6651134

## U.S. UTILITY Patent Application

O.I.P.E.

SCANNED AA Q.A. No

**PATENT DATE**

NOV 18 2003

| APPLICATION NO. | CONT/PRIOR | CLASS | SUBCLASS | ART UNIT | EXAMINER |
|---|---|---|---|---|---|
| 09/504344 | | 365 711 | 104 | 282 | Chow |

RSD 2188

APPLICANTS

Cathal Phelan

TITLE

Fixed burst memories

PTO-2040
12/99

## ISSUING CLASSIFICATION

| ORIGINAL | | CROSS REFERENCE(S) | | | | | |
|---|---|---|---|---|---|---|---|
| CLASS | SUBCLASS | CLASS | SUBCLASS (ONE SUBCLASS PER BLOCK) | | | | |
| 711 | 104 | 711 | 105 | 167 | 169 | | |
| INTERNATIONAL CLASSIFICATION | | 710 | 35 | | | | |
| G 0 6 F 12/00 | | 365 | 233 | 238.5 | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |

☐ Continued on Issue Slip Inside File Jacket

| TERMINAL DISCLAIMER | DRAWINGS | | | CLAIMS ALLOWED | |
|---|---|---|---|---|---|
| ☐ | Sheets Drwg. | Figs. Drwg. | Print Fig. | Total Claims | Print Claim for O.G. |
| | 53 | 7 | 5A 5B | 21 | 1 |

☐ The term of this patent subsequent to _____ (date) has been disclaimed.

Medhi Namazi 6-12-03
(Assistant Examiner) (Date)

Donald Sparks
Supervisory Patent Examiner
Technology Center 2100 6-13-03
(Primary Examiner) (Date)

☐ The term of this patent shall not extend beyond the expiration date of U.S. Patent No. _____

**NOTICE OF ALLOWANCE MAILED**

6/16/03

**ISSUE FEE**

| Amount Due | Date Paid |
|---|---|
| $1300.00 | 9-17-03 |

☐ The terminal _____ months of this patent have been disclaimed.

(Legal Instruments Examiner) 6/24/03
(Date)

**ISSUE BATCH NUMBER**

**WARNING:**
The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368. Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.

Form PTO-436A
(Rev. 6/99)

## ISSUE FEE IN FILE

FILED WITH: ☐ DISK (CRF) ☐ FICHE ☐ CD-ROM
(Attached in pocket on right inside flap)

(FACE)

**Bib Data Sheet**

**UNITED STATES DEPARTMENT OF COMMERCE**
**Patent and Trademark Office**
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

| SERIAL NUMBER 09/504,344 | FILING DATE 02/14/2000 RULE – | CLASS 365 711 | GROUP ART UNIT 2824 2187 | ATTORNEY DOCKET NO. 0325.000309 |
|---|---|---|---|---|

**APPLICANTS**

    Cathal G. Phelan, Mountain View, CA ;

** CONTINUING DATA ************************ *none* *m.w*

** FOREIGN APPLICATIONS ******************* *m.w*

**IF REQUIRED, FOREIGN FILING LICENSE GRANTED** **
** 05/02/2000

| Foreign Priority claimed ☐ yes ☑ no | STATE OR COUNTRY CA | SHEETS DRAWING 5 | TOTAL CLAIMS 17 | INDEPENDENT CLAIMS 3 |
|---|---|---|---|---|
| 35 USC 119 (a-d) conditions met ☐ yes ☑ no ☐ Met after Allowance | | | | |
| Verified and Acknowledged _____ Examiner's Signature _____ Initials | | | | |

**ADDRESS**

021363

**TITLE** *Memory Device with Fixed Length Non Interruptible Burst*
~~Fixed burst memories~~

| FILING FEE RECEIVED 690 | FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following: | ☐ All Fees |
|---|---|---|
| | | ☐ 1.16 Fees ( Filing ) |
| | | ☐ 1.17 Fees ( Processing Ext. of time ) |
| | | ☐ 1.18 Fees ( Issue ) |
| | | ☐ Other _____ |
| | | ☐ Credit |

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

02/24/2000 SCARMICH 00000016 09504344

01 FC:101                    690.00 OP

PTO-1556
(5/87)

*U.S. GPO: 1999-459-082/19144

02-15-00

# CHRISTOPHER P. MAIORANA, P.C.

24025 Greater Mack, Suite 200
St. Clair Shores, Michigan 48080

Utility Patent Application Transmittal
(Only for new non-provisional applications Under 37 CFR 1.53(b))

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D. C. 20231

Case Docket No.0325.00030

Date: February 14, 2000

Sir:

Transmitted herewith for filing is a patent application of:

Inventor(s):    Cathal G. Phelan

For:            FIXED BURST MEMORIES

Enclosed are:

1.   X        Specification (13 pages); Claims (4 pages); Abstract (1 page)

2.   X        _5_ sheets of formal drawings.

3.   X        Oath or Declaration          Total Pages _2_
              a. _X_  Newly executed (original or copy)
              b. ___  Copy from a prior application (37 CFR 1.63(d))
                      (for continuation/divisional with Item 5 completed)
              c. ___  Copy of Revocation of Previous Power

4.   ___      Incorporation By Reference (usable if Item 3b is checked)
              The entire disclosure of the prior application, from which a copy of the oath or
              declaration is supplied under Item 3b, is considered as being part of the disclosure
              of the accompanying application and is hereby incorporated by reference therein.

5.   ___      If a Continuing Application, check appropriate box and supply the requisite
              information below and in a preliminary amendment:

              ___ Continuation    _____ Divisional    _____ Continuation-in-part (CIP)
              of prior application no.: _____

6.   X        An assignment to CYPRESS SEMICONDUCTOR CORP. along with PTO form
              1595.

7.   ___      A PTO Form 1449 with a copy of the references not previously cited.

8.   X        Return Receipt Postcard

9.   ___      Other:

The filing fee has been calculated as shown below:

|  | No. Filed | No. Extra | Fee | Amount |
|---|---|---|---|---|
| Basic Fee | -- | -- | -- | $690.00 |
| Total Claims | 17 | 0 | x  $ 18.00 | $ 0.00 |
| Indep. Claims | 3 | 0 | x  $ 78.00 | $ 0.00 |
| Mult. Dep. Claims |  |  | $260.00 | $ 0.00 |

SUB-TOTAL . . . . . . . . . . . . . . . . . $690.00

__  SMALL ENTITY STATUS (divide SUB-TOTAL by two) . . . . . . $\_\_\_\_

X   Assignment Recordal Fee ($40.00) . . . . . . . . . . . . . . . . . . . . . . . $ 40.00

TOTAL . . . . . . . . . . . . . . . . . . . . . $730.00

X    A check in the amount of $730.00 to cover the filing fee is enclosed.

X    The Commissioner is hereby authorized to charge any fees under 37 CFR 1.16 and 1.17 which may be required by this paper or associated with this filing to Deposit Account No. 50-0541. A duplicate copy of this sheet is enclosed.

---

**Correspondence Address:**

---

Customer Number or Bar Code Label:

**021363**

PATENT TRADEMARK OFFICE

---

## CERTIFICATE OF EXPRESS MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service via Express Mail Label No. EL417953316US in an envelope addressed to: BOX PATENT APPLICATION, Assistant Commissioner for Patents, Washington, D.C. 20231, on February 14, 2000.

By: *Mary Donna Berkley*

Mary Donna Berkley

Respectfully submitted,

By

Christopher P. Maiorana
Reg. No. 42,829
CHRISTOPHER P. MAIORANA, P.C.
24025 Greater Mack, Suite 200
St. Clair Shores, Michigan 48080
(810) 498-0670

**Date:** February 14, 2000

**Attorney Docket No.: 0325.00309**

illustrate externally measurable signals for four and eight word fixed burst read/write architectures. In general, an operation (e.g., read or write) of the circuit 100 begins with loading an initial address (e.g., portions 150, 154, and 158 of FIG. 5A; portions 150', 154', and 158' of FIG. 5B). Starting with the initial address, a fixed number of words are generally transferred (e.g., line DQ of FIGS. 5A and 5B). During the transfer of the fixed number of words, the address and control buses (e.g., ADDR, CE, R/W, etc.) are generally available to other devices (e.g., portions 152, 156, and 160 of FIG. 5A; portions 152', 156', and 160' of FIG. 5B). In one example, the control and address bus activity may be one-fourth (FIG. 5A) or one-eighth (FIG. 5B) the data bus activity (e.g., compare line ADDR with line DQ of FIGS. 5A and 5B). The reduced bus activity may be an effect of the architecture. The data bus may be, in one example, active nearly 100% of the time (e.g., line DQ of FIGS. 5A and 5B) In one example, there may be no inefficiencies switching from read to write to read etcetera (e.g., see labels under line DQ of FIGS. 5A and 5B).

Referring to FIG. 6, a timing diagram illustrating a fixed burst length long enough to hide a writeback and a refresh cycle is shown. Internally the action being performed may

12

completely hide DRAM refresh activity inside nominal external

activities. A portion 162 illustrates that refresh activity (e.g.,

writeback, read for refresh, and writeback for refresh) may be

completed within the time of the burst transfer. When a fixed

5    burst long enough to completely hide refresh activity is provided,

there may be no penalty for using DRAM instead of SRAM for the

memory 104.

While the invention has been particularly shown and

described with reference to the preferred embodiments thereof, it

10   will be understood by those skilled in the art that various changes

in form and details may be made without departing from the spirit

and scope of the invention.

13

## CLAIMS

1.    An integrated circuit comprising:

a memory comprising a plurality of storage elements each configured to read and write data in response to an internal address signal; and

a logic circuit configured to generate a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

2.    The integrated circuit according to claim 1, wherein said predetermine number of internal address signals is determined by a fixed burst length.

3.    The integrated circuit according to claim 1, wherein said predetermined number of internal address signals is 4.

4.    The integrated circuit according to claim 1, wherein said predetermined number of internal address signals is 8.

0325.00309
CD99073

5.    The integrated circuit according to claim 2, wherein said fixed burst length is programmable.

6.    The integrated circuit according to claim 5, wherein said fixed burst length is  programmed by bond options.

7.    The integrated circuit according to claim 5, wherein said fixed burst length is  programmed by voltage levels on external pins.

8.    The integrated circuit according to claim 1, wherein said memory comprises a static random access memory.

9.    The integrated circuit according to claim 1, wherein said memory comprises a dynamic random access memory.

10.    The integrated circuit according to claim 9, wherein said predetermined number of internal address signals is chosen to provide time for writeback and refresh cycles.

15

11.  The integrated circuit according to claim 1, wherein said predetermined number of internal address signals is chosen to meet predetermined criteria for sharing address and control busses.

12.  An integrated circuit comprising:

means for reading and writing data in response to an internal address signal; and

means for generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

13.  A method of providing a fixed burst length data transfer comprising the steps of:

reading from and writing data to a memory in response to an internal address signal; and

generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) a control signal, wherein said generation

5

16

of said predetermined number of internal address signals is non-interruptible.

14.   The method according to claim 13, further comprising the step of programming said predetermined number.

15.   The method according to claim 14, wherein said programming step is performed using bond options.

16.   The method according to claim 14, wherein said programming step is performed using voltage levels.

17.   The method according to claim 13, further comprising the step of selecting said predetermined number to provide time for writeback and refresh cycles.

17

0325.00309
CD99073

## ABSTRACT OF THE DISCLOSURE

An integrated circuit comprising a memory and a logic circuit. The memory may comprise a plurality of storage elements each configured to read and write data in response to an internal address signal. The logic circuit may be configured to generate a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals. The generation of the predetermined number of internal address signals may be non-interruptible.

5

18

Docket No. <u>0325.00309</u>

# DECLARATION, POWER OF ATTORNEY AND PETITION

I, the undersigned inventor, hereby declare that:

My residence, post office address and citizenship are given next to my name;

I believe that I am the first, original and sole inventor of the subject matter claimed in the application for patent entitled "**HIDDEN DRAM REFRESH IN FIXED BURST MEMORIES**", which:

    <u>X</u>   is submitted herewith;

    <u>     </u>   was filed on <u>      </u> as Application Serial No. <u>   </u> and amended on <u>    </u>;

I have reviewed and understand the contents of the above-identified application for patent (hereinafter, "this application"), including the claims;

I acknowledge the duty under Title 37, Code of Federal Regulations, Section 1.56, to disclose to the United States Patent and Trademark Office information known to be material to the patentability of this application. I also acknowledge that information is material to patentability when it is not cumulative to information already provided to the United States Patent and Trademark Office and when it either

    compels, by itself or in combination with other information, a conclusion that a claim is unpatentable under the preponderance of evidence standard, giving each term in the claim its broadest reasonable construction consistent with the application, and before any consideration is given to evidence which may be submitted to establish a contrary conclusion of patentability, or

    refutes or is inconsistent with a position taken in either (i) asserting an argument of patentability, or (ii) opposing an argument of unpatentability relied on by the United States Patent and Trademark Office;

I hereby claim the priority benefit under Title 35, Section 119(e), of the following United States provisional patent applications:

<u>Application No.</u>                                          <u>Filing Date</u>

I hereby claim the priority benefit under Title 35, Section 120, of the following United States patent applications:

<u>Serial No.</u>                  <u>Filing Date</u>                  <u>Status</u>

Docket No. 0325.00309                                                        Page 2 of 2

I hereby claim the priority benefit under Title 35, Section 365(c), of the following PCT International patent applications designating the United States:

Application No.                                                   Filing Date

Where the subject matter of the claims of this application is not disclosed in the United States or PCT priority patent applications identified above, I acknowledge the duty to disclose information known to be material to the patentability of this application that became available between the filing dates of this application and of the priority United States or PCT patent applications.

I hereby appoint as my attorneys with full power of substitution to prosecute this application and conduct all business in the United States Patent and Trademark Office associated with this application: Customer No. 021363.

||||||| |||| ||||| ||||| |||| ||||| ||||

## 021363

PATENT TRADEMARK OFFICE

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.

Cathal G. Phelan                                 Post Office Address:_____
Inventor                                           __394 Mountain View Ave._____
                                                    Mountain View, CA 94041_____

Signature of Inventor                           Citizen of:__Ireland_____
                                                Residence:__394 Mountain View Ave._
2/11/00                                                     Mountain View, CA 94041
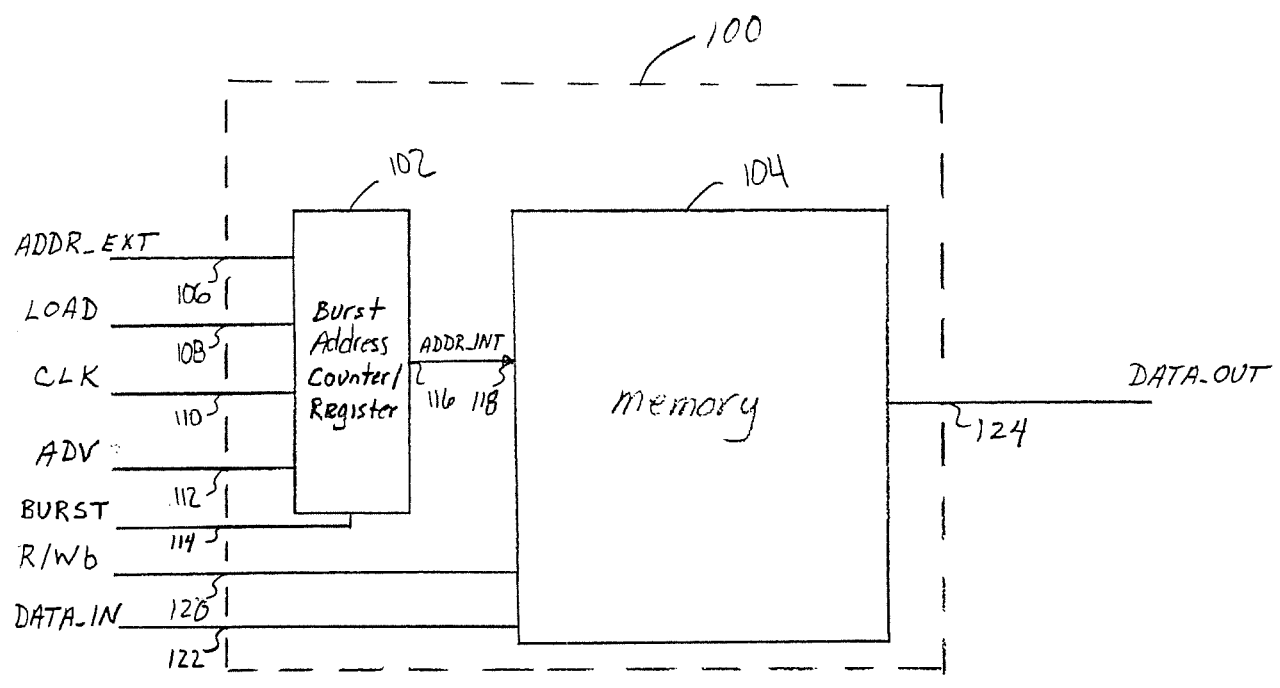
Date

FIG. 1

Applicant:             Cathal G. Phelan
Serial No.:
Filing Date:           Herewith
For:                   FIXED BURST MEMORIES
Attorney:              CPM
Attorney Docket No:    0325.00309

Sheet 1 of 5

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. |
|---|---|---|---|
| 09/504,344 | 02/14/00 | PHELAN | C    0325.000309 |

| EXAMINER |
|---|
| NAMAZI,M |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2187 | 3 |

021363                              TM02/1002
CHRISTOPHER P. MAIORANA, P.C.
24025 GREATER MACK
SUITE 200
ST. CLAIR SHORES MI 48080

DATE MAILED:
10/02/01

**Please find below and/or attached an Office communication concerning this application or proceeding.**

Commissioner of Patents and Trademarks

1- File Copy

| | Application No. | Applicant(s) | |
|---|---|---|---|
| **Office Action Summary** | 09/504,344 | Phelan | |
| | Examiner | Art Unit | |
| | Mehdi Namazi | 2187 | |

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _three_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1) ☒ Responsive to communication(s) filed on _Feb 14, 2000_

2a) ☐ This action is FINAL.        2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

## Disposition of Claims

4) ☒ Claim(s) _1-17_ is/are pending in the applica

4a) Of the above, claim(s) _____ is/are withdrawn from considera

5) ☐ Claim(s) _____ is/are allowed.

6) ☐ Claim(s) _____ is/are rejected.

7) ☒ Claim(s) _1-17_ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

## Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____ .

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

## Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). ___2___

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other: _____

## DETAILED ACTION

1.    Claims 1-17 are presented for examination.  This office

action is in response to the application filed 02/14/2000.

### In the Title

2.    The title of the invention is not descriptive.  A new title

is required that is clearly indicative of the invention to which

the claims are directed.  It appears --A memory device that

transfers a fixed number of words of data with non-interruptible

burst-- or other similar language(see claim 1, specification,

pages 1 and 9, e.g.).  The loss in brevity of title is more than

offset by the gain in its informative value in indexing,

classifying, searching, etc.  See MPEP 606 and 606.01.

### Claim Rejections - 35 USC § 112

3.    The following is a quotation of the first paragraph of 35

U.S.C. 112:

> The specification shall contain a written description of the
> invention, and of the manner and process of making and using
> it, in such full, clear, concise, and exact terms as to enable
> any person skilled in the art to which it pertains, or with
> which it is most nearly connected, to make and use the same
> and shall set forth the best mode contemplated by the inventor
> of carrying out his invention.

4.    Claims 6 and 15 are rejected under 35 U.S.C. 112, first

paragraph, as containing subject matter which was not described

in the specification in such a way as to enable one skilled in

the art to which it pertains, or with which it is most nearly

connected, to make and/or use the invention.

As per claims 6 and 15, the specification does not provide

support for limitation such as *bond options*.


### Claim Rejections - 35 USC § 102

5.    The following is a quotation of the appropriate paragraphs

of 35 U.S.C. 102 that form the basis for the rejections under

this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for
> patent by another filed in the United States before the invention thereof
> by the applicant for patent, or on an international application by another
> who has fulfilled the requirements of paragraphs (1), (2), and (4) of
> section 371© of this title before the invention thereof by the applicant
> for patent.

6.    Claims 1-17 are rejected under 35 U.S.C. 102(e) as being

anticipated by Yip et al.(YIP)(U.S.Patent No. 6,289,138).

As per claims 1 and 12-13 Yip teaches an integrated circuit

comprising: a memory comprising a plurality of storage elements

each configured to read and write data in response to an internal

address signal(fig. 144B, element 230); and  a logic circuit

configured to generate a predetermined number of said internal

address signals in response to (I) an external address

signal(fig. 144A, "ext_addr"), (ii) a clock signal(inherent) and

(iii) one or more control signals(col. 2, lines 15-20), wherein said generation of said predetermined number of internal address signals is non-interruptible(col. 115, lines 60-64).

As per claims 2, Yip teaches wherein said predetermine number of internal address signals is determined by a fixed burst length(col. 115, lines 62-63).

As per claims 3-4 and 14, Yip teaches wherein said predetermined number of internal address signals are 4 or 8(col. 115, lines 62-63 teaches preset number of words, which means preset numbers of internal signals).

As per claim 5, Yip teaches wherein said fixed burst length is programmable(col. 109, lines 35-43).

As per claims 6 and 15, Yip teaches wherein said fixed burst length is programmed by bond options(col. 109, lines 35-43).

As per claims 7 and 16, Yip teaches wherein said fixed burst length is programmed by voltage levels on external pins(it is inherent to have voltage levels for each burst).

As per claim 8, Yip teaches wherein said memory comprises a static random access memory(fig. 1, element 230).

As per claim 9, Yip teaches wherein said memory comprises a dynamic random access memory(fig. 146, element 1910).

As per claims 10 and 17, Yip teaches wherein said predetermined number of internal address signals is chosen to provide time for writeback and refresh cycles(it is inherent to have time included for writeback and refresh cycle during each burst).

As per claim 11, Yip teaches wherein said predetermined number of internal address signals is chosen to meet predetermined criteria for sharing address and control busses(col. 115, lines 62-63).

## Conclusion

7.    The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 5,651,138(Le et al.) Teaches data processor with controlled burst memory accesses and method therefor.

U.S. Patent 5,805,928(Lee) Teaches burst length detection circuit for detecting a burst end time point and generating a burst mode signal without using a conventional burst length detection counter.

_U.S. Patent 5,936,975 (Okamura)_ Teaches semiconductor memory device with switching circuit for controlling internal addresses in parallel test.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mehdi Namazi whose telephone number is (703) 306-2758. The examiner can normally be reached on Monday-Thursday from 7:00 to 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do Hyun yoo, can be reached on (703) 308-4908.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-9600.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

**or faxed to:**

(703) 746-7239 (for formal communications intended for entry)


**Or:**
(703) 746-7240 (for informal or draft communications, please label PROPOSED or DRAFT )

Hand-delivered responses should be brought to Crystal Park 2,

2121 Crystal Drive,

Arlington, VA., Sixth Floor (Receptionist).


M. Namazi
October 1, 2001

DO HYUN YOO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

| FORM PTO-892 | U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE | SERIAL NO. 09/504,344 | GROUP ART UNIT 2187 | ATTACHMENT TO PAPER NO. | 3 |
|---|---|---|---|---|---|
| NOTICE OF REFERENCES CITED | | APPLICANT(S) Phelan | | | |

## U.S. PATENT DOCUMENTS

| * | | DOCUMENT NO. | DATE | NAME | CLASS | SUB-CLASS | FILING DATE |
|---|---|---|---|---|---|---|---|
| | A | 5,651,138 | 7/1997 | Le et al. | 711 | 154 | |
| | B | 5,805,928 | 9/1998 | Lee | 710 | 35 | |
| | C | 5,936,975 | 8/1999 | Okamura | 714 | 719 | |
| | D | 6,289,138 | 9/2001 | Yip et al. | 382 | 307 | |
| | E | 6,085,261 | 7/2000 | McIntyre, Jr. et al. | 710 | 35 | |
| | F | | | | | | |
| | G | | | | | | |
| | H | | | | | | |
| | I | | | | | | |
| | J | | | | | | |
| | K | | | | | | |

## FOREIGN PATENT DOCUMENTS

| * | | DOCUMENT NO. | DATE | COUNTRY | NAME | CLASS | SUB-CLASS |
|---|---|---|---|---|---|---|---|
| | L | | | | | | |
| | M | | | | | | |
| | N | | | | | | |
| | O | | | | | | |
| | P | | | | | | |
| | Q | | | | | | |

## OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

| | |
|---|---|
| R | |
| S | |
| T | |
| U | |

| EXAMINER Mehdi Namazi | DATE September 27, 2001 | Form892ccs2106b |
|---|---|---|

* A copy of this reference is not being furnished with this office action.
(See Manual of Patent Examining Procedure, section 707.05(a).)

# NOTICE OF DRAFTSPERSON'S
## PATENT DRAWING REVIEW

The drawing(s) filed (insert date) 2/14/00 are:

A. ☐ approved by the Draftsperson under 37 CFR 1.84 or 1.152.

B. ☒ objected to by the Draftsperson under 37 CFR 1.84 or 1.152 for the reasons indicated below. The Examiner will require submission of new, corrected drawings when necessary. Corrected drawing must be sumitted according to the instructions on the back of this notice.

1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings:
   Black ink. Color.
   ____ Color drawings are not acceptable until petiton is granted.
   Fig(s) _____
   ____ Pencil and non black ink not permitted. Fig(s) _____
2. PHOTOGRAPHS. 37 CFR 1.84 (b)
   ____ 1 full-tone set is required. Fig(s) _____
   ____ Photographs not properly mounted (must use brystol board or photographic double-weight paper). Fig(s) _____
   ____ Poor quality (half-tone). Fig(s) _____
3. TYPE OF PAPER. 37 CFR 1.84(e)
   ____ Paper not flexible, strong, white, and durable.
   Fig(s) _____
   ____ Erasures, alterations, overwritings, interlineations, folds, copy machine marks not accepted. Fig(s) _____
   ____ Mylar, velum paper is not acceptable (too thin).
   Fig(s) _____
4. SIZE OF PAPER. 37 CFR 1.84(f): Acceptable sizes:
   ____ 21.0 cm by 29.7 cm (DIN size A4)
   ____ 21.6 cm by 27.9 cm (8 1/2 x 11 inches)
   ____ All drawing sheets not the same size.
   Sheet(s) _____
   ____ Drawings sheets not an acceptable size. Fig(s) _____
5. MARGINS. 37 CFR 1.84(g): Acceptable margins:

   Top 2.5 cm  Left 2.5cm  Right 1.5 cm  Bottom 1.0 cm
   SIZE: A4 Size
   Top 2.5 cm  Left 2.5 cm  Right 1.5 cm  Bottom 1.0 cm
   SIZE: 8 1/2 x 11
   Margins not acceptable. Fig(s) 2,3,5A
   ____ Top (T)  ____ Left (L)
   ____ Right (R)  ____ Bottom (B)
6. VIEWS. 37 CFR 1.84(h)
   REMINDER: Specification may require revision to correspond to drawing changes.
   Partial views. 37 CFR 1.84(h)(2)
   ____ Brackets needed to show figure as one entity.
   Fig(s) _____
   ____ Views not labeled separately or properly.
   Fig(s) _____
   ____ Enlarged view not labeled seperetely or properly.
   Fig(s) _____
7. SECTIONAL VIEWS. 37 CFR 1.84 (h)(3)
   ____ Hatching not indicated for sectional portions of an object.
   Fig(s) _____
   ____ Sectional designation should be noted with Arabic or Roman numbers. Fig(s) _____

8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)
   ____ Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned so that the top becomes the right side, except for graphs. Fig(s) _____
9. SCALE. 37 CFR 1.84(k)
   ____ Scale not large enough to show mechanism without crowding when drawing is reduced in size to two-thirds in reproduction.
   Fig(s) _____
10. CHARACTER OF LINES, NUMBERS, & LETTERS.
    37 CFR 1.84(i)
    ____ Lines, numbers & letters not uniformly thick and well defined, clean, durable, and black (poor line quality).
    Fig(s) 1-6
11. SHADING. 37 CFR 1.84(m)
    ____ Solid black areas pale. Fig(s) _____
    ____ Solid black shading not permitted. Fig(s) _____
    ____ Shade lines, pale, rough and blurred. Fig(s) _____
12. NUMBERS, LETTERS, & REFERENCE CHARACTERS.
    37 CFR 1.84(p)
    ____ Numbers and reference characters not plain and legible.
    Fig(s) _____
    ____ Figure legends are poor. Fig(s) _____
    ____ Numbers and reference characters not oriented in the same direction as the view. 37 CFR 1.84(p)(1)
    Fig(s) _____
    ____ English alphabet not used. 37 CFR 1.84(p)(2)
    Figs _____
    ____ Numbers, letters and reference characters must be at least .32 cm (1/8 inch) in height. 37 CFR 1.84(p)(3)
    Fig(s) 1-6
13. LEAD LINES. 37 CFR 1.84(q)
    ____ Lead lines cross each other. Fig(s) _____
    ____ Lead lines missing. Fig(s) _____
14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.84(t)
    ____ Sheets not numbered consecutively, and in Arabic numerals beginning with number 1. Sheet(s) _____
15. NUMBERING OF VIEWS. 37 CFR 1.84(u)
    ____ Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig(s) _____
16. CORRECTIONS. 37 CFR 1.84(w)
    ____ Corrections not made from prior PTO-948 dated _____
17. DESIGN DRAWINGS. 37 CFR 1.152
    ____ Surface shading shown not appropriate. Fig(s) _____
    ____ Solid black shading not used for color contrast.
    Fig(s) _____

COMMENTS

REVIEWER  M.O  DATE 9/27/01  TELEPHONE NO. _____

ATTACHMENT TO PAPER NO. 3

# INFORMATION ON HOW TO EFFECT DRAWING CHANGES

## 1. Correction of Informalities--37 CFR 1.85

File new drawings with the changes incorporated therein. The application number or the title of the invention, inventor's name, docket number (if any), and the name and telephone number of a person to call if the Office is unable to match the drawings to the proper application, should be placed on the back of each sheet of drawings in accordance with 37 CFR 1.84(c). Applicant may delay filing of the new drawings until receipt of the Notice of Allowability (PTOL-37). Extensions of time may be obtained under the provisions of 37 CFR 1.136. The drawing should be filed as a separate paper with a transmittal letter addressed to the Drawing Processing Branch.

## 2. Timing for Corrections

Applicant is required to submit **acceptable** corrected drawings within the three-month shortened statutory period set in the Notice of Allowability (PTOL-37). If a correction is determined to be unacceptable by the Office, applicant must arrange to have acceptable corrections resubmitted within the original three-month period to avoid the necessity of obtaining an extension of time and paying the extension fee. Therefore, applicant should file corrected drawings as soon a possible.

Failure to take corrective action within set (or extended) period will result in **ABANDONMENT** of the Application.

## 3. Corrections other than Informalities Noted by the Drawing Review Branch on the Form PTO-948

All changes to the drawings, other than informalities noted by the Drawing Review Branch, **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes.

# Attachment for PTO-948 (Rev. 03/01, or earlier)
## 6/18/01

## The below text replaces the pre-printed text under the heading, "Information on How to Effect Drawing Changes," on the back of the PTO-948 (Rev. 03/01, or earlier) form.

## INFORMATION ON HOW TO EFFECT DRAWING CHANGES

### 1. Correction of Informalities -- 37 CFR 1.85

New corrected drawings must be filed with the changes incorporated therein. Identifying indicia, if provided, should include the title of the invention, inventor's name, and application number, or docket number (if any) if an application number has not been assigned to the application. If this information is provided, it must be placed on the front of each sheet and centered within the top margin. If corrected drawings are required in a Notice of Allowability (PTOL-37), the new drawings **MUST** be filed within the **THREE MONTH** shortened statutory period set for reply in the Notice of Allowability. Extensions of time may NOT be obtained under the provisions of 37 CFR 1.136(a) or (b) for filing the corrected drawings after the mailing of a Notice of Allowability. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

### 2. Corrections other than Informalities Noted by Draftsperson on form PTO-948.

All changes to the drawings, other than informalities noted by the Draftsperson, **MUST** be made in the same manner as above except that, normally, a highlighted (preferably red ink) sketch of the changes to be incorporated into the new drawings **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes.

### Timing of Corrections

Applicant is required to submit the drawing corrections <u>within the time period set in the attached Office communication</u>. See 37 CFR 1.85(a).

Failure to take corrective action within the set period will result in **ABANDONMENT** of the application.

06/01/01

Attorn    Docket: 0325.003

IN RE APPLICATION OF:    Cathal G. Phelan

SERIAL NO.:    09/504,344

TITLE:    FIXED BURST MEMORIES

FILED:    February 14, 2000

EXAMINER:    Namzai, M.

ART UNIT:    2187

RESPONSE TRANSMITTAL AND
EXTENSION OF TIME REQUEST
(IF REQUIRED)

*Ext of time
2-26-02*

RECEIVED

FEB 2 2 2002

Technology Center 2100

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Sir:

Enclosed please find an amendment, copies of three patents and a postcard along with the fee calculation below:

**FEE CALCULATION FOR ENCLOSED AND EXTENSION REQUEST (IF ANY)**

|  | Claims Remaining | Highest No. Previous | Extra    Rate | Additional Fee |
|---|---|---|---|---|
| Total Claims | 20    minus | 20    = | 0    x $ 18.00 | $ 0.00 |
| Independent Claims | 3    minus | 3    = | 0    x $ 84.00 | $ 0.00 |
| Multiple Dependent Claim First Added | | | + $280.00    $ 0.00 | |

TOTAL IF NOT SMALL ENTITY .. $0.00

[ ]    SMALL ENTITY STATUS - If applicable, divide by 2 ..................... $0.00
[ ]    Verified statement enclosed, if not previously filed.

[X]    Applicant also requests a __one__ month extension of time
       for response to the outstanding Office Action. The fee is .................. $110.00

[ ]    Fee set forth in 37 C.F.R. 1.17 (p) for Information Disclosure
       under 37 C.F.R. 1.97 (c) ........................................ $0.00

       TOTAL FEE ........................................ $110.00

The Commissioner is hereby authorized to charge any overpayment or underpayment of the above fee associated with this Communication to Deposit Account No. 50-0541. A duplicate copy of this sheet is attached.

CHRISTOPHER P. MAIORANA, P.C.

24025 Greater Mack, Suite 200          By: _____
St. Clair Shores, Michigan 48080              Christopher P. Maiorana
(586) 498-0670                                Registration No.: 42,829

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on __February 4, 2002__.

2/21/2002 BNGUYEN1 00000033 09504344

By: _____
       Mary Donna Berkley

1 FC:115                110.00 OP

# US PATENT & TRADEMARK OFFICE
## PATENT FULL TEXT AND IMAGE DATABASE

Home    Boolean    Manual    Number    Help

Hit List    Prev    Next    Bottom

View Shopping Cart    Add to Shopping Cart

Images

( 5 of 17 )

United States Patent                                             6,188,638

Kuhne                                                  February 13, 2001

Integrated semiconductor memory with control device for clock-synchronous writing and reading

### Abstract

In an integrated semiconductor memory with clock-synchronous read and write accesses, the access control device is configured to be switchable between one-way and two-way data strobe mode. The access mode is set using a bond option or a mode register.

RECEIVED
FEB 2 2 2002
Technology Center 2100

Inventors:  **Kuhne; Sebastian** (Munchen, DE)
Assignee:   **Siemens Aktiengesellschaft** (Munich, DE)
Appl. No.:  **384701**
Filed:      **August 27, 1999**

### Foreign Application Priority Data

Aug 27, 1998[DE]                              198 39 105

**Current U.S. Class:**                    **365/233**; 365/51; 365/63
**Intern'l Class:**                           G11C 008/18
**Field of Search:**                  365/233,63,51,189.12

### References Cited [Referenced By]

#### U.S. Patent Documents

| 5572479 | Nov., 1996 | Satou | 365/230. |
|---------|-----------|-------|----------|
| 5629903 | May., 1997 | Agata | 365/233. |

#### Foreign Patent Documents

| 54-123841 | Sep., 1979 | JP | |
|-----------|-----------|----|----|

## Other References

"A 2.5-ns Clock Access, 250-MHz, 256 Mb SDRAM with Synchronous Mirror Delay",
Takanori Saeki et al., IEEE Journal of Solid-State Circuit, vol. 31, No. 11, Nov. 1996, pp.
1656-1668.
JEDEC, Solid State Technology Division, Council Ballot, JCB-98-46, Apr. 20, 1998,
Arlington, Virginia, pp. 1-16.

---

## *Claims*

---

I claim:

1. An integrated semiconductor memory, comprising:

a multiplicity of storage cells;

a control device for clock-synchronous writing and for reading a data value to and from one of said multiplicity of storage cells, said control device controlling the writing such that the data value represented in a data signal received by the control device is coupled to a second clock signal and the second clock signal is coupled to a first clock signal received by said control device, said control device controlling the reading such that, in a first operating mode, the data value represented by the data signal being coupled only to the first clock signal, and in a second operating mode the data value represented by the data signal being coupled to the second clock signal and the second clock signal is coupled to the first clock signal; and

a device for producing a control signal to be fed to said control device for switching over between the first operating mode and the second operating mode.

2. The integrated semiconductor memory according to claim 1, wherein said device includes at least two connection pads having a first pad coupled to said control device for providing the control signal and a second pad for receiving a constant potential, said first pad connected to said second pad in one of the first operating mode and the second operating mode, and no connection is made between said first pad and said second pad in the other of the first operating mode and the second operating mode.

3. The integrated semiconductor memory according to claim 2, including a bonding wire for forming a connection between said first pad and said second pad.

4. The integrated semiconductor memory according to claim 3, including a lead frame having fingers and said bonding wire is fed from said first pad to one of said fingers of said lead frame, said one of said fingers connected to said second pad.

5. The integrated semiconductor memory according to claim 2, wherein said second pad is to be connected to a first pole of a supply voltage.

6. The integrated semiconductor memory according to claim 5, including a resistor and a conductor carrying the control signal, said conductor is coupled via said resistor to a second pole of the supply voltage.

7. The integrated semiconductor memory according to claim 1, including a storage element having an output connected to said control device for delivering the control signal to said control device.

8. The integrated semiconductor memory according to claim 7, wherein during a initializing phase, a status of said storage element can be set as a function of a further data value that can be input externally.

---

## *Description*

---

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The invention relates to an integrated semiconductor memory having a multiplicity of storage cells as well as a control device for clock-synchronous writing and reading of a data value.

Integrated semiconductor memories with clock-synchronous input and output are known as SDRAMs. Standardization is desirable for a time profile of the signals during the input and output, for example JEDEC, Solid State Technology Division, Council Ballot, JCB-98-46, 20 April 1998, Arlington, Va. According to the standardization proposal, data input and data output signals are coupled to a sampling signal (data strobe signal). The data strobe signal is produced internally to the chip. It is for its part coupled to an externally provided clock which also controls the other functional units of the semiconductor memory. The respective signal profiles for the data output and data input are presented in FIG. 5-1 and FIG. 9.1 of the JEDEC standardization proposal. The data strobe signal is also provided outside the integrated semiconductor memory. It is then available to the modules communicating with the semiconductor memory, in order to control the data interchange during a memory access. This requires a corresponding circuit outlay in the system environment of the semiconductor memory.

SUMMARY OF THE INVENTION

It is accordingly an object of the invention to provide an integrated semiconductor memory with a control device for clock-synchronous writing and reading that overcomes the above-mentioned disadvantages of the prior art devices of this general type, which is universally usable.

With the foregoing and other objects in view there is provided, in accordance with the invention, an integrated semiconductor memory, including:

a multiplicity of storage cells;

a control device for clock-synchronous writing and for reading a data value to and from one of the multiplicity of storage cells, the control device controlling the writing such that the data value represented in a data signal being received by the control device is coupled to a second clock signal and the second clock signal is coupled to a first clock signal received by the control device, the control device controlling the reading such that, in a first operating mode, the data value represented by the data signal is coupled only to the first clock signal, and in a second operating mode the data value represented by the data signal is coupled to the second clock signal and the second clock signal is coupled to the first clock signal; and

a device for producing a control signal to be fed to the control device for switching over between the first operating mode and the second operating mode.

The semiconductor memory according to the invention is operated in the first or the second operating mode during a reading operation. In the first operating mode, the output data signal is coupled only to the system clock that is present in any case and controls the other functional units of the semiconductor memory. In the second operating mode, as in the JEDEC standardization proposal, a further clock signal is provided which is used as a data strobe signal and to which the data output signal is coupled. Since, according to the JEDEC standardization proposal, the coupling between the clock signal, data strobe signal and data signal is tight, that is to say the time tolerance of the relative time reference of the signals with respect to one another is small, the first operating mode without using the data strobe signal is compatible with the second operating mode with use of the data strobe signal. Therefore, the user of the integrated semiconductor memory has a multifunctional semiconductor memory which allows clock-synchronous reading of the semiconductor memory both with and without a data strobe signal.

Refinements of the invention relate to the ways of setting the first and second operating modes. The operating mode can be set using what is referred to as *bond options*. To do this, a control signal controlling the switching between the first and second operating modes is provided by a bonding pad. The way in which it is bonded defines the signal. A constant voltage, for example a supply voltage, is applied to the pad in order to set one operating mode. To do this, a bonding wire is bonded from the pad to a lead finger which is at a supply potential. The lead finger is conventionally also bonded to a further supply potential pad. For the other operating mode, the pad remains unconnected, the control signal being produced internally to the circuit by pull-up or pull-down elements.

As an alternative to the bond option, the control signal may be set by a mode register. A register of this type is in any case present on the integrated semiconductor chip for setting other operating parameters. The control signal is tapped at the output of a memory element of the mode register. The memory element is set to the desired status during a phase of initializing the semiconductor chip. This status is externally delivered to the mode register, for example by a microcontroller controlling the system.

Although the semiconductor memory can be operated in various operating modes during reading, only a single circuit configuration is necessary. By simple methods such as the bond option or setting the mode register, the operating mode is tailored to the system environment in question.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied in an integrated semiconductor memory with a control device for clock-synchronous writing and reading, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagrammatic, fragmentary, view of an integrated semiconductor memory with operating modes being set using a bond option according to the invention;

FIG. 2 is a block diagram of an excerpt for the case in which the operating modes are set using a mode register;

FIG. 3 is a circuit diagram of a circuit input of a control device for the bond option;

FIG. 4 is a signal diagram for a write access;

FIG. 5 is a signal diagram for a read and write access according to a first operating mode; and

FIG. 6 is a signal diagram for a read and write access according to a second operating mode.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

In all the figures of the drawing, sub-features and integral parts that correspond to one another bear the same reference symbol in each case. Referring now to the figures of the drawing in detail and first, particularly, to FIG. 1 thereof, there is shown a semiconductor memory containing four memory banks 1, 2, 3, 4. Each memory bank 1-4 contains a multiplicity of storage cells. Between the memory banks 1-4, usually at an edge of each memory bank 1-4, functional units are disposed which control the operation of the memory bank 1-4. They may be circuits for address decoding, for storage cell refresh of dynamic memories and similar circuits. In particular, a control device 5 for time control of memory accesses is provided at the edge of the memory bank 1. A line 11 leads into a memory cell array in order to write data values there into a storage cell or read data values from it. A line 12 is connected to a connection pad 10 at which data represented by a data signal DQ are taken from the memory or delivered to it. Via a connection pad 6, a clock signal CK, which controls the functional units within the memory, is fed to the memory. The time control of the control device 5 is likewise derived from the clock signal CK.

The signal profile during a write access to the memory is represented in FIG. 4. FIG. 4 shows the clock signal CK as well as its complement, a further clock signal DQS coupled to the clock signal CK and a data signal DQ with the data values to be entered. The further clock signal DQS is a so-called data strobe signal using which the data DQ are validated. The data strobe signal DQS is necessary for preventing runtime problems. For this purpose, the data signal DQ is always transmitted together with the data strobe signal DQS. The data signal DQ is available clock-synchronized with the data strobe signal DQS. The data strobe signal DQS is produced inside the control device 5 coupled to the system clock CK. The data values of the data signal DQ are coupled to the data strobe signal DQS to within a certain tolerance. Therefore, the data values of the data signal DQ are, in relation to the data strobe signal DQS validly applied at least at a predetermined setup time tQDQSS before a reference edge of the signal DQS and a holding time tQDQSH after the edge. Overall, the data signal DQ is therefore temporally coupled to the data strobe signal DQS, which is in turn coupled to the system clock CK.

A data value is read from the semiconductor memory alternately according to a first or a second operating mode. The access control device 5 switches between the two operating modes according to a control signal CTRL delivered to it. The time profile of the relevant signals during the first operating mode is represented in FIG. 5. The data signal DQ is coupled directly within certain time tolerances to the system clock CK. A tolerance tAC for the access time is indicated in FIG. 5.

In the second operating mode, for which the time profile of the relevant signals in represented in FIG. 6, the data strobe signal DQS, to which the output signal DQ is coupled within the window for the access time tAC, is provided. For its part, the data strobe signal DQS is coupled to the system clock CK. There is a tolerance tDQSCK between the system clock CK and the data strobe signal DQS. In the second operating mode, the data signal DQ is therefore coupled to the data strobe signal DQS, which is in turn coupled to the

system clock CK.

If the control device 5 is in the first operating mode setting, the data strobe signal DSQ is used when writing, but not when reading. This operating mode setting is therefore referred to as one-way data strobe mode. When the control device 5 is in the second operating mode setting, the data strobe signal is used both for writing and for reading. This operating mode setting is therefore referred to as two-way data strobe mode. The control device 5 can be switched over between one-way and two-way data strobe mode using the control signal CTRL.

In order to switch over between the two modes, or operating mode settings, the alternative embodiment options shown in FIGS. 1 and 2 are available. The representation in FIG. 1 uses the so-called bond option. For this purpose, a connection pad 7 is provided, which is connected to the control device 5. The control signal CTRL is provided at the pad 7. In order to set one of the operating modes, for example the two-way data strobe mode, one of the supply potentials, in this case the supply potential VDD, is applied to the pad 7. To do this, the pad 7 is connected via a bonding wire 13 to a finger 15 of a lead frame 14-16 that is at the potential VDD. The finger 15 of the lead frame 14-16 is further connected via a bonding wire 17 to a pad 8, which delivers the supply potential VDD to the other functional units of the semiconductor memory. The finger 15 expediently has a branch 15a on the chip side, to which the bonding wire 13 is connected. In the known way, the lead frame contains a multiplicity of fingers, of which the fingers 14, 15 and 16 are represented. These are respectively bonded at one end to a pad on the integrated circuit. The other end is fed out of the package and is used, for example, as a connection pin to which a supply potential or a signal is to be applied. In the embodiment represented, the control signal CTRL is at the potential VDD that is interpreted in the control device 5 as an instruction to set the two-way data strobe mode. In order, instead of this, to set the one-way data strobe mode, the pad 7 is unconnected. The control signal CTRL is then at the potential VSS for the one-way data strobe mode, this being obtained by a pull-down resistor 21 in the device 5 (see FIG. 3).

FIG. 3 represents an input stage of the control device 5. It contains an inverter 20 that is connected on an input side to the pad 7. On an output side, the inverter 20 carries a signal CTRL' which is further processed in the device 5. While one of the operating mode settings, for example two-way data strobe mode, is established using a bonding connection of the pad 7 to the lead finger 15 for the supply potential VDD, for setting the other operating mode, for example one-way data. strobe mode, the pad 7 remains unconnected. The pull-down resistor 21 draws the potential of a line 22 to ground potential VSS. If, as an alternative, the pad 7 for connection to a lead finger for the supply potential VSS is provided, then a pull-up resistor is connected between the input of the inverter 20 and the positive supply potential VDD. The two-way data strobe mode is in this case obtained by the control signal CTRL with the level of the supply potential VSS, when the pad 7 is connected to the lead finger which is at this potential VSS, and the one-way data strobe mode is obtained by the control signal with the level of the supply potential VDD when the pad 7 is unconnected.

As an alternative to the bond option, it is expedient to set the operating mode of the control device 5 using a mode register 30. The mode register 30 has a multiplicity of storage cells 31 whose stored statuses define operating parameters of the semiconductor memory. A storage cell 31 contains one of the two statuses of the control signal CTRL and is connected on an output side to the control device 5.

The mode register 30 is conventionally preloaded with data MI during an initialization procedure. Preferably, the initialization procedure takes place following the application of the supply voltage during the so-called power-up phase. At the start of normal operations, the desired operating mode setting is therefore already provided. The initialization data MI for the mode register 30 are externally delivered to the semiconductor memory and, for example, produced by a microcontroller that controls the application system which contains the semiconductor memory.
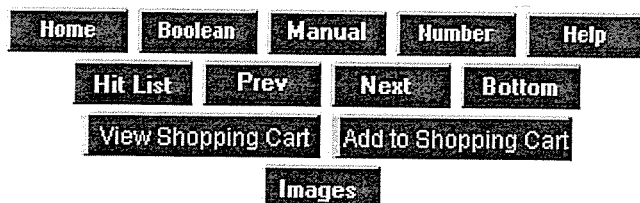
Irrespective of the desired operating mode (one-way or two-way data strobe mode) the same circuit configurations are used. The operating mode is not set until bonding after the silicon production in the back end processing or, as an alternative, the desired operating mode is set in the target system itself during the initialization phase.
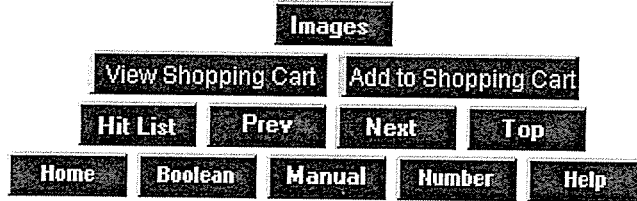
\* \* \* \* \*

Images

View Shopping Cart    Add to Shopping Cart

Hit List    Prev    Next    Top

Home    Boolean    Manual    Number    Help

# US PATENT & TRADEMARK OFFICE
## PATENT FULL TEXT AND IMAGE DATABASE

United States Patent                                                                                       **5,900,021**

**Tiede , et al.**                                                                                          **May 4, 1999**

## Pad input select circuit for use with *bond options*

### Abstract

A configurable input device for an integrated circuit having a plurality of input pads, the input device including a plurality of buffers, where each buffer is associated with one of the input pads. Each buffer receives a mode select signal and the buffer is responsive to the mode select signal to place the buffer in an enabled mode or a disabled mode. A receiver portion within each buffer is coupled to the associated input pad. The receiver portion pulls the associated input pad to a preselected logic state while the buffer is in the disabled mode. An output driver within each buffer generates an output signal responsive to a signal on the associated input pad while the buffer is in the enable mode and provides a high impedance while the buffer is in the disabled mode. An output node is coupled to the output drivers of the plurality of buffers.

| | |
|---|---|
| Inventors: | **Tiede; John William** (Colorado Springs, CO); **Faue; Jon Allan** (Colorado Springs, CO) |
| Assignee: | **United Memories, Inc.** (Colorado Springs); **Nippon Steel Semiconductor Corporation** (Chiba, JP) |
| Appl. No.: | **833105** |
| Filed: | **April 4, 1997** |

| | |
|---|---|
| **Current U.S. Class:** | 711/170; 365/189.02; 365/230.02 |
| **Intern'l Class:** | G06F 012/00; G11C 007/00 |
| **Field of Search:** | 711/170 365/189.02,230.02 395/653 |

### References Cited [Referenced By]

#### U.S. Patent Documents

| 4551634 | Nov., 1985 | Takahashi et al. | |
| 4825099 | Apr., 1989 | Barton | 307/270. |
| 5373470 | Dec., 1994 | Jones, Jr. | 365/189. |
| 5406525 | Apr., 1995 | Nicholes. | |
| 5572718 | Nov., 1996 | Scriber et al. | |
| 5600271 | Feb., 1997 | Erickson et al. | 327/108. |
| 5706235 | Jan., 1998 | Roohparvar et al. | 365/201. |
| 5757704 | May., 1998 | Hachiya | 365/189. |

## Foreign Patent Documents

| 0 198 429 A2 | Oct., 1986 | EP. |
| 0 513 968 A2 | Nov., 1992 | EP. |
| 2 271 449 | Apr., 1994 | GB. |

*Primary Examiner:* Swann; Tod R.
*Assistant Examiner:* Thai; Tuan V.
*Attorney, Agent or Firm:* Bachand; Richard A., Langley; Stuart T. Holland & Hart llp

---

## *Claims*

---

We claim:

1. A configurable memory device comprising:

an array of memory cells arranged in a plurality of rows and columns;

a control circuit receiving a plurality of address and control signals and generating a plurality of row select signals to selected rows in the array, a plurality of column select signals to selected columns in the array, and timing signals;

a first input receiving node capable of receiving a first external signal;

a second input receiving node capable of receiving a second external signal;

an input select circuit having data inputs coupled to the first and second input receiving nodes, and an output coupled to provide one of the address and control signals to the control circuit, wherein the input select circuit includes a select device coupled to receive a mode select signal, the input select circuit being responsive to the mode select signal to couple a selected one of the first and second input receiving nodes to the output of the input select circuit; and

a pull-down device responsive to the mode select signal to couple the unselected one of the first and second input pads to a power supply voltage.

2. The configurable memory device of claim 1 further comprising an enable device responsive to the mode select signal to provide a high impedance between the unselected one of the first and second input receiving nodes and the output.

3. The configurable memory circuit of claim 1 wherein the select device comprises a third input receiving node coupled to a power supply terminal.

4. The configurable memory circuit of claim 1 wherein the input select circuit comprises:

a first buffer having an input coupled to the first input receiving node and an output responsive to a signal on the first input receiving node;

an enable input node, wherein the first buffer is responsive to the enable input node to provide a high impedance between the first input receiving node and the first buffer output; and

a second buffer having an input coupled to the second input receiving node and an output responsive to a signal on the second input receiving node, wherein the second buffer is responsive to the enable input node to provide a high impedance between the second input receiving node and the second buffer output, wherein the output node of the input select circuit is coupled to the outputs of the first and second buffers.

5. The configurable memory circuit of claim 4 wherein the first buffer further comprises:

an n-channel transistor having a first source/drain electrode coupled to the output node of the input select circuit, a second source/drain electrode coupled to ground, and a gate electrode;

a p-channel transistor having a first source/drain electrode coupled to Vcc, a second source/drain electrode coupled to the output node of the input select circuit, a gate electrode coupled the first input receiving node, and coupled to the gate of the n-channel transistor.

6. The configurable memory circuit of claim 1 wherein the pull down device comprises:

a first p-channel transistor coupling the first input receiving node to the power supply voltage under control of a first control signal;

a second p-channel transistor coupling the second input receiving node to the power supply voltage under control of a second control signal;

combinatorial logic coupled to receive the mode select signal and generate the first and second control signals.

7. An input device comprising:

an input pad capable of receiving an input signal;

a mode select node providing a mode select signal;

a pull-down device coupled to the input pad for pulling the input pad to a first logic state under control of the mode select signal;

a first n-channel transistor pulling an output of the input device to the first logic state under control of the input pad;

a first p-channel transistor having an output under control of the input pad, wherein the output of the first p-channel transistor is pulled to a second logic state when the input pad is in the first logic state;

a power gate node for providing a power gate signal;

a second p-channel transistor having an output coupling the output of the input device to the output of the first p-channel transistor under control of the power gate signal

a second n-channel transistor having an output under control of the power gate signal, wherein the output of the second n-channel transistor is pulled to the first logic state when the power gate signal is in the second logic state; and

a third n-channel transistor having an output coupling the output of the second n-channel transistor to the output of the input device under control of an inverted form of the mode select signal.

8. The input device of claim 7 further comprising a transmission gate coupled to the power gate node for coupling an external power gate signal to the power gate node under control of the mode select signal.

9. The input device of claim 7 wherein when the mode select signal is in the first logic state the output of input device is responsive to the input signal, and when the mode select signal is in the second logic state all of the transistors directly coupled to the output node of the input device are turned off.

10. A configurable input device for an integrated circuit having a plurality of input pads, the input device comprising:

a plurality of buffers, wherein each buffer is associated with one of the input pads and each buffer receives a mode select signal, wherein the buffer is responsive to the mode select signal to place the buffer in an enabled mode or a disabled mode;

a receiver portion within each buffer coupled to the associated input pad, the receiver portion pulling the associated input pad to a preselected logic state while the buffer is in the disabled mode;

an output driver within each buffer, the output driver generating an output signal responsive to a signal on the associated input pad while the buffer is in the enable mode and providing a high impedance while the buffer is in the disabled mode, and

an output node coupled to the output drivers of the plurality of buffers.

11. The input circuit of claim 10 further comprising combinatorial logic receiving a control signal and generating the mode select signal to each buffer.

12. The input circuit of claim 11 wherein the combinatorial logic generates the mode select signal such that no more than one of the plurality of buffers is in the enabled mode.

13. The input circuit of claim 10 wherein the output driver comprises:

an n-channel transistor having a source/drain electrode coupled to the output node, a second source/drain electrode coupled to ground, and a gate electrode;

a p-channel transistor having a first source/drain electrode coupled to a first logic state, a second source/drain electrode coupled to the output node, a gate electrode coupled to one of the plurality of pads, and coupled to the gate of the n-channel transistor.

14. The input circuit of claim 13 wherein the output driver further comprise a high impedance switch coupled between the p-channel s/d and the output node, the high impedance switch being responsive to the mode select signal to selectively couple the p-channel s/d to the output node.

15. A method for configurably coupling an input pad to an internal circuit node of an integrated circuit comprising the steps of:

providing a plurality of input pads on an integrated circuit;

providing a mode select signal on a mode select node;

coupling a selected one of the plurality of input pads to an internal circuit node in response to the mode select signal; and

controlling a pull-down device to pull the unselected input pads to a first logical state in response to the mode select signal.

16. The method of claim 15 wherein the first logical state is represented by a ground voltage potential.

17. The method of claim 15 further comprising the steps of:

receiving a power gate signal on a power gate node; and

controlling impedance between the unselected input pads and the internal circuit node in response to the power gate signal in combination with the mode select signal.

18. The method of claim 15 further comprising the steps of:

receiving a power gate signal over a power gate node; and

placing all transistors having outputs coupled to the internal circuit node in a high impedance state in response to the power gate signal in combination with the mode select signal.

---

### *Description*

---

## BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates, in general, to semiconductor integrated circuits, and, more particularly, to a circuit for configuring input devices in an integrated circuit.

2. Relevant Background

In the production and manufacturing of different types of integrated circuits (ICs) it is desirable to have a single IC that can be packaged to operate with different interfaces. For example, a random access memory (RAM) may be configured as a "by-16" device or a "by-8" device. When configured as a by-16 device, the RAM receives sixteen data bits at sixteen data input/output (I/O) pins. These input data bits represent a single 16-bit word that is stored in the RAM at a location determined by address bits received at the

address pins. In a by-8 device only eight bits of data are input to the RAM at one time.

For a given memory size (e.g., a 4 megabyte (MB) dynamic random access memory (DRAM)) much of the internal circuitry of a by-16 device can be identical to that of a by-8 device. However, the external control and data signals that are applied to the device differ between the two configurations. For example, a 4 MB by-16 device is typically packaged in a 40-pin plastic small outline J-lead (SOJ) or a 44-pin thin, small-outline package (TSOP) to provide an adequate number of pins for the 16-bit wide data bus. A 4 MB by-8 device, however, is typically packaged in a 28-pin SOG or 28-pin TSOP package. With respect to control signals, a by-16 device may require two column address strobe (CAS) signals or two write enable (WE) signals to separately activate columns in lower and upper memory banks within the chip. In contrast, a by-8 device uses a single CAS and WE signal, together with an additional address bit, to access data stored in both the upper and lower banks.

In spite of the great similarity between by-16 and by-8 devices from the standpoint of internal circuitry, most manufacturers must produce two separate IC designs to account for the different pin-outs and control signals. A by-16 device may be realized as an entirely different chip design and layout from the by-8 device, or the chips may differ only by customization of one or more metal layers. In either case, a particular chip must be committed to a by-8 or a by-16 design during the wafer fabrication process.

From a manufacturing efficiency standpoint, it is desirable to fabricate multiple device configurations using a single integrated circuit design. Not only is design time used more efficiently, but a single chip design simplifies scheduling and work flow in a wafer fabrication facility. Because the semiconductor fabrication process takes several weeks to process raw substrates into packaged electronic devices, a great deal of effort is placed in predicting customer orders so that finished goods are available when customers demand. For these reasons, it is desirable to be able to select the configuration of a semiconductor device as late as possible in the manufacturing process.

Many configurable circuits are available that allow the end-user to change the configuration after the manufacturing process is completed. Examples include field programmable gate arrays (FPGAs) and programmable logic devices (PLDs). However, these circuits tend to be cost prohibitive except for specialized applications. In cost sensitive markets such as exists for memory devices, user-configurable circuits are usually impractical. What is needed is a configurable input circuit that allows configuration to be chosen late in the manufacturing process, preferably during the assembly and packaging stages.

Semiconductor devices are manufactured to meet industry standards for functionality and performance. These standards dictate the packaging and pin-out configuration of most semiconductor devices. This standardization allows commodity devices supplied by one manufacturer to be substituted for those of another manufacturer. Any internal circuitry used to enable configurability must be implemented in a manner that allows compliance with industry standards, and does not adversely impact device functionality, performance and reliability.

## SUMMARY OF THE INVENTION

Briefly stated, the present invention involves a configurable input device for an integrated circuit having a plurality of input pads, the input device including a plurality of buffers, where each buffer is associated with one of the input pads. Each buffer receives a mode select signal and the buffer is responsive to the mode select signal to place the buffer in an enabled mode or a disabled mode. A receiver portion within each buffer is coupled to the associated input pad. The receiver portion pulls the associated input pad to a preselected logic state while the buffer is in the disabled mode. An output driver within each buffer generates an output signal responsive to a signal on the associated input pad while the buffer is in the enable mode and provides a high impedance while the buffer is in the disabled mode. An output node is

f 12

coupled to the output drivers of the plurality of buffers.

In another aspect, the present invention involves a method for configurably coupling an input pad to an internal circuit node of an integrated circuit. In accordance with the method a mode select signal is provided on a mode select node. A selected one of the plurality of input pads is coupled to an internal circuit node in response to the mode select signal. A pull-down device is controlled to pull the unselected input pads to a first logical state in response to the mode select signal.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows in outline form a representation of a first implementation of a memory circuit embodying the present invention;

FIG. 2 shows in outline form a representation of a second implementation of the memory circuit in accordance with the present invention;

FIG. 3 shows in block diagram form a memory circuit embodying an pad input select circuit in accordance with the present invention;

FIG. 4 shows in block diagram form a first portion of a generic implementation of a configurable input circuit in accordance with the present invention;

FIG. 5 illustrates in block diagram form a second portion of the generic implementation of the configurable input circuit in accordance with the present invention; and

FIG. 6 illustrates a particular embodiment of the present invention in a memory device.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Typically, an input pad is coupled to a buffer circuit that may latch, invert, or simply buffer a signal on the input pad. The output of the buffer is then coupled through an internal circuit node to additional logic on the integrated circuit (IC). Often, the buffer output is gated by a power gating signal that is generated by internal circuitry on the IC. This gating allows the input pads to be decoupled from the internal circuitry to prevent conflicts that may interfere with circuit performance. Gating is optional.

As used herein, the term "configurable ICs" means devices that can be configured during manufacturing to operate in one of several selected modes. The term is not intended to include programmable logic or user configurable logic such as programmable gate arrays unless such devices also include configuration options that are fixed during manufacturing. Specifically, the present invention is directed to configuration options that are selected during the packaging process by, for example, bond wire options.

Using **bond options** configuration, a mode select signal can be permanently provided to the IC by selectively bonding mode configuration pads to ground or power busses. Combinatorial logic coupled to the mode configuration pads generates internal configuration signals that enable and/or disable portions of the internal circuitry to realize a desired configuration option. Because the mode select signals are chosen by permanent bonds, the configuration cannot be changed after packaging. However, bonding occurs very late in the IC manufacturing process and allows great flexibility to select the final device configuration to meet customer demand just before completing manufacturing.

**Bond options** are an increasingly important feature in many modern semiconductor devices, especially memory devices. By tying a configuration pad high or low it is possible to change the entire configuration

of an IC. For example, a 4 MB DRAM can be organized as a 512K.times.8 device (i.e., a "by-8" device shown in FIG. 1) or as a 256K.times.16 device (i.e., a "by-16" device shown in FIG. 2) depending on the state of the configuration pad. In accordance with the present invention, the same chip 101 can be used in either the configuration of FIG. 1 or FIG. 2. IC 101 is not configured until bonds coupling pads 103 to device pins 102 and 202 are formed.

Because **bond options** or mode configuration options are available on IC 101, the exact input pad 103 from which a control or data signal may come may change depending on the configuration. For example, by-16 device 200 receives active-low upper CAS (labeled UCAS) and active-low lower CAS (labeled LCAS) control signals while by-8 device 100 requires only one CAS signal. As used herein, a signal identifier designated with a bar indicates an active low signal, while the absence of a bar indicates an active high signal. Input circuit 301 (shown in FIG. 3) in accordance with the present invention steers the correct input pad 103 to the internal circuit path where it is required. This allows various internal circuitry and circuit paths to function the same regardless of the mode specified by the bond option. Preferably, all of the unused input pads 103 are disabled.

FIG. 3 shows an exemplary IC 101 incorporating a pad input select circuit 301 in accordance with the present invention. In the particular example, IC 101 is a 4 MB DRAM circuit that is configurable as a by-8 or a by-16 device. The configuration of IC 101 is accomplished by setting the signal level on the configuration pad (labeled CONFIG) to select circuit 301. The preferred technique for setting the voltage level is to bond the CONFIG pad to either the VCC or the VSS power supply bus.

A single CONFIG pad with a binary signal level will allow pad input select circuit 301 to select between two configuration options. If more configuration options are desired, multiple binary CONFIG pads can be provided. In cases where only one CONFIG pad is used, the signal on the CONFIG pad can be used directly as a mode select signal in pad input select circuit 301. In cases where multiple CONFIG pads are used, pad input select circuit will require additional combinatorial logic (not shown) to generate one or more mode select signals having desired properties to meet the needs of a particular application. Design and implementation of the combinatorial logic can be accomplished using available logic design techniques.

Pad input select circuit 301 receives the active-low output enable (OE) signal, the active-low by-16 lower column address strobe (X16 LCAS on node 310), the active-low by-16 upper column address strobe (X16 UCAS on node 315) and the active-low by-8 column address strobe (X8 CAS on node 305) signals. Pad input select circuit 301 serves to select one of the X16 UCAS and X8 CAS signals to couple as the modified active-low upper column address strobe (UCAS') signal to timing and control signal generator 302. Also, pad input select circuit 301 serves to select one of the X16 LCAS and X8 CAS signals to couple as the modified active-low lower column address strobe (LCAS') signal to timing and control signal generator 302. Pad input select circuit 301 also generates one or more modified active-low output enable signals such as OE' (L) and OE' (U) to output control circuit 316 in the preferred implementation.

Control signal generator 302 receives two active-low column address strobe signals as expected by a convention control signal generator used in a by-16 device. IC 101 has three input pads supporting CAS signals, of which only one or two are used for any selected configuration. A first of the column address strobe inputs is selected from either the input pad coupled to node 305 or the input pad coupled to node 310 by input pad selector 301. A second of the column address strobe inputs is selected from either the input pad coupled to node 305 or the input pad coupled to node 315 by input pad selector 301. In accordance with the present invention, the unused input pad(s) are pulled to a selected power supply voltage to avoid problems associated with "floating" input pads.

To configure IC 101 as a by-8 device, the input pad coupled to node 305 is bonded to the CAS input pin of

the industry standard package (e.g., a 28-pin SOJ package). The mode select input is bonded to indicate a by-8 configuration causing pad input select circuit 301 to select the input pad coupled to node 305 as both the LCAS' and UCAS' outputs. Hence, when configured as a by-8 device, both CAS inputs to control signal generator 302 come from the single CAS provided by the industry standard by-8 package.

To configure IC 101 as a by-16 device, the input pad coupled to node 310 is coupled to X16 LCAS and the input pad coupled to node 315 is coupled to X16 UCAS. The mode select input is bonded to indicate a by-16 configuration causing pad input select circuit 301 to select the input pad coupled to node 310 as the LCAS' output and the input pad coupled to node 315 as the UCAS' output. Hence, when configured as a by-16 device, the CAS inputs to control signal generator 302 come from the dual CAS pins provided by the industry standard by-16 package (e.g., a 40 pin SOJ package).

Pad input select circuit 301 also generates active-low upper and lower output enable signals OE' (L) and OE' (U) coupled to output control circuit 316. In a conventional by-16 design, two output enable signals are used to independently enable data output buffers 312 and 314.

In this manner, pad input select circuit 301 in accordance with the present invention enables the remainder of the circuitry shown in FIG. 3 to be substantially identical to a conventional by-16 memory device. Pad input select circuit 301 generates the expected signals for a by-16 device so that downstream circuitry that is responsive to pad inputs need not be modified in order to function properly as either a by-8 or a by-16 configured memory circuit. Timing and control signal generator 302 generates required timing signals to row address buffer 303 and column address buffer 304 to load address information A0-A9. For a by-8 device, all of A0-A9 are used, whereas for a by-16 device, A0-A8 are used. Invention does not impact or change column and row address method.

Row address buffer 303 and column address buffer 304 couple to row decoder 306 and column decoder 307 respectively in a conventional manner. Row decoder 306 outputs row select signals to memory cell array 309 and column decoder 307 outputs column select signals to sense amplifier array 308 in a conventional manner. Sense amplifier array 308 drives column lines within memory cell array 309 in a conventional manner. Together, row decoder 306, column decoder 307, and sense amplifier array 308 select a desired address space within memory cell array 309 for read and write operations. Data is coupled through sense amplifier array 308 from data in and data out buffers 311, 312, 313 and 314 in a conventional manner. U.S. Pat. No. 5,373,470 describes several circuits suitable for implementation of data I/O circuits buffers 311-314 that are capable of configurably steering data signals to/from appropriate output pins in either a by-8 or by-16 configuration.

FIG. 4 shows in block diagram form a first portion of pad input select circuit 301 in accordance with the present invention. FIG. 4 represents a receiver portion of the input pad select circuit 301 while FIG. 5 represents a buffer and output driver portion of input pad select circuit 301. It should be understood that FIG. 4 and FIG. 5 show a general implementation in accordance with the present invention while FIG. 6 shows a specific implementation useful in the memory circuit shown in FIG. 3.

In FIG. 4, a mode select signal such as the CONFIG signal shown in FIG. 3 is applied to inverter 401 to generate an inverted mode select signal on the MODE A SELECT line. The mode select signal is coupled directly to the MODE B SELECT line. In the examples herein, each device has two configurable modes that can be adequately identified by a single bit binary mode select signal and the complementary MODE A SELECT and MODE B SELECT lines. Where the modes are complementary, the only combinatorial logic required can be supplied by inverter 401. The present invention is also useful to select one input pad from among three or more input pads, however. In these cases, more complex combinatorial logic could be used in place of inverter 401 to generate multiple MODE SELECT signals such that only one input pad is selected.

Pad A is coupled to a source/drain terminal of pull-down transistor 403. In the preferred embodiment, pull-down transistor 403 comprises an n-channel transistor having a second source/drain terminal coupled to a logic level voltage supplied by V.sub.ss or ground. The gate of transistor 403 is controlled by the mode select signal such that when the mode select signal is a logic high, transistor 403 is activated, and input pad A as well as the PADA signal are pulled to logic low or ground. In this manner when the mode select signal is bonded to the V.sub.cc power supply, input pad A is disabled and pulled to a logic low. When the mode select signal is bonded to the ground or V.sub.ss power supply, transistor 403 is off and the PADA signal is passed from the input pad A to the circuitry shown in FIG. 5. This feature of the present invention ensures that the unselected input pad is tied to a fixed power supply voltage and not left floating.

As shown in FIG. 4, it is preferable that pull-down device 403 is implemented as an N-channel transistor such that the unselected input pad is pulled to ground. Alternatively, pull-down transistor 403 could be replaced by a p-channel pull-up transistor (not shown) to pull the unselected pad to a logic high (i.e., V.sub.cc). However, in a CMOS circuit built on a charge pumped p-type substrate, p-channel source/drain nodes form one terminal of a parasitic four layer PNPN structure that has a greater tendency to latch up than does the source/drain of an n-channel device built in the same circuit. It is recommended that input pads, which are more likely to experience transients than internal circuitry, be coupled directly to only N-channel device S/D to avoid latch up. However, in some applications p-channel pull-up devices may be adequate in which case they are equivalent to the preferred embodiment disclosed herein.

Preferably, input pad select circuit 301 also includes power gating circuitry to generate an active-low BUFFER A ENABLE control signal used by the circuitry shown in FIG. 5. Transmission gate 404 is responsive to the MODE B SELECT signal and the MODE A SELECT signal to pass the power gate signal when the MODE SELECT signal is a logic high and block the power gate signal when the MODE SELECT signal is a logic low. Also, transistor 405 is coupled to the MODE A SELECT signal to such that while the MODE B SELECT signal is a logic low (i.e., the MODE SELECT signal is a logic high) transistor 405 is on and the BUFFER A ENABLE is tied to the V.sub.cc power supply.

This configuration places the BUFFER A ENABLE signal in a permanently disabled state when the MODE SELECT signal is a logic high. Also, this configuration places the BUFFER A ENABLE under control of the power gate signal when the MODE SELECT signal is a logic low.

The receiver circuitry coupled to pad B at node 412 is substantially identical to the circuitry described above with respect to pad A at node 402. However, a gate of pull down device 413 is controlled by the BUFFER A ENABLE line to pull pad B to the logic low voltage while mode A is selected. Transmission gate 414 passes the power gate signal to the active-low buffer B enable line (BUFFER B ENABLE) while mode B is high, and transistor 415 is off while the MODE B SELECT signal is a logic high. In a complementary fashion, transmission gate 414 blocks the power gate signal and transistor 415 pulls the BUFFER B ENABLE signal to a logic high (i.e., disabled) while mode A is selected.

Pad input select circuit 301 can be configured to select from any desired number of input pads by duplicating the pull-down device 403, 413, transmission gate 404, 414 and transistor 405, 415 as well as providing multiple MODE SELECT signals to independently control each pad under control of the pad input select signal.

Referring to FIG. 5, the PADA, BUFFER A ENABLE, and MODE A SELECT lines are coupled to a buffer/output portion of input pad select circuit 301. Similarly, the PADB, BUFFER B ENABLE, and MODE B SELECT lines are coupled to the buffer/output portion of input pad select circuit 301. Transistors 501 and 502 form a buffer for the PADA signal. One source/drain of p-channel transistor 501 is coupled to V.sub.cc and the gate of transistor 501 is coupled to the PADA signal. The output of transistor

501 is provided on the second source/drain terminal of transistor 501. Transistor 502 is preferably an N-channel transistor having a first source/drain terminal coupled to ground or V.sub.ss and a second source/drain terminal coupled to output node 510. Node 510 is an output node of input pad select circuit 301 and is coupled to internal circuitry of IC 101.

The BUFFER A ENABLE line is coupled to control the gates of p-channel transistor 503 and n-channel transistor 504. When the BUFFER A ENABLE line is a logic high, transistor 503 is off creating a high impedance between the output node of transistor 501 and output node 510. As set out hereinbefore, the BUFFER A ENABLE signal is pulled to a logic high when MODE A SELECT is a logic low. Also, the PADA signal is pulled to a logic low by pull-down device 403 shown in FIG. 4 when the MODE A SELECT signal is a logic low. The logic low PADA signal turns off transistor 502. Hence, when the MODE A SELECT signal is a logic low all of the transistors coupled directly to output node 510 from pad A are off. This minimizes the parasitic capacitance presented by the pad A buffer circuit (i.e., transistors 501-505) while pad A is unselected.

When the MODE A SELECT signal is a logic high, transistor 505 is on and the PADA signal follows the signal on input pad A shown in FIG. 4. Also, when the MODE A SELECT signal is high the BUFFER A ENABLE signal follows the power gate signal shown in FIG. 4. In the case that the BUFFER A ENABLE is a logic high, transistor 504 place pulls output node 510 low through transistor 505. In the case that the BUFFER A ENABLE is a logic low, transistor 503 couples the output of transistor 501 to output node 510, hence, node 510 is under the control of input pad A shown in FIG. 4.

In a similar manner, transistors 511, 512, 513, 514, and 515 selectively couple the PADB signal to output node 510 while MODE B SELECT is high and BUFFER B ENABLE is low. While MODE B SELECT is low, all transistors directly coupled to node 510 in the B buffer are off and in a high impedance state to avoid loading node 510. Any number of output buffer/driver circuits such as shown in FIG. 5 can be used for each input pad under control of input pad selector circuit 301 so long as only one is selected.

FIG. 6 illustrates a portion of particular embodiment of the present invention in a input pad select circuit 301 shown in FIG. 3. The circuit portion shown in FIG. 6 is used to select either the by-8 CAS or the by-16 LCAS for output to the modified LCAS' signal to timing and control signal generator 302. The circuit portion shown in FIG. 6 is substantially duplicated to enable selection of either the by-8 CAS or the by-16 UCAS to generate the modified UCAS') to timing and control signal generator 302 as shown in FIG. 3.

While the by-8 SELECT line is high, the by-16 SELECT line is low. Hence, when the by-8 SELECT line is high, the by-16 LCAS pad is pulled low as described hereinbefore. Transistors 612, 613, and 615 are turned off to prevent loading of node 610 while the by-16 SELECT line is low. In contrast, transistor 605 is on, and transistor 603 is turned on under control of the by-8 CAS BUFFER ENABLE signal. The by-8 CAS BUFFER ENABLE signal is under control of a power gating signal, if used.

While the by-8 SELECT line is high, transistors 601 and 602 that make up the by-8 input buffer are responsive to a signal on the input pad designated to receive the active-low by-8 CAS signal. The signal at node 610 is thus controlled by the by-8 CAS signal when by-8 CAS BUFFER ENABLE is low, and is pulled to a logic low by transistor 604 when the by-8 CAS BUFFER ENABLE is high. In the particular implementation shown in FIG. 6, node 610 is the inverse of the signal on the selected input pad because transistors 601 and 602 form an inverting buffer.

While the by-8 SELECT line is low, the by-16 SELECT line is high. Hence, when the by-16 SELECT line is high, the active-low by-16 LCAS pad is pulled low as described hereinbefore. Transistors 602, 603, and 605 are turned off to prevent loading of node 610 while the by-8 SELECT line is low. In contrast, transistor 615 is on, and transistor 613 is turned on under control of the by-16 CAS BUFFER ENABLE
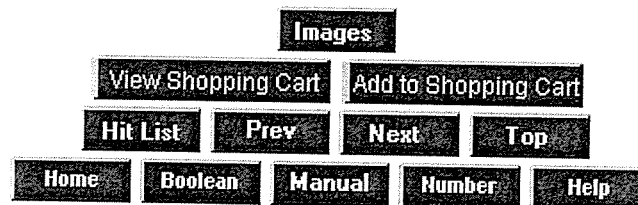
signal. The by-16 CAS BUFFER ENABLE signal is under control of the power gating signal, if used.

While the by-16 SELECT line is high, transistors 611 and 612 that make up the by-16 input buffer are responsive to a signal on the input pad designated to receive the active-low by-16 CAS signal. The signal at node 610 is thus controlled by the by-16 CAS signal when the by-16 CAS BUFFER ENABLE is low, and is low by transistor 614 when the by-16 CAS BUFFER ENABLE is high. In the particular implementation shown in FIG. 6, node 610 is the inverse of the signal on the selected input pad because transistors 611 and 612 form an inverting buffer.

Signal conditioning circuitry 620 affects the delay and edge characteristics of the output UCAS' signal in a conventional manner and can be implemented in any manner appropriate for a particular application. The modified output enable signal OE' (L) is generated by NOR gate 621 having a first node coupled to node 610 and a second node coupled to receive the active-high output enable signal (OE) from an output enable buffer (not shown). The OE signal is supplied to IC 101 through and external pin in the industry standard package for either an by-8 or by-16 configuration.

Although the invention has been described and illustrated with a certain degree of particularity, it is understood that the present disclosure has been made only by way of example. Numerous changes in the combination and arrangement of parts can be resorted to by those skilled in the art without departing from the spirit and scope of the invention, as hereinafter claimed. For example, the present invention is useful in any semiconductor device for which the input signals to a particular path change or are selected based on the devices configuration mode or bond option. Accordingly, these and other are equivalent to the embodiments specifically disclosed herein.

\* \* \* \* \*

# US PATENT & TRADEMARK OFFICE
## PATENT FULL TEXT AND IMAGE DATABASE
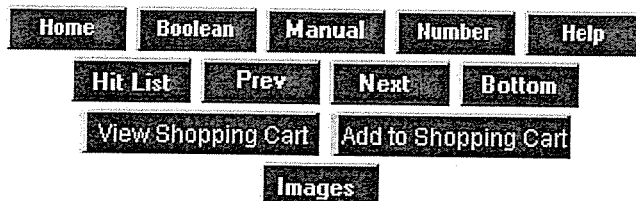
| Home | Boolean | Manual | Number | Help |

| Hit List | Prev | Next | Bottom |

| View Shopping Cart | Add to Shopping Cart |

| Images |

| United States Patent | 5,360,992 |
| Lowrey, et al. | November 1, 1994 |

# Two piece assembly for the selection of pinouts and *bond options* on a semiconductor device

## Abstract

The invention comprises a semiconductor package which allows pinouts and *bond options* to be customized after the encasement of a die in plastic, ceramic, or other suitable materials. A first embodiment of the invention has a first assembly comprising an encapsulated die having bond pads connected to bond wires which terminate in exterior pad portions on the exterior of the encapsulant. Conductive paths which are part of a second assembly electrically connect with the exterior pad portions of the first assembly and pass signals to device pinouts, which can be leads or other connecting means, to an electronic device into which the module is installed. By selectively connecting the exterior pad portions of the first assembly to the connection points of the conductive paths of the second assembly, the device pinouts and *bond options* can be selected. To manufacture a device having different pinouts or *bond options,* a bottom section having a different design is used.

Inventors: **Lowrey; Tyler A.** (Boise, ID); **Reinberg; Alan R.** (Westport, CT); **Martin; Kevin D.** (Boise, ID)

Assignee: **Micron Technology, Inc.** (Boise, ID)

Appl. No.: **221974**

Filed: **April 1, 1994**

| Current U.S. Class: | 257/666; 257/692; 257/698 |
| Intern'l Class: | H01L 023/48; H01L 029/44; H01L 029/52; H01L 029/60 |
| Field of Search: | 257/691,698,692,693,690,666 |

## References Cited [Referenced By]

## U.S. Patent Documents

| | | | |
|---|---|---|---|
| 3663868 | May., 1972 | Noguchi et al. | 257/698. |
| 4901136 | Feb., 1990 | Neugebauer et al. | 257/691. |
| 4922324 | May., 1990 | Sudo | 257/698. |
| 5045921 | Sep., 1991 | Lin et al. | 257/698. |
| 5302849 | Apr., 1994 | Covasin | 257/676. |

## Other References

"Z-Axis Conductive Adhesive" Zymet Inc., 7 Great Meadow Lane, E. Hanover, N.J. 07936.

*Primary Examiner:* James; Andrew J.
*Assistant Examiner:* Clark; S. V.
*Attorney, Agent or Firm:* Martin; Kevin D.

## *Parent Case Text*

## CROSS REFERENCE TO RELATED APPLICATION

This is a continuation of application Ser. No. 07/811,768, filed Dec. 20, 1991, now abandoned.

## *Claims*

We claim:

1. A semiconductor device, comprising:

a) a first assembly comprising:

i) a wafer section with bond pads for the passage of signals therethrough;

ii) a first assembly frame supporting said wafer section, said first assembly frame having conductive pads;

iii) means for electrically connecting said bond pads with said first frame assembly;

wherein said wafer section, said means for electrically connecting, and a portion of said first assembly frame are hermetically sealed within a protective encasement, said conductive pads having portions exterior to said encasement, wherein said first assembly frame is electrically connected to said exterior pad portions;

b) a second assembly comprising a second assembly frame, said second assembly frame comprising:

i) outputs for connecting with an electronic device into which said semiconductor device is installed;

FIG.2

**Applicant:** Cathal G. Phelan
**Serial No.:**
**Filing Date:** Herewith
**For:** FIXED BURST MEMORIES
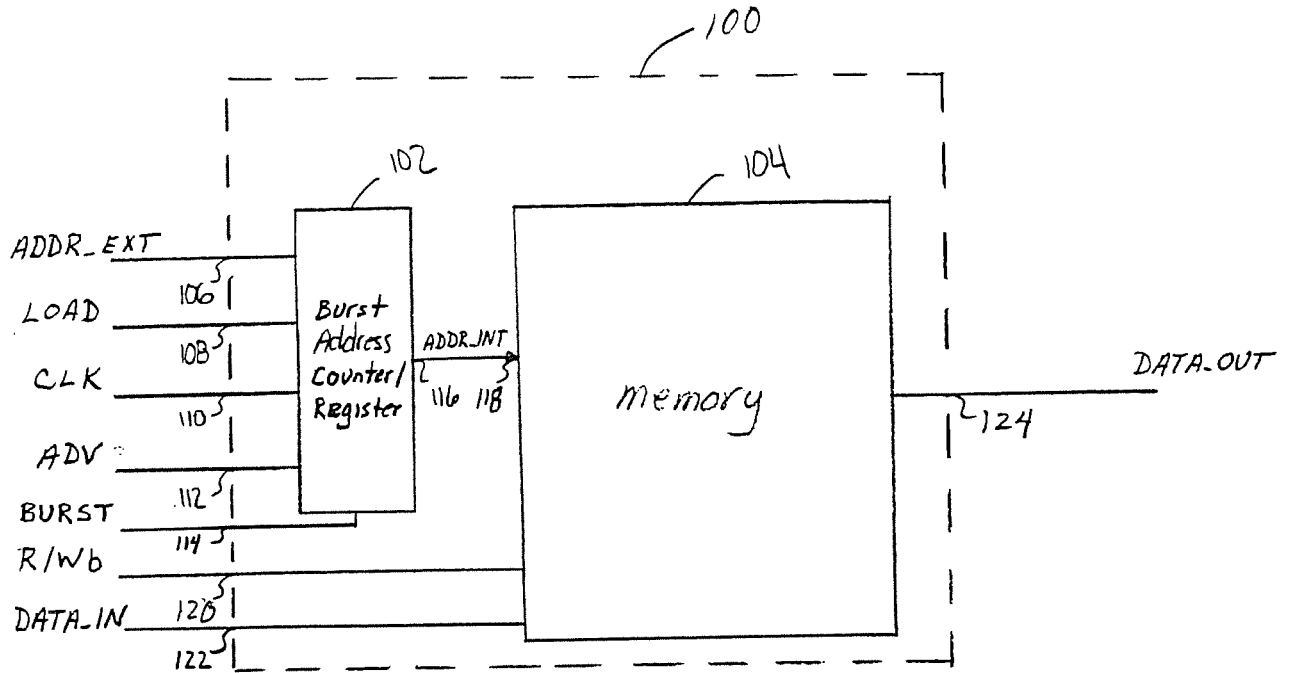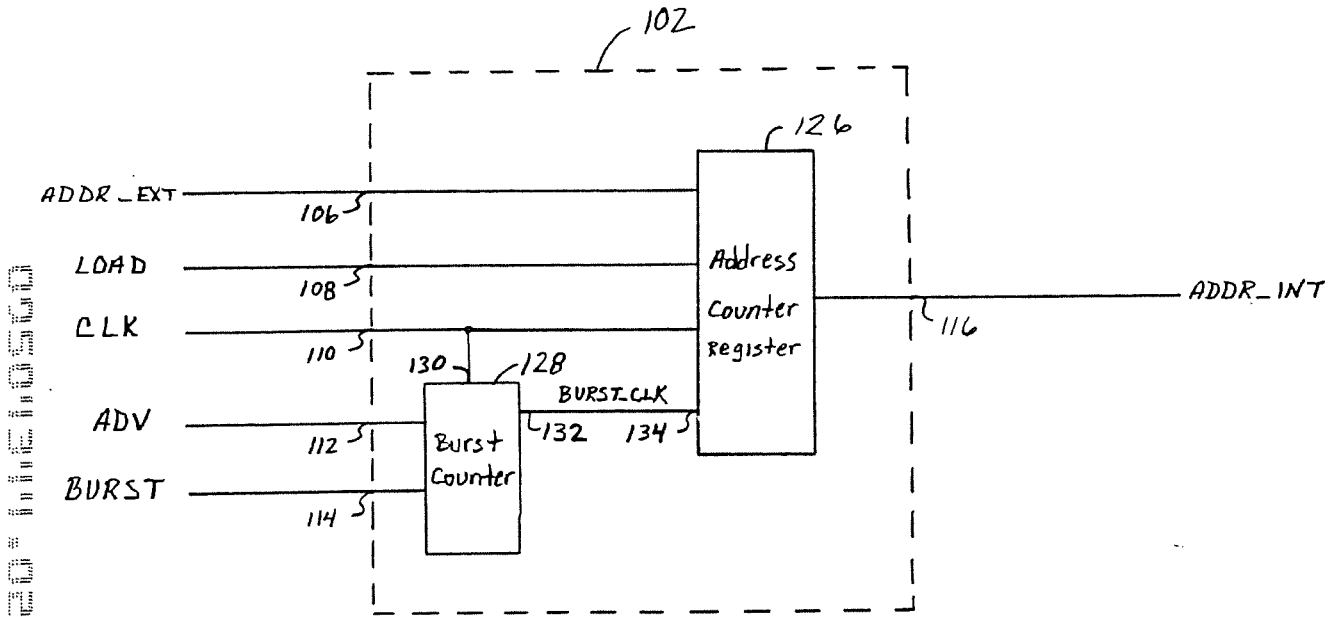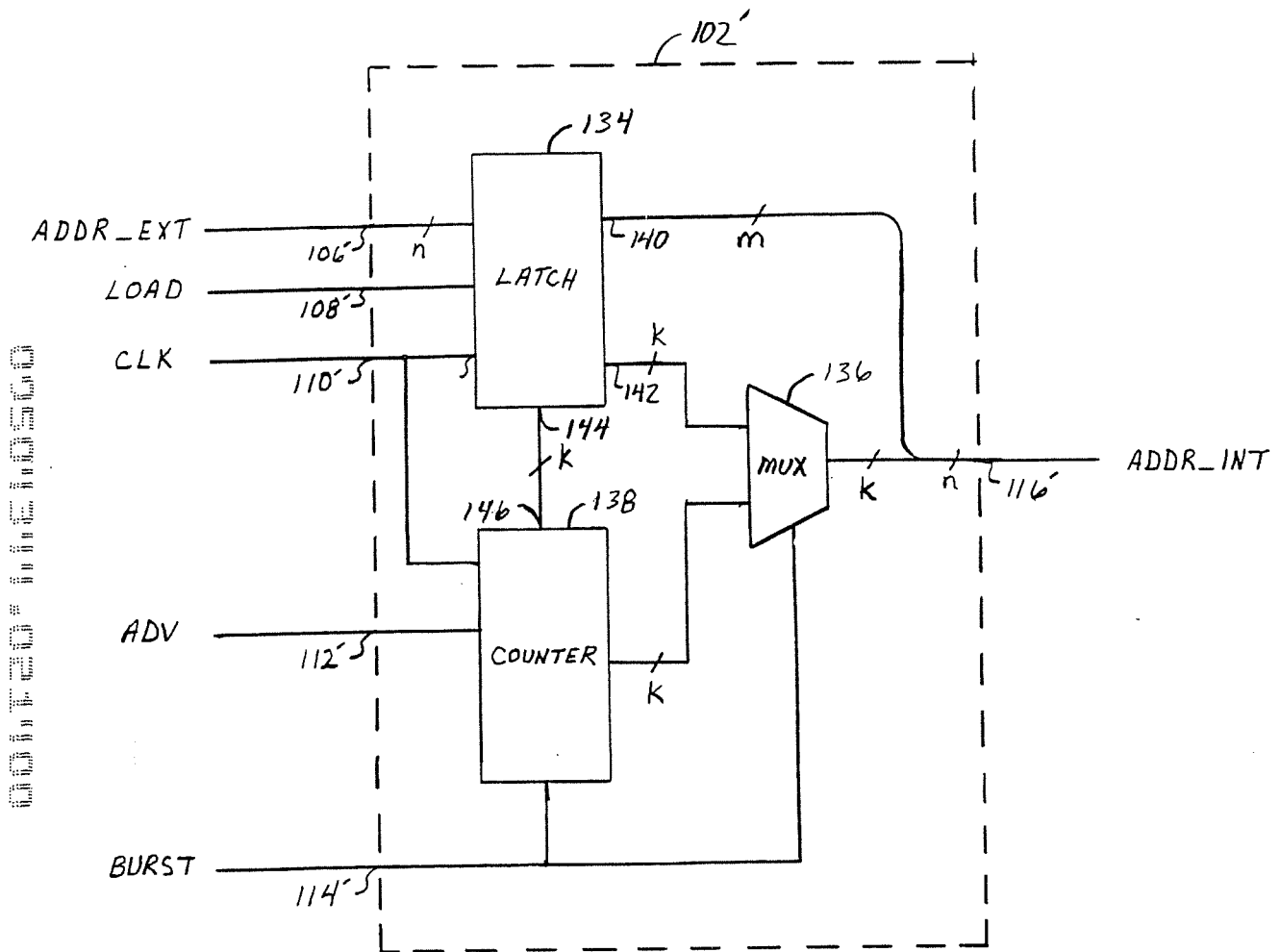**Attorney:** CPM
**Attorney Docket No:** 0325.00309

Sheet 2 of 5

FIG.3

**Applicant:**          Cathal G. Phelan
**Serial No.:**
**Filing Date:**        Herewith
**For:**                FIXED BURST MEMORIES
**Attorney:**           CPM
**Attorney Docket No:**   0325.00309

Sheet 3 of 5
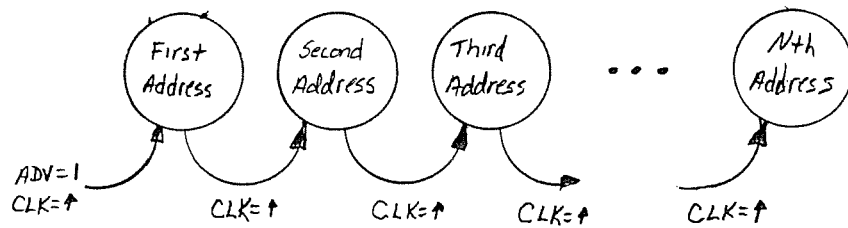
FIG. 4

**Applicant:** Cathal G. Phelan
**Serial No.:**
**Filing Date:** Herewith
**For:** FIXED BURST MEMORIES
**Attorney:** CPM
**Attorney Docket No:** 0325.00309

Sheet 4 of 5
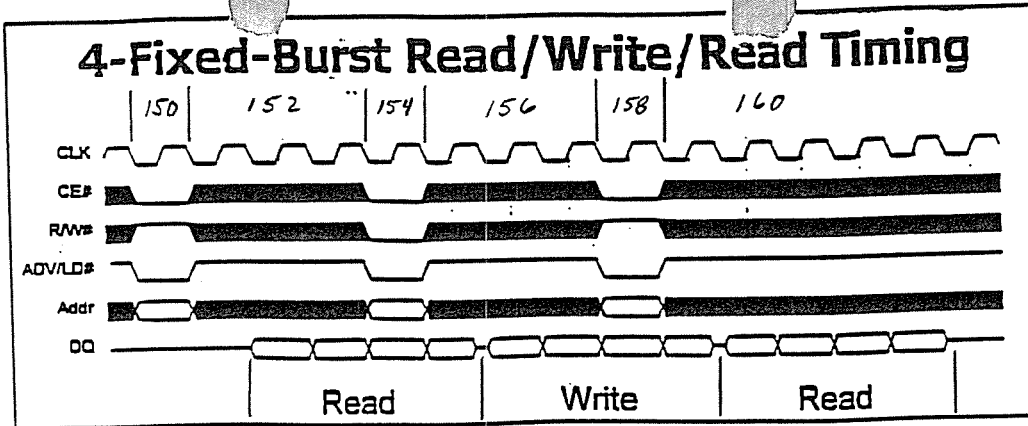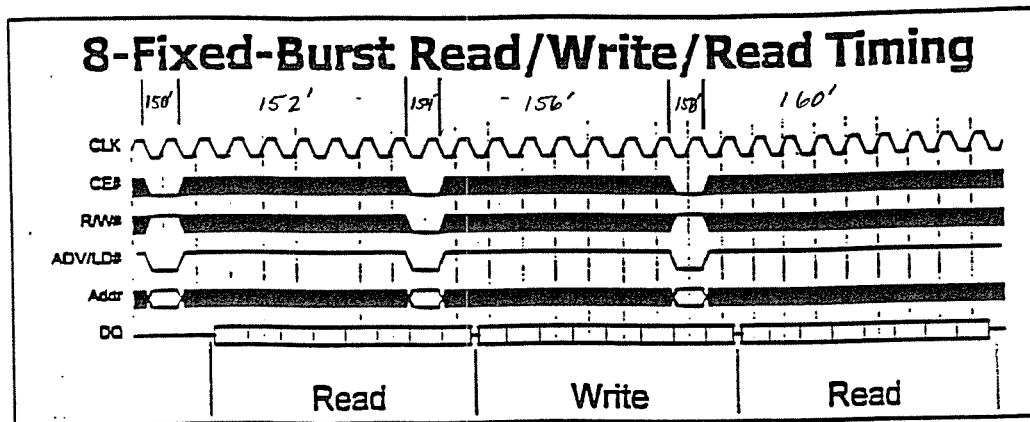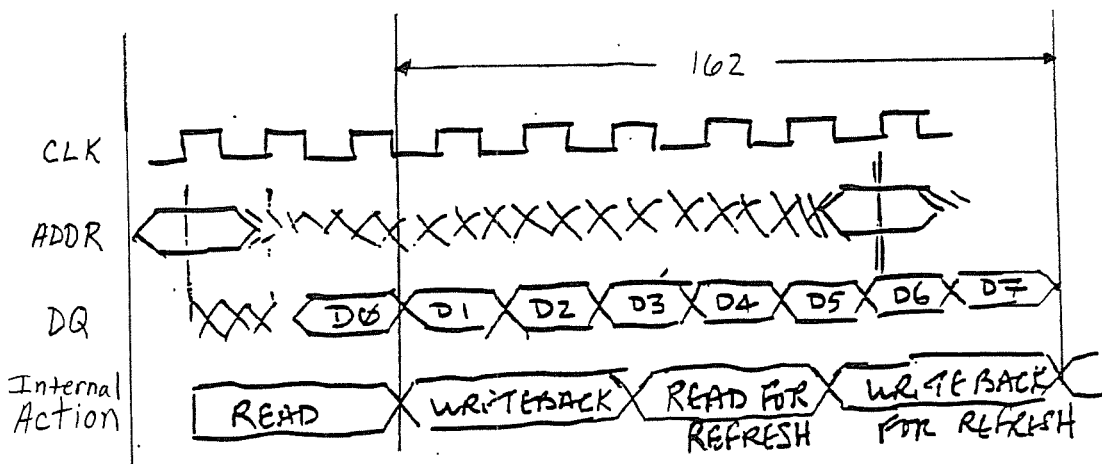
## 4-Fixed-Burst Read/Write/Read Timing

|150| 152 |154| 156 |158| 160

CLK
CE#
R/W#
ADV/LD#
Addr
DQ

| Read | Write | Read |

FIG. 5A

## 8-Fixed-Burst Read/Write/Read Timing

|150'| 152' |154| 156' |158| 160'

CLK
CE#
R/W#
ADV/LD#
Addr
DQ

| Read | Write | Read |

FIG. 5B

162

CLK

ADDR

DQ       D0 X D1 X D2 X D3 X D4 X D5 X D6 X D7

Internal
Action | READ X WRITEBACK X READ FOR X WRITE BACK
                              REFRESH  FOR REFRESH

FIG. 6

Applicant: Cathal G. Phelan
Serial No.:
Filing Date: Herewith
For: FIXED BURST MEMORIES
Attorney: CPM
Attorney Docket No: 0325.00309

Sheet 5 of 5

FIG. 1

FIG.2

FIG.3

First Address — Second Address — Third Address — ... — Nth Address

ADV=1
CLK=↑     CLK=↑     CLK=↑     CLK=↑     CLK=↑

FIG. 4

## 4-Fixed-Burst Read/Write/Read Timing

CLK

CE#

R/W#

ADV/LD#

Addr

DQ

| Read | Write | Read |

## FIG. 5A

## 8-Fixed-Burst Read/Write/Read Timing

CLK

CE#

R/W#

ADV/LD#

Addr

DQ

| Read | Write | Read |

## FIG. 5B

CLK

ADDR

DQ

Internal Action

| READ | WRITEBACK | READ FOR REFRESH | WRITE BACK FOR REFRESH |
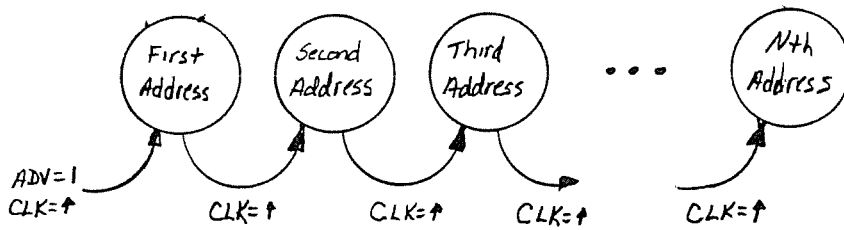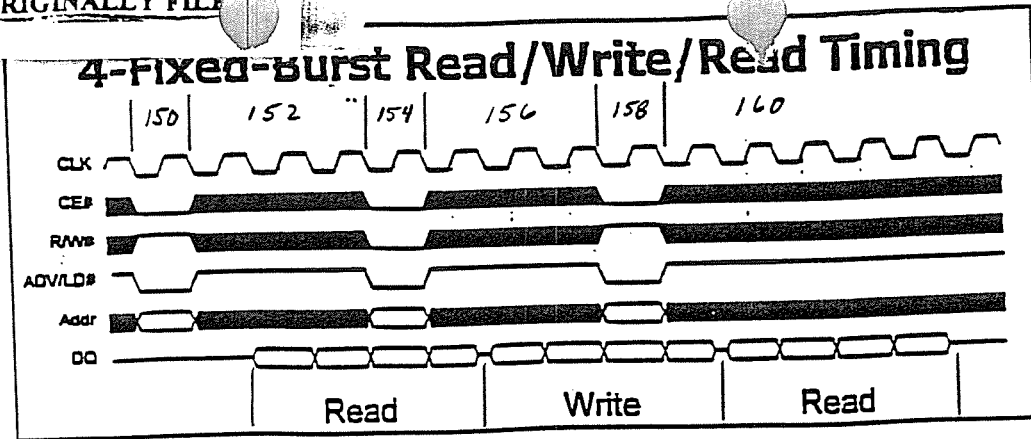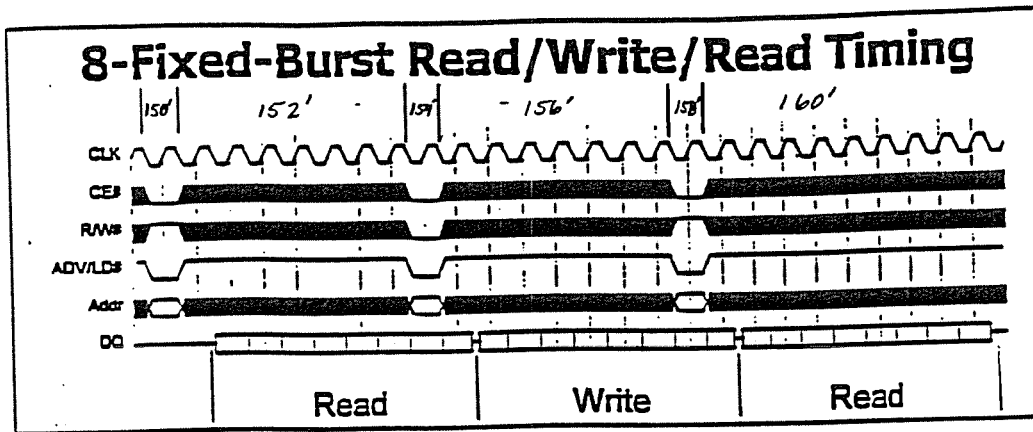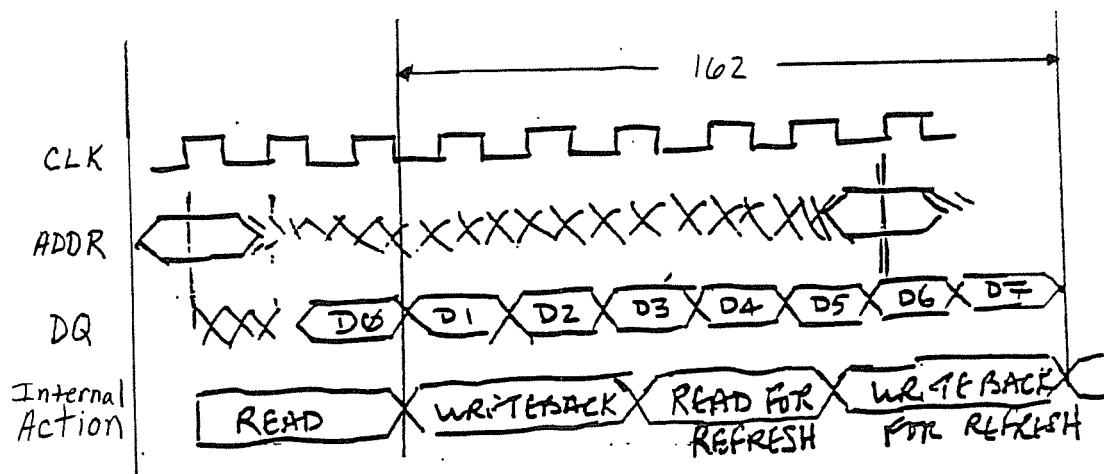
## FIG. 6

$GP2802\#2$

Attorney's Docket No. <u>0325.00309</u>

PATENT

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:    Cathal G. Phelan
Serial No.:              09/504,344                   Art Unit:      2824
Filed:                   February 14, 2000            Examiner:
For:                     FIXED BURST MEMORIES

**Assistant Commissioner For Patents**
**Washington, D.C. 20231**

## TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT
## WITHIN THREE MONTHS OF FILING OR
## BEFORE MAILING OF FIRST OFFICE ACTION (37 CFR 1.97(b))

NOTE:  "An information disclosure statement shall be considered by the Office if filed: (1) within three
months of the filing date of a national application; (2) within three months of the date of entry of the
national stage as set forth in § 1.491 in an international application; or (3) before the mailing date of a
first Office action on the merits, whichever event occurs last." 37 CFR 1.97(b).

---

## IDENTIFICATION OF TIME OF FILING THE ACCOMPANYING
## INFORMATION DISCLOSURE STATEMENT

The information disclosure statement submitted herewith is being filed within three months of the filing date
of the application or date of entry into the national stage of an international application before the mailing date of a first
Office action on the merits, whichever event occurs last. 37 CFR 1.97(b).

CHRISTOPHER P. MAIORANA, P.C.

_____
Christopher P. Maiorana
Registration No. 42,829
24025 Greater Mack, Suite 200
St. Clair Shores, MI 48080
(810) 498-0670
Dated:  <u>May 8, 2000</u>

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United
States Postal Service as first class mail in an envelope addressed to Assistant Commissioner for Patents,
Washington, D.C.  20231, on <u>May 8, 2000</u>.

By: _____
Mary Donna Berkley

| Form PTO-1449   U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE | ATTY DOCKET NO. 0325.00309 | SERIAL NO. 09/504,344 |
|---|---|---|
| INFORMATION DISCLOSURE STATEMENT BY APPLICANT | APPLICANT: Cathal G. Phelan | |
| | FILING DATE February 14, 2000 | GROUP 2824 2187 |

*(OIPE stamp: MAY 1 1 2000 PATENT & TRADEMARK OFFICE)*

## U.S. PATENT DOCUMENTS

| Examiner Initial | Document No. | Date | Name | Class | Sub Class | Filing Date |
|---|---|---|---|---|---|---|
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |

*(stamps: TECH CENTER 2700 / RECEIVED JUN 26 2000)*

## FOREIGN PATENT DOCUMENTS

| | Document No. | Date | Country | Class | Sub-Class | Transl. Yes | Transl. No |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |

## OTHER DOCUMENTS (Incl. Author, Title, Date, Pertinent Pages, etc.)

| | |
|---|---|
| ∧∨∼∨ | Understanding Burst Modes in Synchronous SRAMs, Cypress Semiconductor Corp., June 30, 1999. |
| | |
| | |

| Examiner | Date Considered  9/25/01 |
|---|---|

Examiner: Initial if references considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

# CYPRESS

# Understanding Burst Modes in Synchronous SRAMs

## Introduction

With the addition of the clock, synchronous SRAMs are able to provide several features that are not possible with asynchronous SRAMs. These include:

- Controlled timings on outputs
- Different write modes (ADSP/ADSC)
- Reading multiple locations using a single address using Burst modes

One of the more useful features of synchronous SRAMs is the burst mode. This application note discusses the different burst modes on synchronous SRAMs.

## What is a Burst Mode?

Synchronous SRAMs are able to provide data from multiple address locations with the association of a single address. The advantage of this operation is that, by providing a single address, data from four locations can be obtained, thereby reducing the activity on the address bus.

*Figure 1* shows the signals associated with the burst feature.
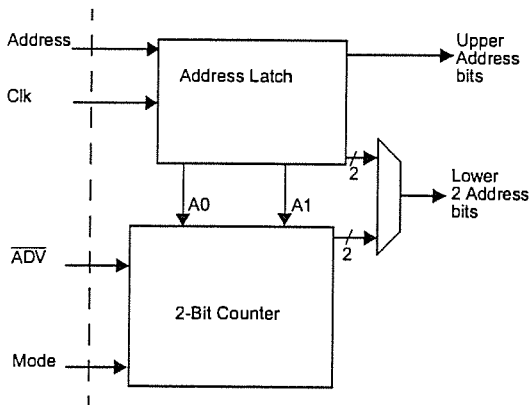


**Figure 1. Key Signals for Burst Feature on Typical SRAMs**

*Table 1* provides the definitions for the signals shown in *Figure 1*.

## Function

On the rising edge of the clock, the address and control pins are latched into the SRAM. All accesses for standard synchronous SRAMs are initiated the same way. Depending on the control signals, a read or write transaction is initiated. On the next rising edge of the clock, the ADV pin is sampled. If ADV is sampled active LOW, a burst access is initiated and the SRAM continues the present operation with an address obtained from the internal counter. The burst continues until

## Table 1. Definition of Signals

| Pin | Definition |
|---|---|
| Address | Address Inputs used to select one of the address locations in the SRAM. Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and CE is sampled active. A[1:0] feed the 2-bit counter. |
| CLK | Clock Input. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW, during a burst operation. |
| ADV | Advance Input signal, sampled on the rising edge of CLK. When asserted, it automatically increments the address in a burst cycle. |
| Mode | Selects burst order. When tied to GND selects linear burst sequence. When tied HIGH or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. |

the advance pin is HIGH, or a new cycle is started. If the ADV is asserted sufficiently, the SRAM will wrap around to the originally accessed address location. This is a result of a 2-bit burst counter that can access four address locations.

The Mode pin controls the order or sequence of the burst. Currently, two popular different burst sequences are available. Both of them are described below.
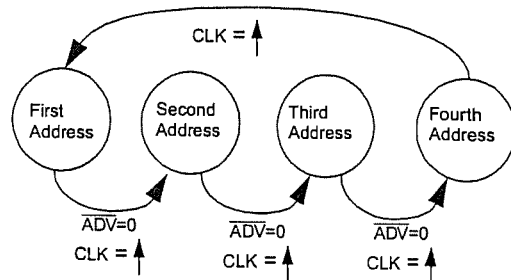


**Figure 2. Burst Mode Address Update**

## Linear Burst

If the Mode pin is tied LOW, the device operates in the linear method of operation. In the Linear Burst mode of operation, the internal counter counts in a linear fashion up from the present value with A1 and A0 being the LSBs. This is shown in the table below.

CYPRESS

|  | Case 1 | | Case 2 | | Case 3 | | Case 4 | |
|---|---|---|---|---|---|---|---|---|
|  | A1 | A0 | A1 | A0 | A1 | A0 | A1 | A0 |
| First Address | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Second Address | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| Third Address | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Fourth Address | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

From an implementation standpoint, this is a simple 2-bit counter.

### Interleaved Burst

If the Mode pin is tied HIGH, the device operates in the interleaved method of operation.

In the Interleaved Burst mode of operation, the internal counter behaves a bit differently. The sequence in the interleaved burst is determined by the first address. The sequence is shown below.

|  | Case 1 | | Case 2 | | Case 3 | | Case 4 | |
|---|---|---|---|---|---|---|---|---|
|  | A1 | A0 | A1 | A0 | A1 | A0 | A1 | A0 |
| First Address | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Second Address | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| Third Address | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Fourth Address | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

From an implementation stand point, this is a 2-bit counter with some added logic as shown in *Figure 3*. The 2-bit counter is reset on every new address cycle and A0/A1 are the bits latched from the start of the cycle. The Interleaved Burst order is especially popular with Intel-based systems.
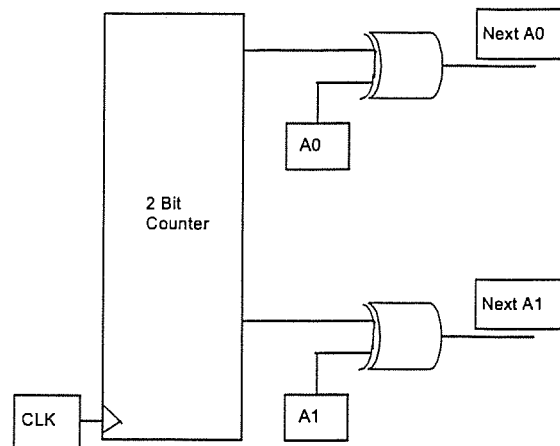


**Figure 3. Implementation to Generate the Interleaved Burst Sequence.**

## Conclusion

In terms of general operation, one method of burst does not have any significant advantages over the other. Different processors support different kinds of bursts. Intel processors support the interleaved burst scheme, while the Power PC microprocessors support the linear burst mode of operation.

Burst Modes in Synchronous SRAMs can be very useful. The advantages are:

- Reduced activity on the address bus (four memory locations accessed with a single address)
- Address generation to the SRAM allowing the controller to perform other functions
- More reliable since the address location is generated inside the SRAM.

ple t    of Application

U.S. DEPARTMENT OF COMMERCI
PATENT & TRADEMARK OFFICI

# APPLICATION TRANSFER REQUEST FOR S.N. _09/504 344_

---

**Section L TRANSFER REQUEST BY** (PRINT NAME) _H. Ho_ Date_____

TO: Art Unit _2752_ Class/sub_711_ From: A.U._2818_ Class_365_

REASON:

_It is not proper for a class 365_
_Burst Mode & write back_

Gatekeeper concurrence_NB for YN_ Hand carried: Personally accepted by _____
_5/15/00_

---

**Section II. DISPOSITION BY RECEIVING TC** A.U._2709_ Date_5/18/00_

[X] ACCEPTED BY RECEIVING T.C.

NOT ACCEPTED ☐ Forward to Post Classifier

☐ Return to Originating Technology Center /AU_____

REASON:

### DISPOSITION BY RECEIVING TC POST CLASSIFIER

☐ This dispute was resolved. Forward to Class/Sub_____ TC/AU_____ Post Classifier_____ Date_____

Concurring_____ Date_____

☐ This dispute was not resolved, forward to DISPUTE RESOLUTION PANEL.
**Post Classifier Assessment:**

Gatekeeper Concurrence _____

---

**Section III. DISPOSITION BY DISPUTE RESOLUTION PANEL** Date_____

**Panel Decision:** Forward to Technology Center / Art Unit_____ Class/sub_____

REASON:

Panel Member _____ Concurring Panel Member _____

☐ This application MAY be returned to the dispute resolution panel if reconsideration is desired (use form 447R).

☐ This application MAY NOT be returned to the dispute resolution panel. THIS IS A FINAL DISPOSITION.

| | Type | L # | Hits | Search Text | DBs | Time Stamp |
|---|------|-----|------|-------------|-----|------------|
| 1 | BRS | L1 | 802 | fix$3 near5 length near5 (interrupt$4 or stop$3 or terminat$4) | USPAT; US-PGPUB; EPO; DERWENT | 2001/09/26 09:49 |
| 2 | BRS | L2 | 11 | 1 and ((internal or external) adj signal) | USPAT; US-PGPUB; EPO; DERWENT | 2001/09/26 09:54 |
| 3 | BRS | L3 | 2 | 6085261.pn. | USPAT; US-PGPUB; EPO; DERWENT | 2001/09/26 10:34 |
| 4 | BRS | L4 | 3 | dell and namazi | USPAT; US-PGPUB; EPO; DERWENT | 2001/09/26 10:42 |

09/26/2001, EAST Version: 1.02.0008

|   | Type | L # | Hits | Search Text | DBs | Time Stamp |
|---|------|-----|------|-------------|-----|------------|
| 5 | BRS | L5 | 2 | 4 and mod$ | USPAT;<br>US-PGPUB;<br>EPO;<br>DERWENT | 2001/09/26<br>10:48 |
| 6 | BRS | L6 | 290 | fix$3 with burst with length | USPAT;<br>US-PGPUB;<br>EPO;<br>DERWENT | 2001/09/26<br>11:02 |

09/26/2001, EAST Version: 1.02.0008

|   | Type | L # | Hits | Search Text | DBs | Time Stamp |
|---|------|-----|------|-------------|-----|------------|
| 7 | BRS | L7 | 8002 | external with address with signal | USPAT; US-PGPUB; EPO; DERWENT | 2001/09/26 10:50 |
| 8 | BRS | L8 | 6655 | internal with address with signal | USPAT; US-PGPUB; EPO; DERWENT | 2001/09/26 10:50 |
| 9 | BRS | L10 | 3 | 8 same 6 | USPAT; US-PGPUB; EPO; DERWENT | 2001/09/26 10:51 |
| 10 | BRS | L9 | 26 | 6 and 7 and 8 | USPAT; US-PGPUB; EPO; DERWENT | 2001/09/26 11:02 |
| 11 | BRS | L12 | 40 | 6.ab. | USPAT; US-PGPUB; EPO; DERWENT | 2001/09/26 11:03 |
| 12 | BRS | L11 | 40 | (fix$3 with burst with length).ab. | USPAT; US-PGPUB; EPO; DERWENT | 2001/09/26 11:35 |
| 13 | BRS | L13 | 84 | 6 and interrupt$5 | USPAT; US-PGPUB; EPO; DERWENT | 2001/09/26 11:36 |
| 14 | BRS | L14 | 0 | 6 and (noninterrupt$5 or "non" adj interuppt$4) | USPAT; US-PGPUB; EPO; DERWENT | 2001/09/26 11:37 |
| 15 | BRS | L15 | 179 | 6 and (interrupt$4 or stop$4 or terminat$4) | USPAT; US-PGPUB; EPO; DERWENT | 2001/09/26 11:38 |

09/26/2001, EAST Version: 1.02.0008

| | Type | L # | Hits | Search Text | DBs | Time Stamp |
|---|------|-----|------|-------------|-----|------------|
| 16 | BRS | L16 | 20 | 15 and 7 and 8 | USPAT; US-PGPUB; EPO; DERWENT | 2001/09/26 12:35 |
| 17 | BRS | L17 | 241 | non-interrupt | USPAT; US-PGPUB; EPO; DERWENT | 2001/09/26 12:36 |
| 18 | BRS | L18 | 0 | 6 and 17 | USPAT; US-PGPUB; EPO; DERWENT | 2001/09/26 12:36 |
| 19 | BRS | L19 | 1545 | non-interrupt$4 | USPAT; US-PGPUB; EPO; DERWENT | 2001/09/26 12:36 |
| 20 | BRS | L20 | 0 | 6 and 17 | USPAT; US-PGPUB; EPO; DERWENT | 2001/09/26 12:36 |
| 21 | BRS | L21 | 0 | 6 and 19 | USPAT; US-PGPUB; EPO; DERWENT | 2001/09/26 12:51 |
| 22 | BRS | L22 | 2903 | burst near10 (terminat$4 or interrupt$5 or stop$4) | USPAT; US-PGPUB; EPO; DERWENT | 2001/09/26 12:57 |
| 23 | BRS | L23 | 365 | 22 and refresh | USPAT; US-PGPUB; EPO; DERWENT | 2001/09/26 12:58 |
| 24 | BRS | L24 | 25 | 23 and (fix$3 adj length) | USPAT; US-PGPUB; EPO; DERWENT | 2001/09/26 12:59 |

09/26/2001, EAST Version: 1.02.0008

ii) a plurality of conductive paths, each of said conductive paths routing one of said signals between one of said external pad portions and one of said outputs,

wherein a design of said conductive paths determines which one of said signals passes through each of said outputs.

2. The semiconductor device of claim 1 wherein said means for electrically connecting said wafer section inputs and outputs with said first frame assembly comprises a bond wire.

3. The semiconductor device of claim 1 wherein said conductive paths are electrically connected to said exterior pad portions with solder.

4. The semiconductor device of claim 1 wherein said conductive paths are electrically connected to said exterior pad portions through a nonconductive sheet having voids therein, said voids receiving a conductive material which connects said exterior pad portions with said conductive paths.

5. The semiconductor device of claim 1 wherein said conductive paths comprise bars for making an electrical connection anywhere along said bars.

6. The semiconductor device of claim 1 further comprising a third assembly interposed between said first assembly and said second assembly, said third assembly comprising traces, each trace having first and second ends with said first end of one of said traces electrically connected to one of said conductive pads, and said second end connected to one of said conductive paths, said conductive path being electrically connected to said conductive pad through said trace.

7. The semiconductor device of claim 1 wherein said protective encasement comprises plastic and wherein a portion of said second assembly is encapsulated in plastic.

8. The semiconductor device of claim 1 wherein said protective encasement comprises ceramic and wherein said second assembly further comprises ceramic to support said conductive paths.

9. The semiconductor device of claim 1 wherein said wafer section is connected to said first assembly frame by flip chip bonding.

10. A semiconductor device, comprising:

a) a first assembly comprising:

i) a wafer section with bond pads for the passage of signals therethrough;

ii) a first assembly frame supporting said wafer section, said first assembly frame having conductive pads;

iii) bond wires electrically connecting said bond pads with said first assembly frame;

wherein said wafer section, said bond wires, and a portion of said first assembly frame are hermetically sealed within a protective encasement, said conductive pads having portions exterior to said encasement, wherein said first assembly frame is electrically connected to said exterior pad portions;

b) a second assembly comprising a second assembly frame, said second assembly frame comprising:

i) outputs for connecting with an electronic device into which said semiconductor device is installed;

ii) a plurality of conductive paths, each of said conductive paths routing one of said signals between one of said exterior pad portions and one of said outputs,

wherein said signals are routed between said exterior pad portions and said outputs by said conductive paths, and a design of said conductive paths determines which one of said signals passes through each of said outputs.

11. The semiconductor device of claim 10 wherein said conductive paths are electrically connected to said exterior pad portions with solder.

12. The semiconductor device of claim 10 wherein said conductive paths are electrically connected to said exterior pad portions through a nonconductive sheet having voids therein, said voids receiving a conductive material which connects said conductive pads with said conductive paths.

13. The semiconductor device of claim 10 wherein said conductive paths comprise bars for making an electrical connection anywhere along said bars.

14. The semiconductor device of claim 10 further comprising a third assembly interposed between said first assembly and said second assembly, said third assembly comprising traces, each trace having first and second ends with said first end of one of said traces electrically connected to one of said exterior pad portions, and said second end connected to one of said conductive paths, said conductive path being electrically connected to said exterior pad portion through said trace.

15. The semiconductor device of claim 10 wherein said protective encasement comprises plastic and wherein a portion of said second assembly is encapsulated in plastic.

16. The semiconductor device of claim 10 wherein said protective encasement comprises ceramic and wherein said second assembly further comprises ceramic to support said conductive paths.

17. A semiconductor memory device, comprising:

a) a first assembly comprising:

i) a semiconductor die with bond pads, said bond pads for the passage of signals therethrough, each of said bond pads having a different signal passing therethrough, said signals comprising *bond options* and addresses;

ii) a first assembly frame supporting said semiconductor die, said first assembly frame having conductive pads;

iii) bond wires electrically connecting said bond pads with said first assembly frame;

wherein said semiconductor die, said bond wires, and a portion of said first assembly frame are hermetically sealed within a protective encasement, said conductive pads having portions exterior to said encasement, wherein said first assembly frame is electrically connected to said exterior pad portions;

b) a second assembly comprising a second assembly frame, said second assembly frame comprising:

i) pinouts for connecting with an electronic device into which said semiconductor device is installed;

10

ii) a plurality of conductive paths, each of said conductive paths routing one of said signals between one of said exterior pad portions and one of said pinouts,

wherein said signals are routed between said outputs and said exterior pad portions by said conductive paths, and a design of said conductive paths determines which one of said signals passes through each of said outputs.

18. The semiconductor device of claim 17 wherein said protective encasement comprises plastic and wherein a portion of said second assembly is encapsulated in plastic.

19. The semiconductor device of claim 17 wherein said protective encasement comprises ceramic and wherein said second assembly further comprises ceramic to support said conductive paths.

20. The semiconductor device of claim 17 wherein said pinouts have signals from only one semiconductor die passing therethrough.

---

## *Description*

---

FIELD OF THE INVENTION

This invention relates to the field of semiconductor packaging. More specifically, several semiconductor package design embodiments are described which allow for various backend- and user-selectable wire bond options and pinouts.

BACKGROUND OF THE INVENTION

Various types of semiconductor devices are manufactured in much the same way. A starting substrate, usually a thin wafer of silicon or gallium arsenide, is masked, etched, and doped through several process steps, the steps depending on the type of semiconductor devices being manufactured. This process yields a number of die on each wafer produced. The die are separated with a wafer saw, and then packaged into individual components.

During the packaging process, several semiconductor die are attached to a lead frame, often with materials such as conductive epoxy, various metals and alloys, or other adhesives. Bond wires electrically connect (i.e. couple, directly or through intermediate paths) a number of bond pads on each die to conductive lead "fingers" on the lead frame. Leads are interposed between the lead fingers and the host into which the device is installed. The die, the wires, and a portion of the leads are encapsulated in plastic. The leads on the lead frame connect the die with the device into which the component is installed, thereby forming an electrical pathway and a means of input/output (I/O) between the die and the host.

The particular lead finger with which a bond pad is connected determines the pinout for that bond pad. For example, in a dynamic random access memory (DRAM) if a bond pad on the die which corresponds to Address 0 (A0) is bonded to the lead finger corresponding to Output Pin 5, then pin 5 on the package is used as A0. This hardwires the bond pad on the die to the output of the lead frame, and remains that way for the life of the package. Once the die is encapsulated, the output pins for the signals required to operate the die cannot be changed.

In addition to providing external access to standard input and output signals, the wire bond step may also be used to select various optional operating features of an integrated circuit (IC) product (such as a

DRAM). In the case of a DRAM IC, device data width may be selected at the wire bond step thereby determining whether the die is written to and read from, for example, 1 or 4 bits at a time. A 4 megabit (Mbit) device, therefore, can be configured as a 4Mbit.times.1 or a 1Mbit.times.4, depending on how the bond pads are wire bonded to the lead frame.

Fast page mode is another option which might be selected at wire bond. Fast page mode allows for two or more successive reads or writes from the same row without requiring another row address strobe (RAS) signal. For example, if RAS is kept low after a read, another cell or plurality of cells in the row can be read by issuing a different address on the address lines and then toggling the column address strobe (CAS), thus executing faster memory access cycles.

Similarly, static column mode might be selected at the wire bond stage. Static column mode is similar to fast page mode, but both RAS and CAS remain low, and a new address is presented to the address lines in order to read from or write to a different address in the row. Various other device modes and options are selected during the wire bond step. Sometimes a bond pad is not connected with an output lead, and the option is not selected.

One problem with selecting options by wire bonding an option into a package is that once the die is encapsulated the package options cannot be changed. Various customers require a different combination of options or a number of different package options. The manufacturer must either assemble the package as the order is placed, or the manufacturer or buyer must keep a stock of each of the various device types. Assembling the devices as they are ordered implies long lead times, while keeping a large stock increases operating costs of the manufacturer or the buyer.

Devices have been designed which allow for the selection of *bond options* after packaging of the die using an electrical in-package late programming technique. To fabricate this type of part, the die is attached to the lead frame and the die is encapsulated in plastic. Circuitry on the die allows the bond option to be electrically selected. Using this technique, however, only options that are compatible with the package pin count in which the part was assembled are selectable.

A package which allows the semiconductor manufacturer or buyer to package a die and configure *bond options* and pin counts as they are required would help solve the problems listed above. Note that even though many of the devices used as examples herein specifically mention die encapsulated in plastic, similar problems and solutions are workable for die housed in ceramic or other package materials.

SUMMARY OF THE INVENTION

One embodiment of the invention comprises the use of an inventive two-piece package. In some embodiments, the addition of a third middle section as described herein may have advantages over the two piece embodiments.

A first assembly comprises a semiconductor die encased in plastic, ceramic, or other suitable material. All available *bond options* (bond pads) are routed to the exterior portion of the package by a first assembly frame. Portions of the first assembly frame are exterior to the encasement and terminate in exterior pad portions which can be conductively bonded to.

A second assembly of the invention comprises a second assembly frame which provides a means of input/output (I/O) between the die and the host into which it is installed. The second assembly frame comprises conductive paths to which the exterior pad portions are connected, the first assembly being conductively mounted to the second assembly thereby. With the two-piece embodiment of the invention, the frame of the second assembly determines the pinouts (the pin numbers associated with each of the

signals of the device) of the various signals of the die contained within the first assembly.

An optional third assembly, which, if used, is interposed between the first and second assemblies, comprises means for "keying" the exterior pad portions to desired locations on the second assembly frame. The third assembly can comprise at least two different embodiments.

In a first embodiment, the third assembly is a nonconductive membrane having voids therethrough. The conductive paths of the second assembly are located in an "X" direction, while the exterior pad portions of the first assembly of this embodiment are bars extending in a "Y" direction. By selectively placing the voids in the membrane, the pads of the first assembly can either be connected with the conductive paths of the second assembly, or isolated from the conductive paths if no void is formed. Using said X-Y arrangement, any of the *bond options* can be connected with any of the pinouts. Connecting is accomplished by coating the bars with a conductive material and interposing the insulative membrane between the first and second assemblies. The conductive material fills the voids, thereby passing signals between the first and second assemblies.

In a second embodiment, the third assembly comprises a flex circuit as used with tape automated bonding. The second assembly has a single design, and the layout of the flex circuit determines the pinouts and options of the semiconductor device. The flex circuit is conductively mounted to the first and second assemblies in a fashion consistent with tape automated bonding (TAB) technology, for instance with solder, or by some other means such as the Z-axis conductive epoxy described below. This nonmetallic material is conductive in a Z direction (vertically), but is substantially nonconductive in an X-Y direction (horizontally).

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is an isometric view, and 1B is a cross section, showing a die mounted and wire bonded to a first assembly frame as used with the inventive device, which is then hermetically sealed in an encasement;

FIG. 2A is an exploded view of a two piece embodiment of the invention which has a first assembly directly connected with the second assembly with solder or other workable means;

FIG. 2B shows the embodiment of 2A with the second assembly supported by a nonconductive material such as plastic or ceramic;

FIG. 3 is an exploded view (inverted from the view of FIGS. 1 and 2 to show detail of the first assembly) of a three piece embodiment of the invention having a thin insulative membrane with voids therein to receive a conductive material which electrically connects the first and second assemblies;

FIG. 4 is an isometric view of the die-first assembly frame assembly of FIG. 3 before encapsulation;

FIG. 5 is an isometric view of an alternate method of forming the first assembly of FIG. 3; and

FIG. 6 is an exploded view of a three piece embodiment of the invention having a flex circuit interposed between the first and second assemblies which routes the signals from the first assembly to the appropriate conductive paths on the second assembly.

## DETAILED DESCRIPTION OF THE INVENTION

The invention comprises at least two assemblies. FIGS. 1A and 1B show one embodiment of a first assembly, generally described as element 8. In this embodiment of a die-first assembly frame attachment,

the die 10 is supported by a die paddle 12. The paddle 12 is connected to the frame 14 by a tie bar 16 as is known in the art. Bond pads 18 on the die 10 are wire bonded 20 to lead fingers 22 of the lead frame 14. Other embodiments having a die flip-chip mounted to the lead frame may provide advantages. In any case, the lead fingers 22 terminate in exterior conductive pads 24 which are exterior to the first assembly 8. The pads 24 in the embodiments shown herein are flush with the exterior of the package (element 26 in FIG. 1B), although other embodiments are possible. For example, the lead fingers 22 could terminate in J-leads, or other types of leads to form the exterior pads.

A ceramic embodiment of this first assembly is possible and would serve a similar function, the bond pads on the die being connected by bond wires to traces running through the ceramic body, and terminating in pads or leads on the exterior of the first assembly. In the ceramic embodiment, a lid would be required to hermetically seal the die in the ceramic body as is presently known in the art of semiconductor technology.

In various embodiments of the invention, more than one bond pad may connect with a single exterior pad, or more than one exterior pad can connect with a single bond pad. More often, however, one bond pad will connect with a single lead finger, which will terminate in a single pad on the exterior of the package. These exterior pads allow for an electrical signal to pass between the die and a second assembly described below. On a DRAM, these signals could comprise addresses, power, ground, and *bond options* such as data width and other device modes (page mode, fast page mode, write-per-bit, etc.). Other signals are possible and likely on other types of semiconductor devices such as static RAMs (SRAMS), microprocessors, and other logic and memory.

An embodiment of a second assembly of the invention, generally labeled as element 29 as shown in FIG. 2A comprises a second assembly frame 30 which would most often be manufactured from a conductive material such as a copper alloy. A ceramic, plastic, or other nonconductive material 32 can be added to the second assembly to support the elongated conductive paths 34, as shown in FIG. 2B, and prevent them from bending or shorting together. The paths 34 connect with the exterior pads 24 of the first assembly. As this second assembly is manufactured from a conductive material, connecting with the first assembly can occur at any point along a path 34. The paths 34 of the second assembly are connected with (or are formed into) outputs 36 which will connect with an electronic host into which the inventive device is installed. Connection of the exterior pads 24 of the first assembly and the paths 34 of the second assembly are accomplished by any workable means, such as by reflowing solder bumps formed on the exterior pads 24 of the first assembly or by using a conductive adhesive such as a Z-Axis Conductive Adhesive available from Zymet of E. Hanover, N.J. In any case, the paths 34 are routed between the exterior pads 24 of the first assembly to avoid undesired contact with other paths. With this two-piece embodiment, if an exterior pad 24 comprises a bond option which is not desired, a path 34 will not be located below it, and therefore it will not make contact therewith; since the exterior pad 24 is not connected with a path 34, this bond option would not be selected. Also, selection of a pinout for a particular signal is accomplished simply by connecting a pad 24 of the first assembly with the path 34 of the second assembly corresponding to that pinout. To move the signal to a different pinout, (a different output) a different second assembly is substituted. After the first and second assemblies are connected, the tie bars 38 of the lower assembly are trimmed to isolate each of the outputs 36. The outputs 36 are then formed into a desired configuration, such as zigzag inline (ZIP), dual inline (DIP), gull wing, or other lead types. FIGS. 2a and 2b show a complete second assembly frame before a trim and form step. In either case, the unnecessary metal of the second assembly frame is trimmed away to disconnect each of the outputs 36, and the outputs 36 are then formed into a desired shape. With the inventive semiconductor device, different device pinouts can be selected after the die has been encapsulated in plastic or encased in ceramic or another suitable material.

An inventive embodiment comprising an optional third assembly, generally described as element 39 may have advantages. A first embodiment of this third assembly 40, as shown in FIG. 3 (inverted to show detail of the first assembly 8), is manufactured from a substantially insulative material such as polyimide or

plastic, and contains a number of holes or voids 42 through which a conductive substance (not shown) can pass to connect the pads 44 on a second embodiment of the first assembly with the paths 34 on the second assembly 29. Each exterior pad 44 of the first assembly 8 of this embodiment is connected with a bond pad on the die, and, as with the first embodiment, usually only one bond pad of the die will be connected with one pad 44 of the first assembly. The pads 44 of the first assembly and paths 34 of the second assembly form a grid. By placing the holes 42 in the membrane 40 in a particular location, any of the conductive pads 44 of the first assembly can be connected with any of the paths 34 of the second assembly to select any of the **bond options** and pinouts available on the die. The conductive pads 44 of the first assembly extend in a substantially X direction, while the paths 34 of the second assembly extend in a substantially Y direction, thus making possible the connecting of any bond option to any pinout.

For example, to provide a device having a pin 7 ground signal, a hole is placed in the membrane at the junction of the pad 44 which is connected with the ground bond pad on the die, and the pin 7 bar of the second assembly.

Holes 42 in the membrane 40 are filled with conductive material (not shown) and connect selected pads 44 to the paths 34. By using membranes 40 having different designs (i.e. holes 42 in different locations) different pads 44 can be connected with the paths 34 on the second assembly. The conductive substance which fills the voids 42 in the membrane 40 and connects the pads 44 with the paths 34 could comprise a metal-based material such as solder, a curable silver-glass conductive paste such as that available from Johnson-Matthey of San Diego, Calif., or the Z-axis conductive epoxy available from Zymet described above, or other workable means.

FIG. 4 shows the die-first assembly frame attachment of the first assembly 8 of the FIG. 3 embodiment. Each bond pad 18 on the die 10 is connected with a conductive pad 44 or pads with a bond wire 20 or wires. The conductive pads 44 themselves replace the die paddle 12, thus supporting the die 10. A substance such as a nonconductive epoxy or Kapton.RTM. tape mechanically supports the die 10 on the pads 44. The die 10 is wire bonded 20 to the first assembly frame 50. The die, bond wires, and a portion of the pads 44 are then encased in plastic or other suitable material. A ceramic embodiment of the inventive first assembly is also possible, and can be easily constructed from this description by an artisan of skill in the art.

FIG. 5 shows a third embodiment of the first assembly 8 of FIG. 3. In this embodiment, the die (not shown) is placed on the paddle (not shown) of a first assembly frame (not shown), the frame having extremely long paths 52. The die, die paddle, and a portion of the frame are encased in plastic or other material, then the pads 52 are formed and adhered to the encasement material to form the first assembly 8. Attachment to the second assembly with the first assembly is accomplished in a manner similar to that of FIG. 3.

Another embodiment of the first assembly for use with the embodiment as shown in FIG. 3 uses the first assembly of FIG. 1B. After forming the first assembly of FIG. 1B, lines are formed by patterning a conductive material such as conductive epoxy, conductive paste (such as silver-filled paste), conductive ink or any other workable material to form lines similar to 44 as shown in the first assembly 8 of FIG. 3. The lines couple with the exterior pads 24 as shown on FIG. 1B.

In accordance with FIG. 6, another inventive embodiment which may have advantages is to manufacture the third assembly 39 from a flex circuit 60 using tape automated bonding (TAB) techniques. This embodiment shows a first assembly of FIG. 1 with additional pads 24 manufactured therein. Using this arrangement, changing the design of the second assembly 29 to change outputs would not be required, but a flex circuit 60 having different trace 62 routings would connect exterior pads 24 on the first assembly 8 with paths 64 on the second assembly. In this embodiment, long paths on the second assembly would not

be required which may solve problems of lead movement associated in conventional lead frame designs that may be present in the inventive second assembly if the paths are not supported with an insulative material. With the FIG. 6 embodiment, a second assembly is standard within output lead 66 types, and could comprise any number of lead types including ZIP, DIP, single inline (SIP), J-leads, or leadless chip carrier (LCC). To change pinouts or device options, a flex circuit 60 having a different design would be used during the assembly of the device. The first and second assemblies would be connected to the flex circuit 60 using solder techniques known in the art, or by using other materials.

Typical TAB technology employs one or more layers of copper or alloy traces 62 interposed between two or more layers of nonconductive material such as plastic or polyimide. On the top and bottom of the TAB tape are first and second ends where the traces are not covered, which allows for connecting with a conductive material such as solder. To facilitate bonding of the copper or alloy traces with the tin/lead solder, these exposed trace areas are often flashed with layers of gold or platinum chromium, copper, tungsten, nickel, or gold, and solder bumps for reflow are formed over the flashing. Alternately, a Z-axis conductive adhesive can be interposed between the first assembly and the flex circuit, and/or between the second assembly and the flex circuit. This adhesive would electrically connect the pads and paths of the first and second assemblies to the traces in a vertical direction, while providing an adhesive and an insulator in a horizontal direction.

The semiconductor devices as described above provide a means for allowing pinouts and wire **bond options** to be selected after the die is hermetically sealed. The invention is a relatively thin device, and would allow the pinouts and **bond options** to be selected late in the manufacturing process by the semiconductor manufacturer or a large scale semiconductor user.

What have been described are specific configurations of the invention, as applied to particular embodiments. Clearly, variations can be made to the original designs described in this document for adapting the invention to other embodiments. For example, various materials can be used for encapsulation, adhesion, and conductance, and the device can comprise a zig-zag inline package, dual inline package, gull wing package, leadless chip carriers, or a number of other pin types. Additional mechanical attachments for connection of the first and second assemblies are possible. Also, the die as described can comprise several unsingularized die on a section of wafer material, or a number of singularized die. Therefore, the invention should be read as limited only by the appended claims.
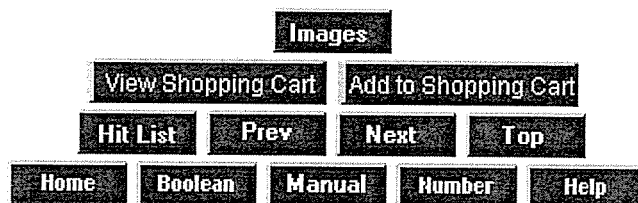
\* \* \* \* \*

IN RE APPLICATION OF:    Cathal G. Phelan

SERIAL NO.:    09/504,344

TITLE:    FIXED BURST MEMORIES

FILED:    February 14, 2000

EXAMINER:    Namzai, M.

ART UNIT:    2187

**RESPONSE TRANSMITTAL AND
EXTENSION OF TIME REQUEST
(IF REQUIRED)**

*RECEIVED
FEB 2 2 2002
Technology Center 2100*

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Sir:

Enclosed please find an amendment, copies of three patents and a postcard along with the fee calculation below:
**FEE CALCULATION FOR ENCLOSED AND EXTENSION REQUEST (IF ANY)**

| | Claims Remaining | Highest No. Previous | Extra Rate | Additional Fee |
|---|---|---|---|---|
| Total Claims | 20 minus | 20 = | 0 x $ 18.00 | $ 0.00 |
| Independent Claims | 3 minus | 3 = | 0 x $ 84.00 | $ 0.00 |
| Multiple Dependent Claim First Added | | | + $280.00 | $ 0.00 |

TOTAL IF NOT SMALL ENTITY .. $0.00

[ ]    SMALL ENTITY STATUS - If applicable, divide by 2 ...................... $0.00
[ ]    Verified statement enclosed, if not previously filed.

[X]    Applicant also requests a __one__ month extension of time
for response to the outstanding Office Action. The fee is .................. $110.00

[ ]    Fee set forth in 37 C.F.R. 1.17 (p) for Information Disclosure
under 37 C.F.R. 1.97 (c) ..................................................... $0.00

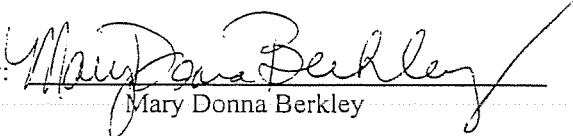TOTAL FEE ..................................................... $110.00

The Commissioner is hereby authorized to charge any overpayment or underpayment of the above fee associated with this Communication to Deposit Account No. 50-0541. A duplicate copy of this sheet is attached.

CHRISTOPHER P. MAIORANA, P.C.

24025 Greater Mack, Suite 200
St. Clair Shores, Michigan 48080
(586) 498-0670

By: _____
Christopher P. Maiorana
Registration No.: 42,829

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on February 4, 2002 .

By: _____
Mary Donna Berkley

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:    Cathal G. Phelan

Serial No.:    09/504,344

Title:    FIXED BURST MEMORIES

Filed:    February 14, 2000

Attorney Docket No.:    0325.00309

Examiner:    Namzai, M.

Art Unit:    2187

In Response To:    Office Action mailed October 2, 2001

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on  February 4, 2002 .

By: _____
Mary Donna Berkley

## AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action mailed October 2, 2001

please amend the above-identified application as follows:

## IN THE SPECIFICATION

Please replace the title with the following:

MEMORY DEVICE WITH FIXED LENGTH NON-INTERRUPTIBLE BURST

1

<u>**VERSION WITH MARKINGS TO SHOW CHANGES MADE**</u>

Please replace the title with the following:

[FIXED BURST MEMORIES] <u>MEMORY DEVICE WITH FIXED LENGTH</u>

<u>NON-INTERRUPTIBLE BURST</u>

2

## IN THE CLAIMS

Please amend the claims as follows:

1. (AMENDED) A circuit comprising:

a memory comprising a plurality of storage elements each configured to read and write data in response to an internal address signal; and

a logic circuit configured to generate a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

2. (AMENDED) The circuit according to claim 1, wherein said predetermined number of internal address signals is determined by a fixed burst length.

3. (AMENDED) The circuit according to claim 1, wherein said predetermined number of internal address signals is at least 4.

4. (AMENDED) The circuit according to claim 1, wherein said predetermined number of internal address signals is 8.

3

5. (AMENDED) The circuit according to claim 2, wherein said fixed burst length is programmable.

6. (AMENDED) The circuit according to claim 5, wherein said fixed burst length is programmed by bond options.

7. (AMENDED) The circuit according to claim 5, wherein said fixed burst length is programmed by voltage levels on external pins.

8. (AMENDED) The circuit according to claim 1, wherein said memory comprises a static random access memory.

9. (AMENDED) The circuit according to claim 1, wherein said memory comprises a dynamic random access memory.

10. (AMENDED) The circuit according to claim 9, wherein said predetermined number of internal address signals is chosen to provide time for at least one writeback or refresh cycle.

11. (AMENDED) The circuit according to claim 1, wherein said predetermined number of internal address signals is chosen to meet predetermined criteria for sharing address and control busses.

4

12. (AMENDED) A circuit comprising:

means for reading data from and writing data to a plurality of storage elements in response to a plurality of internal address signals; and

means for generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

13. (AMENDED) A method of providing a fixed burst length data transfer comprising the steps of:

accessing a memory in response to a plurality of internal address signals; and

generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) a control signal, wherein said generation of said predetermined number of internal address signals is non-interruptible.

14. The method according to claim 13, further comprising the step of programming said predetermined number.

5

15. The method according to claim 14, wherein said programming step is performed using bond options.

16. The method according to claim 14, wherein said programming step is performed using voltage levels.

17. (AMENDED) The method according to claim 13, further comprising the step of selecting said predetermined number to provide time for at least one writeback or refresh cycle.

Please add the following new claims:

18. (NEW) The circuit according to claim 1, wherein said logic circuit comprises a counter configured to generate said predetermined number of internal address signals.

19. (NEW) The circuit according to claim 1, wherein said external address signal comprises an initial address for data transfers to an from said memory.

20. (NEW) A memory device according to claim 1, wherein said circuit is an integrated circuit.

6

## VERSION WITH MARKINGS TO SHOW CHANGES MADE

1.    (AMENDED) [An integrated] A circuit comprising:

a memory comprising a plurality of storage elements each configured to read and write data in response to an internal address signal; and

a logic circuit configured to generate a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

2.    (AMENDED)    The [integrated] circuit according to claim 1, wherein said [predetermine] predetermined number of internal address signals is determined by a fixed burst length.

3.    (AMENDED)    The [integrated] circuit according to claim 1, wherein said predetermined number of internal address signals is at least 4.

4.    (AMENDED)    The [integrated] circuit according to claim 1, wherein said predetermined number of internal address signals is 8.

7

5. (AMENDED) The [integrated] circuit according to claim 2, wherein said fixed burst length is programmable.

6. (AMENDED) The [integrated] circuit according to claim 5, wherein said fixed burst length is programmed by bond options.

7. (AMENDED) The [integrated] circuit according to claim 5, wherein said fixed burst length is programmed by voltage levels on external pins.

8. (AMENDED) The [integrated] circuit according to claim 1, wherein said memory comprises a static random access memory.

9. (AMENDED) The [integrated] circuit according to claim 1, wherein said memory comprises a dynamic random access memory.

10. (AMENDED) The [integrated] circuit according to claim 9, wherein said predetermined number of internal address signals is chosen to provide time for at least one writeback [and] or refresh [cycles] cycle.

8

11. (AMENDED) The [integrated] circuit according to claim 1, wherein said predetermined number of internal address signals is chosen to meet predetermined criteria for sharing address and control busses.

12. (AMENDED) [An integrated] A circuit comprising:

means for reading data from and writing data to a plurality of storage elements in response to [an] a plurality of internal address [signal] signals; and

means for generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

13. (AMENDED) A method of providing a fixed burst length data transfer comprising the steps of:

[reading from and writing data to] accessing a memory in response to [an] a plurality of internal address [signal] signals; and

generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) a control signal, wherein said generation

9

of said predetermined number of internal address signals is non-

10  interruptible.


17. (AMENDED) The method according to claim 13, further comprising the step of selecting said predetermined number to provide time for at least one writeback [and] or refresh [cycles] cycle.


18. (NEW) The circuit according to claim 1, wherein said logic circuit comprises a counter configured to generate said predetermined number of internal address signals.


19. (NEW) The circuit according to claim 1, wherein said external address signal comprises an initial address for data transfers to an from said memory.


20. (NEW) A memory device according to claim 1, wherein said circuit is an integrated circuit.


10

# R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns an integrated circuit comprising a memory and a logic circuit. The memory may comprise a plurality of storage elements each configured to read and write data in response to an internal address signal. The logic circuit may be configured to generate a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals. The generation of the predetermined number of internal address signals is non-interruptible.

## SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims and new claims 18-20 may be found in the drawings (e.g., FIGS. 1-6) and the specification (e.g., page 5, lines 2-14 and page 6, line 19 thru page 8, line 2) as originally filed. As such, no new matter has been added.

## OBJECTION TO THE TITLE

The objection to the title has been obviated by appropriate amendment and should be withdrawn.

11

## CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claims 6 and 15 under 35 U.S.C. §112, second paragraph, is respectfully traversed and should be withdrawn.

Support for claims 6 and 15 may be found on page 8, lines 3-8 of the specification. Furthermore, bond options are well known in the art and, therefore, one skilled in the art would understand how to make and/or use bond options. Copies of U.S. patents 6,188,636 (issued February 13, 2001), 5,900,021 (issued May 4, 1999) and 5,360,992 (issued November 1, 1994) from the USPTO web site (www.uspto.gov) are attached as evidence of bond options being well known in the art.

## CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-17 under 35 U.S.C. §102(e) as being anticipated by Yip et al. '138 (hereinafter Yip) is respectfully traversed and should be withdrawn.

Yip discloses a general image processor (Title). The image processor includes a raster image coprocessor with a cache memory (elements 224 and 230 of FIG. 1 of Yip) connected to an external DRAM (element 1910 of FIG. 146 of Yip) via a local memory controller and an external interface (see FIG. 2). Accesses to the cache 230 and the external DRAM 1910 are interruptible (see column

12

54, lines 42-47, column 115, lines 26-29 and lines 52-55 and column 116, lines 20-22 of Yip).

In contrast, the present invention provides a logic circuit configured to generate a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, where **the generation of the predetermined number of internal address signals is non-interruptible**. Assuming, *arguendo*, that the cache 230 of Yip is similar to the presently claimed memory (as suggested by the Office Action in the last paragraph on page 3 and for which Applicants' representative does not necessarily agree), Yip does not disclose or suggest the generation of a predetermined number of internal address signals that is non-interruptible, as presently claimed. As such, the present invention is fully patentable over the cited reference and the rejection should be withdrawn.

In particular, during an access of the cache 230, Yip teaches that when a cache miss occurs the cache access is stalled until all the values needed are read from an external memory and stored in the cache (column 54, lines 42-47 of Yip). Since the access to the cache 230 can be stalled and writing of updated data to the cache must be accommodated, it follows that the generation of addresses for accessing the cache 230 is interruptible. Yip

13

teaches a cache access that can be stalled. Yip fails to disclose or suggest the generation of a predetermined number of internal address signals that is **non-interruptible**, as presently claimed. As such, the present invention is fully patentable over the cited reference and the rejection should be withdrawn.

Furthermore, assuming, *arguendo*, that the external DRAM 1910 of Yip is similar to the presently claimed memory (as suggested by the Office Action on page 4, lines 20-21 and for which Applicants' representative does not necessarily agree), Yip still does not disclose or suggest the generation of a predetermined number of internal address signals that is non-interruptible, as presently claimed. As such, the present invention is fully patentable over the cited reference and the rejection should be withdrawn.

Specifically, Yip teaches that a write burst to the DRAM 1910 can be interrupted when there is a cycle request from a higher priority port (column 115, lines 26-29 of Yip). Similarly, Yip teaches that a read burst will be terminated when a higher priority DRAM request is received (column 115, lines 52-55 of Yip). Since Yip teaches that a burst can be interrupted, Yip fails to disclose or suggest the generation of a predetermined number of internal address signals that is non-interruptible, as presently claimed.

14

As such, the present invention is fully patentable over the cited reference and the rejection should be withdrawn.

Despite the suggestion of the Office Action on page 4, lines 1-3, Yip does not disclose or suggest generating a predetermined number of internal address signals that is **non-interruptible**, as presently claimed. Restricting rearbitration for the DRAM 1910 so that an interruptible burst is not interrupted until a preset number of data words have been transferred (see column 115, lines 60-64 of Yip) is not the same as generating a predetermined number of internal address signals that is **non-interruptible**, as presently claimed. Therefore, Yip does not disclose or suggest generating a predetermined number of internal address signals that is **non-interruptible**, as presently claimed. As such, the present invention is fully patentable over the cited reference and the rejection should be withdrawn.

New claims 18-20 depend directly from independent claim 1, which is believed to be allowable, and, therefore, are fully patentable over the cited reference.
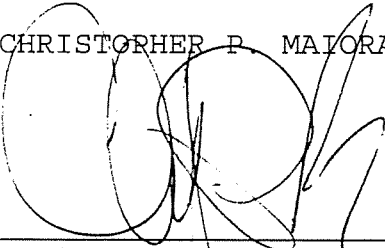
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

15

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.

Christopher P. Maiorana
Registration No. 42,829
24025 Greater Mack, Suite 200
St. Clair Shores, MI 48080
(586) 498-0670

Dated: February 4, 2002

Docket No.: 0325.00309

16

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/504,344 | 02/14/2000 | Cathal G. Phelan | 0325.000309 | 7771 |

21363    7590    04/25/2002

CHRISTOPHER P. MAIORANA, P.C.
24025 GREATER MACK
SUITE 200
ST. CLAIR SHORES, MI   48080

| EXAMINER |
|---|
| NAMAZI, MEHDI |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2187 | |

DATE MAILED: 04/25/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ___*three*___ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) ☒ Responsive to communication(s) filed on _Feb 14, 2002_

2a) ☐ This action is **FINAL.**    2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

**Disposition of Claims**

4) ☒ Claim(s) _1-20_ is/are pending in the applica

    4a) Of the above, claim(s) _____ is/are withdrawn from considerá

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) _1-20_ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requireme

**Application Papers**

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. § 119**

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

    a)☐ All b) ☐ Some* c) ☐None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    *See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

**Attachment(s)**

15) ☐ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other: _____

## DETAILED ACTION

1.    This office action is in response to the amendment filed

February 14, 2002 ( Amendment A ).

2.    Claims 1-17 are presented for further examination in view of

the foregoing amendments and remarks. Claims 1-13, and 17 have

been amended. No claim has been canceled. New claims 18-20 have

been added.     Therefore, claims 1-20 are pending.


### *Response to Arguments*

3.    Applicant's arguments with respect to claims 1-17 have been

considered but are moot in view of the new ground(s) of

rejection.


### *Claim Objections*

4.    Claim 19 is objected to because of the following

informalities:

        As per claim 19, line 3, replace "an" with --and--.

        Appropriate correction is required.

### Claim Rejections - 35 USC § 102

5.    The following is a quotation of the appropriate paragraphs

of 35 U.S.C. 102 that form the basis for the rejections under

this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in
> this or a foreign country or in public use or on sale in this country, more
> than one year prior to the date of application for patent in the United
> States.

6.    Claims 1-17 are rejected under 35 U.S.C. 102(b) as being

anticipated by Cowles(U.S.Patent No. 5,729,504).

As per claims 1 and 12-13 Cowles teaches a circuit

comprising: a memory comprising a plurality of storage elements

each configured to read and write data in response to an internal

address signal(fig. 1, element 12); and  a logic circuit

configured to generate a predetermined number of said internal

address signals in response to (I) an external address signal

(col. 2, lines 20-21), (ii) a clock signal(col. 9, lines 59-61)

and (iii) one or more control signals(fig. 1, element 38, produce

control signal), wherein said generation of said predetermined

number of internal address signals is non-interruptible(col. 8,

lines 18-22).

As per claims 2, Cowles teaches wherein said predetermine number of internal address signals is determined by a fixed burst length(col. 5, lines 47-53).

As per claims 3-4 and 14, Cowles teaches wherein said predetermined number of internal address signals are 4 or 8(fig. 2, shows various burst length of 2, 4, and 8).

As per claim 5, Cowles teaches wherein said fixed burst length is programmable(col. 5, lines 31-34).

As per claims 6 and 15, Cowles teaches wherein said fixed burst length is programmed by bond options(it is well known in the art to include multiple modes of operation selected by bond options).

As per claims 7 and 16, Cowles teaches wherein said fixed burst length is programmed by voltage levels on external pins(it is inherent to have voltage levels for each burst).

As per claim 8, Cowles teaches wherein said memory comprises a static random access memory(fig. 1, element 12).

As per claim 9, Cowles teaches wherein said memory comprises a dynamic random access memory(fig. 1, element 12).

As per claims 10 and 17, Cowles teaches wherein said predetermined number of internal address signals is chosen to provide time for at least one writeback or refresh cycle(it is

inherent to have time included for writeback and refresh cycle during each burst).

As per claim 11, Cowles teaches wherein the predetermined number of internal address signals is chosen to meet predetermined criteria for sharing address and control busses (col. 8, lines 18-22).

As per claim 18, Cowles teaches wherein the logic circuit comprises a counter configured to generate the predetermined number of internal address signals(fig. 1, element 26).

As per claim 19, Cowles teaches wherein the external address signal comprises an initial address for data transfers to and from the memory(col. 2, lines 21-22).

As per claim 20, Cowles teaches wherein the circuit is an integrated circuit(abstract).

**Conclusion**

7.    The prior art made of record and not relied upon is considered pertinent to applicant's
disclosure.

_U.S. Patent (5,966,724) (Ryan)_ Teaches synchronous memory device with dual page and burst mode operations.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mehdi

Namazi whose telephone number is (703) 306-2758. The examiner

can normally be reached on Monday-Thursday from 7:00 to 5:30.

If attempts to reach the examiner by telephone are

unsuccessful, the examiner's supervisor, Do Hyun yoo, can be

reached on (703) 308-4908.

Any inquiry of a general nature or relating to the status of

this application or proceeding should be directed to the Group

receptionist whose telephone number is (703) 305-9600.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

**or faxed to:**

(703) 746-7239 (for formal communications intended for
entry)


**Or:**

(703) 746-7240 (for informal or draft communications, please

label PROPOSED or DRAFT )

Hand-delivered responses should be brought to Crystal Park 2,

2121 Crystal Drive,

Arlington, VA., Sixth Floor (Receptionist).

M. Namazi
April 21, 2002

DO HYUN YOO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

| FORM PTO-892 | U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE | SERIAL NO. 09/504,344 | GROUP ART UNIT 2187 | ATTACHMENT TO PAPER NO. | 6 |
|---|---|---|---|---|---|
| **NOTICE OF REFERENCES CITED** | | APPLICANT(S) Phelan | | | |

### U.S. PATENT DOCUMENTS

| * | | DOCUMENT NO. | DATE | NAME | CLASS | SUB-CLASS | FILING DATE |
|---|---|---|---|---|---|---|---|
| | A | 5,729,504 | 3/1998 | Cowles | 365 | 236 | |
| | B | 5,966,724 | 10/1999 | Ryan | 711 | 105 | |
| | C | | | | | | |
| | D | | | | | | |
| | E | | | | | | |
| | F | | | | | | |
| | G | | | | | | |
| | H | | | | | | |
| | I | | | | | | |
| | J | | | | | | |
| | K | | | | | | |

### FOREIGN PATENT DOCUMENTS

| * | | DOCUMENT NO. | DATE | COUNTRY | NAME | CLASS | SUB-CLASS |
|---|---|---|---|---|---|---|---|
| | L | | | | | | |
| | M | | | | | | |
| | N | | | | | | |
| | O | | | | | | |
| | P | | | | | | |
| | Q | | | | | | |

### OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

| | |
|---|---|
| R | |
| S | |
| T | |
| U | |

| EXAMINER Mehdi Namazi | DATE April 21, 2002 | Form892ccs2106b |
|---|---|---|

\* A copy of this reference is not being furnished with this office action.
(See Manual of Patent Examining Procedure, section 707.05(a).)
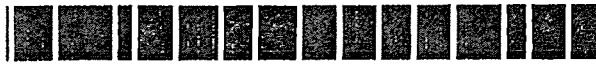
[54] **CONTINUOUS BURST EDO MEMORY DEVICE**

[75] Inventor: Timothy B. Cowles, Boise, Id.

[73] Assignee: Micron Technology, Inc., Boise, Id.

[21] Appl. No.: 572,487

[22] Filed: Dec. 14, 1995

[51] Int. Cl.$^6$ .................................................. G11C 8/00
[52] U.S. Cl. ..................... 365/236; 365/238.5; 365/239; 395/496
[58] Field of Search ............................. 365/236, 238.5, 365/239; 395/496

[56] **References Cited**

U.S. PATENT DOCUMENTS

| 4,344,156 | 8/1982 | Eaton et al. | 365/203 |
| 4,484,308 | 11/1984 | Lewandowski et al. | 364/900 |
| 4,562,555 | 12/1985 | Ouchi et al. | 365/233 |
| 4,567,579 | 1/1986 | Patel et al. | 365/189 |
| 4,575,825 | 3/1986 | Ozaki et al. | 365/189 |
| 4,603,403 | 7/1986 | Toda | 365/189 |

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

19507562 9/1995 Germany .

OTHER PUBLICATIONS

"Dram 1 Meg X 4 Dram 5Vedo Page Mode", *1995 DRAM Data Book*, pp. 1–1 thru 1–30, (Micron Technology, I).
"Rossini, Pentium, PCI–ISA, Chip Set", *Symphony Laboratories*, entire book.

"4DRAM 1991", *Toshiba America Electronic Components, Inc.*, pp. A–137—A–159.

"Application Specific DRAM", *Toshiba America Electronic Components, Inc.*, C178, C–260, C 218, (1994).

"Burst DRAM Function & Pinout", *Oki Electric Ind., Co., Ltd., 2nd Presentation, Item #619*, (Sep. 1994)

(List continued on next page.)

Primary Examiner—David C. Nelms
Assistant Examiner—F. Niranjan
Attorney, Agent, or Firm—Schwegman, Lundberg, Woessner & Kluth, P.A.

[57] **ABSTRACT**

An integrated circuit memory device is described which can operate at high data speeds. The memory device can either store or retrieve data from the memory in a burst access operation. The burst operations latch a memory address from external address lines and internally generates additional memory addresses. The integrated circuit memory can output data in a continuous stream while new rows of the memory are accessed. A method and circuit are described for outputting a burst of data stored in a first row of the memory while accessing a second row of the memory.

**20 Claims, 7 Drawing Sheets**
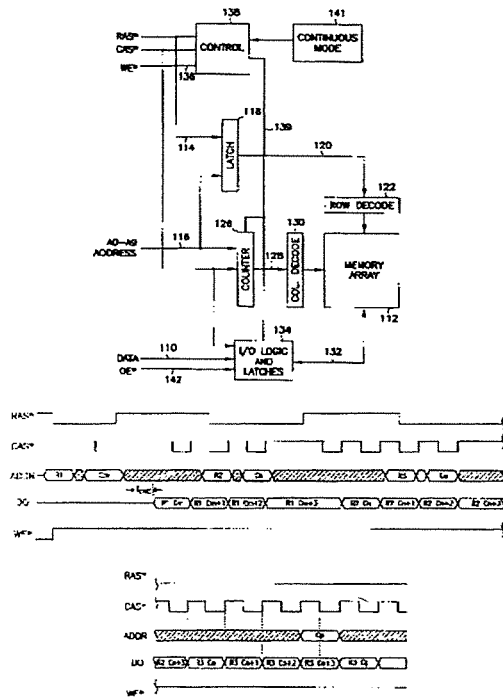
## U.S. PATENT DOCUMENTS

| | | | |
|---|---|---|---|
| 4,618,947 | 10/1986 | Tran et al. | 365/230 |
| 4,649,522 | 3/1987 | Kirsch | 365/189 |
| 4,685,089 | 8/1987 | Patel et al. | 365/233 |
| 4,707,811 | 11/1987 | Takemae et al. | 365/239 |
| 4,788,667 | 11/1988 | Nakano | 365/193 |
| 4,870,622 | 9/1989 | Aria et al. | 365/230 |
| 4,875,192 | 10/1989 | Matsumoto | 365/193 |
| 5,058,066 | 10/1991 | Yu | 365/189.05 |
| 5,126,975 | 6/1992 | Handy et al. | 365/230 |
| 5,257,200 | 10/1993 | Tobita | 365/189 |
| 5,268,865 | 12/1993 | Takasugi | 365/189 |
| 5,280,594 | 1/1994 | Young et al. | |
| 5,305,284 | 4/1994 | Iwase | 365/238.5 |
| 5,325,330 | 6/1994 | Morgan | 365/189.05 |
| 5,325,502 | 6/1994 | McLaury | 395/425 |
| 5,349,566 | 9/1994 | Merritt et al. | 365/233.5 |
| 5,357,469 | 10/1994 | Sommer et al. | 365/193 |
| 5,373,227 | 12/1994 | Keeth | 323/313 |
| 5,379,261 | 1/1995 | Jones, Jr. | 365/230 |
| 5,392,239 | 2/1995 | Margulis et al. | 365/189 |
| 5,410,670 | 4/1995 | Hansen et al. | 365/425 |
| 5,452,261 | 9/1995 | Chung et al. | 365/233 |
| 5,457,659 | 10/1995 | Schaefer | 365/222 |
| 5,526,320 | 6/1996 | Zagar et al. | 365/233.5 |

## OTHER PUBLICATIONS

"Hyper Page Mode DRAM", *8029 Electronic Engineering*, 66, No. 813, Woolwich, London, GB, pp. 47–48, (Sep. 1994).

"Mosel–Vitelic V53C8257H DRAM Specification Sheet, 20 pages, Jul. 2, 1994".

"Pipelined Burst DRAM", *Toshiba, JEDEC JC 42.3 Hawaii*, (Dec. 1994).

"Samsung Synchronous DRAM", *Samsung Electronics*, pp. 1–16, (Mar. 1993).

"Synchronous DRAM 2 MEG x 8 SDRAM", *Micron Semiconductor, Inc.*, pp. 2–43 through 2–8.

Dave Bursky, "Novel I/O Options and Innovative Architectures Let DRAMs Achieve SRAM Performance; Fast DRAMS can be swapped for SRAM Caches", *Electronics Design*, vol. 41, No. 15, Cleveland, Ohio, pp. 55–67, (Jul. 22, 1993).

Shiva P. Gowni, et al., "A 9NS, 32K X 9, BICMOS TTL Synchronous Cache RAM With Burst Mode Access", *IEEE*, Custom Integrated Circuits Conference, pp. 781–786, (Mar. 3, 1992).
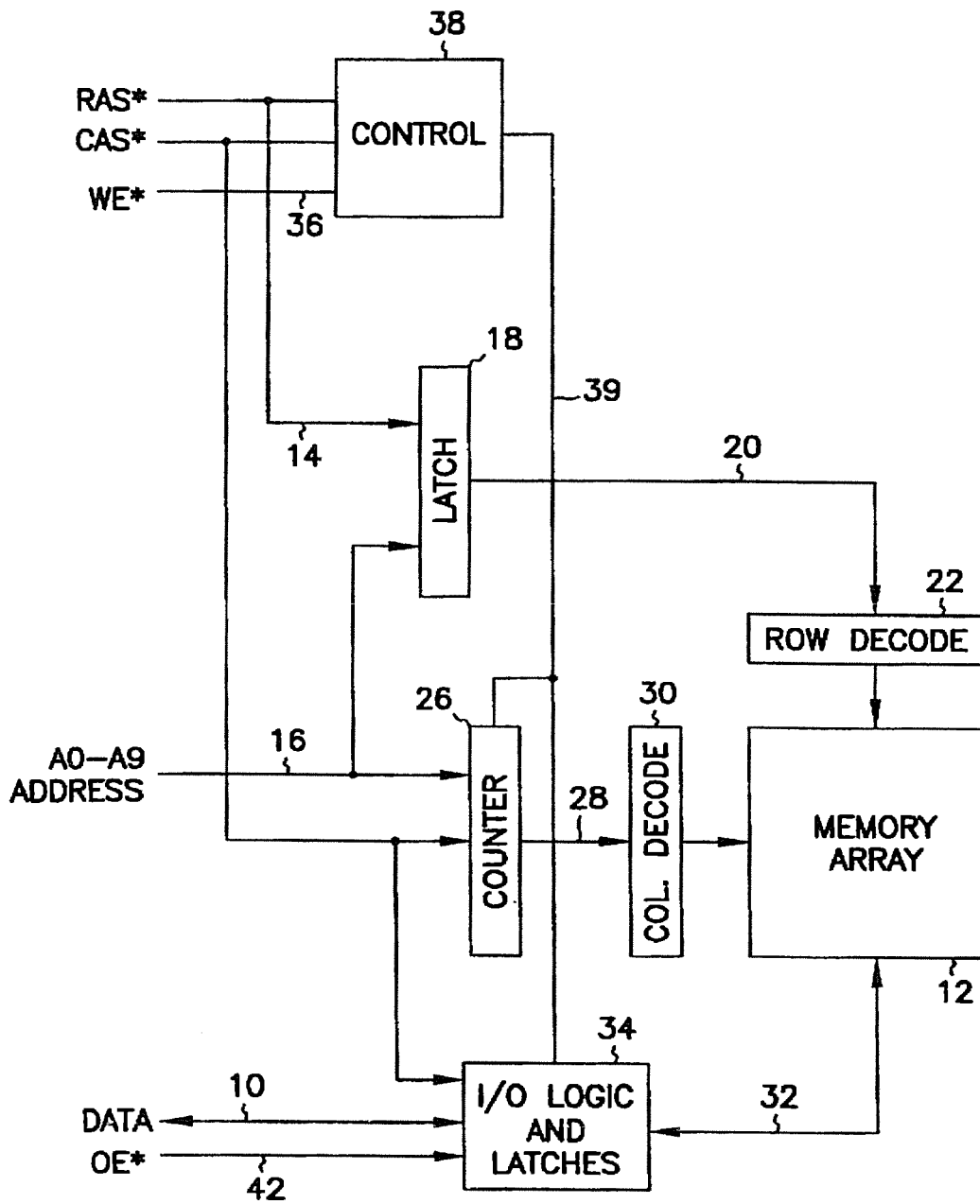
FIG. 1 (PRIOR ART)

| Burst Length | Starting Column Address | | | Linear | Interleave |
|---|---|---|---|---|---|
| | $A_2$ | $A_1$ | $A_0$ | | |
| 2 | V | V | 0 | 0-1 | 0-1 |
| | V | V | 1 | 1-0 | 1-0 |
| 4 | V | 0 | 0 | 0-1-2-3 | 0-1-2-3 |
| | V | 0 | 1 | 1-2-3-0 | 1-0-3-2 |
| | V | 1 | 0 | 2-3-0-1 | 2-3-0-1 |
| | V | 1 | 1 | 3-0-1-2 | 3-2-1-0 |
| 8 | 0 | 0 | 0 | 0-1-2-3-4-5-6-7 | 0-1-2-3-4-5-6-7 |
| | 0 | 0 | 1 | 1-2-3-4-5-6-7-0 | 1-0-3-2-5-4-7-6 |
| | 0 | 1 | 0 | 2-3-4-5-6-7-0-1 | 2-3-0-1-6-7-4-5 |
| | 0 | 1 | 1 | 3-4-5-6-7-0-1-2 | 3-2-1-0-7-6-5-4 |
| | 1 | 0 | 0 | 4-5-6-7-0-1-2-3 | 4-5-6-7-0-1-2-3 |
| | 1 | 0 | 1 | 5-6-7-0-1-2-3-4 | 5-4-7-6-1-0-3-2 |
| | 1 | 1 | 0 | 6-7-0-1-2-3-4-5 | 6-7-4-5-2-3-0-1 |
| | 1 | 1 | 1 | 7-0-1-2-3-4-5-6 | 7-6-5-4-3-2-1-0 |

FIG. 2
(PRIOR ART)

RAS

CAS

ADDR        ROW      COLm      COLn      COLp

WE

DQ        m    m+1    m+2    m+3    n    n+1        p    p+1    p+2

OE

**FIG. 4** (PRIOR ART)

FIG. 6A

RAS*

CAS*

ADDR — R1 — Cm — R2 — Cn — R3 — Co

DQ — R1 Cm — R1 Cm+1 — R1 Cm+2 — R1 Cm+3 — R2 Cn — R2 Cn+1 — R2 Cn+2 — R2 Cn+3

→ Tcac ←

WE*

FIG. 6B

RAS*

CAS*

ADDR — Cp

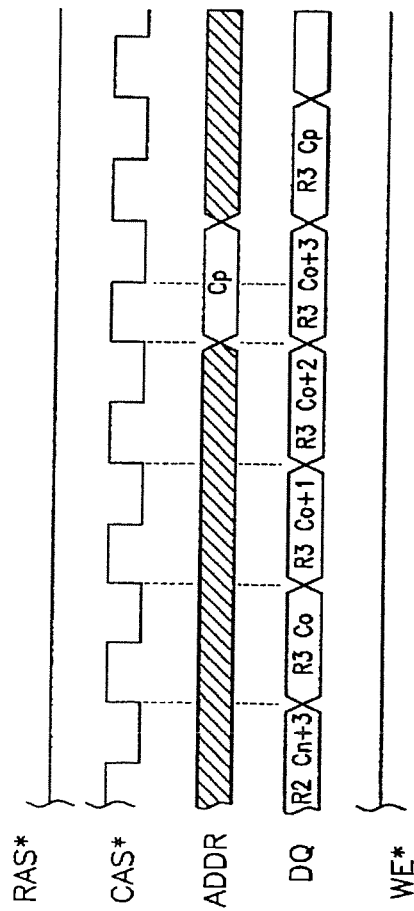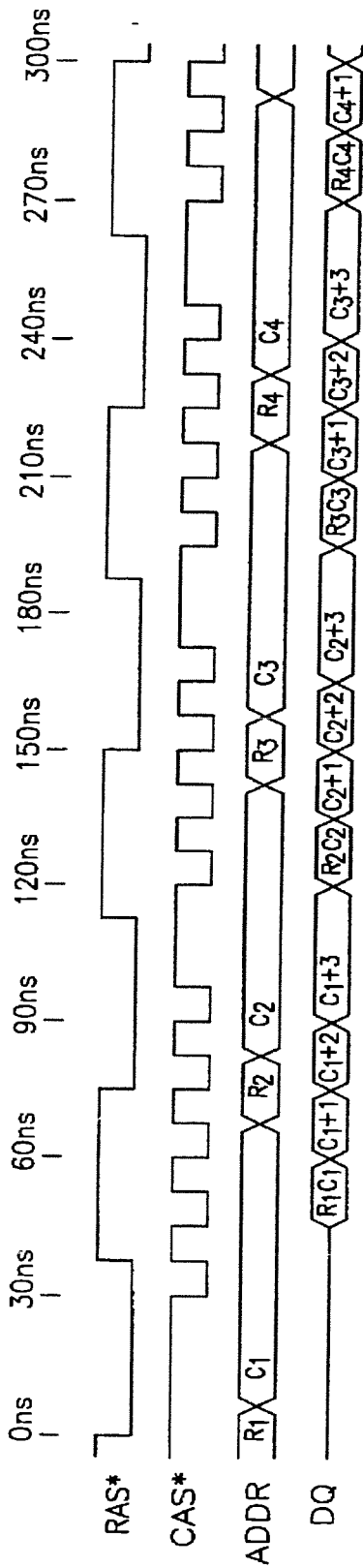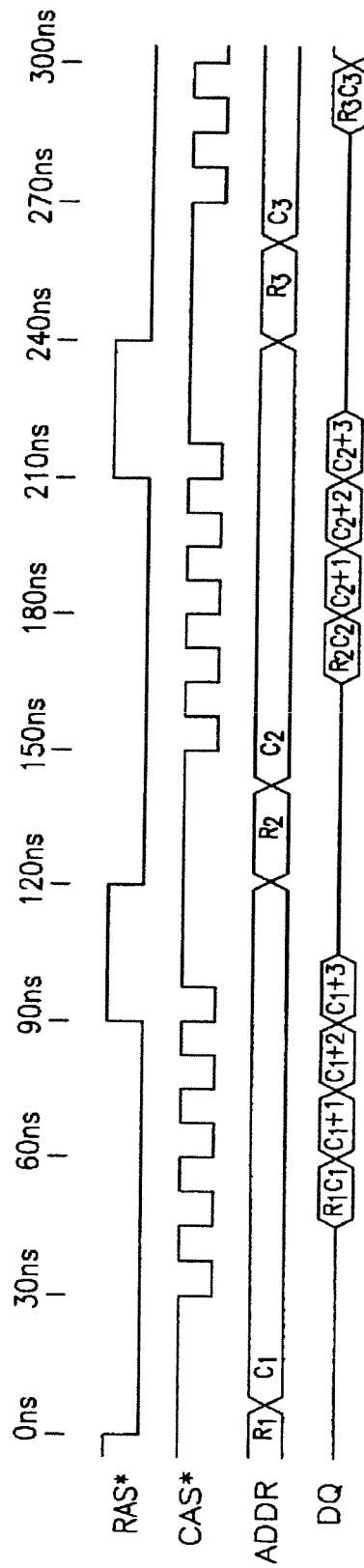DQ — R2 Cn+3 — R3 Co — R3 Co+1 — R3 Co+2 — R3 Co+3 — R3 Cp

WE*
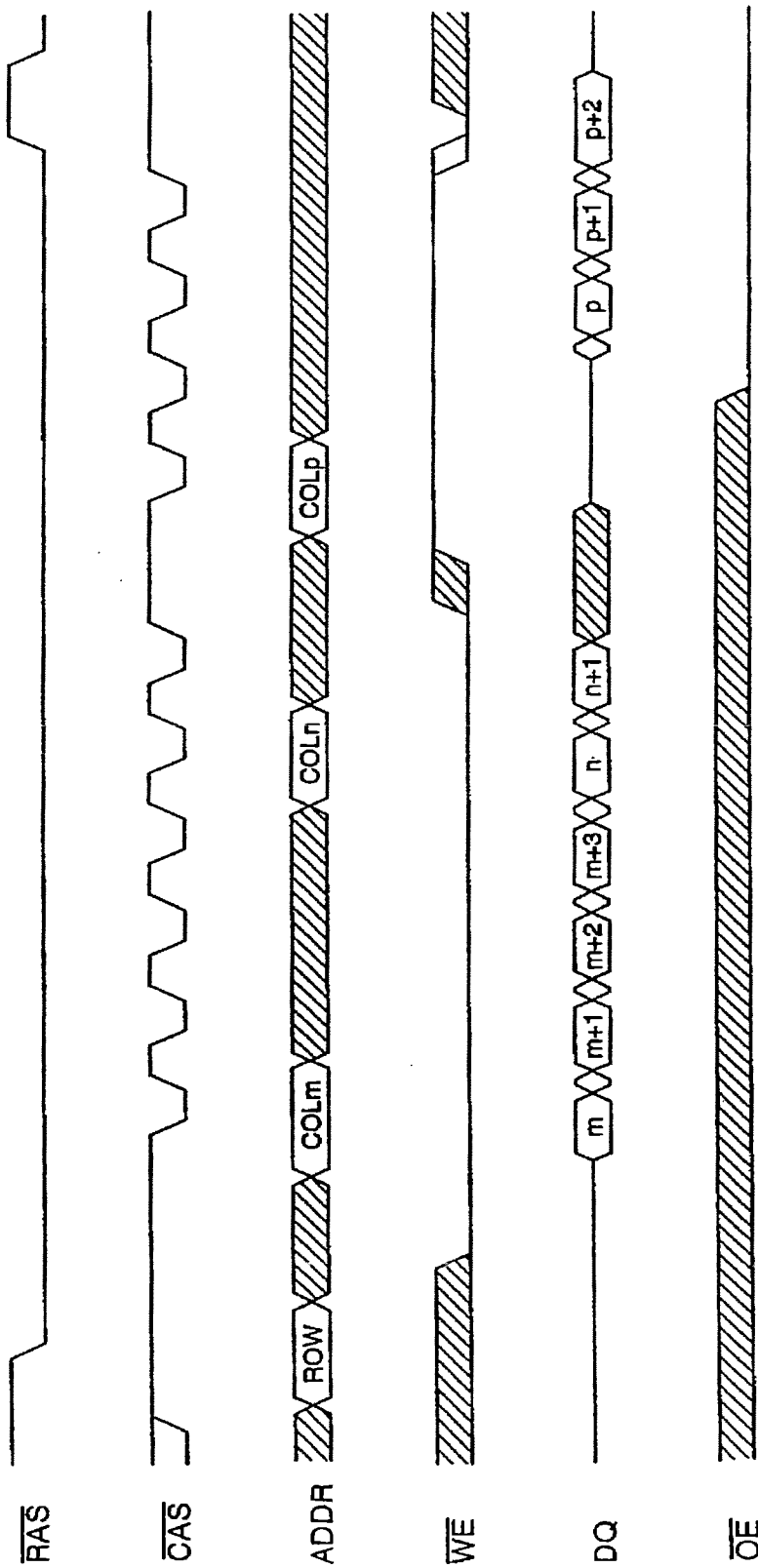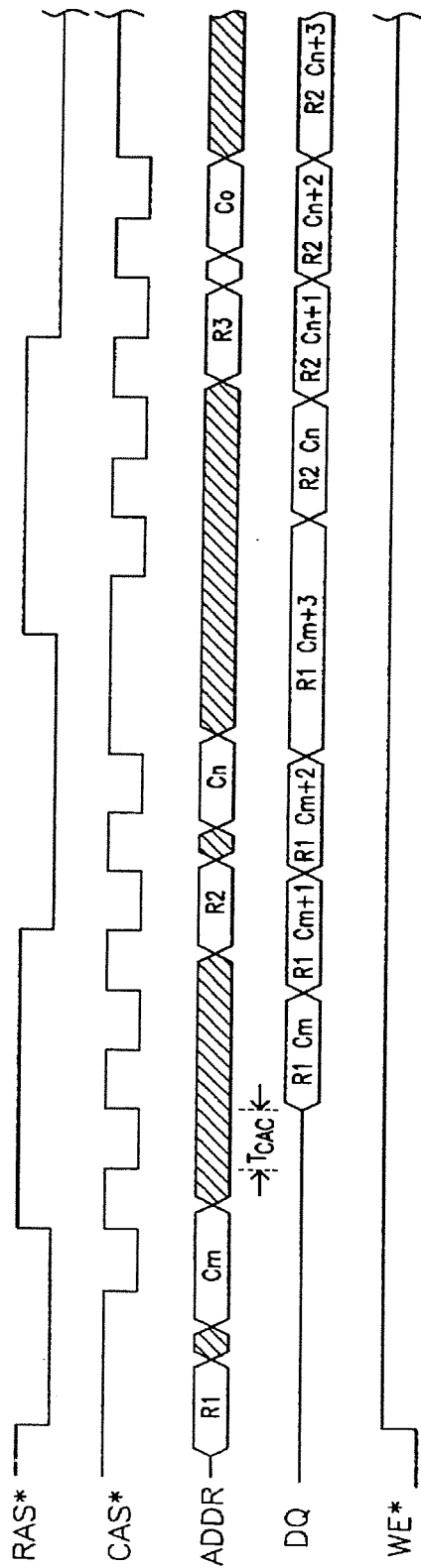
FIG. 7A



FIG. 7B

# CONTINUOUS BURST EDO MEMORY DEVICE

## TECHNICAL FIELD OF THE INVENTION

The present invention relates generally to integrated circuit memories and in particular the present invention relates to burst access memories.

## BACKGROUND OF THE INVENTION

A wide variety of integrated circuit memories are available for storing data. One type of memory is the dynamic random access memory (DRAM). A DRAM is designed to store data in memory cells formed as capacitors. The data is stored in a binary format; a logical "one" is stored as a charge on a capacitor, and a logical "zero" is stored as a discharged capacitor. The typical DRAM is arranged in a plurality of addressable rows and columns. To access a memory cell, a row is first addressed so that all memory cells coupled with that row are available for accessing. After a row has been addressed, at least one column can be addressed to pinpoint at least one specific memory cell for either reading data from, or writing data to via external data communication lines. The data stored in the memory cells is, therefore, accessible via the columns.

With the constant development of faster computer and communication applications, the data rates in which a memory circuit must operate continue to increase. To address the need for increased data rates, a variety of DRAMs are commercially available. These memories are produced in a variety of designs which provide different methods of reading from and writing to the dynamic memory cells of the memory. One such method is page mode operation. Page mode operations in a DRAM are defined by the method of accessing a row of a memory cell array and randomly accessing different columns of the array. Data stored at the row and column intersection can be read and output while that column is accessed. Page mode DRAMs require access steps which limit the communication speed of the memory circuit.

An alternate type of memory circuit is the extended data output (EDO) memory which allows data stored at a memory array address to be available as output after the addressed column has been closed. This memory circuit can increase some communication speeds by allowing shorter access signals without reducing the time in which memory output data is available on the communication lines. Column access times are, therefore, "masked" by providing the extended data output. A more detailed description of a DRAM having EDO features is provided in the "1995 DRAM Data Book" pages 1—1 to 1–30 available from Micron Technology, Inc. Boise, Id., which is incorporated herein by reference.

Yet another type of memory circuit is a burst access memory which receives one address of a memory array on external address lines and automatically addresses a sequence of columns without the need for additional column addresses to be provided on the external address lines. By reducing the external address input signals, burst EDO memory circuits (BEDO) are capable of outputting data at significantly faster communication rates than the above described memory circuits.

Although BEDO memories can operate at significantly faster data rates than non-burst memories, bursts of output data are terminated when changing from one memory row to another. The alternative to terminating a data burst is to wait until a data burst is complete until the memory row is

changed. Changing memory rows is time consuming and because data is interrupted during the transition between rows, the data rate of the memory circuits is slowed.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a burst access memory which allows a data burst to continue while receiving and addressing a new memory row address.

## SUMMARY OF THE INVENTION

The above mentioned problems with integrated memory circuits and other problems are addressed by the present invention and which will be understood by reading and studying the following specification. A burst access memory device is described which allows a new memory array row to be accessed while continually bursting data out from a prior memory row.

In particular, the present invention describes a memory device comprising addressable memory elements, external address inputs, and an address counter for receiving an address on the external address inputs. The address counter also generates a sequence of addresses. The memory further comprises an output buffer adapted to drive a sequence of data from the memory device. The output buffer circuitry can drive the sequence of data from the memory device while a new address is received by the address counter.

In one embodiment, the memory includes a write enable signal input for receiving an enable signal, and termination circuitry for terminating an output of the sequence of data. In another embodiment, a memory device is described which comprises addressable memory elements arranged in rows and columns, external address inputs, and address circuitry for receiving row addresses and column addresses from the external address inputs. Counter circuitry is included for generating a sequence of column addresses in response to a first received column address. The memory also includes row access circuitry for accessing a row of memory elements in response to a received first row address, and an output buffer for outputting a sequence of data from the memory device. The sequence of data being stored in the addressable memory elements having addresses corresponding to the sequence of addresses and the first row address. The memory further includes control circuitry for controlling the output buffer circuitry and the access circuitry, wherein a second row of memory elements can be accessed without interrupting the output sequence of data from the first row address.

In yet another embodiment, a method of burst reading data from a memory device having addressable memory elements arranged in rows and columns is described. The method comprises the steps of receiving a first row address, receiving a first column address, and accessing a row of memory elements having the first row address. The method also includes the steps of generating a sequence of column addresses starting at the first column address, outputting data stored at the sequence of column addresses, receiving a second row address, and accessing a row of memory elements having the second row address while outputting the data stored at the sequence of column addresses.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a memory device incorporating burst access;

FIG. 2 illustrates linear and interleaved addressing sequences;

3

FIG. 3 is a timing diagram of a burst read followed by a burst write of the device of FIG. 1;

FIG. 4 is a timing diagram of a burst write followed by a burst read of the device of FIG. 1;

FIG. 5 is a block diagram of a memory device incorporating the features of the present invention;

FIG. 6a is a timing diagram of the operation of the device of FIG. 5;

FIG. 6b is a continuation of the timing diagram of FIG. 6a;

FIG. 7a is a timing diagram of a series of continuous burst read operations; and

FIG. 7b is a timing diagram of a series of burst read operations.

## DETAILED DESCRIPTION OF THE INVENTION

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the inventions may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present inventions. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present inventions is defined only by the appended claims.

### BEDO Memories

To fully understand the present invention, a detailed description is provided of a burst extended data output memory circuit (BEDO). FIG. 1 is a schematic representation of a sixteen megabit device designed to operate in a burst access mode. The device is organized as a 2 Meg×8 burst EDO DRAM having an eight bit data input/output path 10 providing data storage for 2,097,152 bytes of information in the memory array 12. An active-low row address strobe (RAS*) signal 14 is used to latch a first portion of a multiplexed memory address, from address inputs A0 through A10 16, in latch 18. The latched row address 20 is decoded in row decoder 22. The decoded row address is used to select a row of the memory array 12. An active-low column address strobe (CAS*) signal 24 is used to latch a second portion of a memory address from address inputs 16 into column address counter 26. The latched column address 28 is decoded in column address decoder 30. The decoded column address is used to select a column of the memory array 12.

In a burst read cycle, data within the memory array located at the row and column address selected by the row and column address decoders is read out of the memory array and sent along data path 32 to output latches 34. Data 10 driven from the burst EDO DRAM may be latched external to the device with a CAS* signal after a predetermined number of CAS* cycle delays (latency). For a two cycle latency design, the first CAS* failing edge during a RAS* cycle is used to latch the initial address for the burst access. The first burst data from the memory is driven from the memory after the second CAS* falling edge, and remains valid through the third CAS* failing edge. Once the memory device begins to output data in a burst read cycle, the output drivers 34 will continue to drive the data lines without

4

tri-stating the data outputs during CAS* high intervals dependent on the state of the output enable 42 and write enable 36 (OE* and WE*) control lines, thus allowing additional time for the system to latch the output data. Once a row and a column address are selected, additional transitions of the CAS* signal are used to advance the column address within the column address counter in a predetermined sequence. The time at which data will be valid at the outputs of the burst EDO DRAM is dependent only on the timing of the CAS* signal provided that OE* is maintained low, and WE* remains high. The output data signal levels may be driven in accordance with standard CMOS, TTL, LVTTL, GTL, or HSTL output level specifications.

The address may be advanced linearly, or in an interleaved fashion for maximum compatibility with the overall system requirements. FIG. 2 is a table which shows linear and interleaved addressing sequences for burst lengths of 2, 4 and 8 cycles. The "V" for starting addresses A1 and A2 in the table represent address values that remain unaltered through the burst sequence. The column address may be advanced with each CAS* transition. When the address is advanced with each transition of the CAS* signal, data is also driven from the part after each transition following the device latency which is then referenced to each edge of the CAS* signal. This allows for a burst access cycle where CAS* toggles only once (high to low or low to high) for each memory cycle. This is in contrast to standard DRAMs which require CAS* to go low and then high for each cycle, and synchronous DRAMs which require a full CAS* cycle (high and low transitions) for each memory cycle.

In the burst access memory device, each new column address from the column address counter is decoded and is used to access additional data within the memory array without the requirement of additional column addresses being specified on the address inputs 16. This burst sequence of data will continue for each CAS* failing edge until a predetermined number of data accesses equal to the burst length has occurred. A CAS* falling edge received after the last burst address has been generated will latch another column address from the address inputs 16 and a new burst sequence will begin. Read data is latched and output with each falling edge of CAS* after the first CAS* latency. For a burst write cycle, data 10 is latched in input data latches 34. Data targeted at the first address specified by the row and column addresses is latched with the CAS* signal when the first column address is latched (write cycle data latency is zero). Other write cycle data latency values are possible; however, for today's memory systems, zero is preferred. Additional input data words for storage at incremented column address locations are latched by CAS* on successive CAS* pulses. Input data from the input latches 34 is passed along data path 32 to the memory array where it is stored at the location selected by the row and column address decoders. As in the burst read cycle previously described, a predetermined number of burst access writes will occur without the requirement of additional column addresses being provided on the address lines 16. After the predetermined number of burst writes has occurred, a subsequent CAS* will latch a new beginning column address, and another burst read or write access will begin.

Control circuitry 38, in addition to performing standard DRAM control functions, controls the I/O circuitry 34 and the column address counter/latch 26. The control circuitry determines when a current data burst should be terminated based upon the state of RAS* 14, CAS* 24 and WE* 36. The write enable signal is used in burst access cycles to select read or write burst accesses when the initial column address

for a burst cycle is latched by CAS*. WE* low at the column address latch time selects a burst write access. WE* high at the column address latch time selects a burst read access. The level of the WE* signal must remain high for read and low for write burst accesses throughout the burst access. A low to high transition within a burst write access will terminate the burst access, preventing further writes from occurring. A high to low transition on WE* within a burst read access will likewise terminate the burst read access and will place the data output 10 in a high impedance state. Transitions of the WE* signal may be locked out during critical timing periods within an access cycle in order to reduce the possibility of triggering a false write cycle. After the critical timing period, the state of WE* will determine whether a burst access continues, is initiated, or is terminated. Termination of a burst access resets the burst length counter and places the DRAM in a state to receive another burst access command. In the case of burst reads, WE* will transition from high to low to terminate a first burst read, and then WE* will transition back high prior to the next falling edge of CAS* in order to specify a new burst read cycle. For burst writes, WE* would transition high to terminate a current burst write access, then back low prior to the next falling edge of CAS* to initiate another burst write access. Both RAS* and CAS* going high during a burst access will also terminate the burst access cycle placing the data drivers in a high impedance output state, and resetting the burst length counter.

A basic implementation of the device of FIG. 1 may include a fixed burst length of 4, a fixed CAS* latency of 2 and a fixed interleaved sequence of burst addresses. Further, just as fast page mode DRAMs and EDO DRAMs are available in numerous configurations including x1, x4, x8 and x16 data widths, and 1 Megabit, 4 Megabit, 16 Megabit and 64 Megabit densities; the burst access memory device of FIG. 1 may take the form of many different memory organizations.

FIG. 3 is a timing diagram for performing a burst read followed by a burst write of the device of FIG. 1. In FIG. 3, a row address is latched by the RAS* signal. WE* is low when RAS* falls for an embodiment of the design where the state of the WE* pin is used to specify a burst access cycle at RAS* time. Next, CAS* is driven low with WE* high to initiate a burst read access, and the column address is latched. The data out signals (DQ's) are not driven in the first CAS* cycle. On the second falling edge of the CAS* signal, the internal address generation circuitry advances the column address and begins another access of the array, and the first data out is driven from the device after a CAS* to data access time (T_CAC). Additional burst access cycles continue, for a device with a specified burst length of four, until the fifth falling edge of CAS* which latches a new column address for a new burst read access. WE* falling in the fifth CAS* cycle terminates the burst access, and initializes the device for additional burst accesses. The sixth falling edge of CAS* with WE* low is used to latch a new burst address, latch input data and begin a burst write access of the device. Additional data values are latched on successive CAS* falling edges until RAS* rises to terminate the burst access.

FIG. 4 is a timing diagram depicting burst write access cycles followed by burst read cycles. As in FIG. 3, the RAS* signal is used to latch the row address. The first CAS* falling edge in combination with WE* low begins a burst write access with the first data being latched. Additional data values are latched with successive CAS* falling edges, and the memory address is advanced internal to the device in

either an interleaved or sequential manner. On the fifth CAS* falling edge a new column address and associated write data are latched. The burst write access cycles continue until the WE* signal goes high in the sixth—CAS* cycle. The transition of the WE* signal terminates the burst write access. The seventh CAS* low transition latches a new column address and begins a burst read access (WE* is high). The burst read continues until RAS* rises terminating the burst cycles.

### Continuous BEDO (CBEDO)

FIG. 5 illustrates a continuous memory circuit which includes all of the features of the standard BEDO memory as described above. The continuous memory circuit, however, operates differently than the previously described BEDO memory when the row access signal (RAS*) is inactive. That is, as explained above, a burst access operation is terminated when the RAS* and the CAS* signals go high in a standard BEDO circuit. Time specifications for the BEDO circuitry dictates that the RAS* signal remain high for a minimum time of $T_{RP}$ (precharge time). Further, a minimum access time $T_{RAC}$, measured from the falling edge of RAS*, is required to access the new row. As a result, a new memory row cannot be accessed until a minimum time of $T_{RAC} + T_{RP}$ has passed following the rising edge of RAS*. Typical times for $T_{RAC}$ and $T_{RP}$ are 60 ns and 40 ns, respectively. To eliminate this 100 ns time period in which data is not being provided as output, circuitry is provided in control 139 of the memory circuit.

FIG. 5 is a schematic representation of a sixteen megabit device designed to operate in a burst access mode and incorporating the features of present invention. The device is organized as a 2 Meg×8 burst EDO DRAM having an eight bit data input/output path 110 providing data storage for 2,097,152 bytes of information in the memory array 112. An active-low row address strobe (RAS*) signal 114 is used to latch a first portion of a multiplexed memory address, from address inputs A0 through A10 116, in latch 118. The latched row address 120 is decoded in row decoder 122. The decoded row address is used to select a row of the memory array 112. An active-low column address strobe (CAS*) signal 124 is used to latch a second portion of a memory address from address inputs 116 into column address counter 126. The latched column address 128 is decoded in column address decoder 130. The decoded column address is used to select a column of the memory array 112.

In a burst read cycle, data within the memory array located at the row and column address selected by the row and column address decoders is read out of the memory array and sent along data path 132 to output latches 134. Data 110 driven from the burst EDO DRAM may be latched external to the device with a CAS* signal after a predetermined number of CAS* cycle delays (latency). Once the memory device begins to output data in a burst read cycle, the output drivers 134 will continue to drive the data lines without tri-stating the data outputs during CAS* high intervals dependent on the state of the output enable and write enable (OE* and WE*) control lines, thus allowing additional time for the system to latch the output data. Once a row and a column address are selected, additional transitions of the CAS* signal are used to advance the column address within the column address counter in a predetermined sequence. The time at which data will be valid at the outputs of the burst EDO DRAM is dependent only on the timing of the CAS* signal provided that OE* is maintained low, and WE* remains high. As with the memory of FIG. 1, the output data signal levels may be driven in accordance with

standard CMOS, TTL, LVTTL, GTL, or HSTL output level specifications. Further, the address may be advanced linearly, or in an interleaved fashion for maximum compatibility with the overall system requirements as shown in FIG. 2.

In the burst access memory device, each new column address from the column address counter is decoded and is used to access additional data within the memory array without the requirement of additional column addresses being specified on the address inputs 116. This burst sequence of data will continue for each CAS* falling edge until a predetermined number of data accesses equal to the burst length has occurred. A CAS* falling edge received after the last burst address has been generated will latch another column address from the address inputs 116 and a new burst sequence will begin. Read data is latched and output with each falling edge of CAS* after the first CAS* latency.

Input data from the input latches 134 is passed along data path 132 to the memory array where it is stored at the location selected by the row and column address decoders. As in the burst read cycle previously described, a predetermined number of burst access writes will occur without the requirement of additional column addresses being provided on the address lines 116. After the predetermined number of burst writes has occurred, a subsequent CAS* will latch a new beginning column address, and another burst read or write access will begin.

The write enable signal is used in burst access cycles to select read or write burst accesses when the initial column address for a burst cycle is latched by CAS*. WE* low at the column address latch time selects a burst write access. WE* high at the column address latch time selects a burst read access. The level of the WE* signal must remain high for read and low for write burst accesses throughout the burst access. A low to high transition within a burst write access will terminate the burst access, preventing further writes from occurring. A high to low transition on WE* within a burst read access will likewise terminate the burst read access and will place the data output 110 in a high impedance state. Transitions of the WE* signal may be locked out during critical timing periods within an access cycle in order to reduce the possibility of triggering a false write cycle. After the critical timing period, the state of WE* will determine whether a burst access continues, is initiated, or is terminated. Termination of a burst access resets the burst length counter and places the DRAM in a state to receive another burst access command.

Control circuitry 138, in addition to performing standard DRAM control functions, controls the I/O circuitry 134 and the column address counter/latch 126. The control circuitry determines when a current data burst should be terminated based upon the states of RAS* 114, CAS* 124 and WE* 136. In the standard BEDO operation described above, control circuitry 138 terminated a data burst when WE* transitioned during a burst, or when both CAS* and RAS* transitioned high. In a CBEDO operation, control circuitry 138 does not terminate a burst operation when CAS* and RAS* go high, but looks to WE* for an indication that a burst operation is to be terminated. Continuous mode circuitry 141 can be optionally provided to allow the memory device to operate in either the standard BEDO operation or a CBEDO operation.

A basic implementation of the device of FIG. 5 may include a fixed burst length of 4, a fixed CAS* latency of 2 and a fixed interleaved sequence of burst addresses. Further,

just as fast page mode DRAMs and EDO DRAMs are available in numerous configurations including x1, x4, x8 and x16 data widths, and 1 Megabit, 4 Megabit, 16 Megabit and 64 Megabit densities; the burst access memory device of FIG. 5 may take the form of many different memory organizations.

FIGS. 6a and 6b is a timing diagram for performing a continuous burst read of the device of FIG. 5. In FIGS. 6a and 6b, row address 1 is latched on the first falling edge of the RAS* signal. WE* is low when RAS* falls for an embodiment of the memory device where the state of the WE* pin is used to specify a burst access cycle at RAS* time. Next, with WE* high, CAS* is driven low to initiate a burst read access, and column address m is latched. The data out signals (DQ's) are not driven in the first CAS* cycle, but remain tri-state. On the second falling edge of the CAS* signal, data stored at column m is output on the DQ lines after a CAS* to data access time ($T_{CAC}$). On the rising edges of CAS*, the internal address generation circuitry advances the column address. Data stored at column addresses m+1, m+2, and m+3 are output on the falling edges of CAS*. After column address m is latched, the RAS* signal goes high to begin the sequence of accessing a new row. While data is being provided on the DQ lines from row 1, RAS* goes low to latch a new row address (2) from the address inputs. It will be appreciated that the RAS* signal transitioned high and low without interrupting the data output on the DQ lines. A new column address will be loaded on the last CAS* cycle of a burst, For example in FIGS. 6a and 6b, a new column address (n) is latched on the first CAS* active transition following the beginning of the RAS* cycle. The burst read operation continues uninterrupted for rows 2 and 3, and columns n, o, and p. To terminate a continuous burst read operation, the WE* signal merely has to transition high prior to a falling edge of the CAS* signal.

It will be appreciated that the read and write operations performed on a single memory row of the memory of FIG. 5 are identical to the operation of the memory of FIG. 1 as shown in FIG. 3. That is, after completing a burst read, the WE* signal transitions low and the next falling edge of CAS* latches a new column address for a burst write operation. Likewise, the timing diagram of FIG. 4 depicting burst write access cycles followed by burst read cycles can be replicated with the memory of the present invention. As such, BEDO memory devices can be replaced with CBEDO memory devices without effecting the operation of the memory support system. It will further be appreciated by those skilled in the art that the memory device of FIG. 5 can operate with burst lengths of 2, 4, 8, or full row cycles.

FIGS. 7a and 7b are provided to more clearly illustrate the advantages of the CBEDO memory over BEDO memory devices. The timing diagram of FIG. 7a shows one possible series of burst read operations on four different memory rows (R1, R2, R3 and R4) in a CBEDO memory device. FIG. 7b shows burst read operations in a BEDO memory device. On the first CAS* cycle of the first RAS* cycle, an initial column address is latched from the external address inputs. Data out is burst onto the DQ lines on the next four CAS* cycles. Once the initial column has been latched and the $T_{RAS}$ minimum specification has been satisfied, RAS* can toggle high and then low again without disrupting the burst. To avoid a premature termination of a burst, RAS* cannot transition high until after the last column associated with each row has been latched. For the example shown in FIG. 7, the second RAS* cycle cannot transition high until after the CAS* cycle which latches column C2. This ensures

the column which is to be bursted upon is latched prior to RAS* going high and terminating the burst.

As described above, a memory cell cannot be accessed until time $T_{RAC}$ following the start of a RAS cycle. It can be seen that the CBEDO memory device reduces the time needed to burst read data from several memory rows. For example, using a 66 MHz clock, a CBEDO memory operating with a 4 bit burst length can output 26 different bits of data from 7 different rows in 600 ns, while a BEDO memory device operating with a 4 bit burst length is limited to 16 bits from 4 different rows during the same time period. It is also important to point out that for multiple bursts upon the same row (RAS* cycles low and stays low for several different columns) the CBEDO and BEDO perform identically.

The CBEDO memory device of the present invention allows both RAS* and CAS* to transition high during a burst read operation without terminating the burst output stream on the DQ lines. Thus, a data burst read is continued when RAS* both transitions high and transitions low and the data drivers are not placed in a high impedance output state. While operating in a continuous burst mode, the memory device continues a burst read data while a new memory array row is being addressed. It will be understood by those skilled in the art that a word line coupled to access transistors in a memory do not need to remain active during a full burst operation. That is, each memory row word line is connected to an access transistor for each memory cell in that array row. All memory cells are, therefore, accessed at once when the word line is activated. By latching the data stored in the memory cell with latches 134, a first word line can be deactivated and another word line activated. As known to those skilled in the art, digit lines and sense amplifiers are used to read data stored in the memory cells. These bit lines must be equilibrated prior to reading a memory cell. The equilibration and memory cell access processes require a minimum specified time. These processes can be accomplished in the memory device of FIG. 5 during a continuing burst operation, as explained above, thereby increasing the data rate of the memory device.

## Conclusion

A memory device has been described which can operate at fast data rates. The memory device is a random access memory having rows and columns of memory elements. After accessing an array row, an internal memory addressing circuit allows access to numerous columns of data while requiring only one external column address. The memory device can receive and access a new memory row without interrupting the burst of data from the previously accessed row. This continuous burst operation allows for faster data rates by eliminating the need to terminate a output data while addressing a new memory row.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. For example, an external clock signal could be used to synchronize the burst access operation in place of the CAS* signal. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. A memory device comprising:
   a plurality of addressable memory elements;
   a plurality of external address inputs;
   address counter circuitry for receiving a first address on the plurality of external address inputs, and for generating a sequence of addresses in response to the first address; and
   output buffer circuitry adapted to drive a sequence of data from the memory device, the output buffer circuitry further adapted to continue to drive the sequence of data from the memory device while a new address is received by the address counter circuity.

2. The memory device of claim 1 wherein the address counter circuitry comprises:
   an address latch circuit coupled to the plurality of external address inputs; and
   a counter coupled to the address latch circuit for generating the sequence of addresses.

3. The memory device of claim 1 further comprising:
   access circuitry for reading data stored in the plurality of addressable memory elements.

4. The memory device of claim 1 further comprising:
   a write enable signal input for receiving an enable signal; and
   termination circuitry coupled to the output buffer circuitry for terminating an output of the sequence of data.

5. A burst access memory, comprising:
   a memory array having a plurality of addressable elements arranged in rows and columns;
   row access circuitry for latching a row address and accessing a row of memory elements;
   an output buffer for outputting a sequence of data stored in a plurality of columns; and
   control circuitry for controlling the output buffer and the row access circuitry, wherein a new row of memory elements can be accessed without interrupting an active output sequence.

6. The burst access memory of claim 5 further comprising:
   a write enable signal input for receiving an enable signal; and
   termination circuitry coupled to the output buffer for terminating an output of the sequence of data.

7. The burst access memory of claim 5 further comprising:
   a counter circuit for generating a sequence of column addresses.

8. The burst access memory of claim 5 further comprising:
   a column address latch circuit for latching a column address received on a plurality of external address inputs.

9. The burst access memory of claim 8 further comprising:
   a burst length counter coupled to the column address latch circuit for enabling the column address latch circuit after a sequence of data has been output.

10. A memory device comprising:
   a plurality of addressable memory elements arranged in rows and columns;
   a plurality of external address inputs;
   address circuitry for receiving row addresses and column addresses from the plurality of external address inputs;
   counter circuitry for generating a sequence of column addresses in response to a first received column address;
   row access circuitry for accessing a row of memory elements in response to a received first row address;

output buffer circuitry adapted to output a sequence of data from the memory device, the sequence of data being stored in the plurality of addressable memory elements having addresses corresponding to the sequence of addresses and the first row address; and

control circuitry for controlling the output buffer circuitry and the access circuitry, wherein a second row of memory elements can be accessed without interrupting an active output sequence of data from the first row address.

11. The memory device of claim 10 further comprising:

a write enable signal input for receiving an enable signal; and

termination circuitry coupled to the output buffer circuitry for terminating an output of the sequence of data.

12. A method of burst reading data from a memory device having a plurality of addressable memory elements arranged in rows and columns, the method comprising the steps of:

receiving a first row address;

receiving a first column address;

accessing a row of memory elements having the first row address;

generating a sequence of column addresses starting at the first column address;

outputting data stored at the sequence of column addresses;

receiving a second row address while outputting the data stored at the sequence of column addresses; and

accessing a row of memory elements having the second row address while outputting the data stored at the sequence of column addresses.

13. The method of claim 12 further including the step of:

initializing a burst read operation on an active edge of a row address latch signal.

14. The method of claim 12 further including the steps of:

receiving a signal on a write enable input; and

terminating the step of outputting data in response to the signal.

15. The method of claim 12 further including the steps of:

initializing a burst write operation on an active edge of a column address latch signal;

receiving a second column address;

generating a second sequence of column addresses starting at the second column address; and

storing data in a plurality of addressable memory elements having address corresponding to the second sequence of column addresses.

16. The method of claim 12 further including the steps of:

receiving a second column address;

accessing a row of memory elements having the second row address;

generating a second sequence of column addresses starting at the second column address; and

outputting data stored at the second sequence of column addresses.

17. The method of claim 12 wherein the sequence of data is output in response to an external clock signal.

18. A method of burst reading data from a memory device having a plurality of addressable memory elements arranged in rows and columns, the method comprising the steps of:

latching a first row address in response to an active transition of a row address latch signal;

latching a first column address in response to an active transition of a column address latch signal;

accessing a row of memory elements having the first row address;

reading data stored in a plurality of memory elements;

latching the data stored in the plurality of memory elements;

generating a sequence of column addresses starting at the first column address;

outputting the latched data in response to active transitions of the column address latch signal;

receiving a second row address while outputting the latched data; and

accessing a row of memory elements having the second row address while outputting the latched data.

19. The method of claim 18 further including the steps of:

receiving a signal on a write enable input; and

terminating the step of outputting the latched data in response to the signal.

20. The method of claim 18 wherein the step of generating a sequence of column addresses starting at the first column address comprises the step of:

advancing a counter circuit in response to in-active transitions of the column address latch signal.

* * * * *

DOCUMENT-IDENTIFIER: US 5729504 A
TITLE: Continuous burst edo memory device

---------- KWIC ----------

DEPR:
A basic implementation of the device of FIG. 1 may include a **fixed**
**burst length**
of 4, a fixed CAS* latency of 2 and a fixed interleaved sequence of
burst
addresses. Further, just as fast page mode DRAMs and EDO DRAMs are
available
in numerous configurations including x1, x4, x8 and x16 data widths,
and 1
Megabit, 4 Megabit, 16 Megabit and 64 Megabit densities; the burst
access
memory device of FIG. 1 may take the form of many different memory
organizations.

DEPR:
A basic implementation of the device of FIG. 5 may include a **fixed**
**burst length**
of 4, a fixed CAS* latency of 2 and a fixed interleaved sequence of
burst
addresses. Further, just as fast page mode DRAMs and EDO DRAMs are
available
in numerous configurations including x1, x4, x8 and x16 data widths,
and 1
Megabit, 4 Megabit, 16 Megabit and 64 Megabit densities; the burst
access
memory device of FIG. 5 may take the form of many different memory
organizations.

DEPR:
FIGS. 6a and 6b is a timing diagram for performing a continuous burst
read of
the device of FIG. 5. In FIGS. 6a and 6b, row address 1 is latched on
the
first failing edge of the RAS* signal. WE* is low when RAS* falls for
an
embodiment of the memory device where the state of the WE* pin is used
to
specify a burst access cycle at RAS* time. Next, with WE* nigh, CAS*
is driven
low to initiate a burst read access, and column address m is latched.
The data
out signals (DQ's) are not driven in the first CAS* cycle, but remain
tri-state. On the second falling edge of the CAS* signal, data stored
at
column m is output on the DQ lines after a CAS* to data access time
(T.sub.CAC). On the rising edges of CAS*, the internal address
generation
circuitry advances the column address. Data stored at column addresses

m+1,
m+2, and m+3 are output on the falling edges of CAS*. After column
address m
is latched, the RAS* signal goes high to begin the sequence of
accessing a new
row. While data is being provided on the DQ lines from row 1, RAS*
goes low to
latch a new row address (2) from the address inputs. It will be
appreciated
that the RAS* signal transitioned high and low without interrupting the
data
output on the DQ lines. A new column address will be loaded on the
last CAS*
cycle of a burst. For example in FIGS. 6a and 6b, a new column address
(n) is
latched on the first CAS* active transition following the beginning of
the RAS*
cycle. The burst read operation continues **uninterrupted** for rows 2 and
3, and
columns n, o, and p. To terminate a continuous burst read operation,
the WE*
signal merely has to transition high prior to a falling edge of the
CAS*
signal.

UNITED STATES PATENT AND TRADEMARK OFFICE

RECEIVED

JUL 1 6 2002

Technology Center 2100

Application of: Cathal G. Phelan

Serial No.: 09/504,344

Title: MEMORY DEVICE WITH FIXED LENGTH NON-INTERRUPTIBLE BURST

Filed: February 14, 2000

Attorney Docket No.: 0325.00309

Examiner: Namazi, M.

Art Unit: 2187

In Response To: Office Action mailed April 25, 2002

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on _June 26, 2002_.

By: _Mary Donna Berkley_
Mary Donna Berkley

## AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action mailed April 25, 2002 please amend the above-identified application as follows:

## IN THE CLAIMS

Please amend the claims as follows:

07/15/2002 NNOHAMM1 00000026 09504344
01 FC:103                     18.00 OP

1

1.    (AMENDED) A circuit comprising:

a memory comprising a plurality of storage elements each configured to read and write data in response to an internal address signal; and

a logic circuit configured to generate a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

2.    (AMENDED) The circuit according to claim 1, wherein said predetermined number of internal address signals is determined by a fixed burst length.

3.    (AMENDED) The circuit according to claim 1, wherein said predetermined number of internal address signals is at least 4.

4.    (AMENDED) The circuit according to claim 1, wherein said predetermined number of internal address signals is 8.

5.    (AMENDED) The circuit according to claim 2, wherein said fixed burst length is programmable.

2

6. (AMENDED) The circuit according to claim 5, wherein said fixed burst length is programmed by bond options.

7. (AMENDED) The circuit according to claim 5, wherein said fixed burst length is programmed by voltage levels on external pins.

8. (AMENDED) The circuit according to claim 1, wherein said memory comprises a static random access memory.

9. (AMENDED) The circuit according to claim 1, wherein said memory comprises a dynamic random access memory.

10. (AMENDED) The circuit according to claim 9, wherein said predetermined number of internal address signals is chosen to provide time for at least one writeback or refresh cycle.

11. (AMENDED) The circuit according to claim 1, wherein said predetermined number of internal address signals is chosen to meet predetermined criteria for sharing address and control busses.

3

12. (AMENDED) A circuit comprising:

means for reading data from and writing data to a plurality of storage elements in response to a plurality of internal address signals; and

5     means for generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.


13. (AMENDED) A method of providing a fixed burst length data transfer comprising the steps of:

accessing a memory in response to a plurality of internal address signals; and

5     generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) a control signal, wherein said generation of said predetermined number of internal address signals is non-interruptible.


14. The method according to claim 13, further comprising the step of programming said predetermined number.

4

15. The method according to claim 14, wherein said programming step is performed using bond options.

16. The method according to claim 14, wherein said programming step is performed using voltage levels.

17. (AMENDED) The method according to claim 13, further comprising the step of selecting said predetermined number to provide time for at least one writeback or refresh cycle.

18. The circuit according to claim 1, wherein said logic circuit comprises a counter configured to generate said predetermined number of internal address signals.

19. (AMENDED) The circuit according to claim 1, wherein said external address signal comprises an initial address for data transfers to and from said memory.

20. A memory device according to claim 1, wherein said circuit is an integrated circuit.

Please add the following new claim:

21.  (NEW)  The circuit according to claim 1, further comprising an address and control bus configured to present said external address signal and said one or more control signals, wherein said bus is freed up during the generation of said predetermined number of internal address signals.

6

19.    (AMENDED)  The circuit according to claim 1, wherein said external address signal comprises an initial address for data transfers to [an] and from said memory.


21.    (NEW) The circuit according to claim 1, further comprising an address and control bus configured to present said external address signal and said one or more control signals, wherein said bus is freed up during the generation of said

5      predetermined number of internal address signals.

7

## R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns an integrated circuit comprising a memory and a logic circuit. The memory may comprise a plurality of storage elements each configured to read and write data in response to an internal address signal. The logic circuit may be configured to generate a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals. The generation of the predetermined number of internal address signals is non-interruptible.

## SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims can be found in the drawing as originally filed, for example, FIGS. 5A, 5B and 6, and in the specification as originally filed, for example, on page 9, lines 3-11. As such, no new matter has been added.

## OBJECTION TO THE CLAIMS

The objection to claim 19 has been obviated by appropriate amendment and should be withdrawn.

8

## CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-20 under 35 U.S.C. §102(b) as being anticipated by Cowles is respectfully traversed and should be withdrawn.

Cowles is directed to a continuous burst EDO memory device (Title). Cowles does not disclose or suggest generating a predetermined number of internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, where the generation of the predetermined number of internal address signals is **non-interruptible**, as presently claimed.

In contrast, the present invention (claim 1) provides a circuit comprising a memory comprising a plurality of storage elements each configured to read and write data in response to an internal address signal and a logic circuit configured to generate a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals. The generation of the predetermined number of internal address signals is **non-interruptible**. Claims 12 and 13 recite similar limitations.

Assuming, *arguendo*, that the memory array 12 of Cowles is similar to the presently claimed memory (as suggested by the Office Action in section no. 6, on page 3 and for which Applicants'

9

representative does not necessarily agree), Cowles does not disclose or suggest the generation of a predetermined number of internal address signals that is non-interruptible, as presently claimed. As such, the present invention is fully patentable over the cited reference and the rejection should be withdrawn.

In particular, Cowles teaches that a continuous burst read operation can be **terminated** "merely" by a low to high transition of the write enable signal WE* prior to a falling edge of the CAS* signal (column 8, lines 32-36 of Cowles). Since the burst read operation can be **terminated**, it follows that the generation of addresses for accessing the memory array of Cowles is **interruptible**. Cowles teaches a burst read access that can be terminated. Cowles fails to disclose or suggest the generation of a predetermined number of internal address signals that is **non-interruptible**, as presently claimed. As such, the present invention is fully patentable over the cited reference and the rejection should be withdrawn.

Furthermore, Cowles teaches that a low to high transition of the WE* signal within a burst write access to the memory array 112 will **terminate** the burst access, preventing further writes from occurring (column 7, lines 36-38 of Cowles). Likewise, a high to low transition of the WE* signal within a burst read access will **terminate** the burst read access (column 7, lines 38-41 of Cowles).

10

Similarly, Cowles teaches that control circuitry can **terminate** a data burst based upon the states of signals CAS*, RAS* and WE* (column 7, lines 50-61 of Cowles). Since Cowles teaches that a burst can be terminated, Cowles fails to disclose or suggest the generation of a predetermined number of internal address signals that is **non-interruptible**, as presently claimed. As such, the present invention is fully patentable over the cited reference and the rejection should be withdrawn.

Despite the suggestion of the Office Action on page 3, paragraph no. 6, Cowles does not disclose or suggest generating a predetermined number of internal address signals that is **non-interruptible**, as presently claimed. Therefore, Cowles does not disclose or suggest each and every element of the presently pending claims, arranged as in the presently pending claims. As such, the present invention is fully patentable over the cited reference and the rejection should be withdrawn.

New claim 21 depends directly from claim 1, which is believed to be fully patentable over the cited reference, and, therefore, is also believed to be fully patentable over the cited reference.
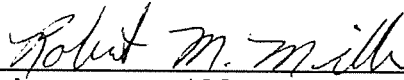
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

11

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.


Robert M. Miller
Registration No. 42,892
24025 Greater Mack, Suite 200
St. Clair Shores, MI 48080
(586) 498-0670

Dated: June 26, 2002

Docket No.: 0325.00309

12

JUL 0 9 2002

\ttoi_.y Docket: 0325.00309

IN \_APPLICATION OF:   Cathal G. Phelan

SERIAL NO.:   09/504,344

RESPONSE TRANSMITTAL AND
EXTENSION OF TIME REQUEST
(IF REQUIRED)

TITLE:   FIXED BURST MEMORIES

FILED:   February 14, 2000

EXAMINER:   Namzai, M.

ART UNIT:   2187

**RECEIVED**

**JUL 1 6 2002**

Technology Center 2100

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Sir:

Enclosed please find an amendment and a postcard along with the fee calculation below:

**FEE CALCULATION FOR ENCLOSED AND EXTENSION REQUEST (IF ANY)**

|  | Claims Remaining | Highest No. Previous | Extra    Rate | Additional Fee |
|---|---|---|---|---|
| Total Claims | 21   minus | 20   = | 0    x $ 18.00 | $ 18.00 |
| Independent Claims | 3   minus | 3   = | 0    x $ 84.00 | $ 0.00 |
| Multiple Dependent Claim First Added |  |  | + $280.00      $ 0.00 |  |

TOTAL IF NOT SMALL ENTITY .. $0.00

[ ]   SMALL ENTITY STATUS - If applicable, divide by 2 ..................... $0.00
[ ]   Verified statement enclosed, if not previously filed.

[ ]   Applicant also requests a _____ month extension of time
for response to the outstanding Office Action. The fee is ................... $0.00

[ ]   Fee set forth in 37 C.F.R. 1.17 (p) for Information Disclosure
under 37 C.F.R. 1.97 (c) ........................................ $0.00

TOTAL FEE ....................................................... $18.00

The Commissioner is hereby authorized to charge any overpayment or underpayment of the above fee associated with this Communication to Deposit Account No. 50-0541. A duplicate copy of this sheet is attached.

CHRISTOPHER P. MAIORANA, P.C.

24025 Greater Mack, Suite 200
St. Clair Shores, Michigan 48080
(586) 498-0670

By: _____
Robert M. Miller
Registration No.: 42,892

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on June 26, 2002 .

By: _____
Mary Donna Berkley

| | Application No. | Applicant(s) |
|---|---|---|
| **Office Action Summary** | 09/504,344 | Phelan |
| | Examiner<br>Mehdi Namazi | Art Unit<br>2188 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ___*three*___ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) ☒ Responsive to communication(s) filed on *Jul 9, 2002* _____ .

2a) ☒ This action is **FINAL.**      2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

**Disposition of Claims**

4) ☒ Claim(s) *1-21* _____ is/are pending in the application.

    4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-21* _____ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

**Application Papers**

9) ☒ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *02/14/00* is/are a) ☐ accepted or b) ☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

    If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All  b) ☐ Some*  c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    *See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

    a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

4) ☐ Interview Summary (PTO-413) Paper No(s). _____

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____

U. S. Patent and Trademark Office
PTO-326 (Rev. 04-01)                    Office Action Summary                    Part of Paper No. **8**

## DETAILED ACTION

1.    This office action is in response to the amendment filed

June 9, 2002.  Applicant's amendment and arguments have been

considered with results that follow.


### Claims

2.    Claims 1-20 have been presented in this application for

examination.  Claim 19 has been amended.  Claim 21 has been

added.  No claim have been canceled.  Therefore, claims 1-21

remain pending in the application.


### Response to Arguments

3.    Applicant's arguments filed on June 9, 2002 have been fully

considered.  With regard to claims 1, 12 and 13 the applicant's

arguments is not persuasive.

Examiner is agree with applicant's arguments on pages 9-11

with regard to termination of continuous burst (col. 8, lines 32-

36 or col. 7, lines 36-38, or col. 7, lines 38-41).  However, I

should point out this fact that the termination is with regard to

continuous burst and not with a row burst which represents a

fixed burst length with no interruption.  Cowles provides a

solution for avoiding termination of row burst, "To avoid a

premature termination of a burst, RSA* cannot transition high

until after the column associated with each row has been

latched".(col. 8, lines 63-65)


### Drawings

4.    The drawings are objected to under 37 CFR 1.83(a).  The

drawings must show every feature of the invention specified in

the claims.  Therefore, the "address and control bus" must be

shown or the feature(s) canceled from the claim(s).  No new

matter should be entered.

A proposed drawing correction or corrected drawings are

required in reply to the Office action to avoid abandonment of

the application.  The objection to the drawings will not be held

in abeyance.


### Specification

5.    The amendment filed on June 9, 2002 is objected to under 35

U.S.C. 132 because it introduces new matter into the disclosure.

35 U.S.C. 132 states that no amendment shall introduce new matter

into the disclosure of the invention.  The added material which

is not supported by the original disclosure is as follows:

as per claim 21, line 2, "an address and control bus" is not

supported by specification.  Page 9, lines 8 of specification

teaches two separate address bus and control bus.

Applicant is required to cancel the new matter in the reply

to this Office Action.

### Claim Rejections - 35 USC § 112

6.    The following is a quotation of the first paragraph of 35

U.S.C. 112:

> The specification shall contain a written description of the invention,
> and of the manner and process of making and using it, in such full,
> clear, concise, and exact terms as to enable any person skilled in the
> art to which it pertains, or with which it is most nearly connected, to
> make and use the same and shall set forth the best mode contemplated by
> the inventor of carrying out his invention.

7.    Claim 21 is rejected under 35 U.S.C. 112, first paragraph,

as containing subject matter which was not described in the

specification in such a way as to reasonably convey to one

skilled in the relevant art that the inventor(s), at the time the

application was filed, had possession of the claimed invention.

As per claim 21, line 2, "an address and control bus" is not

supported by specification.

### Claim Rejections - 35 USC § 102

8.    The following is a quotation of the appropriate paragraphs

of 35 U.S.C. 102 that form the basis for the rejections under

this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in
> this or a foreign country or in public use or on sale in this country, more
> than one year prior to the date of application for patent in the United
> States.

9.    Claims 1-21 are rejected under 35 U.S.C. 102(b) as being

anticipated by Cowles(U.S.Patent No. 5,729,504).

As per claims 1 and 12-13 Cowles teaches a circuit

comprising: a memory comprising a plurality of storage elements

each configured to read and write data in response to an internal

address signal(fig. 4, element 112); and  a logic circuit

configured to generate a predetermined number of said internal

address signals in response to (I) an external address signal

(col. 2, lines 20-21), (ii) a clock signal(col. 9, lines 59-61)

and (iii) one or more control signals(fig. 4, element 138,

produce control signal), wherein said generation of said

predetermined number of internal address signals is non-

interruptible(col. 8, lines 18-22).

As per claims 2, Cowles teaches wherein said predetermine number of internal address signals is determined by a fixed burst length(col. 5, lines 47-53).

As per claims 3-4 and 14, Cowles teaches wherein said predetermined number of internal address signals are 4 or 8(fig. 2, shows various burst length of 2, 4, and 8).

As per claim 5, Cowles teaches wherein said fixed burst length is programmable(col. 5, lines 31-34).

As per claims 6 and 15, Cowles teaches wherein said fixed burst length is programmed by bond options(it is well known in the art to include multiple modes of operation selected by bond options).

As per claims 7 and 16, Cowles teaches wherein said fixed burst length is programmed by voltage levels on external pins(it is inherent to have voltage levels for each burst).

As per claim 8, Cowles teaches wherein said memory comprises a static random access memory(fig. 4, element 112).

As per claim 9, Cowles teaches wherein said memory comprises a dynamic random access memory(fig. 4, element 112).

As per claims 10 and 17, Cowles teaches wherein said predetermined number of internal address signals is chosen to provide time for at least one writeback or refresh cycle(col. 8,

lines 33-36, lines 63-65)(Cowles teaches that continuous burst between rows are intruptable but row or fixed burst are not).

As per claim 11, Cowles teaches wherein the predetermined number of internal address signals is chosen to meet predetermined criteria for sharing address and control busses (col. 8, lines 18-22).

As per claim 18, Cowles teaches wherein the logic circuit comprises a counter configured to generate the predetermined number of internal address signals(fig. 4, element 126).

As per claim 19, Cowles teaches wherein the external address signal comprises an initial address for data transfers to and from the memory(col. 2, lines 21-22).

As per claim 20, Cowles teaches wherein the circuit is an integrated circuit(abstract).

As per claim 21, Cowles teaches an address and control bus configured to present the external address signal and the one or more control signals, wherein the bus is freed up during the generation of the predetermined number of internal address signal(fig. 5)(col. 6, lines 47-50).

*Conclusion*

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the

extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action

is set to expire THREE MONTHS from the mailing date of this

action.  In the event a first reply is filed within TWO MONTHS of

the mailing date of this final action and the advisory action is

not mailed until after the end of the THREE-MONTH shortened

statutory period, then the shortened statutory period will expire

on the date the advisory action is mailed, and any extension fee

pursuant to 37 CFR 1.136(a) will be calculated from the mailing

date of the advisory action.  In no event, however, will the

statutory period for reply expire later than SIX MONTHS from the

mailing date of this final action.

Any inquiry concerning this communication or earlier

communications from the examiner should be directed to Mehdi

Namazi whose telephone number is (703) 306-2758.  The examiner

can normally be reached on Monday-Thursday from 7:00 to 5:30.

If attempts to reach the examiner by telephone are

unsuccessful, the examiner's supervisor, Do Hyun yoo, can be

reached on (703) 308-4908.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-9600.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

**or faxed to:**

(703) 746-7239 (for formal communications intended for entry)

**Or:**

(703) 746-7240 (for informal or draft communications, please label PROPOSED or DRAFT )

Hand-delivered responses should be brought to Crystal Park 2,

2121 Crystal Drive,

Arlington, VA., Sixth Floor (Receptionist).

M. Namazi
October 18, 2002

Reginald D. Bragdon
REGINALD G. BRAGDON
PRIMARY EXAMINER

# Official

RECEIVED 12/16/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:        Cathal G. Phelan

Serial No.:            09/504,344

Title:                 MEMORY   DEVICE   WITH   FIXED   LENGTH   NON-INTERRUPTIBLE BURST

Filed:                 February 14, 2000

Attorney Docket No.:   0325.00309

Examiner:              Namazi, M.

Art Unit:              2187

In Response To:        Office Action mailed October 22, 2002

## CERTIFICATE OF FACSIMILE

The undersigned hereby certifies that the foregoing documents were sent via facsimile to the following: Assistant Commissioner for Patents, Washington, D.C. 20231, Examiner M. Namazi at (703) 746-7238 on December 16, 2002.

By: _Mary Donna Berkley_
    Mary Donna Berkley

## AMENDMENT AFTER FINAL

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action mailed October 22, 2002 please amend the above-identified application as follows:

## IN THE CLAIMS

Please amend the claims as follows:

1

1.    (AMENDED) A circuit comprising:

a memory comprising a plurality of storage elements each configured to read and write data in response to an internal address signal; and

a logic circuit configured to generate a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

2.    (AMENDED) The circuit according to claim 1, wherein said predetermined number of internal address signals is determined by a fixed burst length.

3.    (AMENDED) The circuit according to claim 1, wherein said predetermined number of internal address signals is at least 4.

4.    (AMENDED) The circuit according to claim 1, wherein said predetermined number of internal address signals is 8.

5.    (AMENDED) The circuit according to claim 2, wherein said fixed burst length is programmable.

2

6.    (AMENDED) The circuit according to claim 5, wherein said fixed burst length is programmed by bond options.

7.    (AMENDED) The circuit according to claim 5, wherein said fixed burst length is programmed by voltage levels on external pins.

8.    (AMENDED) The circuit according to claim 1, wherein said memory comprises a static random access memory.

9.    (AMENDED) The circuit according to claim 1, wherein said memory comprises a dynamic random access memory.

10.   (AMENDED) The circuit according to claim 9, wherein said predetermined number of internal address signals is chosen to provide time for at least one writeback or refresh cycle.

11.   (AMENDED) The circuit according to claim 1, wherein said predetermined number of internal address signals is chosen to meet predetermined criteria for sharing address and control busses.

3

16.   (AMENDED) A circuit comprising:

means for reading data from and writing data to a plurality of storage elements in response to a plurality of internal address signals; and

means for generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

17.   (AMENDED) A method of providing a fixed burst length data transfer comprising the steps of:

accessing a memory in response to a plurality of internal address signals; and

generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) a control signal, wherein said generation of said predetermined number of internal address signals is non-interruptible.

18.   The method according to claim 17, further comprising the step of programming said predetermined number.

4

19. The method according to claim 18, wherein said programming step is performed using bond options.

20. The method according to claim 18, wherein said programming step is performed using voltage levels.

21. (AMENDED) The method according to claim 17, further comprising the step of selecting said predetermined number to provide time for at least one writeback or refresh cycle.

12. The circuit according to claim 1, wherein said logic circuit comprises a counter configured to generate said predetermined number of internal address signals.

13. (AMENDED) The circuit according to claim 1, wherein said external address signal comprises an initial address for data transfers to and from said memory.

14. A memory device according to claim 1, wherein said circuit is an integrated circuit.

15. (AMENDED) The circuit according to claim 1, further comprising address and control busses configured to present said

5

## VERSION WITH MARKINGS TO SHOW CHANGES MADE

21.    (AMENDED) The circuit according to claim 1, further comprising [an] address and control [bus] busses configured to present said external address signal and said one or more control signals, wherein said [bus is] busses are freed up during the generation of said predetermined number of internal address signals.

7

## R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns an integrated circuit comprising a memory and a logic circuit. The memory may comprise a plurality of storage elements each configured to read and write data in response to an internal address signal. The logic circuit may be configured to generate a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals. The generation of the predetermined number of internal address signals is non-interruptible.

## SUPPORT FOR CLAIM AMENDMENTS

Support for the amendment to claim 21 can be found in the drawings as originally filed, for example, FIGS. 1-3, 5A and 5B, and in the specification as originally filed, for example, on page 9, lines 5-10; and page 12, lines 7-15. As such, no new matter has been added.

Furthermore, the present amendment does not raise new issues. The amendment to claim 21 merely changes the grammatically singular "address and control bus" (which Applicant's representatives believe is supported by the specification) to the

8

grammatically plural "address and control busses." The Examiner has already considered this issue (see page 4, first paragraph of the Office Action dated October 22, 2002). Therefore, the present amendment raises no new issues, and should be entered and considered.

Claim 21 has been amended. Claims 1-21 remain active in the present application.


## OBJECTION TO THE DRAWINGS

The objection to the drawings has been obviated by appropriate amendment and should be withdrawn.


## OBJECTION TO THE CLAIMS

The objection to claim 21 has been obviated by appropriate amendment and should be withdrawn.


## CLAIM REJECTIONS UNDER 35 U.S.C. §112

The objection to claim 21 under 35 U.S.C. § 112, first paragraph, has been obviated by appropriate amendment and should be withdrawn.

9

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-21 under 35 U.S.C. §102(b) as being anticipated by Cowles is respectfully traversed.

Cowles is directed to a continuous burst EDO memory device (Title). The invention disclosed by Cowles improves upon a conventional burst "extended data out" (or "BEDO") memory architecture. Despite the statements to the contrary in the Office Action dated October 22, 2002 (hereinafter "the Office Action"), Cowles does not disclose or suggest generating a predetermined number of internal address signals non-interruptibly, as presently claimed. Instead, Cowles teaches that the improvement disclosed therein relates to an ability to access a second row of memory while bursting data out of a first row (a so-called "continuous BEDO," or "CBEDO" architecture; see, e.g., FIG. 5 and col. 2, ll. 15-18, 44-48 and 55-61; col. 6, ll. 17-29; col. 7, ll. 55-64; col. 8, ll. 26-33 and 60-63; and col. 9, ll. 4-11, 21-23 and 47-52 of Cowles). This ability to access a second row of memory while bursting data out of first row has little or nothing to do with whether a "burst" can be interrupted. In fact, each of the various burst accesses disclosed by Cowles _can_ be interrupted. Consequently, it appears that any generation of internal addresses performed by the various memory architectures of Cowles can also be interrupted (see, e.g., the detailed discussion below and FIG. 4;

10

col. 5, l. 61 through col. 6, l. 9; and col. 8, ll. 37-48 of Cowles).

In contrast, the present claim 1 recites a circuit comprising a memory comprising a plurality of storage elements each configured to read and write data in response to an internal address signal and a logic circuit configured to generate non-interruptibly a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals. Claims 12 and 13 recite similar limitations. Therefore, Cowles neither discloses nor suggests the presently claimed invention.

The Office Action appears to draw a distinction between a "continuous burst" and a "row burst" as they relate to interruptibility (see, e.g., the paragraph bridging pages 2-3 of the Office Action, which appears to suggest that a continuous burst can be terminated or interrupted, while a row burst cannot). However, Cowles draws such a distinction for only one of three conditions under which a burst can be prematurely terminated or interrupted. In fact, Cowles discloses that a BEDO access can be interrupted under any of the three conditions, whereas a CBEDO access can be interrupted under only two of the three conditions. The passage relied upon in the Office Action to support the distinction between a "continuous burst" and a "row burst" is

11

actually directed to a difference between BEDO and CBEDO memories that affects only one of the three BEDO termination conditions; see the detailed discussion below.   As a result, both the "continuous burst" and "row burst" modes disclosed by Cowles are interruptible.

For example, with regard to BEDO memories, Cowles states that:

> "The time at which data will be valid at the outputs of the burst EDO DRAM is dependent only on the timing of the CAS* signal provided that OE* is maintained low, and WE* remains high."   (Col. 4, ll. 8-11 of Cowles; emphasis added.)

Furthermore, with regard to BEDO memories, Cowles also states that:

> "Once the memory device begins to output data in a burst read cycle, the output drivers 34 will continue to drive the data lines without tri-stating the data outputs during CAS* high intervals dependent on the state of the output enable 42 and write enable 36 (OE* and WE*) control lines, thus allowing additional time for the system to latch the output data."   (Col. 3, l. 65-col. 4, l. 4 of Cowles; emphasis added.)

> "The control circuit[r]y determines when a current data burst should be terminated based upon the state of RAS* 14, CAS* 24 and WE* 36."   (Col. 4, ll. 63-65 of Cowles; emphasis added.)

> "The level of the WE* signal must remain high for read and low for write burst accesses throughout the burst access. A low to high transition within a burst write access will terminate the burst access, preventing further writes from occurring. A high to low transition on WE* within a burst read access will likewise terminate the burst read access and will place the data output 10 in a high impedance state."   (Col. 5, ll. 4-10 of Cowles; emphasis added.)

12

"Both RAS* and CAS* going high during a burst access will also terminate the burst access cycle placing the data drivers in a high impedance output state, and resetting the burst length counter." (Col. 5, 11. 25-28 of Cowles; emphasis added.)

Thus, in BEDO memories, Cowles teaches that there are three conditions that will terminate a BEDO access:

1.  WE* transitioning, either from low to high or from high to low;

2.  RAS* and CAS* going high; or

3.  OE* going high (although, arguably, the state of OE* may have little, if anything, to do with generating a predetermined number of internal addresses).

The improvement to BEDO memories disclosed by Cowles and discussed above is directed to minimizing the impact of condition #2 above when accessing a different row. If we assume *arguendo* that the OE* signal disclosed by Cowles has little, if anything, to do with generation of internal addresses, there remains one condition (WE* transitioning) under which the CBEDO memory of Cowles will terminate a burst access, and thus, interrupt the generation of internal addresses, contrary to the present claims.

With regard to CBEDO memories, Cowles states that:

"The time at which data will be valid at the outputs of the burst EDO DRAM is dependent only on the timing of the CAS* signal provided that OE* is maintained low, and WE* remains high." (Col. 6, 11. 63-66 of Cowles [emphasis added]; note the similarities to col. 4, 11. 8-11 of Cowles, cited above.)

13

"Once the memory device begins to output data in a burst read cycle, the output drivers 134 will continue to drive the data lines without tri-stating the data outputs during CAS* high intervals dependent on the state of the output enable and write enable (OE* and WE*) control lines, thus allowing additional time for the system to latch the output data."   (Col. 7, ll. 53-59 of Cowles [emphasis added]; note the similarities to col. 3, l. 65-col. 4, l. 4 of Cowles, cited above.)

"The control circuit[r]y determines when a current data burst should be terminated based upon the state of RAS* 114, CAS* 124 and WE* 136."   (Col. 7, ll. 52-54 of Cowles [emphasis added]; note the similarities [including the typographical error] to col. 4, ll. 63-65 of Cowles, cited above.)

"The level of the WE* signal must remain high for read and low for write burst accesses throughout the burst access. A low to high transition within a burst write access will terminate the burst access, preventing further writes from occurring. A high to low transition on WE* within a burst read access will likewise terminate the burst read access and will place the data output 110 in a high impedance state."   (Col. 7, ll. 34-41 of Cowles [emphasis added]; note the similarities to col. 5, ll. 4-10 of Cowles, cited above.)

Thus, in CBEDO memories, Cowles teaches that at least two of the three conditions above that terminate a BEDO access (WE* transitioning and OE* going high) will also terminate a CBEDO access. Cowles is quite clear in this teaching with regard to WE* transitions:

"In a CBEDO operation, control circuitry 138 does not terminate a burst operation when CAS* and RAS* go high, but looks to WE* for an indication that a burst operation is to be terminated."   (Col. 7, ll. 57-61 of Cowles; emphasis added.)

14

"To terminate a continuous burst read operation, the WE*
signal merely has to transition high prior to a falling
edge of the CAS* signal." (Col. 8, 11. 33-36 of Cowles;
emphasis added.)

Therefore, even if we assume for the sake of argument
that OE* does not affect the generation of internal addresses,
there is still one condition under which the memories of Cowles
will interrupt (or prematurely terminate) an access: WE*
transitioning. Cowles rather explicitly teaches how such a
premature termination can take place.

For example, in FIG. 4 of Cowles, the access at "COLn" is
prematurely terminated when WE* transitions from low to high,
causing the "COLp" address to be latched and data from the "COLp"
address to be read out (see, e.g., the "ADDR," "WE" and "DQ"
waveforms in FIG. 4 and the corresponding description at col. 5, 1.
61-col. 6, 1. 9 of Cowles). Cowles correlates the read and write
operations of the BEDO memory of FIG. 3 and the CBEDO memory of
FIG. 5; i.e., in both memories, the next falling edge of CAS* after
the WE* signal transitions low latches a new column address for a
burst write operation (see, e.g., col. 8, 11. 37-48 of Cowles).
One of ordinary skill in the art would understand that the next
falling edge of CAS* after the WE* signal transitions high latches
a new column address for a burst read operation. Thus, this

15

passage further substantiates the interruptibility of both the BEDO
and CBEDO memories of Cowles.

Thus, it appears that Cowles consistently discloses at
least one condition under which the generation of internal
addresses can be interrupted, contrary to the non-interruptible
internal address generation presently claimed.

As noted in the Office Action, Cowles discloses that:

"To avoid a premature termination of a burst, RAS* cannot
transition high until after the last column associated
with each row has been latched." (Col. 8, ll. 63-65 of
Cowles.)

However, as discussed above, this statement refers to
reducing the impact of burst termination condition #2 above (see,
e.g., col. 8, l. 65-col. 9, l. 15 of Cowles), a condition that also
terminates a burst access in the BEDO memory of Cowles. More to
the point of the present claims, Cowles discloses that:

"Transitions of the WE* signal may be locked out during
critical timing periods _within an access cycle_ in order
to reduce the possibility of triggering a false write
cycle. After the critical timing period, _the state of
WE* will determine whether a burst access continues,_ is
initiated, or is terminated." (Col. 5, ll. 11-16 and
col. 7, ll. 42-47 of Cowles; emphasis added.)

These statements in Cowles apply to both the BEDO and
CBEDO memory architectures (consistent with the WE*-initiated
interrupt shown in FIG. 4 applying to both BEDO and CBEDO
memories). However, as the plain language of the passage

16

indicates, locking out transitions of the WE* signal during "critical timing periods" does not necessarily prevent termination or interruption of a burst access. Otherwise, how could the state of WE* determine whether a burst access continues? If the access was not interruptible, the state of WE* would only determine whether the next burst access is a read access or a write access; it could not determine whether the ongoing burst access continues or not.

Furthermore, Cowles provides very little guidance as to what the "critical timing periods" might be. Cowles teaches that RAS* must remain high for a minimum of about 100 ns in a BEDO memory (col. 6, ll. 18-29 of Cowles). However, other than to refer to a specified minimum time period relating to the RAS signal (see col. 8, ll. 60-63), Cowles is largely silent as to what the "critical timing periods" are for a CBEDO memory. From these indications, one of ordinary skill in the art could only surmise that "critical timing periods within an access cycle" means something considerably less than an entire access cycle. Thus, it is entirely possible, if not likely, that a burst access can be interrupted during an access cycle by a WE* transition outside the "critical timing period." Consequently, the disclosure that WE* transitions "may be locked out during critical timing periods

17

within an access cycle" does not mean that burst accesses in a BEDO and/or CBEDO memory are non-interruptible, as presently claimed.

Since Cowles teaches that a burst can be terminated during a read or write access, whether in BEDO or CBEDO mode, Cowles fails to disclose or suggest the non-interruptible generation of a predetermined number of internal address signals, as presently claimed. As such, Cowles does not disclose or suggest each and every element of the presently pending claims, arranged as in the presently pending claims. Therefore, Cowles does not anticipate the present claims, and the rejection should be withdrawn.

## CONCLUSION
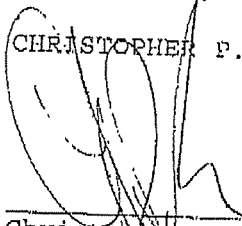
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

18

If any additional fees are due, please charge our office
Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.

Christopher P. Maiorana
Registration No. 42,829
24025 Greater Mack, Suite 200
St. Clair Shores, MI 48080
(586) 498-0670

Dated: December 16, 2002

Docket No.: 0325.00309

19

LAW OFFICES

# CHRISTOPHER P. MAIORANA, P.C.

24025 GREATER MACK, SUITE 200
ST. CLAIR SHORES, MICHIGAN 48080

CHRISTOPHER P. MAIORANA
ROBERT M. MILLER
JOHN J. KINATOWSKI

(586) 498-0670
Fax (586) 498-0673
maioranapc.com

PATENTS, TRADEMARKS
& COPYRIGHTS

## FACSIMILE MESSAGE

TO:            Examiner M. Namazi

COMPANY:       U.S. Patent and Trademark Office

RE:            Serial No.: 09/504,344 - Filed: February 14, 2000

FILE NO.:      0325.00309

FAX NO.:       (703) 746-7238

FROM:          Christopher P. Maiorana, Esq.

DATE:          December 16, 2002                    TIME: _____

**TOTAL NUMBER OF PAGES**    20    (including cover sheet)

*If you do not receive any of these pages, please telephone us at (586) 498-0670 or telefax us at (586) 498-0673.*

## COMMENTS:

*Enclosed is the following:*

*Amendment After Final (19 pages).*

LAW OFFICES

# CHRISTOPHER P. MAIORANA, P.C.

24025 GREATER MACK, SUITE 200
ST. CLAIR SHORES, MICHIGAN 48080

CHRISTOPHER P. MAIORANA
ROBERT M. MILLER
JOHN J. IGNATOWSKI

(586) 498-0670
Fax (586) 498-0673
maioranapc.com

PATENTS, TRADEMARKS
& COPYRIGHTS

December 16, 2002

Meredith McKenzie, Esq.
Manager of Intellectual Property
Cypress Semiconductor Corp.
3901 North First Street, Building 2
San Jose, CA 95134-1599

Re:    United States Patent Application Entitled:
       FIXED BURST MEMORIES
       Cypress Reference No.: CD99073
       Our Reference No.: 0325.00309
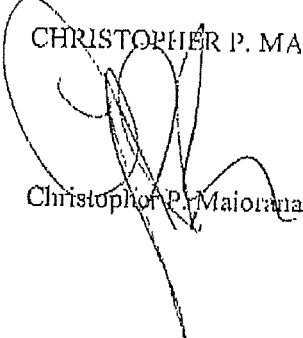
Dear Meredith:

Enclosed is a copy of the Amendment After Final and accompanying documents that were filed today, via facsimile, with the United States Patent and Trademark Office for the above-identified patent application.

Please call me if you have any questions.

Very truly yours,

CHRISTOPHER P. MAIORANA, P.C.

Christopher P. Maiorana

CPM/mdb
Enclosure
G:\CYPR0325\00309\AMEND1.ltr.wpd

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/504,344 | 02/14/2000 | Cathal G. Phelan | 0325.000309 | 7771 |

21363     7590     01/10/2003

CHRISTOPHER P. MAIORANA, P.C.
24025 GREATER MACK
SUITE 200
ST. CLAIR SHORES, MI 48080

| EXAMINER |
|---|
| NAMAZI, MEHDI |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2188 | |

DATE MAILED: 01/10/2003

*10*

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

| *Advisory Action* | Application No.<br>09/504,344 | Applicant(s)<br>Phelan | |
|---|---|---|---|
| | Examiner<br>Mehdi Namazi | Art Unit<br>2188 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

THE REPLY FILED _Dec 16, 2002_ FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid the abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

THE PERIOD FOR REPLY [check only a) or b)]

a) ☒ The period for reply expires ___three___ months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☐ The proposed amendment(s) will not be entered because:

    (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);

    (b) ☐ they raise the issue of new matter (see NOTE below);

    (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

    (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

    NOTE: _____

3. ☐ Applicant's reply has overcome the following rejection(s): _____

4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☒ The a) ☐ affidavit, b) ☐ exhibit, or c) ☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because:
*See attached paper.*

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☒ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

    The status of the claim(s) is (or will be) as follows:

    Claim(s) allowed: _____

    Claim(s) objected to: _____

    Claim(s) rejected: *1-21* _____

    Claim(s) withdrawn from consideration: _____

8. ☐ The proposed drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9. ☐ Note the attached Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

10. ☐ Other: _____

REGINALD G. BRAGDON
PRIMARY EXAMINER
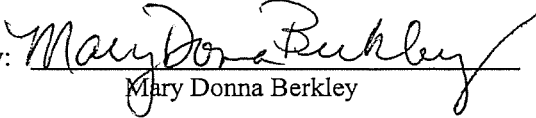
The examiner respectfully disagree with applicant's
argument.  Broadly interpreting the claim language, applicant's
invention teaches "the fixed burst length may allow the circuit
100 to operate at higher frequencies then a conventional DRAM
without needing interrupts to preform refreshes of
data."(specification , page 8, lines 12-15).  Cowles clearly
teaches a continuous (non-interruptible) stream while new rows of
the memory are accessed(abstract). In fact Cowles does not
interrupt any signal **during refreshing of data**.

# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

𝒫|(

| | |
|---|---|
| **Group Art Unit:** | 2188 |
| **Examiner:** | Namazi, M. |
| **Applicant:** | Cathal G. Phelan |
| **Serial No:** | 09/504,344 |
| **Filing Date:** | February 14, 2000 |
| **For:** | MEMORY DEVICE WITH FIXED LENGTH NON-INTERRUPT BURST |

---

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on <u>January 22, 2003</u>.

By: _Mary Donna Berkley_
Mary Donna Berkley

## NOTICE OF APPEAL

Patent and Trademark Board of Appeals and Interferences
Assistant Commissioner for Patents
Washington, DC   20231

Dear Sir:

The Applicant of the above-captioned patent application hereby appeals to the Board of Patent Appeals and Interferences from the decision dated October 22, 2002 of the Examiner finally rejecting Claims 1-21.

The payment for the appeal fee is enclosed herewith.

01/30/2003 EWILLIAM 00000002 09504344
01 FC:1401                     320.00 OP

If Applicant has not requested a sufficient extension and/or has not paid a sufficient fee for this matter, and/or for the extension necessary to prevent the abandonment of this application, please consider this as a request for an extension for the required time period and/or authorization to charge our Deposit Account No. 50-0541 for any fee which may be due.

Respectfully submitted,

By: Robert M. Miller
Robert M. Miller
Reg. No. 42,892
CHRISTOPHER P. MAIORANA, P.C.
24025 Greater Mack, Suite 200
St. Clair Shores, MI 48080
(586) 498-0670

**Date: January 22, 2003**

**Attorney Docket No.: 0325.00309**

2

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

| | | | |
|---|---|---|---|
| Applicant | Cathal G. Phelan | | |
| Application No.: | 09/504,344 | Examiner: | Namazi, M. |
| Filed: | February 14, 2000 | Art Group: | 2188 |
| For: | MEMORY DEVICE WITH FIXED LENGTH NON-INTERRUPTIBLE BURST | | |

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on _March 24, 2003_.

By: _Mary Donna Berkley_
Mary Donna Berkley

### APPEAL BRIEF

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Appellants submit, in triplicate, the following Appeal Brief pursuant to 37 C.F.R. §1.192 for

consideration by the Board of Patent Appeals and Interferences. Appellants also submit herewith

a PTO-2038 Form in the amount of $320.00 to cover the cost of filing the opening brief as required

by 37 C.F.R. §1.17(c). Please charge any additional fees or credit any overpayment to our Deposit

Account Number 50-0541.

Docket Number:0325.00309
Application No.: 09/504,344                    1

# I. REAL PARTY IN INTEREST

The real party in interest is the Assignee, Cypress Semiconductor Corporation.

# II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the Appellant, the Appellant's legal representative, or the Assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

# III. STATUS OF CLAIMS

Claims 1-21 are pending and remain rejected. The Appellant hereby appeals the rejection of claims 1-21. A copy of the currently pending claims is included in the Appendix.

# IV. STATUS OF AMENDMENTS

Appellant is appealing a final Office Action issued by the Examiner on October 22, 2002. On December 16, 2002, Appellant filed an Amendment After Final. An Advisory Action dated January 10, 2003 entered the amendment and maintained the rejection. Appellant filed a Notice of Appeal on January 22, 2003. The Notice of Appeal was received by the B.P.A.I. on January 28, 2003.

Docket Number:0325.00309
Application No.: 09/504,344

3

# V. **SUMMARY OF INVENTION**

In one embodiment, the present invention concerns a circuit (100) comprising a memory (104) and a logic circuit(102). The memory may comprise a plurality of storage elements each configured to read and write data in response to an internal address signal (ADDR_INT). The logic circuit may be configured to generate a predetermined number of the internal address signals in response to (i) an external address signal (ADDR_EXT), (ii) a clock signal (CLK) and (iii) one or more control signals (LOAD, ADV, BURST). The generation of the predetermined number of internal address signals is non-interruptible[2].

In another embodiment, the present invention concerns a circuit (100) comprising (a) means for reading data from and writing data to a plurality of storage elements in response to a plurality of internal address signals (104) and (b) means for generating a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals (102). The generation of the predetermined number of internal address signals is non-interruptible.[3]

In yet another embodiment, the present invention concerns a method of providing a fixed burst length data transfer (see the signal DQ in FIGS. 5A, 5B and 6) comprising the steps of (A) accessing a memory in response to a plurality of internal address signals and (B) generating a predetermined number of the internal address signals in response to (i) an external address signal

---

[2] See FIG. 4 and page11, lines 11-17 of the specification.

[3] *Id.*

Docket Number:0325.00309
Application No.: 09/504,344                   4

(ADDR), (ii) a clock signal (CLK) and (iii) a control signal (ADV), where the generation of the predetermined number of internal address signals is non-interruptible.[4]

## VI. ISSUE

The issue is whether claims 1-21 are patentable under 35 U.S.C. §102(b) over Cowles.[5]

## VII. GROUPING OF CLAIMS

Appellant contends that the claims of the present invention do not stand or fall together. In particular, the following groups of claims are separately patentable:

Group 1:     Claims 1, 2-5, 8, 9, and 18-20 stand together.

Group 2:     Claim 6 stands alone.

Group 3:     Claim 7 stands alone.

Group 4:     Claim 10 stands alone.

Group 5:     Claim 11 stands alone.

Group 6:     Claim 12 stands alone.

Group 7:     Claim 13, 14 and 16 stand together.

Group 8:     Claim 15 stands alone.

Group 9:     Claim 17 stands alone.

Group 10:    Claim 21 stands alone.

---

[4] See FIG. 4 and page11, lines 11-17 of the specification.

[5] U.S. Patent No. 5,729,504.

Docket Number:0325.00309
Application No.: 09/504,344                    5

Group 3 is separately patentable over groups 1 and 2 due to the added structure of group 3. In particular, the recitation in claim 7 that the fixed burst length is programmed by voltage levels at external pins provides claim 7 of group 3 with structure not recited the independent claim 1 of group 1 or the dependent claim 6 of group 2. Therefore, the dependent claim 7 in group 3 may be found patentable over the cited reference even if the independent claim 1 in group 1 and the dependent claim 6 in group 2 are not. As such, group 3 is separately patentable as compared to groups 1 and 2. Detailed reasons why claim 7 is separately distinguishable over the cited reference is provided in the Arguments below.

Group 4 is separately patentable over groups 1-3 due to the added structure of group 4. In particular, the recitation in claim 10 that the predetermined number of internal address signals is chosen to provide time for at least one writeback or refresh cycle provides claim 10 of group 4 with structure not recited the independent claim 1 of group 1 or the dependent claims 6 and 7 of groups 2 and 3. Therefore, the dependent claim 10 in group 4 may be found patentable over the cited reference even if the independent claim 1 in group 1 and the dependent claims 6 and 7 in groups 2 and 3 are not. As such, group 4 is separately patentable as compared to groups 1, 2 and 3. Detailed reasons why claim 10 is separately distinguishable over the cited reference is provided in the Arguments below.

Group 5 is separately patentable over groups 1-4 due to the added structure of group 5. In particular, the recitation in claim 11 that the predetermined number of internal address signals is chosen to meet predetermined criteria for sharing address and control busses provides claim 11 of group 5 with structure not recited the independent claim 1 of group 1 or the dependent claims 6, 7 and 10 of groups 2-4. Therefore, the dependent claim 11 in group 5 may be found patentable over

the cited reference even if the independent claim 1 in group 1 and the dependent claims 6, 7 and 10 in groups 2-4 are not. As such, group 5 is separately patentable as compared to groups 1-4. Detailed reasons why claim 11 is separately distinguishable over the cited reference is provided in the Arguments below.

The means plus function of group 6 is separately patentable over the circuit of groups 1-5 and/or the method of groups 7-10 because group 6 includes the means to perform the claimed functions. In particular, independent claim 12 in group 6 provides means for generating a predetermined number of the internal address signals where the generation of the predetermined number of internal address signals is non-interruptible not necessarily provided for in groups 1-5 and 7-10. References to the specific means plus the respective specific functions in claim 12 provide separately distinguishable limitations over the cited reference. Therefore, claim 12 may be found patentable over the cited reference even if groups 1-5 and 7-10 are not. As such, group 6 is separately patentable as compared to groups 1-5 and 7-10. Detailed reasons why claim 12 is separately distinguishable over the cited reference is provided in the Arguments below.

The method of group 7 is separately patentable over the apparatus of groups 1-5 and/or the means plus function of group 6 because group 7 involves process steps and/or specific circuit elements not necessarily in groups 1-6. In particular, independent claim 13 in group 7 provides the step of generating a predetermined number of the internal address signals where the generation of the predetermined number of internal address signals is non-interruptible. Independent claim 1 in group 1, dependent claims 6, 7, 10, and 11 in groups 2-5, and/or independent claim 12 in group 6 recite structure not necessarily provided for in group 7. Therefore, claims 1, 6, 7, 10, 11 and 12 in groups 1-6 may be found patentable over the cited reference even if claim 14 in group 7

is not. As such, group 7 is separately patentable as compared to groups 1-6. Detailed reasons why claim 14 is separately distinguishable over the cited reference is provided in the Arguments below.

Group 8 is separately patentable over group 7 due to the added step of group 8. In particular, claim 15 includes the step of programming the fixed burst length using bond options not provided for by the independent claim 13 in group 7. Therefore, the dependent claim 15 in group 8 may be found patentable over the cited reference even if the independent claim 13 in group 7 is not. As such, group 8 is separately patentable as compared to group 7. Detailed reasons why claim 15 is separately distinguishable over the cited reference is provided in the Arguments below.

Group 9 is separately patentable over group 7 due to the added step of group 9. In particular, claim 17 which includes the step of selecting the predetermined number to provide time for at least one writeback or refresh cycle. Independent claim 1 in group 1, dependent claims 6, 7, 10, and 11 in groups 2-5, and/or independent claim 12 in group 6 recite structure not necessarily provided for in group 9. Therefore, claims 1, 6, 7, 10, 11 and 12 in groups 1-6 may be found patentable over the cited reference even if claim 17 in group 9 is not. As such, group 9 is separately patentable as compared to groups 1-7. Detailed reasons why claim 17 is separately distinguishable over the cited reference is provided in the Arguments below.

Group 10 is separately patentable over group 1 due to the added structure of group 10. In particular, the recitation in claim 21 of address and control busses configured to present the external address signal and the one or more control signals, where the busses are freed up during the generation of the predetermined number of internal address signals provides claim 21 of group 10 with structure not recited the independent claim 1 of group 1. Therefore, the dependent claim 21 in group 10 may be found patentable over the cited reference even if the independent claim 1 in group

Docket Number:0325.00309
Application No.: 09/504,344                    9

1 is not. As such, group 10 is separately patentable as compared to group 1. Detailed reasons why claim 21 is separately distinguishable over the cited reference is provided in the Arguments below.

## VIII. ARGUMENTS

### A. Selected groupings of the claims are each patentable over Cowles

### 35 U.S.C. § 102

As set forth in the Final Office Action,[8] claims 1-21 are rejected under 35 U.S.C. § 102(b) as anticipated by Cowles.[9]

The Federal Circuit has stated that "[a]nticipation requires the presence in a single prior art reference disclosure of **each and every element** of the claimed invention, **arranged as in the claim.**"[10] The Federal circuit has added that the anticipation determination is viewed from one of ordinary skill in the art: "There must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention."[11] As explained herein below, because Cowles does not disclose or suggest each and every element of the presently pending claims, arranged as in the claims, Cowles does not anticipate the presently claimed invention.

---

[8] Page 5, paragraph no. 9 of the Final Office Action mailed October 22, 2002.

[9] U.S. Patent No. 5,729,504.

[10] *Brown v. 3M*, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) citing *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383, 58 USPQ2d 1286, 1291 (Fed. Cir. 2001); *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991) (Emphasis added by Appellant.).

[11] *Scripps Clinic & Research Found. V. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991).

Docket Number:0325.00309
Application No.: 09/504,344                    10

1. **Group 1 (claims 1, 2-5, 8, 9 and 18-20) is fully patentable over Cowles.**

The presently pending claim 1 provides a circuit comprising a memory and a logic circuit. The memory comprises a plurality of storage elements each configured to read and write data in response to an internal address signal. The logic circuit is configured to generate a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals. The generation of the predetermined number of internal address signals is non-interruptible.

Cowles does not disclose or suggest each and every element of the presently pending claim 1, arranged as in claim 1. Specifically, Cowles does not disclose or suggest the non-interruptible generation of the predetermined number of address signals as presently claimed. Cowles is directed to a continuous burst EDO memory device.[12] The Examiner admits that a continuous burst of Cowles is interruptible.[13] Specifically, the Examiner states that he agrees with Appellant's arguments with regard to termination of a continuous burst.[14] In particular, the Examiner admits that the interruptibility of a continuous burst is supported by the following passages in Cowles:[15]

> **To terminate** a continuous burst read operation, **the WE\* signal merely has to transition high** prior to a falling edge of the CAS\* signal. (Column 8, lines 33-36 of Cowles; emphasis added).

---

[12]Title of Cowles.

[13] See page 2, paragraph no. 3, lines 4-6 of the Office Action mailed October 22, 2002.

[14] *Id.*

[15] *Id.*

Docket Number:0325.00309
Application No.: 09/504,344                    11

The level of the WE* signal must remain high for read and low for write burst accesses throughout the burst access. **A low to high transition within a burst write access will terminate the burst access,** preventing further writes from occurring. **A high to low transition on WE* within a burst read access will likewise terminate the burst read access** and will place the data output 110 in a high impedance state. (Column 7, lines 34-41 of Cowles; emphasis added).

However, the Examiner urges that while a "continuous burst" can be terminated, a "row burst" represents a fixed burst length with no interruption.[16] Despite the position taken by the Examiner, Cowles does not appear to draw such a distinction between bursts. Specifically, with regard to a burst from a BEDO memory, Cowles states:

Once the memory device begins to output data in a burst read cycle, the output drivers 34 will continue to drive the data lines without tri-stating the data outputs during CAS* high intervals **dependent on the state of the output enable 42 and write enable 36 (OE* and WE*) control lines,** thus allowing additional time for the system to latch the output data. (Column 3, line 65 through column 4, line 4 of Cowles; emphasis added).

The control circuit[r]y determines when a current data burst should be terminated **based upon the state of RAS* 14, CAS* 24 and WE* 36.** (Column 4, lines 63-65 of Cowles; emphasis added).

**The level of the WE* signal must remain high for read and low for write burst accesses throughout the burst access.** A low to high transition within a burst write access will terminate the burst access, preventing further writes from occurring. A high to low transition on WE* within a burst read access will likewise terminate the burst read access and will place the data output 10 in a high impedance state. (Column 5, lines 4-10 of Cowles; emphasis added).

**Both RAS* and CAS* going high during a burst access will also terminate the burst access cycle** placing the data drivers in a high

---

[16] See page 2, paragraph no. 3, lines 6-9 of the Office Action mailed October 22, 2002, which appears to suggest that a continuous burst can be terminated or interrupted, while a row burst cannot.

Docket Number:0325.00309
Application No.: 09/504,344                    12

impedance output state, and resetting the burst length counter. (Column 5, lines 25-28 of Cowles; emphasis added).

Thus, in BEDO memories, Cowles clearly teaches that there are three conditions that will terminate (i.e., interrupt) a burst access:

1. WE* transitioning, either from low to high or from high to low;

2. RAS* and CAS* going high; or

3. OE* going high.[17]

Cowles is quite clear that WE* transitions will terminate both a row burst and a continuous burst access. In particular, Cowles states:

> The control circuit[r]y determines when a current data burst should be terminated based upon the states of RAS* 114, CAS* 124 and WE* 136. In the standard BEDO operation described above, **control circuitry 138 terminated a data burst when WE* transitioned during a burst**, or when both CAS* and RAS* transitioned high. In a CBEDO operation, **control circuitry 138** does not terminate a burst operation when CAS* and RAS* go high, but **looks to WE* for an indication that a burst operation is to be terminated.** (Column 7, lines 52-61 of Cowles; emphasis added).

> **To terminate** a continuous burst read operation, **the WE* signal merely has to transition high** prior to a falling edge of the CAS* signal. (Col. 8, ll. 33-36 of Cowles; emphasis added).

Therefore, since Cowles states that a transition of the signal WE* during a burst can terminate the burst in both the standard BEDO operation and in the continuous BEDO (CBEDO) operation, Cowles explicitly teaches that a premature termination of a row burst can take place.

FIG. 4 of Cowles further evidences that row bursts are interruptible. Specifically, FIG. 4 illustrates a burst access starting at column address "COLn" is terminated (i.e., interrupted)

---

[17] However, the state of OE*, arguably, may have little, if anything, to do with generating a predetermined number of internal addresses.

Docket Number:0325.00309
Application No.: 09/504,344       13

when the signal WE* transitions from low to high.[18] Furthermore, Cowles shows addressing

sequences for burst lengths of 2, 4, and 8 cycles.[19] However, FIG. 4 of Cowles illustrates a burst

access starting at the column address "COLp" is interrupted after only three cycles by the signal

RAS* rising.[20] With regard to the operations illustrated in FIG. 4, Cowles further states:

> It will be appreciated that the read and write operations performed on a single memory row of the memory of FIG. 5 are identical to the operation of the memory of FIG. 1 as shown in FIG. 3. That is, after completing a burst read, the WE* signal transitions low and the next falling edge of CAS* latches a new column address for a burst write operation. **Likewise, the timing diagram of FIG. 4 depicting burst write access cycles followed by burst read cycles can be replicated with the memory of the present invention.** As such, BEDO memory devices can be replaced with CBEDO memory devices without effecting the operation of the memory support system. It will further be appreciated by those skilled in the art that the memory device of FIG. 5 can operate with burst lengths of 2, 4, 8, or full row cycles. (Column 8, lines 37-50 of Cowles; emphasis added).

Therefore, despite the position taken by the Examiner,[21] Cowles does not disclose or suggest

generating a predetermined number of internal address signals, where the generation of the

predetermined number of internal address signals is non-interruptible, as presently claimed.

Furthermore, contrary to the position taken by the Examiner,[22] merely because

Cowles teaches that a premature termination of a burst may be avoided, it does not necessarily (or

---

[18] See column 6, lines 1-6 of Cowles.

[19] See FIG. 2, column 4, lines 14-18 and column 8, lines 48-50 of Cowles.

[20] See FIG. 4 and column 6, lines 6-9 of Cowles).

[21] See page 2, paragraph no. 3, lines 6-9 of the Office Action mailed October 22, 2002.

[22] See page 2, last two lines through page 3, line 3 of the Office Action mailed October 22, 2002.

Docket Number:0325.00309
Application No.: 09/504,344                     14

logically) follow that the burst is non-interruptible, as presently claimed. Specifically, Cowles recites that:

> To avoid a premature termination of a burst, RAS* cannot transition high until after the last column associated with each row has been latched. (Column 8, lines 63-65 of Cowles).

However, the sentence cited by the Examiner only pertains to termination of a burst in response to a transition of the signal RAS*. The passage is silent with respect to the signal WE*. As discussed above, Cowles discloses that a transition of the signal WE* during a burst can terminate the burst in both the standard BEDO operation and in the continuous BEDO (CBEDO) operation. In particular, Cowles states:

> The control circuit[r]y determines when a current data burst should be terminated based upon the states of RAS* 114, CAS* 124 and WE* 136. In the standard BEDO operation described above, **control circuitry 138 terminated a data burst when WE* transitioned during a burst**, or when both CAS* and RAS* transitioned high. In a CBEDO operation, **control circuitry 138** does not terminate a burst operation when CAS* and RAS* go high, but **looks to WE* for an indication that a burst operation is to be terminated.** (Column 7, lines 52-61 of Cowles; emphasis added).

> **To terminate** a continuous burst read operation, **the WE* signal merely has to transition high** prior to a falling edge of the CAS* signal. (Col. 8, ll. 33-36 of Cowles; emphasis added).

Cowles expressly states that the method of operation of the memory device includes (i) receiving a signal on a write enable input and (ii) terminating the step of outputting data in response to the signal.[23] Furthermore, the fact that Cowles addresses a way to **avoid** a premature termination of a burst due to the signal RAS* is acknowledgment that the burst **can** be prematurely terminated (i.e.,interrupted). Therefore, the burst is not non-interruptible, as presently claimed.

---

[23] See column 11, lines 37-41 and column 12, lines 36-40 of Cowles.

Docket Number:0325.00309
Application No.: 09/504,344                      15

Because Cowles teaches that a burst can be terminated by at least a transition of a write enable signal WE* during a read or write access, whether in a BEDO or a CBEDO operating mode, Cowles fails to disclose or suggest the **non-interruptible** generation of a predetermined number of internal address signals, as presently claimed. Therefore, Cowles does not disclose or suggest each and every element of the presently pending claim 1, arranged as in the presently pending claim 1. As such, the presently pending claim 1 is fully patentable over the cited reference[24] and the rejection should be reversed.

## 2. Group 2 (claim 6) is fully patentable over Cowles

Claim 6 depends indirectly from claim 1 and, therefore, includes the limitations of claim 1. Consequently, the arguments presented in support of the patentability of claim 1 are hereby incorporated by reference in support of claim 6. Claim 6 further recites that a fixed burst length is programmed by bond options.

Cowles does not disclose or suggest each and every element of the presently pending claim 6. Specifically, Cowles is silent regarding programming a fixed burst length by bond options.[25] In particular, the Office Action fails to point to any specific language or figure in Cowles that is considered to disclose or suggest a fixed burst length is **programmed by bond options**, as

---

[24] *Brown v. 3M*, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) citing *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383, 58 USPQ2d 1286, 1291 (Fed. Cir. 2001); *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991). *Scripps Clinic & Research Found. V. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991).

[25] Appellant's representative has downloaded an electric version of the Cowles reference and performed a search for the words "bond" and "bond option", with no such occurrences.

Docket Number:0325.00309
Application No.: 09/504,344                16

presently claimed.[26] Furthermore, the position taken in the Office Action that "it is well known in the art to include multiple modes of operation selected by bond options"[27] does not adequately address the deficiencies of Cowles to support the rejection under 35 U.S.C. § 102. In particular, the Federal Circuit has stated:

> To serve as anticipation, when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and it would be so recognized by persons of ordinary skill.[28]

Even assuming, *arguendo*, it is well known in the art to include multiple modes of operation selected by bond options as urged by the Examiner,[29] the Examiner failed to present any evidence that a person of ordinary skill would recognize bond options for programming a burst length are necessarily present in Cowles. Inherency requires certainty of results, not mere possibility.[30] Therefore, because Cowles does not disclose or suggest each and every element of the presently pending claim 6, arranged as in the present claim 6, the Examiner failed to meet the

---

[26] See page 6, lines 9-12 of the Office Action mailed October 22, 2002.

[27] See page 6, lines 9-12 of the Office Action mailed October 22, 2002.

[28] Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 20 USPQ 2d 1746, 1749 (Fed. Cir. 1991) (citations omitted) See also In re Sun, 31 USPQ 2d 1451, 1453 (Fed. Cir. 1993) (unpublished) ("under section 102(b), anticipation requires that the prior art reference disclose either expressly or under the principles of inherency, every limitation of the claim").

[29] See page 6, lines 9-12 of the Office Action mailed October 22, 2002.

[30] See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). See also, In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981).

Office's burden of factually establishing a *prima facie* case of anticipation.[31] As such, the presently

pending claim 6 is fully patentable over the cited reference and the rejection should be reversed.

### 3. Group 3 (claim 7) is fully patentable over Cowles

Claim 7 depends indirectly from claim 1 and, therefore, includes the limitations of

claim 1. Consequently, the arguments presented in support of the patentability of claim 1 are hereby

incorporated by reference in support of claim 7. Claim 7 further recites that a fixed burst length is

programmed by voltage levels on external pins.

Cowles does not disclose or suggest each and every element of the presently pending

claim 7. Specifically, Cowles is silent regarding programming a fixed burst length by **voltage levels**

**on external pins.**[32] In particular, the Examiner failed to point to any specific language or figure in

Cowles that is considered to disclose or suggest a fixed burst length is **programmed by voltage**

**levels on external pins**, as presently claimed.[33] Furthermore, the conclusory statement in the Office

Action that "it is inherent to have voltage levels for each burst"[34] does not adequately address why

---

[31] *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). (Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim). *In re* Skinner, 2 USPQ2d 1788, 1788-89 (B.P.A.I. 1986) ("[i]t is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office"). *See also Ex parte* Natale, 11 USPQ2d 1222, 1226 (B.P.A.I. 1989).

[32] Appellant's representative has downloaded an electronic version of the Cowles reference and performed a search for the words "bond" and "bond option", with no such occurrences.

[33] See page 6, lines 9-12 of the Office Action mailed October 22, 2002.

[34] See page 6, lines 9-12 of the Office Action mailed October 22, 2002.

Docket Number:0325.00309
Application No.: 09/504,344          18

a person of ordinary skill would recognize **programming a fixed burst length by voltage levels on external pins** as being **necessarily** present in Cowles. In particular,

> To serve as anticipation, when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and it would be so recognized by persons of ordinary skill.[35]

The Examiner has presented no evidence to support such a position.[36] Inherency requires certainty of results, not mere possibility.[37]

Thus, the Examiner failed to factually establish that Cowles discloses or suggests each and every element of the presently pending claim 7, arranged as in the present claim 7.[38] Therefore, the Examiner has not met the Office's burden of factually establishing a *prima facie* case of anticipation.[39] As such, claim 7 is fully patentable over Cowles and the rejection should be reversed.

---

[35] Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 20 USPQ 2d 1746, 1749 (Fed. Cir. 1991) (citations omitted) See also In re Sun, 31 USPQ 2d 1451, 1453 (Fed. Cir. 1993) (unpublished) ("under section 102(b), anticipation requires that the prior art reference disclose either expressly or under the principles of inherency, every limitation of the claim").

[36] See page 6, lines 13-15 of the Office Action.

[37] See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). See also, In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981).

[38] *Brown v. 3M*, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) citing *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383, 58 USPQ2d 1286, 1291 (Fed. Cir. 2001); *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991).

[39] *In re* Skinner, 2 USPQ2d 1788, 1788-89 (B.P.A.I. 1986). *See also Ex parte* Natale, 11 USPQ2d 1222, 1226 (B.P.A.I. 1989) ("[i]t is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office").

## 4. Group 4 (claim 10) is fully patentable over Cowles

Claim 10 depends indirectly from claim 1 and, therefore, includes the limitations of claim 1. Consequently, the arguments presented in support of the patentability of claim 1 are hereby incorporated by reference in support of claim 10. Claim 10 further recites that the predetermined number of internal address signals is chosen to provide time for at least one writeback or refresh cycle.[40]

Cowles does not disclose or suggest each and every element of the presently pending claim 10. Specifically, Cowles is silent regarding choosing the predetermined number of internal address signals to provide time for at least one writeback or refresh cycle.[41] In particular, the lines of Cowles cited by the Examiner in support of the rejection do not address choosing the predetermined number of internal address signals to provide time for at least one writeback or refresh cycle, as presently claimed.[42] The Federal Circuit has stated:

> To serve as anticipation, when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and it would be so recognized by persons of ordinary skill.[43]

---

[40] See page 3, paragraph no. 12 of the final Office Action dated May 24, 2002.

[41] Appellant's representative has downloaded an electric version of the Cowles reference and performed a search for the words "writeback" and "refresh", with no such occurrences.

[42] See page 6, line 20 through page 7, line 2 of the Office Action mailed October 22, 2002.

[43] Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 20 USPQ 2d 1746, 1749 (Fed. Cir. 1991) (citations omitted) See also In re Sun, 31 USPQ 2d 1451, 1453 (Fed. Cir. 1993) (unpublished) ("under section 102(b), anticipation requires that the prior art reference disclose either expressly or under the principles of inherency, every limitation of the claim").

Docket Number:0325.00309
Application No.: 09/504,344                    20

The Examiner failed to present any evidence that a person of ordinary skill would recognize that Cowles necessarily chooses a burst length to provide time for at least one writeback or refresh cycle.[44] Inherency requires certainty of results, not mere possibility.[45] Therefore, because Cowles does not disclose or suggest each and every element of the presently pending claim 10, arranged as in the present claim 10, the Examiner failed to meet the Office's burden of factually establishing a *prima facie* case of anticipation.[46] As such, the presently pending claim 10 is fully patentable over the cited reference and the rejection should be reversed.

### 5. Group 5 (claim 11) is fully patentable over Cowles

Claim 11 depends directly from claim 1 and, therefore, includes the limitations of claim 1. Consequently, the arguments presented in support of the patentability of claim 1 are hereby incorporated by reference in support of claim 11. Claim 11 further recites that the predetermined number of internal address signals is chosen to meet predetermined criteria for sharing address and control busses.

Cowles does not disclose or suggest each and every element of the presently pending claim 11. Specifically, Cowles is silent regarding choosing the predetermined number of internal

---

[44] See page 6, line 20 through page 7, line 2 of the Office Action mailed October 22, 2002.

[45] See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). See also, In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981).

[46] *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). (Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim). *In re* Skinner, 2 USPQ2d 1788, 1788-89 (B.P.A.I. 1986) ("[i]t is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office"). *See also Ex parte* Natale, 11 USPQ2d 1222, 1226 (B.P.A.I. 1989).

Docket Number:0325.00309
Application No.: 09/504,344                    21

address signals to meet predetermined criteria for sharing address and control busses.[47] In particular,

the lines of Cowles cited by the Examiner in support of the rejection do not address choosing the

predetermined number of internal address signals to meet predetermined criteria for sharing address

and control busses, as presently claimed.[48] The Federal Circuit has stated:

> To serve as anticipation, when the reference is silent about the
> asserted inherent characteristic, such gap in the reference may be
> filled with recourse to extrinsic evidence. Such evidence must make
> clear that the missing descriptive matter is necessarily present in the
> thing described in the reference, and it would be so recognized by
> persons of ordinary skill.[49]

The Examiner failed to present any evidence that a person of ordinary skill would

recognize that Cowles necessarily chooses a burst length to meet predetermined criteria for sharing

address and control busses.[50] Inherency requires certainty of results, not mere possibility.[51]

Therefore, because Cowles does not disclose or suggest each and every element of the presently

pending claim 11, arranged as in the present claim 11, the Examiner failed to meet the Office's

---

[47] Appellant's representative has downloaded an electric version of the Cowles reference and performed a search for the words "free," "freed up," "share" and "sharing", with no such occurrences.

[48] See page 7, lines 3-6 of the Office Action mailed October 22, 2002.

[49] Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 20 USPQ 2d 1746, 1749 (Fed. Cir. 1991) (citations omitted) See also In re Sun, 31 USPQ 2d 1451, 1453 (Fed. Cir. 1993) (unpublished) ("under section 102(b), anticipation requires that the prior art reference disclose either expressly or under the principles of inherency, every limitation of the claim").

[50] See page 7, lines 3-6 of the Office Action mailed October 22, 2002.

[51] See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). See also, In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981).

Docket Number:0325.00309
Application No.: 09/504,344                  22

burden of factually establishing a *prima facie* case of anticipation.[52] As such, the presently pending

claim 11 is fully patentable over the cited reference and the rejection should be reversed.

### 6. Group 6 (claim 12) is fully patentable over Cowles

The presently pending claim 12 provides (a) means for reading data from and writing

data to a plurality of storage elements in response to a plurality of internal address signals and (b)

means for generating a predetermined number of the internal address signals in response to (i) an

external address signal, (ii) a clock signal and (iii) one or more control signals, where the generation

of the predetermined number of internal address signals is non-interruptible.

Cowles does not disclose or suggest each and every element of the presently pending

claim 12, arranged as in claim 12. Specifically, Cowles does not disclose or suggest the

non-interruptible generation of the predetermined number of address signals, as presently claimed.

Cowles is directed to a continuous burst EDO memory device.[53] The Examiner admits that a

continuous burst of Cowles is interruptible.[54] Specifically, the Examiner states that he agrees with

Appellant's arguments with regard to termination of a continuous burst.[55] In particular, the

---

[52] *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). (Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim). *In re* Skinner, 2 USPQ2d 1788, 1788-89 (B.P.A.I. 1986) ("[i]t is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office"). *See also Ex parte* Natale, 11 USPQ2d 1222, 1226 (B.P.A.I. 1989).

[53] Title of Cowles.

[54] See page 2, paragraph no. 3, lines 4-6 of the Office Action mailed October 22, 2002.

[55] *Id.*

Docket Number:0325.00309
Application No.: 09/504,344                     23

Examiner admits that the interruptibility of a continuous burst is supported by the following passages

in Cowles:[56]

> **To terminate** a continuous burst read operation, **the WE\* signal merely has to transition high** prior to a falling edge of the CAS\* signal. (Column 8, lines 33-36 of Cowles; emphasis added).

> The level of the WE\* signal must remain high for read and low for write burst accesses throughout the burst access. **A low to high transition within a burst write access will terminate the burst access,** preventing further writes from occurring. **A high to low transition on WE\* within a burst read access will likewise terminate the burst read access** and will place the data output 110 in a high impedance state. (Column 7, lines 34-41 of Cowles; emphasis added).

However, the Examiner urges that while a "continuous burst" can be terminated, a

"row burst" represents a fixed burst length with no interruption.[57] Despite the position taken by the

Examiner, Cowles does not appear to draw such a distinction between bursts. Specifically, with

regard to a burst from a BEDO memory, Cowles states:

> Once the memory device begins to output data in a burst read cycle, the output drivers 34 will continue to drive the data lines without tri-stating the data outputs during CAS\* high intervals **dependent on the state of the output enable 42 and write enable 36 (OE\* and WE\*) control lines,** thus allowing additional time for the system to latch the output data. (Column 3, line 65 through column 4, line 4 of Cowles; emphasis added).

> The control circuit[r]y determines when a current data burst should be terminated **based upon the state of RAS\* 14, CAS\* 24 and WE\* 36.** (Column 4, lines 63-65 of Cowles; emphasis added).

---

[56] *Id.*

[57] See page 2, paragraph no. 3, lines 6-9 of the Office Action mailed October 22, 2002, which appears to suggest that a continuous burst can be terminated or interrupted, while a row burst cannot.

Docket Number:0325.00309
Application No.: 09/504,344        24

**The level of the WE\* signal must remain high for read and low for write burst accesses throughout the burst access.** A low to high transition within a burst write access will terminate the burst access, preventing further writes from occurring. A high to low transition on WE\* within a burst read access will likewise terminate the burst read access and will place the data output 10 in a high impedance state. (Column 5, lines 4-10 of Cowles; emphasis added).

**Both RAS\* and CAS\* going high during a burst access will also terminate the burst access cycle** placing the data drivers in a high impedance output state, and resetting the burst length counter. (Column 5, lines 25-28 of Cowles; emphasis added).

Thus, in BEDO memories, Cowles clearly teaches that there are three conditions that will terminate (i.e., interrupt) a burst access:

1.  WE\* transitioning, either from low to high or from high to low;

2.  RAS\* and CAS\* going high; or

3.  OE\* going high.[58]

Cowles is quite clear that WE\* transitions will terminate both a row burst and a continuous burst access. In particular, Cowles states:

The control circuit[r]y determines when a current data burst should be terminated based upon the states of RAS\* 114, CAS\* 124 and WE\* 136. In the standard BEDO operation described above, **control circuitry 138 terminated a data burst when WE\* transitioned during a burst**, or when both CAS\* and RAS\* transitioned high. In a CBEDO operation, **control circuitry 138** does not terminate a burst operation when CAS\* and RAS\* go high, but **looks to WE\* for an indication that a burst operation is to be terminated.** (Column 7, lines 52-61 of Cowles; emphasis added).

**To terminate** a continuous burst read operation, **the WE\* signal merely has to transition high** prior to a falling edge of the CAS\* signal. (Col. 8, ll. 33-36 of Cowles; emphasis added).

---

[58] However, the state of OE\*, arguably, may have little, if anything, to do with generating a predetermined number of internal addresses.

Docket Number:0325.00309
Application No.: 09/504,344                    25

Therefore, since Cowles states that a transition of the signal WE* during a burst can terminate the burst in both the standard BEDO operation and in the continuous BEDO (CBEDO) operation, Cowles explicitly teaches that a premature termination of a row burst can take place.

FIG. 4 of Cowles further evidences that row bursts are interruptible. Specifically, FIG. 4 illustrates a burst access starting at column address "COLn" is terminated (i.e., interrupted) when the signal WE* transitions from low to high.[59] Furthermore, Cowles shows addressing sequences for burst lengths of 2, 4, and 8 cycles.[60] However, FIG. 4 of Cowles illustrates a burst access starting at the column address "COLp" is interrupted after only three cycles by the signal RAS* rising.[61] With regard to the operations illustrated in FIG. 4, Cowles further states:

> It will be appreciated that the read and write operations performed on a single memory row of the memory of FIG. 5 are identical to the operation of the memory of FIG. 1 as shown in FIG. 3. That is, after completing a burst read, the WE* signal transitions low and the next falling edge of CAS* latches a new column address for a burst write operation. **Likewise, the timing diagram of FIG. 4 depicting burst write access cycles followed by burst read cycles can be replicated with the memory of the present invention.** As such, BEDO memory devices can be replaced with CBEDO memory devices without effecting the operation of the memory support system. It will further be appreciated by those skilled in the art that the memory device of FIG. 5 can operate with burst lengths of 2, 4, 8, or full row cycles. (Column 8, lines 37-50 of Cowles; emphasis added).

---

[59] See column 6, lines 1-6 of Cowles.

[60] See FIG. 2, column 4, lines 14-18 and column 8, lines 48-50 of Cowles.

[61] See FIG. 4 and column 6, lines 6-9 of Cowles.

Docket Number:0325.00309
Application No.: 09/504,344                     26

Therefore, despite the position taken by the Examiner,[62] Cowles does not disclose or suggest generating a predetermined number of internal address signals, where the generation of the predetermined number of internal address signals is non-interruptible, as presently claimed.

Furthermore, contrary to the position taken by the Examiner,[63] merely because Cowles teaches that a premature termination of a burst may be avoided, it does not necessarily (or logically) follow that the burst is non-interruptible, as presently claimed. Specifically, Cowles recites that:

> To avoid a premature termination of a burst, RAS* cannot transition high until after the last column associated with each row has been latched. (Column 8, lines 63-65 of Cowles).

However, the sentence cited by the Examiner only pertains to termination of a burst in response to a transition of the signal RAS*. The passage is silent with respect to the signal WE*. As discussed above, Cowles discloses that a transition of the signal WE* during a burst can terminate the burst in both the standard BEDO operation and in the continuous BEDO (CBEDO) operation. In particular, Cowles states:

> The control circuit[r]y determines when a current data burst should be terminated based upon the states of RAS* 114, CAS* 124 and WE* 136. In the standard BEDO operation described above, **control circuitry 138 terminated a data burst when WE* transitioned during a burst**, or when both CAS* and RAS* transitioned high. In a CBEDO operation, **control circuitry 138** does not terminate a burst operation when CAS* and RAS* go high, but **looks to WE* for an indication that a burst operation is to be terminated**. (Column 7, lines 52-61 of Cowles; emphasis added).

---

[62] See page 2, paragraph no. 3, lines 6-9 of the Office Action mailed October 22, 2002.

[63] See page 2, last two lines through page 3, line 3 of the Office Action mailed October 22, 2002.

Docket Number:0325.00309
Application No.: 09/504,344               27

> **To terminate** a continuous burst read operation, **the WE\* signal merely has to transition high** prior to a falling edge of the CAS\* signal. (Col. 8, ll. 33-36 of Cowles; emphasis added).

Cowles expressly states that the method of operation of the memory device includes (i) receiving a signal on a write enable input and (ii) terminating the step of outputting data in response to the signal.[64] Furthermore, the fact that Cowles addresses a way to **avoid** a premature termination of a burst due to the signal RAS\* is acknowledgment that the burst **can** be prematurely terminated (i.e.,interrupted). Therefore, the burst is not non-interruptible, as presently claimed.

Because Cowles teaches that a burst can be terminated by at least a transition of a write enable signal WE\* during a read or write access, whether in a BEDO or a CBEDO operating mode, Cowles fails to disclose or suggest the **non-interruptible** generation of a predetermined number of internal address signals, as presently claimed. Therefore, Cowles does not disclose or suggest each and every element of the presently pending claim 12, arranged as in the presently pending claim 12. As such, the presently pending claim 12 is fully patentable over the cited reference[65] and the rejection should be reversed.

---

[64] See column 11, lines 37-41 and column 12, lines 36-40 of Cowles.

[65] *Brown v. 3M*, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) citing *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383, 58 USPQ2d 1286, 1291 (Fed. Cir. 2001); *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991). *Scripps Clinic & Research Found. V. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991).

## 7.     Group 7 (claims 13, 14 and 16) is fully patentable over Cowles

The presently pending claim 13 provides the steps of (a) accessing a memory in response to a plurality of internal address signals and (b) generating a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, where the generation of the predetermined number of internal address signals is non-interruptible.

Cowles does not disclose or suggest each and every element of the presently pending claim 13, arranged as in claim 13.   Specifically, Cowles does not disclose or suggest the non-interruptible generation of the predetermined number of address signals as presently claimed. Cowles is directed to a continuous burst EDO memory device.[66]  The Examiner admits that a continuous burst of Cowles is interruptible.[67]  Specifically, the Examiner states that he agrees with Appellant's arguments with regard to termination of a continuous burst.[68]  In particular, the Examiner admits that the interruptibility of a continuous burst is supported by the following passages in Cowles:[69]

> **To terminate** a continuous burst read operation, **the WE\* signal merely has to transition high** prior to a falling edge of the CAS\* signal. (Column 8, lines 33-36 of Cowles; emphasis added).
>
> The level of the WE\* signal must remain high for read and low for write burst accesses throughout the burst access. **A low to high transition within a burst write access will terminate the burst**

---

[66]Title of Cowles.

[67] See page 2, paragraph no. 3, lines 4-6 of the Office Action mailed October 22, 2002.

[68] *Id.*

[69] *Id.*

Docket Number:0325.00309
Application No.: 09/504,344                 29

**access**, preventing further writes from occurring. **A high to low transition on WE\* within a burst read access will likewise terminate the burst read access** and will place the data output 110 in a high impedance state. (Column 7, lines 34-41 of Cowles; emphasis added).

However, the Examiner urges that while a "continuous burst" can be terminated, a "row burst" represents a fixed burst length with no interruption.[70] Despite the position taken by the Examiner, Cowles does not appear to draw such a distinction between bursts. Specifically, with regard to a burst from a BEDO memory, Cowles states:

> Once the memory device begins to output data in a burst read cycle, the output drivers 34 will continue to drive the data lines without tri-stating the data outputs during CAS\* high intervals **dependent on the state of the output enable 42 and write enable 36 (OE\* and WE\*) control lines**, thus allowing additional time for the system to latch the output data. (Column 3, line 65 through column 4, line 4 of Cowles; emphasis added).

> The control circuit[r]y determines when a current data burst should be terminated **based upon the state of RAS\* 14, CAS\* 24 and WE\* 36**. (Column 4, lines 63-65 of Cowles; emphasis added).

> **The level of the WE\* signal must remain high for read and low for write burst accesses throughout the burst access.** A low to high transition within a burst write access will terminate the burst access, preventing further writes from occurring. A high to low transition on WE\* within a burst read access will likewise terminate the burst read access and will place the data output 10 in a high impedance state. (Column 5, lines 4-10 of Cowles; emphasis added).

> **Both RAS\* and CAS\* going high during a burst access will also terminate the burst access cycle** placing the data drivers in a high impedance output state, and resetting the burst length counter. (Column 5, lines 25-28 of Cowles; emphasis added).

---

[70] See page 2, paragraph no. 3, lines 6-9 of the Office Action mailed October 22, 2002, which appears to suggest that a continuous burst can be terminated or interrupted, while a row burst cannot.

Docket Number:0325.00309
Application No.: 09/504,344                      30

Thus, in BEDO memories, Cowles clearly teaches that there are three conditions that will terminate (i.e., interrupt) a burst access:

1. WE* transitioning, either from low to high or from high to low;

2. RAS* and CAS* going high; or

3. OE* going high.[71]

Cowles is quite clear that WE* transitions will terminate both a row burst and a continuous burst access. In particular, Cowles states:

> The control circuit[r]y determines when a current data burst should be terminated based upon the states of RAS* 114, CAS* 124 and WE* 136. In the standard BEDO operation described above, **control circuitry 138 terminated a data burst when WE* transitioned during a burst**, or when both CAS* and RAS* transitioned high. In a CBEDO operation, **control circuitry 138** does not terminate a burst operation when CAS* and RAS* go high, but **looks to WE* for an indication that a burst operation is to be terminated**. (Column 7, lines 52-61 of Cowles; emphasis added).

> **To terminate** a continuous burst read operation, **the WE* signal merely has to transition high** prior to a falling edge of the CAS* signal. (Col. 8, ll. 33-36 of Cowles; emphasis added).

Therefore, since Cowles states that a transition of the signal WE* during a burst can terminate the burst in both the standard BEDO operation and in the continuous BEDO (CBEDO) operation, Cowles explicitly teaches that a premature termination of a row burst can take place.

FIG. 4 of Cowles further evidences that row bursts are interruptible. Specifically, FIG. 4 illustrates a burst access starting at column address "COLn" is terminated (i.e., interrupted)

---

[71] However, the state of OE*, arguably, may have little, if anything, to do with generating a predetermined number of internal addresses.

Docket Number:0325.00309
Application No.: 09/504,344                31

when the signal WE* transitions from low to high.[72] Furthermore, Cowles shows addressing

sequences for burst lengths of 2, 4, and 8 cycles.[73] However, FIG. 4 of Cowles illustrates a burst

access starting at the column address "COLp" is interrupted after only three cycles by the signal

RAS* rising.[74] With regard to the operations illustrated in FIG. 4, Cowles further states:

> It will be appreciated that the read and write operations performed on a single memory row of the memory of FIG. 5 are identical to the operation of the memory of FIG. 1 as shown in FIG. 3. That is, after completing a burst read, the WE* signal transitions low and the next falling edge of CAS* latches a new column address for a burst write operation. **Likewise, the timing diagram of FIG. 4 depicting burst write access cycles followed by burst read cycles can be replicated with the memory of the present invention.** As such, BEDO memory devices can be replaced with CBEDO memory devices without effecting the operation of the memory support system. It will further be appreciated by those skilled in the art that the memory device of FIG. 5 can operate with burst lengths of 2, 4, 8, or full row cycles. (Column 8, lines 37-50 of Cowles; emphasis added).

Therefore, despite the position taken by the Examiner,[75] Cowles does not disclose or suggest

generating a predetermined number of internal address signals, where the generation of the

predetermined number of internal address signals is non-interruptible, as presently claimed.

Furthermore, contrary to the position taken by the Examiner,[76] merely because

Cowles teaches that a premature termination of a burst may be avoided, it does not necessarily (or

---

[72] See column 6, lines 1-6 of Cowles.

[73] See FIG. 2, column 4, lines 14-18 and column 8, lines 48-50 of Cowles.

[74] See FIG. 4 and column 6, lines 6-9 of Cowles.

[75] See page 2, paragraph no. 3, lines 6-9 of the Office Action mailed October 22, 2002.

[76] See page 2, last two lines through page 3, line 3 of the Office Action mailed October 22, 2002.

Docket Number:0325.00309
Application No.: 09/504,344                    32

logically) follow that the burst is non-interruptible, as presently claimed. Specifically, Cowles recites that:

> To avoid a premature termination of a burst, RAS* cannot transition high until after the last column associated with each row has been latched. (Column 8, lines 63-65 of Cowles).

However, the sentence cited by the Examiner only pertains to termination of a burst in response to a transition of the signal RAS*. The passage is silent with respect to the signal WE*. As discussed above, Cowles discloses that a transition of the signal WE* during a burst can terminate the burst in both the standard BEDO operation and in the continuous BEDO (CBEDO) operation. In particular, Cowles states:

> The control circuit[r]y determines when a current data burst should be terminated based upon the states of RAS* 114, CAS* 124 and WE* 136. In the standard BEDO operation described above, **control circuitry 138 terminated a data burst when WE* transitioned during a burst**, or when both CAS* and RAS* transitioned high. In a CBEDO operation, **control circuitry 138** does not terminate a burst operation when CAS* and RAS* go high, but **looks to WE* for an indication that a burst operation is to be terminated**. (Column 7, lines 52-61 of Cowles; emphasis added).

> **To terminate** a continuous burst read operation, **the WE* signal merely has to transition high** prior to a falling edge of the CAS* signal. (Col. 8, ll. 33-36 of Cowles; emphasis added).

Cowles expressly states that the method of operation of the memory device includes (i) receiving a signal on a write enable input and (ii) terminating the step of outputting data in response to the signal.[77] Furthermore, the fact that Cowles addresses a way to **avoid** a premature termination of a burst due to the signal RAS* is acknowledgment that the burst **can** be prematurely terminated (i.e.,interrupted). Therefore, the burst is not non-interruptible, as presently claimed.

---

[77] See column 11, lines 37-41 and column 12, lines 36-40 of Cowles.

Because Cowles teaches that a burst can be terminated by at least a transition of a write enable signal WE* during a read or write access, whether in a BEDO or a CBEDO operating mode, Cowles fails to disclose or suggest the **non-interruptible** generation of a predetermined number of internal address signals, as presently claimed. Therefore, Cowles does not disclose or suggest each and every element of the presently pending claim 13, arranged as in the presently pending claim 13. As such, the claims of Group 7 are fully patentable over the cited reference[78] and the rejection should be reversed.

### 8.    Group 8 (claim 15) is fully patentable over Cowles

Claim 15 depends indirectly from claim 13 and, therefore, includes the limitations of claim 13. Consequently, the arguments presented in support of the patentability of claim 13 are hereby incorporated by reference in support of claim 15. Claim 15 further recites that a programming step is performed using bond options.

Cowles does not disclose or suggest each and every element of the presently pending claim 6. Specifically, Cowles is silent regarding bond options.[79] In particular, the Office Action fails to point to any specific language or figure in Cowles that is considered to disclose or suggest

---

[78] *Brown v. 3M*, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) citing *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383, 58 USPQ2d 1286, 1291 (Fed. Cir. 2001); *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991). *Scripps Clinic & Research Found. V. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991).

[79] Appellant's representative has downloaded an electric version of the Cowles reference and performed a search for the words "bond" and "bond option", with no such occurrences.

a programming step **performed using bond options**, as presently claimed.[80] Furthermore, the

position taken in the Office Action that "it is well known in the art to include multiple modes of

operation selected by bond options"[81] does not adequately address the deficiencies of Cowles to

support the rejection under 35 U.S.C. § 102. In particular, the Federal Circuit has stated:

> To serve as anticipation, when the reference is silent about the
> asserted inherent characteristic, such gap in the reference may be
> filled with recourse to extrinsic evidence. Such evidence must make
> clear that the missing descriptive matter is **necessarily present** in the
> thing described in the reference, and it would be so recognized by
> persons of ordinary skill.[82]

Even assuming, *arguendo*, it is well known in the art to include multiple modes of

operation selected by bond options as urged by the Examiner,[83] the Examiner failed to present any

evidence that a person of ordinary skill would recognize a programming step performed **using bond**

**options**, as necessarily present in Cowles. Inherency requires certainty of results, not mere

possibility.[84] Therefore, because Cowles does not disclose or suggest each and every element of the

presently pending claim 15, arranged as in the present claim 15, the Examiner has not met the

---

[80] See page 6, lines 9-12 of the Office Action mailed October 22, 2002.

[81] See page 6, lines 9-12 of the Office Action mailed October 22, 2002.

[82] Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 20 USPQ 2d 1746, 1749 (Fed. Cir. 1991) (citations omitted, emphasis added) See also In re Sun, 31 USPQ 2d 1451, 1453 (Fed. Cir. 1993) (unpublished) ("under section 102(b), anticipation requires that the prior art reference disclose either expressly or under the principles of inherency, every limitation of the claim").

[83] See page 6, lines 9-12 of the Office Action mailed October 22, 2002.

[84] See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). See also, In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981).

Docket Number:0325.00309
Application No.: 09/504,344                               35

Office's burden of factually establishing a *prima facie* case of anticipation.[85] As such, the presently pending claim 15 is fully patentable over Cowles and the rejection should be reversed.

### 9. Group 9 (claim 17) is fully patentable over Cowles

Claim 17 depends directly from claim 13 and, therefore, includes the limitations of claim 13. Consequently, the arguments presented in support of the patentability of claim 13 are hereby incorporated by reference in support of claim 17. Claim 17 further recites the step of selecting the predetermined number of internal address signals to provide time for at least one writeback or refresh cycle.[86]

Cowles does not disclose or suggest each and every element of the presently pending claim 17. Specifically, Cowles is silent regarding selecting the predetermined number of internal address signals **to provide time for at least one writeback or refresh cycle**, as presently claimed.[87] In particular, the lines of Cowles cited by the Examiner in support of the rejection do not address selecting the predetermined number of internal address signals **to provide time for at least one writeback or refresh cycle**, as presently claimed.[88] The Federal Circuit has stated:

---

[85] *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). (Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim). *In re* Skinner, 2 USPQ2d 1788, 1788-89 (B.P.A.I. 1986)("[i]t is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office"). *See also Ex parte* Natale, 11 USPQ2d 1222, 1226 (B.P.A.I. 1989) .

[86] See page 3, paragraph no. 12 of the final Office Action dated May 24, 2002.

[87] Appellant's representative has downloaded an electric version of the Cowles reference and performed a search for the words "writeback" and "refresh", with no such occurrences.

[88] See page 6, line 20 through page 7, line 2 of the Office Action mailed October 22, 2002.

Docket Number:0325.00309
Application No.: 09/504,344                          36

To serve as anticipation, when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and it would be so recognized by persons of ordinary skill.[89]

The Examiner failed to present any evidence that a person of ordinary skill would recognize that selecting a burst length to provide time for at least one writeback or refresh cycle is necessarily present in Cowles.[90] Specifically, the sections of Cowles cited by the Examiner in support of the rejection of claim 17 provide:

To terminate a continuous burst read operation, the WE* signal merely has to transition high prior to a falling edge of the CAS* signal.

\*\*\*

To avoid a premature termination of a burst, RAS* cannot transition high until after the last column associated with each row has been latched.[91]

The portions of Cowles cited by the Examiner are silent regarding selecting the predetermined number of internal address signals to provide time for at least one writeback or refresh cycle, as presently claimed. Furthermore, the Examiner provided no line of reasoning why the passages were considered to make clear that the missing descriptive matter was necessarily present in the memory

---

[89] Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 20 USPQ 2d 1746, 1749 (Fed. Cir. 1991) (citations omitted) See also In re Sun, 31 USPQ 2d 1451, 1453 (Fed. Cir. 1993) (unpublished) ("under section 102(b), anticipation requires that the prior art reference disclose either expressly or under the principles of inherency, every limitation of the claim").

[90] See page 6, line 20 through page 7, line 2 of the Office Action mailed October 22, 2002.

[91] See page 6, line 20 through page 7, line 2 of the Office Action mailed October 22, 2002 (citing column 8, lines 33-36 and 63-65 of Cowles).

Docket Number:0325.00309
Application No.: 09/504,344                      37

device of Cowles. Inherency requires certainty of results, not mere possibility.[92] Therefore, because Cowles does not disclose or suggest each and every element of the presently pending claim 17, arranged as in the present claim 17, the Examiner failed to meet the Office's burden of factually establishing a *prima facie* case of anticipation.[93] As such, the presently pending claim 17 is fully patentable over the cited reference and the rejection should be reversed.

### 10.    Group 10 (claim 21) is fully patentable over Cowles

Claim 21 depends directly from claim 1 and, therefore, includes the limitations of claim 1. Consequently, the arguments presented in support of the patentability of claim 1 are hereby incorporated by reference in support of claim 21. Claim 21 further recites that the circuit further comprises address and control busses configured to present the external address signal and one or more control signals, where the busses are **freed up during the generation of the predetermined number of internal address signals**.

Cowles does not disclose or suggest each and every element of the presently pending claim 21, arranged as in the presently pending claim 21. Specifically, Cowles is silent regarding address and control busses configured to present the external address signal and one or more control signals, where the busses are **freed up during the generation of the predetermined number of**

---

[92] See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). See also, In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981).

[93] *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). (Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim). *In re* Skinner, 2 USPQ2d 1788, 1788-89 (B.P.A.I. 1986)("[i]t is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office"). *See also Ex parte* Natale, 11 USPQ2d 1222, 1226 (B.P.A.I. 1989).

Docket Number:0325.00309
Application No.: 09/504,344                    38

**internal address signals,** as presently claimed.[94] In particular, the lines of Cowles cited by the Examiner in support of the rejection do not address address and control busses configured to present the external address signal and one or more control signals, where the busses are **freed up during the generation of the predetermined number of internal address signals,** as presently claimed.[95] Furthermore, the Federal Circuit has stated:

> To serve as anticipation, when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and it would be so recognized by persons of ordinary skill.[96]

The Examiner failed to present any evidence that a person of ordinary skill would recognize that Cowles necessarily presents address and control busses configured to present the external address signal and one or more control signals, where the busses are **freed up during the generation of the predetermined number of internal address signals,** as presently claimed.[97] Inherency requires certainty of results, not mere possibility.[98] Therefore, because Cowles does not

---

[94] Appellant's representative has downloaded an electric version of the Cowles reference and performed a search for the words "free," "freed up," "share" and "sharing", with no such occurrences.

[95] See page 7, lines 15-19 of the Office Action mailed October 22, 2002.

[96] Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 20 USPQ 2d 1746, 1749 (Fed. Cir. 1991) (citations omitted) See also In re Sun, 31 USPQ 2d 1451, 1453 (Fed. Cir. 1993) (unpublished) ("under section 102(b), anticipation requires that the prior art reference disclose either expressly or under the principles of inherency, every limitation of the claim").

[97] See page 7, lines 15-19 of the Office Action mailed October 22, 2002.

[98] See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.,* 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). See also, In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981).

Docket Number:0325.00309
Application No.: 09/504,344                    39

disclose or suggest each and every element of the presently pending claim 21, arranged as in the present claim 21, the Examiner failed to meet the Office's burden of factually establishing a *prima facie* case of anticipation.[99] As such, the presently pending claim 21 is fully patentable over the cited reference and the rejection should be reversed.

## B.    CONCLUSION
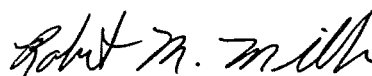
Cowles does not disclose or suggest a logic circuit configured to generate a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, where the generation of the predetermined number of internal address signals is **non-interruptible**, as presently claimed. Hence, the Examiner has clearly erred with respect to the patentability of the claimed invention. It is respectfully requested that the Board overturn the Examiner's rejection of all pending claims, and hold that the

---

[99] *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). (Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim). *In re* Skinner, 2 USPQ2d 1788, 1788-89 (B.P.A.I. 1986) ("[i]t is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office"). *See also Ex parte* Natale, 11 USPQ2d 1222, 1226 (B.P.A.I. 1989).

claims are not rendered anticipated or obvious by the cited reference. However, should the Board find the arguments herein in support of independent claims 1, 12 and/or 13 unpersuasive, the Board is respectfully requested to carefully consider the arguments set forth above in support of each of the independently patentable groups.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.

Robert M. Miller
Reg. No. 42,892

Dated: March 24, 2003

24025 Greater Mack
Suite 200
St. Clair Shores, MI 48080
(586) 498-0670

Docket Number:0325.00309
Application No.: 09/504,344                41

## IX. APPENDIX

### CLAIMS IN CURRENT FORM

1        1.        (AMENDED) A circuit comprising:

2        a memory comprising a plurality of storage elements each

3    configured to read and write data in response to an internal

4    address signal; and

5        a logic circuit configured to generate a predetermined

6    number of said internal address signals in response to (i) an

7    external address signal, (ii) a clock signal and (iii) one or more

8    control signals, wherein said generation of said predetermined

9    number of internal address signals is non-interruptible.


1        2.        (AMENDED) The circuit according to claim 1, wherein

2    said predetermined number of internal address signals is determined

3    by a fixed burst length.


1        3.        (AMENDED) The circuit according to claim 1, wherein

2    said predetermined number of internal address signals is at least

3    4.


1        4.        (AMENDED) The circuit according to claim 1, wherein

2    said predetermined number of internal address signals is 8.

1        5.    (AMENDED) The circuit according to claim 2, wherein

2    said fixed burst length is programmable.


1        6.    (AMENDED) The circuit according to claim 5, wherein

2    said fixed burst length is programmed by bond options.


1        7.    (AMENDED) The circuit according to claim 5, wherein

2    said fixed burst length is programmed by voltage levels on external

3    pins.


1        8.    (AMENDED) The circuit according to claim 1, wherein

2    said memory comprises a static random access memory.


1        9.    (AMENDED) The circuit according to claim 1, wherein

2    said memory comprises a dynamic random access memory.


1        10.    (AMENDED) The circuit according to claim 9, wherein

2    said predetermined number of internal address signals is chosen to

3    provide time for at least one writeback or refresh cycle.

1     11.   (AMENDED) The circuit according to claim 1, wherein

2     said predetermined number of internal address signals is chosen to

3     meet predetermined criteria for sharing address and control busses.


1     12.   (AMENDED) A circuit comprising:

2          means for reading data from and writing data to a

3     plurality of storage elements in response to a plurality of

4     internal address signals; and

5          means for generating a predetermined number of said

6     internal address signals in response to (i) an external address

7     signal, (ii) a clock signal and (iii) one or more control signals,

8     wherein said generation of said predetermined number of internal

9     address signals is non-interruptible.


1     13.   (AMENDED) A method of providing a fixed burst length

2     data transfer comprising the steps of:

3          accessing a memory in response to a plurality of internal

4     address signals; and

5          generating a predetermined number of said internal

6     address signals in response to (i) an external address signal, (ii)

7     a clock signal and (iii) a control signal, wherein said generation

8      of said predetermined number of internal address signals is non-interruptible.

1          14.   The method according to claim 13, further comprising
2      the step of programming said predetermined number.

1          15.   The method according to claim 14, wherein said
2      programming step is performed using bond options.

1          16.   The method according to claim 14, wherein said
2      programming step is performed using voltage levels.

1          17.   (AMENDED) The method according to claim 13, further
2      comprising the step of selecting said predetermined number to
3      provide time for at least one writeback or refresh cycle.

1          18.   The circuit according to claim 1, wherein said logic
2      circuit comprises a counter configured to generate said
3      predetermined number of internal address signals.

1          19.   (AMENDED) The circuit according to claim 1, wherein
2      said external address signal comprises an initial address for data
3      transfers to and from said memory.

1        20.  A memory device according to claim 1, wherein said

2    circuit is an integrated circuit.


1        21.  (AMENDED) The circuit according to claim 1, further

2    comprising address and control busses configured to present said

3    external address signal and said one or more control signals,

4    wherein said busses are freed up during the generation of said

5    predetermined number of internal address signals.

Our Docket No.: 0325.00309

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

| | | | |
|---|---|---|---|
| Applicant | Cathal G. Phelan | | |
| Application No.: | 09/504,344 | Examiner: | Namazi, M. |
| Filed: | February 14, 2000 | Art Group: | 2188 |
| For: | MEMORY DEVICE WITH FIXED LENGTH NON-INTERRUPTIBLE BURST | | |

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on __March 24, 2003__.

By: _Mary Donna Berkley_
Mary Donna Berkley

### APPEAL BRIEF

Assistant Commissioner for Patents
Washington, D.C. 20231

**RECEIVED**

MAR 3 1 2003

Technology Center 2100

Dear Sir:

Appellants submit, in triplicate, the following Appeal Brief pursuant to 37 C.F.R. §1.192 for

consideration by the Board of Patent Appeals and Interferences. Appellants also submit herewith

a PTO-2038 Form in the amount of $320.00 to cover the cost of filing the opening brief as required

by 37 C.F.R. §1.17(c). Please charge any additional fees or credit any overpayment to our Deposit

Account Number 50-0541.

Docket Number:0325.00309
Application No.: 09/504,344                    1

# TABLE OF CONTENTS

---

[1] U.S. Patent No. 5, 729,504.

Docket Number:0325.00309
Application No.: 09/504,344                     2

# I. **REAL PARTY IN INTEREST**

The real party in interest is the Assignee, Cypress Semiconductor Corporation.

# II. **RELATED APPEALS AND INTERFERENCES**

There are no related appeals or interferences known to the Appellant, the Appellant's

legal representative, or the Assignee which will directly affect or be directly affected by or have a

bearing on the Board's decision in the pending appeal.

# III. **STATUS OF CLAIMS**

Claims 1-21 are pending and remain rejected. The Appellant hereby appeals the

rejection of claims 1-21. A copy of the currently pending claims is included in the Appendix.

# IV. **STATUS OF AMENDMENTS**

Appellant is appealing a final Office Action issued by the Examiner on October 22,

2002. On December 16, 2002, Appellant filed an Amendment After Final. An Advisory Action

dated January 10, 2003 entered the amendment and maintained the rejection. Appellant filed a

Notice of Appeal on January 22, 2003. The Notice of Appeal was received by the B.P.A.I. on

January 28, 2003.

# V. **SUMMARY OF INVENTION**

In one embodiment, the present invention concerns a circuit (100) comprising a memory (104) and a logic circuit(102). The memory may comprise a plurality of storage elements each configured to read and write data in response to an internal address signal (ADDR_INT). The logic circuit may be configured to generate a predetermined number of the internal address signals in response to (i) an external address signal (ADDR_EXT), (ii) a clock signal (CLK) and (iii) one or more control signals (LOAD, ADV, BURST). The generation of the predetermined number of internal address signals is non-interruptible[2].

In another embodiment, the present invention concerns a circuit (100) comprising (a) means for reading data from and writing data to a plurality of storage elements in response to a plurality of internal address signals (104) and (b) means for generating a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals (102). The generation of the predetermined number of internal address signals is non-interruptible.[3]

In yet another embodiment, the present invention concerns a method of providing a fixed burst length data transfer (see the signal DQ in FIGS. 5A, 5B and 6) comprising the steps of (A) accessing a memory in response to a plurality of internal address signals and (B) generating a predetermined number of the internal address signals in response to (i) an external address signal

---

[2] See FIG. 4 and page11, lines 11-17 of the specification.

[3] *Id.*

Docket Number:0325.00309
Application No.: 09/504,344                    4

(ADDR), (ii) a clock signal (CLK) and (iii) a control signal (ADV), where the generation of the predetermined number of internal address signals is non-interruptible.[4]

# VI. ISSUE

The issue is whether claims 1-21 are patentable under 35 U.S.C. §102(b) over Cowles.[5]

# VII. GROUPING OF CLAIMS

Appellant contends that the claims of the present invention do not stand or fall together. In particular, the following groups of claims are separately patentable:

Group 1:     Claims 1, 2-5, 8, 9, and 18-20 stand together.

Group 2:     Claim 6 stands alone.

Group 3:     Claim 7 stands alone.

Group 4:     Claim 10 stands alone.

Group 5:     Claim 11 stands alone.

Group 6:     Claim 12 stands alone.

Group 7:     Claim 13, 14 and 16 stand together.

Group 8:     Claim 15 stands alone.

Group 9:     Claim 17 stands alone.

Group 10:    Claim 21 stands alone.

---

[4] See FIG. 4 and page11, lines 11-17 of the specification.

[5] U.S. Patent No. 5,729,504.

Docket Number:0325.00309
Application No.: 09/504,344                 5

The claim(s) in each group is(are) separately patentable from the claim(s) in any other groups. During prosecution, each independent and dependent claim is considered to be separately patentable over every other claim.[6] As such, each of the above groups is considered to be separately patentable over every other group.[7]

In particular, groups 1-5 concern a circuit, group 6 concerns a means plus function and groups 7-10 concern a method. Since the means plus function claim of group 6 and the method claims of groups 7-10 do not necessarily encompass all the structure comprising the circuit of the claims of any of the groups 1-5, groups 1-5 are separately patentable with respect to groups 6-10. Detailed reasons why the groups are patentable over the cited references are provided in the Arguments below.

Group 2 is separately patentable over group 1 due to the added structure of group 2. In particular, the recitation in claim 6 that the fixed burst length is programmed by bond options provides claim 6 of group 2 with structure not recited the independent claim 1 of group 1. Therefore, the dependent claim 2 in group 2 may be found patentable over the cited reference even if the independent claim 1 in group 1 is not. As such, group 2 is separately patentable as compared to group 1. Detailed reasons why claim 2 is separately distinguishable over the cited reference is provided in the Arguments below.

---

[6] See, e.g., *Rowe v. Dror*, 42 USPQ2d 1550, 1552 (Fed. Cir. 1997), *Preemption Devices, Inc. v. Minnesota Mining and Manufacturing Company*, 221 USPQ 841, 843 (Fed. Cir. 1984), and *Jones v. Hardy*, 727 F.2d 1524, 1528, 220 USPQ 1021, 1024 (Fed. Cir. 1984) (It is well established that each claim in a patent constitutes a separate invention.).

[7] Manual of Patent Examining Procedure (M.P.E.P.), Eighth Edition, August, 2001, §1206.

Group 3 is separately patentable over groups 1 and 2 due to the added structure of group 3. In particular, the recitation in claim 7 that the fixed burst length is programmed by voltage levels at external pins provides claim 7 of group 3 with structure not recited the independent claim 1 of group 1 or the dependent claim 6 of group 2. Therefore, the dependent claim 7 in group 3 may be found patentable over the cited reference even if the independent claim 1 in group 1 and the dependent claim 6 in group 2 are not. As such, group 3 is separately patentable as compared to groups 1 and 2. Detailed reasons why claim 7 is separately distinguishable over the cited reference is provided in the Arguments below.

Group 4 is separately patentable over groups 1-3 due to the added structure of group 4. In particular, the recitation in claim 10 that the predetermined number of internal address signals is chosen to provide time for at least one writeback or refresh cycle provides claim 10 of group 4 with structure not recited the independent claim 1 of group 1 or the dependent claims 6 and 7 of groups 2 and 3. Therefore, the dependent claim 10 in group 4 may be found patentable over the cited reference even if the independent claim 1 in group 1 and the dependent claims 6 and 7 in groups 2 and 3 are not. As such, group 4 is separately patentable as compared to groups 1, 2 and 3. Detailed reasons why claim 10 is separately distinguishable over the cited reference is provided in the Arguments below.

Group 5 is separately patentable over groups 1-4 due to the added structure of group 5. In particular, the recitation in claim 11 that the predetermined number of internal address signals is chosen to meet predetermined criteria for sharing address and control busses provides claim 11 of group 5 with structure not recited the independent claim 1 of group 1 or the dependent claims 6, 7 and 10 of groups 2-4. Therefore, the dependent claim 11 in group 5may be found patentable over

the cited reference even if the independent claim 1 in group 1 and the dependent claims 6, 7 and 10 in groups 2-4 are not. As such, group 5 is separately patentable as compared to groups 1-4. Detailed reasons why claim 11 is separately distinguishable over the cited reference is provided in the Arguments below.

The means plus function of group 6 is separately patentable over the circuit of groups 1-5 and/or the method of groups 7-10 because group 6 includes the means to perform the claimed functions. In particular, independent claim 12 in group 6 provides means for generating a predetermined number of the internal address signals where the generation of the predetermined number of internal address signals is non-interruptible not necessarily provided for in groups 1-5 and 7-10. References to the specific means plus the respective specific functions in claim 12 provide separately distinguishable limitations over the cited reference. Therefore, claim 12 may be found patentable over the cited reference even if groups 1-5 and 7-10 are not. As such, group 6 is separately patentable as compared to groups 1-5 and 7-10. Detailed reasons why claim 12 is separately distinguishable over the cited reference is provided in the Arguments below.

The method of group 7 is separately patentable over the apparatus of groups 1-5 and/or the means plus function of group 6 because group 7 involves process steps and/or specific circuit elements not necessarily in groups 1-6. In particular, independent claim 13 in group 7 provides the step of generating a predetermined number of the internal address signals where the generation of the predetermined number of internal address signals is non-interruptible. Independent claim 1 in group 1, dependent claims 6, 7, 10, and 11 in groups 2-5, and/or independent claim 12 in group 6 recite structure not necessarily provided for in group 7. Therefore, claims 1, 6, 7, 10, 11 and 12 in groups 1-6 may be found patentable over the cited reference even if claim 14 in group 7

Docket Number:0325.00309
Application No.: 09/504,344      8

is not. As such, group 7 is separately patentable as compared to groups 1-6. Detailed reasons why claim 14 is separately distinguishable over the cited reference is provided in the Arguments below.

Group 8 is separately patentable over group 7 due to the added step of group 8. In particular, claim 15 includes the step of programming the fixed burst length using bond options not provided for by the independent claim 13 in group 7. Therefore, the dependent claim 15 in group 8 may be found patentable over the cited reference even if the independent claim 13 in group 7 is not. As such, group 8 is separately patentable as compared to group 7. Detailed reasons why claim 15 is separately distinguishable over the cited reference is provided in the Arguments below.

Group 9 is separately patentable over group 7 due to the added step of group 9. In particular, claim 17 which includes the step of selecting the predetermined number to provide time for at least one writeback or refresh cycle. Independent claim 1 in group 1, dependent claims 6, 7, 10, and 11 in groups 2-5, and/or independent claim 12 in group 6 recite structure not necessarily provided for in group 9. Therefore, claims 1, 6, 7, 10, 11 and 12 in groups 1-6 may be found patentable over the cited reference even if claim 17 in group 9 is not. As such, group 9 is separately patentable as compared to groups 1-7. Detailed reasons why claim 17 is separately distinguishable over the cited reference is provided in the Arguments below.

Group 10 is separately patentable over group 1 due to the added structure of group 10. In particular, the recitation in claim 21 of address and control busses configured to present the external address signal and the one or more control signals, where the busses are freed up during the generation of the predetermined number of internal address signals provides claim 21 of group 10 with structure not recited the independent claim 1 of group 1. Therefore, the dependent claim 21 in group 10 may be found patentable over the cited reference even if the independent claim 1 in group

1 is not. As such, group 10 is separately patentable as compared to group 1. Detailed reasons why

claim 21 is separately distinguishable over the cited reference is provided in the Arguments below.

## VIII. <u>ARGUMENTS</u>

A.    <u>Selected groupings of the claims are each patentable over Cowles</u>

### <u>35 U.S.C. § 102</u>

As set forth in the Final Office Action,[8] claims 1-21 are rejected under 35 U.S.C. §

102(b) as anticipated by Cowles.[9]

The Federal Circuit has stated that "[a]nticipation requires the presence in a single

prior art reference disclosure of **each and every element** of the claimed invention, **arranged as in**

**the claim.**"[10] The Federal circuit has added that the anticipation determination is viewed from one

of ordinary skill in the art: "There must be no difference between the claimed invention and the

reference disclosure, as viewed by a person of ordinary skill in the field of the invention."[11] As

explained herein below, because Cowles does not disclose or suggest each and every element of the

presently pending claims, arranged as in the claims, Cowles does not anticipate the presently claimed

invention.

---

[8] Page 5, paragraph no. 9 of the Final Office Action mailed October 22, 2002.

[9] U.S. Patent No. 5,729,504.

[10] *Brown v. 3M*, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) citing *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383, 58 USPQ2d 1286, 1291 (Fed. Cir. 2001); *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991) (Emphasis added by Appellant.).

[11] *Scripps Clinic & Research Found. V. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991).

Docket Number:0325.00309
Application No.: 09/504,344                                   10

## 1. Group 1 (claims 1, 2-5, 8, 9 and 18-20) is fully patentable over Cowles.

The presently pending claim 1 provides a circuit comprising a memory and a logic circuit. The memory comprises a plurality of storage elements each configured to read and write data in response to an internal address signal. The logic circuit is configured to generate a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals. The generation of the predetermined number of internal address signals is non-interruptible.

Cowles does not disclose or suggest each and every element of the presently pending claim 1, arranged as in claim 1. Specifically, Cowles does not disclose or suggest the non-interruptible generation of the predetermined number of address signals as presently claimed. Cowles is directed to a continuous burst EDO memory device.[12] The Examiner admits that a continuous burst of Cowles is interruptible.[13] Specifically, the Examiner states that he agrees with Appellant's arguments with regard to termination of a continuous burst.[14] In particular, the Examiner admits that the interruptibility of a continuous burst is supported by the following passages in Cowles:[15]

> **To terminate** a continuous burst read operation, **the WE\* signal merely has to transition high** prior to a falling edge of the CAS\* signal. (Column 8, lines 33-36 of Cowles; emphasis added).

---

[12]Title of Cowles.

[13] See page 2, paragraph no. 3, lines 4-6 of the Office Action mailed October 22, 2002.

[14] *Id.*

[15] *Id.*

Docket Number:0325.00309
Application No.: 09/504,344                    11

The level of the WE* signal must remain high for read and low for write burst accesses throughout the burst access. **A low to high transition within a burst write access will terminate the burst access,** preventing further writes from occurring. **A high to low transition on WE* within a burst read access will likewise terminate the burst read access** and will place the data output 110 in a high impedance state. (Column 7, lines 34-41 of Cowles; emphasis added).

However, the Examiner urges that while a "continuous burst" can be terminated, a "row burst" represents a fixed burst length with no interruption.[16] Despite the position taken by the Examiner, Cowles does not appear to draw such a distinction between bursts. Specifically, with regard to a burst from a BEDO memory, Cowles states:

Once the memory device begins to output data in a burst read cycle, the output drivers 34 will continue to drive the data lines without tri-stating the data outputs during CAS* high intervals **dependent on the state of the output enable 42 and write enable 36 (OE* and WE*) control lines,** thus allowing additional time for the system to latch the output data. (Column 3, line 65 through column 4, line 4 of Cowles; emphasis added).

The control circuit[r]y determines when a current data burst should be terminated **based upon the state of RAS* 14, CAS* 24 and WE* 36.** (Column 4, lines 63-65 of Cowles; emphasis added).

**The level of the WE* signal must remain high for read and low for write burst accesses throughout the burst access.** A low to high transition within a burst write access will terminate the burst access, preventing further writes from occurring. A high to low transition on WE* within a burst read access will likewise terminate the burst read access and will place the data output 10 in a high impedance state. (Column 5, lines 4-10 of Cowles; emphasis added).

**Both RAS* and CAS* going high during a burst access will also terminate the burst access cycle** placing the data drivers in a high

---

[16] See page 2, paragraph no. 3, lines 6-9 of the Office Action mailed October 22, 2002, which appears to suggest that a continuous burst can be terminated or interrupted, while a row burst cannot.

Docket Number:0325.00309
Application No.: 09/504,344                    12

impedance output state, and resetting the burst length counter. (Column 5, lines 25-28 of Cowles; emphasis added).

Thus, in BEDO memories, Cowles clearly teaches that there are three conditions that will terminate (i.e., interrupt) a burst access:

1.    WE* transitioning, either from low to high or from high to low;

2.    RAS* and CAS* going high; or

3.    OE* going high.[17]

Cowles is quite clear that WE* transitions will terminate both a row burst and a continuous burst access. In particular, Cowles states:

> The control circuit[r]y determines when a current data burst should be terminated based upon the states of RAS* 114, CAS* 124 and WE* 136. In the standard BEDO operation described above, **control circuitry 138 terminated a data burst when WE* transitioned during a burst**, or when both CAS* and RAS* transitioned high. In a CBEDO operation, **control circuitry 138** does not terminate a burst operation when CAS* and RAS* go high, but **looks to WE* for an indication that a burst operation is to be terminated**. (Column 7, lines 52-61 of Cowles; emphasis added).

> **To terminate** a continuous burst read operation, **the WE* signal merely has to transition high** prior to a falling edge of the CAS* signal. (Col. 8, ll. 33-36 of Cowles; emphasis added).

Therefore, since Cowles states that a transition of the signal WE* during a burst can terminate the burst in both the standard BEDO operation and in the continuous BEDO (CBEDO) operation, Cowles explicitly teaches that a premature termination of a row burst can take place.

FIG. 4 of Cowles further evidences that row bursts are interruptible. Specifically, FIG. 4 illustrates a burst access starting at column address "COLn" is terminated (i.e., interrupted)

---

[17] However, the state of OE*, arguably, may have little, if anything, to do with generating a predetermined number of internal addresses.

Docket Number:0325.00309
Application No.: 09/504,344                    13

when the signal WE* transitions from low to high.[18] Furthermore, Cowles shows addressing sequences for burst lengths of 2, 4, and 8 cycles.[19] However, FIG. 4 of Cowles illustrates a burst access starting at the column address "COLp" is interrupted after only three cycles by the signal RAS* rising.[20] With regard to the operations illustrated in FIG. 4, Cowles further states:

> It will be appreciated that the read and write operations performed on a single memory row of the memory of FIG. 5 are identical to the operation of the memory of FIG. 1 as shown in FIG. 3. That is, after completing a burst read, the WE* signal transitions low and the next falling edge of CAS* latches a new column address for a burst write operation. **Likewise, the timing diagram of FIG. 4 depicting burst write access cycles followed by burst read cycles can be replicated with the memory of the present invention.** As such, BEDO memory devices can be replaced with CBEDO memory devices without effecting the operation of the memory support system. It will further be appreciated by those skilled in the art that the memory device of FIG. 5 can operate with burst lengths of 2, 4, 8, or full row cycles. (Column 8, lines 37-50 of Cowles; emphasis added).

Therefore, despite the position taken by the Examiner,[21] Cowles does not disclose or suggest generating a predetermined number of internal address signals, where the generation of the predetermined number of internal address signals is non-interruptible, as presently claimed.

Furthermore, contrary to the position taken by the Examiner,[22] merely because Cowles teaches that a premature termination of a burst may be avoided, it does not necessarily (or

---

[18] See column 6, lines 1-6 of Cowles.

[19] See FIG. 2, column 4, lines 14-18 and column 8, lines 48-50 of Cowles.

[20] See FIG. 4 and column 6, lines 6-9 of Cowles).

[21] See page 2, paragraph no. 3, lines 6-9 of the Office Action mailed October 22, 2002.

[22] See page 2, last two lines through page 3, line 3 of the Office Action mailed October 22, 2002.

Docket Number:0325.00309
Application No.: 09/504,344                          14

logically) follow that the burst is non-interruptible, as presently claimed. Specifically, Cowles recites that:

> To avoid a premature termination of a burst, RAS* cannot transition high until after the last column associated with each row has been latched. (Column 8, lines 63-65 of Cowles).

However, the sentence cited by the Examiner only pertains to termination of a burst in response to a transition of the signal RAS*. The passage is silent with respect to the signal WE*. As discussed above, Cowles discloses that a transition of the signal WE* during a burst can terminate the burst in both the standard BEDO operation and in the continuous BEDO (CBEDO) operation. In particular, Cowles states:

> The control circuit[r]y determines when a current data burst should be terminated based upon the states of RAS* 114, CAS* 124 and WE* 136. In the standard BEDO operation described above, **control circuitry 138 terminated a data burst when WE* transitioned during a burst**, or when both CAS* and RAS* transitioned high. In a CBEDO operation, **control circuitry 138** does not terminate a burst operation when CAS* and RAS* go high, but **looks to WE* for an indication that a burst operation is to be terminated**. (Column 7, lines 52-61 of Cowles; emphasis added).
>
> **To terminate** a continuous burst read operation, **the WE* signal merely has to transition high** prior to a falling edge of the CAS* signal. (Col. 8, ll. 33-36 of Cowles; emphasis added).

Cowles expressly states that the method of operation of the memory device includes (i) receiving a signal on a write enable input and (ii) terminating the step of outputting data in response to the signal.[23] Furthermore, the fact that Cowles addresses a way to **avoid** a premature termination of a burst due to the signal RAS* is acknowledgment that the burst **can** be prematurely terminated (i.e.,interrupted). Therefore, the burst is not non-interruptible, as presently claimed.

---

[23] See column 11, lines 37-41 and column 12, lines 36-40 of Cowles.

Docket Number:0325.00309
Application No.: 09/504,344                    15

Because Cowles teaches that a burst can be terminated by at least a transition of a write enable signal WE* during a read or write access, whether in a BEDO or a CBEDO operating mode, Cowles fails to disclose or suggest the **non-interruptible** generation of a predetermined number of internal address signals, as presently claimed. Therefore, Cowles does not disclose or suggest each and every element of the presently pending claim 1, arranged as in the presently pending claim 1. As such, the presently pending claim 1 is fully patentable over the cited reference[24] and the rejection should be reversed.

2.    **Group 2 (claim 6) is fully patentable over Cowles**

Claim 6 depends indirectly from claim 1 and, therefore, includes the limitations of claim 1. Consequently, the arguments presented in support of the patentability of claim 1 are hereby incorporated by reference in support of claim 6. Claim 6 further recites that a fixed burst length is programmed by bond options.

Cowles does not disclose or suggest each and every element of the presently pending claim 6. Specifically, Cowles is silent regarding programming a fixed burst length by bond options.[25] In particular, the Office Action fails to point to any specific language or figure in Cowles that is considered to disclose or suggest a fixed burst length is **programmed by bond options**, as

---

[24] *Brown v. 3M*, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) citing *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383, 58 USPQ2d 1286, 1291 (Fed. Cir. 2001); *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991). *Scripps Clinic & Research Found. V. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991).

[25] Appellant's representative has downloaded an electric version of the Cowles reference and performed a search for the words "bond" and "bond option", with no such occurrences.

Docket Number:0325.00309
Application No.: 09/504,344                    16

presently claimed.[26] Furthermore, the position taken in the Office Action that "it is well known in the art to include multiple modes of operation selected by bond options"[27] does not adequately address the deficiencies of Cowles to support the rejection under 35 U.S.C. § 102. In particular, the Federal Circuit has stated:

> To serve as anticipation, when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and it would be so recognized by persons of ordinary skill.[28]

Even assuming, *arguendo*, it is well known in the art to include multiple modes of operation selected by bond options as urged by the Examiner,[29] the Examiner failed to present any evidence that a person of ordinary skill would recognize bond options for programming a burst length are necessarily present in Cowles. Inherency requires certainty of results, not mere possibility.[30] Therefore, because Cowles does not disclose or suggest each and every element of the presently pending claim 6, arranged as in the present claim 6, the Examiner failed to meet the

---

[26] See page 6, lines 9-12 of the Office Action mailed October 22, 2002.

[27] See page 6, lines 9-12 of the Office Action mailed October 22, 2002.

[28] Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 20 USPQ 2d 1746, 1749 (Fed. Cir. 1991) (citations omitted) See also In re Sun, 31 USPQ 2d 1451, 1453 (Fed. Cir. 1993) (unpublished) ("under section 102(b), anticipation requires that the prior art reference disclose either expressly or under the principles of inherency, every limitation of the claim").

[29] See page 6, lines 9-12 of the Office Action mailed October 22, 2002.

[30] See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). See also, In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981).

Office's burden of factually establishing a *prima facie* case of anticipation.[31] As such, the presently

pending claim 6 is fully patentable over the cited reference and the rejection should be reversed.

### 3. Group 3 (claim 7) is fully patentable over Cowles

Claim 7 depends indirectly from claim 1 and, therefore, includes the limitations of

claim 1. Consequently, the arguments presented in support of the patentability of claim 1 are hereby

incorporated by reference in support of claim 7. Claim 7 further recites that a fixed burst length is

programmed by voltage levels on external pins.

Cowles does not disclose or suggest each and every element of the presently pending

claim 7. Specifically, Cowles is silent regarding programming a fixed burst length by **voltage levels**

**on external pins.**[32] In particular, the Examiner failed to point to any specific language or figure in

Cowles that is considered to disclose or suggest a fixed burst length is **programmed by voltage**

**levels on external pins**, as presently claimed.[33] Furthermore, the conclusory statement in the Office

Action that "it is inherent to have voltage levels for each burst"[34] does not adequately address why

---

[31] *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). (Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim). *In re* Skinner, 2 USPQ2d 1788, 1788-89 (B.P.A.I. 1986) ("[i]t is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office"). *See also Ex parte* Natale, 11 USPQ2d 1222, 1226 (B.P.A.I. 1989).

[32] Appellant's representative has downloaded an electronic version of the Cowles reference and performed a search for the words "bond" and "bond option", with no such occurrences.

[33] See page 6, lines 9-12 of the Office Action mailed October 22, 2002.

[34] See page 6, lines 9-12 of the Office Action mailed October 22, 2002.

Docket Number:0325.00309
Application No.: 09/504,344                18

a person of ordinary skill would recognize **programming a fixed burst length by voltage levels on external pins** as being **necessarily** present in Cowles. In particular,

> To serve as anticipation, when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and it would be so recognized by persons of ordinary skill.[35]

The Examiner has presented no evidence to support such a position.[36] Inherency requires certainty of results, not mere possibility.[37]

Thus, the Examiner failed to factually establish that Cowles discloses or suggests each and every element of the presently pending claim 7, arranged as in the present claim 7.[38] Therefore, the Examiner has not met the Office's burden of factually establishing a *prima facie* case of anticipation.[39] As such, claim 7 is fully patentable over Cowles and the rejection should be reversed.

---

[35] Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 20 USPQ 2d 1746, 1749 (Fed. Cir. 1991) (citations omitted) See also In re Sun, 31 USPQ 2d 1451, 1453 (Fed. Cir. 1993) (unpublished) ("under section 102(b), anticipation requires that the prior art reference disclose either expressly or under the principles of inherency, every limitation of the claim").

[36] See page 6, lines 13-15 of the Office Action.

[37] See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). See also, In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981).

[38] *Brown v. 3M*, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) citing *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383, 58 USPQ2d 1286, 1291 (Fed. Cir. 2001); *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991).

[39] *In re* Skinner, 2 USPQ2d 1788, 1788-89 (B.P.A.I. 1986). *See also Ex parte* Natale, 11 USPQ2d 1222, 1226 (B.P.A.I. 1989) ("[i]t is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office").

Docket Number:0325.00309
Application No.: 09/504,344                    19

## 4. Group 4 (claim 10) is fully patentable over Cowles

Claim 10 depends indirectly from claim 1 and, therefore, includes the limitations of claim 1. Consequently, the arguments presented in support of the patentability of claim 1 are hereby incorporated by reference in support of claim 10. Claim 10 further recites that the predetermined number of internal address signals is chosen to provide time for at least one writeback or refresh cycle.[40]

Cowles does not disclose or suggest each and every element of the presently pending claim 10. Specifically, Cowles is silent regarding choosing the predetermined number of internal address signals to provide time for at least one writeback or refresh cycle.[41] In particular, the lines of Cowles cited by the Examiner in support of the rejection do not address choosing the predetermined number of internal address signals to provide time for at least one writeback or refresh cycle, as presently claimed.[42] The Federal Circuit has stated:

> To serve as anticipation, when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and it would be so recognized by persons of ordinary skill.[43]

---

[40] See page 3, paragraph no. 12 of the final Office Action dated May 24, 2002.

[41] Appellant's representative has downloaded an electric version of the Cowles reference and performed a search for the words "writeback" and "refresh", with no such occurrences.

[42] See page 6, line 20 through page 7, line 2 of the Office Action mailed October 22, 2002.

[43] Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 20 USPQ 2d 1746, 1749 (Fed. Cir. 1991) (citations omitted) See also In re Sun, 31 USPQ 2d 1451, 1453 (Fed. Cir. 1993) (unpublished) ("under section 102(b), anticipation requires that the prior art reference disclose either expressly or under the principles of inherency, every limitation of the claim").

Docket Number:0325.00309
Application No.: 09/504,344                    20

The Examiner failed to present any evidence that a person of ordinary skill would recognize that Cowles necessarily chooses a burst length to provide time for at least one writeback or refresh cycle.[44] Inherency requires certainty of results, not mere possibility.[45] Therefore, because Cowles does not disclose or suggest each and every element of the presently pending claim 10, arranged as in the present claim 10, the Examiner failed to meet the Office's burden of factually establishing a *prima facie* case of anticipation.[46] As such, the presently pending claim 10 is fully patentable over the cited reference and the rejection should be reversed.

### 5.    Group 5 (claim 11) is fully patentable over Cowles

Claim 11 depends directly from claim 1 and, therefore, includes the limitations of claim 1. Consequently, the arguments presented in support of the patentability of claim 1 are hereby incorporated by reference in support of claim 11. Claim 11 further recites that the predetermined number of internal address signals is chosen to meet predetermined criteria for sharing address and control busses.

Cowles does not disclose or suggest each and every element of the presently pending claim 11. Specifically, Cowles is silent regarding choosing the predetermined number of internal

---

[44] See page 6, line 20 through page 7, line 2 of the Office Action mailed October 22, 2002.

[45] See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). See also, In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981).

[46] *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). (Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim). *In re* Skinner, 2 USPQ2d 1788, 1788-89 (B.P.A.I. 1986) ("[i]t is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office"). *See also Ex parte* Natale, 11 USPQ2d 1222, 1226 (B.P.A.I. 1989).

Docket Number:0325.00309
Application No.: 09/504,344                21

address signals to meet predetermined criteria for sharing address and control busses.[47] In particular, the lines of Cowles cited by the Examiner in support of the rejection do not address choosing the predetermined number of internal address signals to meet predetermined criteria for sharing address and control busses, as presently claimed.[48] The Federal Circuit has stated:

> To serve as anticipation, when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and it would be so recognized by persons of ordinary skill.[49]

The Examiner failed to present any evidence that a person of ordinary skill would recognize that Cowles necessarily chooses a burst length to meet predetermined criteria for sharing address and control busses.[50] Inherency requires certainty of results, not mere possibility.[51] Therefore, because Cowles does not disclose or suggest each and every element of the presently pending claim 11, arranged as in the present claim 11, the Examiner failed to meet the Office's

---

[47] Appellant's representative has downloaded an electric version of the Cowles reference and performed a search for the words "free," "freed up," "share" and "sharing", with no such occurrences.

[48] See page 7, lines 3-6 of the Office Action mailed October 22, 2002.

[49] Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 20 USPQ 2d 1746, 1749 (Fed. Cir. 1991) (citations omitted) See also In re Sun, 31 USPQ 2d 1451, 1453 (Fed. Cir. 1993) (unpublished) ("under section 102(b), anticipation requires that the prior art reference disclose either expressly or under the principles of inherency, every limitation of the claim").

[50] See page 7, lines 3-6 of the Office Action mailed October 22, 2002.

[51] See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). See also, In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981).

burden of factually establishing a *prima facie* case of anticipation.[52] As such, the presently pending claim 11 is fully patentable over the cited reference and the rejection should be reversed.

### 6.     Group 6 (claim 12) is fully patentable over Cowles

The presently pending claim 12 provides (a) means for reading data from and writing data to a plurality of storage elements in response to a plurality of internal address signals and (b) means for generating a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, where the generation of the predetermined number of internal address signals is non-interruptible.

Cowles does not disclose or suggest each and every element of the presently pending claim 12, arranged as in claim 12.   Specifically, Cowles does not disclose or suggest the non-interruptible generation of the predetermined number of address signals, as presently claimed. Cowles is directed to a continuous burst EDO memory device.[53] The Examiner admits that a continuous burst of Cowles is interruptible.[54] Specifically, the Examiner states that he agrees with Appellant's arguments with regard to termination of a continuous burst.[55] In particular, the

---

[52] *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). (Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim). *In re* Skinner, 2 USPQ2d 1788, 1788-89 (B.P.A.I. 1986) ("[i]t is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office"). *See also Ex parte* Natale, 11 USPQ2d 1222, 1226 (B.P.A.I. 1989).

[53] Title of Cowles.

[54] See page 2, paragraph no. 3, lines 4-6 of the Office Action mailed October 22, 2002.

[55] *Id.*

Docket Number:0325.00309
Application No.: 09/504,344                              23

Examiner admits that the interruptibility of a continuous burst is supported by the following passages in Cowles:[56]

> **To terminate** a continuous burst read operation, **the WE\* signal merely has to transition high** prior to a falling edge of the CAS\* signal. (Column 8, lines 33-36 of Cowles; emphasis added).

> The level of the WE\* signal must remain high for read and low for write burst accesses throughout the burst access. **A low to high transition within a burst write access will terminate the burst access,** preventing further writes from occurring. **A high to low transition on WE\* within a burst read access will likewise terminate the burst read access** and will place the data output 110 in a high impedance state. (Column 7, lines 34-41 of Cowles; emphasis added).

However, the Examiner urges that while a "continuous burst" can be terminated, a "row burst" represents a fixed burst length with no interruption.[57] Despite the position taken by the Examiner, Cowles does not appear to draw such a distinction between bursts. Specifically, with regard to a burst from a BEDO memory, Cowles states:

> Once the memory device begins to output data in a burst read cycle, the output drivers 34 will continue to drive the data lines without tri-stating the data outputs during CAS\* high intervals **dependent on the state of the output enable 42 and write enable 36 (OE\* and WE\*) control lines,** thus allowing additional time for the system to latch the output data. (Column 3, line 65 through column 4, line 4 of Cowles; emphasis added).

> The control circuit[r]y determines when a current data burst should be terminated **based upon the state of RAS\* 14, CAS\* 24 and WE\* 36.** (Column 4, lines 63-65 of Cowles; emphasis added).

---

[56] *Id.*

[57] See page 2, paragraph no. 3, lines 6-9 of the Office Action mailed October 22, 2002, which appears to suggest that a continuous burst can be terminated or interrupted, while a row burst cannot.

Docket Number:0325.00309
Application No.: 09/504,344                    24

**The level of the WE\* signal must remain high for read and low for write burst accesses throughout the burst access.** A low to high transition within a burst write access will terminate the burst access, preventing further writes from occurring. A high to low transition on WE\* within a burst read access will likewise terminate the burst read access and will place the data output 10 in a high impedance state. (Column 5, lines 4-10 of Cowles; emphasis added).

**Both RAS\* and CAS\* going high during a burst access will also terminate the burst access cycle** placing the data drivers in a high impedance output state, and resetting the burst length counter. (Column 5, lines 25-28 of Cowles; emphasis added).

Thus, in BEDO memories, Cowles clearly teaches that there are three conditions that

will terminate (i.e., interrupt) a burst access:

1.    WE\* transitioning, either from low to high or from high to low;

2.    RAS\* and CAS\* going high; or

3.    OE\* going high.[58]

Cowles is quite clear that WE\* transitions will terminate both a row burst and a continuous burst

access. In particular, Cowles states:

The control circuit[r]y determines when a current data burst should be terminated based upon the states of RAS\* 114, CAS\* 124 and WE\* 136. In the standard BEDO operation described above, **control circuitry 138 terminated a data burst when WE\* transitioned during a burst**, or when both CAS\* and RAS\* transitioned high. In a CBEDO operation, **control circuitry 138** does not terminate a burst operation when CAS\* and RAS\* go high, but **looks to WE\* for an indication that a burst operation is to be terminated.** (Column 7, lines 52-61 of Cowles; emphasis added).

**To terminate** a continuous burst read operation, **the WE\* signal merely has to transition high** prior to a falling edge of the CAS\* signal. (Col. 8, ll. 33-36 of Cowles; emphasis added).

---

[58] However, the state of OE\*, arguably, may have little, if anything, to do with generating a predetermined number of internal addresses.

Docket Number:0325.00309
Application No.: 09/504,344                  25

Therefore, since Cowles states that a transition of the signal WE* during a burst can terminate the burst in both the standard BEDO operation and in the continuous BEDO (CBEDO) operation, Cowles explicitly teaches that a premature termination of a row burst can take place.

FIG. 4 of Cowles further evidences that row bursts are interruptible. Specifically, FIG. 4 illustrates a burst access starting at column address "COLn" is terminated (i.e., interrupted) when the signal WE* transitions from low to high.[59] Furthermore, Cowles shows addressing sequences for burst lengths of 2, 4, and 8 cycles.[60] However, FIG. 4 of Cowles illustrates a burst access starting at the column address "COLp" is interrupted after only three cycles by the signal RAS* rising.[61] With regard to the operations illustrated in FIG. 4, Cowles further states:

> It will be appreciated that the read and write operations performed on a single memory row of the memory of FIG. 5 are identical to the operation of the memory of FIG. 1 as shown in FIG. 3. That is, after completing a burst read, the WE* signal transitions low and the next falling edge of CAS* latches a new column address for a burst write operation. **Likewise, the timing diagram of FIG. 4 depicting burst write access cycles followed by burst read cycles can be replicated with the memory of the present invention.** As such, BEDO memory devices can be replaced with CBEDO memory devices without effecting the operation of the memory support system. It will further be appreciated by those skilled in the art that the memory device of FIG. 5 can operate with burst lengths of 2, 4, 8, or full row cycles. (Column 8, lines 37-50 of Cowles; emphasis added).

---

[59] See column 6, lines 1-6 of Cowles.

[60] See FIG. 2, column 4, lines 14-18 and column 8, lines 48-50 of Cowles.

[61] See FIG. 4 and column 6, lines 6-9 of Cowles.

Docket Number:0325.00309
Application No.: 09/504,344      26

Therefore, despite the position taken by the Examiner,[62] Cowles does not disclose or suggest generating a predetermined number of internal address signals, where the generation of the predetermined number of internal address signals is non-interruptible, as presently claimed.

Furthermore, contrary to the position taken by the Examiner,[63] merely because Cowles teaches that a premature termination of a burst may be avoided, it does not necessarily (or logically) follow that the burst is non-interruptible, as presently claimed. Specifically, Cowles recites that:

> To avoid a premature termination of a burst, RAS* cannot transition high until after the last column associated with each row has been latched. (Column 8, lines 63-65 of Cowles).

However, the sentence cited by the Examiner only pertains to termination of a burst in response to a transition of the signal RAS*. The passage is silent with respect to the signal WE*. As discussed above, Cowles discloses that a transition of the signal WE* during a burst can terminate the burst in both the standard BEDO operation and in the continuous BEDO (CBEDO) operation. In particular, Cowles states:

> The control circuit[r]y determines when a current data burst should be terminated based upon the states of RAS* 114, CAS* 124 and WE* 136. In the standard BEDO operation described above, **control circuitry 138 terminated a data burst when WE* transitioned during a burst**, or when both CAS* and RAS* transitioned high. In a CBEDO operation, **control circuitry 138** does not terminate a burst operation when CAS* and RAS* go high, but **looks to WE* for an indication that a burst operation is to be terminated**. (Column 7, lines 52-61 of Cowles; emphasis added).

---

[62] See page 2, paragraph no. 3, lines 6-9 of the Office Action mailed October 22, 2002.

[63] See page 2, last two lines through page 3, line 3 of the Office Action mailed October 22, 2002.

Docket Number:0325.00309
Application No.: 09/504,344       27

> **To terminate** a continuous burst read operation, **the WE\* signal merely has to transition high** prior to a falling edge of the CAS\* signal. (Col. 8, ll. 33-36 of Cowles; emphasis added).

Cowles expressly states that the method of operation of the memory device includes (i) receiving a signal on a write enable input and (ii) terminating the step of outputting data in response to the signal.[64] Furthermore, the fact that Cowles addresses a way to **avoid** a premature termination of a burst due to the signal RAS\* is acknowledgment that the burst **can** be prematurely terminated (i.e.,interrupted). Therefore, the burst is not non-interruptible, as presently claimed.

Because Cowles teaches that a burst can be terminated by at least a transition of a write enable signal WE\* during a read or write access, whether in a BEDO or a CBEDO operating mode, Cowles fails to disclose or suggest the **non-interruptible** generation of a predetermined number of internal address signals, as presently claimed. Therefore, Cowles does not disclose or suggest each and every element of the presently pending claim 12, arranged as in the presently pending claim 12. As such, the presently pending claim 12 is fully patentable over the cited reference[65] and the rejection should be reversed.

---

[64] See column 11, lines 37-41 and column 12, lines 36-40 of Cowles.

[65] *Brown v. 3M*, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) citing *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383, 58 USPQ2d 1286, 1291 (Fed. Cir. 2001); *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991). *Scripps Clinic & Research Found. V. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991).

Docket Number:0325.00309
Application No.: 09/504,344          28

7.    **Group 7 (claims 13, 14 and 16) is fully patentable over Cowles**

The presently pending claim 13 provides the steps of (a) accessing a memory in response to a plurality of internal address signals and (b) generating a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, where the generation of the predetermined number of internal address signals is non-interruptible.

Cowles does not disclose or suggest each and every element of the presently pending claim 13, arranged as in claim 13. Specifically, Cowles does not disclose or suggest the non-interruptible generation of the predetermined number of address signals as presently claimed. Cowles is directed to a continuous burst EDO memory device.[66] The Examiner admits that a continuous burst of Cowles is interruptible.[67] Specifically, the Examiner states that he agrees with Appellant's arguments with regard to termination of a continuous burst.[68] In particular, the Examiner admits that the interruptibility of a continuous burst is supported by the following passages in Cowles:[69]

> **To terminate** a continuous burst read operation, **the WE\* signal merely has to transition high** prior to a falling edge of the CAS\* signal. (Column 8, lines 33-36 of Cowles; emphasis added).
>
> The level of the WE\* signal must remain high for read and low for write burst accesses throughout the burst access. **A low to high transition within a burst write access will terminate the burst**

---

[66]Title of Cowles.

[67] See page 2, paragraph no. 3, lines 4-6 of the Office Action mailed October 22, 2002.

[68] *Id.*

[69] *Id.*

**access, preventing further writes from occurring. A high to low transition on WE\* within a burst read access will likewise terminate the burst read access** and will place the data output 110 in a high impedance state. (Column 7, lines 34-41 of Cowles; emphasis added).

However, the Examiner urges that while a "continuous burst" can be terminated, a "row burst" represents a fixed burst length with no interruption.[70] Despite the position taken by the Examiner, Cowles does not appear to draw such a distinction between bursts. Specifically, with regard to a burst from a BEDO memory, Cowles states:

> Once the memory device begins to output data in a burst read cycle, the output drivers 34 will continue to drive the data lines without tri-stating the data outputs during CAS\* high intervals **dependent on the state of the output enable 42 and write enable 36 (OE\* and WE\*) control lines**, thus allowing additional time for the system to latch the output data. (Column 3, line 65 through column 4, line 4 of Cowles; emphasis added).

> The control circuit[r]y determines when a current data burst should be terminated **based upon the state of RAS\* 14, CAS\* 24 and WE\* 36.** (Column 4, lines 63-65 of Cowles; emphasis added).

> **The level of the WE\* signal must remain high for read and low for write burst accesses throughout the burst access.** A low to high transition within a burst write access will terminate the burst access, preventing further writes from occurring. A high to low transition on WE\* within a burst read access will likewise terminate the burst read access and will place the data output 10 in a high impedance state. (Column 5, lines 4-10 of Cowles; emphasis added).

> **Both RAS\* and CAS\* going high during a burst access will also terminate the burst access cycle** placing the data drivers in a high impedance output state, and resetting the burst length counter. (Column 5, lines 25-28 of Cowles; emphasis added).

---

[70] See page 2, paragraph no. 3, lines 6-9 of the Office Action mailed October 22, 2002, which appears to suggest that a continuous burst can be terminated or interrupted, while a row burst cannot.

Docket Number:0325.00309
Application No.: 09/504,344                     30

Thus, in BEDO memories, Cowles clearly teaches that there are three conditions that will terminate (i.e., interrupt) a burst access:

1.    WE* transitioning, either from low to high or from high to low;

2.    RAS* and CAS* going high; or

3.    OE* going high.[71]

Cowles is quite clear that WE* transitions will terminate both a row burst and a continuous burst access. In particular, Cowles states:

> The control circuit[r]y determines when a current data burst should be terminated based upon the states of RAS* 114, CAS* 124 and WE* 136. In the standard BEDO operation described above, **control circuitry 138 terminated a data burst when WE* transitioned during a burst**, or when both CAS* and RAS* transitioned high. In a CBEDO operation, **control circuitry 138** does not terminate a burst operation when CAS* and RAS* go high, but **looks to WE* for an indication that a burst operation is to be terminated.** (Column 7, lines 52-61 of Cowles; emphasis added).

> **To terminate** a continuous burst read operation, **the WE* signal merely has to transition high** prior to a falling edge of the CAS* signal. (Col. 8, ll. 33-36 of Cowles; emphasis added).

Therefore, since Cowles states that a transition of the signal WE* during a burst can terminate the burst in both the standard BEDO operation and in the continuous BEDO (CBEDO) operation, Cowles explicitly teaches that a premature termination of a row burst can take place.

FIG. 4 of Cowles further evidences that row bursts are interruptible. Specifically, FIG. 4 illustrates a burst access starting at column address "COLn" is terminated (i.e., interrupted)

---

[71] However, the state of OE*, arguably, may have little, if anything, to do with generating a predetermined number of internal addresses.

Docket Number:0325.00309
Application No.: 09/504,344                31

when the signal WE* transitions from low to high.[72] Furthermore, Cowles shows addressing sequences for burst lengths of 2, 4, and 8 cycles.[73] However, FIG. 4 of Cowles illustrates a burst access starting at the column address "COLp" is interrupted after only three cycles by the signal RAS* rising.[74] With regard to the operations illustrated in FIG. 4, Cowles further states:

> It will be appreciated that the read and write operations performed on a single memory row of the memory of FIG. 5 are identical to the operation of the memory of FIG. 1 as shown in FIG. 3. That is, after completing a burst read, the WE* signal transitions low and the next falling edge of CAS* latches a new column address for a burst write operation. **Likewise, the timing diagram of FIG. 4 depicting burst write access cycles followed by burst read cycles can be replicated with the memory of the present invention.** As such, BEDO memory devices can be replaced with CBEDO memory devices without effecting the operation of the memory support system. It will further be appreciated by those skilled in the art that the memory device of FIG. 5 can operate with burst lengths of 2, 4, 8, or full row cycles. (Column 8, lines 37-50 of Cowles; emphasis added).

Therefore, despite the position taken by the Examiner,[75] Cowles does not disclose or suggest generating a predetermined number of internal address signals, where the generation of the predetermined number of internal address signals is non-interruptible, as presently claimed.

Furthermore, contrary to the position taken by the Examiner,[76] merely because Cowles teaches that a premature termination of a burst may be avoided, it does not necessarily (or

---

[72] See column 6, lines 1-6 of Cowles.

[73] See FIG. 2, column 4, lines 14-18 and column 8, lines 48-50 of Cowles.

[74] See FIG. 4 and column 6, lines 6-9 of Cowles.

[75] See page 2, paragraph no. 3, lines 6-9 of the Office Action mailed October 22, 2002.

[76] See page 2, last two lines through page 3, line 3 of the Office Action mailed October 22, 2002.

Docket Number:0325.00309
Application No.: 09/504,344        32

logically) follow that the burst is non-interruptible, as presently claimed. Specifically, Cowles recites that:

> To avoid a premature termination of a burst, RAS* cannot transition high until after the last column associated with each row has been latched. (Column 8, lines 63-65 of Cowles).

However, the sentence cited by the Examiner only pertains to termination of a burst in response to a transition of the signal RAS*. The passage is silent with respect to the signal WE*. As discussed above, Cowles discloses that a transition of the signal WE* during a burst can terminate the burst in both the standard BEDO operation and in the continuous BEDO (CBEDO) operation. In particular, Cowles states:

> The control circuit[r]y determines when a current data burst should be terminated based upon the states of RAS* 114, CAS* 124 and WE* 136. In the standard BEDO operation described above, **control circuitry 138 terminated a data burst when WE* transitioned during a burst**, or when both CAS* and RAS* transitioned high. In a CBEDO operation, **control circuitry 138** does not terminate a burst operation when CAS* and RAS* go high, but **looks to WE* for an indication that a burst operation is to be terminated**. (Column 7, lines 52-61 of Cowles; emphasis added).

> **To terminate** a continuous burst read operation, **the WE* signal merely has to transition high** prior to a falling edge of the CAS* signal. (Col. 8, ll. 33-36 of Cowles; emphasis added).

Cowles expressly states that the method of operation of the memory device includes (i) receiving a signal on a write enable input and (ii) terminating the step of outputting data in response to the signal.[77] Furthermore, the fact that Cowles addresses a way to **avoid** a premature termination of a burst due to the signal RAS* is acknowledgment that the burst **can** be prematurely terminated (i.e.,interrupted). Therefore, the burst is not non-interruptible, as presently claimed.

---

[77] See column 11, lines 37-41 and column 12, lines 36-40 of Cowles.

Docket Number:0325.00309
Application No.: 09/504,344                     33

Because Cowles teaches that a burst can be terminated by at least a transition of a write enable signal WE* during a read or write access, whether in a BEDO or a CBEDO operating mode, Cowles fails to disclose or suggest the **non-interruptible** generation of a predetermined number of internal address signals, as presently claimed. Therefore, Cowles does not disclose or suggest each and every element of the presently pending claim 13, arranged as in the presently pending claim 13. As such, the claims of Group 7 are fully patentable over the cited reference[78] and the rejection should be reversed.


### 8. Group 8 (claim 15) is fully patentable over Cowles

Claim 15 depends indirectly from claim 13 and, therefore, includes the limitations of claim 13. Consequently, the arguments presented in support of the patentability of claim 13 are hereby incorporated by reference in support of claim 15. Claim 15 further recites that a programming step is performed using bond options.

Cowles does not disclose or suggest each and every element of the presently pending claim 6. Specifically, Cowles is silent regarding bond options.[79] In particular, the Office Action fails to point to any specific language or figure in Cowles that is considered to disclose or suggest

---

[78] *Brown v. 3M*, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) citing *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383, 58 USPQ2d 1286, 1291 (Fed. Cir. 2001); *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991). *Scripps Clinic & Research Found. V. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991).

[79] Appellant's representative has downloaded an electric version of the Cowles reference and performed a search for the words "bond" and "bond option", with no such occurrences.

Docket Number:0325.00309
Application No.: 09/504,344        34

a programming step **performed using bond options**, as presently claimed.[80] Furthermore, the

position taken in the Office Action that "it is well known in the art to include multiple modes of

operation selected by bond options"[81] does not adequately address the deficiencies of Cowles to

support the rejection under 35 U.S.C. § 102. In particular, the Federal Circuit has stated:

> To serve as anticipation, when the reference is silent about the
> asserted inherent characteristic, such gap in the reference may be
> filled with recourse to extrinsic evidence. Such evidence must make
> clear that the missing descriptive matter is **necessarily present** in the
> thing described in the reference, and it would be so recognized by
> persons of ordinary skill.[82]

Even assuming, *arguendo*, it is well known in the art to include multiple modes of

operation selected by bond options as urged by the Examiner,[83] the Examiner failed to present any

evidence that a person of ordinary skill would recognize a programming step performed **using bond**

**options**, as necessarily present in Cowles. Inherency requires certainty of results, not mere

possibility.[84] Therefore, because Cowles does not disclose or suggest each and every element of the

presently pending claim 15, arranged as in the present claim 15, the Examiner has not met the

---

[80] See page 6, lines 9-12 of the Office Action mailed October 22, 2002.

[81] See page 6, lines 9-12 of the Office Action mailed October 22, 2002.

[82] Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 20 USPQ 2d 1746, 1749 (Fed. Cir. 1991) (citations omitted, emphasis added) See also In re Sun, 31 USPQ 2d 1451, 1453 (Fed. Cir. 1993) (unpublished) ("under section 102(b), anticipation requires that the prior art reference disclose either expressly or under the principles of inherency, every limitation of the claim").

[83] See page 6, lines 9-12 of the Office Action mailed October 22, 2002.

[84] See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). See also, In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981).

Docket Number:0325.00309
Application No.: 09/504,344                    35

Office's burden of factually establishing a *prima facie* case of anticipation.[85] As such, the presently pending claim 15 is fully patentable over Cowles and the rejection should be reversed.

### 9. Group 9 (claim 17) is fully patentable over Cowles

Claim 17 depends directly from claim 13 and, therefore, includes the limitations of claim 13. Consequently, the arguments presented in support of the patentability of claim 13 are hereby incorporated by reference in support of claim 17. Claim 17 further recites the step of selecting the predetermined number of internal address signals to provide time for at least one writeback or refresh cycle.[86]

Cowles does not disclose or suggest each and every element of the presently pending claim 17. Specifically, Cowles is silent regarding selecting the predetermined number of internal address signals **to provide time for at least one writeback or refresh cycle**, as presently claimed.[87] In particular, the lines of Cowles cited by the Examiner in support of the rejection do not address selecting the predetermined number of internal address signals **to provide time for at least one writeback or refresh cycle**, as presently claimed.[88] The Federal Circuit has stated:

---

[85] *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). (Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim). *In re* Skinner, 2 USPQ2d 1788, 1788-89 (B.P.A.I. 1986)("[i]t is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office"). *See also Ex parte* Natale, 11 USPQ2d 1222, 1226 (B.P.A.I. 1989) .

[86] See page 3, paragraph no. 12 of the final Office Action dated May 24, 2002.

[87] Appellant's representative has downloaded an electric version of the Cowles reference and performed a search for the words "writeback" and "refresh", with no such occurrences.

[88] See page 6, line 20 through page 7, line 2 of the Office Action mailed October 22, 2002.

Docket Number:0325.00309
Application No.: 09/504,344                    36

To serve as anticipation, when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and it would be so recognized by persons of ordinary skill.[89]

The Examiner failed to present any evidence that a person of ordinary skill would recognize that selecting a burst length to provide time for at least one writeback or refresh cycle is necessarily present in Cowles.[90] Specifically, the sections of Cowles cited by the Examiner in support of the rejection of claim 17 provide:

To terminate a continuous burst read operation, the WE* signal merely has to transition high prior to a falling edge of the CAS* signal.

***

To avoid a premature termination of a burst, RAS* cannot transition high until after the last column associated with each row has been latched.[91]

The portions of Cowles cited by the Examiner are silent regarding selecting the predetermined number of internal address signals to provide time for at least one writeback or refresh cycle, as presently claimed. Furthermore, the Examiner provided no line of reasoning why the passages were considered to make clear that the missing descriptive matter was necessarily present in the memory

---

[89] Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 20 USPQ 2d 1746, 1749 (Fed. Cir. 1991) (citations omitted) See also In re Sun, 31 USPQ 2d 1451, 1453 (Fed. Cir. 1993) (unpublished) ("under section 102(b), anticipation requires that the prior art reference disclose either expressly or under the principles of inherency, every limitation of the claim").

[90] See page 6, line 20 through page 7, line 2 of the Office Action mailed October 22, 2002.

[91] See page 6, line 20 through page 7, line 2 of the Office Action mailed October 22, 2002 (citing column 8, lines 33-36 and 63-65 of Cowles).

Docket Number:0325.00309
Application No.: 09/504,344                    37

device of Cowles. Inherency requires certainty of results, not mere possibility.[92] Therefore, because Cowles does not disclose or suggest each and every element of the presently pending claim 17, arranged as in the present claim 17, the Examiner failed to meet the Office's burden of factually establishing a *prima facie* case of anticipation.[93] As such, the presently pending claim 17 is fully patentable over the cited reference and the rejection should be reversed.

### 10. Group 10 (claim 21) is fully patentable over Cowles

Claim 21 depends directly from claim 1 and, therefore, includes the limitations of claim 1. Consequently, the arguments presented in support of the patentability of claim 1 are hereby incorporated by reference in support of claim 21. Claim 21 further recites that the circuit further comprises address and control busses configured to present the external address signal and one or more control signals, where the busses are **freed up during the generation of the predetermined number of internal address signals**.

Cowles does not disclose or suggest each and every element of the presently pending claim 21, arranged as in the presently pending claim 21. Specifically, Cowles is silent regarding address and control busses configured to present the external address signal and one or more control signals, where the busses are **freed up during the generation of the predetermined number of**

---

[92] See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). See also, In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981).

[93] *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). (Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim). *In re* Skinner, 2 USPQ2d 1788, 1788-89 (B.P.A.I. 1986)("[i]t is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office"). *See also Ex parte* Natale, 11 USPQ2d 1222, 1226 (B.P.A.I. 1989).

Docket Number:0325.00309
Application No.: 09/504,344                 38

**internal address signals**, as presently claimed.[94]  In particular, the lines of Cowles cited by the

Examiner in support of the rejection do not address address and control busses configured to present

the external address signal and one or more control signals, where the busses are **freed up during**

**the generation of the predetermined number of internal address signals**, as presently claimed.[95]

Furthermore, the Federal Circuit has stated:

> To serve as anticipation, when the reference is silent about the
> asserted inherent characteristic, such gap in the reference may be
> filled with recourse to extrinsic evidence.  Such evidence must make
> clear that the missing descriptive matter is necessarily present in the
> thing described in the reference, and it would be so recognized by
> persons of ordinary skill.[96]

The Examiner failed to present any evidence that a person of ordinary skill would

recognize that Cowles necessarily presents address and control busses configured to present the

external address signal and one or more control signals, where the busses are **freed up during the**

**generation of the predetermined number of internal address signals**, as presently claimed.[97]

Inherency requires certainty of results, not mere possibility.[98]  Therefore, because Cowles does not

---

[94] Appellant's representative has downloaded an electric version of the Cowles reference and performed a search for the words "free," "freed up," "share" and "sharing", with no such occurrences.

[95] See page 7, lines 15-19 of the Office Action mailed October 22, 2002.

[96] Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 20 USPQ 2d 1746, 1749 (Fed. Cir. 1991) (citations omitted) See also In re Sun, 31 USPQ 2d 1451, 1453 (Fed. Cir. 1993) (unpublished) ("under section 102(b), anticipation requires that the prior art reference disclose either expressly or under the principles of inherency, every limitation of the claim").

[97] See page 7, lines 15-19 of the Office Action mailed October 22, 2002.

[98] See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988).  See also, In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981).

Docket Number:0325.00309
Application No.: 09/504,344                                          39

claims are not rendered anticipated or obvious by the cited reference. However, should the Board

find the arguments herein in support of independent claims 1, 12 and/or 13 unpersuasive, the Board

is respectfully requested to carefully consider the arguments set forth above in support of each of the

independently patentable groups.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.

Robert M. Miller
Reg. No. 42,892

Dated: <u>March 24, 2003</u>

24025 Greater Mack
Suite 200
St. Clair Shores, MI 48080
(586) 498-0670

Docket Number:0325.00309
Application No.: 09/504,344                41

CLAIMS IN CURRENT FORM

1        1.      (AMENDED) A circuit comprising:

2        a memory comprising a plurality of storage elements each

3    configured to read and write data in response to an internal

4    address signal; and

5        a logic circuit configured to generate a predetermined

6    number of said internal address signals in response to (i) an

7    external address signal, (ii) a clock signal and (iii) one or more

8    control signals, wherein said generation of said predetermined

9    number of internal address signals is non-interruptible.


1        2.      (AMENDED) The circuit according to claim 1, wherein

2    said predetermined number of internal address signals is determined

3    by a fixed burst length.


1        3.      (AMENDED) The circuit according to claim 1, wherein

2    said predetermined number of internal address signals is at least

3    4.


1        4.      (AMENDED) The circuit according to claim 1, wherein

2    said predetermined number of internal address signals is 8.

1    5.    (AMENDED) The circuit according to claim 2, wherein
2  said fixed burst length is programmable.


1    6.    (AMENDED) The circuit according to claim 5, wherein
2  said fixed burst length is programmed by bond options.


1    7.    (AMENDED) The circuit according to claim 5, wherein
2  said fixed burst length is programmed by voltage levels on external
3  pins.


1    8.    (AMENDED) The circuit according to claim 1, wherein
2  said memory comprises a static random access memory.


1    9.    (AMENDED) The circuit according to claim 1, wherein
2  said memory comprises a dynamic random access memory.


1    10.    (AMENDED) The circuit according to claim 9, wherein
2  said predetermined number of internal address signals is chosen to
3  provide time for at least one writeback or refresh cycle.

1       11.   (AMENDED) The circuit according to claim 1, wherein

2    said predetermined number of internal address signals is chosen to

3    meet predetermined criteria for sharing address and control busses.


1       12.   (AMENDED) A circuit comprising:

2          means for reading data from and writing data to a

3    plurality of storage elements in response to a plurality of

4    internal address signals; and

5          means for generating a predetermined number of said

6    internal address signals in response to (i) an external address

7    signal, (ii) a clock signal and (iii) one or more control signals,

8    wherein said generation of said predetermined number of internal

9    address signals is non-interruptible.


1       13.   (AMENDED) A method of providing a fixed burst length

2    data transfer comprising the steps of:

3          accessing a memory in response to a plurality of internal

4    address signals; and

5          generating a predetermined number of said internal

6    address signals in response to (i) an external address signal, (ii)

7    a clock signal and (iii) a control signal, wherein said generation

8    of said predetermined number of internal address signals is non-interruptible.

1         14.   The method according to claim 13, further comprising

2    the step of programming said predetermined number.

1         15.   The method according to claim 14, wherein said

2    programming step is performed using bond options.

1         16.   The method according to claim 14, wherein said

2    programming step is performed using voltage levels.

1         17.   (AMENDED) The method according to claim 13, further

2    comprising the step of selecting said predetermined number to

3    provide time for at least one writeback or refresh cycle.

1         18.   The circuit according to claim 1, wherein said logic

2    circuit comprises a counter configured to generate said

3    predetermined number of internal address signals.

1         19.   (AMENDED) The circuit according to claim 1, wherein

2    said external address signal comprises an initial address for data

3    transfers to and from said memory.

Docket Number:0325.00309
Application No.: 09/504,344                    45

1          20. A memory device according to claim 1, wherein said

2    circuit is an integrated circuit.


1          21. (AMENDED) The circuit according to claim 1, further

2    comprising address and control busses configured to present said

3    external address signal and said one or more control signals,

4    wherein said busses are freed up during the generation of said

5    predetermined number of internal address signals.

Docket Number:0325.00309
Application No.: 09/504,344         46

Attorney Docket: 0325.00309

IN RE APPLICATION OF:  Cathal G. Phelan

SERIAL NO.: 09/504,344

RESPONSE TRANSMITTAL AND
EXTENSION OF TIME REQUEST
(IF REQUIRED)

TITLE: FIXED BURST MEMORIES

FILED: February 14, 2000

EXAMINER: Namzai, M.

ART UNIT: 2187

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Sir:

Enclosed please find an appeal brief and a postcard along with the fee calculation below:

**FEE CALCULATION FOR ENCLOSED AND EXTENSION REQUEST (IF ANY)**

| | Claims Remaining | Highest No. Previous | Extra Rate | Additional Fee |
|---|---|---|---|---|
| Total Claims | 21 minus | 21 = | 0 x $ 18.00 | $ 0.00 |
| Independent Claims | 3 minus | 3 = | 0 x $ 84.00 | $ 0.00 |
| Multiple Dependent Claim First Added | | | + $280.00 $ 0.00 | |

TOTAL IF NOT SMALL ENTITY .. $0.00

[ ] SMALL ENTITY STATUS - If applicable, divide by 2 ..................... $0.00
[ ] Verified statement enclosed, if not previously filed.

[ ] Applicant also requests a _____ month extension of time
for response to the outstanding Office Action. The fee is ................... $0.00

[X] Fee set forth for Appeal Brief ................................. $320.00

TOTAL FEE ......................................................... $320.00

The Commissioner is hereby authorized to charge any overpayment or underpayment of the above fee associated with this Communication to Deposit Account No. 50-0541. A duplicate copy of this sheet is attached.

CHRISTOPHER P. MAIORANA, P.C.

24025 Greater Mack, Suite 200
St. Clair Shores, Michigan 48080
(586) 498-0670

By: _Robert M. Miller_
Robert M. Miller
Registration No.: 42,892

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on _March 24, 2003_ .

By: _Mary Donna Berkley_
Mary Donna Berkley

| | Application No. | Applicant(s) |
|---|---|---|
| ***Notice of Allowability*** | 09/504,344 | PHELAN, CATHAL G. |
| | Examiner | Art Unit |
| | Mehdi Namazi | 2188 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--*
All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included
herein (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS
NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative
of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *03/28/2003*.

2. ☒ The allowed claim(s) is/are *1-21*.

3. ☐ The drawings filed on _____ are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a) ☐ All    b) ☐ Some*   c) ☐ None   of the:
       1. ☐ Certified copies of the priority documents have been received.
       2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
       3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the
           International Bureau (PCT Rule 17.2(a)).
     * Certified copies not received: _____ .

5. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
    (a) ☐ The translation of the foreign language provisional application has been received.

6. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted
below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE**

7. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF
INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

8. ☒ CORRECTED DRAWINGS must be submitted.
    (a) ☒  including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
        1) ☐ hereto or 2) ☒ to Paper No. *3*.
    (b) ☐  including changes required by the proposed drawing correction filed _____, which has been approved by the Examiner.
    (c) ☐  including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No. _____ .

    Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of
    each sheet.

9. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the
attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1 ☐ Notice of References Cited (PTO-892)
3 ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
5 ☐ Information Disclosure Statements (PTO-1449), Paper No. _____ .
7 ☐ Examiner's Comment Regarding Requirement for Deposit
    of Biological Material

2 ☐ Notice of Informal Patent Application (PTO-152)
4 ☐ Interview Summary (PTO-413), Paper No._____ .
6 ☐ Examiner's Amendment/Comment
8 ☒ Examiner's Statement of Reasons for Allowance
9 ☐ Other     .

## DETAILED ACTION

### Drawings

1.   The application having been allowed, formal drawings are required in response to this Office Action.

### Allowable Subject Matter
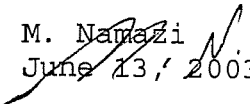
2.   The following is an examiner's statement of reasons for allowance: the prior art discloses an integrated circuit memory device which can operate at high data speeds.  The integrated circuit memory can output data of a "fixed burst length" in a continuous stream while rows of the memory are accessed. However, to terminate a continuous burst read operation, the WE signal merely has to transition high prior to a falling edge of the CAS signal (see, for example, Cowles). thus prior art of record does not teach or fairly suggest the non-interruptible generation of a predetermined number of internal address signals. Accordingly, the invention as claimed is not seen to be anticipated or made obvious, within the meaning of 35 U.S.C. 103, by the prior art of record.

3.   Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to
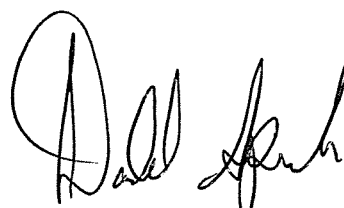
avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mehdi Namazi whose telephone number is (703) 306-2758. The examiner can normally be reached on Monday-Friday from 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks, can be reached on (703) 308-1756. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-9600.

M. Namazi
June 13, 2003

Donald A. Sparks
Supervisory Patent Examiner
TC 2100

# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

## NOTICE OF ALLOWANCE AND FEE(S) DUE

| | | |
|---|---|---|
| 021363 | 7590 | 06/16/2003 |

CHRISTOPHER P. MAIORANA, P.C.
24025 GREATER MACK
SUITE 200
ST. CLAIR SHORES, MI 48080

| EXAMINER |
|---|
| NAMAZI, MEHDI |

| ART UNIT | CLASS-SUBCLASS |
|---|---|
| 2188 | 711-104000 |

DATE MAILED: 06/16/2003

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/504,344 | 02/14/2000 | Cathal G. Phelan | 0325.000309 | 7771 |

TITLE OF INVENTION: MEMORY DEVICE WITH FIXED LENGTH NON-INTERRUPTIBLE BURST

| APPLN. TYPE | SMALL ENTITY | ISSUE FEE | PUBLICATION FEE | TOTAL FEE(S) DUE | DATE DUE |
|---|---|---|---|---|---|
| nonprovisional | NO | $1300 | $0 | $1300 | 09/16/2003 |

**THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.**

**THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.**

**HOW TO REPLY TO THIS NOTICE:**

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status is changed, pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above and notify the United States Patent and Trademark Office of the change in status, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check the box below and enclose the PUBLICATION FEE and 1/2 the ISSUE FEE shown above.

❏ Applicant claims SMALL ENTITY status.
See 37 CFR 1.27.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

**IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.**

Page 1 of 4

PTOL-85 (REV. 05-03) Approved for use through 04/30/2004.

# PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
**Commissioner for Patents**
**Alexandria, Virginia 22313-1450**
**Fax** **(703)746-4000**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

| CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1) | Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission. |
|---|---|

021363    7590    06/16/2003

CHRISTOPHER P. MAIORANA, P.C.
24025 GREATER MACK
SUITE 200
ST. CLAIR SHORES, MI 48080

**Certificate of Mailing or Transmission**
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above, or being facsimile transmitted to the USPTO, on the date indicated below.

|  |
|---|
| (Depositor's name) |
| (Signature) |
| (Date) |

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/504,344 | 02/14/2000 | Cathal G. Phelan | 0325.000309 | 7771 |

TITLE OF INVENTION: MEMORY DEVICE WITH FIXED LENGTH NON-INTERRUPTIBLE BURST

| APPLN. TYPE | SMALL ENTITY | ISSUE FEE | PUBLICATION FEE | TOTAL FEE(S) DUE | DATE DUE |
|---|---|---|---|---|---|
| nonprovisional | NO | $1300 | $0 | $1300 | 09/16/2003 |

| EXAMINER | ART UNIT | CLASS-SUBCLASS |
|---|---|---|
| NAMAZI, MEHDI | 2188 | 711-104000 |

| 1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).<br><br>❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.<br><br>❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.** | 2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. | 1_____<br><br>2_____<br><br>3_____ |

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the USPTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE                     (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent)     ❑ individual  ❑ corporation or other private group entity  ❑ government

| 4a. The following fee(s) are enclosed:<br><br>❑ Issue Fee<br>❑ Publication Fee<br>❑ Advance Order - # of Copies _____ | 4b. Payment of Fee(s):<br><br>❑ A check in the amount of the fee(s) is enclosed.<br>❑ Payment by credit card. Form PTO-2038 is attached.<br>❑ The Commissioner is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _____(enclose an extra copy of this form). |

Commissioner for Patents is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

(Authorized Signature)                     (Date)

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMIT THIS FORM WITH FEE(S)

PTOL-85 (REV. 05-03) Approved for use through 04/30/2004. OMB 0651-0033    U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/504,344 | 02/14/2000 | Cathal G. Phelan | 0325.000309 | 7771 |

| | | | EXAMINER |
|---|---|---|---|
| 021363 | 7590 | 06/16/2003 | NAMAZI, MEHDI |

CHRISTOPHER P. MAIORANA, P.C.
24025 GREATER MACK
SUITE 200
ST. CLAIR SHORES, MI 48080
UNITED STATES

| ART UNIT | PAPER NUMBER |
|---|---|
| 2188 | |

DATE MAILED: 06/16/2003

## Determination of Patent Term Extension under 35 U.S.C. 154 (b)
### (application filed after June 7, 1995 but prior to May 29, 2000)

The patent term extension is 0 days. Any patent to issue from the above identified application will include an indication of the 0 day extension on the front page.

If a continued prosecution application (CPA) was filed in the above-identified application, the filing date that determines patent term extension is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) system. (http://pair.uspto.gov)

Any questions regarding the patent term extension or adjustment determination should be directed to the Office of Patent Legal Administration at (703)305-1383.

PTOL-85 (REV. 05-03) Approved for use through 04/30/2004.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/504,344 | 02/14/2000 | Cathal G. Phelan | 0325.000309 | 7771 |

| | | | EXAMINER |
|---|---|---|---|
| 021363 | 7590 | 06/16/2003 | NAMAZI, MEHDI |

CHRISTOPHER P. MAIORANA, P.C.
24025 GREATER MACK
SUITE 200
ST. CLAIR SHORES, MI 48080
UNITED STATES

| ART UNIT | PAPER NUMBER |
|---|---|
| 2188 | 13 |

DATE MAILED: 06/16/2003

# Notice of Fee Increase on January 1, 2003

If a reply to a "Notice of Allowance and Fee(s) Due" is filed in the Office on or after January 1, 2003, then the amount due will be higher than that set forth in the "Notice of Allowance and Fee(s) Due" since there will be an increase in fees effective on January 1, 2003. See Revision of Patent and Trademark Fees for Fiscal Year 2003: Final Rule, 67 Fed. Reg. 70847, 70849 (November 27, 2002).

The current fee schedule is accessible from: http://www.uspto.gov/main/howtofees.htm.

If the issue fee paid is the amount shown on the "Notice of Allowance and Fee(s) Due," but not the correct amount in view of the fee increase, a "Notice to Pay Balance of Issue Fee" will be mailed to applicant. In order to avoid processing delays associated with mailing of a "Notice to Pay Balance of Issue Fee," if the response to the Notice of Allowance and Fee(s) due form is to be filed on or after January 1, 2003 (or mailed with a certificate of mailing on or after January 1, 2003), the issue fee paid should be the fee that is required at the time the fee is paid. If the issue fee was previously paid, and the response to the "Notice of Allowance and Fee(s) Due" includes a request to apply a previously-paid issue fee to the issue fee now due, then the difference between the issue fee amount at the time the response is filed and the previously paid issue fee should be paid. See Manual of Patent Examining Procedure, Section 1308.01 (Eighth Edition, August 2001).

Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

PTOL-85 (REV. 05-03) Approved for use through 04/30/2004.

| L Number | Hits | Search Text | DB | Time stamp |
|---|---|---|---|---|
| 1 | 97346 | (burst or ((continuous$3 or serial$3) near2 access$3)) | USPAT; EPO; JPO; DERWENT; IBM_TDB | 2003/06/13 14:51 |
| 2 | 38384 | fixed near2 length | USPAT; EPO; JPO; DERWENT; IBM_TDB | 2003/06/13 14:52 |
| 3 | 2561 | ((burst or ((continuous$3 or serial$3) near2 access$3))) and (fixed near2 length ) | USPAT; EPO; JPO; DERWENT; IBM_TDB | 2003/06/13 14:52 |
| 4 | 28 | (non-interrupt$4 or noninteruppt$4 or (non adj interrupt$4) or uninterrupt$4) with address with generat$4 | USPAT; EPO; JPO; DERWENT; IBM_TDB | 2003/06/13 14:54 |
| 5 | 82 | (non-interrupt$4 or noninteruppt$4 or (non adj interrupt$4) or uninterrupt$4) same (address with generat$4) | USPAT; EPO; JPO; DERWENT; IBM_TDB | 2003/06/13 14:55 |
| 6 | 3 | (((burst or ((continuous$3 or serial$3) near2 access$3))) and (fixed near2 length )) and ((non-interrupt$4 or noninteruppt$4 or (non adj interrupt$4) or uninterrupt$4) same (address with generat$4)) | USPAT; EPO; JPO; DERWENT; IBM_TDB | 2003/06/13 14:56 |

| | |
|---|---|
| Group Art Unit: | 2188 |
| Examiner: | Namazi, M. |
| Applicants: | Cathal G. Phelan |
| Serial No: | 09/504,344 |
| Filing Date: | February 14, 2000 |
| For: | MEMORY DEVICE WITH FIXED LENGTH NON-INTERRUPTIBLE BURST |

## DRAWING TRANSMITTAL
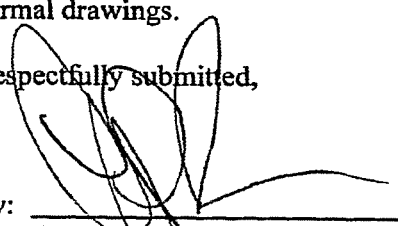
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Notice of Allowance mailed June 16, 2003 indicating that formal drawings are due, enclosed are three (3) sheets of formal drawings.

Respectfully submitted,

By: _____
Christopher P. Maiorana
Registration No. 42,829
CHRISTOPHER P. MAIORANA, P.C.
24025 Greater Mack, Suite 200
St. Clair Shores, Michigan 48080
(586) 498-0670
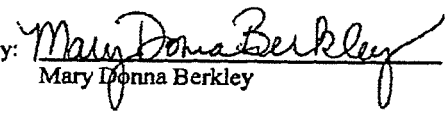
Date: September 15, 2003

Attorney Docket No.: 0325.00309

## CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service via First Class Mail in an envelope with sufficient postage and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on September 15, 2003 .

By: _____
Mary Donna Berkley

FIG. 1



FIG. 2

FIG. 3



FIG. 4

4-FIXED-BURST READ/WRITE/READ TIMING

FIG. 5A

8-FIXED-BURST READ/WRITE/READ TIMING
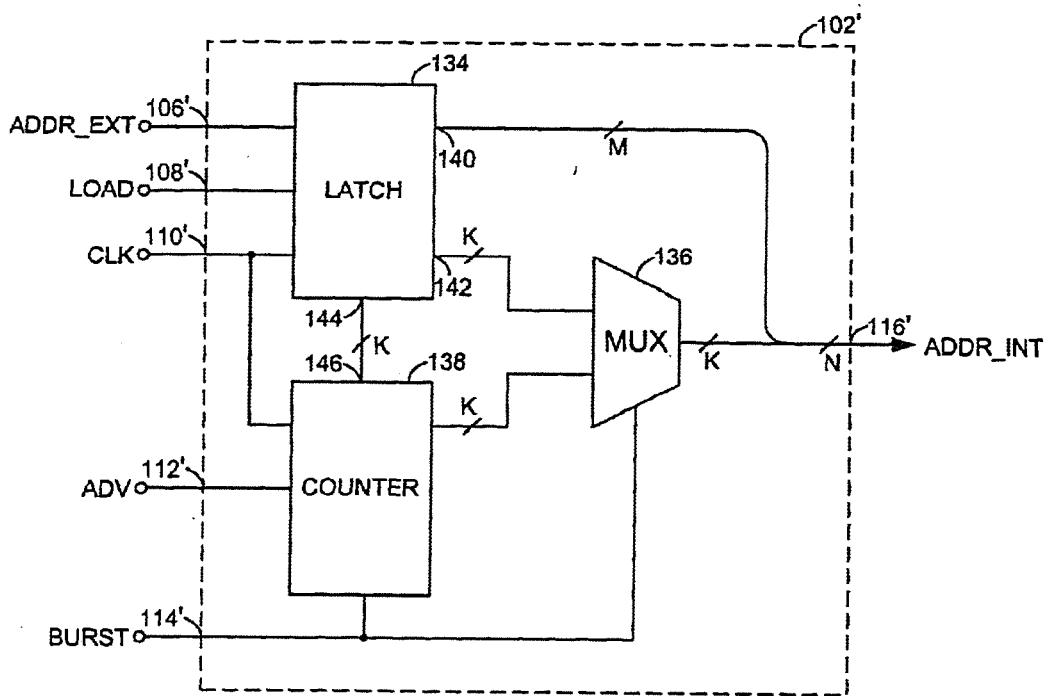
FIG. 5B

FIG. 6

# PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail** Mail Stop ISSUE FEE
Commissioner for Patents
Alexandria, Virginia 22313-1450
**Fax** (703)746-4000

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

021363    7590    06/16/2003

CHRISTOPHER P. MAIORANA, P.C.
24025 GREATER MACK
SUITE 200
ST. CLAIR SHORES, MI 48080

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

**Certificate of Mailing or Transmission**
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above, or being facsimile transmitted to the USPTO, on the date indicated below.

Mary Donna Berkley _(Depositor's name)_

_Mary Donna Berkley_ _(Signature)_

September 15, 2003 _(Date)_

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/504,344 | 02/14/2000 | Cathal G. Phelan | 0325.000309 | 7771 |

TITLE OF INVENTION: MEMORY DEVICE WITH FIXED LENGTH NON-INTERRUPTIBLE BURST

| APPLN. TYPE | SMALL ENTITY | ISSUE FEE | PUBLICATION FEE | TOTAL FEE(S) DUE | DATE DUE |
|---|---|---|---|---|---|
| nonprovisional | NO | $1300 | $0 | $1300 | 09/16/2003 |

| EXAMINER | ART UNIT | CLASS-SUBCLASS |
|---|---|---|
| NAMAZI, MEHDI | 2188 | 711-104000 |

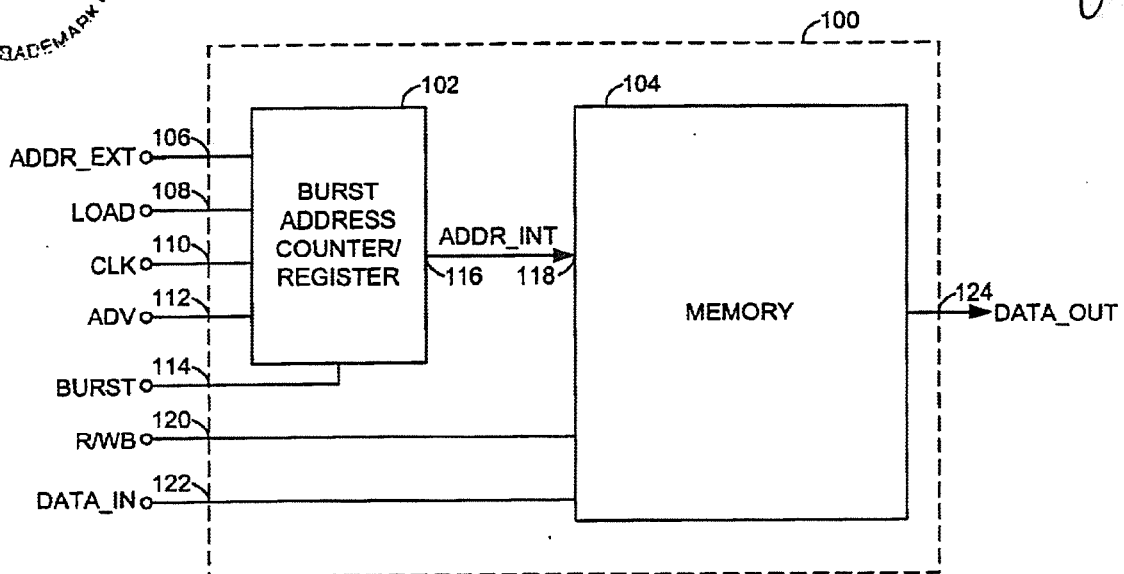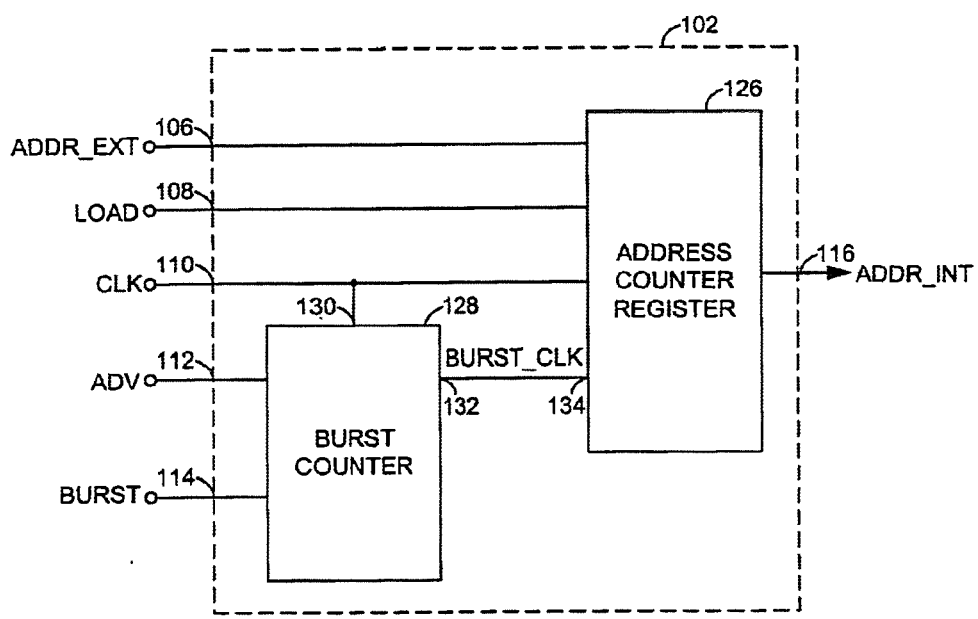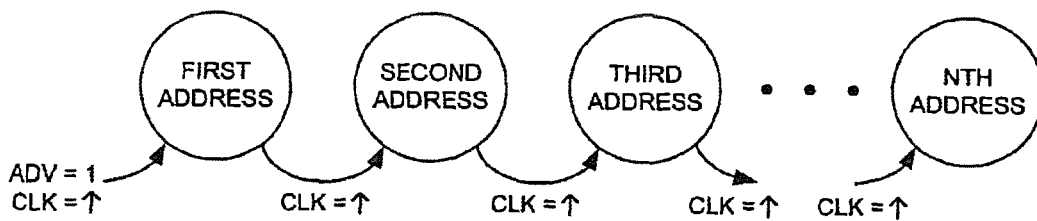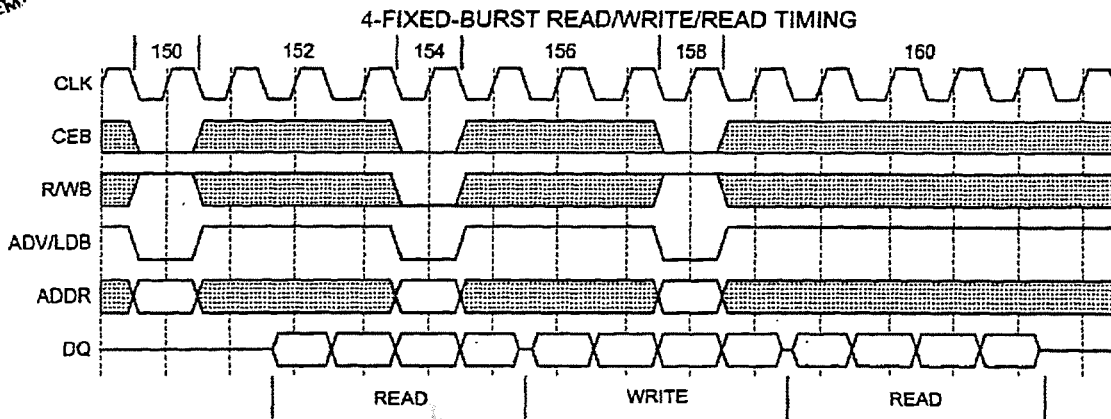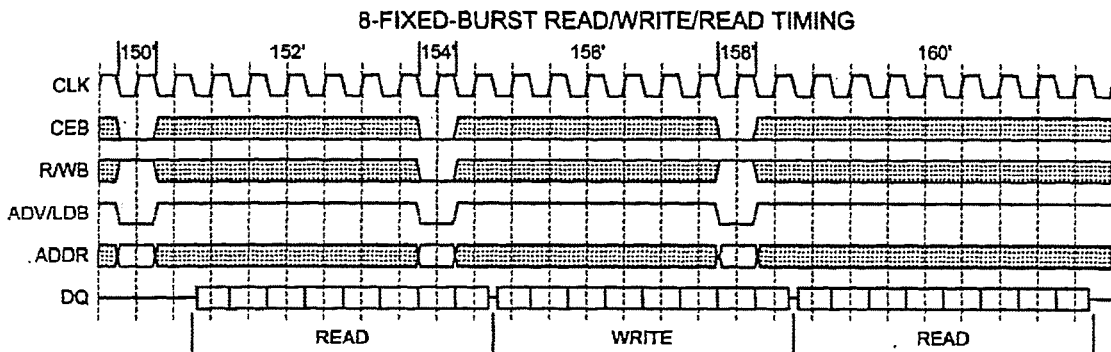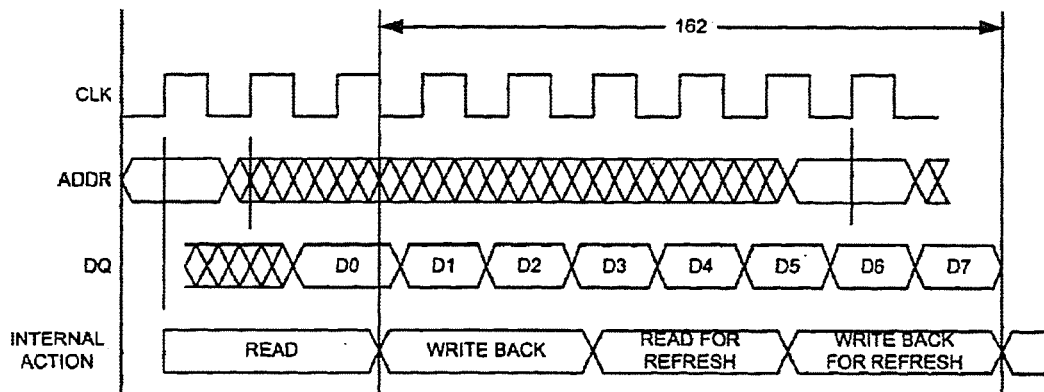1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1. Christopher P. Maiorana, P.C.

2. Robert M. Miller

3. _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the USPTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE    (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Cypress Semiconductor Corp.    San Jose, CA

Please check the appropriate assignee category or categories (will not be printed on the patent)    ❑ individual    ☒ corporation or other private group entity    ❑ government

4a. The following fee(s) are enclosed:
☒ Issue Fee
❑ Publication Fee
❑ Advance Order - # of Copies _____

4b. Payment of Fee(s):
❑ A check in the amount of the fee(s) is enclosed.
☒ Payment by credit card. Form PTO-2038 is attached. _Declined per Greg Gansle on a date_
☒ The Commissioner is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _50-0541_ (enclose an extra copy of this form).

Commissioner for Patents is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

(Authorized Signature)    (Date) 09/15/03

Christopher P. Maiorana (42,829)

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMIT THIS FORM WITH FEE(S)

PTOL-85 (REV. 05-03) Approved for use through 04/30/2004. OMB 0651-0033    U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

US006651134B1

(12) **United States Patent**
Phelan

(10) **Patent No.:** **US 6,651,134 B1**
(45) **Date of Patent:** **Nov. 18, 2003**

(54) **MEMORY DEVICE WITH FIXED LENGTH NON INTERRUPTIBLE BURST**

(75) Inventor: **Cathal G. Phelan**, Mountain View, CA (US)

(73) Assignee: **Cypress Semiconductor Corp.**, San Jose, CA (US)

( * ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/504,344**

(22) Filed: **Feb. 14, 2000**

(51) Int. Cl.$^7$ ............................................. **C06F 12/00**
(52) **U.S. Cl.** ...................... **711/104**; 711/105; 711/167; 711/169; 710/35; 365/233; 365/238.5
(58) **Field of Search** ........................ 711/104–105, 169, 711/167; 365/233, 238.5; 710/35

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,651,138 A * 7/1997 Le et al. ...................... 711/154
5,729,504 A * 3/1998 Cowles ........................ 365/236
5,805,928 A * 9/1998 Lee .............................. 710/35

5,936,975 A * 8/1999 Okamura .................... 714/719
5,966,724 A * 10/1999 Ryan ......................... 711/105
6,085,261 A * 7/2000 McIntyre, Jr. et al. ........ 710/35
6,289,138 B1 * 9/2001 Yip et al. ................... 382/307

OTHER PUBLICATIONS

Understanding Burst Modes in Synchronous SRAMs, Cypress Semiconductor Corp., Jun. 30, 1999.

* cited by examiner

*Primary Examiner*—Donald Sparks
*Assistant Examiner*—Medhi Namazi
(74) *Attorney, Agent, or Firm*—Christopher P. Maiorana, P.C.; Robert M. Miller

(57) **ABSTRACT**

An integrated circuit comprising a memory and a logic circuit. The memory may comprise a plurality of storage elements each configured to read and write data in response to an internal address signal. The logic circuit may be configured to generate a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals. The generation of the predetermined number of internal address signals may be non-interruptible.

21 Claims, 3 Drawing Sheets



4-FIXED-BURST READ/WRITE/READ TIMING



8-FIXED-BURST READ/WRITE/READ TIMING

**FIG. 1**



**FIG. 2**

## FIG. 3

## FIG. 4

4-FIXED-BURST READ/WRITE/READ TIMING



**FIG. 5A**

8-FIXED-BURST READ/WRITE/READ TIMING
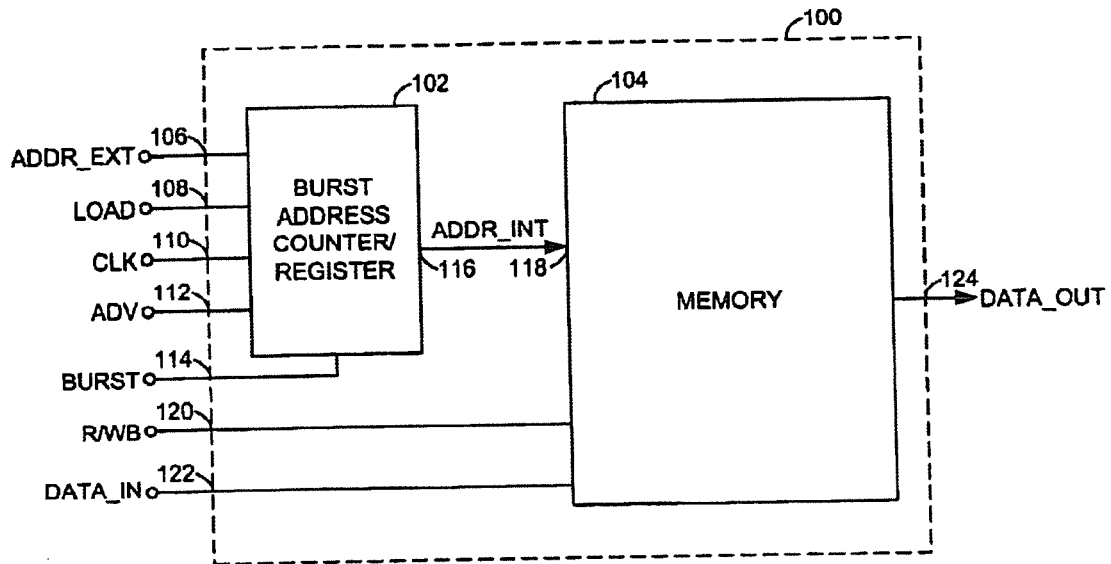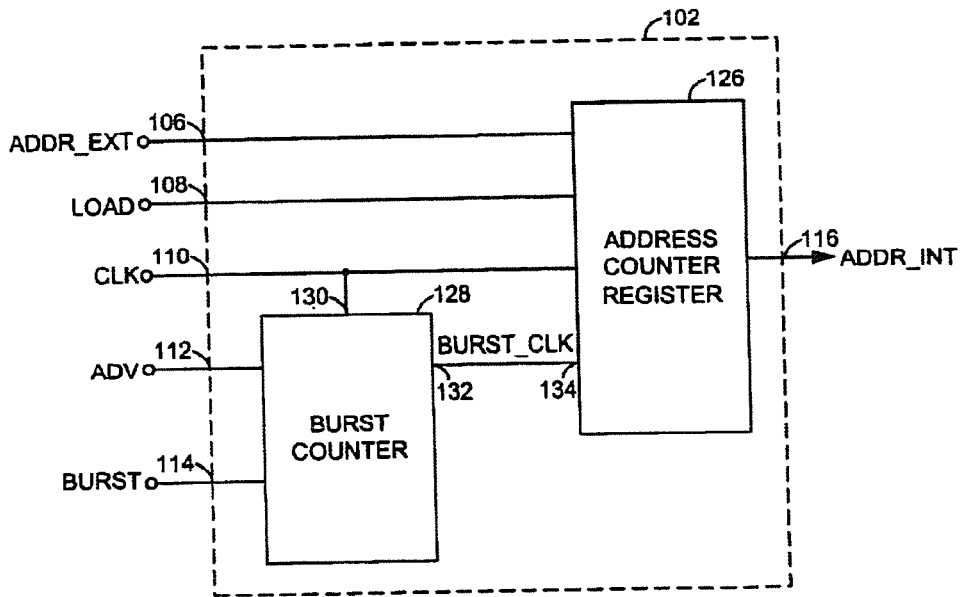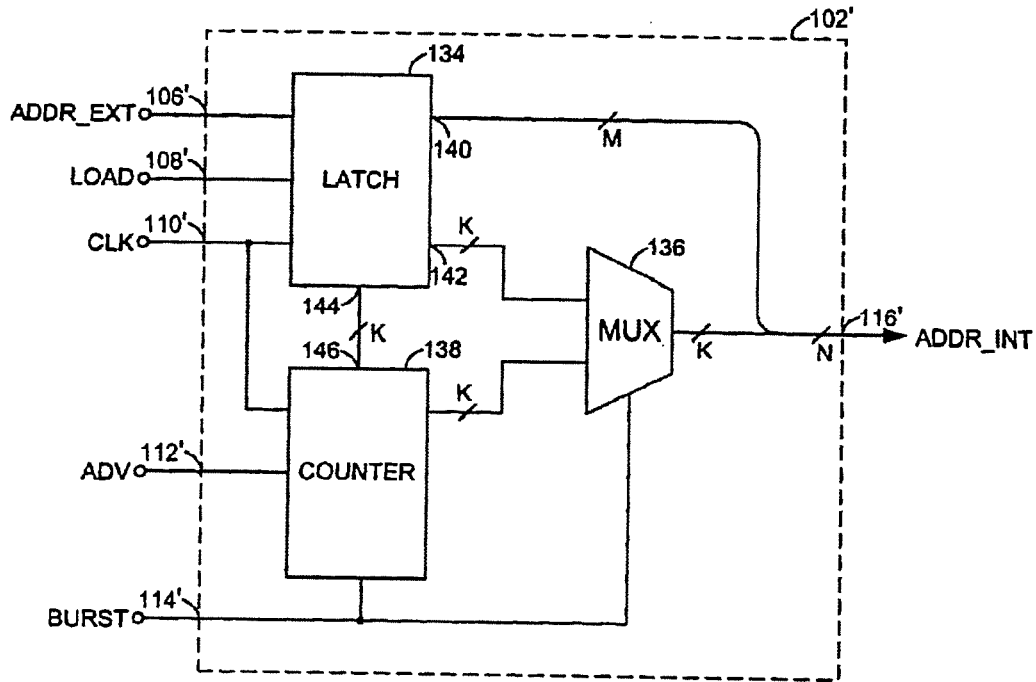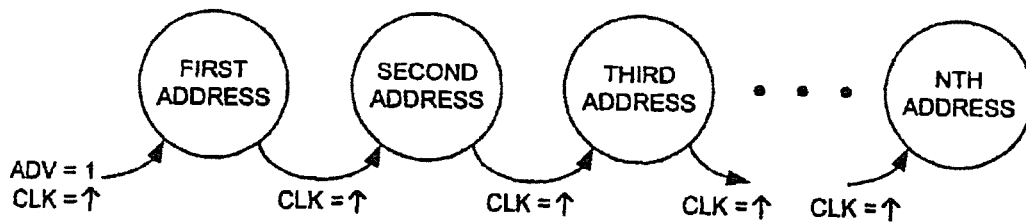


**FIG. 5B**



**FIG. 6**

# MEMORY DEVICE WITH FIXED LENGTH NON INTERRUPTIBLE BURST

## FIELD OF THE INVENTION

The present invention relates to memory devices generally and, more particularly, to a memory device that transfers a fixed number of words of data with each access.

## BACKGROUND OF THE INVENTION

A synchronous Static Random Access Memory (SRAM) can provide data from multiple address locations using a single address. Accessing multiple locations in response to a single address is called a burst mode access. A memory device that provides a burst mode can reduce activity on the address and control buses. The burst mode of a conventional synchronous SRAM can be started and stopped in response to a control signal.

A conventional Dynamic Random Access Memory (DRAM) preserves data during periodic absences of power by implementing a memory cell as a capacitor and an access transistor. Since the charge on the capacitor will slowly leak away, the cells need to be "refreshed" once every few milliseconds. Depending on the frequency of accesses, a conventional DRAM can need an interrupt to perform data refreshes. Using a DRAM in a burst application is difficult because of the need to refresh. Completely hiding refresh cycles (e.g., refreshing data without the need for interrupts) in a DRAM cannot happen with conventional memory devices due to architecture choices that have been made. Data word bursts can be interrupted while in progress since conventional architectures support both burst and single access modes. Conventional DRAM access takes about 10 ns to get data, but nearly 20 ns to complete writeback and equalization. The addition of another 20 ns for a refresh results in a total access of 40 ns.

Since the data burst transfers of conventional memories can be interrupted and single accesses made, the amount of time that the data, address and control busses are not in use can vary. The variability of bus availability complicates the design of systems with shared data, address and control busses.

It would be desirable to have a memory device that has a fixed burst length.

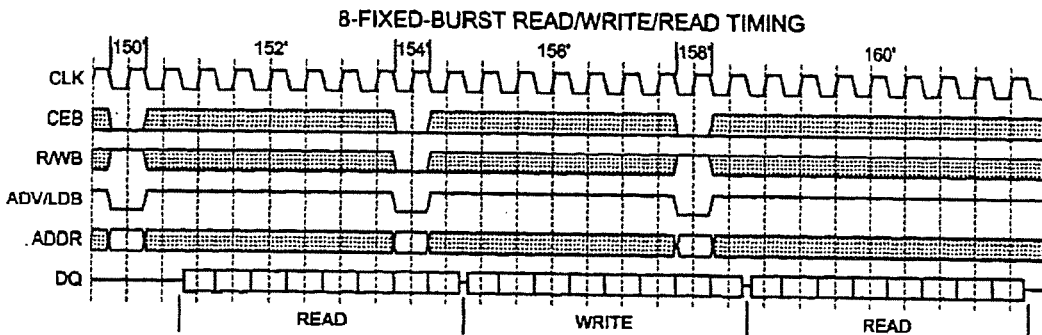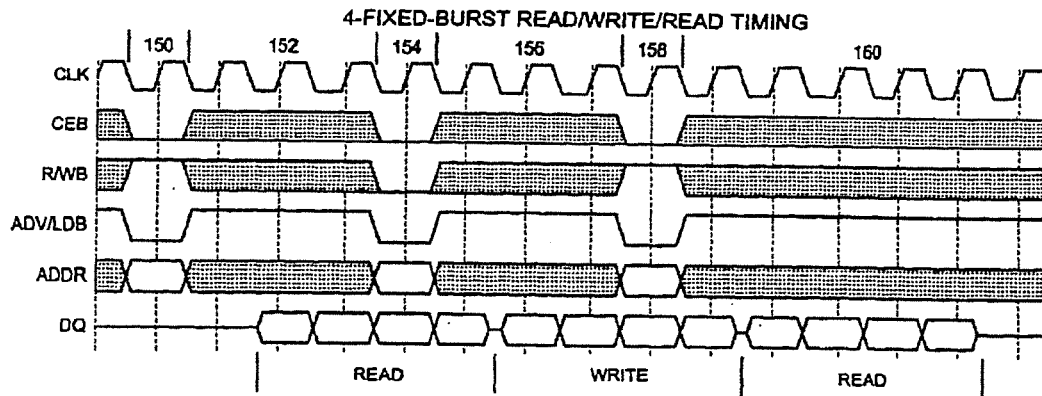## SUMMARY OF THE INVENTION

The present invention concerns an integrated circuit comprising a memory and a logic circuit. The memory may comprise a plurality of storage elements each configured to read and write data in response to an internal address signal. The logic circuit may be configured to generate a predetermined number of the internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals. The generation of the predetermined number of internal address signals may be non-interruptible.

The objects, features and advantages of the present invention include providing a fixed burst memory that may (i) give network customers who typically burst large data lengths the ability to set a fixed burst length that suits particular needs; (ii) have non-interruptible bursts; (iii) free up the address bus and control bus for a number of cycles; (iv) provide programmability for setting the burst length by using DC levels [Vss or Vcc] on external pins; (v) hide required DRAM refreshes inside a known fixed burst length of data words; and/or (vi) operate at higher frequencies without needing interrupts to perform refreshes of data.

## BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects, features and advantages of the present invention will be apparent from the following detailed description and the appended claims and drawings in which:

FIG. 1 is a block diagram illustrating a preferred embodiment of the present invention;

FIG. 2 is a detailed block diagram illustrating a circuit 102 of FIG. 1;

FIG. 3 is a detailed block diagram of a circuit 102' illustrating an alternative embodiment of the circuit 102 of FIG. 1;

FIG. 4 is a flow diagram illustrating an example burst address sequence;

FIGS. 5A and 5B are diagrams illustrating example operations of a 4 word (FIG. 5A) and an 8 word (FIG. 5B) fixed burst access in accordance with the present invention; and

FIG. 6 is a diagram illustrating an example operation where a burst length may be long enough to include a writeback and a refresh cycle.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. 1, a block diagram of a circuit 100 is shown in accordance with a preferred embodiment of the present invention. The circuit 100 may be implemented, in one example, as a fixed burst memory. The circuit 100 may be configured to transfer a fixed number of words of data with each access (e.g., read or write). A number of words transferred as a group is called a burst. The circuit 100 generally comprises a circuit 102 and a memory array (or circuit) 104. The circuit 102 may be implemented, in one example, as a burst address counter/register. The memory array 104 may be implemented, in one example, as a static random access memory (SRAM), a dynamic random access memory (DRAM), or other appropriate memory to meet the design criteria of a particular implementation.

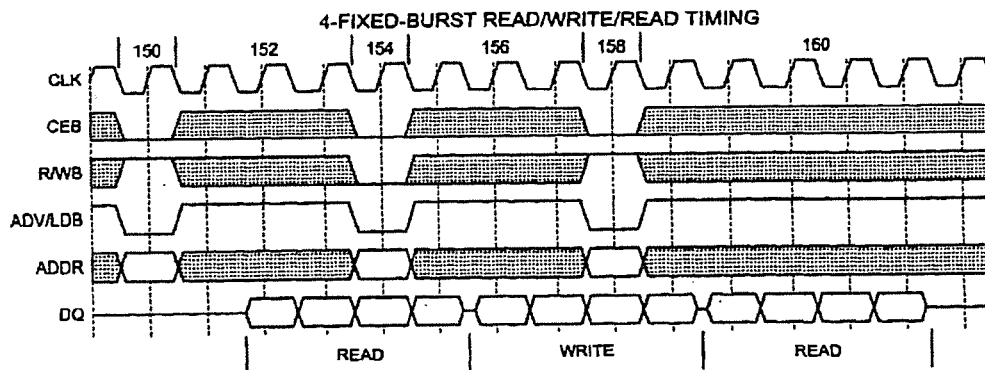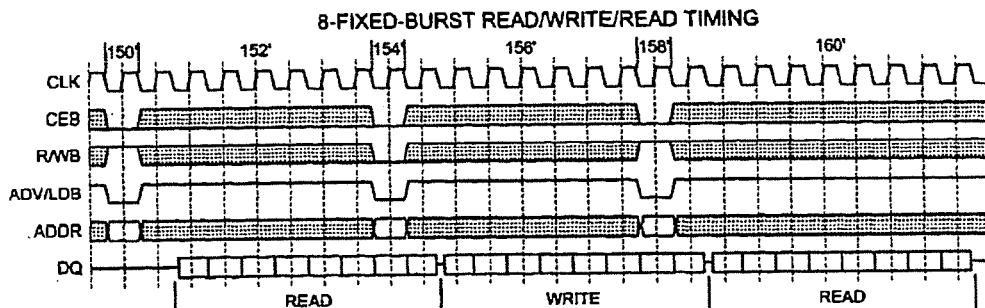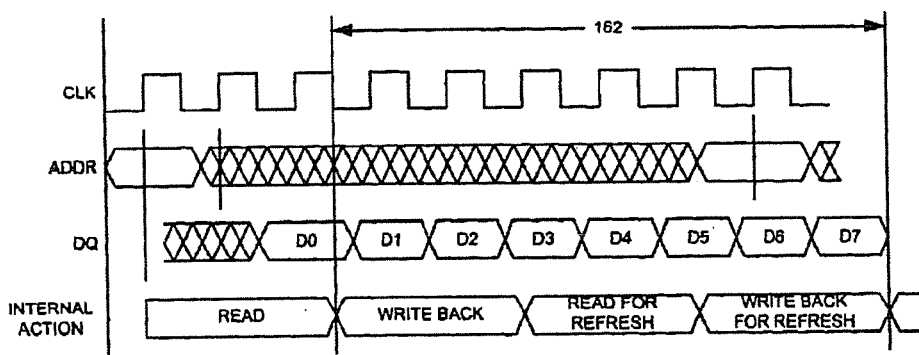The circuit 102 may have an input 106 that may receive a signal (e.g., ADDR_EXT), an input 108 that may receive a signal (e.g., LOAD), an input 110 that may receive a signal (e.g., CLK), an input 112 that may receive a signal (e.g., ADV), and an input 114 that may receive a signal (e.g., BURST). The circuit 102 may have an output 116 that may present a signal (e.g., ADDR_INT) to an input 118 of the memory 104. The memory 104 may have an input 120 that may receive a signal (e.g., R/Wb), an input 122 that may receive a signal (e.g., DATA_IN) and an output 122 that may present a signal (e.g., DATA_OUT). The various signals are generally "on" (e.g., a digital HIGH, or 1) or "off" (e.g., a digital LOW, or 0). However, the particular polarities of the on (e.g., asserted) and off (e.g., de-asserted) states of the signals may be adjusted (e.g., reversed) accordingly to meet the design criteria of a particular implementation.

The signal ADDR_EXT may be, in one example, an external address signal. The signal ADDR_EXT may be n-bits wide, where n is an integer. The signal CLK may be a clock signal. The signal R/Wb may be a control signal that may be in a first state or a second state. When the signal R/Wb is in the first state, the circuit 100 will generally read data from the memory circuit 104 for presentation as the signal DATA_OUT. When the signal R/Wb is in the second state, the circuit 100 will generally store data received as the signal DATA_IN.

The signal LOAD may be, in one example, an address load control signal. The circuit 100 may be configured to

load an initial address, presented by the signal ADDR_EXT, in response to the signal LOAD. The initial address may determine the initial location where data transfers to and from the memory 104 will generally begin.

The signal ADV may be, in one example, used as a control signal. The circuit 100 may be configured to transfer a fixed number of words to or from the memory 104 in response to the signals ADV, CLK and R/Wb. When the signal ADV is asserted, the circuit 100 will generally begin transferring a predetermined number of words. The transfer is generally non-interruptible. In one example, the signal ADV may initiate the generation of a number of addresses for presentation as the signal ADDR_INT.

The signals ADV and LOAD may be, in one example, a single signal (e.g., ADV/LDb). The signal ADV/LDb may be a control signal that may be in a first state or a second state. When the signal ADV/LDb is in the first state, the circuit 102 will generally load an address presented by the signal ADDR_EXT as an initial address. When the signal ADV/LDb is in the second state, the circuit 102 may be configured to generate the signal ADDR_INT as a fixed number of addresses in response to the signal CLK. The signal ADDR_INT may be, in one example, an internal address signal. The signal ADDR_INT may be n-bits wide. Once the circuit 102 has started generating the fixed number of addresses, the circuit 102 will generally not stop until the fixed number of addresses has been generated (e.g., a non-interruptible burst).

The signal BURST may be, in one example, a configuration signal for programming the fixed number of addresses that the circuit 102 may generate in response to the signals CLK and ADV/LDb. The signal BURST may be generated, in one example, by (i) using bond options, (ii) voltage levels applied to external pins, or (iii) other appropriate signal generation means.

When the memory 104 is implemented as a DRAM, the circuit 100 may be configured to hide required DRAM refreshes (e.g., refreshes may occur without affecting external environment) inside a known fixed burst length of data words. The fixed burst length may allow the circuit 100 to operate at higher frequencies than a conventional DRAM without needing interrupts to perform refreshes of data. In one example, the fixed burst length may be four or eight words. However, the burst length may be set to whatever length is necessary to meet the design criteria of a particular application. For example, the burst length may be programmed, in one example, to allow both writeback and refresh to occur within a single access. The fixed burst-length may be set, in one example, longer or shorter depending upon a frequency or technology to be used.

The circuit 100 may be configured to provide a fixed burst length that may suit the requirements of network customers who typically burst large data lengths. By providing a fixed burst length, the circuit 100 may allow shared usage of data, address and control busses. A fixed length non-interruptible burst generally frees up the address bus and control bus for a known number of cycles. The address and control busses may be shared by a number of memory devices. The circuit 100 may provide a more reliable and/or accurate burst than is possible with multiple chips.

Referring to FIG. 2, a detailed block diagram illustrating implementation of the circuit 102 is shown. The circuit 102 may comprise an address counter register 126 and a burst counter 128. The address counter register 126 generally receives the signals ADDR_EXT, LOAD, and CLK. The address counter register 126 may be configured to present

the signal ADDR_INT. The signal ADV and the signal BURST may be presented to a burst counter 128. The signal CLK may be presented at an input 130 of the burst counter 128. The burst counter 128 may have an output 132 that may present a signal (e.g., BURST_CLK) at an input 134 of the circuit 126. An initial address may be loaded into the address counter register 126 by presenting the initial address in the signal ADDR_EXT and asserting the signal LOAD. The circuit 126 may be configured to increment an address in response to the signal BURST_CLK. When the signal ADV is asserted, the burst counter 128 will generally present the signal BURST_CLK in response to the signal CLK. The signal BURST_CLK generally contains a number of pulses that has been programmed by the signal BURST.

Referring to FIG. 3, a detailed block diagram illustrating an alternative embodiment of the circuit 102 is shown. The circuit 102' may comprise a latch 134, a multiplexer 136 and a counter 138. The signals ADDR_EXT, LOAD and CLK may be presented to the latch 134. The latch 134 may have an output 140 that may present a portion (e.g., m bits, where m is an integer smaller than n) of the signal ADDR_EXT as a portion of the signal ADDR_INT, an output 142 that may present a second portion (e.g., k bits, where k is an integer smaller than n) of the signal ADDR_EXT to a first input of the multiplexer 136, and an output 144 that may present the second portion of the signal ADDR_EXT to an input 146 of the counter 138.

The signals ADV, CLK and BURST may be presented to inputs of the counter 138. The counter 138 may be configured to generate a number of addresses in response to the signals CLK, BURST and ADV. The number of addresses generated by the counter 138 may be programmed by the signal BURST.

The signal BURST may be presented to a control input of the multiplexer 136. The multiplexer 136 may select between a number of signals from the latch 134 and a number of signals from the counter 138 to be presented as a second portion of the signal ADDR_INT in response to the signal BURST.

Referring to FIG. 4, a flow diagram illustrating an example burst address sequence is shown. When the signal ADV is asserted, the circuit 100 will generally generate a number of address signals, for example, N where N is an integer. The address signals may be generated, in one example, on a rising edge of the signal CLK. The address signals will generally continue to be generated until the Nth address signal is generated.

Referring to FIGS. 5A and 5B, timing diagrams illustrating example operations for a four word (FIG. 5A) and an eight word (FIG. 5B) fixed burst memory in accordance with the present invention are shown. The timing diagrams generally illustrate externally measurable signals for four and eight word fixed burst read/write architectures. In general, an operation (e.g., read or write) of the circuit 100 begins with loading an initial address (e.g., portions 150, 154, and 158 of FIG. 5A; portions 150', 154', and 158' of FIG. 5B). Starting with the initial address, a fixed number of words are generally transferred (e.g., line DQ of FIGS. 5A and 5B). During the transfer of the fixed number of words, the address and control buses (e.g., ADDR, CE, R/W, etc.) are generally available to other devices (e.g., portions 152, 156, and 160 of FIG. 5A; portions 152', 156', and 160' of FIG. 5B). In one example, the control and address bus activity may be one-fourth (FIG. 5A) or one-eighth (FIG. 5B) the data bus activity (e.g., compare line ADDR with line DQ of FIGS. 5A and 5B). The reduced bus activity may be an effect of the

architecture. The data bus may be, in one example, active nearly 100% of the time (e.g., line DQ of FIGS. 5A and 5B) In one example, there may be no inefficiencies switching from read to write to read etcetera (e.g., see labels under line DQ of FIGS. 5A and 5B).

Referring to FIG. 6, a timing diagram illustrating a fixed burst length long enough to hide a writeback and a refresh cycle is shown. Internally the action being performed may completely hide DRAM refresh activity inside nominal external activities. A portion 162 illustrates that refresh activity (e.g., writeback, read for refresh, and writeback for refresh) may be completed within the time of the burst transfer. When a fixed burst long enough to completely hide refresh activity is provided, there may be no penalty for using DRAM instead of SRAM for the memory 104.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. A circuit comprising:

a memory comprising a plurality of storage elements each configured to read and write data in response to an internal address signal; and

a logic circuit configured to generate a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

2. The circuit according to claim 1, wherein said predetermined number of internal address signals is determined by a fixed burst length.

3. The circuit according to claim 1, wherein said predetermined number of internal address signals is at least 4.

4. The circuit according to claim 1, wherein said predetermined number of internal address signals is 8.

5. The circuit according to claim 2, wherein said fixed burst length is programmable.

6. The circuit according to claim 5, wherein said fixed burst length is programmed by bond options.

7. The circuit according to claim 5, wherein said fixed burst length is programmed by voltage levels on external pins.

8. The circuit according to claim 1, wherein said memory comprises a static random access memory.

9. The circuit according to claim 1, wherein said memory comprises a dynamic random access memory.

10. The circuit according to claim 9, wherein said predetermined number of internal address signals is chosen to provide time for at least one writeback or refresh cycle.

11. The circuit according to claim 1, wherein said predetermined number of internal address signals is chosen to meet predetermined criteria for sharing address and control busses.

12. The circuit according to claim 1, wherein said logic circuit comprises a counter configured to generate said predetermined number of internal address signals.

13. The circuit according to claim 1, wherein said external address signal comprises an initial address for data transfers to and from said memory.

14. A memory device according to claim 1, wherein said circuit is an integrated circuit.

15. The circuit according to claim 1, further comprising address and control busses configured to present said external address signal and said one or more control signals, wherein said busses are freed up during the generation of said predetermined number of internal address signals.

16. A circuit comprising:

means for reading data from and writing data to a plurality of storage elements in response to a plurality of internal address signals; and

means for generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

17. A method of providing a fixed burst length data transfer comprising the steps of:

accessing a memory in response to a plurality of internal address signals; and

generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) a control signal, wherein said generation of said predetermined number of internal address signals is non-interruptible.

18. The method according to claim 17, further comprising the step of programming said predetermined number.

19. The method according to claim 18, wherein said programming step is performed using bond options.

20. The method according to claim 18, wherein said programming step is performed using voltage levels.

21. The method according to claim 17, further comprising the step of selecting said predetermined number to provide time for at least one writeback or refresh cycle.

* * * * *

# PATENT APPLICATION FEE DETERMINATION RECORD
## Effective December 29, 1999

**Application or Docket Number** 09|504344

## CLAIMS AS FILED - PART I

| FOR | (Column 1) NUMBER FILED | (Column 2) NUMBER EXTRA |
|---|---|---|
| BASIC FEE | | |
| TOTAL CLAIMS | 17 minus 20= | * |
| INDEPENDENT CLAIMS | 3 minus 3 = | * |
| MULTIPLE DEPENDENT CLAIM PRESENT | | |

\* If the difference in column 1 is less than zero, enter "0" in column 2

| SMALL ENTITY TYPE ☐ | | | OR | OTHER THAN SMALL ENTITY | |
|---|---|---|---|---|---|
| | RATE | FEE | | RATE | FEE |
| | | 345.00 | OR | | 690.00 |
| | X$ 9= | | OR | X$18= | |
| | X39= | | OR | X78= | |
| | +130= | | OR | +260= | |
| | TOTAL | | OR | TOTAL | 690 |

## CLAIMS AS AMENDED - PART II

### AMENDMENT A

| | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA |
|---|---|---|---|---|
| Total | * 20 | Minus | ** 20 | = 1 |
| Independent | * 3 | Minus | *** 3 | = 1 |
| FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM | | | | |

| SMALL ENTITY | | OR | OTHER THAN SMALL ENTITY | |
|---|---|---|---|---|
| RATE | ADDI-TIONAL FEE | | RATE | ADDI-TIONAL FEE |
| X$ 9= | | OR | X$18= | |
| X39= | | OR | X78= | |
| +130= | | OR | +260= | |
| TOTAL ADDIT. FEE | | OR | TOTAL ADDIT. FEE | |

### AMENDMENT B

| | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA |
|---|---|---|---|---|
| Total | * 21 | Minus | ** 20 | = 1 |
| Independent | * 3 | Minus | *** 3 | = |
| FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM | | | | |

| RATE | ADDI-TIONAL FEE | | RATE | ADDI-TIONAL FEE |
|---|---|---|---|---|
| X$ 9= | | OR | X$18= | 18.00 |
| X39= | | OR | X78= | |
| +130= | | OR | +260= | |
| TOTAL ADDIT. FEE | | OR | TOTAL ADDIT. FEE | |

### AMENDMENT C

| | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA |
|---|---|---|---|---|
| Total | * | Minus | ** | = |
| Independent | * | Minus | *** | = |
| FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM | | | | |

| RATE | ADDI-TIONAL FEE | | RATE | ADDI-TIONAL FEE |
|---|---|---|---|---|
| X$ 9= | | OR | X$18= | |
| X39= | | OR | X78= | |
| +130= | | OR | +260= | |
| TOTAL ADDIT. FEE | | OR | TOTAL ADDIT. FEE | |

\* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
\*\* If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
\*\*\*If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

FORM PTO-875
(Rev. 12/99)

Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

# MULTIPLE DEPENDENT CLAIM FEE CALCULATION SHEET
### (FOR USE WITH FORM PTO-876)

## CLAIMS

| Claim | AS FILED IND. | AS FILED DEP. | AFTER 1st AMENDMENT IND. | AFTER 1st AMENDMENT DEP. | AFTER 2nd AMENDMENT IND. | AFTER 2nd AMENDMENT DEP. |
|---|---|---|---|---|---|---|
| 1 | 1 | | | | | |
| 2 | | 1 | | | | |
| 3 | | 1 | | | | |
| 4 | | 1 | | | | |
| 5 | | 1 | | | | |
| 6 | | 1 | | | | |
| 7 | | 1 | | | | |
| 8 | | 1 | | | | |
| 9 | | 1 | | | | |
| 10 | | 1 | | | | |
| 11 | | 1 | | | | |
| 12 | 1 | | | | | |
| 13 | 1 | | | | | |
| 14 | | 1 | | | | |
| 15 | | | | | | |
| 16 | | | | | | |
| 17 | | | | | | |
| 18 | | | | | | |
| 19 | | | | | | |
| 20 | | | | | | |
| 21 | | | | | | |
| 22 | | | | | | |
| 23 | | | | | | |
| 24 | | | | | | |
| 25 | | | | | | |
| 26 | | | | | | |
| 27 | | | | | | |
| 28 | | | | | | |
| 29 | | | | | | |
| 30 | | | | | | |
| 31 | | | | | | |
| 32 | | | | | | |
| 33 | | | | | | |
| 34 | | | | | | |
| 35 | | | | | | |
| 36 | | | | | | |
| 37 | | | | | | |
| 38 | | | | | | |
| 39 | | | | | | |
| 40 | | | | | | |
| 41 | | | | | | |
| 42 | | | | | | |
| 43 | | | | | | |
| 44 | | | | | | |
| 45 | | | | | | |
| 46 | | | | | | |
| 47 | | | | | | |
| 48 | | | | | | |
| 49 | | | | | | |
| 50 | | | | | | |
| TOTAL IND. | 3 | | | | | |
| TOTAL DEP. | 14 | | | | | |
| TOTAL | 17 | | | | | |

| Claim | IND. | DEP. | IND. | DEP. | IND. | DEP. |
|---|---|---|---|---|---|---|
| 51 | | | | | | |
| 52 | | | | | | |
| 53 | | | | | | |
| 54 | | | | | | |
| 55 | | | | | | |
| 56 | | | | | | |
| 57 | | | | | | |
| 58 | | | | | | |
| 59 | | | | | | |
| 60 | | | | | | |
| 61 | | | | | | |
| 62 | | | | | | |
| 63 | | | | | | |
| 64 | | | | | | |
| 65 | | | | | | |
| 66 | | | | | | |
| 67 | | | | | | |
| 68 | | | | | | |
| 69 | | | | | | |
| 70 | | | | | | |
| 71 | | | | | | |
| 72 | | | | | | |
| 73 | | | | | | |
| 74 | | | | | | |
| 75 | | | | | | |
| 76 | | | | | | |
| 77 | | | | | | |
| 78 | | | | | | |
| 79 | | | | | | |
| 80 | | | | | | |
| 81 | | | | | | |
| 82 | | | | | | |
| 83 | | | | | | |
| 84 | | | | | | |
| 85 | | | | | | |
| 86 | | | | | | |
| 87 | | | | | | |
| 88 | | | | | | |
| 89 | | | | | | |
| 90 | | | | | | |
| 91 | | | | | | |
| 92 | | | | | | |
| 93 | | | | | | |
| 94 | | | | | | |
| 95 | | | | | | |
| 96 | | | | | | |
| 97 | | | | | | |
| 98 | | | | | | |
| 99 | | | | | | |
| 100 | | | | | | |
| TOTAL IND. | | | | | | |
| TOTAL DEP. | | | | | | |
| TOTAL | | | | | | |

ISSUE SLIP STAPLE AREA (for additional cross references)

| POSITION | INITIALS | ID NO. | DATE |
|---|---|---|---|
| | | | |
| FEE DETERMINATION | SM | | 2/23/0 |
| O.I.P.E. CLASSIFIER | | 16 | 3300 |
| FORMALITY REVIEW | | | |
| RESPONSE FORMALITY REVIEW | | | |
| | QM | 64830 | 5·2 |

## INDEX OF CLAIMS

| | | | | | |
|---|---|---|---|---|---|
| ✔ | ................................ Rejected | | N | ................................ | Non-elected |
| = | ................................ Allowed | | I | ................................ | Interference |
| — | (Through numeral)... Canceled | | A | ................................ | Appeal |
| ÷ | ................................ Restricted | | O | ................................ | Objected |

| Claim Final | Original | Date | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | ✓ | ✓ | ✓ | ✓ | | | | | | |
| 2 | 2 | | | | = | | | | | | |
| 3 | 3 | | | | = | | | | | | |
| 4 | 4 | | | | z | | | | | | |
| 5 | 5 | | | | z | | | | | | |
| 6 | 6 | | | | z | | | | | | |
| 7 | 7 | | | | z | | | | | | |
| 8 | 8 | | | | z | | | | | | |
| 9 | 9 | | | | z | | | | | | |
| 1-2 | 10 | | | | z | | | | | | |
| 11 | 11 | | | | z | | | | | | |
| 16 | 12 | | | | = | | | | | | |
| 17 | 13 | | | | z | | | | | | |
| 18 | 14 | | | | z | | | | | | |
| 19 | 15 | | | | z | | | | | | |
| 20 | 16 | | | | z | | | | | | |
| 21 | 17 | ✓ | | | z | | | | | | |
| 12 | 18 | | | | = | | | | | | |
| 13 | 19 | | | | z | | | | | | |
| 14 | 20 | | ✓ | | = | | | | | | |
| 15 | 21 | | | ✓ | z | | | | | | |
| | 22 | | | | | | | | | | |
| | 23 | | | | | | | | | | |
| | 24 | | | | | | | | | | |
| | 25 | | | | | | | | | | |
| | 26 | | | | | | | | | | |
| | 27 | | | | | | | | | | |
| | 28 | | | | | | | | | | |
| | 29 | | | | | | | | | | |
| | 30 | | | | | | | | | | |
| | 31 | | | | | | | | | | |
| | 32 | | | | | | | | | | |
| | 33 | | | | | | | | | | |
| | 34 | | | | | | | | | | |
| | 35 | | | | | | | | | | |
| | 36 | | | | | | | | | | |
| | 37 | | | | | | | | | | |
| | 38 | | | | | | | | | | |
| | 39 | | | | | | | | | | |
| | 40 | | | | | | | | | | |
| | 41 | | | | | | | | | | |
| | 42 | | | | | | | | | | |
| | 43 | | | | | | | | | | |
| | 44 | | | | | | | | | | |
| | 45 | | | | | | | | | | |
| | 46 | | | | | | | | | | |
| | 47 | | | | | | | | | | |
| | 48 | | | | | | | | | | |
| | 49 | | | | | | | | | | |
| | 50 | | | | | | | | | | |

| Claim Final | Original | Date | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | 51 | | | | | | | | | | |
| | 52 | | | | | | | | | | |
| | 53 | | | | | | | | | | |
| | 54 | | | | | | | | | | |
| | 55 | | | | | | | | | | |
| | 56 | | | | | | | | | | |
| | 57 | | | | | | | | | | |
| | 58 | | | | | | | | | | |
| | 59 | | | | | | | | | | |
| | 60 | | | | | | | | | | |
| | 61 | | | | | | | | | | |
| | 62 | | | | | | | | | | |
| | 63 | | | | | | | | | | |
| | 64 | | | | | | | | | | |
| | 65 | | | | | | | | | | |
| | 66 | | | | | | | | | | |
| | 67 | | | | | | | | | | |
| | 68 | | | | | | | | | | |
| | 69 | | | | | | | | | | |
| | 70 | | | | | | | | | | |
| | 71 | | | | | | | | | | |
| | 72 | | | | | | | | | | |
| | 73 | | | | | | | | | | |
| | 74 | | | | | | | | | | |
| | 75 | | | | | | | | | | |
| | 76 | | | | | | | | | | |
| | 77 | | | | | | | | | | |
| | 78 | | | | | | | | | | |
| | 79 | | | | | | | | | | |
| | 80 | | | | | | | | | | |
| | 81 | | | | | | | | | | |
| | 82 | | | | | | | | | | |
| | 83 | | | | | | | | | | |
| | 84 | | | | | | | | | | |
| | 85 | | | | | | | | | | |
| | 86 | | | | | | | | | | |
| | 87 | | | | | | | | | | |
| | 88 | | | | | | | | | | |
| | 89 | | | | | | | | | | |
| | 90 | | | | | | | | | | |
| | 91 | | | | | | | | | | |
| | 92 | | | | | | | | | | |
| | 93 | | | | | | | | | | |
| | 94 | | | | | | | | | | |
| | 95 | | | | | | | | | | |
| | 96 | | | | | | | | | | |
| | 97 | | | | | | | | | | |
| | 98 | | | | | | | | | | |
| | 99 | | | | | | | | | | |
| | 100 | | | | | | | | | | |

| Claim Final | Original | Date | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | 101 | | | | | | | | | | |
| | 102 | | | | | | | | | | |
| | 103 | | | | | | | | | | |
| | 104 | | | | | | | | | | |
| | 105 | | | | | | | | | | |
| | 106 | | | | | | | | | | |
| | 107 | | | | | | | | | | |
| | 108 | | | | | | | | | | |
| | 109 | | | | | | | | | | |
| | 110 | | | | | | | | | | |
| | 111 | | | | | | | | | | |
| | 112 | | | | | | | | | | |
| | 113 | | | | | | | | | | |
| | 114 | | | | | | | | | | |
| | 115 | | | | | | | | | | |
| | 116 | | | | | | | | | | |
| | 117 | | | | | | | | | | |
| | 118 | | | | | | | | | | |
| | 119 | | | | | | | | | | |
| | 120 | | | | | | | | | | |
| | 121 | | | | | | | | | | |
| | 122 | | | | | | | | | | |
| | 123 | | | | | | | | | | |
| | 124 | | | | | | | | | | |
| | 125 | | | | | | | | | | |
| | 126 | | | | | | | | | | |
| | 127 | | | | | | | | | | |
| | 128 | | | | | | | | | | |
| | 129 | | | | | | | | | | |
| | 130 | | | | | | | | | | |
| | 131 | | | | | | | | | | |
| | 132 | | | | | | | | | | |
| | 133 | | | | | | | | | | |
| | 134 | | | | | | | | | | |
| | 135 | | | | | | | | | | |
| | 136 | | | | | | | | | | |
| | 137 | | | | | | | | | | |
| | 138 | | | | | | | | | | |
| | 139 | | | | | | | | | | |
| | 140 | | | | | | | | | | |
| | 141 | | | | | | | | | | |
| | 142 | | | | | | | | | | |
| | 143 | | | | | | | | | | |
| | 144 | | | | | | | | | | |
| | 145 | | | | | | | | | | |
| | 146 | | | | | | | | | | |
| | 147 | | | | | | | | | | |
| | 148 | | | | | | | | | | |
| | 149 | | | | | | | | | | |
| | 150 | | | | | | | | | | |

If more than 150 claims or 10 actions
staple additional sheet here

(LEFT INSIDE)

# SEARCHED

| Class | Sub. | Date | Exmr. |
|---|---|---|---|
| 711 | 104-105 | 9/26/01 | m. w |
|  | 169 |  |  |
|  | 167 |  |  |
| 365 | 233 |  |  |
|  | 238.5 |  |  |
| 710 | 35 | 9/26/01 | M. N |
| Update search | | 4-19-02 | m. p |
| Update search | | 10-18-02 | m. w |
| Update Search | | 6-12-03 | m. w |

## INTERFERENCE SEARCHED

| Class | Sub. | Date | Exmr. |
|---|---|---|---|
| 711 | 104 |  |  |
|  | 105 |  |  |
|  | 169 |  |  |
|  | 167 |  |  |
| 365 | 233 |  |  |
|  | 238.5 |  |  |
| 710 | 35 |  |  |

# SEARCH NOTES
## (INCLUDING SEARCH STRATEGY)

|  | Date | Exmr. |
|---|---|---|
| Glen Cassaye | 9-25-01 | m. w |
| Reginald Bragdon | 9-26-01 | m. w |
| EAST | 9-26-01 | m. N |
| Glen Cassaye | 4-19-02 | m. w |
| EAST | 4-19-02 | m. w |
| Reginald Bragdon | 10-18-02 | m. w |
| Glen Cassaye | 6-13-03 | m. w |
| EAST | 6-13-03 | m. m |

(RIGHT OUTSIDE)

# PATENT APPLICATION

‖‖‖‖‖‖‖‖‖‖‖

09504344

MAR 0 3 0 0 2 7

INITIALS _____

# CONTENTS

| | Date Received (Incl. C. of M.) or Date Mailed | | | Date Received (Incl. C. of M.) or Date Mailed |
|---|---|---|---|---|
| 1. Application 5 nts. papers. | | 42. | | |
| 2. I.D.S. | 5-11-00 | 43. | | |
| 3. Rej 3 mos | 10/2/01 | 44. | | |
| 4. Ext of time (mo) | 2-4-02 5-4-02 | 45. | | |
| 5. Amdt A | 2-14-02 2-4-02 | 46. | | |
| 6. Rej 3mo | 4-25-02 | 47. | | |
| 7. Amdt B | 7-09-02 | 48. | | |
| 8. Final Rej (3months) | 10-22-02 | 49. | | |
| 9. Amdt C | 12/16/02 | 50. | | |
| 10. Advisory Action | 1/10/03 | 51. | | |
| 11. Notice of Appeal | 1-28-03 | 52. | | |
| 12. Appeal Brief | 3-28-03 | 53. | | |
| 13. Notice of Allowability | 6/16/03 | 54. | | |
| 14. Formal Drawings (3 shts/set) | 9/17/03 | 55. | | |
| 15. | | 56. | | |
| 16. | | 57. | | |
| 17. | | 58. | | |
| 18. | | 59. | | |
| 19. | | 60. | | |
| 20. | | 61. | | |
| 21. | | 62. | | |
| 22. | | 63. | | |
| 23. | | 64. | | |
| 24. | | 65. | | |
| 25. | | 66. | | |
| 26. | | 67. | | |
| 27. | | 68. | | |
| 28. | | 69. | | |
| 29. | | 70. | | |
| 30. | | 71. | | |
| 31. | | 72. | | |
| 32. | | 73. | | |
| 33. | | 74. | | |
| 34. | | 75. | | |
| 35. | | 76. | | |
| 36. | | 77. | | |
| 37. | | 78. | | |
| 38. | | 79. | | |
| 39. | | 80. | | |
| 40. | | 81. | | |
| 41. | | 82. | | |

(LEFT OUTSIDE)