



US006132564A

United States Patent [19]

[11] Patent Number: 6,132,564

Licata

[45] Date of Patent: Oct. 17, 2000

[54] IN-SITU PRE-METALLIZATION CLEAN AND METALLIZATION OF SEMICONDUCTOR WAFERS

FOREIGN PATENT DOCUMENTS

0536664 4/1993 European Pat. Off. .
61-190070 8/1986 Japan .
08176823 7/1996 Japan .

[75] Inventor: Thomas J. Licata, Mesa, Ariz.

Primary Examiner—Maria Nuzzolillo
Assistant Examiner—Julian A. Mercado
Attorney, Agent, or Firm—Wood, Herron & Evans, L.L.P.

[73] Assignee: Tokyo Electron Limited, Tokyo, Japan

[57] ABSTRACT

[21] Appl. No.: 08/971,512

A method is provided of cleaning device surfaces for the metallization thereof by treating the surfaces in a chamber equipped for ionized physical vapor deposition or other plasma-based metal deposition process. The surfaces are plasma etched, preferably in a chamber in which the next metal layer is to be deposited onto the surfaces. Also or in the alternative, the surfaces are plasma etched with a plasma containing ions of the metal to be deposited. Preferably also, the etching process is followed by depositing a film of the metal, preferably by ionized physical vapor deposition, in the chamber. The metal may, for example, be titanium that is sputtered from a target within the chamber. The process of depositing the metal, where the metal is titanium, may, for example, be followed by the deposition of a titanium nitride layer. The process steps may be used to passivate the surfaces for transfer of the substrate containing the device surfaces through an oxygen or water vapor containing atmosphere or through another atmosphere containing potential contaminants such as through the transfer chamber of a cluster tool to which are connected CVD or other chemical processing modules. In the preferred embodiment, etching is achieved by maintaining a high ion fraction and high bombardment energy, for example, by applying a high negative bias to the substrate, operating the plasma in a net etching mode, then, by lowering the bombardment energy, for example by lowering the bias voltage, or by lowering the ion fraction, such as by increasing sputtering power, or decreasing plasma power, chamber pressure, a net deposition of the metal by IPVD is brought about.

[22] Filed: Nov. 17, 1997

[51] Int. Cl. 7 C23C 14/34

[52] U.S. Cl. 204/192.15; 204/192.17; 204/192.25; 204/192.3; 204/298.35; 216/37

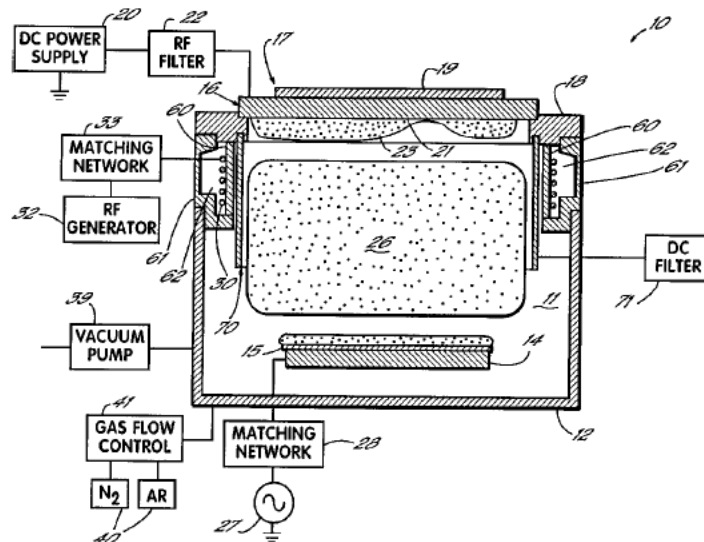
[58] Field of Search 204/192.15, 192.17, 204/192.25, 192.3, 298.25, 192.32, 192.13, 298.35, 298.05; 438/582; 216/37

[56] References Cited

U.S. PATENT DOCUMENTS

Re. 34,106 10/1992 Ohmi .
3,594,295 7/1971 Meckel et al. .
4,250,009 2/1981 Cuomo et al. .
4,464,223 8/1984 Gorin .
4,585,517 4/1986 Stemple 156/643
4,844,775 7/1989 Keeble .
4,863,549 9/1989 Grunwald .
4,925,542 5/1990 Kidd .
4,999,096 3/1991 Nihei et al. .
5,178,739 1/1993 Barnes et al. .
5,401,350 3/1995 Patrick et al. .
5,431,799 7/1995 Mosely et al. .
5,449,432 9/1995 Hanawa .
5,468,296 11/1995 Patrick et al. .
5,540,800 7/1996 Qian .
5,540,824 7/1996 Yin et al. .
5,560,776 10/1996 Sugai et al. .
5,569,363 10/1996 Bayer et al. .
5,747,384 5/1998 Miyamoto .
5,755,888 5/1998 Torii et al. 118/719
5,834,371 11/1998 Ameen et al. .

22 Claims, 2 Drawing Sheets



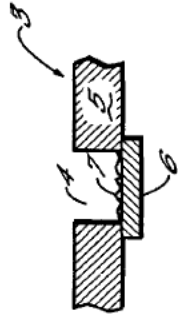


FIG. 1

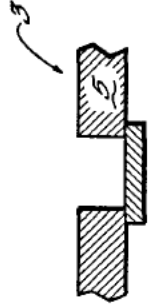


FIG. 1A

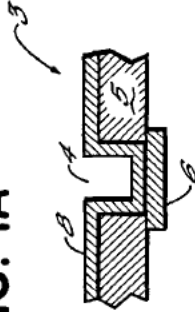


FIG. 1B

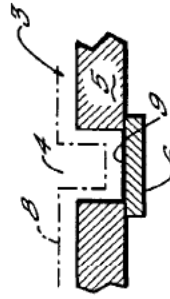
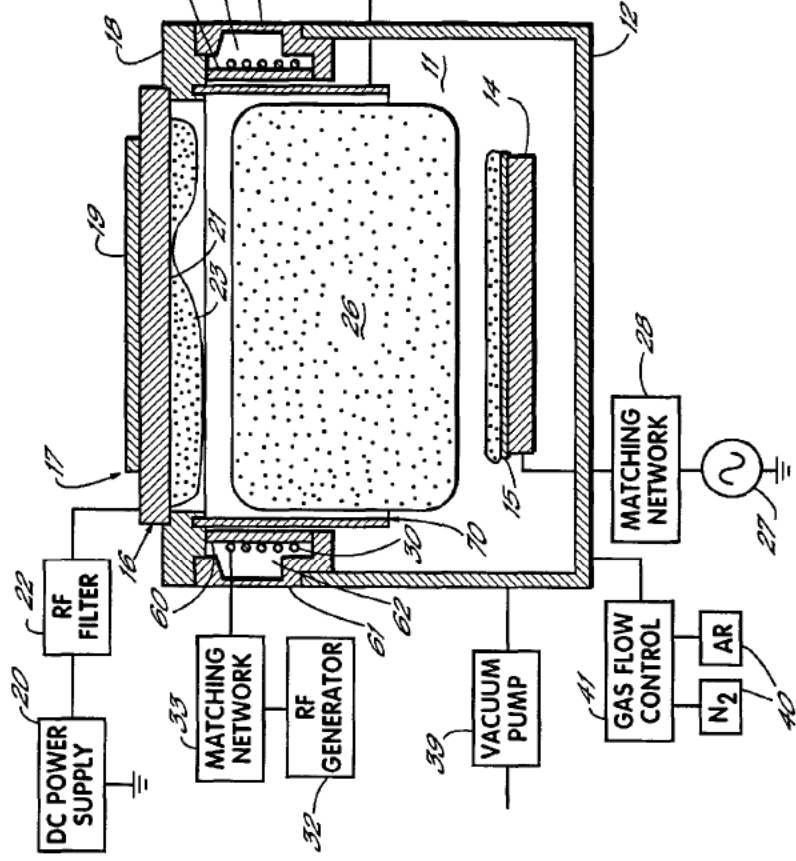
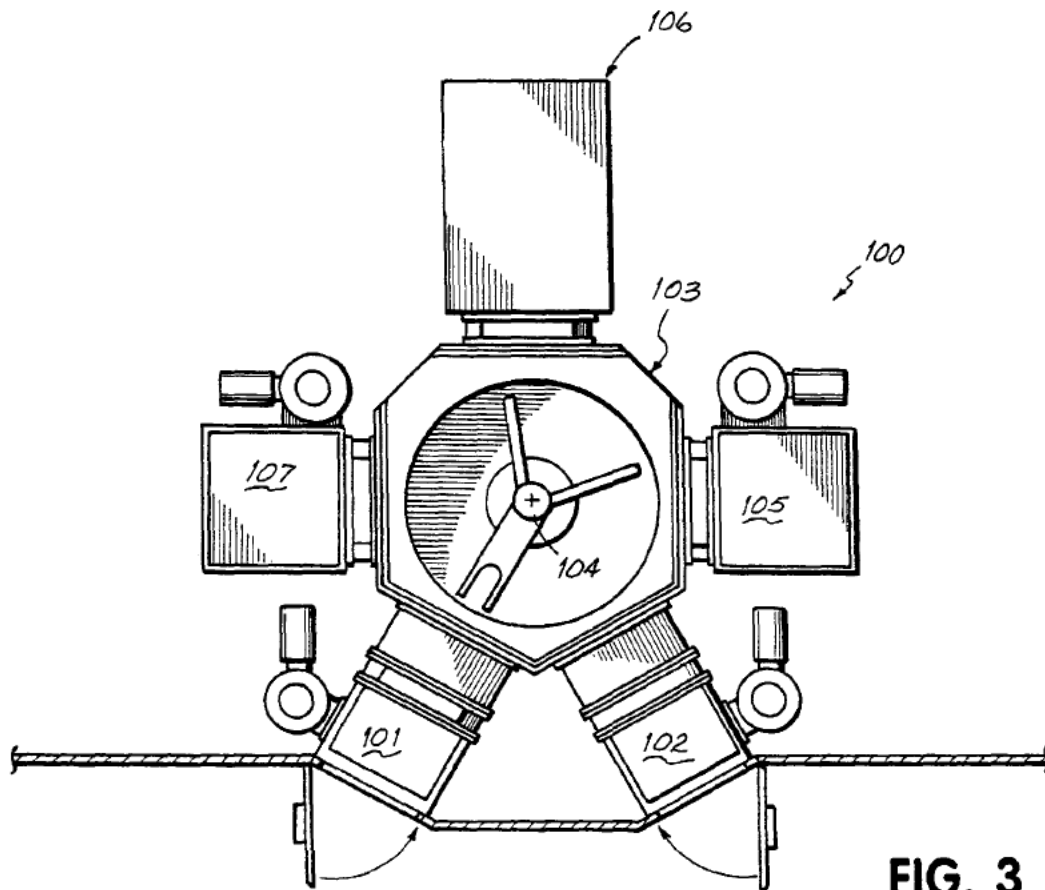


FIG. 1C





IN-SITU PRE-METALLIZATION CLEAN AND METALLIZATION OF SEMICONDUCTOR WAFERS

This invention relates to the cleaning of electrical device surfaces in preparation for the deposition of a metallization layer and to the deposit of the initial film of the metallization layer thereon.

BACKGROUND OF THE INVENTION

The manufacture of semiconductor devices and integrated circuits involves the blanket and selective deposition and removal of many layers of conductive, insulating and semi-conductive materials on substrates that are usually in the form of silicon wafers. The manufacturing processes typically include the formation of a series of metal interconnect film stacks on a wafer by a plurality of sequential processes performed in a series of processing chambers of one or more multi-process vacuum processing tools. Between the formation of the various stacks of the series, wafers are typically removed from a vacuum processing tool and a photo-resist pattern is applied thereto. The application of the pattern is followed by reactive etching processes that are rendered selective by the pattern. By these processes, troughs and/or holes through insulating layers on the underlying stack are formed, exposing contact areas on underlying conductors that are to be connected to the conductors of devices of subsequently applied overlying layers. Before such layers are applied, the masking layer may be removed.

Following selective etching and, in the case of the first metal layer also following an ion implantation process, patterned wafers are reintroduced into a processing tool where a subsequent stack of conductive layers is applied. The lowermost layer of the new stack to be applied is usually a layer of a reactive elemental metal such as titanium, chromium or tantalum, but may also be a metal nitride, silicide or alloy. One function of this lowermost metal layer is to form a bond or contact with an exposed conductive layer, such as silicon or metal, at the bottom of a contact hole in the underlying insulator. The bond serves to form the initial film portion of a conductive path between the underlying layer and the conductor of a new layer of the new stack.

Before the metallization layer is applied, however, it is usually necessary to clean from the wafer native oxides and other contaminants that characteristically formed on the contacts during prior processes or when the wafer was transferred through atmosphere from tool to tool. Even if such wafers were transferred under vacuum, the vacuum is not perfect so contaminating layers of atoms and molecules usually have formed on the surfaces of the contacts in proportion to the exposure duration. Such contaminating layers would, if not removed, interfere with the application of the metallization layer, usually resulting in degraded conductivity between the contact and the metallization layer.

The standard approach to dealing with the problem of contaminants on a contact surface is to subject the wafer to an inductively coupled plasma (ICP) soft sputter etch step immediately before initiating the metallization process. Such a soft etch step is typically carried out by first transferring the wafer, after placement into a vacuum processing tool in which the new stack is to be applied, into a soft etch chamber. In the soft etch chamber, a plasma is formed of an inert gas, usually argon. Then the plasma ions are electrically accelerated toward the wafer, usually by applying a bias to the wafer. The contaminant materials removed from

the contacts by sputtering redistribute through the process chamber or onto the walls of high aspect ratio features, where they do not interfere with the subsequent electrical contact. Such a soft sputter etch is additionally beneficial in that it produces a uniform repeatable surface that facilitates the manufacturable deposition of PVD and CVD films.

The argon soft etch is not an ideal cleaning process since it cleans only by physical removal of contaminants afforded by sputtering. Such sputtering can damage the structure to be cleaned or the underlying device structures, either due to the mechanical sputtering action or through the accumulation of charge. Further, the argon is chemically inert and thus does not react with or chemically reduce the native oxides and other contaminant materials that are to be cleaned from the wafer surface.

Additions of reactive gases to the soft etch plasma have aided in the removal of contaminants from the contacts during soft etch cleaning, but have generally been found undesirable in other ways, particularly since these gases tend to migrate out of the process area and contaminate other portions of the process tool. Further, reactive components such as hydrogen can damage collateral device structures since hydrogen and other commonly used reactive components readily diffuse through the wafer.

In addition, freshly soft etched surfaces can be recontaminated in a processing tool by gases such as water vapor and oxygen from normal outgassing and from gases originating from CVD process modules. Further, the need for separate etch and deposition modules adds to the product cost and to the size of the processing equipment.

Accordingly, there is a need for a more effective and less costly process for preventing oxides and other contaminants from interfering with the metallization of surfaces at which contacts on the lowermost layer of a stack or other interconnects are to be formed, for example, on intra-stack layers that are otherwise prone to oxidation or contamination with water vapor or other material prior to the metallization of the such surfaces.

SUMMARY OF THE INVENTION

A primary objective of the present invention is to provide a method of cleaning the surface of a semiconductor wafer prior to the metallization thereof that overcomes the disadvantages of process sequences of the prior art that employ soft sputter or hard etch processes, or that have avoided etch-based precleaning that would otherwise be beneficial. A more particular objective of the present invention is to provide an improved method of cleaning contacts of semiconductor wafers for metallization. A still further objective of the present invention is to improve the efficiency and reduce the cost of semiconductor wafer processing.

According to principles of the present invention, cleaning of contacts and other surfaces for metallization is carried out in situ, that is, in the same chamber used for metal depositions in the following metallization process, without removing the wafer from the chamber between the cleaning and coating processes and preferably without venting the chamber to atmosphere. The cleaning is carried out by a soft sputter etch with ions of an inert gas such as argon. Preferably, the cleaning is carried out by the use of a plasma that includes ions of the material to be deposited in the metallization process.

According to further principles of the present invention, the cleaning of the contacts or other surfaces for metallization is carried out using a plasma formed in part at least by the same material that is to be used for metallization of the

contacts, preferably with the cleaning and metallization being carried out in the same chamber, which is preferably an ionized physical vapor deposition (IPVD) chamber in which metallization is carried out by IPVD.

According to further principles of the invention, the cleaning of a substrate, particularly contacts or other surfaces thereon that are to be metallized, is carried out and then those surfaces are capped by deposition of a layer of metallization material. For example, the contacts are soft sputter etched with argon ions or argon and titanium ions followed immediately by the deposition of titanium, such as by IPVD, which may also be followed by a deposition of TiN, before the substrate is subjected to exposure to a potentially contaminating environment, such as the atmosphere of a transfer chamber of a CVD module, an external ambient atmosphere or such other atmosphere from which contamination could result.

Preferably, the surface of the substrate is first bombarded with ionized metal at an energy level that results in a net etching of the surface of the substrate, particularly the contacts or other surfaces to be metallized. Then, a film of the same metal is preferably deposited by an ionized physical vapor deposition (IPVD) process, following reduction of the energy level of the ions so that there is a net buildup of the material on the surface.

In accordance with one preferred embodiment of the invention, the surface to be cleaned for metallization is bombarded with titanium ions in an IPVD chamber. Preferably, the titanium is produced by the sputtering of a titanium target with an argon plasma, and the titanium particles that are ejected from the target surface are then ionized by passing the sputtered titanium particles through a dense inductively coupled plasma (ICP) or electron cyclotron resonance (ECR) plasma, for example. While these methods of generating the material ionizing plasma are preferred, helicon, hollow cathode and a number of other methods of generating a plasma may also be employed. The ionized titanium atoms and other ionized sputtered titanium particles are then accelerated toward the substrate by electrically biasing the substrate to a negative potential.

In the preferred method of the invention, the particles are initially directed toward the substrate with a relatively high ion fraction and relatively high bombardment energy so that a net etching effect is achieved on the substrate surface. This etching removes native oxides, water and other contaminants that may have accumulated on the substrate prior to or during transport into the IPVD chamber. Preferably following etching with titanium ions, the energy of the titanium ions is reduced, such as by reducing the biasing voltage, so that a net deposition of a titanium film is produced on the surface of the substrate. Alternately, the Ti ion fraction can be reduced by other means including decreasing the ICP power or Ar pressure or by increasing the metal sputter cathode power. In effect, an ionized PVD of the titanium is used to carry out a combination of a precleaning of the wafer and the deposition of the first metal film.

In accordance with the preferred embodiment of the invention, the high energy titanium metal atoms simultaneously sputter clean and react with the surface contaminants. The process takes advantage of the fact that the titanium, unlike neutral argon, reacts with and chemically reduces the oxides and as a film has a high solubility for the oxygen. Further, the titanium atoms, which have a higher atomic mass than atoms of argon, are particularly effective for cleaning contacts at the bottoms of high aspect ratio holes since they are scattered less by gas phase collisions

and therefor remain more closely aligned normal to the surface of the wafer.

Alternatively, certain advantages of the invention can be realized by controlling the bias voltage on the wafer or using other techniques to direct the ions of the metal to the wafer in such a way that the cleaning with the metal and coating with the metal overlap or occur simultaneously. For example, by reducing or eliminating the change in biasing voltage and rather using a voltage that balances the cleaning and coating rates appropriate to the asperity of the feature to be cleaned, effective cleaning and coating with titanium or titanium nitride can be achieved. However, sequentially cleaning and then coating in the manner described above effectively produces the advantages of the invention for most applications and is preferred for simplicity.

Preferably, the invention is carried out according to an IPVD method and apparatus as disclosed in one or more of copending U.S. patent application Ser. Nos. 08/837,551, 08/844,756 and 08/844,757 filed Apr. 21, 1997 and U.S. patent application Ser. No. 08/861,958 filed May 22, 1997, all hereby expressly incorporated by reference herein. The IPVD chamber may use a metal, such as titanium, titanium nitride, tantalum or another metal or compound compatible with the substrate and intended overlying materials, for both cleaning of the substrate and for the initial coating of the substrate. The IPVD chamber is preferably provided as one processing module of a cluster tool and arranged to connect to the transfer module of the tool, to which is also connected a processing module, such as a CVD module, for the application of a metallization layer such as tungsten, aluminum or copper.

A titanium nitride film, once deposited, is resistant to reaction with oxygen or water vapor, and is generally more stable than the contacts which have been only soft etch cleaned with an argon plasma. In addition, a titanium film has a large capacity to buffer disadvantageous effects on exposure to such substances. As a result, wafers can be transferred from the tool through the transfer module of a CVD apparatus with less likelihood of undergoing further contamination. The transfer modules of CVD reactors often contain levels of contaminants from the CVD processing chambers to which they are attached. Contaminants often found in such transfer chambers include, for example, TiCl₄, NH₃, NF₃, H₂, and MOCVD precursors such as tetrakis di-methyl amino titanium (TDMAT). IPVD diffusion barriers such as TiN can, for example, resist contamination by such substances when the wafers are being transferred through the transfer chamber of the CVD tool.

With the combined Ti-ion cleaning and initial Ti film deposition followed by TiN deposition performed in the same chamber, the invention is therefore useful for intra-stack as well as inter-stack applications. For example, transfer of a Ti-ion cleaned and coated wafer, according to the present invention, can be effectively transferred through the transfer chamber of a cluster tool and into a CVD module for the deposition of tungsten with less likelihood of undergoing contamination in the transfer chamber than would an argon soft etch cleaned wafer.

Similarly, IPVD cleaned and deposited metal nitrides or other metals such as a tantalum can be similarly used with the present invention. For example, a Ta-ion cleaning and IPVD Ta and TaN deposition can be performed on a wafer in an IPVD module of a processing tool prior to the transfer of the wafer through the tool transfer chamber to a CVD module of the tool for the deposition of copper.

With the present invention, not only is a superior cleaning and contamination preventing process provided, but both the

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts



Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research



With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips



Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.