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PATENT
Customer Number 22,852
Attorney Docket No. 9140.0016-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Prior Application Art Unit: 2823 Prior Application Examiner: ESTRADA, Michelle

SIR: This is a request for filing a

☐ Continuation ☐ Continuation-in-Part ☒ Divisional Application under 37 C.F.R. § 1.53(b) of pending prior Application No. 10/101,863 filed March 16, 2002, of Hongmei ZHANG, Mukundan NARASINHAN, Ravi B. MULLAPUDI, and Richard E. DEMARAY for BIASED PULSE DC REACTIVE SPUTTERING OF OXIDE FILMS.

1. ☒ Enclosed is a complete copy of the prior application including the oath or Declaration and drawings, if any, as originally filed. I hereby verify that the attached papers are a true copy of prior Application No. 10/101,863 as originally filed on March 16, 2002, which is incorporated herein by reference.

2. ☒ A Preliminary Amendment is enclosed.

3. ☒ The filing fee is calculated on the basis of the claims existing in the prior application as amended in the Preliminary Amendment filed herewith.

Basic Utility Application Filing Fee					$300	$ 300.00
Search Fee					$500	500.00
Examination Fee					$200	200.00
	Number of Claims		Basic	Extra		
Total Claims	7	-	20	0	x $ 50	0
Independent Claims	2	-	3	0	x $200	0
☐ Presentation of Multiple Dep. Claim(s)					+ $360	0
Total Application Pages (specification, drawings, and printed sequence or computer listing)	66	If over 100 pages, add $250 for each additional 50 pages or fraction thereof.				0
Subtotal						$ 1,000.00
Reduction by 1/2 if small entity						- 0
TOTAL APPLICATION FILING FEE						$ 1,000.00

4. ☒ The Commissioner is hereby authorized to charge the fee of $1,000.00 to Deposit Account No. 06-0916.

5. ☒ The Commissioner is hereby authorized to charge any fees which may be required including fees due under 37 C.F.R. § 1.16 and any other fees due under 37 C.F.R. § 1.17, or credit any overpayment during the pendency of this application to Deposit Account No. 06-0916.

6. ☒ The prior application is assigned of record to: Symmorphix, Inc.

7. ☒ The power of attorney in the prior application is to FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P., Customer No. 22,852

8. ☒ Since the power does not appear in the original declaration, a copy of the power in the prior application is enclosed.

9. ☒ Please address all correspondence to FINNEGAN, HENDERSON, FARABOW, GARRETT and DUNNER, L.L.P., **Customer Number 22,852**.

10. ☒ Also enclosed are an Information Disclosure Statement, Form PTO/SB/08, and one cited reference.

PETITION FOR EXTENSION. If any extension of time is necessary for the filing of this application, including any extension in parent Application No. 10/101,863, filed March 16, 2002, for the purpose of maintaining copendency between the parent application and this application, and such extension has not otherwise been requested, such an extension is hereby requested, and the Commissioner is authorized to charge necessary fees for such an extension to our Deposit Account No. 06-0916. A duplicate copy of this paper is enclosed for use in charging the deposit account.

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: September 16, 2005

By:____________________
Gary J. Edwards
Reg. No. 41,008

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER L.L.P.
901 New York Avenue, N.W.
Washington, D.C. 20001-4413
(650) 849-6622

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GARRETT & DUNNER L.L.P.
901 New York Avenue, N.W.
Washington, D.C. 20001-4413
(650) 849-6622

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Biased Pulse DC Reactive Sputtering of Oxide Films

Hongmei Zhang
Mukundan Narasimhan
Ravi Mullapudi
Richard E. Demaray

Background

1. Field of the Invention

[0001] The present invention relates to deposition of oxide and oxynitride films and, in particular, to deposition of oxide and oxynitride films by pulsed DC reactive sputtering.

2. Discussion of Related Art

[0002] Deposition of insulating materials and especially optical materials is technologically important in several areas including production of optical devices and production of semiconductor devices. In semiconductor devices, doped alumina silicates can be utilized as high dielectric insulators.

[0003] The increasing prevalence of fiber optic communications systems has created an unprecedented demand for devices for processing optical signals. Planar devices such as optical waveguides, couplers, splitters, and amplifiers, fabricated on planar substrates, like those commonly used for integrated circuits, and configured to receive and process signals from optical fibers are highly desirable. Such devices hold promise for integrated optical and electronic signal processing on a single semiconductor-like substance.

[0004] The basic design of planar optical waveguides and amplifiers is well known, as described, for example, in U. S. Patent Nos. 5,119,460 and 5,563,979 to Bruce et al., 5,613,995 to Bhandarkar et al., 5,900,057 to Buchal et al., and 5,107,538 to Benton et al., to cite only a few. These devices, very generally, include a core region, typically bar shaped, of a certain refractive index surrounded by a cladding region of a lower refractive index. In the case of an optical amplifier, the core region includes a certain concentration of a dopant, typically a rare earth ion such as an erbium or praseodymium ion which, when pumped by a laser, fluoresces, for example, in the 1550 nm and 1300 nm wavelength ranges used for optical communication, to amplify the optical signal passing through the core.

[0005] As described, for example in the patents by Bruce et al., Bhandarkar et al, and Buchal et al., planar optical devices may be fabricated by process sequences including forming a layer of cladding material on a substrate; forming a layer of core material on the layer of cladding mater; patterning the core layer using a photolighotgraphic mask and an etching process to form a core ridge; and covering the core ridge with an upper cladding layer.

[0006] The performance of these planar optical devices depends sensitively on the value and uniformity of the refractive index of the core region and of the cladding region, and particularly on the difference in refractive index, Δn, between the regions. Particularly for passive devices such as waveguides, couplers, and splitters, Δn should be carefully controlled, for example to values within about 1 %, and the refractive index of both core and cladding need to be highly uniform, for some applications at the fewer than parts per thousand level. In the case of doped materials forming the core region of planar optical amplifiers, it is important that the dopant be uniformly distributed so as to avoid non-radiative quenching or radiative quenching, for example by upconversion. The refractive index and other desirable properties of the core and cladding regions, such as physical and chemical uniformity, low stress, and high density, depend, of course, on the choice of materials for the devices and on the processes by which they are fabricated.

[0007] Because of their optical properties, silica and refractory oxides such as Al_2O_3, are good candidate materials for planar optical devices. Further, these oxides serve as suitable hosts for rare earth dopants used in optical amplifiers. A common material choice is so-called low temperature glasses, doped with alkali metals, boron, or phosphorous, which have the advantage of requiring lower processing temperatures. In addition, dopants are used to modify the refractive index. Methods such as flame hydrolysis, ion exchange for introducing alkali ions in glasses, sputtering, and various chemical vapor deposition processes (CVD) have been used to form films of doped glasses. However, dopants such as phosphorous and boron are hygroscopic, and alkalis are undesirable for integration with electronic devices. Control of uniformity of doping in CVD processes can be difficult and CVD deposited films can have structural defects leading to scattering losses when used to guide light. In addition, doped low temperature glasses may require further processing after deposition. A method for eliminating bubbles in thin films of sodium-boro-silicate glass by high temperature sintering is described, for example, in the '995 patent to Bhandarkar et al.

[0008] Typically, RF sputtering has been utilized for deposition of oxide dielectric films. However, RF sputtering utilizes ceramic targets which are typically formed of multiple smaller tiles. Since the tiles can not be made very large, there may be a large problem of arcing between tiles and therefore contamination of the deposited film due to this arcing. Further, the reactors required for RF sputtering tend to be rather complicated. In particular, the engineering of low capacitance efficient RF power distribution to the cathode is difficult in RF systems. Routing of low capacitance forward and return power into a vacuum vessel of the reaction chamber often exposes the power path in such a way that diffuse plasma discharge is allowed under some conditions of impedance tuning of the matching networks.

[0009] Therefore, there is a need for new methods of depositing oxide and oxynitride films and for forming planar optical devices.

Summary

[0010] In accordance with the present invention, a sputtering reactor apparatus for depositing oxide and oxynitride films is presented. Further, methods for depositing oxide and oxynitride films for optical waveguide devices are also presented. A sputtering reactor according to the present invention includes a pulsed DC power supply coupled through a filter to a target and a substrate electrode coupled to an RF power supply. A substrate mounted on the substrate electrode is therefore supplied with a bias from the RF power supply.

[0011] The target can be a metallic target made of a material to be deposited on the substrate. In some embodiments, the metallic target is formed from Al, Si and various rare-earth ions. A target with an erbium concentration, for example, can be utilized to deposit a film that can be formed into a waveguide optical amplifier.

[0012] A substrate can be any material and, in some embodiments, is a silicon wafer. In some embodiments, RF power can be supplied to the wafer. In some embodiments, the wafer and the electrode can be separated by an insulating glass.

[0013] In some embodiments, up to about 10 kW of pulsed DC power at a frequency of between about 40 kHz and 350 kHz and a reverse pulse time of up to about 5 μs is supplied to the target. The wafer can be biased with up to about several hundred watts of RF power. The temperature of the substrate can be controlled to within about 10° C and can vary from about -50° C to several hundred degrees C. Process gasses can be fed into the reaction chamber of the reactor apparatus. In some embodiments, the process gasses can include combinations of Ar, N_2, O_2, C_2F_6, CO_2, CO and other process gasses.

[0014] Several material properties of the deposited layer can be modified by adjusting the composition of the target, the composition and flow rate of the process gasses, the power supplied to the target and the substrate, and the temperature of the substrate. For example, the index of refraction of the deposited layer depends on deposition parameters. Further, in some embodiments stress can be relieved on the substrate by depositing a thin film of material on a back side of the wafer. Films deposited according to the present invention can be utilized to form optical waveguide devices such as multiplexers and rare-earth doped amplifiers.

[0015] These and other embodiments, along with examples of material layers deposited according to the present invention, are further described below with respect to the following figures.

Brief Description of the Figures

[0016] Figures 1A and 1B show a pulsed DC sputtering reactor according to the present invention.

[0017] Figure 2 shows a planar view of target utilized in a reactor as shown in Figures 1A and 1B.

[0018] Figure 3 shows a cross-section view of an example target utilized in a reactor as shown in Figures 1A and 1B.

[0019] Figure 4 shows a flow chart of an embodiment of a process for depositing a film on a substrate according to the present invention.

[0020] Figure 5 shows a hysterises curve of target voltage versus oxygen flow rates for an example target in an embodiment of a reactor according to the present invention.

[0021] Figure 6 shows a photo-luminescence and lifetimes of a film deposited in a process according to the present invention as a function of after deposition anneal temperature.

[0022] Figure 7 shows the relationship between the index of refraction of a film as a function of deposited oxide layers according to the present invention and due to oxide build-up on the target.

[0023] Figure 8 shows a graph of the index of refraction of a film deposited according to the present invention as a function of the aluminum content in a composite Al/Si target.

[0024] Figure 9 shows a graph of typical indices of refraction of material layers deposited according to the present invention.

[0025] Figure 10 shows a table of indices of refraction for a silica layer deposited according to the present invention as a function of different process parameters.

[0026] Figure 11 shows the refractive indices as a function of O_2/Ar ratio utilized in an Alumina process according to the present invention.

[0027] Figure 12 shows the refractive indices as a function of DC pulsed power frequency for an Alumina layer deposited according to the present invention.

[0028] Figure 13 shows variation in the refractive index over time during repeated depositions from a single target.

[0029] Figure 14 shows variation in refractive index over time for repeated depositions from a target of another material layer according to the present invention.

[0030] Figure 15 shows the variation refractive index over time for repeated depositions from a target of another material layer according to the present invention.

[0031] Figure 16A through 16D shows a TEM film deposited according to the present invention.

[0032] Figure 17 shows the transparency of a film deposited according to the present invention.

[0033] Figure 18 shows an uppercladding layer deposited according to the present invention over a multiple-waveguide structure such that the deposited layer is substantially planarized.

[0034] Figure 19 illustrates the deposition of a film over a waveguide structure.

[0035] Figures 20 and 21 illustrate different etch and deposition rates for deposition of films as a function of the surface angle of the film.

[0036] Figure 22 illustrates calculation of the planarization time for a particular deposition process.

[0037] Figures 23 through 25 through illustrate adjustment of process parameters in order to achieve planarization of a film deposited over a waveguide structure according to the present invention.

[0038] Figure 26 shows the gain characteristics of an erbium doped waveguide amplifier formed of films depositions according to the present invention.

[0039] Figures 27 shows gain, insertion loss of a waveguide with an active core deposited according to the present invention.

[0040] Figure 28 shows up-conversion constants, and lifetimes of the active core layer of Figure 27 deposited according to the present invention.

[0041] Figure 29 shows drift in the index of refraction with subsequent depositions for films deposited from a target according to the present invention.

[0042] Figure 30 shows drift in the photoluminescence with subsequent depositions according to the present invention.

[0043] Figure 31 shows drift in the excited state lifetime with subsequent depositions according to the present invention.

[0044] Figure 32 shows stabilization of the index of refraction in subsequent depositions.

[0045] Figure 33 shows the index of refraction of a film formed from a pure silicon target as a function of the ratio of O_2/N_2 in the process gas.

[0046] In the figures, elements having the same designation have the same or similar function.

Detailed Description

[0047] Reactive DC magnetron sputtering of nitrides and carbides is a widely practiced technique, but the reactive dc magnetron sputtering of nonconducting oxides is done rarely. Films such as aluminum oxide are almost impossible to deposit by conventional reactive DC magnetron sputtering due to rapid formation of insulating oxide layers on the target surface. The insulating surfaces charges up and result in arcing during process. This arcing can damage the power supply, produce particles and degrade the properties of deposited oxide films.

[0048] RF sputtering of oxide films is discussed in Application Serial No. 09/903,050 (the '050 application) by Demaray et.al., entitled "Planar Optical Devices and Methods for Their Manufacture," assigned to the same assignee as is the present invention, herein incorporated by reference in its entirety. Further, targets that can be utilized in a reactor according to the present invention are discussed in U.S. Application serial no. {Attorney Docket No. M-12247 US} (the '247 application), filed concurrently with the present disclosure, assigned to the same assignee as is the present invention, herein incorporated by reference in its entirety. A gain-flattened amplifier formed of films deposited according to the present invention are described in U.S. Application serial no. {Attorney Docket No. M-12652 US} (the '652 application), filed concurrently with the present disclosure, assigned to the same assignee as is the present invention, herein incorporated by reference in its entirety. Further, a mode size converter formed with films deposited according to the present invention is described in U.S. Application serial no. {Attorney Docket No. M-12138 US} (the '138 application), filed concurrently with the present disclosure, assigned to the same assignee as is the present invention, herein incorporated by reference in its entirety.

[0049] Figure 1A shows a schematic of a reactor apparatus 10 for sputtering of material from a target 12 according to the present invention. In some embodiments, apparatus 10 may, for example, be adapted from an AKT-1600 PVD (400 X 500 mm substrate size) system from Applied Komatsu or an AKT-4300 (600 X 720 mm substrate size) system from Applied Komatsu, Santa Clara, CA. The AKT-1600 reactor, for example, has three deposition chambers connected by a vacuum transport chamber. These Komatsu reactors can be modified such that pulsed DC power is supplied to the target and RF power is supplied to the substrate during deposition of a material film.

[0050] Apparatus 10 includes a target 12 which is electrically coupled through a filter 15 to a pulsed DC power supply 14. In some embodiments, target 12 is a wide area sputter source target, which provides material to be deposited on substrate 16. Substrate 16 is positioned parallel to and opposite target 12. Target 12 functions as a cathode when power is applied to it and is equivalently termed a cathode. Application of power to target 12 creates a plasma 53. Substrate 16 is capacitively coupled to an electrode 17 through an insulator 54. Electrode 17 can be coupled to an RF power supply 18. Magnet 20 is scanned across the top of target 12.

[0051] For pulsed reactive dc magnetron sputtering, as performed by apparatus 10, the polarity of the power supplied to target 12 by power supply 14 oscillates between negative and positive potentials. During the positive period, the insulating layer on the surface of target 12 is discharged and arcing is prevented. To obtain arc free deposition, the pulsing frequency exceeds a critical frequency that depend on target material, cathode current and reverse time. High quality oxide films can be made using reactive pulse DC magnetron sputtering in apparatus 10.

[0052] Pulsed DC power supply 14 can be any pulsed DC power supply, for example an AE Pinnacle plus 10K by Advanced Energy, Inc. With this example supply, up to 10 kW of pulsed DC power can be supplied at a frequency of between 0 and 350 KHz. The reverse voltage is 10% of the negative target voltage. Utilization of other power supplies will lead to different power characteristics, frequency characteristics and reverse voltage percentages. The reverse time on this embodiment of power supply 14 can be adjusted between 0 and 5 μs.

[0053] Filter 15 prevents the bias power from power supply 18 from coupling into pulsed DC power supply 14. In some embodiments, power supply 18 is a 2 MHz RF power supply, for example can be a Nova-25 power supply made by ENI, Colorado Springs, Co.

[0054] Therefore, filter 15 is a 2 MHz band rejection filter. In some embodiments, the band width of the filter can be approximately 100 kHz. Filter 15, therefore, prevents the 2 MHz power from the bias to substrate 16 from damaging power supply 18.

[0055] However, both RF and pulsed DC deposited films are not fully dense and most likely have columnar structures. These columnar structures are detrimental for optical wave guide applications due to the scattering loss caused by the structure. By applying a RF bias on wafer 16 during deposition, the deposited film can be dandified by energetic ion bombardment and the columnar structure can be substantially eliminated.

[0056] In the AKT-1600 based system, for example, target 12 can have an active size of about 675.70 X 582.48 by 4 mm in order to deposit films on substrate 16 that have dimension about 400 X 500 mm. The temperature of substrate 16 can be held at between –50C and 500C. The distance between target 12 and substrate 16 can be between about 3 and about 9 cm. Process gas can be inserted into the chamber of apparatus 10 at a rate up to about 200 sccm while the pressure in the chamber of apparatus 10 can be held at between about .7 and 6 millitorr. Magnet 20 provides a magnetic field of strength between about 400 and about 600 Gauss directed in the plane of target 12 and is moved across target 12 at a rate of less than about 20-30 sec/scan. In some embodiments utilizing the AKT 1600 reactor, magnet 20 can be a race-track shaped magnet with dimension about 150 mm by 600 mm.

[0057] A top down view of magnet 20 and wide area target 12 is shown in Figure 2. A film deposited on a substrate positioned on carrier sheet 17 directly opposed to region 52 of target 12 has good thickness uniformity. Region 52 is the region shown in Figure 1B that is exposed to a uniform plasma condition. In some implementations, carrier 17 can be coextensive with region 52. Region 24 shown in Figure 2 indicates the area below which both physically and chemically uniform deposition can be achieved, where physical and chemical uniformity provide refractive index uniformity, for example. Figure 2 indicates that region 52 of target 12 that provides thickness uniformity is, in general, larger than region 24 of target 12 providing thickness and chemical uniformity. In optimized processes, however, regions 52 and 24 may be coextensive.

[0058] In some embodiments, magnet 20 extends beyond area 52 in one direction, the Y direction in Figure 2, so that scanning is necessary in only one direction, the X direction, to provide a time averaged uniform magnetic field. As shown in Figures 1A and 1B, magnet 20 can be scanned over the entire extent of target 12, which is larger than region 52 of uniform sputter erosion. Magnet 20 is moved in a plane parallel to the plane of target 12.

[0059] The combination of a uniform target 12 with a target area 52 larger than the area of substrate 16 can provide films of highly uniform thickness. Further, the material properties of the film deposited can be highly uniform. The conditions of sputtering at the target surface, such as the uniformity of erosion, the average temperature of the plasma at the target surface and the equilibration of the target surface with the gas phase ambient of the process are uniform over a region which is greater than or equal to the region to be coated with a uniform film thickness. In addition, the region of uniform film thickness is greater than or equal to the region of the film which is to have highly uniform optical properties such as index of refraction, density, transmission or absorptivity.

[0060] Target 12 can be formed of any materials, but is typically metallic materials such as, for example, combinations of Al and Si. Therefore, in some embodiments, target 12 includes a metallic target material formed from intermetalic compounds of optical elements such as Si, Al, Er and Yb. Additionally, target 12 can be formed, for example, from materials such as La, Yt, Ag, Au, and Eu. To form optically active films on substrate 16, target 12 can include rare-earth ions. In some embodiments of target 12 with rare earth ions, the rare earth ions can be pre-alloyed with the metallic host components to form intermetalics. *See* the '247 application.

[0061] In several embodiments of the invention, material tiles are formed. These tiles can be mounted on a backing plate to form a target for apparatus 10. Figure 3A shows an embodiment of target 12 formed with individual tiles 30 mounted on a cooled backplate 25. In order to form a wide area target of an alloy target material, the consolidated material of individual tiles 30 should first be uniform to the grain size of the powder from which it is formed. It also should be formed into a structural material capable of forming and finishing to a tile shape having a surface roughness on the order of the powder size from which it is consolidated. A wide area sputter cathode target can be formed from a close packed array of smaller tiles. Target 12, therefore, may include any number of tiles 30, for example between 2 to 20 individual tiles 30. Tiles 30 are finished to a size so as to provide a margin of non-contact, tile to tile, 29 in Figure 3A, less than about 0.010" to about 0.020" or less than half a millimeter so as to eliminate plasma processes between adjacent ones of tiles 30. The distance between tiles 30 of target 12 and the dark space anode or ground shield 19, in Figure 1B can be somewhat larger so as to provide non contact assembly or provide for thermal expansion tolerance during process chamber conditioning or operation.

[0062] Several useful examples of target 12 that can be utilized in apparatus 10 according to the present invention include the following targets compositions: (Si/Al/Er/Yb) being about (57.0/41.4/0.8/0.8), (48.9/49/1.6/0.5), (92/8/0/0), (60/40/0/0), (50/50/0/0), (65/35/0/0), (70/30/0,0), and (50,48.5/1.5/0) cat. %, to list only a few. These targets can be referred to as the 0.8/0.8 target, the 1.6/.5 target, the 92-8 target, the 60-40 target, the 50-50 target, the 65-35 target, the 70-30 target, and the 1.5/0 target, respectively. The 0.8/0.8, 1.6/0.5, and 1.5/0 targets can be made by pre-alloyed targets formed from an atomization and hot-isostatic pressing (HIPing) process as described in the '247 application. The remaining targets can be formed, for example, by HIPing. Targets formed from Si, Al, Er and Yb can have any composition. In some embodiments, the rare earth content can be up to 10 cat. % of the total ion content in the target. Rare earth ions are added to form active layers for amplification. Targets utilized in apparatus 10 can have any composition and can include ions other than Si, Al, Er and Yb, including: Zn, Ga, Ge, P, As, Sn, Sb, Pb, Ag, Au, and rare earths: Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy Ho, Er, Tm Yb and Lu.

[0063] Optically useful materials to be deposited onto substrate 16 include oxides, fluorides, sulfides, nitrides, phosphates, sulfates, and carbonates, as well as other wide band gap semiconductor materials. To achieve uniform deposition, target 12, itself can be chemically uniform and of uniform thickness over an extended area.

[0064] Target 12 can be a composite target fabricated from individual tiles, precisely bonded together on a backing plate with minimal separation, as is discussed further with respect to Figure 3. In some embodiments, the mixed intermetalllics can be plasma sprayed directly onto a backing plate to form target 12. The complete target assembly can also includes structures for cooling the target, embodiments of which have been described in U. S. Patent No. 5,565,071 to Demaray et al, and incorporated herein by reference.

[0065] Substrate 16 can be a solid, smooth surface. Typically, substrate 16 can be a silicon wafer or a silicon wafer coated with a layer of silicon oxide formed by a chemical vapor deposition process or by a thermal oxidation process. Alternatively, substrate 16 can be a glass, such as Corning 1737 (Corning Inc., Elmira, NY), a glass-like material, quartz, a metal, a metal oxide, or a plastic material. Substrate 16 can be supported on a holder or carrier sheet that may be larger than substrate 16. Substrate 16 can be electrically biased by power supply 18.

[0066] In some embodiments, the area of wide area target 12 can be greater than the area on the carrier sheet on which physically and chemically uniform deposition is accomplished. Secondly, in some embodiments a central region on target 12, overlying substrate 16, can be provided with a very uniform condition of sputter erosion of the target material. Uniform target erosion is a consequence of a uniform plasma condition. In the following discussion, all mention of uniform condition of target erosion is taken to be equivalent to uniform plasma condition. Uniform target erosion is evidenced by the persistence of film uniformity throughout an extended target life. A uniformly deposited film can be defined as a film having a nonuniformity in thickness, when measured at representative points on the entire surface of a substrate wafer, of less than about 5 % or 10%. Thickness nonuniformity is defined, by convention, as the difference between the minimum and maximum thickness divided by twice the average thickness. If films deposited from a target from which more than about 20 % of the weight of the target has been removed continue to exhibit thickness uniformity, then the sputtering process is judged to be in a condition of uniform target erosion for all films deposited during the target life.

[0067] As shown in Figure 1B, a uniform plasma condition can be created in the region between target 12 and substrate 16 in a region overlying substrate 16. A plasma 53 can be created in region 51, which extends under the entire target 12. A central region 52 of target 12, can experience a condition of uniform sputter erosion. As discussed further below, a layer deposited on a substrate placed anywhere below central region 52 can then be uniform in thickness and other properties (i.e., dielectric, optical index, or material concentrations).

[0068] In addition, region 52 in which deposition provides uniformity of deposited film can be larger than the area in which the deposition provides a film with uniform physical or optical properties such as chemical composition or index of refraction. In some embodiments, target 12 is substantially planar in order to provide uniformity in the film deposited on substrate 16. In practice, planarity of target 12 can mean that all portions of the target surface in region 52 are within a few millimeters of a planar surface, and can be typically within 0.5 mm of a planar surface.

[0069] Other approaches to providing a uniform condition of sputter erosion rely on creating a large uniform magnetic field or a scanning magnetic field that produces a time-averaged, uniform magnetic field. For example, rotating magnets or electromagnets can be utilized to provide wide areas of substantially uniform target erosion. For magnetically enhanced sputter deposition, a scanning magnet magnetron source can be used to provide a uniform, wide area condition of target erosion.

[0070] As illustrated in FIG. 1A, apparatus 10 can include a scanning magnet magnetron source 20 positioned above target 12. An embodiment of a scanning magnetron source used for dc sputtering of metallic films is described in U. S. Patent No. 5,855,744 to Halsey, et. al., (hereafter '744), which is incorporated herein by reference in its entirety. The '744 patent demonstrates the improvement in thickness uniformity that is achieved by reducing local target erosion due to magnetic effects in the sputtering of a wide area rectangular target. As described in the '744 patent, by reducing the magnetic field intensity at these positions, the local target erosion was decreased and the resulting film thickness nonuniformity was improved from 8%, to 4%, over a rectangular substrate of 400 x 500 mm.

[0071] The process gas utilized in reactor 10 includes an inert gas, typically argon, used as the background sputtering gas. Additionally, with some embodiments of target 12, reactive components such as, for example, oxygen may be added to the sputtering gas. Other gasses such as N_2, NH_3, CO, NO, CO_2, halide containing gasses other gas-phase reactants can also be utilized. The deposition chamber can be operated at low pressure, often between about .5 millitorr and 8-10 millitorr. Typical process pressure is below about 3-5millitorr where there are very few collisions in the gas phase, resulting in a condition of uniform "free molecular" flow. This ensures that the gas phase concentration of a gaseous component is uniform throughout the process chamber. For example, background gas flow rates in the range of up to about 200 sccm, used with a pump operated at a fixed pumping speed of about 50 liters/second, result in free molecular flow conditions.

[0072] The distance d, in Figure 1A, between target 12 and substrate 16 can, in some embodiments, be varied between about 4 cm and about 9 cm. A typical target to substrate distance d is about 6 cm. The target to substrate distance can be chosen to optimize the thickness uniformity of the film. At large source to substrate distances the film thickness distribution is dome shaped with the thickest region of the film at the center of the substrate. At close source to substrate distance the film thickness is dish shaped with the thickest film formed at the edge of the substrate. The substrate temperature can be held constant in the range of about -40 °C to about 550°C and can be maintained at a chosen temperature to within about 10 °C by means of preheating substrate 16 and the substrate holder prior to deposition. During the course of deposition, the heat energy impressed upon the substrate by the process can be conducted away from substrate 16 by cooling the table on which substrate 16 is positioned during the process, as known to those skilled in the art. The process is performed under conditions of uniform gas introduction, uniform pumping speed, and uniform application of power to the periphery of the target as known to skilled practitioners.

[0073] The speed at which a scanning magnet 20 can be swept over the entire target can be determined such that a layer thickness less than about 5 to 10 Å, corresponding roughly to two to four monolayers of material, is deposited on each scan. Magnet 20 can be moved at rates up to about 30 sec/one-way scan and typically is moved at a rate of about 4 sec/one-way scan. The rate at which material is deposited depends on the applied power and on the distance d, in Figure 1A, between the target 12 and the substrate 16. For deposition of optical oxide materials, for example scanning speeds between about 2 sec/one-way scan across the target to 20-30 sec/scan provide a beneficial layer thickness. Limiting the amount of material deposited in each pass promotes chemical and physical uniformity of the deposited layer.

[0074] Substrate bias has been used previously to planarize RF sputtered deposited quartz films. A theoretical model of the mechanism by which substrate bias operates, has been put forward by Ting et al. (J. Vac. Sci. Technol. 15, 1105 (1978)). When power is applied to the substrate, a so-called plasma sheath is formed about the substrate and ions are coupled from the plasma. The sheath serves to accelerate ions from the plasma so that they bombard the film as it is deposited, sputtering the film, and forward scattering surface atoms, densifying the film and eliminating columnar structure. The effects of adding substrate bias are akin to, but more dramatic than, the effects of adding the low frequency RF component to the sputter source.

[0075] Biasing substrate 16 results in the deposited film being simultaneously deposited and etched. The net accumulation of film at any point on a surface depends on the relative rates of deposition and etching, which depend respectively, on the power applied to the target and to the substrate, and to the angle that the surface makes with the horizontal. The rate of etching is greatest for intermediate angles, on the order of 45 degrees, that is between about 30 and 60 degrees.

[0076] Powers to target 12 and substrate 16 can be adjusted such that the rates of deposition and etching are approximately the same for a range of intermediate angles. In this case, films deposited with bias sputtering have the following characteristics. At a step where a horizontal surface meets a vertical surface, the deposited film makes an intermediate angle with the horizontal. On a surface at an intermediate angle, there will be no net deposition since the deposition rate and etch rate are approximately equal. There is net deposition on a vertical surface.

[0077] Target 12 can have an active size of about 675.70 X 582.48 by 4 mm, for example, in a AKT-1600 based system in order to deposit films on a substrate 16 that is about 400 X 500 mm. The temperature of substrate 16 can be held at between –50C and 500C. The distance between target 12 and substrate 16 can be between 3 and 9 cm. Process gas can be inserted into the chamber of apparatus 10 at a rate of between about 30 to about 100 sccm while the pressure in the chamber of apparatus 10 can be held at below about 2 millitorr. Magnet 20 provides a magnetic field of strength between about 400 and about 600 Gauss directed in the plane of target 12 and is moved across target 12 at a rate of less than about 20-30 sec/scan.

[0078] Therefore, any given process utilizing apparatus 10 can be characterized by providing the power supplied to target 12, the power supplied to substrate 16, the temperature of substrate 16, the characteristics and constituents of the reactive gasses, the speed of the magnet, and the spacing between substrate 16 and target 12.

[0079] Sputtered oxide films according to some embodiments of the present invention can be deposited onto a Si wafer or thermal oxide wafers at pressure of between about 3 and about 6 mTorr. The ratio of O_2/Ar gas flow can be set at a value to ensure that target 12 is operating within a poison mode. The poison mode is defined as the ratio where the oxide is etched from the surface of target 12 as fast as the oxide layer is formed. Operating in the poison mode results in the stoichiometric film. Sub-stoichiometric oxides may not be optically transparent. The pulsing frequency range for power supply 14 can be from about up to about 250 KHz. The frequency 40 KHz is approximately the lowest frequency at which no arcing will occur during deposition in, for example, the AKT 1600 based system. The reverse pulsing time is determined by the amount of arcing generated during the process. Longer reverse time means longer discharge time and thus less arcs. However, if the reverse time is too long, the deposition rate will decrease. Power supply 18 is a 2 MHz RF power supply operated at powers up to several hundred Watts.

[0080] Figure 4 shows an embodiment of a process procedure 400 performed on apparatus 10. In step 401, the target is prepared for the deposition. In some embodiments, target 12 can be cleaned by pure Ar sputtering. In other words, apparatus 10 is operated with pure Ar gas only (referred to as the metal mode) in order to sputter away a surface layer of target 12.

[0081] Figure 7 shows the typical drift in the index of refraction with deposition of oxide layers for several different targets over different runs for each target. In Figure 7, the compositions of the target materials utilized in target 12 for the depositions shown are as follows: Si: 60 cat. % and Al: 40 cat. %; Si: 50 cat. % and Al: 50 cat. %; Si: 85 cat. % and Al: 15 cat. %; Si: 35 cat. % and Al: 65 cat. %; and Si: 92 cat. % and 8 cat. %. Each deposition was operated under the same process parameters: 4.5 kW of pulsed DC power at 200 kHz with a reverse time of 2.3 µs applied to target 12, O_2 flow at 44 sccm, Ar flow at 30 sccm introduced to apparatus 10, 100 W of bias power at 2 MHz applied to substrate 16, the temperature of substrate 16 held at 200° C, and the distance between substrate 16 and target 12 being set at 6 cm. For each target measured, the index drifted up during repeated utilization.

[0082] Figure 8 shows the relationship between the index of refraction of a film deposited according to the present invention and the amount of aluminum in the composite target. As can be seen from Figure 8, the index of refraction of the deposited film depends strongly on the aluminum content. Therefore, as the aluminum in a metal target is depleted, the index of refraction drifts. In some embodiments, the ratio of Ar and O_2 utilized in the process can be maintained to provide films of uniform index over a large number of depositions on the target.

[0083] Reactive sputtering from a metal or metallic alloy target 12 can be characterized by two modes of operation. In the first mode, which is sometimes referred to as the 'metallic mode' the surface of target 12 is substantially metallic. This mode is characterized by a small addition of reactive gas to the inert gas flow of apparatus 10 as well as a higher impedance magnetron discharge. It is also characterized by incomplete oxidation of film deposited on substrate 16 and therefore higher index films. As the proportion of reactive to inert gas is increased, the sputter voltage at target 12 begins to fall at constant power.

[0084] Figure 5 shows the voltage on target 12 of an embodiment of apparatus 10 according to the present invention as a function of process gas constitution. In the example illustrated in Figure 5, for example, a metallic target with composition .8 cat. % Er, .8 cat. % Yb, 57.4 cat. % Si and 41 cat. % Si, which can be formed as described in the '247 application, was sputtered in an embodiment of apparatus 10 based on the AKT-1600 PVD system with 6 kW of pulsed DC power at a frequency of 120 kHz and a reverse time of 2.3 micro seconds. The Argon gas flow was set at 60 sccm and the Oxygen gas flow was varied from zero up to 40 sccm. For more details regarding this deposition, see Example 1 below.

[0085] As shown in Figure 5, the voltage on target 12 during deposition (the "target voltage") was constant at about 420 Volts for oxygen flow rates up to about 20 sccm. This is clearly the metallic mode of operation for this embodiment of target 12. Films deposited in this range of oxygen flow are characterized as metallic with an oxygen content that increases with oxygen flow rate during deposition. As the oxygen flow is increased up to about 26 sccm, the voltage on target 12 begins to decrease, indicating that the surface of target 12 is beginning to form an oxide layer. The oxide layer on the surface of target 12 has a higher secondary electron yield under the influence of the Argon ion flux. The additional electron flux to the magnetron electron trap increases the ion production in the plasma, which, in turn, decreases the impedance of the plasma discharge in apparatus 10.

[0086] At slightly higher oxygen flow during deposition, the oxide layer on target 12 forms a continuous layer and the voltage of target 12 during deposition falls rapidly to the range of about 190 to about 270 Volts, indicating complete coverage of the surface of target 12 with an oxide that is at least as thick as the material removed during one scan of the magnetron. Under this condition, the rate of oxide formation on the surface of target 12 equals or exceeds the rate of sputter removal of the surface of target 12 by the moving magnetron 20. This condition is sometimes referred to as the 'poisoned mode'.

[0087] Under steady state DC voltage conditions, the oxide layer on target 12 soon charges up, leading to reduced rate of sputtering and increased micro-arc discharging in apparatus 10. This discharging leads to particulation of the oxide layer on target 12, which degrades the quality of a film deposited on substrate 16. In the example shown with Figure 5, the negative going DC Voltage is reduced at a frequency of 120 kHz to a positive value for a period of about 2.3 micro seconds per cycle, allowing charge neutralization of the surface of target 12, increasing the steady state sputter and deposition rates as well as decreasing the rate of micro-arcing.

[0088] In the case of a magnetron configuration of magnet 20 having a significant deep local target erosion (rather than a configuration of magnet 20 described above which yields uniform target erosion), the change in the target voltage of target 12 is more gradual with increasing oxygen flow since it is more difficult to establish an oxide condition at the center of an intense region of local erosion. The resulting deposited film, however, will be rich in metallic sputtered flux to the substrate in the region of higher sputter erosion, leading to non uniform stoicheometry and non-uniform indices of refraction in a film deposited on substrate 16. In the case of a scanning magnetron 20 with uniform target erosion, the change in the surface condition from metallic to poisoned is more abrupt, as the formation rate of the oxide increases to equal the sputter removal of the oxide over a wide area of the target. In this case, there is uniform distribution of sputtered oxide from the target. Uniform stoicheometry and uniform indices of refraction result for the film deposited on substrate 16.

[0089] Figure 8 shows the range of indices of refraction of films deposited for targets of differing silica and alumina compositions, as deposited and after a subsequent anneal step. In the case of a pure silicon target, the as-deposited index of refraction can be as high as 3.4 for pure amorphous silicon. In Figure 8, pure silica films (zero Al%) can be deposited with a reactive pulsed DC and substrate bias deposition according to the present invention with substantially complete oxygen stoicheometry, so as to approximate monolithic amorphous silica. The index of refraction of such films decreases with a subsequent heat treatment of between about 700-900° C, indicating somewhat more complete oxidation reaction of the material of the film together with some degree of stress relaxation of the film deposited on substrate 16.

[0090] At the opposite extreme, a pure aluminum embodiment of target 12 (100% Al) can be utilized to deposit films on substrate 16 under similar process conditions as is utilized to deposit pure silica films on substrate 16. In the case of the pure aluminum reactive deposition, the dependence of the index of refraction of the film deposited on substrate 16 on oxygen flow as well as on the frequency of the pulsed DC process can be examined. As a result, a larger range of effective index of refraction is achieved together with a reduced or zero dependence of the index on the subsequent anneal process. Six targets having differing aluminum composition were utilized to evaluate the index of refraction of sputtered films on substrate 16 of related composition. The largest change of index with the sputtering conditions is achieved for composition near the middle of the Al/Si composition range (about 50% Al and 50% Si).

[0091] Figure 7 shows the change in film index for oxide films for several embodiments of target 12 and processes with an initial 30 minutes of Argon only sputtering, followed by continuous deposition with an oxygen flow rate sufficient for operation in the poisonous mode. Note that the rate of increase in the index of refraction of a resulting film deposited on substrate 16 with continuous poisoned mode deposition is proportional to the concentration of aluminum in the composition of target 12. This result is due to the depletion of the aluminum from the target surface during the metallic sputtering or pre-condition process. The aluminum in target 12 is preferentially sputtered over the silicon in target 12, leaving the surface of target 12 rich in silicon. At the onset of poisoned mode sputtering, the film deposited on substrate 16 is rich in silica and demonstrates a systematic and reproducible decrease in index of refraction. During continuous poisoned mode deposition, the silicon rich surface of target 12 can be sputtered away and the aluminum portion substantially returned to the bulk composition of target 12. Consequently, a metallic pre-condition step can be utilized to achieve a subsequent process for the deposition of a film having an increasing index of refraction under conditions of oxide/metal stoicheometry.

[0092] In step 402 of Figure 4, substrate 16 is prepared. Substrate 16 can be mounted on carrier sheet 17 and placed in apparatus 10. In step 403, gas flow parameters are adjusted for the particular deposition to be performed. The constituency and flow rates of the process gas are fixed. In some embodiments, the ratio of Ar and O_2, for example, can be set and the flow rate of each gas set. Further, the combination of flow rate and vacuum system of apparatus 10 determines the pressure during deposition in apparatus 10.

[0093] In step 404, the substrate temperature is set. Substrate 16 may be brought to temperature over a period of time. In step 405, the scan characteristics of magnet 20 are fixed. In step 406, the power setting for power supply 18 is set. Finally, in step 407, the parameters of pulsed DC power supply 14 is set, including the power, frequency, and reverse pulsing time. In step 408, then, a film that depends on the parameters of reactor apparatus 10 is deposited on substrate 16. In some embodiments, films deposited by procedure 400 are thermally annealed after deposition.

[0094] Figure 4 illustrates an example deposition process only. Embodiments of deposition processes according to the present invention can be performed in various different orders.

[0095] Figure 9 shows a chart of various deposition parameters according to the present invention for various embodiments of target 12 and the indices of refraction, both before and after an anneal step, for the resulting deposited film on substrate 16. Each deposition was accomplished with an embodiment of apparatus 10 based on the AKT 1600 PVD reactor. Anneals were accomplished at 725° C for 30 min. Specific examples of particular depositions and characteristics of the resulting films deposited on substrate 16 are further discussed below.

[0096] Figure 10 shows the dependence of the index of refraction of silica layers deposited according to the present invention with process conditions. Figure 11 shows the dependence of index of refraction on the O2/Ar flow ratio for the deposition of pure alumina according to the present invention. Figure 12 shows the dependence of index for pure alumina films on the frequency of the pulsed DC power applied to target 12. Both parameters can be utilized to reliably control the index of refraction of films deposited on substrate 16 over a range of index values without the use of an additional cationic species, a so called 'dopant'. A third process parameter that can be utilized to adjust the index of refraction of a film deposited on substrate 16 is the bias power applied to substrate 16. Increasing the oxygen flow ratio, the frequency of the pulsed DC power applied to target 12 or the bias power applied to substrate 16 will systematically increase the index of refraction of the alumina film deposited on substrate 16. In the case of pure alumina films, minor to no change in the index occurs due to a subsequent anneal process.

[0097] Figure 13 shows the index of refraction of a film deposited on substrate 16 from an embodiment of target 12 with about 92 cat. % of Si and about 8 cat. % of Al for a series of sequential depositions in an embodiment of apparatus 10 based on the AKT 4300 PVD reactor, each following a metallic process condition. For constant high oxygen flow conditions, a small upward trend in the index of refraction is observed. As is generally true, the index of films deposited with higher substrate bias power is systematically lower than films deposited without substrate bias.

[0098] Figure 14 shows the upward trend of the index of refraction after metallic mode precondition of an embodiment of target 12 having composition of about 83 cat. % Si and about 17 cat. % Al for a series of depositions in an embodiment of apparatus 10 based on the AKT 1600 PVD reaction. As is shown in Figure 14, longer metallic preconditioning of target 12 results in the index of refraction of the films deposited on substrate 16 having a higher rate of increase than for cases with less prolonged metallic preconditioning of target 12. The vertical lines on Figure 14 indicate places where target 12 was preconditioned with only Ar for the indicated periods of time. Figure 15 shows a decrease in the change in index for sequential films with this embodiment of target 12 deposited with reduced oxygen flow rates at a constant total pressure. A flow rate for oxygen was determined so that the run to run variation for the index of refraction of the film deposited on substrate 16 from this target was about .0001 (see the circled data points on the graph of Figure 15) which is similar to the variance of the index over the entire wafer of substrate 16, which is about 70 parts per million.

[0099] In some embodiments, films deposited by a pulsed DC biased method according to the present invention are uniformly amorphous throughout their thickness. As has been discussed above, biasing of substrate 16 leads to densification and uniformity in the deposited film. Figures 16A through 16D show a TEM photograph of a film 1601 deposited according to the present invention. Further, diffraction patterns shown in Figures 16B, 16C and 16D at points a, b and c, respectively, in deposited film 1601 show that the film is ammorphous through the thickness of the film. The diffraction patterns of Figures 16B, 16C and 16D show no effects of crystallization. Further, the smoothness of the surface of film 1601 indicates a defect free film. The film deposited in Figure 16A is deposited with an 0.8/0.8 target (i.e., a target having the composition 52.0 cat. % of Si, 41.0 cat. % of Al, 0.8 cat. % of Er and 0.8 cat. % of Yb). The film is deposited at 6 kW of 120 kHz pulsed DC power with a reverse time of 2.3 μs. The Argon and Oxygen flow rates are 60 sccm and 28 sccm, respectively. Substrate 16 is biased with 100 W of power.

[0100] Figure 17 shows the optical loss per centimeter, measured at 1310 nm, using a three prism coupling to the so called slab mode of the film on a 10 micron oxide, silicon wafer. As deposited the biased, pulsed DC film from a 60 cat. % Si and 40 cat. %Al film demonstrated about .1dB/cm loss. After an 800° C anneal in air, the loss was less than the measurement sensitivity of the prism coupling method. This data clearly demonstrates that films deposited according to embodiments of the present invention can be used for the purpose of constructing low loss planar light wave circuits.

[0101] Deposition of films according to the present invention can be utilized to deposit cladding layers, active core layers, and passive core layers of an optical amplifier structure or optical waveguide structure. In some applications, for example multiplexer structures, the separation between adjacent waveguides can be small, for example about 8 μm. In some embodiments, the deposition parameters of the upper cladding layer can be adjusted to not only adjust the index of refraction of the layer, but also to insure that the spacing between adjacent waveguides is small.

[0102] Figure 18 shows an example planarization deposition over a multiplexer structure. In the particular example of upper cladding layer 1803 shown in Figure 18, the deposition parameters from a 92 cat. % Si and 8 cat. % Al is: 5.5 Kw of Pulsed DC power applied at 200 KHz with 2.2 μs of reverse time, gas flow of 75 sccm Ar and 100 sccm O_2, a substrate bias of 650 W (at 2 MHz), and a substrate temperature of 200 °C. Layer 1803 was deposited with an AKT 4300 based embodiment of apparatus 10. As shown in Figure 18, the layer thickness in areas other than over waveguide structures 1801 and 1802 is 11.4 μm. Waveguide structures 1801 and 1802 are 8.20 μm high waveguides and separated by 6.09 μm at the base and by 8.40 μm at their top. In Figure 18, the undercladding layer 1804 is about 1.98 μm thick.

[0103] Figure 19 illustrates deposition of material over a structure. Upper cladding layer 1803, in region 1901, will be angled from the horizontal by an angle θ. The deposition and etching rates of a deposited layer depends on the angle θ. Figures 20 and 21 illustrate different cases of deposition and etch rates as a function of the angle θ. The relationship between the rate of deposition and the etch rates can be adjusted by adjusting the deposition parameters. For example, the bias power to substrate 16 can be adjusted to control the relationship between the etch rates and deposition rates of material.

[0104] Figure 22 illustrates deposition rates over a structure 2201 as a function of time. In Figure 2201, h is the thickness deposited over structure 2201. The planarization when layer 1803 becomes flat.

[0105] The time for planarization can be estimated as

$$t_p = \frac{\frac{W}{2}\tan\alpha + H}{a_{flat} - \frac{a_{\min}}{\cos\alpha}},$$

where W is the width of structure 2201, H is the height of structure 2201, a_{flat} refers to the accumulation rate on the flat surface, a_{min} refers to the accumulation rate on the minimum accumulation slope, and α is the surface angle from the horizontal plane of the minimum accumulation slope.

[0106] Figure 23 shows a deposited film 1803 as shown in Figure 18, except that the bias power to substrate 16 is set to 400 W instead of 650 W. As can be seen in Figure 23, a keyhole 2301 is formed with an incomplete filling of uppercladding layer 1803 between structures 1801 and 1802. Deposition of uppercladding layer 1803 substantially follows the trends illustrated in Figures 19 through 22.

[0107] Figure 24 shows deposition as shown in Figure 18, except that the bias power to substrate 16 is set to 600 W instead of 650 W. As can be seen in Figure 24, keyhole 2301 has closed leaving a small line defect 2401 in the fill.

[0108] Figure 28 shows deposition as shown in Figure 18, except that the bias power to substrate 16 is set to 900 W instead of 650 W. As can be seen in Figure 28, the etch rate has been increased to such an extent that the corners of structures 1801 and 1802 have been etched to form slopes 2501 and 2502, respectively.

[0109] Therefore, as illustrated in figures 18 through 25, an uppercladding layer can be deposited in accordance with the present invention such that it fills the space between adjacently placed waveguides. In general, the parameters can be optimized for index control and the bias power to substrate 16 can be adjusted for fill. In some embodiments, other parameters (e.g., the constituency of process gas, frequency and power of pulsed DC power source 14, and other parameters) in order to adjust the deposition and etch rates and thereby effectively planarize the structure as described.

[0110] Therefore, depositions of various films in embodiments of apparatus 10 according to the present invention with several embodiments of target 12 and the effects on index of refraction, uniformity of films, and fill characteristics of varying several of the process parameters has been discussed above. In some embodiments, stress effects due to wafer bowing of substrate 16 can also be reduced. Wafer bowing of substrate 16 can be reduced, reducing the stress in a film deposited on substrate 16, by, for example, depositing a film on the backside of substrate 16 before deposition of a film on substrate 16. In some embodiments, a film having a similar thickness of a similar layer of material can be deposited on backside of substrate 16 prior to deposition of the film on substrate 16 according to the present invention. The wafer bowing resulting from differing thermal expansions of the film and substrate 16 is therefore countered by a similar stress from another film deposited on the backside of substrate 16.

[0111] Several specific examples film depositions utilizing apparatus 10 are discussed below. Further, examples of optical amplifiers produced utilizing the ceramic tiles according to the present invention are presented. These examples are provided for illustrative purposes only and are not intended to be limiting. Unless otherwise specified, apparatus 10 utilized in the following examples was based on the AKT 1600 reactor. Further, unless otherwise specified, the temperature of substrate 16 was held at about 200° C and the distance between substrate 16 and target 12 was 4 s/scan. The separation between substrate 16 and target 12 is about 6 cm.

EXAMPLE 1

[0112] An AKT 1600 based reactor can be utilized to deposit a film. In this example, a wide area metallic target of dimension 550X 650 mm with composition (Si/Al/Er/Yb) being about 57.0 cat. % Si, 41.4 cat. % Al, 0.8 cat. % Er, and 0.8 cat. % Yb (a ".8/.8" target) was fabricated as described in the '247 patent.

[0113] In step 402, a 150 mm P-type silicon wafer substrate was placed in the center of a 400x500 mm glass carrier sheet 17. Power supply 14 was set to supply 6000 watts of pulse DC power at a frequency of 120KHz with a reverse pulsing time of about 2.3us. Magnet 20, which is a race-track shaped magnet of approximate dimension 150mmx600mm, was swept over the backside of the target at a rate of about 4 seconds per one-way scan. The temperature of substrate 16 was held at 200C and 100W of 2 MHz RF power was applied to substrate 16. The target 12 to substrate 16 distance was about 6.5 cm. The sputtering gas was a mixture of Argon and Oxygen. Substrate 16 and carrier 17 was preheated to 350° C for at least 30min prior to deposition. The active film was deposited in the poison mode. Deposition efficiency was approximately 1um/hr.

[0114] Figure 5 shows the hysteresis curve of this particular embodiment of target 12. When target 12 under goes the transition from metallic to poison mode, the target voltage drops from an average of about 420V to an average of about 260V. Before each film deposition, in step 401, target 12 is cleaned by pure Argon sputtering in the metallic mode. Then target is then conditioned in poison mode with the oxygen flow much higher than the flow required at the transition region.

[0115] Tables 1A through 1C shows some effects on the deposited films of depositions with the 0.8/0.8 target under different operating conditions. Table 1A includes photoluminescence (pumped at 532 nm) and index of refraction for films deposited on substrate 16 with different Ar/O_2 gas flow ratios with no bias power applied to substrate 16.

Table 1A

Target Power (KW)	Ar/O2	Frequency (KHz)	Reverse Pulsing Time (us)	Bias (W)	PL/um (532nm)	Index
6	30/42	200	2.3	0	1973	1.5142
6	30/36	200	2.3	0	2358	1.5215
6	60/30	200	2.3	0	3157	1.5229
6	60/28	200	2.3	0	3421	1.5229

[0116] Table 1B shows the variation in photoluminescence (pumped at 532 nm) and index of refraction of the film deposited on substrate 16 with deposition processes having with the same Ar/O_2 ratios but different pulsed DC power frequencies from power supply 14.

Table 1B

Target Power (KW)	Ar/O2	Frequency (KHz)	Reverse Pulsing Time (us)	Bias (W)	PL/um (532nm)	Index
3	60/28	100	2.3	100	1472	1.5146
4	60/28	75	3.5	100	2340	1.5189
6	60/28	120	2.3	100	5178	1.5220

[0117] Table 1C shows the photoluinescence and index as deposited where the bias power to substrate 16 is varied.

Table 1C

Target Power (KW)	Ar/O2	Frequency (KHz)	Reverse Pulsing Time (us)	Bias (W)	PL/um (532nm)	Index
6	60/28	200	2.3	0	3657	1.5230
6	60/28	200	2.3	100	2187	1.5244
6	60/28	200	2.3	200	3952	1.5229
6	60/28	200	2.3	300	5000	1.5280

[0118] The photoluminescence values can be measured with a Phillips PL-100. The deposited film can be pumped with a 532 nm laser and the luminescence at 980 is measured. The index is the index of refraction. Typically, films deposited are annealed in order to activate the erbium. Figure 6 shows the photoluminescence and lifetime versus anneal temperature for a typical film deposited as described in this example.

EXAMPLE 2

[0119] A waveguide amplifier can be deposited according to the present invention. An embodiment of target 12 having composition 57.4 cat. % Si, 41.0 cat. % Al, 0.8 cat. % Er 0.8 cat. % Yb (the ".8/.8 target") can be formed as disclosed in the '245 application. The Er-Yb (0.8/0.8) co-doped Alumino-Silicate film was deposited onto a 6 inch wafer of substrate 16 which includes a 10 μm thick thermal oxide substrate, which can be purchased from companies such as Silicon Quest International, Santa Clara, CA. Target 12 was first cleaned by sputtering with Ar (80 sccm) only in the metallic mode. Target 12 was then conditioned in poison mode by flowing 60 sccm of Argon and 40 sccm of oxygen respectively. The power supplied to target 12 during conditioning was kept at about 6 kW.

[0120] An active core film was then deposited on substrate 16. The thickness of the deposited film is approximately 1.2 μm. The deposition parameters are shown in Table 2.

Table 2.

. Target Power (KW)	Ar/O2 (sccm)	Pulsing Frequency (KHz)	Bias (W)	Reverse pulsing time (us)
6	60/28	120	100	2.3

[0121] A straight waveguide pattern can then formed by standard photolithography techniques. The active core was etched using reactive ion etch followed by striping and cleaning. Next, a 10 μm top cladding layer is deposited using a similar deposition process according to the present invention. An embodiment of target 12 with composition 92 cat. % Si and 8 cat. % Al as shown in Figure 9 to form the top cladding layer. The index difference between the top cladding layer and the active layer is about 3.7%. The amplifier is then annealed at 725° C for about 30 min (see Figure 6, for example).

[0122] The erbium excited-state lifetime and the up-conversion coefficient were measured to be 3ms and 4.5×10^{-18} cm^3/s, respectively. A net gain of about 4dB for small signal (about -20 dBm) with fiber to waveguide and to fiber coupling was obtained. Waveguide length was 10cm and the width was about 1.5 to 8 μm. The coupling loss between the fiber and the waveguide is 3-4 dB/facet, and passive excess loss is 0.1-0.2 dB/cm for 3um waveguide. The waveguide was both co- and counter pumped with 150 mW 980nm laser per facet.

EXAMPLE 3

[0123] This example describes production of a dual core Erbium/Yttrbium co-doped amplifier according to the present invention. In one example, substrate 16 is a silicon substrate with an undercladding layer of thermally oxidized SiO_2 of about 15 μm thick. Substrate 16 with the thermal oxide layer can be purchased from companies such as Silicon Quest International, Santa Clara, CA. A layer of active core material is then deposited on substrate 16 with a Shadow Mask as described in the '138 application. Use of a shadow mask results in a vertical taper on each side of a finished waveguide which greatly enhances the coupling of light into and out of the waveguide.

[0124] Active core layer is deposited from a 0.8/0.8 target as described in the '247 application having composition 57.4 cat. % Si, 41.0 cat. % Al, 0.8 cat. % Er, and 0.8 cat. % Yb. The deposition parameters are identical to that of Example 2 described above. The active layer is deposited to a thickness of about 1.2 μm.

[0125] A passive layer of aluminasilicate is then deposited over the active layer. A passive layer of about 4.25 μm thickness can be deposited with an embodiment of target 12 having composition of Si/Al of about 87 cat. % Si and about 13 cat. % Al. The passive layer and active layer are then patterned by standard lithography techniques to form a core that has a width of about 5.0 μm for the active core and tapering to about 3.5 μm at the top of the passive core with an effective length of about 9.3 cm.

[0126] Upper cladding layer is then deposited from a Si/Al target of 92 cat. % Si and 8 cat. % Al. Deposition of the upper cladding layer is shown in Figure 9. In some embodiments, the upper cladding layer can be deposited with a non-biased process. The thickness of the upper cladding layer can be about 10 μm. The amplifier formed by this process is then annealed at 725° C for about 30 min.

[0127] The as-deposited Erbium and Ytterbium concentrations in the active layer of core 303 is 2.3×10^{20} cm^{-3} Erbium concentration and 2.3×10^{20} cm^{-3} Ytterbium concentration. The index of the core is 1.508 and the index of cladding layers are 1.4458 for undercladding layer 302 and 1.452 for uppercladding layer 304. The parameter $\Delta n/n$ is therefore about 5.0%.

[0128] A reverse taper mode size converter, *see* the '138 application, is utilized for coupling light into waveguide amplifier 300. The insertion loss at 1310 nm is about 2 dB. Figure 26 shows the amplifier performance of this example. In Figure 26, amplifier 300 is pumped with 150 mW from one side pumping with 984 nm light. Gain flattening is achieved within about 1 dB in the range 1528 nm to 1562 nm for small input signals (-20 dBm). For large input signals (0 dBm), gain flattening is also achieved within about 1 dB.

EXAMPLE 4

[0129] Another example of production of a waveguide amplifier is described here. Again, substrate 16 can be a Si wafer with about a 15 μm thick thermal oxide as can be purchased from Silicon Quest International, Santa Clara, CA. The embodiment of target 12 for the deposition of the active core can have a composition of about 50 cat. % Si, 48.5 cat. % Al, 1.5 cat. % Er (the "1.5/0" target), which can be fabricated as discussed in the '138 application. Target 12 was first cleaned by sputtering with Ar (80 sccm) only in the metallic mode. Target 12 was then conditioned in poison mode by flowing 60 sccm of Argon and 40 sccm of oxygen respectively.

[0130] The pulsed DC power supplied to target 12 was about 6 kW. Whenever a brand new target was used or when the target has been expose to atmosphere, a long time of condition (for example more than 30hrs of conditioning) may be necessary to ensure films with the best active core property (longest life time and highest photoluminescence) are deposited. Substrate 16 is then preheat at about 350° C for about 30min before deposition.

[0131] The active core film was deposited onto a 6 inch thermal oxide wafer, which has been previously discussed, from the 1.5/0 target. The thermal oxide thickness was about 10 μm as described in previous examples. The active core is deposited to a thickness of about 1.2 μm with a deposition time of approximately 1 hr. The process condition are as listed in Table 4 below.

Table 3

Target Power (KW)	Ar/O2 (sccm)	Pulsing Frequency (KHz)	Bias (W)	Reverse pulsing time (us)
6	60/28	120	100	2.3

[0132] A straight waveguide pattern can then be formed by a standard photolithography procedure. The active core was etched using reactive ion etch followed by striping and cleaning. Finally, a 10 μm top cladding layer is deposited using a similar process. A target having composition 92 cat. % Si and 8 cat. % Al with deposition parameters as described in Figure 9 was used to deposit the top cladding. The difference between the index of refraction between the core and the cladding is then about 3.7%.

[0133] In this example, annealing of the amplifier structure was performed at various anneal temperatures. The results of the various anneals are shown graphically in Figures 27 and 28. Figure 27 shows both internal gain in the C-band and insertion loss at 1310 nm of a 2.5μm wide, 10.1 cm long waveguide as deposited in this example as a function of annealing temperature. The life time in ms and up-conversion constants in cm^{-3}/s measurements for the deposited active core film at different annealing temperature are shown in Figure 28.

EXAMPLE 5

[0134] One of the problems encountered during the reactive sputtering from an alloy metallic target is that the film composition drifts from run to run due to the difference in sputtering yields from the elements that forms the target alloy. For example, with Ar as a sputtering gas, the sputtering yield of Aluminum is about 3-4 times that of Silicon, while sputtering yield of Alumina is only about 50% that of Silica. Therefore, during the metal burn in, more Aluminum is sputtered from the target, resulting in a Si rich target surface. When sputtering in the poison mode, more Silica will be removed from target. Thus, as deposition goes on, the composition of the film deposited on substrate 16 will drift from lower Alumina concentration to higher Alumina concentration. This results in the index of refraction of a film drifting up with subsequent depositions from a target 12, as is shown for the deposition described in Example 4 in Figure 29. Figure 30 shows the drift in photoluminescence pumped at 532 nm with subsequent depositions. Figure 31 shows drift in the excited state lifetime with subsequent depositions from a target. The embodiment of target 12 utilized in Figures 29 through 31 is the 1.5/0 target and the deposition parameters are as described above in Example 4.

[0135] The drift can be stabilized by recondition target 12 prior to deposition. The recondition process (or burn in) consists of both sputtering in metallic mode and then sputtering in poison mode to condition target 12. The burn in time in metallic mode needs to be as short as possible and at the same time insure no arcing during the poison mode deposition. Figure 32 shows the much improved drift in the index of refraction and the photoluminescence when target 12 is reconditioned between subsequent depositions.

EXAMPLE 6

[0136] This example describes the fabrication of another Er-Yb codoped waveguide amplifier according to the present invention. The active core is deposited with an embodiment of target 12 with composition about **49 cat. % Si, 48 cat. % Al, 1.6 cat. % Er and 0.5 cat. % Yb,** which can be fabricated as described in the '247 application. Target 12 was first cleaned by sputtering with Ar (80 sccm) only in the metallic mode. Target 12 was then conditioned in poison mode by flowing 60 sccm of Argon and 40 sccm of oxygen respectively. The pulsed DC power supplied to target 12 was kept at 5 kW. Table 4 shows photoluminescence and index of refraction of as-deposited films from this example at some typical process conditions. The units for photoluminescence are the number of counts per micron. Lifetime and photoluminescence measured after annealing at various different temperatures are shown in Table 5.

Target 4

Target Power (KW)	Ar/O2 (sccm)	Pulsing Frequency (KHz)	Bias (W)	Reverse pulsing time (us)	532 nm PL/um	Index
5	60/34	120	100	2.3	3367	1.5333
5	60/30	120	100	2.3	3719	1.5334

Table 5

Anneal Temperature °C	Life Time (ms)	PL (532nm)/um
725	3	7000
775	3	7000
800	4	7500
825	4.7	8560
850	5.8	10000
900	6.9	17000

[0137] A waveguide amplifier was fabricated using this material in the similar fashion as described in examples 2-4. The active core was first deposited on substrate 16, which includes a

10um thermal oxide layer, using the following deposition parameters: target power 5KW, pulsing frequency 120KHz, bias 100W, reverse time 2.3us, Argon and Oxygen flow are 60 sccm and 30sccm respectively. The active core thickness is deposited to a thickness about 1.2μm, which takes approximately 1 hr. All wafers are preheated at about 350° C for 30min before deposition. A straight waveguide pattern is then formed by standard photolithography procedure. The active core was etched using reactive ion etch following by striping and cleaning. Next, a 10μm top cladding layer is deposited using similar process. The "92/8" (92 cat. % Si and 8 cat. % Al) metallic target was used to deposit top clad according to deposition parameters shown in Figure 9, resulting in a 4 % index difference between active core and cladding. The wave guide was then annealed at 800° C for about 30 min.

[0138] This waveguide was tested for gain using the method described in previous examples. However no net gain was observed from this waveguide since the passive loss was too high.

EXAMPLE 7

[0139] In addition to active material layers (i.e., layers having rare-earth ion concentrations), passive layers can also be deposited. Figure 9 shows deposition parameters for several target compositions, including some targets for deposition of passive (i.e., alloys of Al and Si with no rare earth ion concentration) layers. In this example, an embodiment of target 12 with a material composition of pure silicon is utilized.

[0140] Apparatus 10 can be based on an AKT 1600 reactor and deposited with about 1 to 3 kW of pulsed DC target power supplied to target 12. Particular depositions have been accomplished at 2.5 kW and 1.5 kW. The frequency of the pulsed DC power is between about 100 and 200 Khz. Some depositions were performed at 200 kHz while others were performed at 100 kHz. The reverse time was varied between about 2 μs and about 4 μs with particular depositions performed at 2.3 μs and 3.5 μs. The bias power to substrate 16 was set to zero.

[0141] Index variation of SiO2 films with bias to substrate 16 and deposition rates as a function of bias power to substrate 16 is shown in Figure 10.

[0142] The process gas included a mixture of Ar, N_2 and O_2. The Ar flow rates was set at 20 sccm while the O_2 flow rate was varied between about 5 and about 20 sccm and the N_2 flow rate was varied from about 2 to about 35 sccm. Figure 33 shows the variation in the index of refraction of a film deposition on substrate 16 as the O_2/N_2 ratio is varied.

EXAMPLE 8

[0143] Alternatively, films can be deposited on substrate 16 from a pure alumina target. In an example deposition with an embodiment of target 12 of alumina in an embodiment of apparatus 10 based on the AKT 1600 reactor, the pulsed DC target power was set at 3 kW and the frequency was varied between about 60 kHz and 200 kHz. The reverse time was set at 2.5 μs. Again, no bias power was supplied to substrate 16. The O_2 flow rate was varied from about 20 to about 35 sccm, with particular depositions performed at 22 and 35 sccm. The Ar flow rate was set at 26 sccm. A post deposition anneal of substrate 16 at 800° C for 30 min. was performed.

[0144] Figure 12 shows the variation of refractive index of the film deposited on substrate 16 with varying frequency of the pulsed DC power supplied to target 12. Figure 11 shows the variation in refractive index of a film deposited on substrate 16 with varying O_2/Ar ratio. As can be seen from Figures 33, 34 and 35, the index of refraction of films deposited from alumina can be adjusted by adjusting the process gas constituents or by adjusting the frequency of the pulsed DC power supplied to target 12 during deposition.

EXAMPLE 9

[0145] Additionally, passive films can be deposited from targets having a composition of Si and Al. For example, layers have been deposited from embodiments of target 12 with composition 83 % Si and 17 % Al. About 4.5 kW of pulsed DC power at about 200 kHz frequency was supplied to target 12. The reverse time was about 2.2 μs. A bias power of about 150 W was supplied to substrate 16 during deposition. Figures 14 and 15 show variation of the index of refraction for subsequent runs from this target.

[0146] The examples and embodiments discussed above are exemplary only and are not intended to be limiting. One skilled in the art can vary the processes specifically described here in various ways. Further, the theories and discussions of mechanisms presented above are for discussion only. The invention disclosed herein is not intended to be bound by any particular theory set forth by the inventors to explain the results obtained. As such, the invention is limited only by the following claims.

Claims

We claim:

1. A method of depositing a film on a substrate, comprising:

providing pulsed DC power through a filter to a target;

providing bias power to a substrate positioned opposite the target;

providing process gas between the target and the substrate,

wherein the filter protects a pulsed DC power supply from the bias power.

2. The method of Claim 1, further including holding the temperature of the substrate substantially constant.

3. The method of Claim 1, wherein providing pulsed DC power through the filter includes supplying up to about 10 kW of power at a frequency of between about 40 kHz and about 350 kHz and a reverse time pulse between about 1.3 and 5 μs.

4. The method of Claim 1, wherein providing bias power to the substrate includes supplying up to 1000 W of RF power to the substrate.

5. The method of Claim 4, wherein the filter is a band reject filter at the frequency of the bias power.

6. The method of claim 4, wherein the bias power is zero.

7. The method of Claim 1, wherein the film is an upper cladding layer of a waveguide structure and the bias power is optimized to provide planarization.

8. The method of Claim 1, wherein the process gas includes a mixture of Oxygen and Argon.

9. The method of Claim 9, wherein the Oxygen flow is adjusted to adjust the index of refraction of the film.

10. The method of Claim 8, wherein the process gas further includes nitrogen.

11. The method of Claim 1, wherein providing pulsed DC power to a target includes providing pulsed DC power to a target which has an area larger than that of the substrate.

12. The method of Claim 1, further including uniformly sweeping the target with a magnetic field.

13. The method of Claim 12, wherein uniformly sweeping the target with a magnetic field includes sweeping a magnet in one direction across the target where the magnet extends beyond the target in the opposite direction.

14. The method of Claim 1, further including depositing a film on the backside of target 12.

15. A reactor according to the present invention, comprising:

a target area for receiving a target;

a substrate area opposite the target area for receiving a substrate;

a pulsed DC power supply; and

a bias power supply coupled to the substrate.

16. The reactor of Claim 15, wherein the target has a surface area greater than the surface area of the substrate.

17. The reactor of Claim 15, further including a scanning magnet which provides uniform erosion of the target.

18. The reactor of Claim 17, wherein the scanning magnet scans across the target in a first direction and extends in a second direction perpendicular to the first direction.

19. The reactor of Claim 18, wherein the magnet extends beyond the target in the second direction.

20. A method of depositing a film on a substrate, comprising:

conditioning a target;

preparing the substrate;

adjusting the bias power to the substrate;

setting the process gas flow; and

applying pulsed DC power to the target to deposit the film.

21. The method of Claim 20, wherein conditioning the target includes sputtering with the target in a metallic mode to remove the surface of the target and sputtering with the target in poisonous mode to prepare the surface.

22. The method of Claim 21, wherein setting the process gas flow includes adjusting constituents in order to adjust the index of refraction of the film.

23. The method of Claim 21, wherein applying pulsed DC power includes setting the frequency in order to adjust the index of refraction of the film.

24. The method of Claim 21, further including adjusting a temperature of the substrate in order to adjust the index of refraction of the film.

25. A method of forming a waveguide amplifier, comprising:

providing a substrate with an undercladding layer;

providing a target having a concentration of rare-earth ions opposite the substrate;

supplying process gas between the target and the substrate;

applying pulsed DC power through a filter to the target to deposit a film;

patterning the film to form a core;

depositing an uppercladding layer over the core.

26. The method of Claim 25, wherein providing a substrate includes providing a silicon substrate with a thermal oxide layer.

27. The method of Claim 25, wherein providing a target includes providing a target having a concentration of up to about 5 cat. % of rare earth ions.

28. The method of Claim 27, wherein providing a target includes providing a target of Al and Si.

29. The method of claim 25, wherein providing a target includes providing a target with a concentration of Al.

30. The method of Claim 29, wherein providing a target includes providing a target with a concentration of Si.

31. The method of Claim 29, wherein providing a target includes providing a target with a concentration of rare earth ions.

32. The method of Claim 25, further including providing bias power to the substrate.

33. The method of Claim 25, further including scanning a magnet over the target.

34. The method of Claim 25, wherein scanning the magnet over the target includes moving the magnet in a first direction.

35. The method of Claim 34, wherein the magnet extends beyond the target in a second direction perpendicular to the first direction.

36. The method of Claim 25, wherein the target has a surface area greater than the surface area of the substrate.

37. The method of Claim 32, wherein the filter rejects power at a frequency of the bias power.

38. A sputtering apparatus, comprising:

means for providing pulsed DC power to a target; and

means for providing bias power to a substrate.

39. The apparatus of Claim 38, further including

means for providing process gas between the target and the substrate.

Biased Pulse DC Reactive Sputtering of Oxide Films

Hongmei Zhang
Mukundan Narasimhan
Ravi Mullapudi
Richard E. Demaray

Abstract

A biased pulse DC reactor for sputtering of oxide films is presented. The biased pulse DC reactor couples pulsed DC at a particular frequency to the target through a filter which filters out the effects of a bias power applied to the substrate, protecting the pulsed DC power supply. Films deposited utilizing the reactor have controllable material properties such as the index of refraction. Optical components such as waveguide amplifiers and multiplexers can be fabricated using processes performed on a reactor according to the present inention.

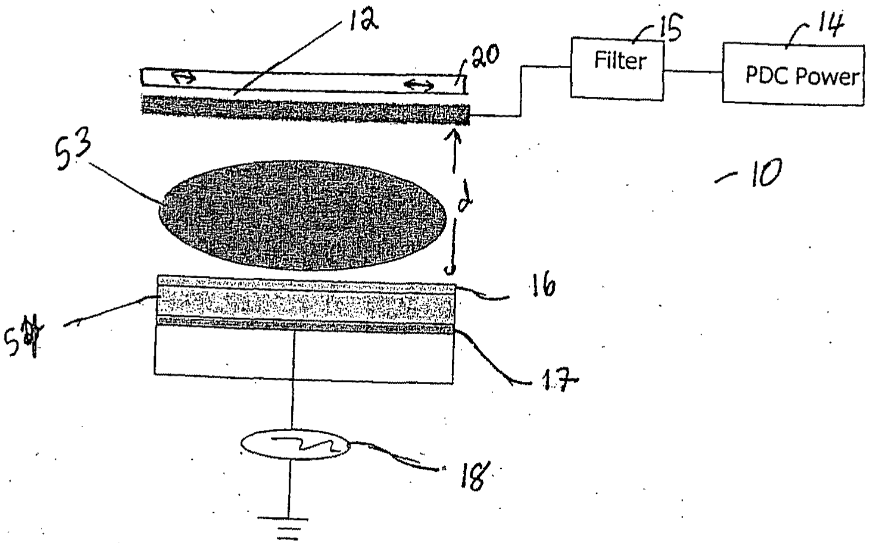

Figure 1A

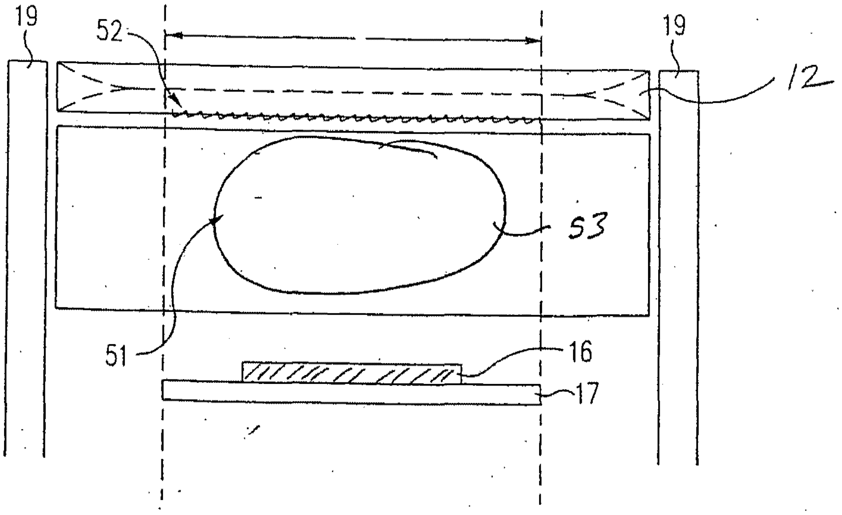

FIG. 1B

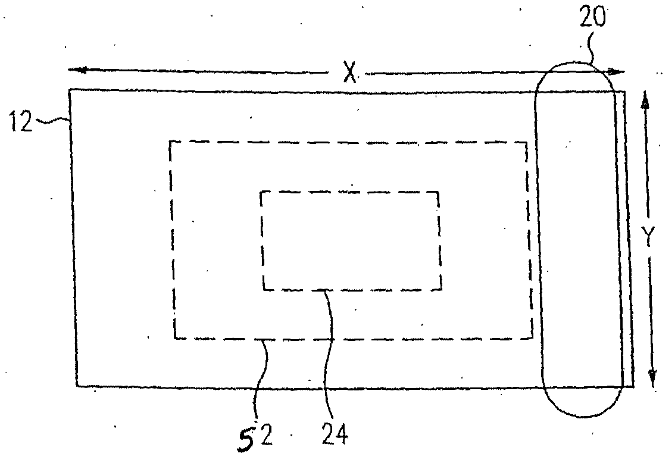

FIG. 2

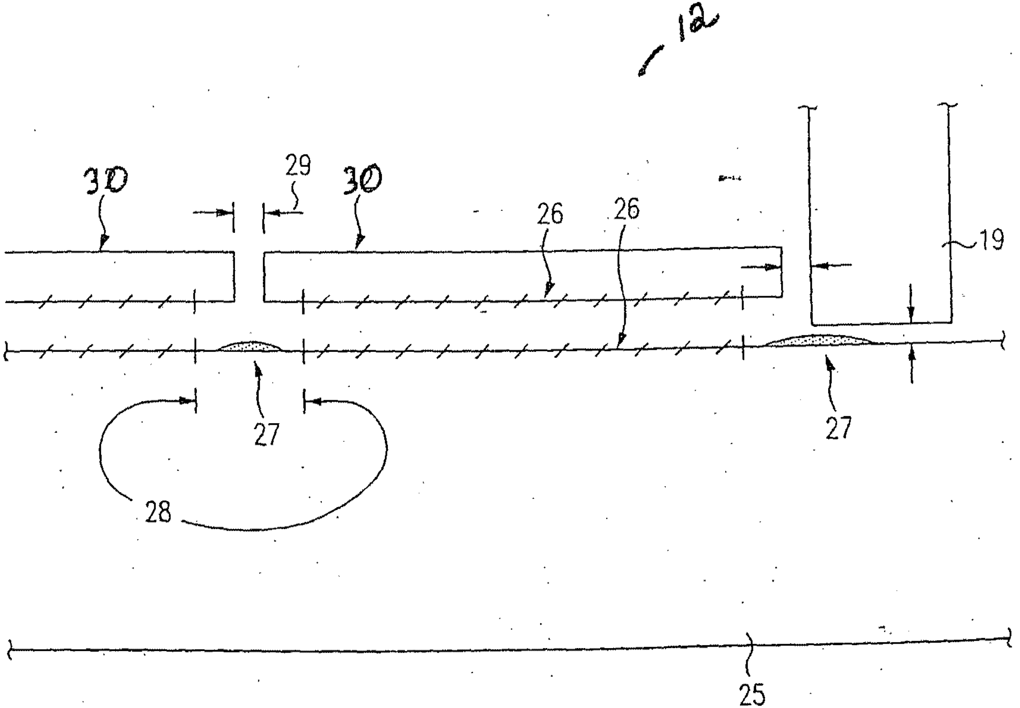

FIG. 3

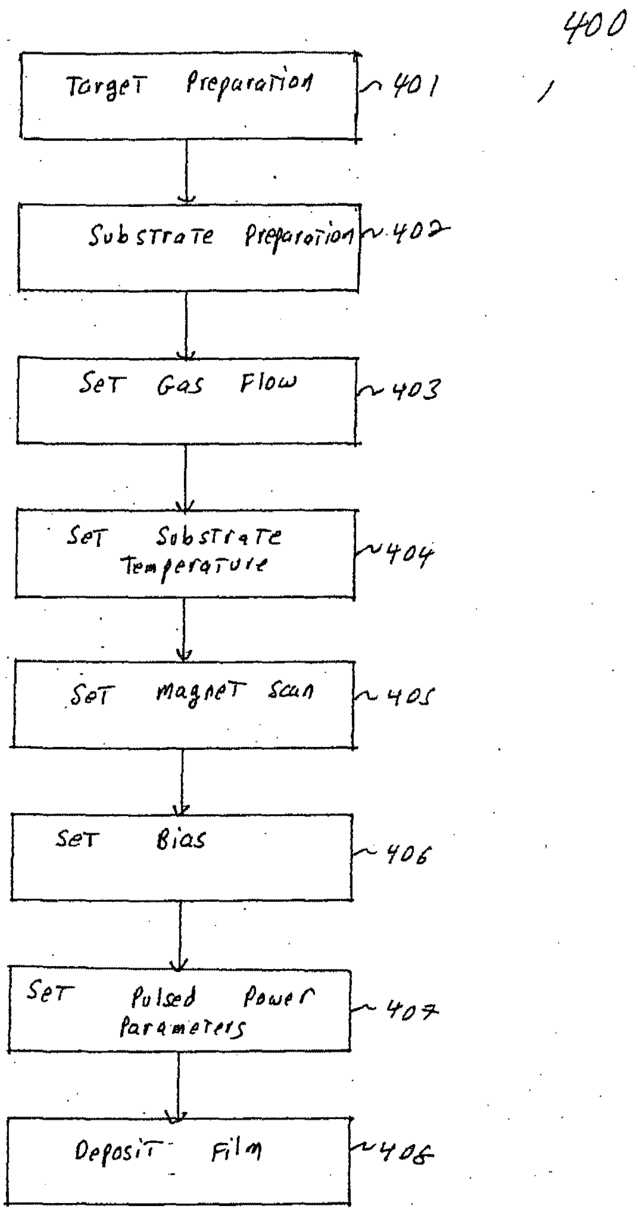
400
Target Preparation
401
Substrate Preparation
402
Set Gas Flow
403
Set Substrate Temperature
404
Set magnet Scan
405
Set Bias
406
Set Pulsed Power Parameters
407
Deposit Film
408

Figure 4

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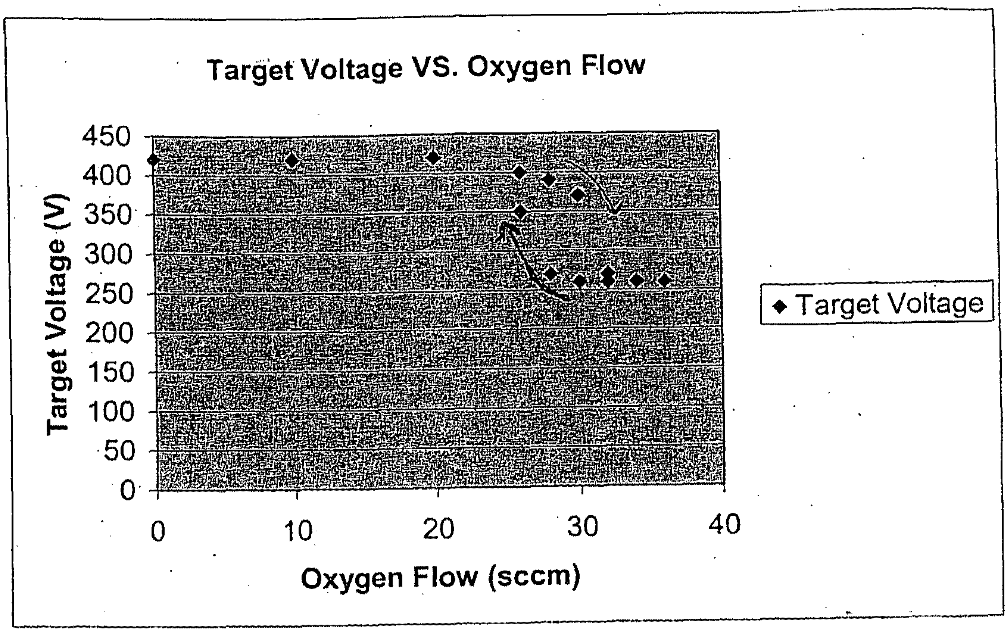

Figure 5

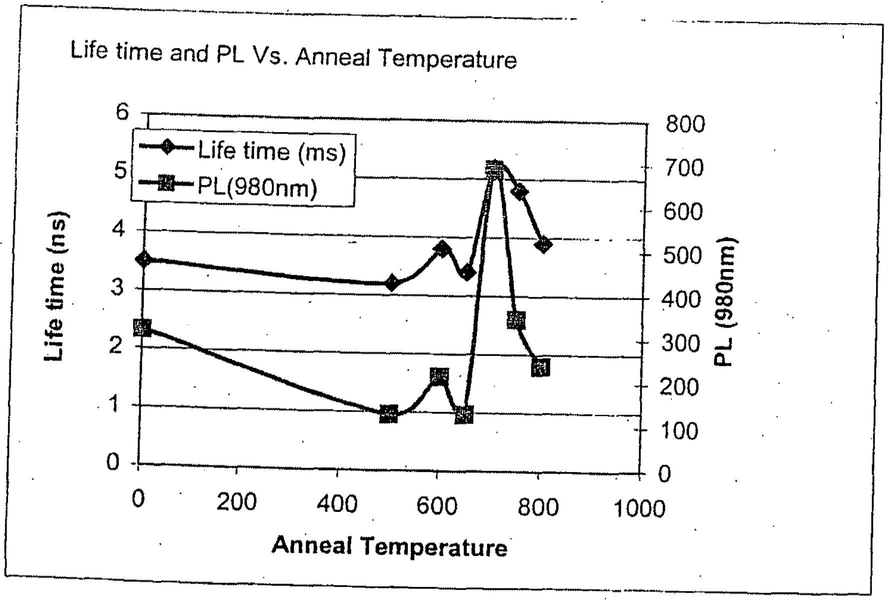

Figure 6

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Alumino Silicates Index Drift in Burn-in Cycle (As Deposited from Al/Si Cast Metal Targets)

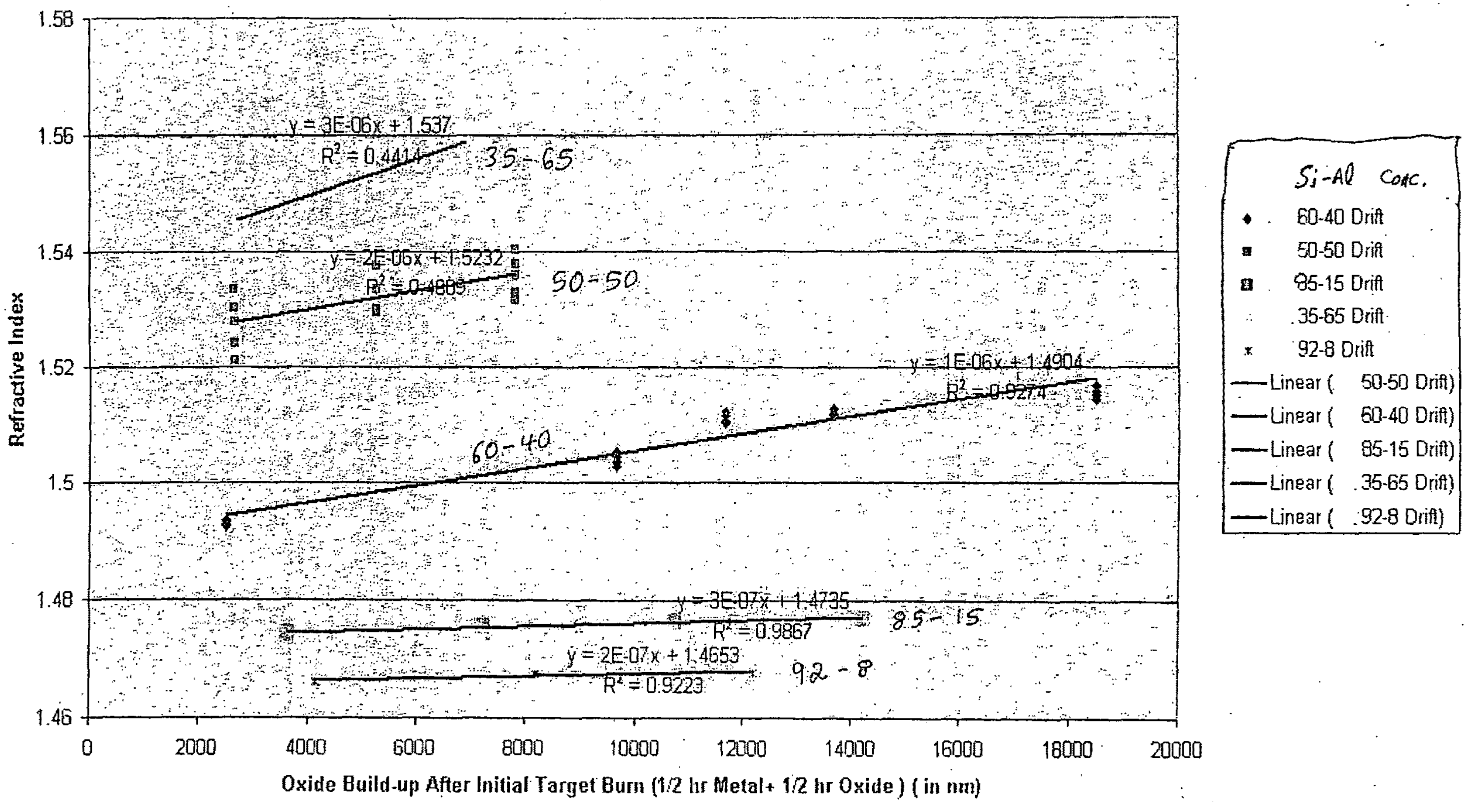

Figure 7

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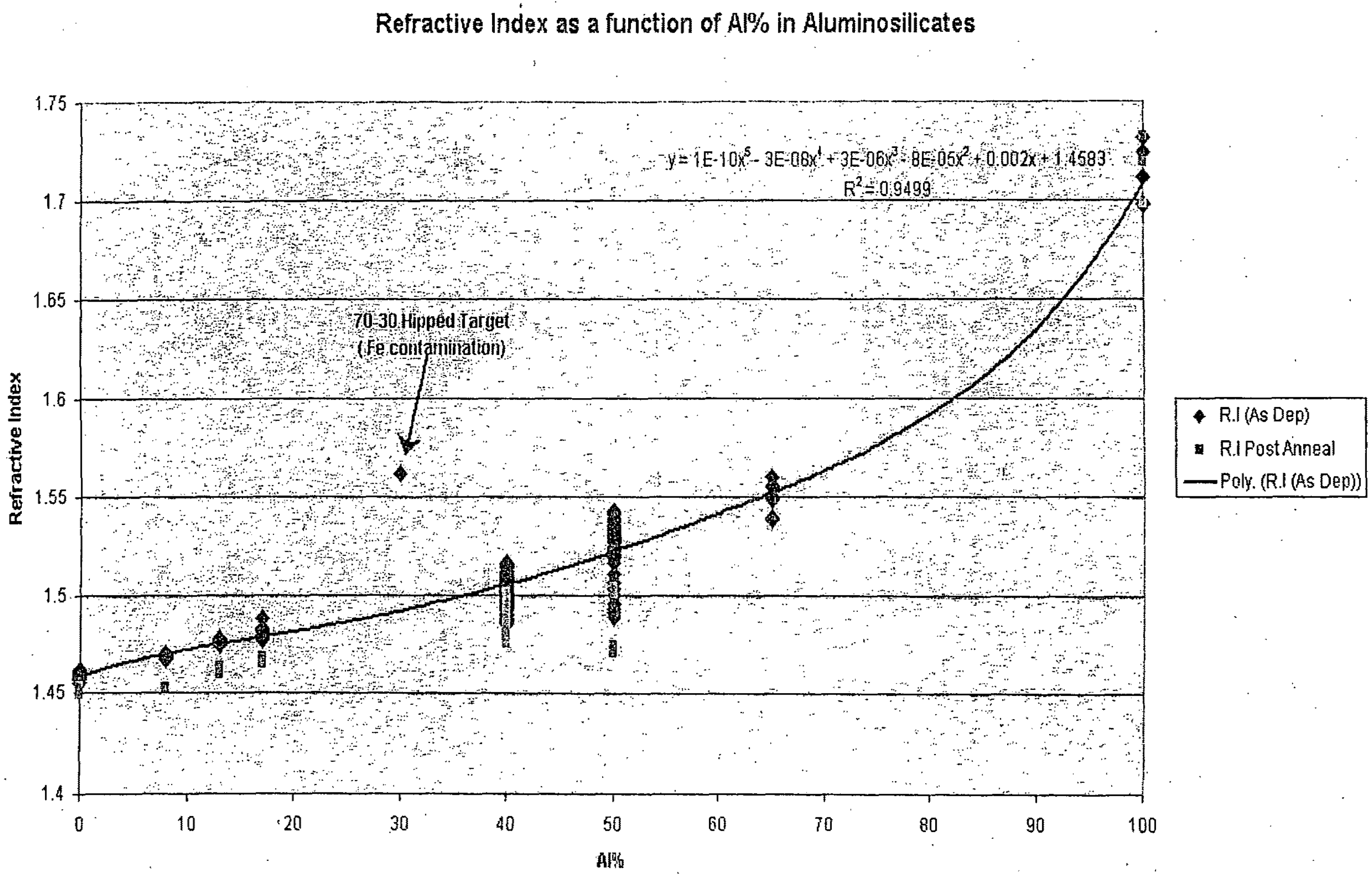

Figure 8

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Material (Er/Yb/Al/Si)	**Expected index (Post anneal)**	**Actual index (Post anneal)**	**Process Conditions (Annealed 725c 30min)**
0.8/0.8/41.4/57	1.506	1.510	6KW, Ar-60,O2-28sccm, 120KHz, 2.2us, 60mm T-W Space, 4-5mm T-M Space, 0-400W Bias
1.6/0.5/49/48.9	1.526	1.528	6KW, Ar-60,O2-28sccm, 120KHz, 2.2us, 60mm T-W Space, 4-5mm T-M Space, 0-400W Bias
0/0/8/92	1.452	1.456-1.459	4.5KW, Ar-30-60,O2-28-44, 120-200Khz, 2.2us, 60-85mm T-W Space, 4-5mm T-M Space, 0-400W Bias
0/0/40/60	1.504	1.486-1.501	3.0-4.5KW, Ar-30,O2-44, 75-200Khz, 2.2-3.0us, 60-85mm T-W Space, 4-5mm T-M Space, 0-400W Bias
0/0/50/50	1.520	1.491-1.503	4.0-4.5KW, Ar-30,O2-44, 75-200Khz, 2.2-3.0us, 60-85mm T-W Space, 4-5mm T-M Space, 0-400W Bias
0/0/65/35	1.544	1.545-1.560	4.5-5.5KW, Ar75-90, O285-100, 200Khz,2.2us, 85mm T-W Space, 4-5mm T-M Space, 0-400W Bias
0/0/30/70	1.490	1.562 (high Fe content)	5.0KW, Ar75, O2-100, 200Khz,2.2us, 85mm T-W Space, 4-5mm T-M Space, 0-400W Bias
1.5/0/48.5/50	1.523	1.509-1.513	6KW, Ar-60,O2-28sccm, 120KHz, 2.2us, 60mm T-W Space, 4-5mm T-M Space, 0-400W Bias

Figure 9

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Bias Power (Watts)	DC Power (KW)	Pulsing Freq (KHz)	Reverse Time (µs)	Ar Flow (sccms)	O2 Flow (sccms)	Wafer Position	Target To Wafer Spacing (mm)	Refractive Index Avg (@1550nm)	Refractive Index STD (@1550nm)	Dep Rate (um/Hr)
150	4.5	200	2.2	100	100	1	55	1.461508	0.000535	0.957654
150	4.5	200	2.2	100	100	2	55	1.462329	0.000376	0.962581
400	4.5	200	2.2	100	100	1	55	1.462774	0.000103	0.814007
400	4.5	200	2.2	100	100	2	55	1.463583	0.000095	0.824566

Figure 10

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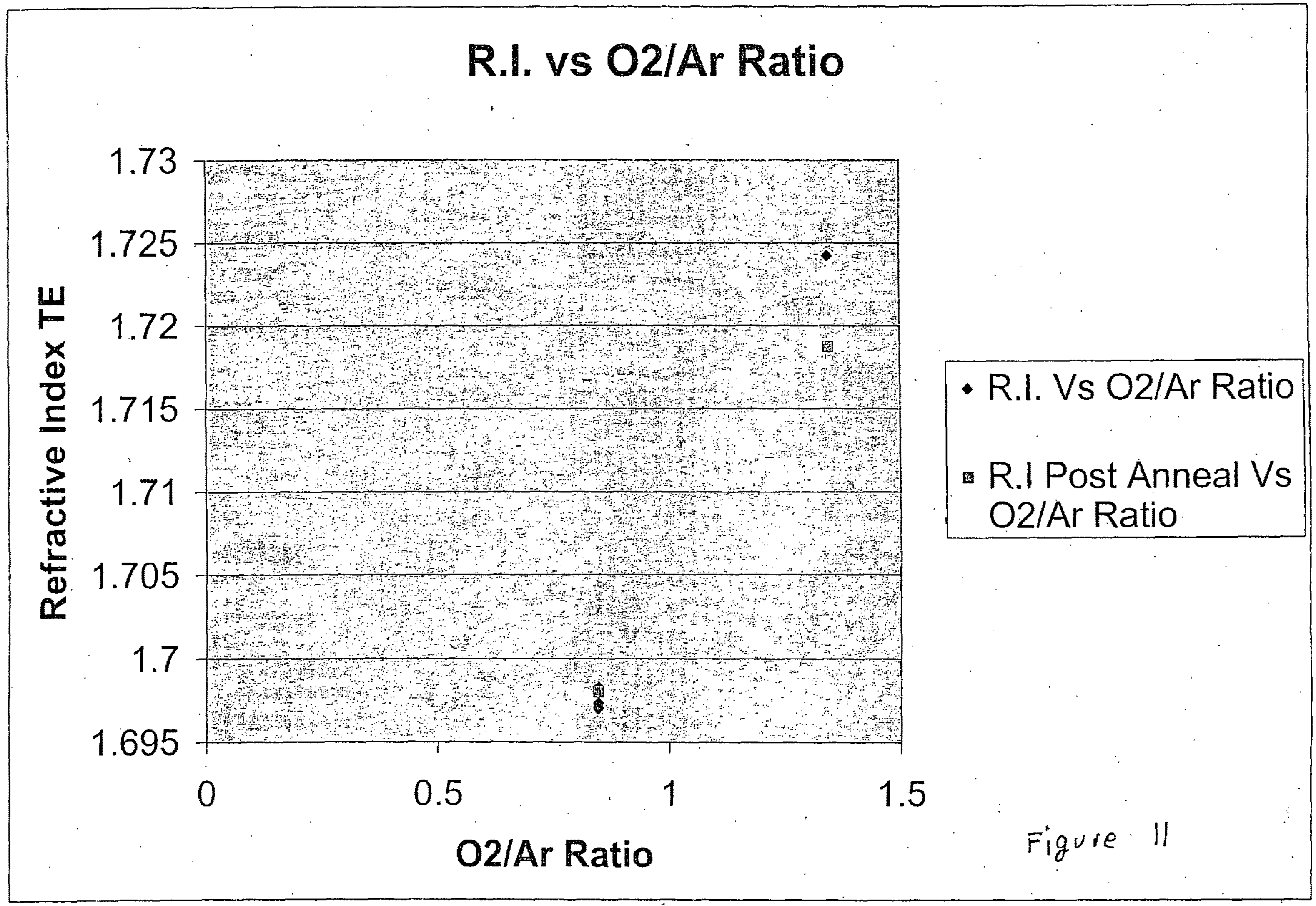

Figure 11

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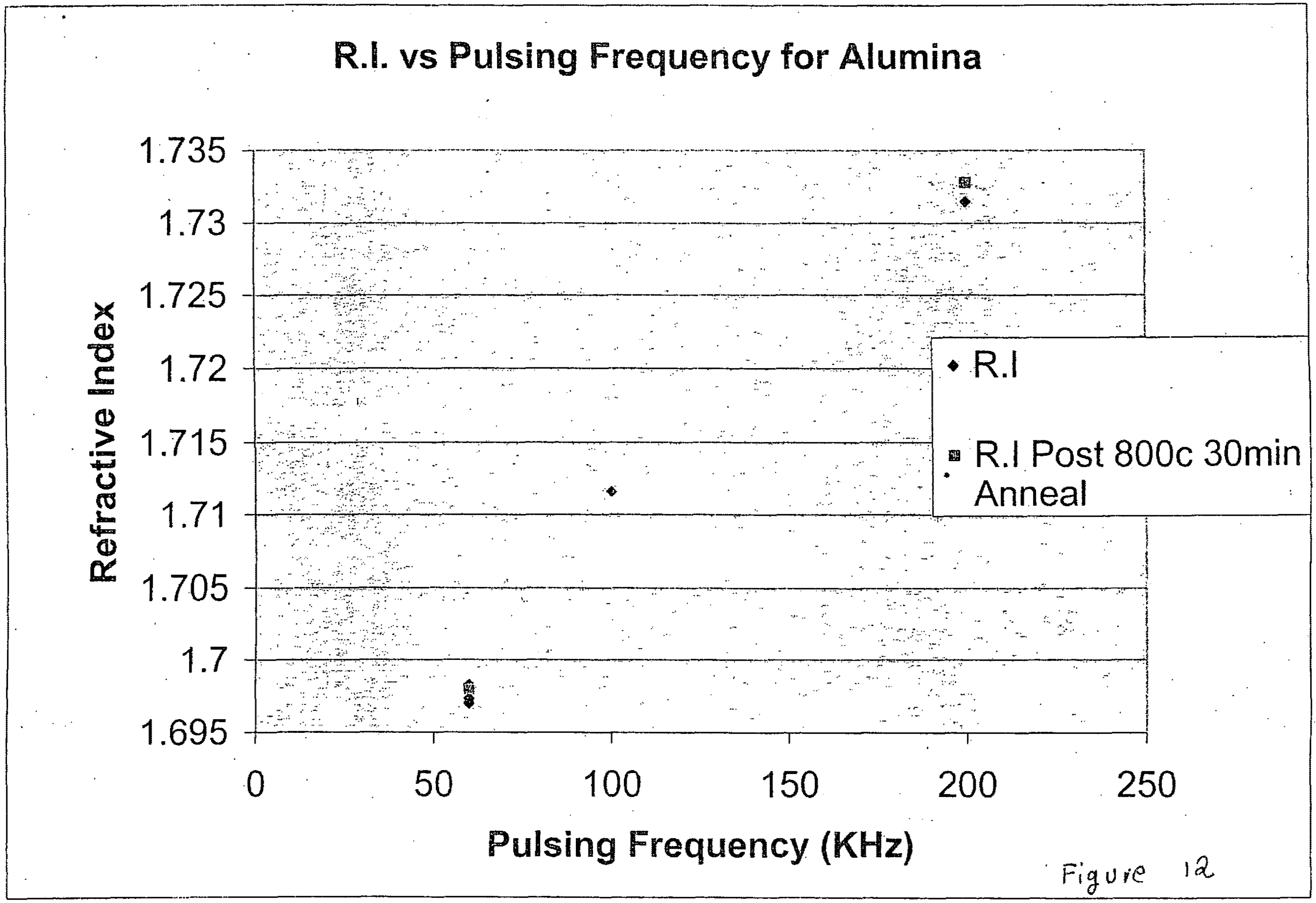

Figure 12

Target 92-8

AET 4300 Based Reactor

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Index and Dep Rate Drifts Pre & Post Anneal

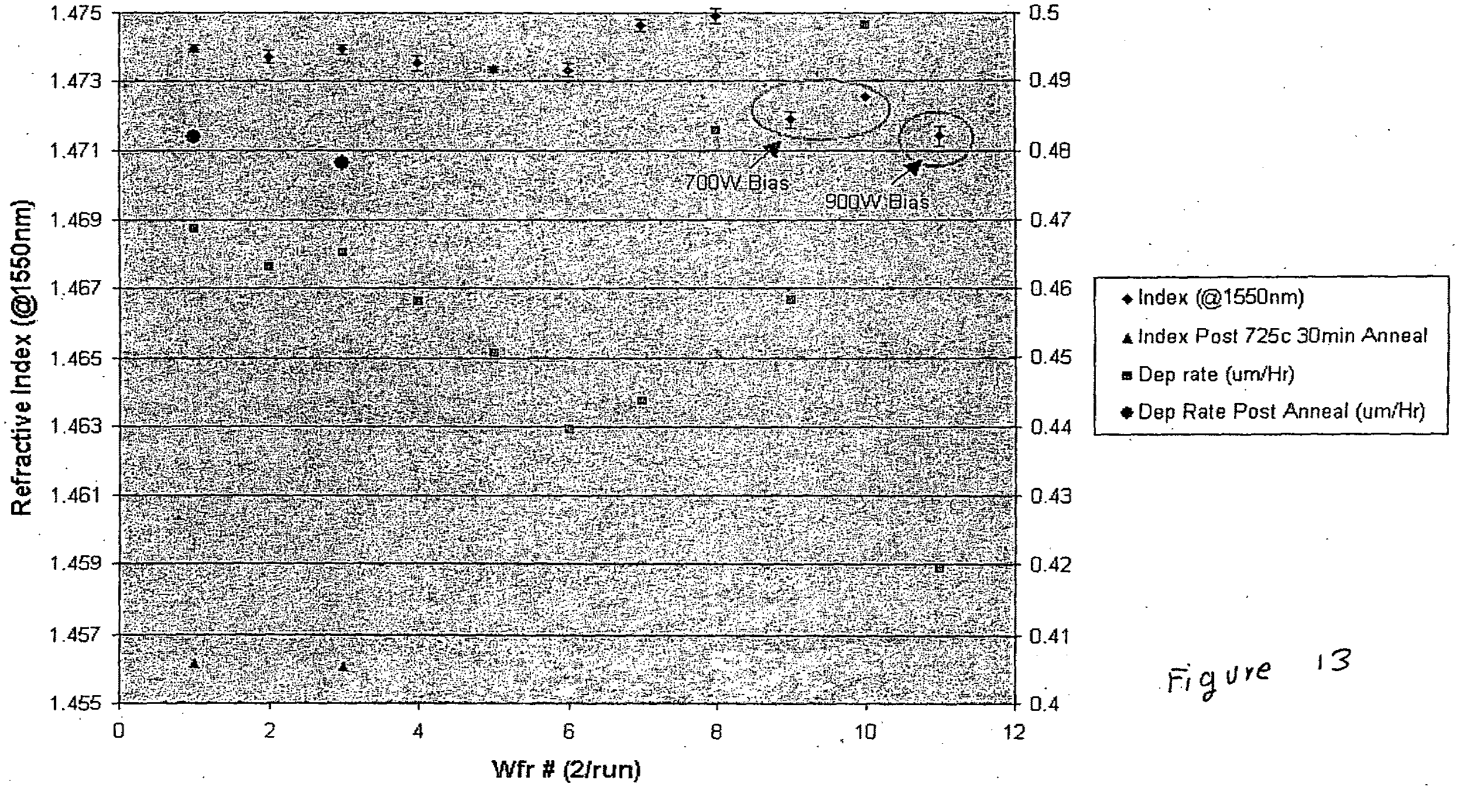

Figure 13

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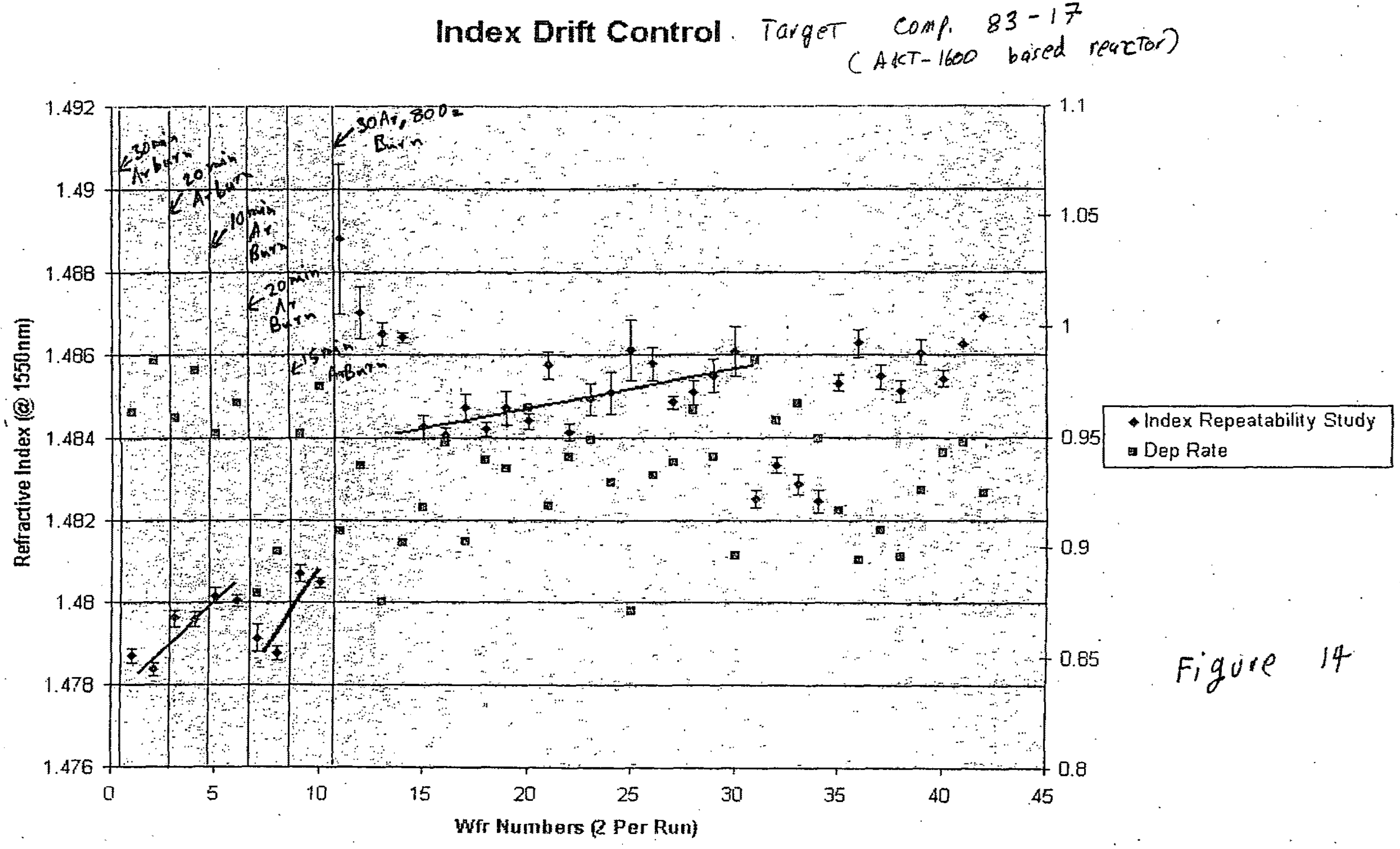

Target Comp. 83-17
(AKT-1600 based reactor)

Figure 14

83-17 Target / AKT 1600 based reactor.

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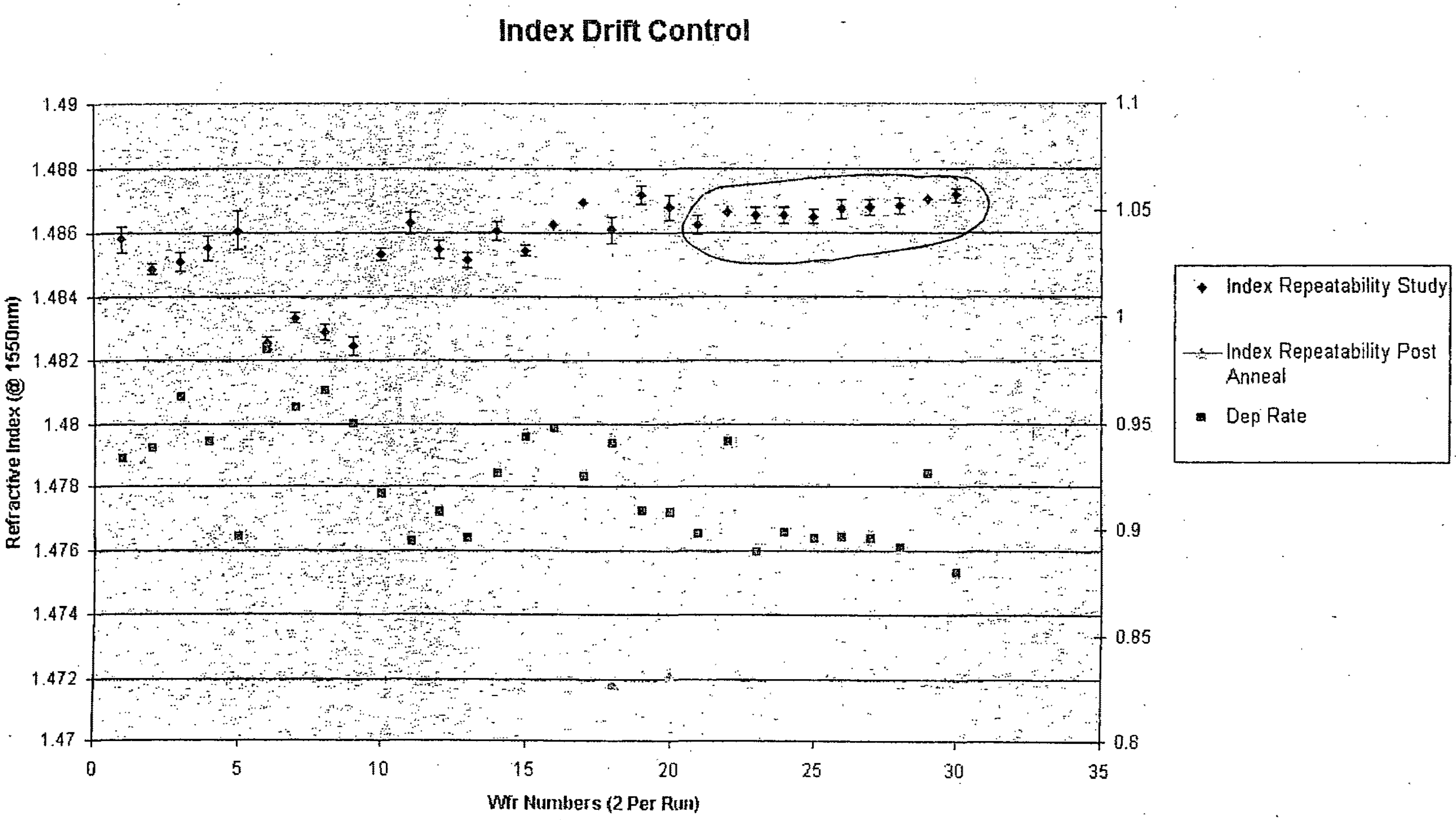

Figure 15

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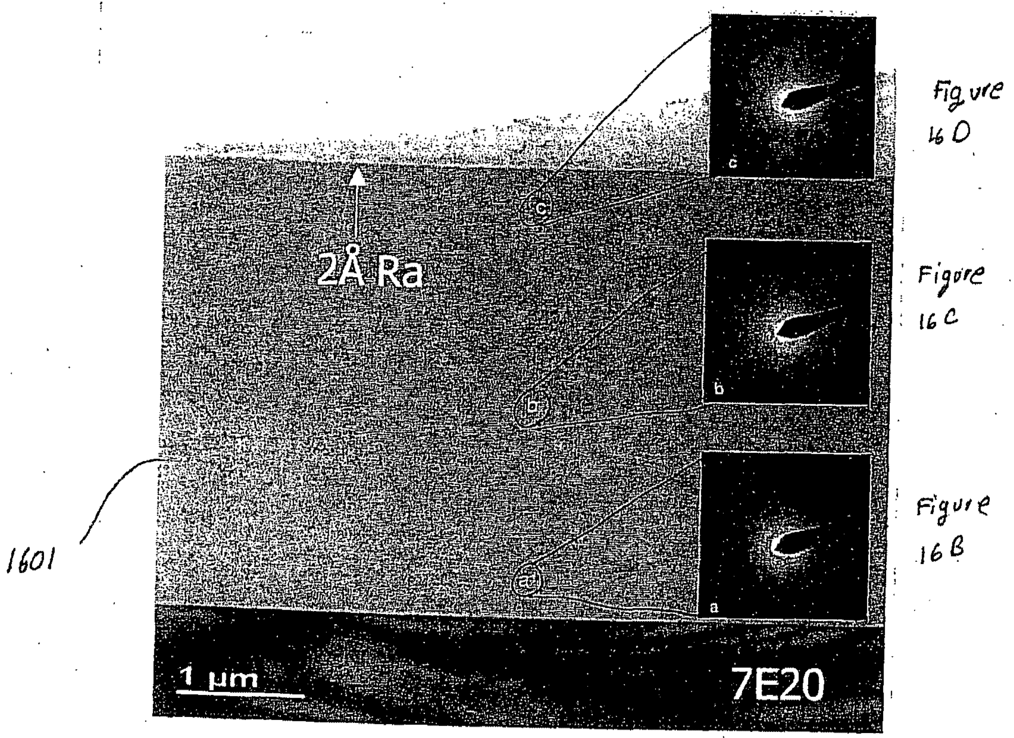

Symmorphix PVD aluminosilicate

Figure 16 A

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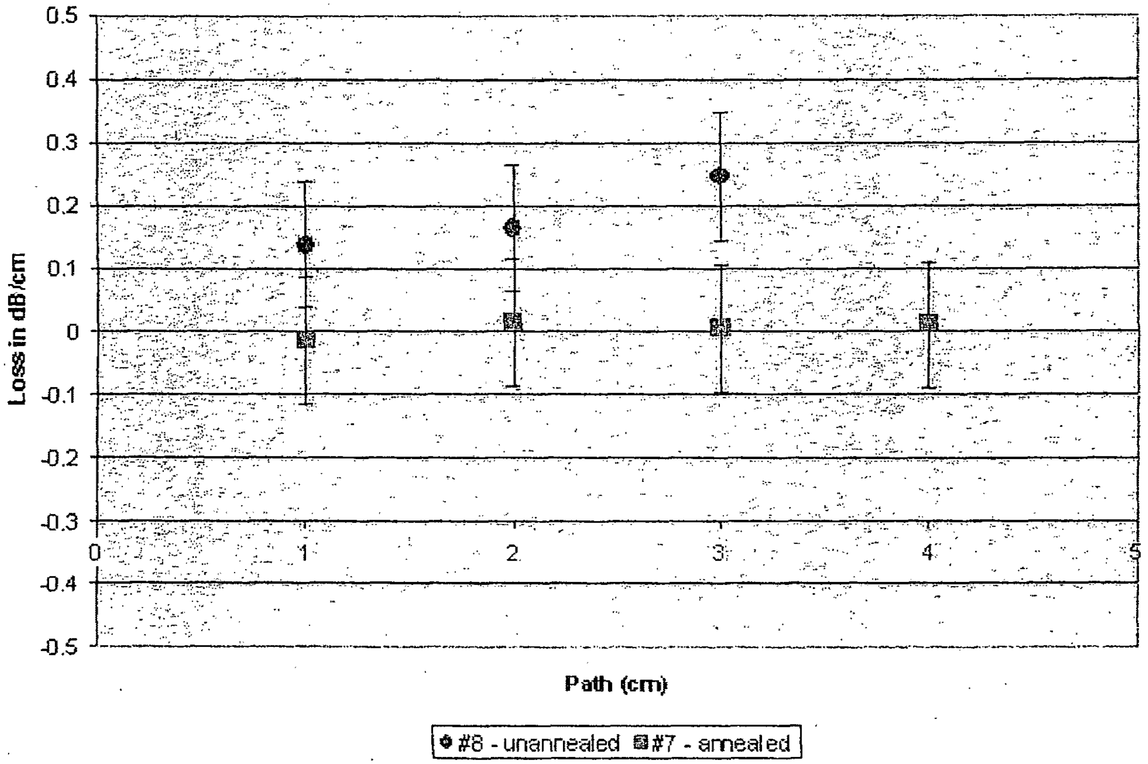

Figure 17

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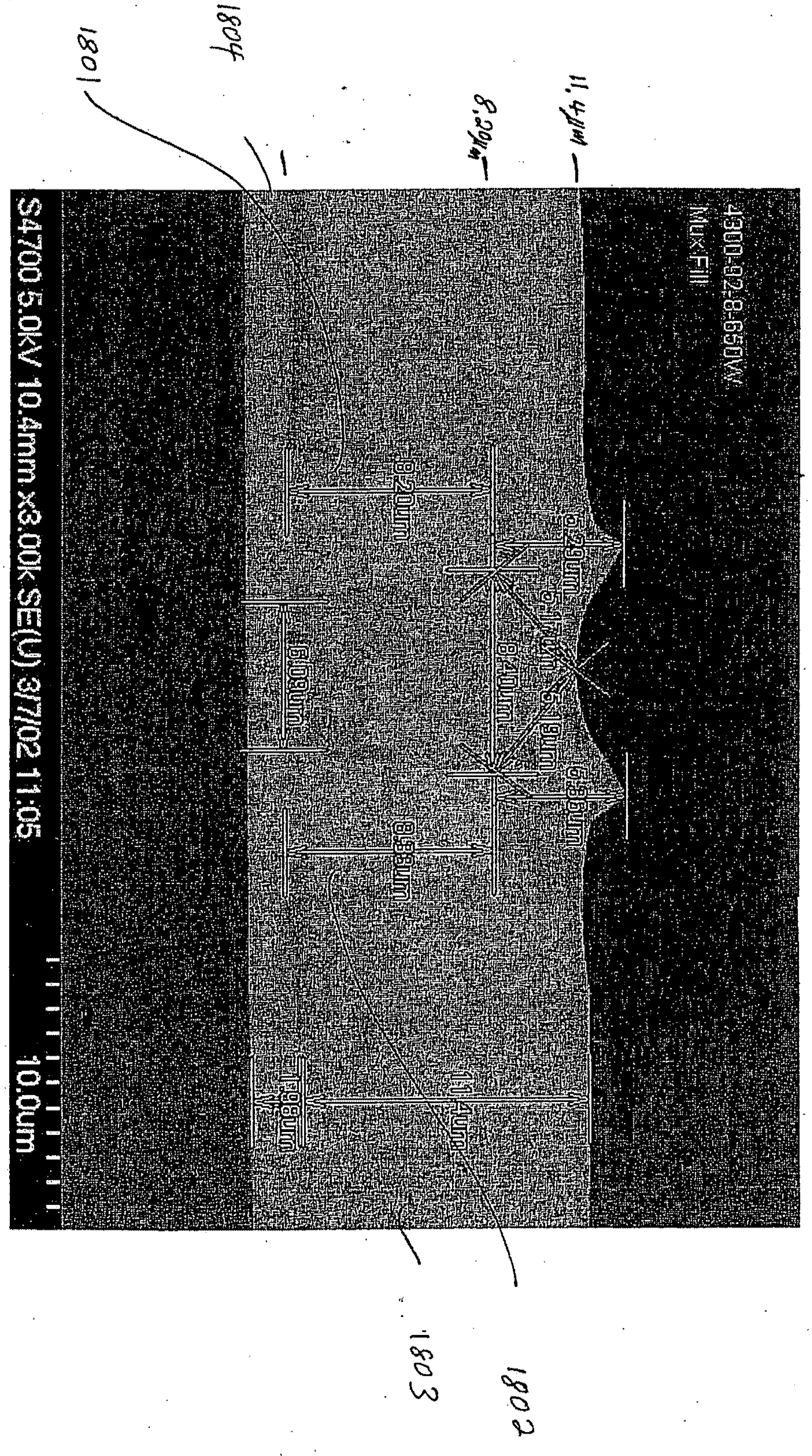


Figure 18

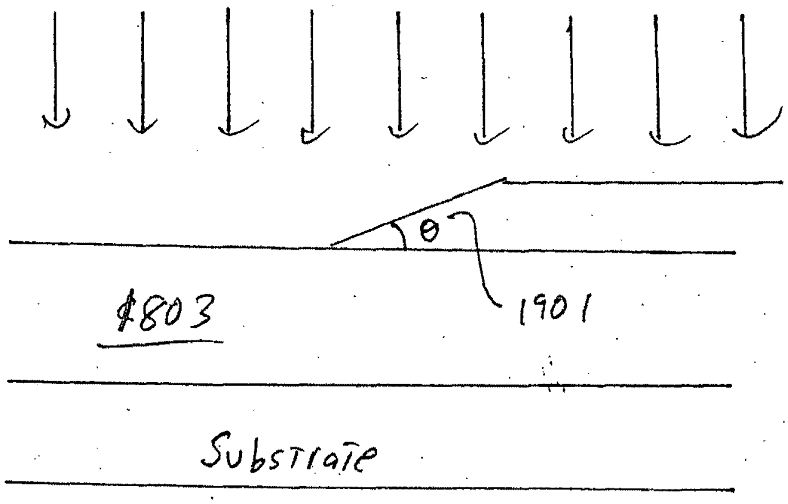


Figure 19

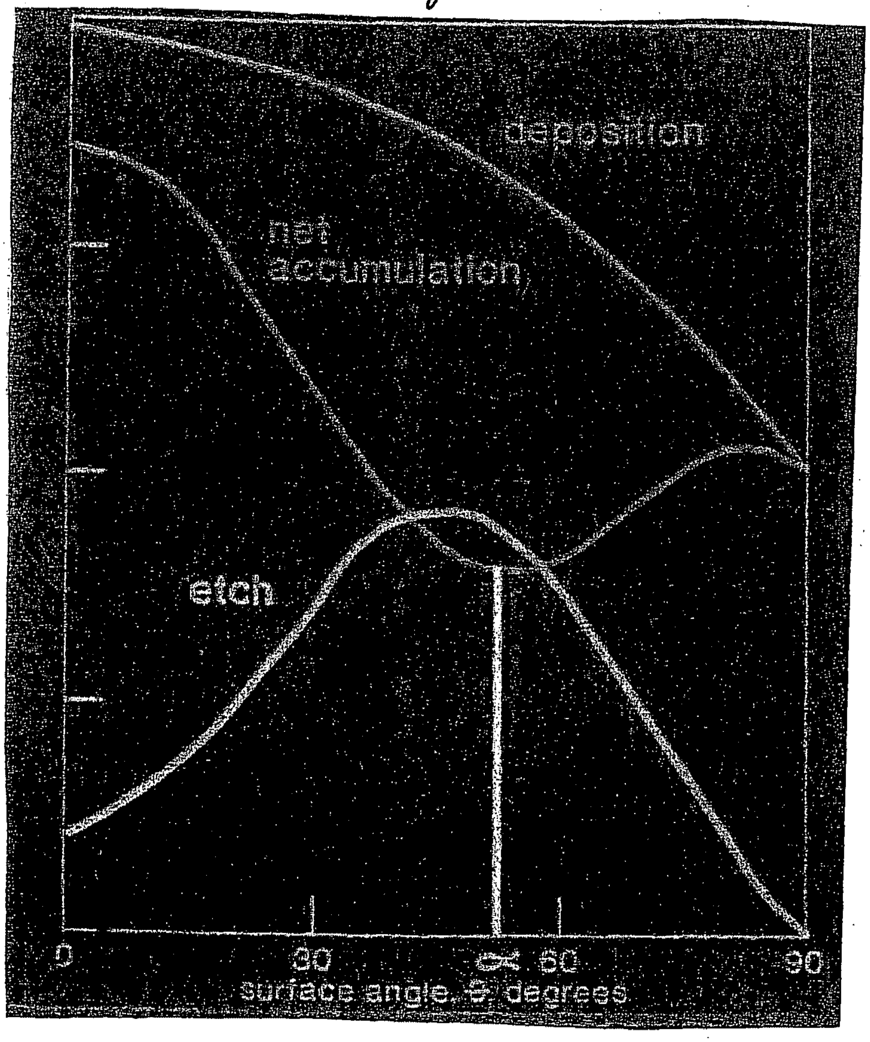


Figure 20

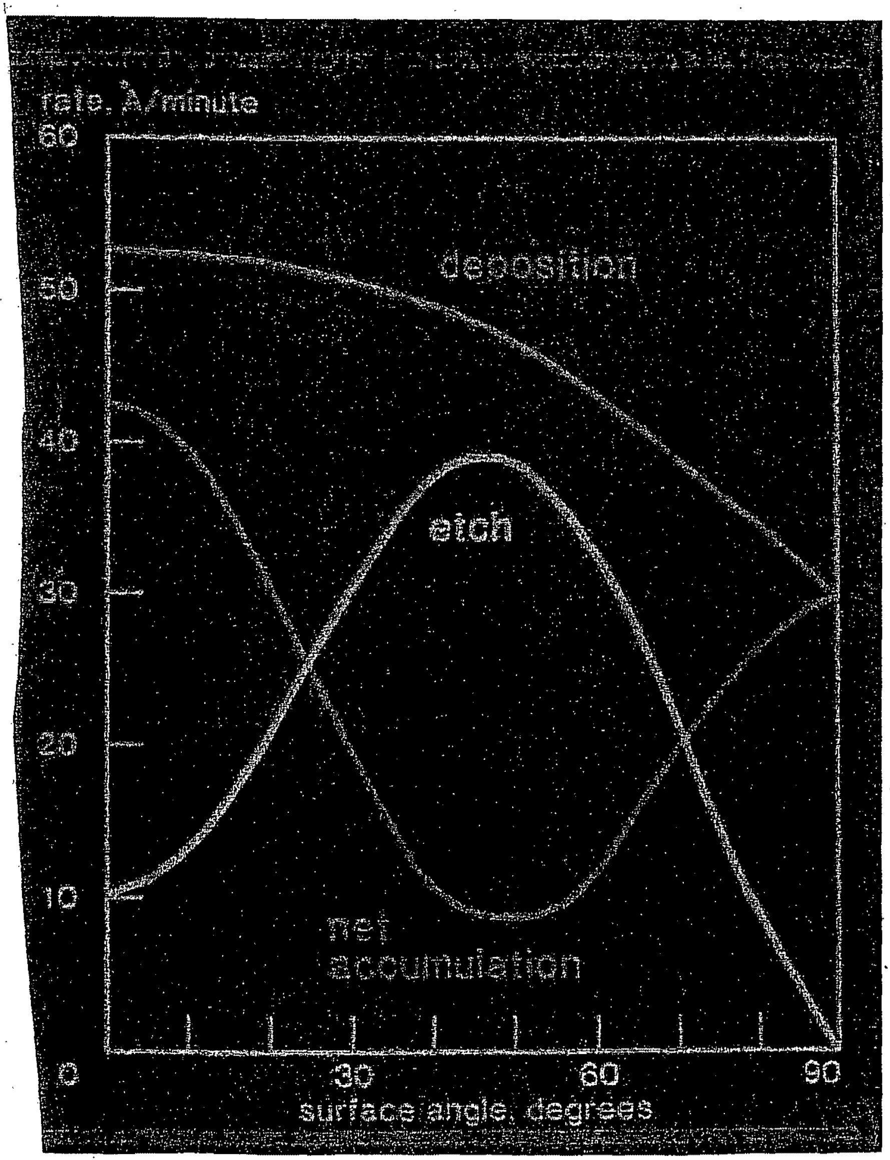

rate, Å/minute
60
50
40
30
20
10
0
deposition
etch
net
accumulation
30
60
90
surface angle, degrees

Figure 21

m-12245 US
19/27

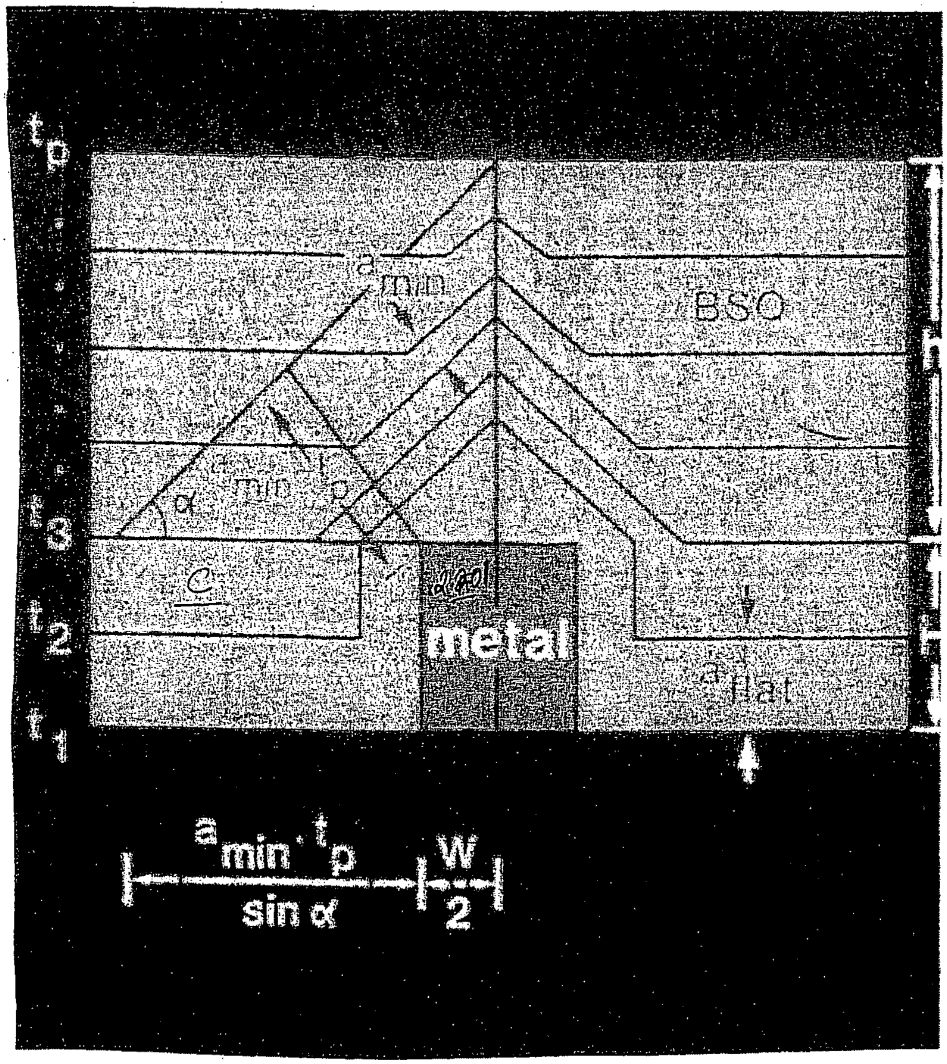


Figure 22

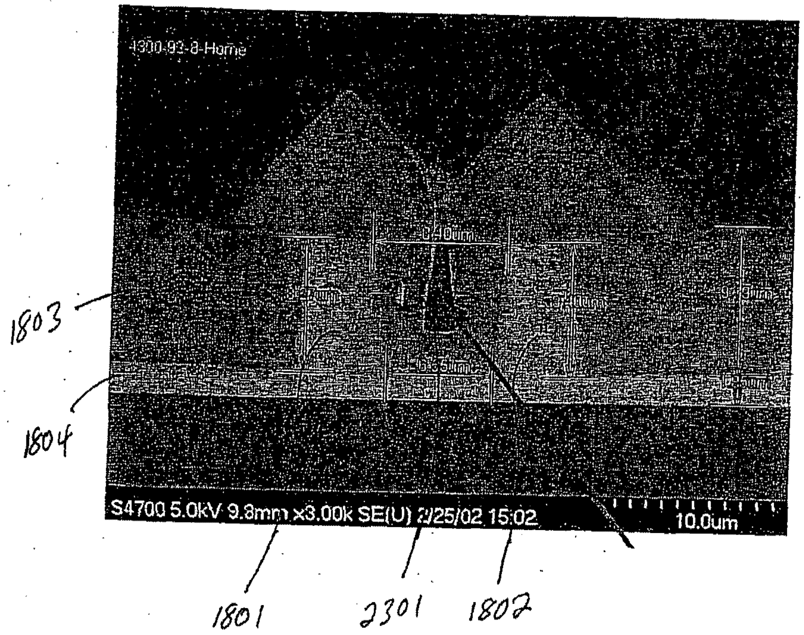

4300-93-8-Home
0.40um
S4700 5.0kV 9.8mm x3.00k SE(U) 2/25/02 15:02
10.0um
1803
1804
1801
2301
1802

Figure 23

m- 12 245 US
21/27

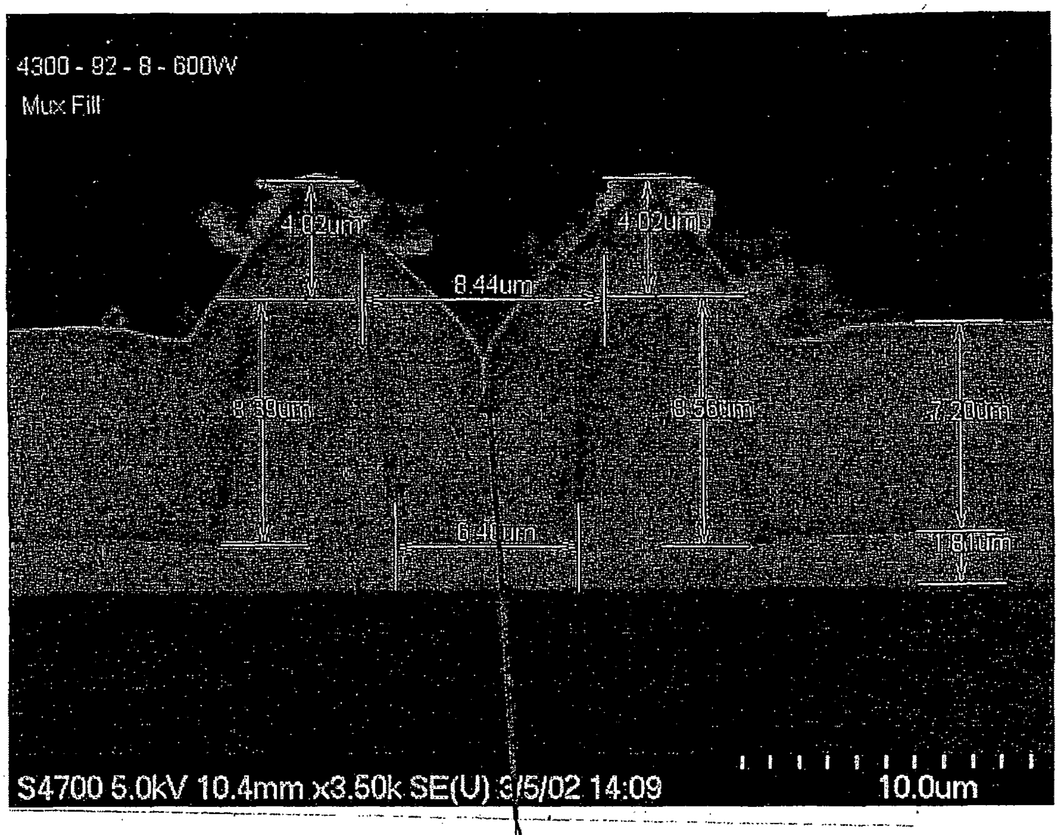


Figure 24

m-12245 US
22/27

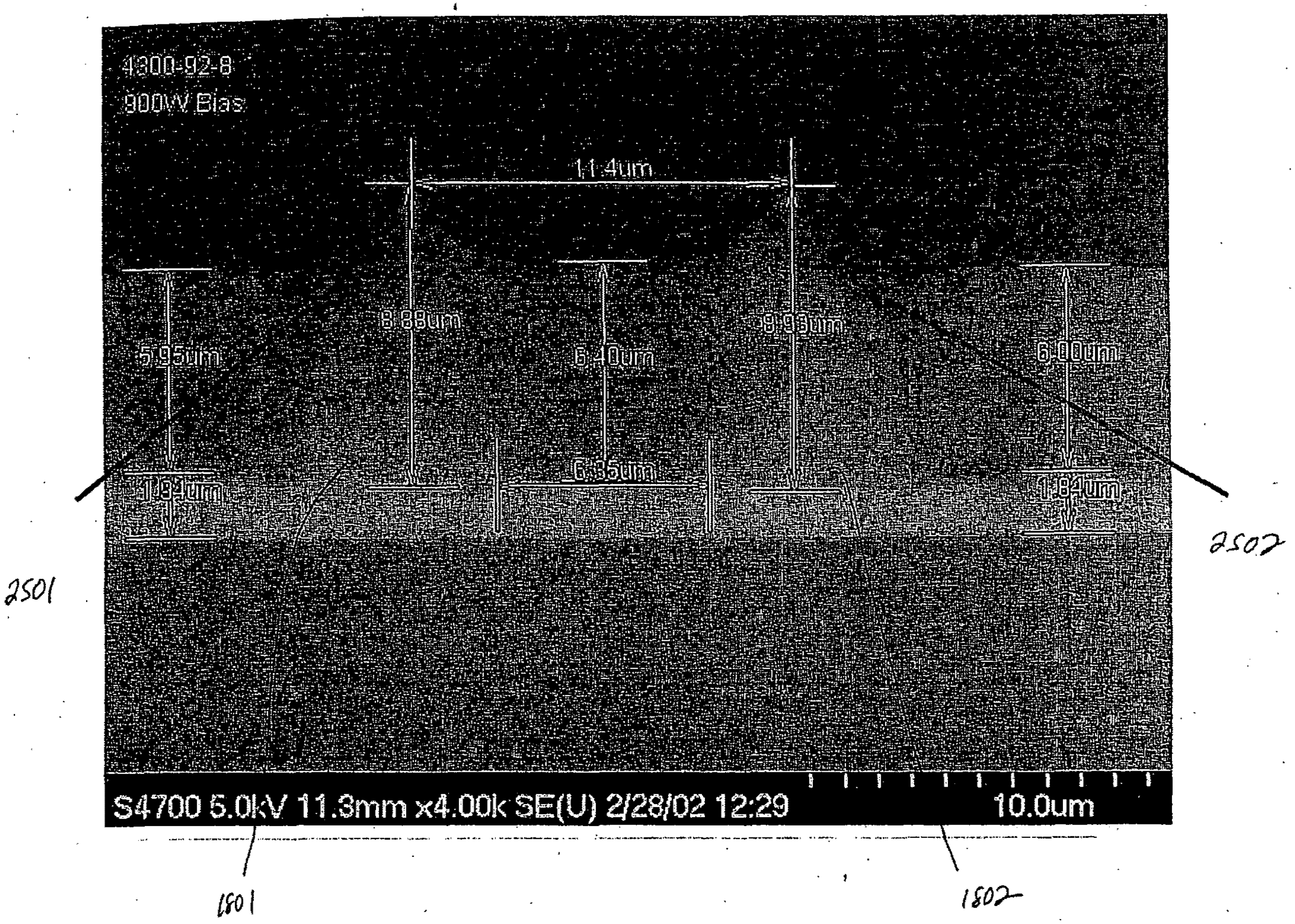


Figure 25

m- 12245 US
23/27

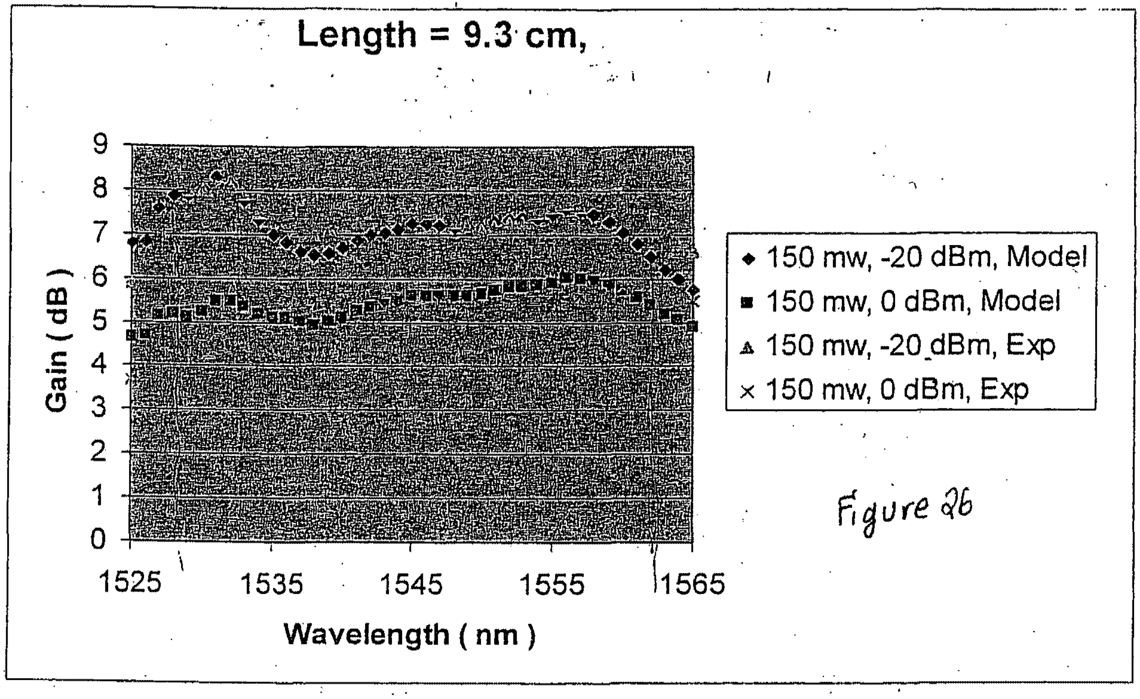


Figure 26

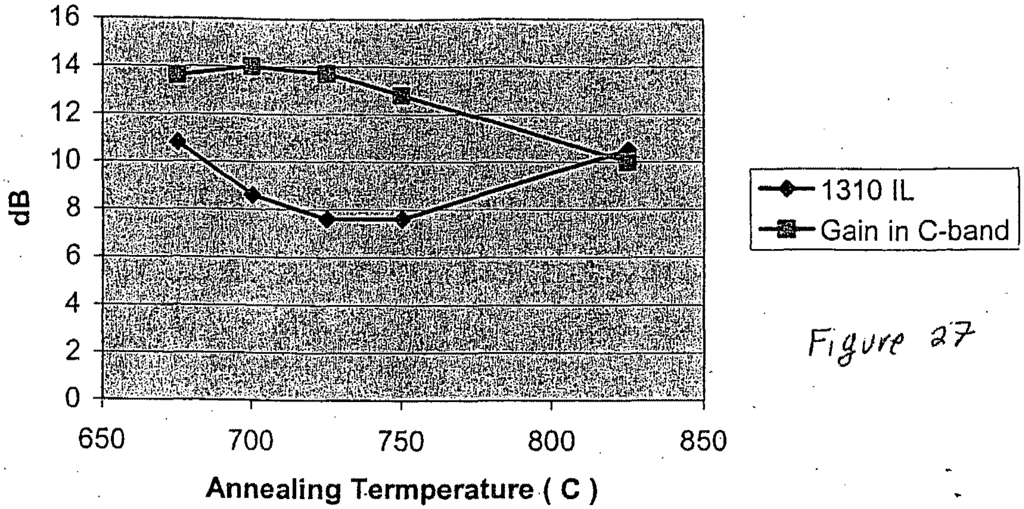
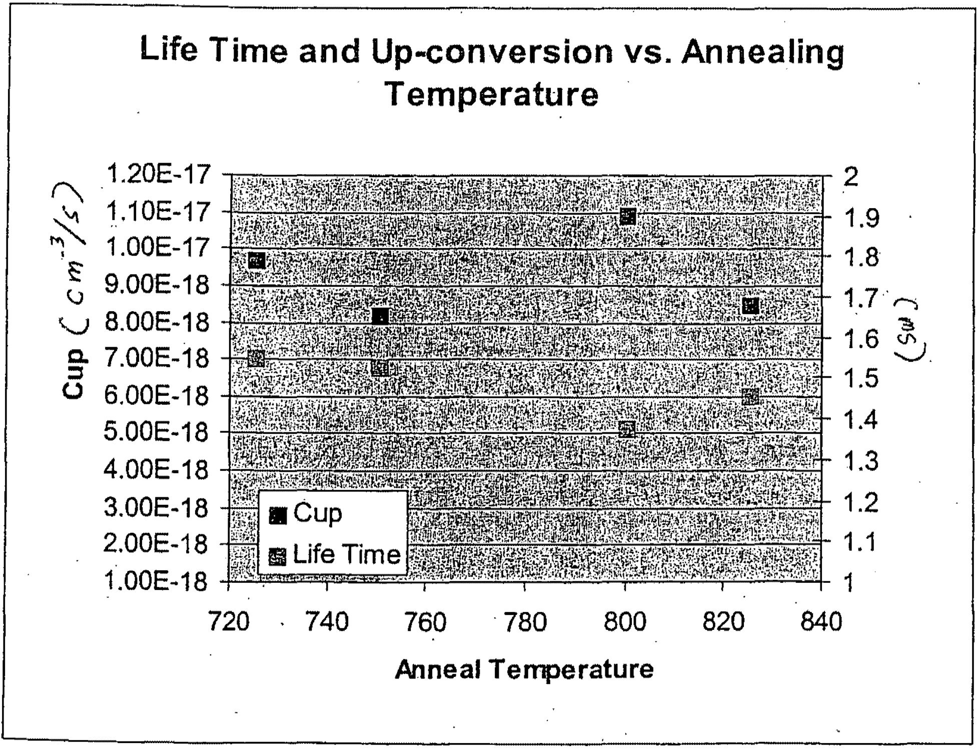


Figure 27

Figure 28



m-12245 US
25/27

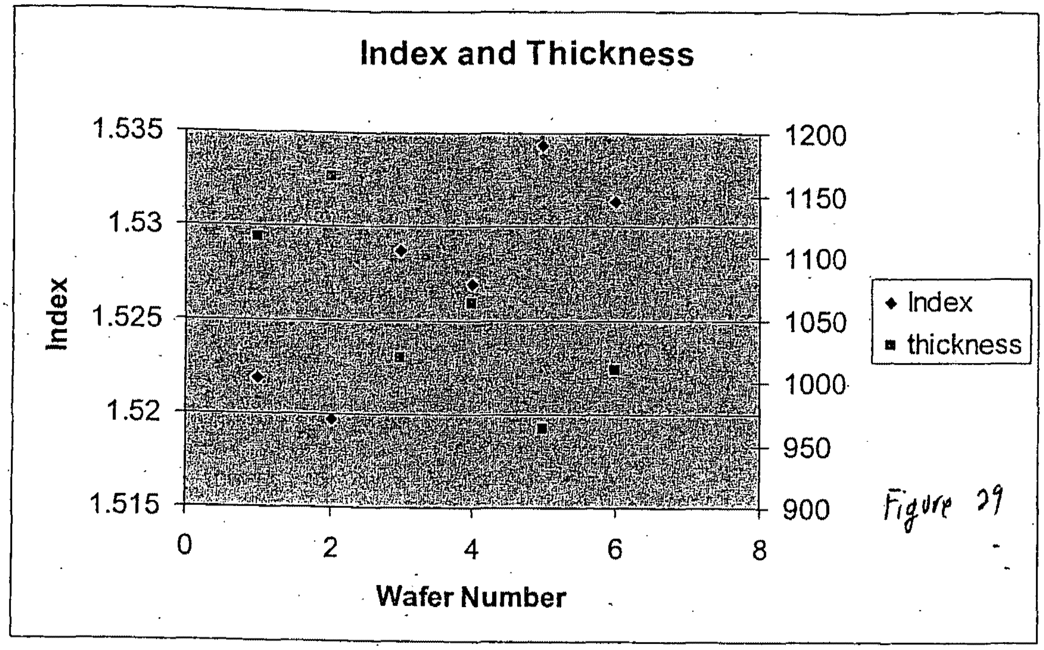


Figure 29

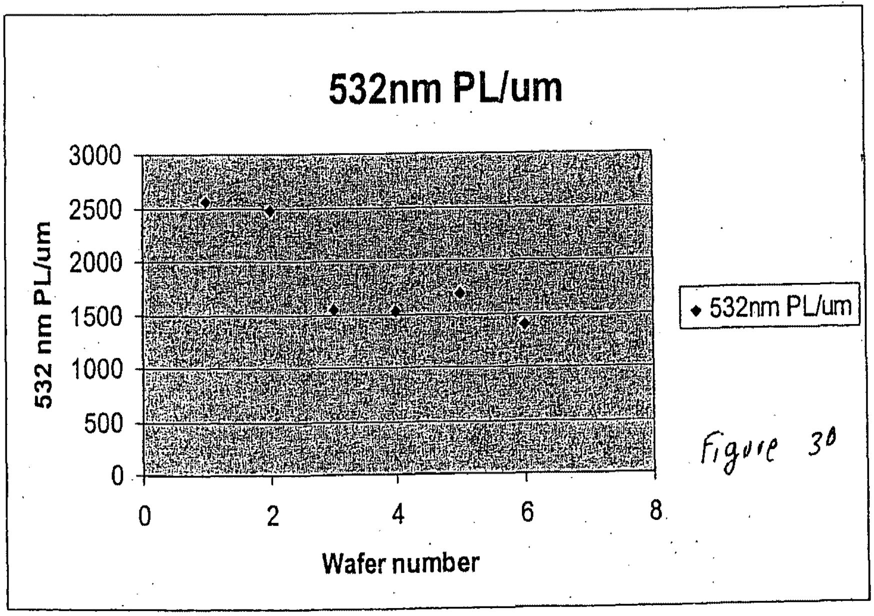


Figure 30

m- 12245 US
26/27

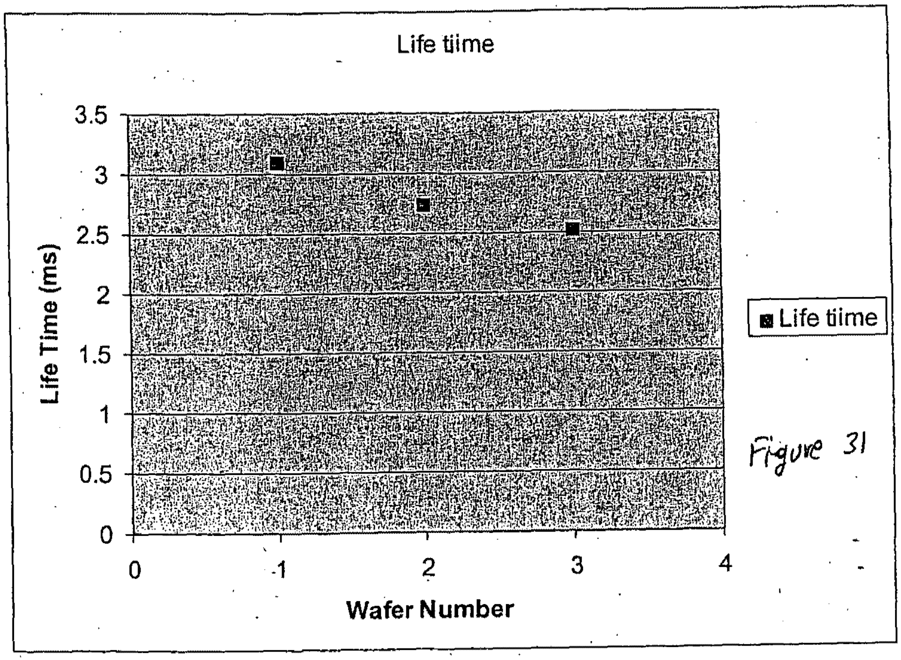


Figure 31

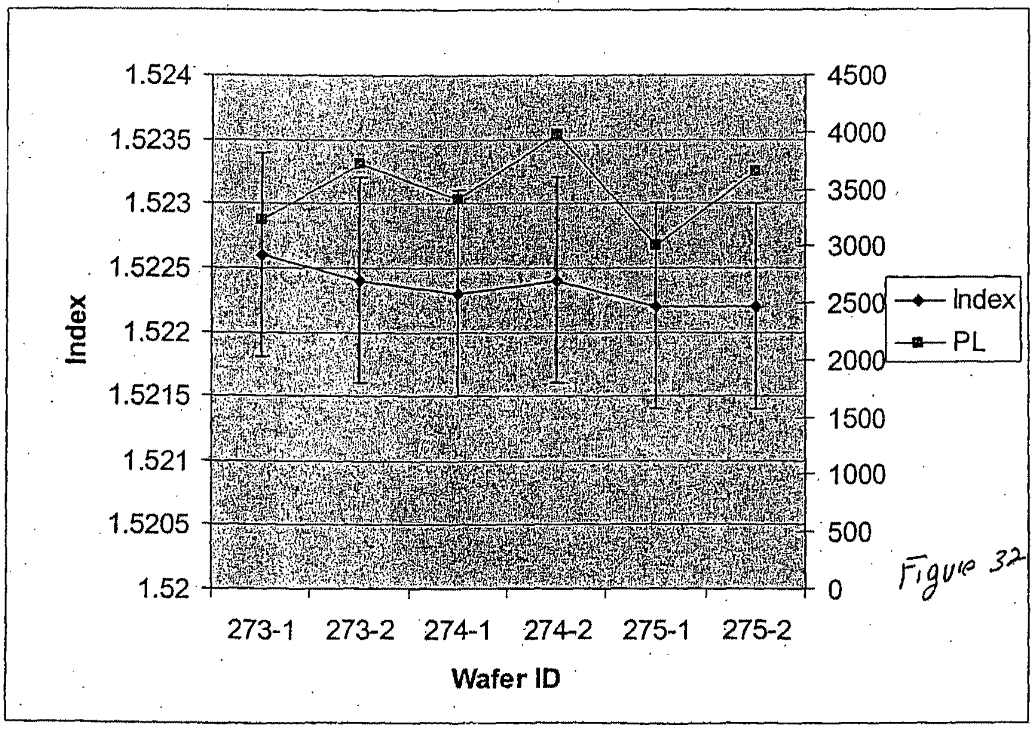


Figure 32

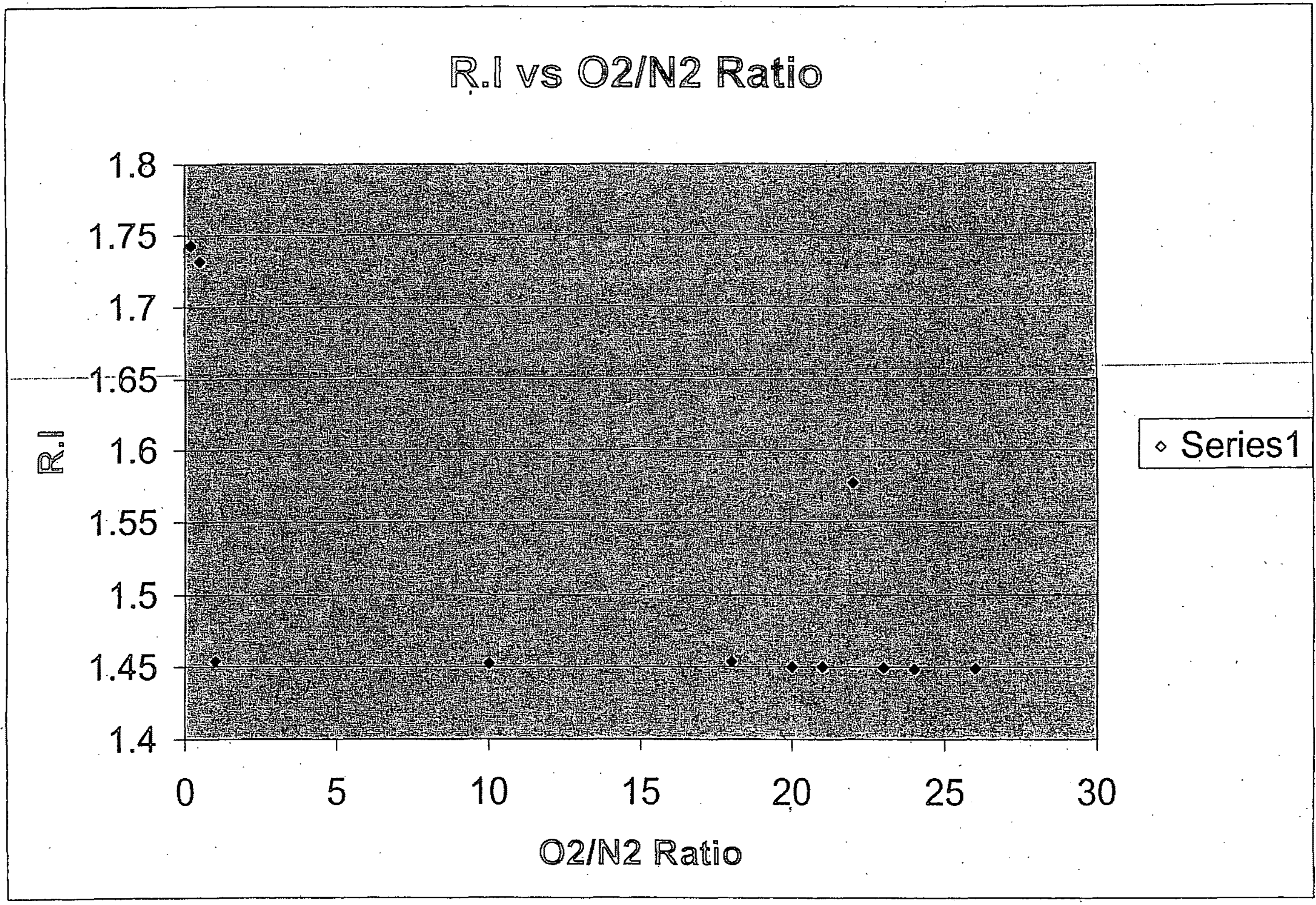


Figure 33

SU Sheet - w
27/27

Attorney Docket No.: M-12245 US

I hereby appoint the following practitioners to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith:

Customer Number 24251

Please direct all telephone calls to:

Gary J. Edwards

Telephone: 408-453-9200

I declare that all statements made herein of my own knowledge are true, all statements made herein on information and belief are believed to be true, and all statements made herein are made with the knowledge that whoever, in any matter within the jurisdiction of the Patent and Trademark Office, knowingly and willfully falsifies, conceals, or covers up by any trick, scheme, or device a material fact, or makes any false, fictitious or fraudulent statements or representations, or makes or uses any false writing or document knowing the same to contain any false, fictitious or fraudulent statement or entry, shall be subject to the penalties including fine or imprisonment or both as set forth under 18 U.S.C. 100 , and that violations of this paragraph may jeopardize the validity of the application or this document, or the validity or enforceability of any patent, trademark registration, or certificate resulting therefrom.

Full name of first joint inventor: Hongmei Zhang
Inventor's Signature: **Date:** 08/08/02
Residence: San Jose, California
Post Office Address: 1330 Rodney Drive
San Jose, California 95118
Citizenship: People of Republic China

Full name of second joint inventor: Mukundan Narasimhan
Inventor's Signature: N. M **Date:** 08/08/02
Residence: San Jose, California
Post Office Address: 293 Bluefield Drive
San Jose, California 95136
Citizenship:

Full name of third joint inventor: Ravi B. Mullapudi
Inventor's Signature: Ravi B. M **Date:** 08/08/02
Residence: San Jose, California
Post Office Address: 2117 Shiangzone Court
San Jose, California 95121
Citizenship: India

Full name of fourth joint inventor: Richard E. Demaray
Inventor's Signature: Richard E. Demaray **Date:** 8/8/02
Residence: Portola Valley, California
Post Office Address: 190 Fawn Lane
Portola Valley, California 94028
Citizenship: USA

PATENT
Customer No. 22,852
Attorney Docket No. 09140.0016
(formerly M-12245 US)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Zhang, et al.	Group Art Unit: 2816
Application No.: 10/101,863	Examiner: Unassigned
Filed: March 16, 2002	
For: BIASED PULSE DC REACTIVE SPUTTERING OF OXIDE FILMS	

Commissioner for Patents
Washington, DC 20231

Sir:

REVOCATION OF POWER OF ATTORNEY AND GRANT OF NEW POWER OF ATTORNEY

The undersigned, a representative authorized to sign on behalf of the Assignee owning all of the interest in this patent, hereby revokes all previous powers of attorney or authorization of agent granted in this application before the date of execution hereof. The undersigned verifies that Symmorphix, Inc. is the Assignee of the entire right, title, and interest in the patent application identified above by virtue of the attached assignment document, which is being concurrently filed for recordation. The undersigned certifies that the evidentiary documents have been reviewed and to the best of the undersigned's knowledge and belief, title is in the Assignee Symmorphix, Inc.

The undersigned hereby grants its power of attorney to **FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.,** Douglas B. Henderson, Reg. No. 20,291; Ford F. Farabow, Jr., Reg. No. 20,630; Arthur S. Garrett, Reg. No. 20,338; Donald R. Dunner, Reg. No. 19,073; Brian G. Brunsvold, Reg. No. 22,593; Tipton D. Jennings, IV, Reg. No. 20,645; Jerry D. Voight, Reg. No. 23,020; Laurence R. Hefter, Reg. No. 20,827; Kenneth E. Payne, Reg. No. 23,098; Herbert H. Mintz, Reg. No. 26,691; C. Larry O'Rourke, Reg. No. 26,014; Albert J. Santorelli, Reg. No. 22,610; Michael C. Elmer, Reg. No. 25,857; Richard H. Smith, Reg. No. 20,609; Stephen L. Peterson, Reg. No. 26,325; John M. Romary, Reg. No. 26,331; Bruce C. Zotter, Reg. No. 27,680; Dennis P. O'Reilley, Reg. No. 27,932; Allen M. Sokal, Reg. No. 26,695; Robert D. Bajefsky, Reg. No. 25,387; Richard L. Stroup, Reg. No. 28,478; David W. Hill, Reg. No. 28,220; Thomas L. Irving, Reg. No. 28,619; Charles E. Lipsey, Reg. No. 28,165; Thomas W. Winland, Reg. No. 27,605; Basil J. Lewris, Reg. No. 28,818; Martin I. Fuchs, Reg. No. 28,508; E. Robert Yoches, Reg. No. 30,120; Barry W. Graham, Reg. No. 29,924; Susan Haberman Griffen, Reg. No. 30,907; Richard B. Racine, Reg. No. 30,415; Thomas H. Jenkins, Reg. No. 30,857; Robert E. Converse, Jr., Reg. No. 27,432; Clair X. Mullen, Jr., Reg. No. 20,348; Christopher P. Foley, Reg. No. 31,354; Roger D. Taylor, Reg. No. 28,992; John C. Paul, Reg. No. 30,413; David M. Kelly, Reg. No. 30,953; Kenneth J. Meyers, Reg. No. 25,146; Carol P. Einaudi, Reg. No. 32,220; Walter Y. Boyd, Jr., Reg. No. 31,738; Steven M. Anzalone, Reg. No. 32,095; Jean B. Fordis, Reg. No. 32,984; Barbara C. McCurdy, Reg. No. 32,120; James K. Hammond, Reg. No. 31,964; Richard V. Burgujian, Reg. No. 31,744; J. Michael Jakes, Reg. No. 32,824; Thomas W. Banks, Reg. No. 32,719; Christopher P. Isaac, Reg. No. 32,616; Bryan C. Diner, Reg. No. 32,409; M. Paul Barker, Reg. No. 32,013; Andrew Chanho Sonu, Reg. No. 33,457; David S. Forman, Reg. No. 33,694; Vincent P. Kovalick, Reg. No. 32,867; James W.

Edmondson, Reg. No. 33,871; Michael R. McGurk, Reg. No. 32,045; Joann M. Neth, Reg. No. 36,363; Gerson S. Panitch, Reg. No. 33,751; Cheri M. Taylor, Reg. No. 33,216; Charles E. Van Horn, Reg. No. 40,266; Linda A. Wadler, Reg. No. 33,218; Jeffrey A. Berkowitz, Reg. No. 36,743; Michael R. Kelly, Reg. No. 33, 921; James B. Monroe, Reg. No. 33,971; Doris Johnson Hines, Reg. No. 34,629; Lori Ann Johnson, Reg. No. 34,498; R. Bruce Bower, Reg. No. 37,099; John Rissman, Reg. No. 33,764; Therese A. Hendricks, Reg. No. 30,389; Leslie I. Bookoff, Reg. No. 38,084; Michele C. Bosch, Reg. No. 40,524; Michael J. Flibbert, Reg. No. 33,234; Scott A. Herbst, Reg. No. 35,189; Leslie A. McDonell, Reg. No. 34,872; Thalia V. Warnement, Reg. No. 39,064; Ronald A. Bleeker, Reg. No. 27,773; Kathleen A. Daley, Reg. No. 36,116; C. Gregory Gramenopoulos, Reg. No. 36,532; Anthony M. Gutowski, Reg. No. 38,742; Yitai Hu, Reg. No. 40,653; Lionel M. Lavenue; Reg. No. 46,859; Christine E. Lehman, Reg. No. 38,535; and Gary J. Edwards, Reg. No. 41,008; both jointly and separately as their attorneys with full power of substitution and revocation to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and to receive the Letters Patent.

Please send all future correspondence concerning this application to Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P. at the following address:

Finnegan, Henderson, Farabow,
Garrett & Dunner, L.L.P.
1300 I Street, N.W.
Washington, D.C. 20005-3315

Dated: Nov 18, 2003

By: Richard E. Demaray
Name: Richard E. Demaray
Title: Chief Technical Officer
Symmorphix, Inc.

PATENT APPLICATION SERIAL NO ____________________

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

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09/21/2005 FMETEKI1 00000020 060916   11228834

01 FC:1011        300.00 DA
02 FC:1111        500.00 DA
03 FC:1311        200.00 DA
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PTO-1556
(5/87)

U.S. Government Printing Office: 2002 — [illegible]

PTO/SB/06 (12-04)
Approved for use through 7/31/2006. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875 Effective December 8, 2004

Application or Docket Number 11228834

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	150.00		N/A	300.00
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	$250		N/A	$500
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	$100		N/A	$200
TOTAL CLAIMS (37 CFR 1.16(i))	7 minus 20 =	* 0	X$ 25 =		OR	X$50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	* 0	X100 =			X200 =	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			+180=			+360=	
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1000

APPLICATION AS AMENDED – PART II

AMENDMENT A

	(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDI-TIONAL FEE ($)		RATE ($)	ADDI-TIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X$ 25 =		OR	X$50 =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X100 =		OR	X200 =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					+180=		OR	+360=	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDI-TIONAL FEE ($)		RATE ($)	ADDI-TIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X$ 25 =		OR	X$50 =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X100 =		OR	X200 =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					+180=		OR	+360=	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PATENT
Customer No. 22,852
Attorney Docket No. 9140.0016-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

ZHANG, Hongmei et al.

Application No.: Not Yet Assigned

Filed: September 16, 2005

For:

Group Art Unit: Not Yet Assigned

Examiner: Not Yet Assigned

Confirmation No.: Not Yet Assigned

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

PRELIMINARY AMENDMENT

Please amend the above-identified patent application as follows:

Amendments to the Specification are included in this paper.

Amendments to the Claims are reflected in the listing of claims in this paper.

AMENDMENTS TO THE SPECIFICATION:

Please amend this application on page 1, line 1, by inserting the following new paragraph:

This is a division of Application No. 10/101,863, filed March 16, 2002, which is incorporated herein by reference.

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

1.-14. (Canceled)

15. (Original) A reactor according to the present invention, comprising:

a target area for receiving a target;

a substrate area opposite the target area for receiving a substrate;

a pulsed DC power supply; and

a bias power supply coupled to the substrate.

16. (Original) The reactor of Claim 15, wherein the target has a surface area greater than the surface area of the substrate.

17. (Original) The reactor of Claim 15, further including a scanning magnet which provides uniform erosion of the target.

18. (Original) The reactor of Claim 17, wherein the scanning magnet scans across the target in a first direction and extends in a second direction perpendicular to the first direction.

19. Original) The reactor of Claim 18, wherein the magnet extends beyond the target in the second direction.

20.-37. (Canceled)

38. (Original) A sputtering apparatus, comprising:

means for providing pulsed DC power to a target; and

means for providing bias power to a substrate.

39. (Original) The apparatus of Claim 38, further including

means for providing process gas between the target and the substrate.

REMARKS

The application has been amended to insert the required reference to the parent applications, for which benefit is claimed, of this new divisional application.

Applicants herein choose to prosecute Group II claims, claims 15-19 and 38-39, from the Restriction Requirement mailed in the parent application on October 2, 2003. Claims 1-14 and 20-37 have been canceled. No new matter has been added.

Please grant any extensions of time required to enter this paper and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: September 16, 2005

By: Gary J. Edwards
Gary J. Edwards
Reg. No. 41,008

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER L.L.P.
901 New York Avenue, N.W.
Washington, D.C. 20001-4413
(650) 849-6622

EXPRESS MAIL LABEL NO.
EV 708643040 US

PATENT
Customer No. 22,852
Attorney Docket No. 9140.0016-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
ZHANG, Hongmei et al.	)	Group Art Unit: Not Yet Assigned
	)	
Application No.: Not Yet Assigned	)	Examiner: Not Yet Assigned
	)	
Filed: September 16, 2005	)	
	)	
For: BIASED PULSE DC REACTIVE SPUTTERING OF OXIDE FILMS	))	Confirmation No.: Not Yet Assigned

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

<u>INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)</u>

Pursuant to 37 C.F.R. §§ 1.56 and 1.97(b), applicants bring to the attention of the Examiner the documents on the attached listing. This Information Disclosure Statement is being filed within three months of the filing date of the above-referenced application.

A copy of one of the references is enclosed.

The listed documents are of record in prior application no. 10/101,863, filing date March 16, 2002, upon which applicants rely for the benefits provided in 35 U.S.C. § 120, and accordingly copies are not enclosed.

Applicants respectfully request that the Examiner consider the listed documents and indicate that they were considered by making appropriate notations on the attached form.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or

constitute "prior art." If the Examiner applies any of the documents as prior art against any claim in the application and applicants determine that the cited documents do not constitute "prior art" under United States law, applicants reserve the right to present to the office the relevant facts and law regarding the appropriate status of such documents.

Applicants further reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: September 16, 2005

By:
Gary J. Edwards
Reg. No. 41,008

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER L.L.P.
901 New York Avenue, N.W.
Washington, D.C. 20001-4413
(650) 849-6622

EXPRESS MAIL LABEL NO.
EV 708643040 US

IDS Form PTO/SB/08: Substitute for form 1449A/PTO **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** *(Use as many sheets as necessary)*				***Complete if Known***	
				Application Number	
				Filing Date	September 16, 2005
				First Named Inventor	ZHANG, Hongmei
				Art Unit	
				Examiner Name	
Sheet	1	of	14	*Attorney Docket Number*	9140.0016-02

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Issue or Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US 2005/0006768 A1	01-13-2005	Narasimhan et al.	
		US 2005/0000794 A1	01-06-2005	Demaray et al.	
		US 2004/0259305 A1	12-23-2004	Demaray et al.	
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		US 2003/0134054 A1	07-17-2003	Demaray et al.	
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		US 2003/0079838 A1	05-01-2003	Brcka	
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		US 2003/0042131 A1	03-06-2003	Johnson	
		US 2003/0022487 A1	01-30-2003	Yoon et al.	
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		US 2003/0141186 A1	07-31-2003	Wang et al.	
		US 2002/0134671 A1	09-26-2002	Demaray et al.	
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Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	
Filing Date	September 16, 2005
First Named Inventor	ZHANG, Hongmei
Art Unit	
Examiner Name	
Attorney Docket Number	9140.0016-02

Sheet 10 of 14

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		Filing Date	September 16, 2005
		First Named Inventor	ZHANG, Hongmei
		Art Unit	
(Use as many sheets as necessary)		*Examiner Name*	
Sheet 11	of 14	*Attorney Docket Number*	9140.0016-02

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Examiner Signature		Date Considered	

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IDS Form PTO/SB/08: Substitute for form 1449A/PTO		**Complete if Known**	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Application Number	
		Filing Date	September 16, 2005
		First Named Inventor	ZHANG, Hongmei
		Art Unit	
(Use as many sheets as necessary)		Examiner Name	
Sheet 12	of 14	Attorney Docket Number	9140.0016-02

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			Application Number	
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			First Named Inventor	ZHANG, Hongmei
			Art Unit	
			Examiner Name	
Sheet	13	of	14	*Attorney Docket Number*	9140.0016-02

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		Response to Office Action filed on March 3, 2004 in U.S. Serial No. 10/101,492 (Attorney Docket No. 09140-0015-00).	
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				Filing Date	September 16, 2005
				First Named Inventor	ZHANG, Hongmei
				Art Unit	
				Examiner Name	
Sheet	14	of	14	*Attorney Docket Number*	9140.0016-02

NON PATENT LITERATURE DOCUMENTS			
		Office Action issued on October 6, 2004 in U.S. Serial No. 10/101,863 (Attorney Docket No. 09140.0016-00).	
		Office Action dated January 13, 2005, received in Application No. 10/101,863 (Attorney Docket No. 09140.0016-00).	
		Response to office Action filed on June 10, 2005 in U.S. Serial No. 10/101,863 (Attorney Docket No. 09140.0016-00).	
		Office Action issued on August 4, 2005, in U.S. Serial No. 10/101,863 (Attorney Docket No. 09140.0016-00).	
		Office Action dated March 25, 2005, received in Application No. 10/954,182 (Attorney Docket No. 09140.0016-01).	
		Office Action issued on October 22, 2003 in U.S. Serial No. 10/101,341 (Attorney Docket No. 09140-0017-00).	
		Response to Office Action filed on February 23, 2004 in U.S. Serial No. 10/101,341 (Attorney Docket No. 09140-0017-00).	
		Office Action issued on June 10, 2004 in U.S. Serial No. 10/101,341 (Attorney Docket No. 09140-0017-00).	
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number 11/228,834

CLAIMS AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY			OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE	FEE	OR	RATE	FEE
BASIC FEE (37 CFR 1.16(a))				$	OR		$
TOTAL CLAIMS (37 CFR 1.16(c))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(b))	minus 3 =	*	X $ =		OR	X $ =	
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(d))			+ $ =		OR	+ $ =	
			TOTAL		OR	TOTAL	

* If the difference in column 1 is less than zero, enter "0" in column 2.

CLAIMS AS AMENDED – PART II

9/16/05

AMENDMENT A	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	ADDITIONAL FEE
Total (37 CFR 1.16(c))	* 3	Minus	** 20	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(b))	* 2	Minus	*** 3	=	X $ =		OR	X $ =	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))					+ $ =		OR	+ $ =	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

15, 38,

AMENDMENT B	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	ADDITIONAL FEE
Total (37 CFR 1.16(c))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(b))	*	Minus	***	=	X $ =		OR	X $ =	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))					+ $ =		OR	+ $ =	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT C	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	ADDITIONAL FEE
Total (37 CFR 1.16(c))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(b))	*	Minus	***	=	X $ =		OR	X $ =	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))					+ $ =		OR	+ $ =	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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PATENT
Customer No. 22,852
Attorney Docket No. 9140.0016-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

ZHANG, Hongmei et al.

Application No.: 11/228,834

Filed: September 16, 2005

For: BIASED PULSE DC REACTIVE SPUTTERING OF OXIDE FILMS

Group Art Unit: Not Yet Assigned

Examiner: Not Yet Assigned

Confirmation No.: Not Yet Assigned

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§ 1.56 and 1.97(b), Applicants bring to the attention of the Examiner the documents on the attached listing. This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits for the above-referenced application. Applicants respectfully request that the Examiner consider the listed documents and indicate that they were considered by making appropriate notations on the attached form.

Copies of the listed non-patent literature documents are attached.

Applicants respectfully request that the Examiner consider the listed documents and indicate that they were considered by making appropriate notations on the attached form.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or

constitute "prior art." If the Examiner applies any of the documents as prior art against any claims in the application and Applicants determine that the cited documents do not constitute "prior art" under United States law, Applicants reserve the right to present to the office the relevant facts and law regarding the appropriate status of such documents.

Applicants further reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: September 30, 2005

By: Gary J. Edwards
Gary J. Edwards
Reg. No. 41,008

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT			*Application Number*	11/228,834
			Filing Date	September 16, 2005
			First Named Inventor	ZHANG, Hongmei
			Art Unit	Not Yet Assigned
(Use as many sheets as necessary)			*Examiner Name*	Not Yet Assigned
Sheet	1	of 1	*Attorney Docket Number*	9140.0016-02

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Issue or Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		5,478,456	12-26-1995	Humpal et al.	
		6,846,765 B2	01-25-2005	Imamura et al.	

Note: Submission of copies of U.S. Patents and published U.S. Patent Applications is not required.

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	Translation[6]

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation[6]
		DOREY, R.A., "Low temperature micromoulding of functional ceramic devices," Grant summary for GR/S84156/01 for the UK Engineering and Physical Sciences Research Council, 2 pages (2004).	
		HOWSON, R.P., "The reactive sputtering of oxides and nitrides," *Pure & Appl. Chem. 66*(6):1311-1318 (1994).	
		Office Action issued on August 4, 2005, in U.S. Serial No. 10/101,863 (Attorney Docket No. 09140-0016-00).	
		Office Action issued on August 8, 2005 in U.S. Serial No. 10/101,341 (Attorney Docket No. 09140-0017-00).	

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Examiner Signature		Date Considered	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
11/228,834	09/16/2005	Hongmei Zhang	9140.0016-02

CONFIRMATION NO. 9006

FORMALITIES LETTER

22852
FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413

Date Mailed: 10/11/2005

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Filing Date Granted

An application number and filing date have been accorded to this application. The application is informal since it does not comply with the regulations for the reason(s) indicated below. Applicant is given TWO MONTHS from the date of this Notice within which to correct the informalities indicated below. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

The required item(s) identified below must be timely submitted to avoid abandonment:

- Replacement drawings in compliance with 37 CFR 1.84 and 37 CFR 1.121(d) are required. The drawings submitted are not acceptable because:
    - The drawings must be reasonably free from erasures and must be free from alterations, overwriting, interlineations, folds, and copy marks. See Figure(s) 7, 8, 14, 15, 17, & 33.

Applicant is cautioned that correction of the above items may cause the specification and drawings page count to exceed 100 pages. If the specification and drawings exceed 100 pages, applicant will need to submit the required application size fee.

Items Required To Avoid Processing Delays:

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

- A new oath or declaration, identifying this application number is required. The oath or declaration does not comply with 37 CFR 1.63 in that it:
- does not state whether the inventor is a sole or joint inventor.
- does not state that the person making the oath or declaration has reviewed and understands the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration.

Replies should be mailed to: Mail Stop Missing Parts

Commissioner for Patents
P.O. Box 1450
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A copy of this notice <u>MUST</u> be returned with the reply.

Office of Initial Patent Examination (571) 272-4000, or 1-800-PTO-9199, or 1-800-972-6382
PART 3 - OFFICE COPY

OIPE IAP58
NOV 28 2005
PATENT & TRADEMARK OFFICE

11-30-05

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APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
11/228,834	09/16/2005	Hongmei Zhang	9140.0016-02

CONFIRMATION NO. 9006

FORMALITIES LETTER

22852
FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413

Date Mailed: 10/11/2005

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- does not state whether the inventor is a sole or joint inventor.
- does not state that the person making the oath or declaration has reviewed and understands the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration.

Replies should be mailed to: Mail Stop Missing Parts

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PART 2 - COPY TO BE RETURNED WITH RESPONSE

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IAP58
NOV 28 2005
PATENT & TRADEMARK OFFICE

PATENT
Customer No. 22,852
Attorney Docket No. 9140.0016-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
)
ZHANG, Hongmei et al.) Group Art Unit: 1753
)
Application No.: 11/228,834) Examiner: Not Yet Assigned
)
Filed: September 16, 2005)
) Confirmation No.: 9006
For: BIASED PULSE DC REACTIVE)
SPUTTERING OF OXIDE FILMS)

MAIL STOP MISSING PARTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

RESPONSE TO NOTICE TO FILE CORRECTED APPLICATION PAPERS

In response to the communication of October 11, 2005, Applicants submit twenty-seven (27) sheets of replacement drawings (Figs. 1A-1B, 2-15, 16A-16D, and 17-33), copy of the Declaration and Power of Attorney from corresponding U.S. Patent Application No. 10/101,863, and a copy of the Notice of To File Corrected Application Papers.

Please grant any extensions of time required to enter this response, and charge any required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: November 28, 2005

By: Gary J. Edwards
Gary J. Edwards
Reg. No. 41,008

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EV 678997735 US

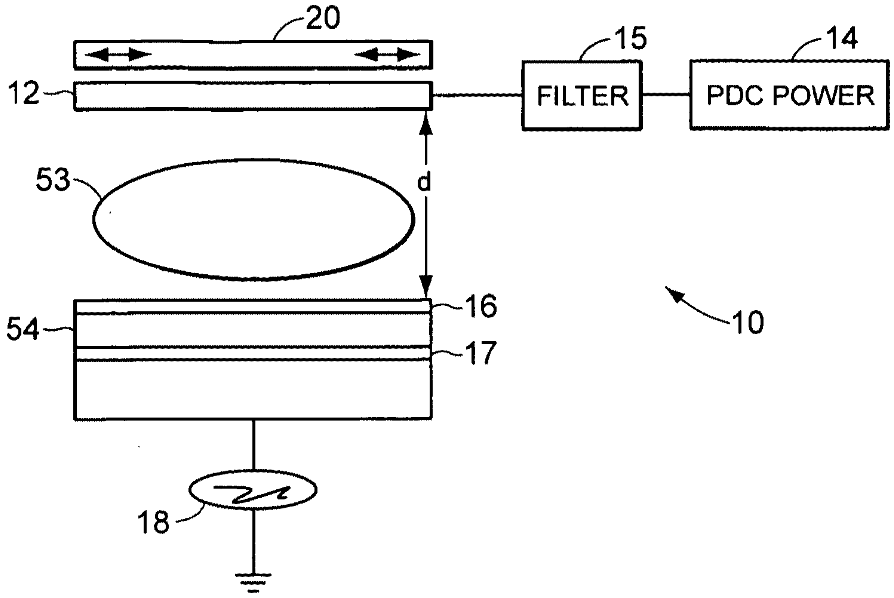
20
15
FILTER
14
PDC POWER
12
53
d
16
54
10
17
18

FIG. 1A

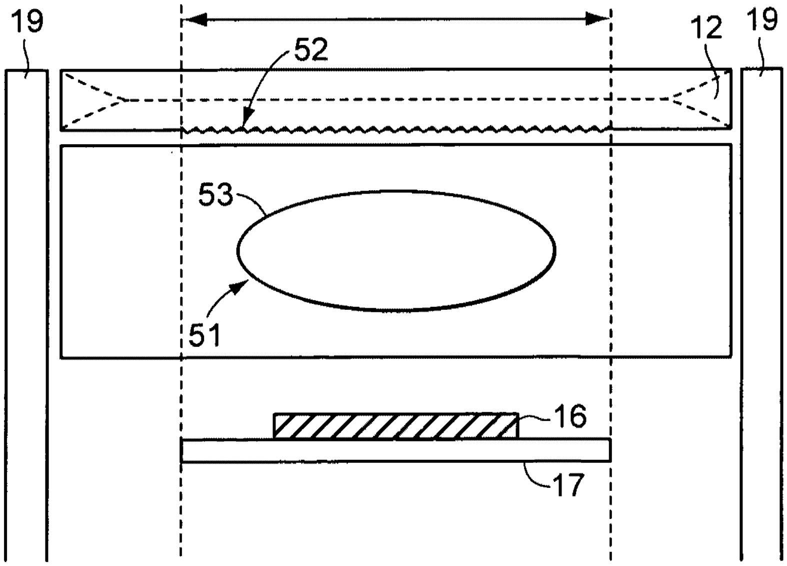
19
12
19
52
53
51
16
17

FIG. 1B

REPLACEMENT SHEET
Inventors: Hongmei ZHANG et al.
Application No. 11/228,834
Title: BIASED PULSE DC REACTIVE
SPUTTERING OF OXIDE FILMS

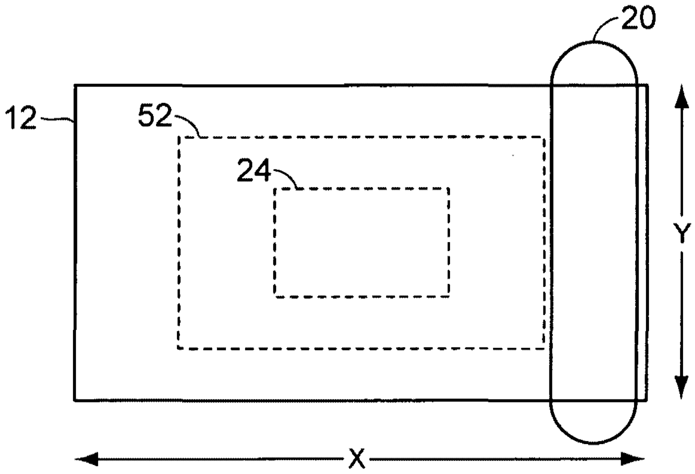

FIG. 2

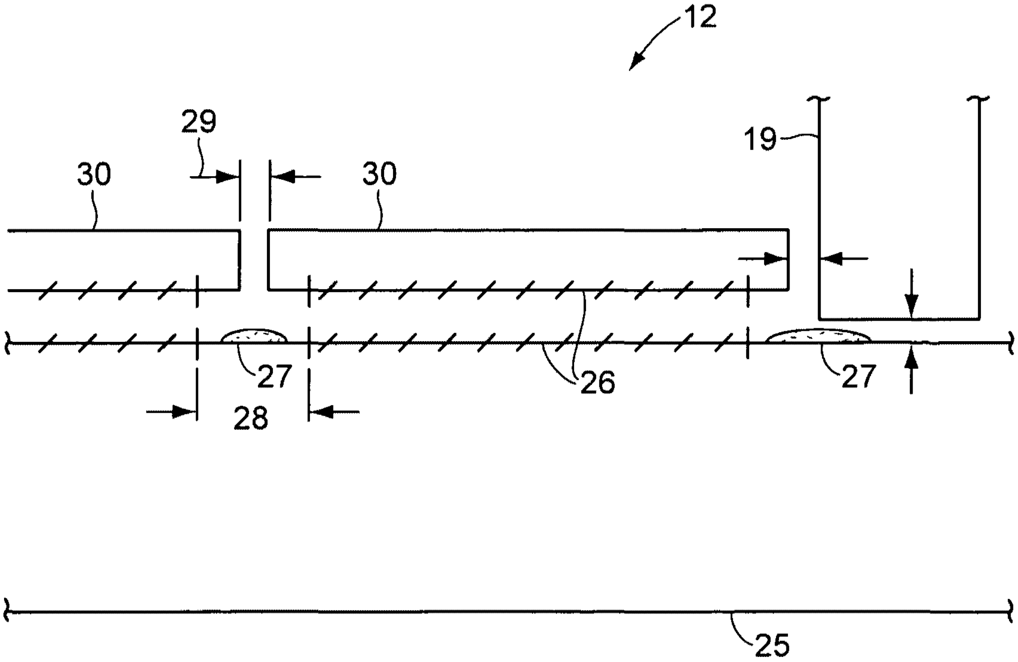

FIG. 3

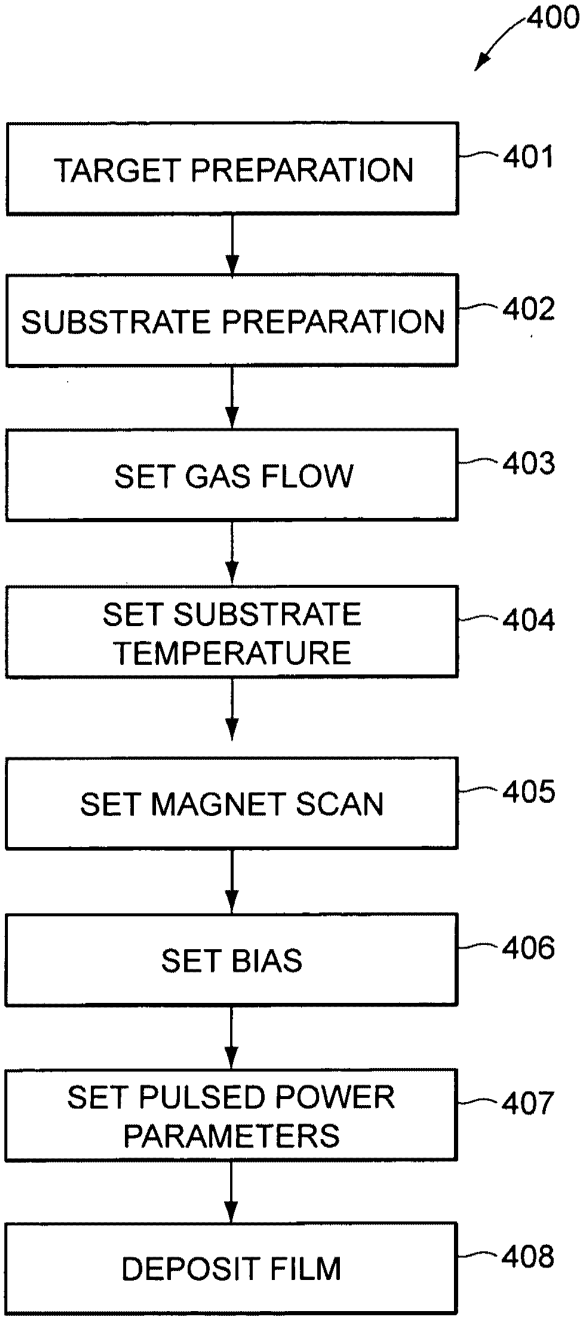
400
TARGET PREPARATION
401
SUBSTRATE PREPARATION
402
SET GAS FLOW
403
SET SUBSTRATE TEMPERATURE
404
SET MAGNET SCAN
405
SET BIAS
406
SET PULSED POWER PARAMETERS
407
DEPOSIT FILM
408

FIG. 4

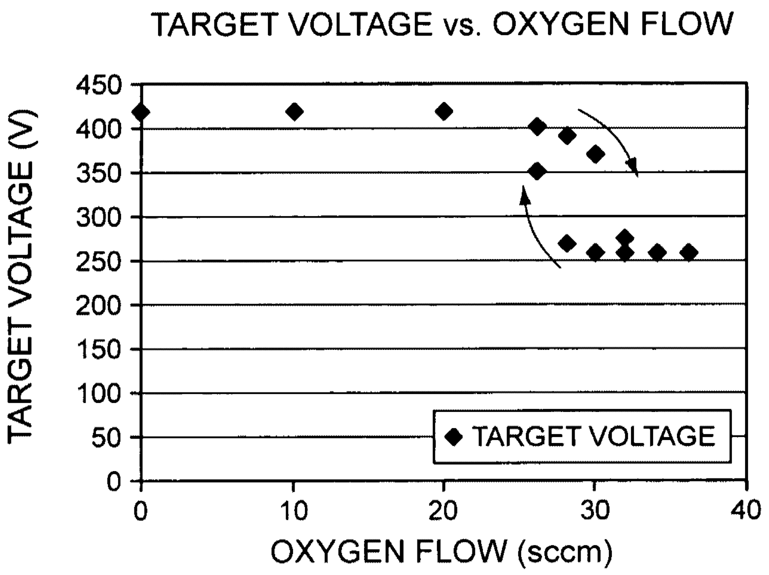
TARGET VOLTAGE vs. OXYGEN FLOW
TARGET VOLTAGE (V)
450
400
350
300
250
200
150
100
50
0
0
10
20
30
40
OXYGEN FLOW (sccm)
◆ TARGET VOLTAGE

FIG. 5

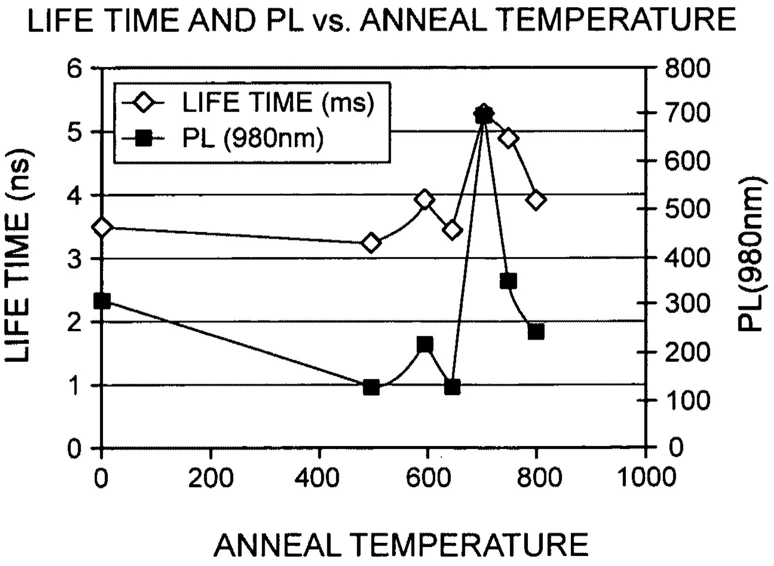
LIFE TIME AND PL vs. ANNEAL TEMPERATURE
LIFE TIME (ns)
6
5
4
3
2
1
0
PL(980nm)
800
700
600
500
400
300
200
100
0
0
200
400
600
800
1000
ANNEAL TEMPERATURE
◇ LIFE TIME (ms)
■ PL (980nm)

FIG. 6

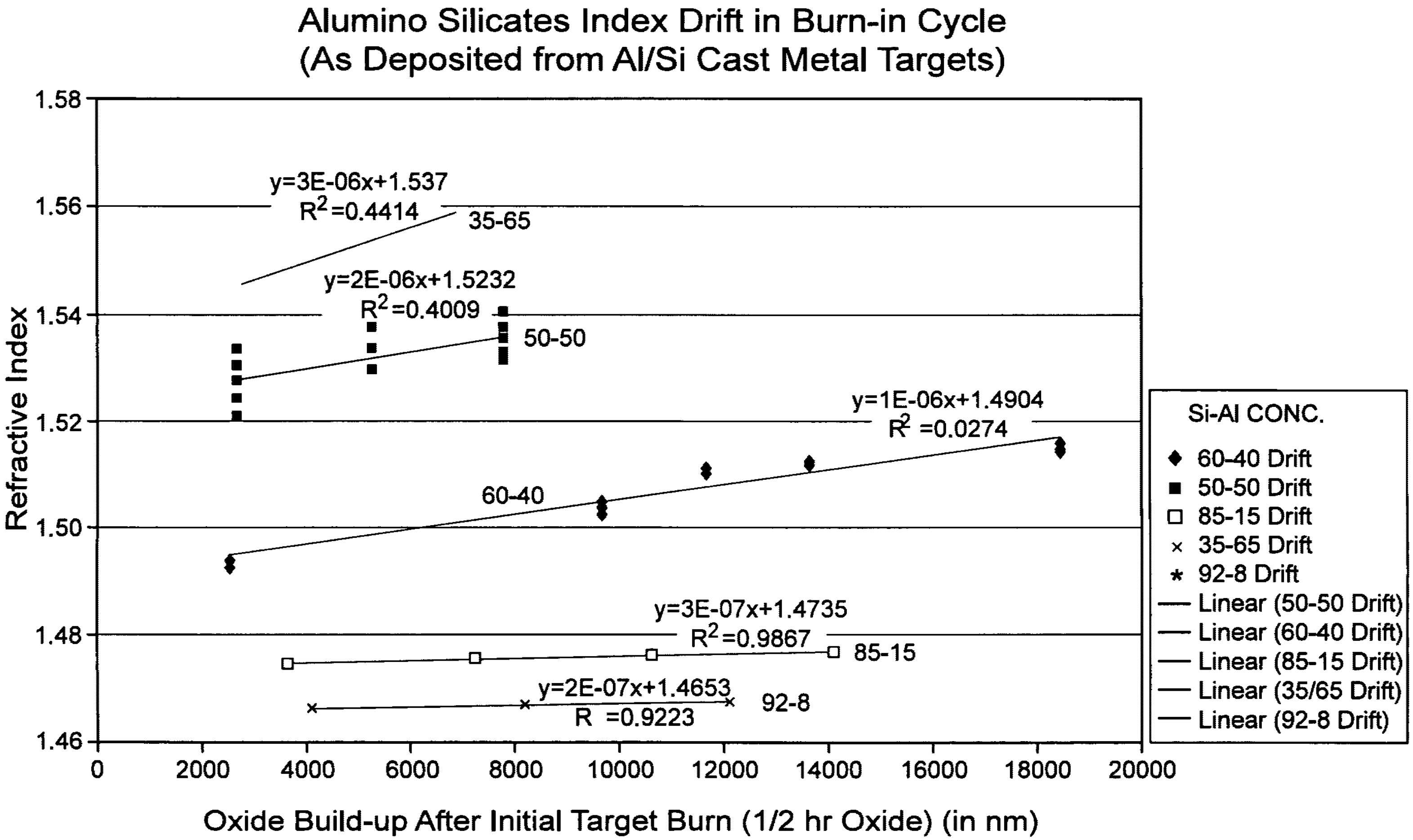
Alumino Silicates Index Drift in Burn-in Cycle
(As Deposited from Al/Si Cast Metal Targets)
Refractive Index
1.58
1.56
1.54
1.52
1.50
1.48
1.46
0
2000
4000
6000
8000
10000
12000
14000
16000
18000
20000
Oxide Build-up After Initial Target Burn (1/2 hr Oxide) (in nm)
y=3E-06x+1.537
R2=0.4414
35-65
y=2E-06x+1.5232
R2=0.4009
50-50
y=1E-06x+1.4904
R2 =0.0274
60-40
y=3E-07x+1.4735
R2=0.9867
85-15
y=2E-07x+1.4653
R =0.9223
92-8
Si-Al CONC.
◆ 60-40 Drift
■ 50-50 Drift
□ 85-15 Drift
× 35-65 Drift
* 92-8 Drift
— Linear (50-50 Drift)
— Linear (60-40 Drift)
— Linear (85-15 Drift)
— Linear (35/65 Drift)
— Linear (92-8 Drift)

FIG. 7

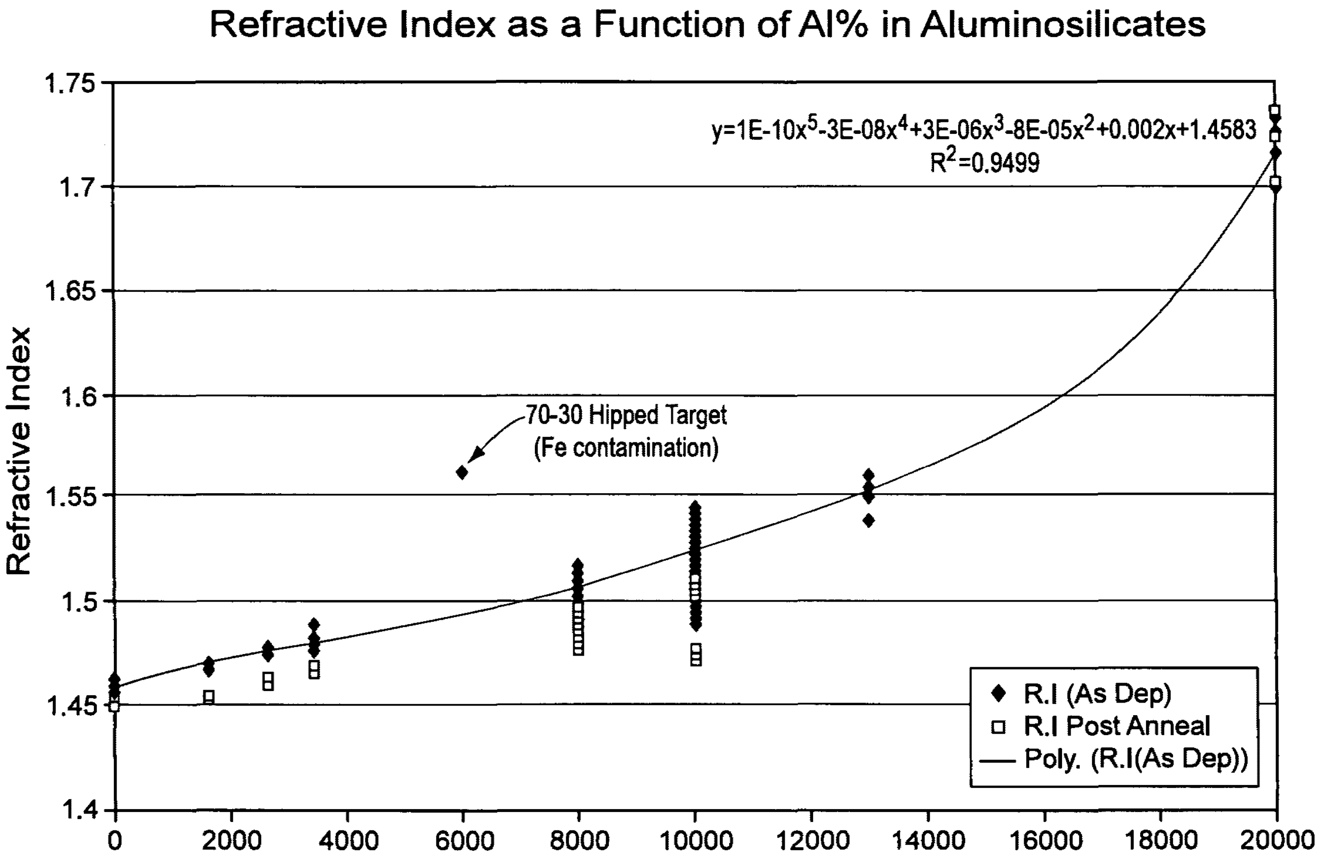
Refractive Index as a Function of Al% in Aluminosilicates
Refractive Index
1.75
1.7
1.65
1.6
1.55
1.5
1.45
1.4
0
2000
4000
6000
8000
10000
12000
14000
16000
18000
20000
y=1E-10x^5-3E-08x^4+3E-06x^3-8E-05x^2+0.002x+1.4583
R^2=0.9499
70-30 Hipped Target
(Fe contamination)
◆ R.I (As Dep)
□ R.I Post Anneal
— Poly. (R.I(As Dep))

FIG. 8

Material (Er/Yb/Al/Si)	Expected index (Post anneal)	Actual index (Post anneal)	Process Conditions (Annealed 725c 30min)
0.8/0.8/41.4/57	1.506	1.510	6KW, Ar-60,02-28sccm, 120Khz, 2.2us, 60mm T-W Space, 4-5mm T-M Space, 0-400W Bias
1.6/0.5/49/48.9	1.526	1.528	6KW, Ar-60,02-28sccm, 120Khz, 2.2us, 60mm T-W Space, 4-5mm T-M Space, 0-400W Bias
0/0/8/92	1.452	1.456-1.459	4.5KW, Ar-30-60,02-28-44, 120-200Khz, 2.2us, 60-85mm T-W Space, 4-5mm T-M Space, 0-400W Bias
0/0/40/60	1.504	1.486-1.501	3.0-4.5KW, Ar-30,02-44, 75-200Khz, 2.2-3.0us, 60-85mm T-W Space, 4-5mm T-M Space, 0-400W Bias
0/0/50/50	1.520	1.491-1.503	4.0-5KW, Ar-30,02-44, 75-200Khz, 2.2-3.0us, 60-85mm T-W Space, 4-5mm T-M Space, 0-400W Bias
0/0/65/35	1.544	1.545-1.560	4.5-5.5KW, Ar-75-90,0285-100, 200Khz, 2.2us, 85mm T-W Space, 4-5mm T-M Space, 0-400W Bias
0/0/30/70	1.490	1.562 (high Fe content)	5.0KW, Ar-75,02-100, 200Khz, 2.2us, 85mm T-W Space, 4-5mm T-M Space, 0-400W Bias
1.5/0/48.5/50	1.523	1.509-1.513	6KW, Ar-60,02-28sccm, 120Khz, 2.2us, 60mm T-W Space, 4-5mm T-M Space, 0-400W Bias

FIG. 9

Bias Power (Watts)	DC Power (KW)	Pulsing Freq (KHz)	Reverse Time (µs)	Ar Flow (sccms)	O2 Flow (sccms)	Wafer Position	Target To Wafer Spacing (mm)	Refractive Index Avg (@1550nm)	Refractive Index STD (@1550nm)	Dep Rate (um/Hr)
150	4.5	200	2.2	100	100	1	55	1.461508	0.000535	0.957654
150	4.5	200	2.2	100	100	2	55	1.462329	0.000376	0.962581
400	4.5	200	2.2	100	100	1	55	1.462774	0.000103	0.814007
400	4.5	200	2.2	100	100	2	55	1.463583	0.000095	0.824566

FIG. 10

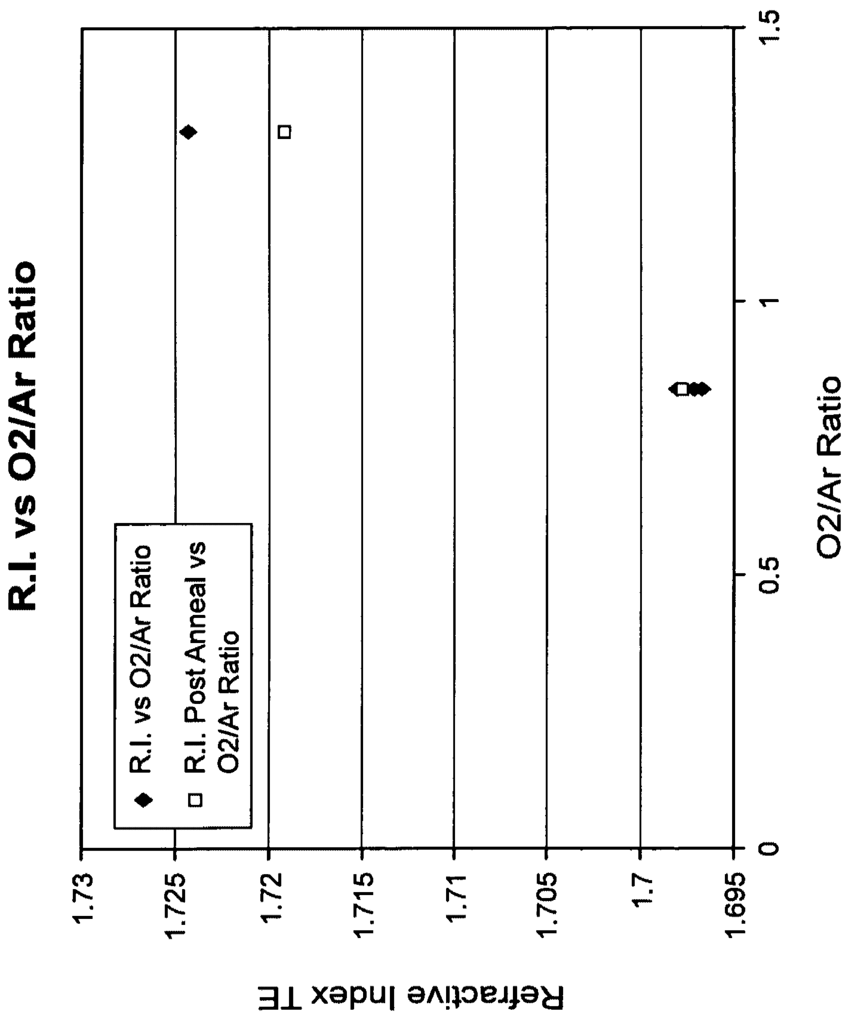
R.I. vs O2/Ar Ratio
◆ R.I. vs O2/Ar Ratio
□ R.I. Post Anneal vs O2/Ar Ratio
Refractive Index TE
1.73
1.725
1.72
1.715
1.71
1.705
1.7
1.695
0
0.5
1
1.5
O2/Ar Ratio

FIG. 11

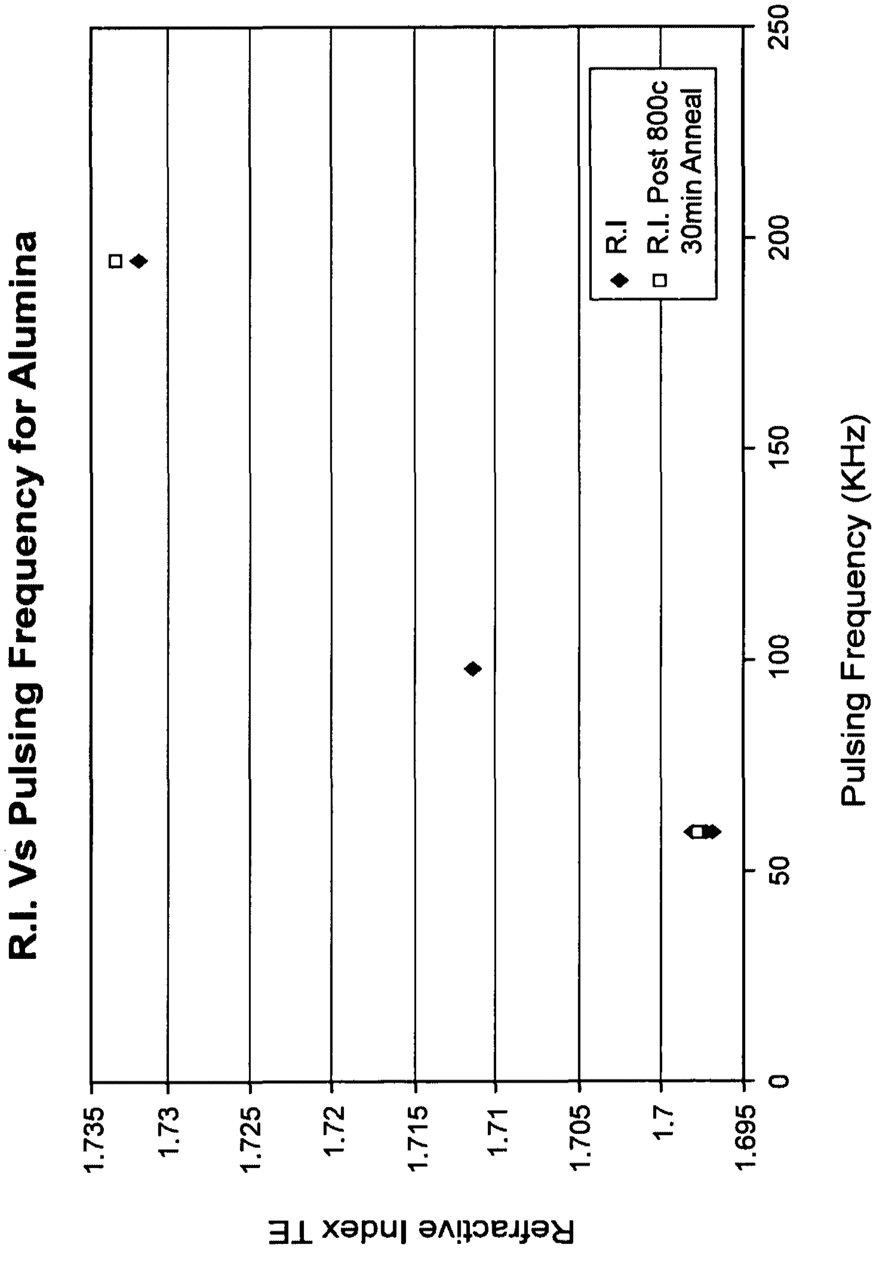
R.I. Vs Pulsing Frequency for Alumina
Refractive Index TE
1.735
1.73
1.725
1.72
1.715
1.71
1.705
1.7
1.695
0
50
100
150
200
250
Pulsing Frequency (KHz)
◆ R.I
□ R.I. Post 800c 30min Anneal

FIG. 12

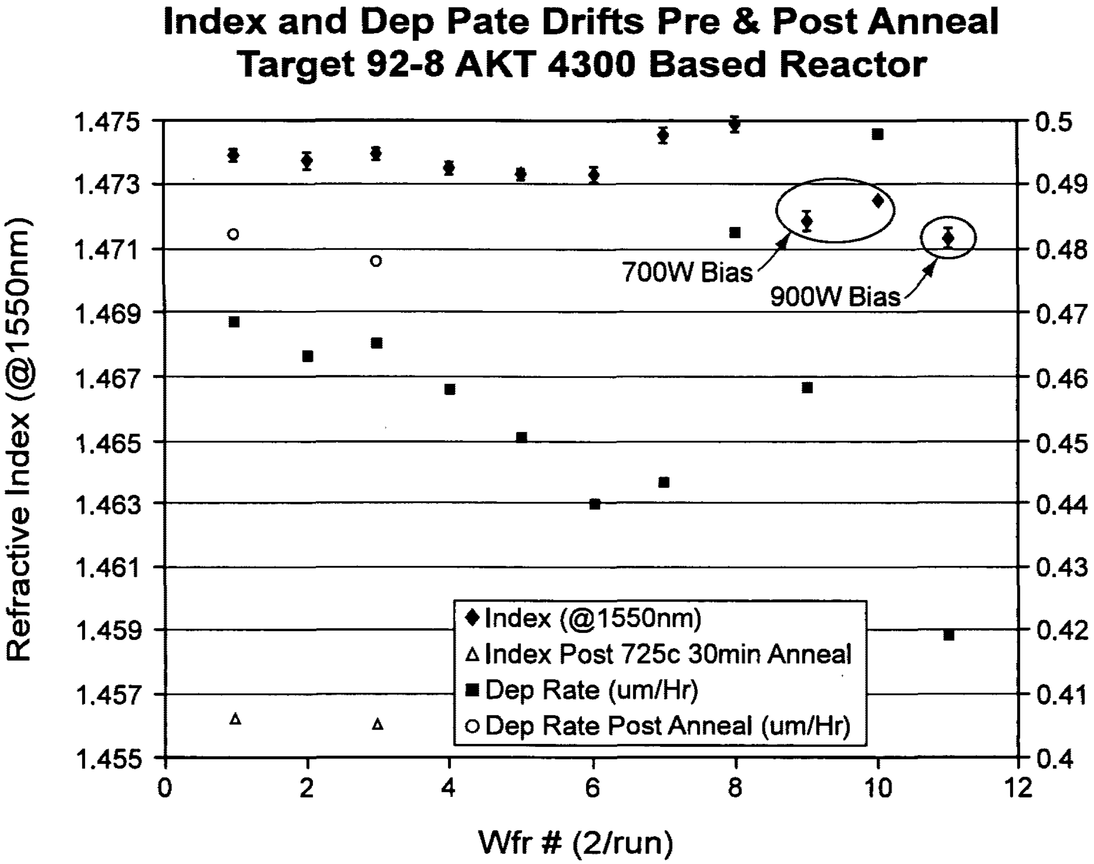
Index and Dep Pate Drifts Pre & Post Anneal
Target 92-8 AKT 4300 Based Reactor
Refractive Index (@1550nm)
1.475
1.473
1.471
1.469
1.467
1.465
1.463
1.461
1.459
1.457
1.455
0.5
0.49
0.48
0.47
0.46
0.45
0.44
0.43
0.42
0.41
0.4
0
2
4
6
8
10
12
Wfr # (2/run)
700W Bias
900W Bias
◆ Index (@1550nm)
△ Index Post 725c 30min Anneal
■ Dep Rate (um/Hr)
○ Dep Rate Post Anneal (um/Hr)

FIG. 13

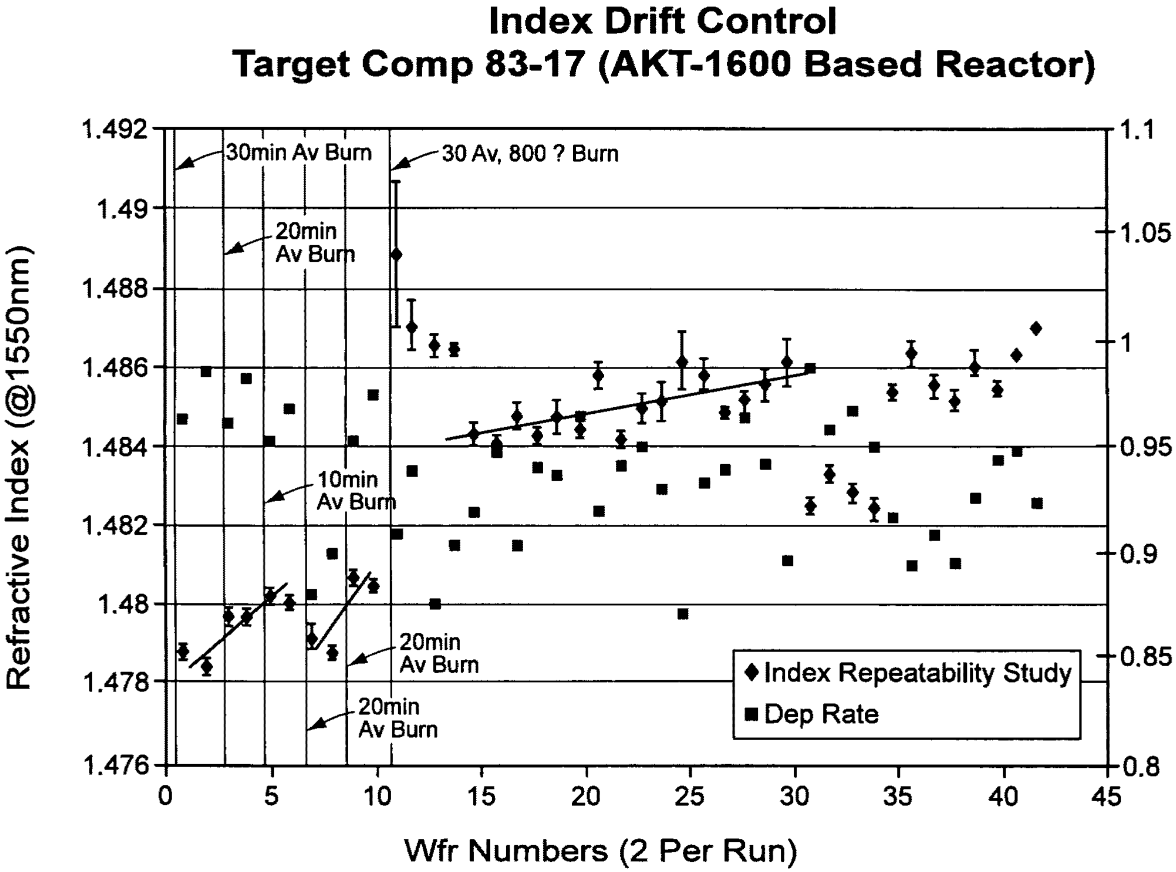
Index Drift Control
Target Comp 83-17 (AKT-1600 Based Reactor)
Refractive Index (@1550nm)
1.492
1.49
1.488
1.486
1.484
1.482
1.48
1.478
1.476
1.1
1.05
1
0.95
0.9
0.85
0.8
0
5
10
15
20
25
30
35
40
45
Wfr Numbers (2 Per Run)
30min Av Burn
30 Av, 800 ? Burn
20min Av Burn
10min Av Burn
20min Av Burn
20min Av Burn
♦ Index Repeatability Study
■ Dep Rate

FIG. 14

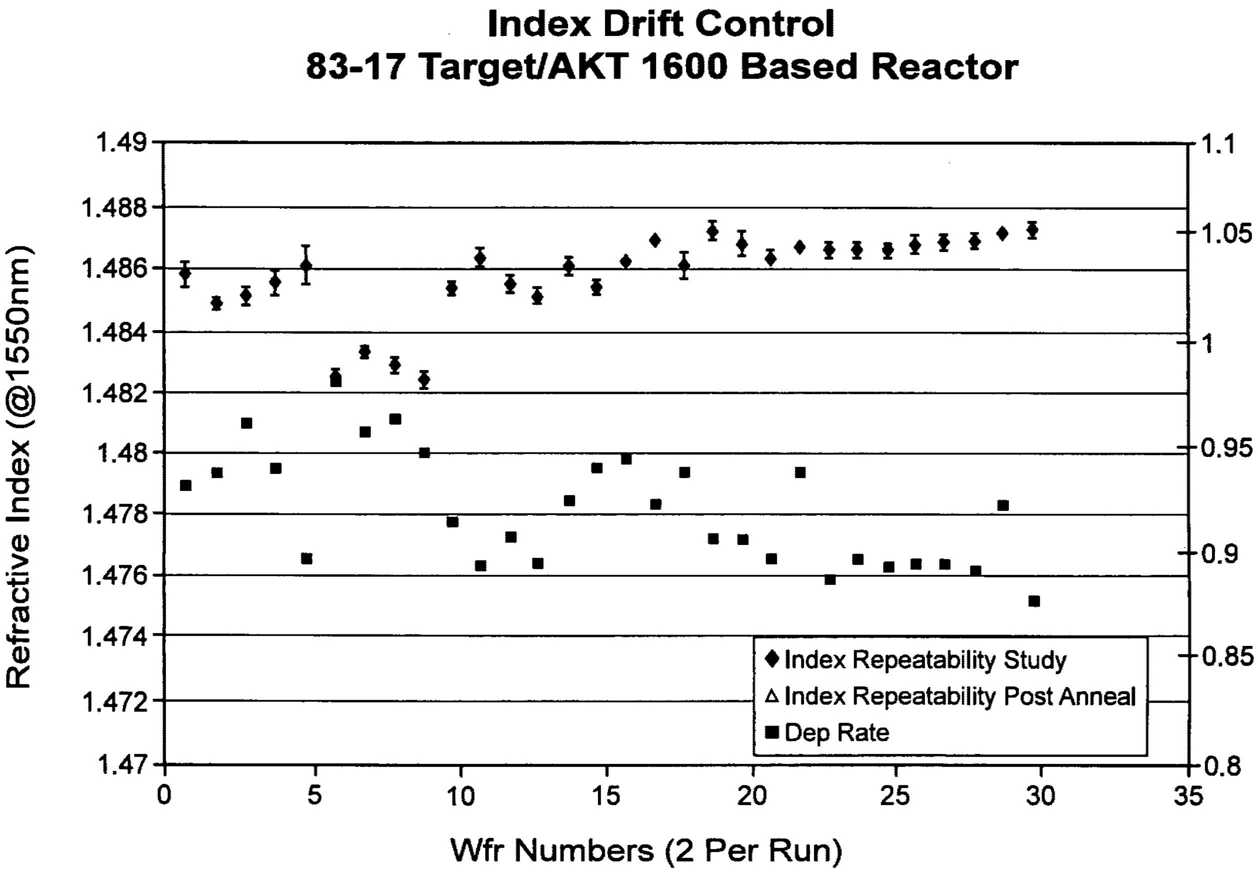
Index Drift Control
83-17 Target/AKT 1600 Based Reactor
Refractive Index (@1550nm)
1.49
1.488
1.486
1.484
1.482
1.48
1.478
1.476
1.474
1.472
1.47
1.1
1.05
1
0.95
0.9
0.85
0.8
0
5
10
15
20
25
30
35
Wfr Numbers (2 Per Run)
♦ Index Repeatability Study
△ Index Repeatability Post Anneal
■ Dep Rate

FIG. 15

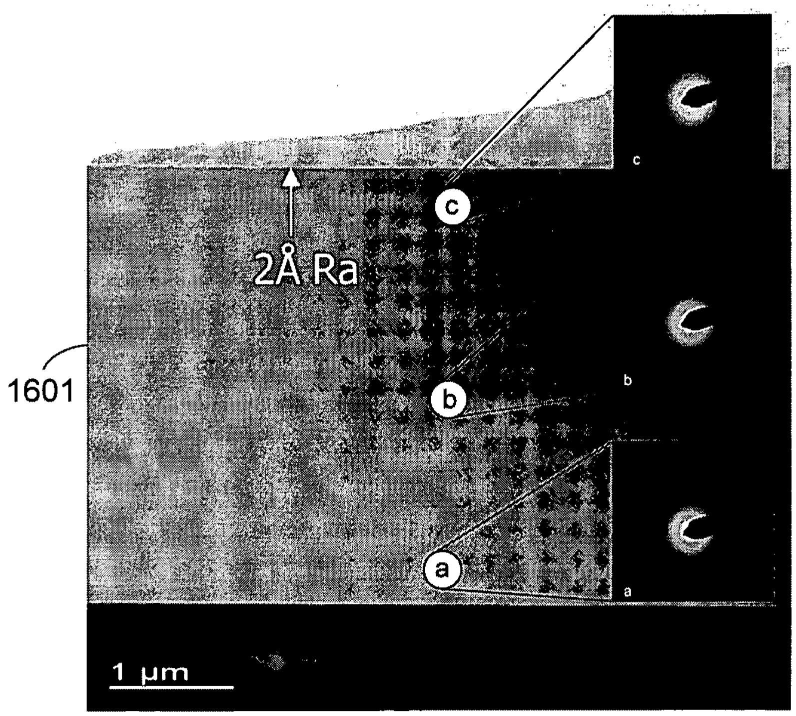

FIG. 16D

FIG. 16C

FIG. 16B

FIG. 16A

SYMMORPHIX PVD ALUMINOSILICATE

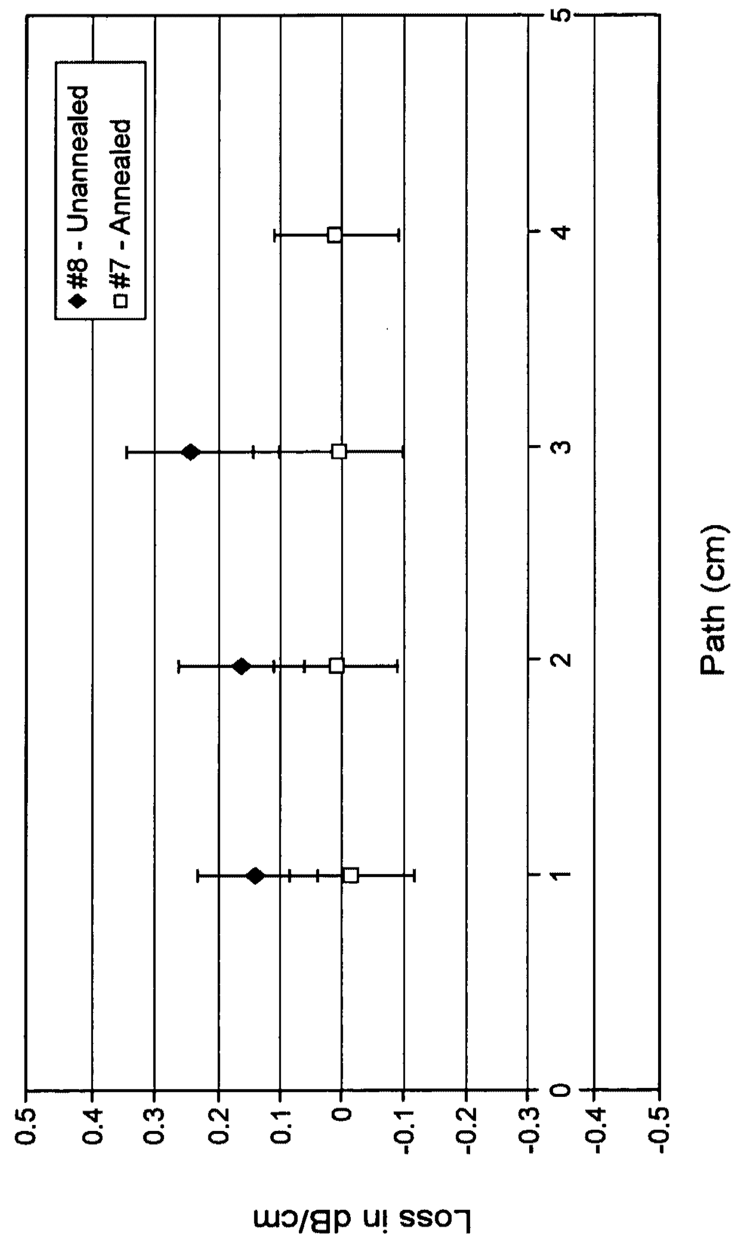
◆ #8 - Unannealed
□ #7 - Annealed
Loss in dB/cm
0.5
0.4
0.3
0.2
0.1
0
-0.1
-0.2
-0.3
-0.4
-0.5
Path (cm)
0
1
2
3
4
5

FIG. 17

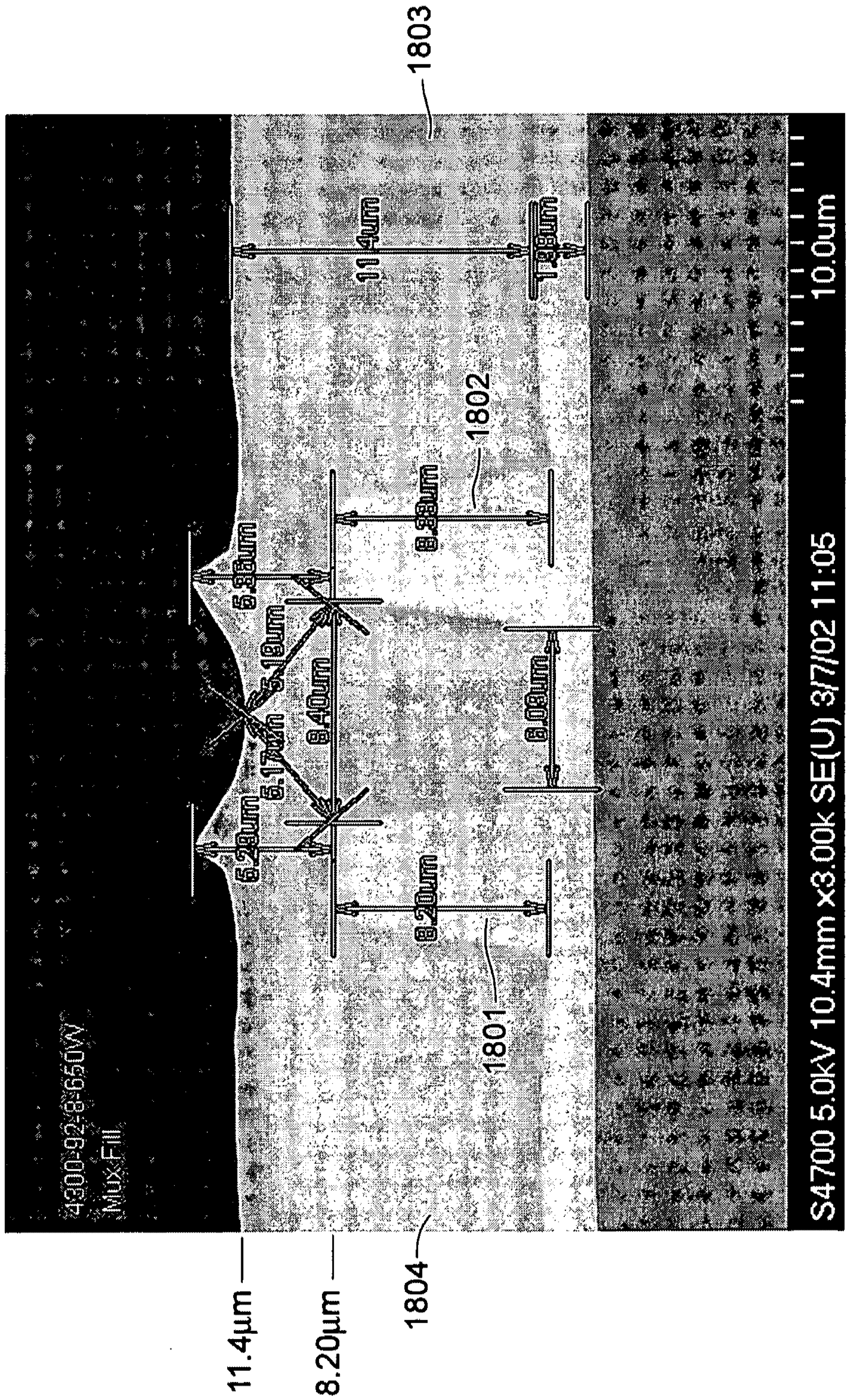
1803
4300-92-8-650W
Mux Fill
11.4um
1.98um
8.33um
1802
5.36um
5.18um
8.40um
8.03um
5.17um
5.28um
8.20um
1801
10.0um
S4700 5.0kV 10.4mm x3.00k SE(U) 3/7/02 11:05
11.4µm
8.20µm
1804

FIG. 18

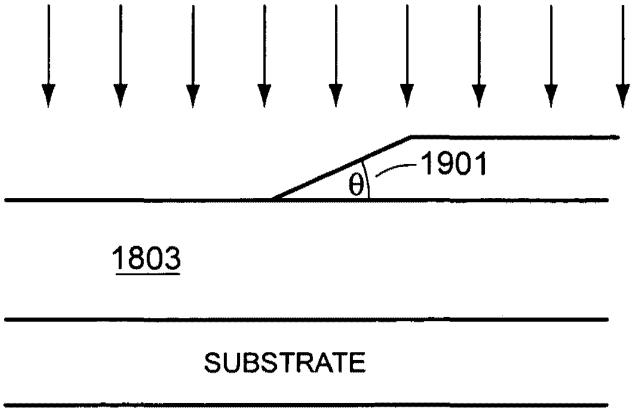
θ
1901
1803
SUBSTRATE

FIG. 19

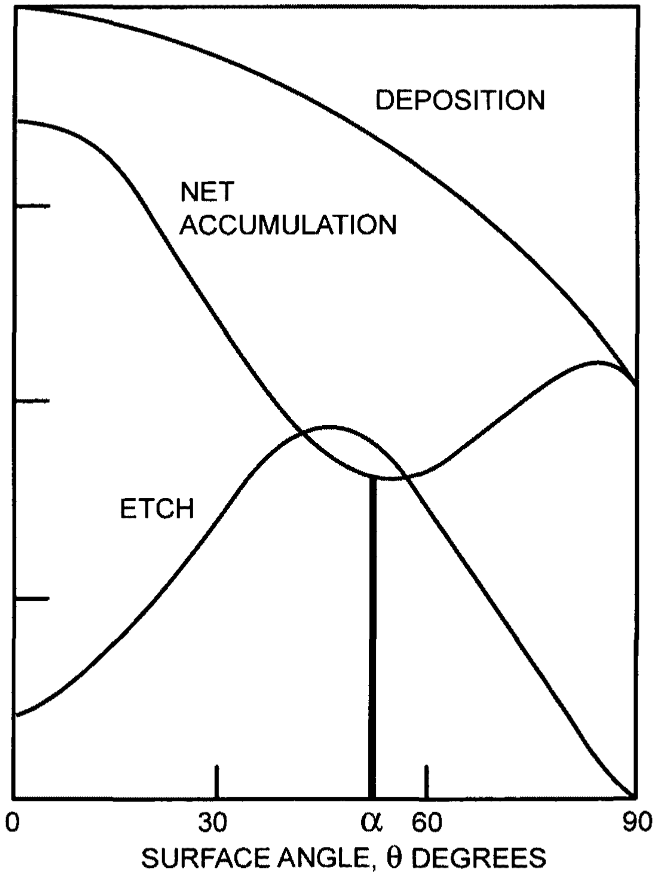
DEPOSITION
NET
ACCUMULATION
ETCH
0
30
α
60
90
SURFACE ANGLE, θ DEGREES

FIG. 20

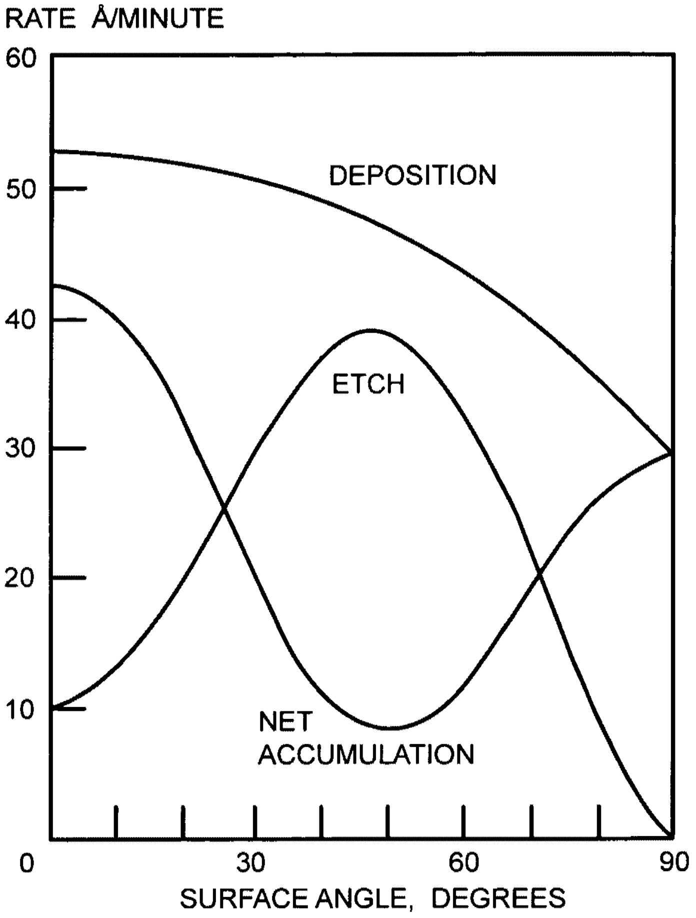
RATE Å/MINUTE
60
50
40
30
20
10
0
DEPOSITION
ETCH
NET
ACCUMULATION
30
60
90
SURFACE ANGLE, DEGREES

FIG. 21

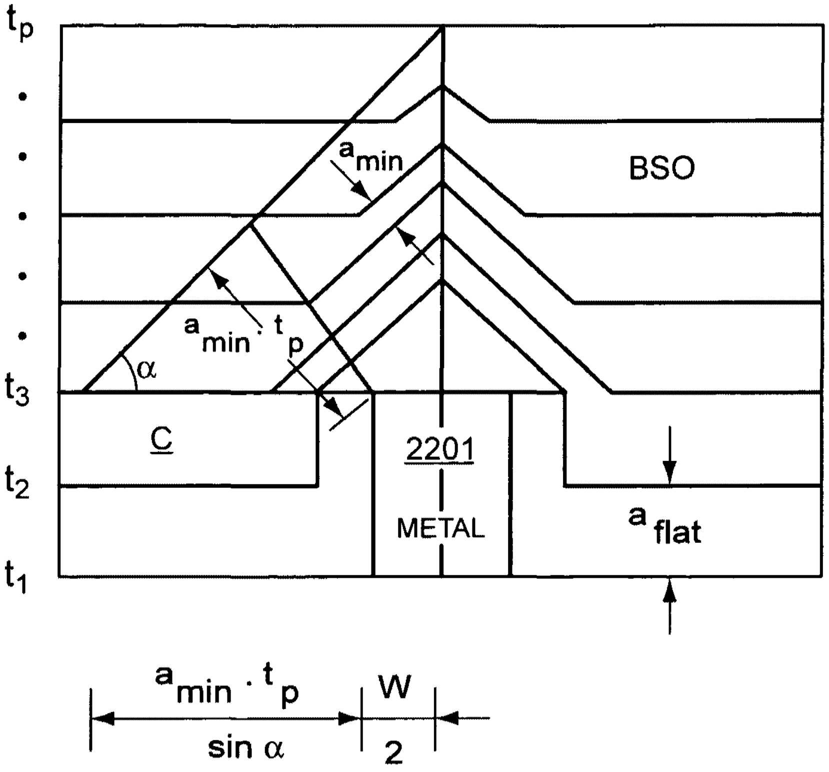
t_p
t_3
t_2
t_1
a_{min}
BSO
$a_{min} \cdot t_p$
α
C
2201
METAL
a_{flat}
$\frac{a_{min} \cdot t_p}{\sin \alpha}$
$\frac{W}{2}$

FIG. 22

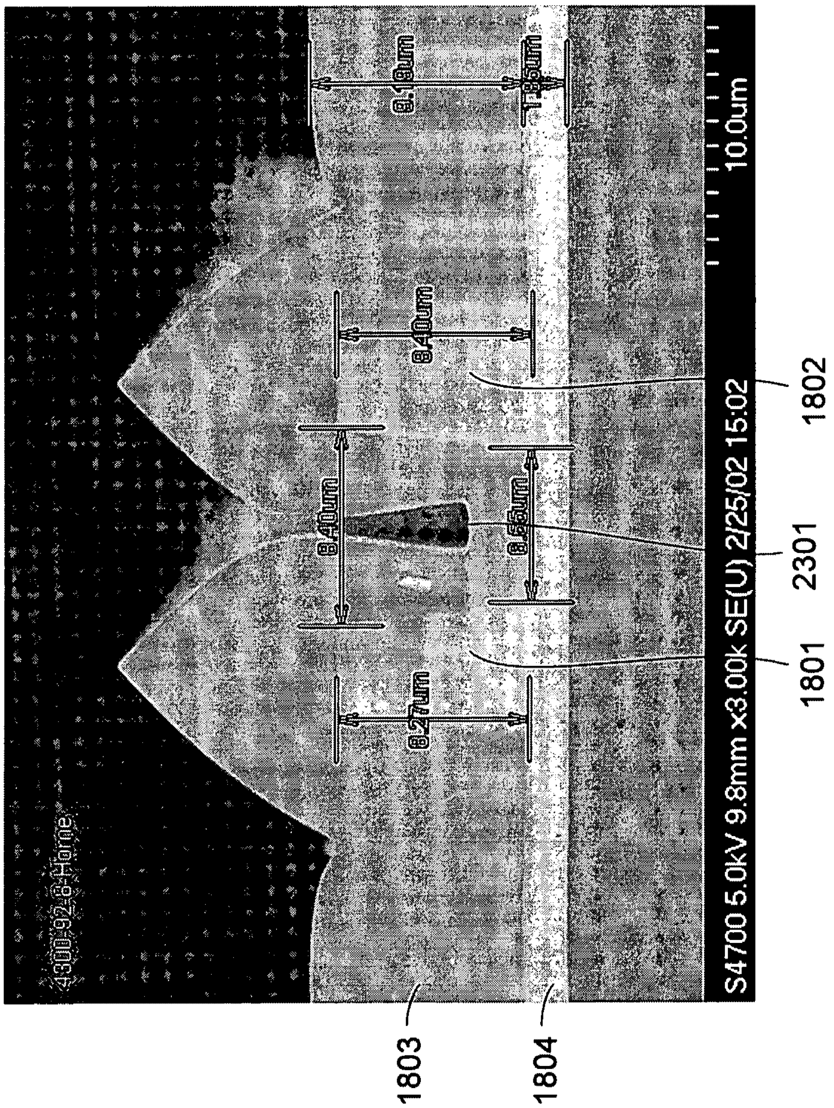
4300-92-8-Horne
8.18um
1.85um
10.0um
8.40um
8.40um
8.55um
8.27um
S4700 5.0kV 9.8mm x3.00k SE(U) 2/25/02 15:02
1802
2301
1801
1803
1804

FIG. 23

REPLACEMENT SHEET
Inventors: Hongmei ZHANG et al.
Application No. 11/228,834
Title: BIASED PULSE DC REACTIVE
SPUTTERING OF OXIDE FILMS

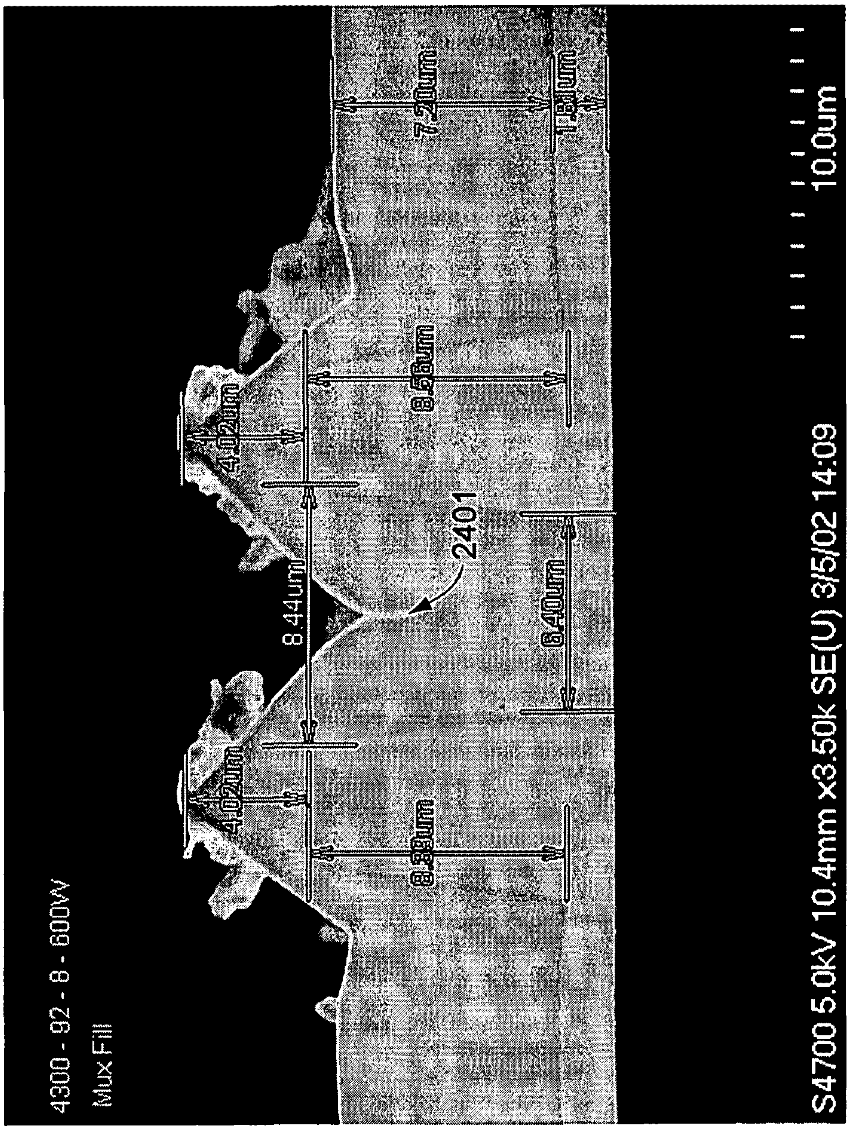

FIG. 24

BEST AVAILABLE COPY

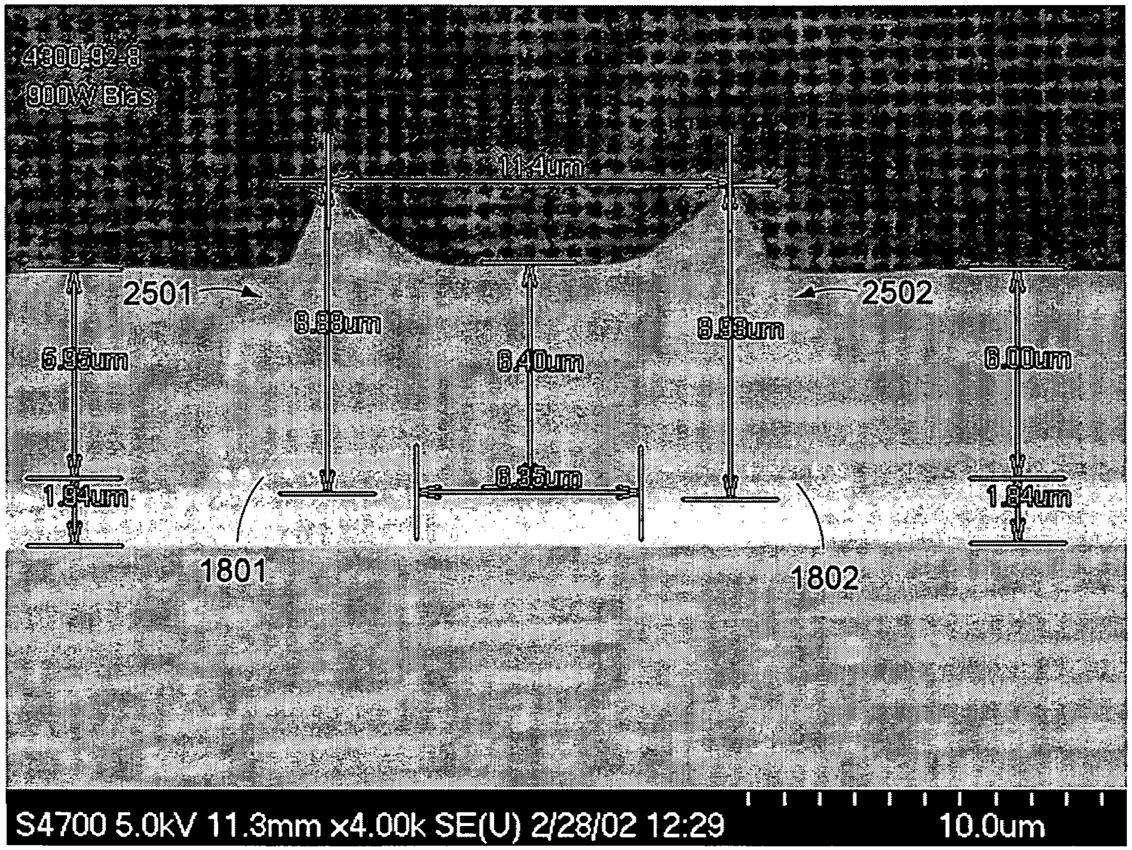
4300-92-8
900W Bias
11.4um
2501
2502
6.95um
8.88um
6.40um
8.93um
6.00um
6.35um
1.94um
1.84um
1801
1802
S4700 5.0kV 11.3mm x4.00k SE(U) 2/28/02 12:29
10.0um

FIG. 25

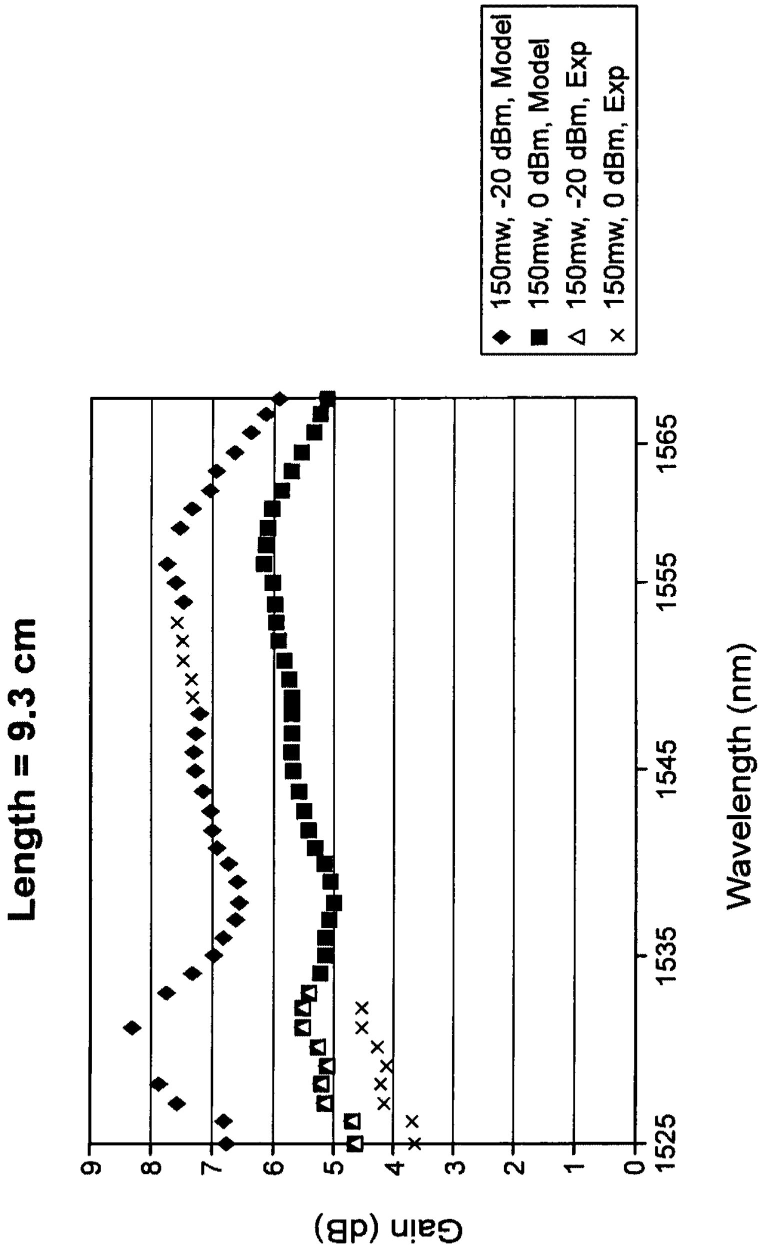
Length = 9.3 cm
Gain (dB)
0
1
2
3
4
5
6
7
8
9
1525
1535
1545
1555
1565
Wavelength (nm)
◆ 150mw, -20 dBm, Model
■ 150mw, 0 dBm, Model
△ 150mw, -20 dBm, Exp
× 150mw, 0 dBm, Exp

FIG. 26

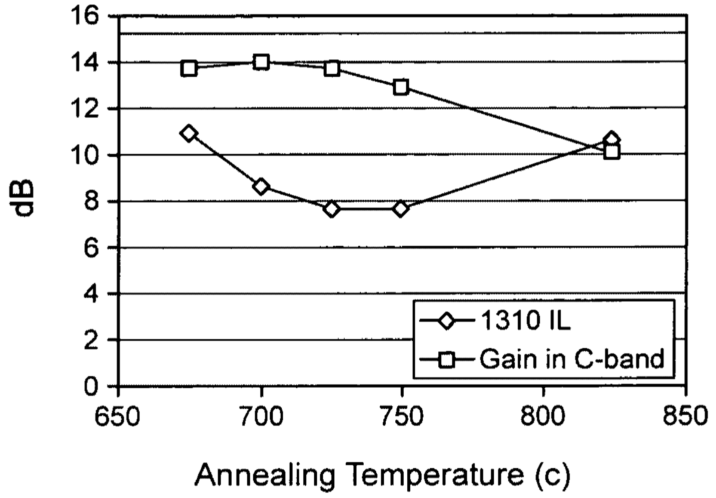
dB
16
14
12
10
8
6
4
2
0
650
700
750
800
850
Annealing Temperature (c)
1310 IL
Gain in C-band

FIG. 27

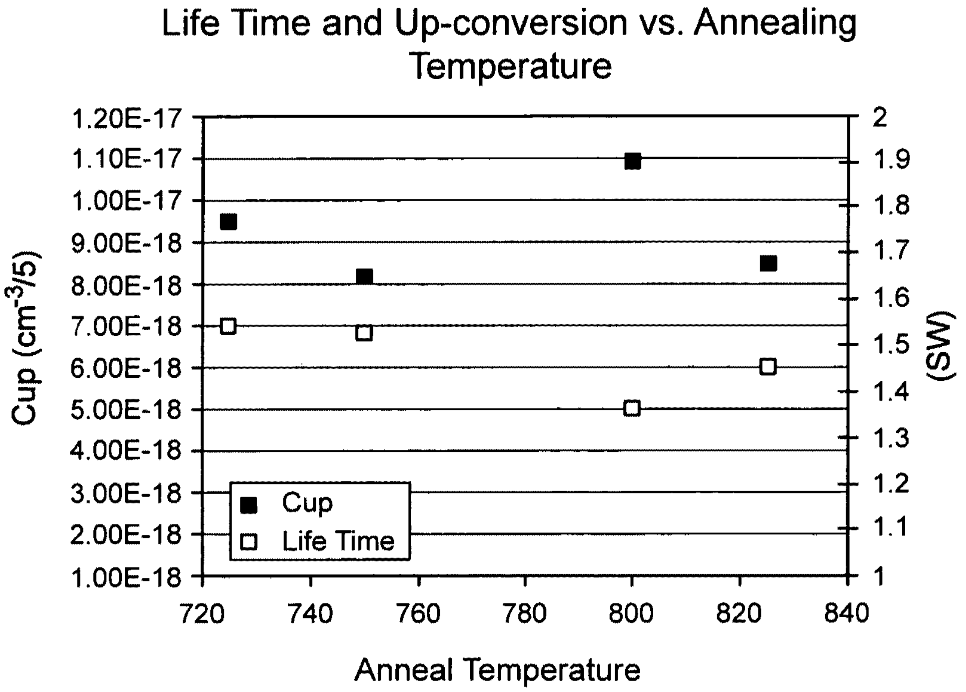
Life Time and Up-conversion vs. Annealing Temperature
Cup (cm-3/5)
1.20E-17
1.10E-17
1.00E-17
9.00E-18
8.00E-18
7.00E-18
6.00E-18
5.00E-18
4.00E-18
3.00E-18
2.00E-18
1.00E-18
(SW)
2
1.9
1.8
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1
720
740
760
780
800
820
840
Anneal Temperature
Cup
Life Time

FIG. 28

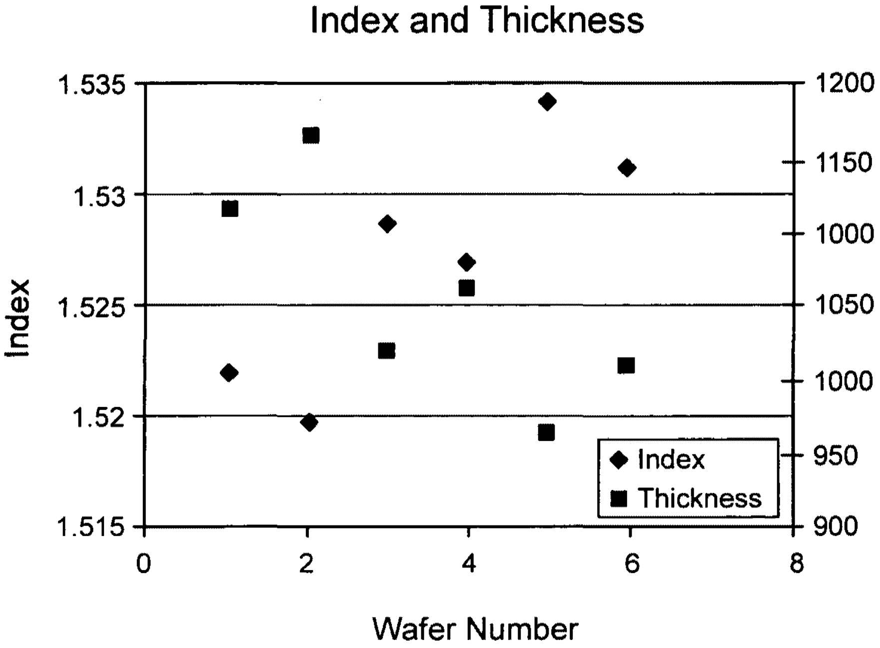
Index and Thickness
Index
1.535
1.53
1.525
1.52
1.515
1200
1150
1000
1050
1000
950
900
0
2
4
6
8
Wafer Number
◆ Index
■ Thickness

FIG. 29

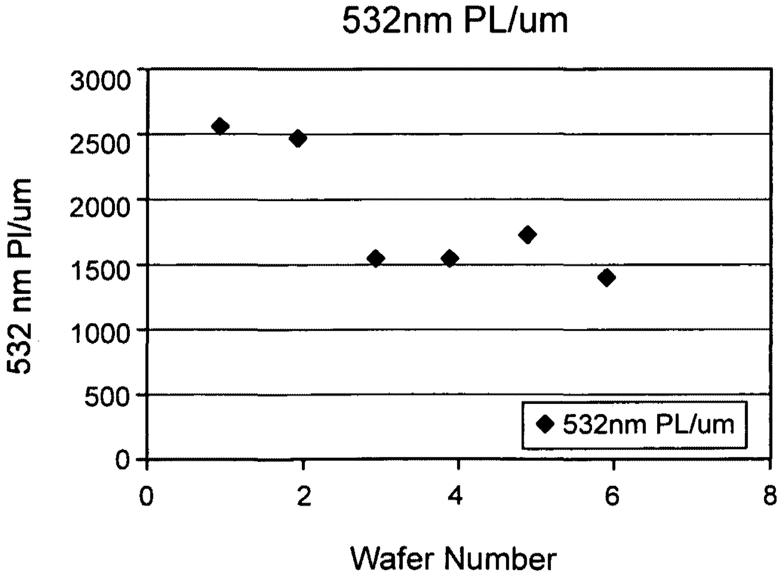
532nm PL/um
532 nm Pl/um
3000
2500
2000
1500
1000
500
0
0
2
4
6
8
Wafer Number
◆ 532nm PL/um

FIG. 30

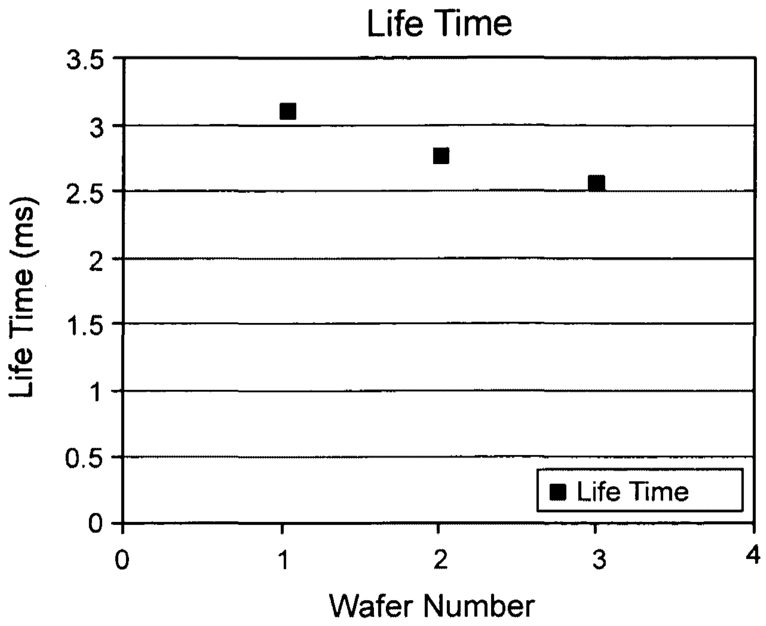
Life Time
3.5
3
2.5
2
1.5
1
0.5
0
Life Time (ms)
0
1
2
3
4
Wafer Number
■ Life Time

FIG. 31

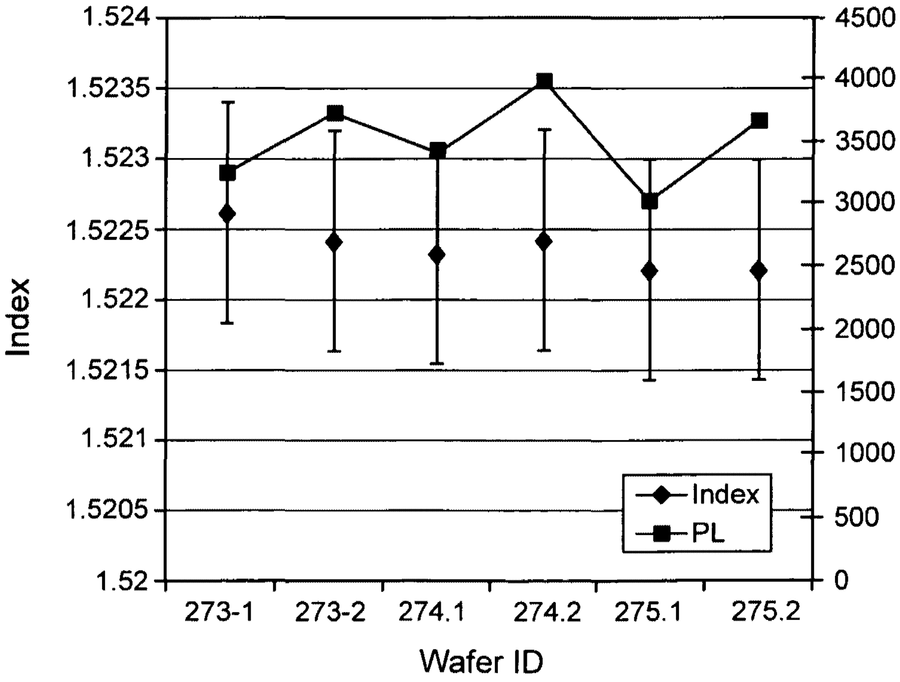
1.524
1.5235
1.523
1.5225
1.522
1.5215
1.521
1.5205
1.52
Index
4500
4000
3500
3000
2500
2000
1500
1000
500
0
273-1
273-2
274.1
274.2
275.1
275.2
Wafer ID
◆ Index
■ PL

FIG. 32

REPLACEMENT SHEET
Inventors: Hongmei ZHANG et al.
Application No. 11/228,834
Title: BIASED PULSE DC REACTIVE
SPUTTERING OF OXIDE FILMS

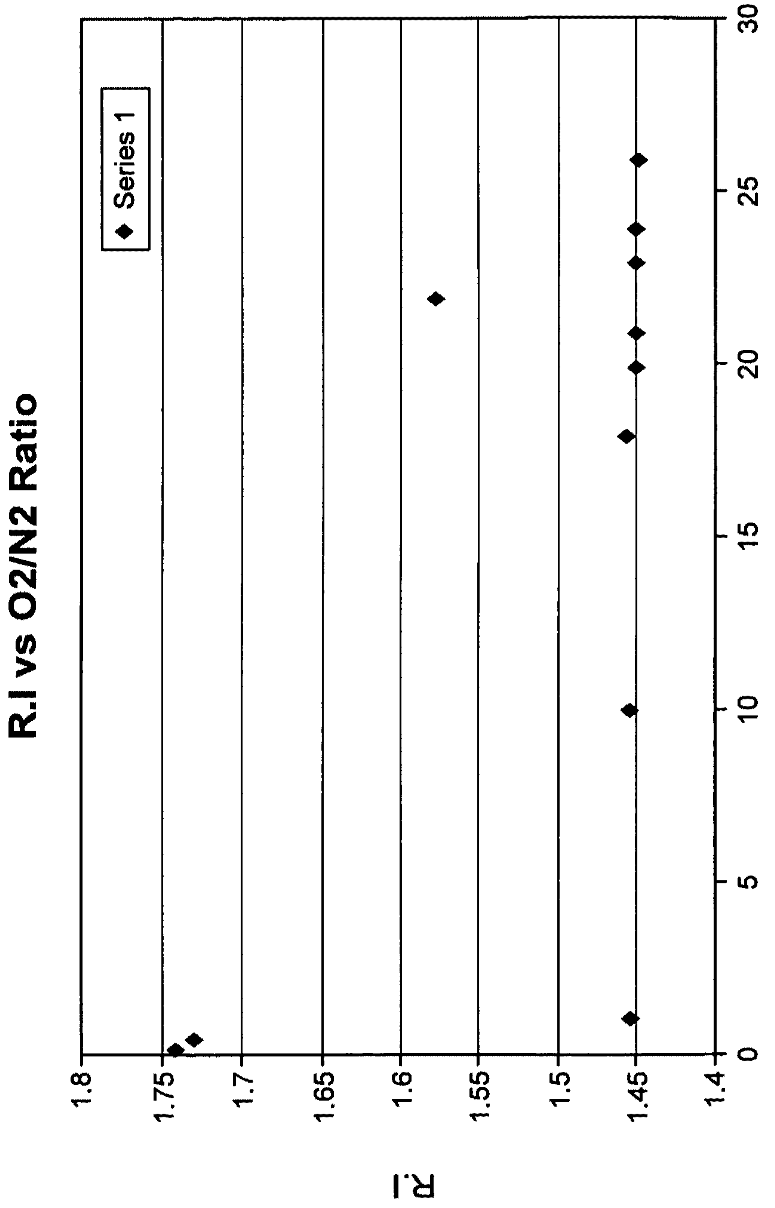

FIG. 33

#3

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Attorney Docket No.: M-12245 US

DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below adjacent to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of subject matter (process, machine, manufacture, or composition of matter, or an improvement thereof) which is claimed and for which a patent is sought by way of the application entitled

Biased Pulse DC Reactive Sputtering of Oxide Films

which (check) ☐ is attached hereto.

☐ and is amended by the Preliminary Amendment attached hereto.

☒ was filed on March 16, 2002 as Application Serial No. 10/10[illegible]863.

☐ and was amended on (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Day/Month/Year Filed	Yes	No
N/A			☐	☐

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

Provisional Application Number	Filing Date
N/A	

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or PCT international application(s) designating the United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56, which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status (patented, pending, abandoned)
N/A		

Attorney Docket No.: M-12245 US

I hereby appoint the following practitioners to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith:

Customer Number 24251

Please direct all telephone calls to:

Gary J. Edwards

Telephone: 408-453-9200

I declare that all statements made herein of my own knowledge are true, all statements made herein on information and belief are believed to be true, and all statements made herein are made with the knowledge that whoever, in any matter within the jurisdiction of the Patent and Trademark Office, knowingly and willfully falsifies, conceals, or covers up by any trick, scheme, or device a material fact, or makes any false, fictitious or fraudulent statements or representations, or makes or uses any false writing or document knowing the same to contain any false, fictitious or fraudulent statement or entry, shall be subject to the penalties including fine or imprisonment or both as set forth under 18 U.S.C. 100 . and that violations of this paragraph may jeopardize the validity of the application or this document, or the validity or enforceability of any patent, trademark registration, or certificate resulting therefrom.

Full name of first joint inventor: Hongmei Zhang
Inventor's Signature: Date: 08/08/02
Residence: San Jose, California
Post Office Address: 1330 Rodney Drive Citizenship: People of Republic China
San Jose, California 95118

Full name of second joint inventor: Mukundan Narasimhan
Inventor's Signature: Date: 08/08/02
Residence: San Jose, California
Post Office Address: 293 Bluefield Drive Citizenship:
San Jose, California 95136

Full name of third joint inventor: Ravi B. Mullapudi
Inventor's Signature: Date: 08/08/02
Residence: San Jose, California
Post Office Address: 2117 Shiangzone Court Citizenship: India
San Jose, California 95121

Full name of fourth joint inventor: Richard E. Demaray
Inventor's Signature: Date: 8/8/02
Residence: Portola Valley, California
Post Office Address: 190 Fawn Lane Citizenship: USA
Portola Valley, California 94028

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NOV 28 2005
PATENT & TRADEMARK OFFICE

PATENT
Customer No. 22,852
Attorney Docket No. 9140.0016-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
)
ZHANG, Hongmei et al.) Group Art Unit: 1753
)
Application No.: 11/228,834) Examiner: Not Yet Assigned
)
Filed: September 16, 2005) Confirmation No.: 9006
)
For: BIASED PULSE DC REACTIVE)
SPUTTERING OF OXIDE FILMS)

MAIL STOP MISSING PARTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

SECOND SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§ 1.56 and 1.97(b), Applicants bring to the attention of the Examiner the documents on the attached listing. This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits for the above-referenced application. Applicants respectfully request that the Examiner consider the listed documents and indicate that they were considered by making appropriate notations on the attached form.

Copies of the listed non-patent literature documents are attached.

Applicants respectfully request that the Examiner consider the listed documents and indicate that they were considered by making appropriate notations on the attached form.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or

constitute "prior art." If the Examiner applies any of the documents as prior art against any claims in the application and Applicants determine that the cited documents do not constitute "prior art" under United States law, Applicants reserve the right to present to the office the relevant facts and law regarding the appropriate status of such documents.

Applicants further reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: November 28, 2005

By: ____________________
Gary J. Edwards
Reg. No. 41,008

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IDS Form PTO/SB/08: Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	1

Complete if Known	
Application Number	11/228,834
Filing Date	September 16, 2005
First Named Inventor	ZHANG, Hongmei
Art Unit	1753
Examiner Name	Not Yet Assigned
Attorney Docket Number	9140.0016-02

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Issue or Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

Note: Submission of copies of U.S. Patents and published U.S. Patent Applications is not required.

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	Translation[6]

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation[6]
		Office Action issued September 21, 2005 in U.S. Application No. 11/100,856 (Attorney Docket No. 09140.0015-01).	
		Office Action issued on October 25, 2005, in U.S. Appl. No. 10/954,182 (Attorney Docket No. 09140-0016-01000).	
		Office Action issued on October 3, 2005 in U.S. Application No. 10/650,461 (Attorney Docket No. 09140-0025-00).	

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Examiner Signature		Date Considered	

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PATENT
Customer No. 22,852
Attorney Docket No. 9140.0016-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
)
ZHANG, Hongmei et al.) Group Art Unit: 1753
)
Application No.: 11/228,834) Examiner: MCDONALD, Rodney Glenn
)
Filed: September 16, 2005)
) Confirmation No.: 9006
For: BIASED PULSE DC REACTIVE)
SPUTTERING OF OXIDE FILMS)

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

THIRD SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§ 1.56 and 1.97(b), Applicants bring to the attention of the Examiner the documents on the attached listing. This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits for the above-referenced application.

Copies of the listed foreign and non-patent literature documents are attached. Copies of the U.S. patents and patent publications are not enclosed.

Applicants respectfully request that the Examiner consider the listed documents and indicate that they were considered by making appropriate notations on the attached form.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or

constitute "prior art." If the Examiner applies any of the documents as prior art against any claim in the application and Applicants determine that the cited documents do not constitute "prior art" under United States law, Applicants reserve the right to present to the office the relevant facts and law regarding the appropriate status of such documents.

Applicants further reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: November 7, 2006

By: Gary J. Edwards
Gary J. Edwards
Reg. No. 41,008

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet	1	of	6

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Application Number	11/228,834
Filing Date	September 16, 2005
First Named Inventor	ZHANG, Hongmei
Art Unit	1753
Examiner Name	MCDONALD, Rodney Glenn
Attorney Docket Number	9140.0016-02

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Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Issue or Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-3,309,302	03-14-1967	Heil	
		US-4,710,940	12-01-1987	Sipes, Jr.	
		US-4,785,459	11-15-1988	Baer	
		US-5,338,625	08-16-1994	Bates et al.	
		US-5,512,147	04-30-1996	Bates et al.	
		US-5,569,520	10-29-1996	Bates	
		US-5,597,660	01-28-1997	Bates	
		US-5,612,152	03-18-1997	Bates	
		US-6,088,492	07-11-2000	Kaneko et al.	
		US-6,236,793 B1	05-22-2001	Lawrence et al.	
		US-6,242,129 B1	06-05-2001	Johnson	
		US-6,288,835 B1	09-11-2001	Nilsson et al.	
		US-6,290,821 B1	09-18-2001	McLeod	
		US-6,306,265 B1	10-23-2001	Fu et al.	
		US-6,356,694 B1	03-12-2002	Weber	
		US-6,452,717 B1	09-17-2002	Endo	
		US-6,632,563 B1	10-14-2003	Krasnov et al.	
		US-6,673,716 B1	01-06-2004	D'Couto et al.	
		US-6,760,520 B1	07-06-2004	Medin et al.	
		US 6,768,855 B1	07-27-2004	Bakke et al.	
		US-6,884,327 B2	04-26-2005	Pan et al.	
		US-2001/0031122 A1	10-18-2001	Lackritz et al.	
		US-2002/0076133 A1	06-20-2002	Li et al.	
		US-2003/0044118 A1	03-06-2003	Zhou et al.	
		US-2003/0143853 A1	07-31-2003	Celii et al.	
		US-2003/0185266 A1	10-02-2003	Henrichs	
		US-2005/0048802 A1	03-02-2005	Zhang et al.	

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				Application Number	11/228,834
				Filing Date	September 16, 2005
				First Named Inventor	ZHANG, Hongmei
				Art Unit	1753
				Examiner Name	MCDONALD, Rodney Glenn
Sheet	2	of	6	*Attorney Docket Number*	9140.0016-02

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

		US-2005/0183946 A1	08-25-2005	Pan et al.	
		US-2006/0057283 A1	03-16-2006	Zhang et al.	
		US-2006/0057304 A1	03-16-2006	Zhang et al.	
		US-2006/0071592 A1	04-06-2006	Narasimhan et al.	
		US-2006/0134522 A1	06-22-2006	Zhang et al.	

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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	Translation[6]
		JP 7-224379 A	08-22-1995	Ulvac Japan Ltd		
		KR 2002-26187	04-06-2002	Hyundai Motor Co Ltd		Abstract
		WO 01/82297 A1	11-01-2001	Koninklijke Philips Electronics N.V.		
		WO 2004/106581 A2	12-09-2004	Symmorphix, Inc.		
		WO 2004/106582 A2	12-09-2004	Symmorphix, Inc.		
		WO 2006/063308 A2	06-15-2006	Symmorphix, Inc.		

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation[6]
		AGRAWAL, G.P., in: Fiber-Optic Communication Systems, 2nd Edition, John Wiley & Sons, New York, pp. 361-399 and 415 (1997).	
		COCORULLO, G. et al., "Amorphous silicon waveguides and light modulators for integrated photonics realized by low-temperature plasma-enhanced chemical-vapor deposition," Optics Lett. 21(24):2002-2004 (1996).	
		MASUDA, H. & KAWAI, S., "Wide-band and gain-flattened hybrid fiber amplifier consisting of an EDFA and a multiwavelength pumped raman amplifier," IEEE Photonics Technology Lett. 11(6):647-649 (1999).	
		SNOEKS, E. et al., "Cooperative upconversion in erbium-implanted soda-lime silicate glass optical waveguides," J. Opt. Soc. Am. B 12(8):1468-1474 (1995).	

Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT		*Application Number*	11/228,834
		Filing Date	September 16, 2005
		First Named Inventor	ZHANG, Hongmei
		Art Unit	1753
(Use as many sheets as necessary)		*Examiner Name*	MCDONALD, Rodney Glenn
Sheet 3	of 6	*Attorney Docket Number*	9140.0016-02

NON PATENT LITERATURE DOCUMENTS

		Response to Office Action filed on October 17, 2005 in U.S. Application No. 10/291,179 (Atty. Docket No. 09140.0001-00).	
		Final Office Action issued on December 14, 2005 in U.S. Application No. 10/291,179 (Atty. Docket No. 09140.0001-00).	
		Response to Final Office Action filed April 14, 2006, in U.S. Appl. No. 10/291,179 (Atty. Docket No. 9140.0001-00).	
		Office Action mailed April 27, 2006, in U.S. Appl. No. 10/291,179 (Atty. Docket No. 9140.0001-00).	
		Response to Office Action filed July 27, 2006, in U.S. Appl. No. 10/291,179 (Atty. Docket No. 9140.0001-00).	
		Final Office Action dated October 12, 2006, in U.S. Application No. 10,291,179 (Attorney Docket No. 9140.0001-00).	
		Response to Final Office Action mailed November 3, 2006, in U.S. Application No. 10,291,179 (Attorney Docket No. 9140.0001-00).	
		Office Action issued November 28, 2001, for US Patent No. 6,506,289 (Atty. Docket No. 09140.0002-01).	
		Response to Office Action filed February 20, 2002, for US Patent No. 6,506,289 (Atty. Docket No. 09140.0002-01).	
		Office Action issued April 17, 2002, for US Patent No. 6,506,289 (Atty. Docket No. 09140.0002-01).	
		Response to Office Action filed July 17, 2002, for US Patent No. 6,506,289 (Atty. Docket No. 09140.0002-01).	
		Notice of Allowance mailed August 6, 2002, for US Patent No. 6,506,289 (Atty. Docket No. 09140.0002-01).	
		Ex parte Quayle Action mailed November 10, 2003 for US Patent No. 6,827,826 (Atty. Docket No. 09140.0002-02).	
		Notice of Allowance mailed March 25, 2004 for US Patent No. 6,827,826 (Atty. Docket No. 09140.0002-02).	
		PCT Invitation to Pay Additional Fees for PCT/US01/22750, dated March 13, 2002 (Atty. Docket No. 09140.0002-00304).	
		PCT International Search Report for PCT/US01/22750, dated July 19, 2002 (Atty. Docket No. 09140.0002-00304).	
		PCT Written Opinion for PCT/US01/22750, dated July 23, 2002 (Atty. Docket No. 09140.0002-00304).	
		PCT International Preliminary Examination Report for PCT/US01/22750, dated	

Examiner Signature		Date Considered	

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IDS Form PTO/SB/08: Substitute for form 1449A/PTO		**Complete if Known**	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		*Application Number*	11/228,834
		Filing Date	September 16, 2005
		First Named Inventor	ZHANG, Hongmei
		Art Unit	1753
(Use as many sheets as necessary)		*Examiner Name*	MCDONALD, Rodney Glenn
Sheet 4	of 6	*Attorney Docket Number*	9140.0016-02

NON PATENT LITERATURE DOCUMENTS

		October 8, 2002 (Atty. Docket No. 09140.0002-00304).	
		Notice of Allowance issued on October 8, 2002, in U.S. Patent No. 6,533,907 (Atty. Docket No. 09140-0004-00).	
		Amendment/RCE filed on March 10, 2005 in U.S. Application No. 09/903,081 (Atty. Docket No. 09140-0014-00).	
		Office Action issued on November 28, 2005 in U.S. Application No. 09/903,081 (Atty. Docket No. 09140-0014-00).	
		Response to Office Action filed February 28, 2006 in U.S. Application No. 09/903,081 (Atty. Docket No. 09140-0014-00).	
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		Notice of Allowance issued on October 21, 2004, in U.S. Application No. 10/101,492 (Atty. Docket No. 09140-0015-00).	
		Response to Office Action filed February 17, 2006 in U.S. Application No. 11/100,856 (Atty. Docket No. 09140.0015-01).	
		Final Office Action mailed June 9, 2006 in U.S. Appl. No. 11/100,856 (Atty. Docket No. 09140.0015-01).	
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		Response to Office Action filed December 5, 2005, in U.S. Application No. 10/101,863 (Atty. Docket No. 09140.0016-00).	
		Final Office Action issued on February 14, 2006, in U.S. Application No. 10/101,863 (Atty. Docket No. 09140.0016-00).	
		Response to Office Action filed February 24, 2006, in U.S. Application No. 10/101,863 (Atty. Docket No. 09140.0016-00).	
		Office Action mailed March 22, 2006, in U.S. Appl. No. 10/101,863 (Atty. Docket No. 09140.0016-00).	
		Response to Office Action filed June 12, 2006, in U.S. Appl. No. 10/101,863 (Atty. Docket No. 09140.0016-00).	
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		Response to Office Action filed on July 25, 2005 in Application No. 10/954,182 (Atty. Docket No. 09140.0016-01).	

Examiner Signature		Date Considered	

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IDS Form PTO/SB/08: Substitute for form 1449A/PTO **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** *(Use as many sheets as necessary)*				***Complete if Known***	
				Application Number	11/228,834
				Filing Date	September 16, 2005
				First Named Inventor	ZHANG, Hongmei
				Art Unit	1753
				Examiner Name	MCDONALD, Rodney Glenn
Sheet	5	of	6	*Attorney Docket Number*	9140.0016-02

NON PATENT LITERATURE DOCUMENTS			
		Response to Office Action filed on December 21, 2005 in Application No. 10/954,182 (Atty. Docket No. 09140.0016-01).	
		Office Action issued on March 9, 2006, in U.S. Appl. No. 10/954,182 (Atty. Docket No. 09140-0016-01000).	
		Response to Office Action filed on August 9, 2006 in Application No. 10/954,182 (Atty. Docket No. 09140.0016-01).	
		Office Action dated October 31, 2006, in Application No. 10/954,182 (Atty. Docket No. 09140.0016-01).	
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		Response to Office Action filed on July 24, 2006, in U.S. Application No. 10/650,461 (Atty. Docket No. 09140-0025-00).	
		Final Office Action mailed October 19, 2006, in U.S. Application No. 10/650,461 (Attorney Docket No. 09140.0025-00).	
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		Response to Office Action filed March 2, 2006 in U.S. Application No. 10/789,953 (Atty. Docket No. 09140.0030-00).	
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		Office Action from Singapore Patent Office in Appl. No. 200505388-9, dated	

Examiner Signature		Date Considered	

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				Art Unit	1753
				Examiner Name	MCDONALD, Rodney Glenn
Sheet	6	of	6	*Attorney Docket Number*	9140.0016-02

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		Office Action issued on October 19, 2005 in U.S. Application No. 10/851,542 (Atty. Docket No. 09140.0033-00).	
		Response to Office Action filed January 19, 2006 in U.S. Application No. 10/851,542 (Atty. Docket No. 09140.0033-00).	
		Office Action mailed April 19, 2006 in U.S. Application No. 10/851,542 (Atty. Docket No. 09140.0033-00).	
		Response to Office Action filed July 26, 2006 in U.S. Application No. 10/851,542 (Atty. Docket No. 09140.0033-00).	
		Final Office Action dated October 26, 2006, in U.S. Application No. 10/851,542 (Atty. Docket No. 09140.0033-00).	
		PCT International Search Report and Written Opinion for Application No. PCT/US2004/014524 dated March 2, 2005 (Atty. Docket No. 09140.0033-00304).	
		PCT International Preliminary Report on Patentability for Application No. PCT/US2004/014524, dated December 8, 2005 (Atty. Docket No. 09140.0033-00304).	
		PCT International Search Report and Written Opinion for Application No. PCT/US2004/014523 dated January 17, 2005 (Atty. Docket No. 09140.0034-00304).	
		PCT International Preliminary Report on Patentability for Application No. PCT/US2004/014523, dated December 8, 2005 (Atty. Docket No. 09140.0034-00304).	

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(71) Applicant **ULVAC JAPAN LTD**

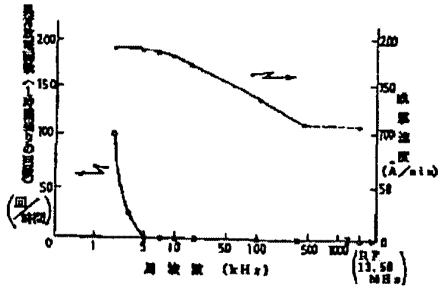
(72) Inventor:
OTA ATSUSHI
HAGA HIDEAKI
TANI NORIAKI
SUU KOUKOU
KOMATSU TAKASHI
NAKAMURA KYUZO
MOMONO TAKESHI
KAWAMURA HIROAKI
SUZUKI IKUO
IKEDA SATOSHI
ISHIKAWA MICHIO
OTA YOSHIFUMI
MATSUMOTO MASAHIRO

(54) SPUTTERING METHOD AND DEVICE THEREFOR

(57) Abstract:

PURPOSE: To form a film at a high rate without generating an abnormal discharge for a long time at the time of sputtering a conductive target in a gaseous reactant atmosphere by DC sputtering by applying a positive potential on a negative-potential target in the form of a pulse.

CONSTITUTION: A substrate and a conductive target are opposed in a vacuum treating chamber, and the target is sputtered in a gaseous reactant atmosphere by DC sputtering to form a thin film on the substrate. In this case, a device with a power source to apply a positive potential on a negative potential connected to the target is used, and a positive potential is applied on the negative-potential target in the form of a pulse at the frequency of 5-400kHz to conduct sputtering. The electron in the plasma is attracted by the positive potential to neutralize the plus ion accumulated on the insulator and high-resistance film, and the abnormal discharge due to an arc discharge is not generated.



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(71)出願人　000231464
日本真空技術株式会社
神奈川県茅ヶ崎市萩園2500番地

(72)発明者　太田　淳
千葉県山武郡山武町横田523　日本真空技術株式会社千葉超材料研究所内

(72)発明者　羽賀　日出明
千葉県山武郡山武町横田523　日本真空技術株式会社千葉超材料研究所内

(72)発明者　谷　典明
千葉県山武郡山武町横田523　日本真空技術株式会社千葉超材料研究所内

(74)代理人　弁理士　北村　欣一　（外２名）

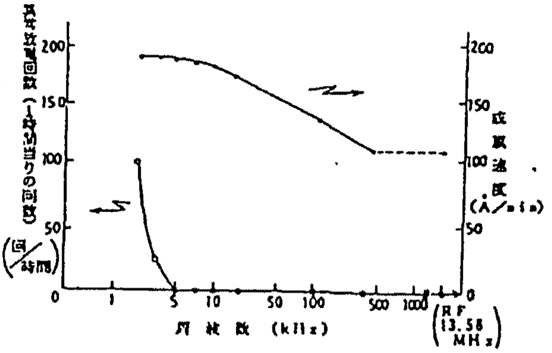
最終頁に続く

(54)【発明の名称】　スパッタ方法およびそのスパッタ装置

(57)【要約】

【目的】　反応ガス雰囲気中で直流スパッタ法により導電性ターゲットにスパッタリングを行っても高速成膜が可能であり、かつ、長時間スパッタリングを行っても異常放電のないスパッタ成膜が出来るスパッタ方法。

【構成】　反応ガス雰囲気中で直流スパッタ法により導電性ターゲットにスパッタリングを行って基板上に薄膜を形成するスパッタ法において、負電位の導電性ターゲットに正電位を一定の周波数でパルス状に印加しながらスパッタリングする。



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【特許請求の範囲】

【請求項１】　反応ガス雰囲気中で直流スパッタ法により導電性ターゲットにスパッタリングを行って基板上に薄膜を形成するスパッタ法において、負電位の導電性ターゲットに正電位を周波数５～４００ｋＨｚでパルス状に印加しながらスパッタリングすることを特徴とするスパッタ方法。

【請求項２】　前記導電性ターゲットはＳｉ、Ａｌ、Ｔａ、Ｔｉ、Ｃ、ＩＴＯ、ＺｎＯ、SnO_2またはこれらの合金であり、また、反応ガスはN_2、O_2、H_2、NH_3、ＣＯ、CO_2、CH_4、C_2H_2、H_2Oのいずれか１つまたは２つ以上の混合ガスであることを特徴とする請求項第１項に記載のスパッタ方法。

【請求項３】　真空処理室内に基板と導電性ターゲットを対向させて設け、反応ガス雰囲気中で直流スパッタ法により導電性ターゲットにスパッタリングを行って基板上に薄膜を形成するスパッタ装置において、負電位に正電位を周波数５～４００ｋＨｚでパルス状に印加する電源を導電性ターゲットに接続したことを特徴とするスパッタ装置。

【請求項４】　前記導電性ターゲットはＳｉ、Ａｌ、Ｔａ、Ｔｉ、Ｃ、ＩＴＯ、ＺｎＯ、SnO_2またはこれらの合金であり、また、反応ガスはN_2、O_2、H_2、NH_3、ＣＯ、CO_2、CH_4、C_2H_2、H_2Oのいずれか１つまたは２つ以上の混合ガスであることを特徴とする請求項第３項に記載のスパッタ装置。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明はスパッタ方法およびそのスパッタ装置に関し、更に詳しくは、反応ガス雰囲気中で導電性ターゲットにスパッタリングを行うスパッタ方法およびそのスパッタ装置に関する。

【０００２】

【従来の技術】従来から、反応ガス雰囲気中で導電性ターゲットにスパッタリングを行って基板上に誘電体膜、光学膜、保護膜等の膜を成膜するスパッタ方法に用いられるスパッタ装置としては、真空処理室内に基板とターゲットカソードを対向して設け、該ターゲットカソードに導電性ターゲットを装着し、真空処理室内を所定の雰囲気とした状態でターゲットに所定電圧を印加してターゲットにスパッタリングを行う装置が知られている。

【０００３】そして、スパッタリング時の電源としては直流電源、または例えば13.56MHzの高周波電源を用いている。

【０００４】

【発明が解決しようとする課題】前記従来のスパッタ装置を用いて基板上に誘電体膜、光学膜、保護膜等の膜を成膜する際、高周波電源を用いるＲＦスパッタリングは長時間異常放電なしに成膜することが可能であるが、成膜速度が遅いという問題がある。

【０００５】また、前記従来のスパッタ装置を用いて基板上に誘電体膜、光学膜、保護膜等の膜を成膜する際、直流電源を用いるＤＣスパッタリングは成膜速度は速いが、スパッタリングの経時と共に、ターゲット表面に絶縁物や高抵抗膜が堆積するため、異常放電を起こすという問題がある。

【０００６】スパッタリング中に異常放電が発生すると欠陥のない均質な膜を成膜する上で致命的な悪影響を及ぼす。

【０００７】従って、従来のスパッタ装置では通常ＲＦスパッタリングを行っているが、高速成膜を必要とする場合は、ＤＣスパッタリングを行い、ターゲット表面に絶縁物や高抵抗膜が堆積しないようにターゲット全面に亘ってエロージョン化するようにしているが、異常放電を十分に除去することが出来ない。

【０００８】本発明はかかる問題点を解消し、反応ガス雰囲気中でスパッタリングを行っても高速成膜が可能であり、かつ、長時間スパッタリングを行っても異常放電のないスパッタ成膜の可能なスパッタ方法およびそれに用いるスパッタ装置を提供することを目的とする。

【０００９】

【課題を解決するための手段】本発明のスパッタ方法は、反応ガス雰囲気中で直流スパッタ法により導電性ターゲットにスパッタリングを行って基板上に薄膜を形成するスパッタ法において、負電位の導電性ターゲットに正電位を周波数５～４００ｋＨｚでパルス状に印加しながらスパッタリングすることを特徴とする。

【００１０】また、前記導電性ターゲットはＳｉ、Ａｌ、Ｔａ、Ｔｉ、Ｃ、ＩＴＯ、ＺｎＯ、SnO_2またはこれらの合金とし、また、反応ガスはN_2、O_2、H_2、NH_3、ＣＯ、CO_2、CH_4、C_2H_2、H_2Oのいずれか１つまたは２つ以上の混合ガスとしてもよい。

【００１１】本発明のスパッタ装置は、真空処理室内に基板と導電性ターゲットを対向させて設け、反応ガス雰囲気中で直流スパッタ法により導電性ターゲットにスパッタリングを行って基板上に薄膜を形成するスパッタ装置において、負電位に正電位を周波数５～４００ｋＨｚでパルス状に印加する電源を導電性ターゲットに接続したことを特徴とする。

【００１２】また、前記導電性ターゲットはＳｉ、Ａｌ、Ｔａ、Ｔｉ、Ｃ、ＩＴＯ、ＺｎＯ、SnO_2またはこれらの合金とし、また、反応ガスはN_2、O_2、H_2、NH_3、ＣＯ、CO_2、CH_4、C_2H_2、H_2Oのいずれか１つまたは２つ以上の混合ガスとしてもよい。

【００１３】

【作用】反応ガス雰囲気中で導電性ターゲットに直流電源より直流電圧を印加し、スパッタリングを行うとターゲットはスパッタされて基板上に薄膜が形成される。

【００１４】長時間連続してスパッタリングを行うと、ターゲット上に堆積した絶縁物や高抵抗膜上に不活性ガスまたは反応ガスのプラス（＋）イオンが蓄積される。このプラス（＋）イオンの電荷がターゲット間、エロージョン部、アース電極等とアーク放電を引き起こして異常放電の原因となる。

【００１５】この異常放電でターゲット材、絶縁物、高抵抗膜が粒子状となって飛散し、基板上に付着し、成膜された薄膜の欠陥となる。

【００１６】ターゲットに直流電圧を印加してＤＣスパッタリングを行う際、負電位のターゲットに正電位を一定の周波数でパルス状に印加すると、正電位によりプラズマ中の電子を引き寄せ、ターゲット上に堆積した絶縁物、高抵抗膜上に蓄積するプラス（＋）イオンの電荷を中和し、アーク放電による異常放電を防止する。

【００１７】その際、ターゲットに印加する正電位の印加時間は負電位の時間に比べて極めて短くとも効果があるため、成膜速度は直流電流のみによる成膜速度より数％の減少となる程度であり、この成膜速度は高周波１３．５６ＭＨｚスパッタ時の成膜速度よりも高い。

【００１８】

【実施例】以下添付図面に従って本発明の実施例について説明する。

【００１９】図１は、スパッタ装置の１例を示すもので、図中、１は真空処理室を示す。

【００２０】真空処理室１を外部のクライオポンプのような真空ポンプ等の真空排気系２にバルブ３を介して接続し、該真空処理室１内の真空度を調節自在とすると共に、真空処理室１内に基板４とターゲットカソード５とを対向に配置し、該ターゲットカソード５の前面に導電性ターゲット６をロウ材でボンデングするようにしたまた、該真空処理室１内にガス導入管７を介してガスボンベ等のガス供給源８よりスパッタガスを導入するようにした。図示例ではガス導入管７を分岐し、一方の分岐管９ａにガス圧調節弁１０ａを介して不活性ガス（例えばアルゴンガス）のガス供給源８ａを接続し、他方の分岐管９ｂにガス圧調節弁１０ｂを介して反応ガス（例えば窒素ガス）のガス供給源８ｂを接続した。

【００２１】また、ターゲットカソード５に直流電源１１をパルスユニット１２を介して接続し、パルスユニット１２を調節して導電性ターゲット６に負電位と正電位を所定の周波数でパルス状に印加するようにした。

【００２２】また、ターゲットカソード５の背面側にマグネトロンスパッタのためのマグネット１３を配設して、ターゲットカソード５に取り付けられた導電性ターゲット６の表面にマグネトロンスパッタに必要な磁場を与えるようにした。

【００２３】次に、図１装置を用いて本発明のスパッタ方法の具体的実施例について説明する。

【００２４】実施例１

先ず、真空処理室１内に基板４と、ターゲットカソード５に導電性ターゲット６としてケイ素（Ｓｉ）製ターゲットを装着した。

【００２５】続いて、真空処理室１内を真空排気系２により 6.7×10^{-5}Pa（ 5×10^{-7}Torr）に排気した後、真空処理室１内にガス供給源８ａからのアルゴン（Ａｒ）ガスと、ガス供給源８ｂからの窒素（N_2 ）ガスとから成る反応ガスをガス導入管７を介して導入して、該真空処理室１内のスパッタ圧が 6.7×10^{-1}Pa（ 5×10^{-3} Ｔｏｒｒ）となるようにした。次に基板４上に形成される窒化ケイ素（ＳｉＮｘ　）の屈折率が2.03となるようにＡｒガスとN_2 ガスの流量をそれぞれ 100sccmと50sccmに調整した後、ＤＣマグネトロンスパッタ法により導電性ターゲット６に直流電源１１より直流電力３ｋＷを印加し、負電位のターゲット６に正電位をパルスユニット１２より周波数を2kHzから400kHzに変化させながらパルス状（図２参照）に印加し、スパッタリングを行って基板４上に膜厚 900Åの窒化ケイ素（ＳｉＮx ）膜を形成した。尚、負電位のターゲットにパルス状に印加する正電位の印加時間は周波数 10kHzまでの場合は10μsecとし、周波数 10kHzを超えて100kHzまでの場合は 5μsecとし、周波数100kHzを超えた場合は1μsec とした。また、ＤＣマグネトロンスパッタ時の磁場強度を 250Ｏｅとした。

【００２６】そして異常放電回数と成膜速度を負電位の導電性ターゲット６に印加する正電位の周波数毎に測定した。得られた測定結果を図３に示す。

【００２７】図３から明らかなように負電位に印加する正電位の周波数の増加に伴い、異常放電回数は減少し、周波数が5kHz以上ではその回数はほとんど０になり、これ以上の周波数で正電位を負電位のターゲットに印加すれば異常放電が発生しないことが分かる。また、負電位に印加する正電位の周波数が400kHz（時間1μsec ）の場合は、通常の高周波電源（13.56MHz）とほぼ同じ成膜速度となり、400kHz以上の周波数では正電位の印加は意味がない。従って、負電位のターゲットに印加する正電位の周波数範囲は 5～400kHzであることが確認された。

【００２８】また、周波数範囲 5～400kHzでの成膜速度は高周波電源（13.56MHz）よりも高い成膜速度である。

【００２９】反応ガス雰囲気中で直流スパッタ法により導電性ターゲットにスパッタリングを行うと、ターゲット上の非エロージョン部分に絶縁物または高抵抗膜が堆積し、従来の直流電源でターゲットに負の電位を放電し続けると、絶縁物上にプラス（＋）の電荷が蓄積し、ターゲット、エロージョン部、アース電極との間でアーク放電を起こし、電荷を放出する。その結果異常放電が発生することになるが、本発明では図２に示すように負電位に正電位を周期的に、即ち一定の周波数で印加することにより前記の電荷を補償して異常放電の発生を防止するようにしている。

【0030】実施例2
反応ガスとして酸素（O_2）ガスを用い、スパッタ圧を6.7×10^{-1}Ｐａ（5×10^{-3}Torr）とし、直流電力を2ｋＷとし、基板上に形成される酸化ケイ素（ＳｉＯｘ）の屈折率が1.46となるように酸素流量を調整した以外は前記実施例1と同様の方法でＤＣマグネトロンスパッタ法によりターゲットにスパッタリングを行って基板上に膜厚1000Åの酸化ケイ素（ＳｉＯｘ）膜を形成した。

【0031】そして異常放電回数を負電位のターゲットに印加する正電位の周波数毎に測定した。得られた測定結果を図4に示す。

【0032】図4から明らかなように負電位に印加する正電位の周波数は約5ｋＨｚで異常放電をほぼ防止し得ることが分かる。

【0033】尚、図4におけるＳｉＮｘの測定結果（黒丸印）は前記実施例1の測定結果を参考のために記載したものである。

【0034】実施例3
導電性ターゲットとしてグラファイト（Ｃ）を用い、反応ガスとしてメタン（CH_4）ガスを用い、スパッタ圧を6.7×10^{-1}Ｐａ（5×10^{-3}Torr）とし、直流電力を2ｋＷとした以外は前記実施例1と同様の方法でＤＣマグネトロンスパッタ法によりターゲットにスパッタリングを行って基板上に膜厚200Åのダイヤモンドライクカーボン（ＤＬＣ）膜を形成した。

【0035】そして異常放電回数を負電位のターゲットに印加する正電位の周波数毎に測定した。得られた測定結果を図4に示す。

【0036】図4から明らかなように負電位に印加する正電位の周波数は約5ｋＨｚで異常放電をほぼ防止し得ることが分かる。

【0037】前記実施例1，2，3の結果から、導電性ターゲット材料、放電状態によりプラス（＋）の電荷の蓄積量が異なるため、異常放電はターゲットに印加する周波数に大きく依存する。従って、周波数5ｋＨｚ以上であれば、種々のターゲット材料でもスパッタリング中の異常放電を大幅に減少することが出来ることになる。

【0038】実施例4
導電性ターゲットとしてアルミニウム（Ａｌ）、チタン（Ｔｉ）、タンタル（Ｔａ）、またはこれらの合金例えばＡｌ－2at％Ｔｉを用い、反応ガスとして窒素（N_2）、酸素（O_2）、水素（H_2）、一酸化炭素（ＣＯ）、二酸化炭素（CO_2）、アンモニア（NH_3）、水（H_2O）を単独、或いは2種以上を用い、これらを種々組み合わせし、その他の条件を前記実施例1と同様にしてＤＣマグネトロンスパッタ法により基板上に酸化物、窒化物、炭化物のいずれかの薄膜を形成したが、負電位に印加する正電位が周波数5ｋＨｚ以上ではスパッタリング中に異常放電の発生は見られなかった。

【0039】また、前記実施例1では導電性ターゲットにＳｉを用い、反応ガスとして窒素ガスを用いて基板上に窒化ケイ素（ＳｉＮｘ）膜を形成したが、導電性ターゲットとしてＳｉの代わりにIn_2O_3－SnO_2焼結体（ＩＴＯ）、酸化亜鉛（ＺｎＯ）、酸化スズ（SnO_2）を用い、反応ガスとして窒素ガスの代わりに酸素（O_2）、一酸化炭素（ＣＯ）、二酸化炭素（CO_2）、水（H_2O）等の酸素を含むガス、またはそのガスに水素ガス（H_2）混合したガスを用い、負電位のターゲットに印加する正電位の周波数を5～400ｋＨｚとした直流スパッタ法（ＤＣマグネトロンスパッタ法）により基板上に透明導電膜であるＩＴＯ、ＺｎＯ、SnO_2の薄膜を形成することが出来る。

【0040】図1装置では負電位に一定の周波数で正電位をパルス状に印加する電源装置として直流電源とパルス電源の組み合わせた装置としたが、これに限定されるものではなく、図2に示すような負電位に正電位が周期的（パルス状）に印加される一体型の電源装置としてもよい。

【0041】
【発明の効果】本発明のスパッタ方法によるときは、反応ガス雰囲気中で、負電位の導電性ターゲットに正電位を一定の周波数でパルス状に印加しながらスパッタリングを行うようにしたので、スパッタリング中にターゲット上に堆積した絶縁物、高抵抗膜上に蓄積するプラスイオンの電荷を中和することが出来て、アーク放電による異常放電を防止しながら長時間に亘って速い成膜速度で基板上に欠陥のない均質な薄膜を形成することが出来る効果がある。

【0042】また、本発明のスパッタ装置によるときは、導電性ターゲットに負電位に正電位を一定の周波数でパルス状に印加する電源を接続するようにしたので、アーク放電による異常放電を防止しながら長時間に亘って速い成膜速度で基板上に欠陥のない均質な薄膜を形成することが出来るスパッタ装置を提供する効果がある。

【図面の簡単な説明】

【図1】　本発明のスパッタ方法を実施するためのスパッタ装置の1例の概略截断側面図。

【図2】　図1装置による導電性ターゲットに印加される電位のモデル図。

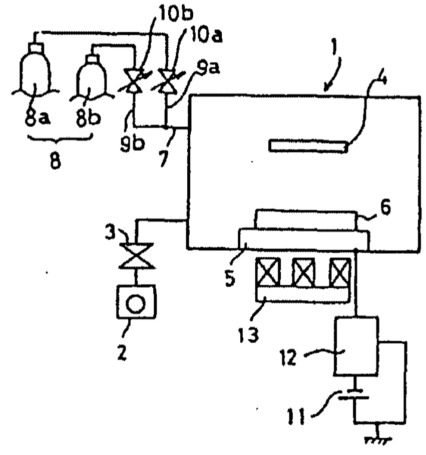
【図3】　本発明スパッタ方法の1実施例における成膜時の周波数と異常放電回数との関係、並びに周波数と成膜速度との関係を示す特性線図。

【図4】　本発明スパッタ方法の他の実施例における成膜時の周波数と異常放電回数との関係を示す特性線図。

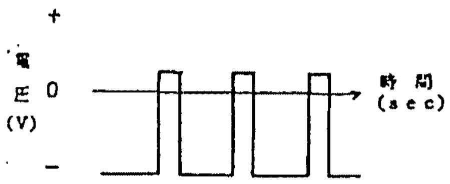
【符号の説明】

1　真空処理室、　2　真空排気系、　4　基板、　6　導電性ターゲット、　7　ガス導入管、　8　スパッタガス供給源、　11　直流電源、　12　パルスユニット。

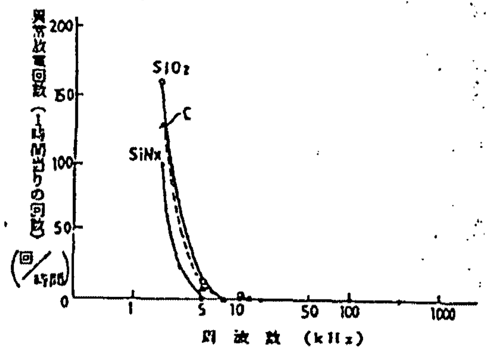
【図1】



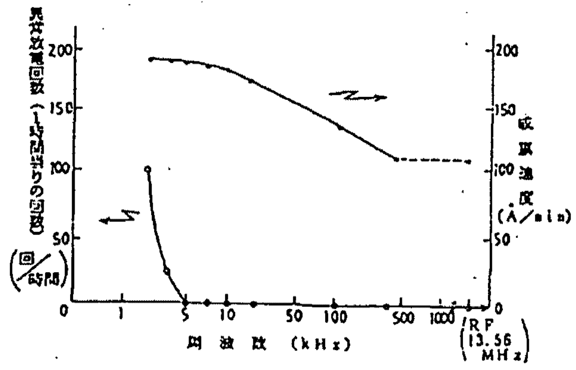
【図2】



【図4】



【図3】



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(72)発明者　鄒　紅▲こう▼
千葉県山武郡山武町横田523　日本真空技術株式会社千葉超材料研究所内

(72)発明者　小松　孝
千葉県山武郡山武町横田523　日本真空技術株式会社千葉超材料研究所内

(72)発明者　中村　久三
千葉県山武郡山武町横田523　日本真空技術株式会社千葉超材料研究所内

(72)発明者　桃野　健
千葉県山武郡山武町横田523　日本真空技術株式会社千葉超材料研究所内

(72)発明者　川村　裕明
千葉県山武郡山武町横田523　日本真空技術株式会社千葉超材料研究所内

(72)発明者　鈴木　郁生
千葉県山武郡山武町横田523　日本真空技術株式会社千葉超材料研究所内

(72)発明者　池田　智
千葉県山武郡山武町横田523　日本真空技術株式会社千葉超材料研究所内

(72)発明者　石川　道夫
千葉県山武郡山武町横田523　日本真空技術株式会社千葉超材料研究所内

(72)発明者　太田　賀文
千葉県山武郡山武町横田523　日本真空技術株式会社千葉超材料研究所内

(72)発明者　松本　昌弘
千葉県山武郡山武町横田523　日本真空技術株式会社千葉超材料研究所内

Derwent WPI

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WPI Acc no: 2004-222504/200421

Flywheel for radiating heat and increasing rigidity

Patent Assignee: HYUNDAI MOTOR CO LTD (HYUN-N)
Inventor: SONG J H
Patent Family: 2 patents, 1 countries

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
KR 2003088236	A	20031119	KR 200226187	A	20020513	200421	B
KR 507142	B	20050809	KR 200226187	A	20020513	200662	E

Priority Applications (no., kind, date): KR 200226187 A 20020513

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
KR 2003088236	A	KO	1	10		
KR 507142	B	KO			Previously issued patent	KR 2003088236

Alerting Abstract KR A

NOVELTY - A flywheel for radiating and reinforcing is provided to prevent crack by absorbing burst force with elastic force and radiating friction heat in operating the clutch because the flywheel is divided into plural portions and manufactured with different materials.
DESCRIPTION - A flywheel(10) is composed of a support plate(10a) combined with a crankshaft with pressing and fitting a ring gear(11); a cover plate(10b) fixed to the support plate and bent to form the storage space; an insert plate(10c) fastened inside the cover plate; and a friction plate(10d) contacted to the insert plate and inserted to the cover plate to receive clamping load from a clutch plate in operating the clutch. The durability is improved by preventing crack from burst force in the flywheel and radiating friction heat from clamping load.

(19)대한민국특허청(KR)
(12) 등록특허공보(B1)

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(73) 특허권자 현대자동차주식회사
서울 서초구 양재동 231

(72) 발명자 송진호
경기도안양시만안구박달2동139-101

(74) 대리인 한양특허법인

심사관 : 방승훈

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(54) 방열과 강성 강화용 플라이 휠

요약

본 발명은 방열과 강성 강화용 플라이 휠에 관한 것으로, 플라이휠을 서로 결합되는 여러 부분으로 분리해 제작하면서 그 재질을 달리해 버스트포스를 자체적인 탄성을 통해 흡수하면서 클러치의 조작에 따라 발생되는 마찰열의 방열성도 향상시켜 균열을 방지함에 그 목적이 있다.

상기와 같은 목적을 달성하기 위한 본 발명은, 플라이휠(10)이 링기어(11)가 외주 측에 압입되면서 크랭크축(5)에 결합되는 지지플레이트(10a)와, 이 지지플레이트(10a)에 일단이 고정되면서 절곡된 내부로 수용공간을 형성하는 커버플레이트(10b), 이 커버플레이트(10b)의 안쪽에서 고정되는 인서트플레이트(10c) 및 이 인서트플레이트(10c)에 접촉됨과 더불어 커버플레이트(10b)내에 삽입·고정되어 클러치 조작에 따라 클러치플레이트(22)로부터 클램핑 로드(F')를 받는 마찰플레이트(10d)로 이루어진 것을 특징으로 한다.

대표도

도 4

명세서

도면의 간단한 설명

도 1은 일반적인 엔진의 구성도

도 2는 종래에 따른 플라이 휠부위의 구성도

도 3은 종래에 따른 플라이휠의 구성 단면도

도 4는 본 발명에 따른 플라이휠의 구성 단면도

<도면의 주요부분에 대한 부호의 설명>

1 : 실린더 2 : 피스톤

3 : 커넥팅 로드 5 : 크랭크축

6 : 워터펌프 7 : 밸브기구

8 : 크랭크풀리 9 : 타이밍 기어

10 : 플라이휠 10a : 지지플레이트

10b : 커버플레이트 10c : 인서트플레이트

10d : 마찰플레이트 10d' : 슬랏

11 : 링기어 20 : 클러치어셈블리

21 : 클러치커버 22 : 클러치플레이트

H : 휠하우징

F' : 클램핑로드 K : 캡

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

본 발명은 방열과 강성 강화용 플라이 휠에 관한 것으로, 보다 상세하게는 엔진의 회전력에 의한 모서리부위의 균열을 방지하도록 강성을 강화함과 더불어 클러치와의 마찰에 의한 마찰열의 방열성도 향상할 수 있도록 된 방열과 강성 강화용 플라이휠에 관한 것이다.

일반적으로 엔진은 도 1에 도시된 바와 같이 실린더(1) 내에서 혼합 가스가 폭발하여 피스톤(2)이 왕복 운동되고, 상기 피스톤(2)과 커넥팅 로드(3)로 연결된 크랭크축(5)이 회전 운동되면서 회전 동력이 발생하게 된다.

또한, 상기 크랭크축(5)에는 그 선단측에 워터펌프(6) 및 밸브기구(7)를 작동하기 위한 크랭크풀리(8) 및 타이밍기어(9)가 설치되어 있고, 반대쪽에는 하우징(H)내로 수용되어 엔진의 초기 시동시에 스타트 모터의 피니언 기어와 맞물려 회전력을 전달받는 링기어(11)가 외주 측에 열 박음으로 압입되면서 클러치와 변속기에 회전 동력을 전달하는 플라이휠(10)이 설치되어 있다.

여기서, 상기 플라이휠(10)은 도 2에 도시된 바와 같이, 링기어(11)가 압입된 반대측으로 클러치페달에 의해 플라이휠(10)과 마찰되는 클러치플레이트(22)를 감싸는 클러치커버(21)로 이루어져 엔진과 변속기사이의 회전 전달을 분리·연결하는 클러치어셈블리(20)가 구비되어진다.

이러한 플라이휠(10)은 엔진의 4행정 중에서 폭발행정에서 얻어진 토크(Torque)를 흡입·압축·배기 행정에 고르게 분배하여 승차감 및 차량 출발성에 맞춘 형상으로 설계됨은 물론 엔진과 변속기를 연결하는 역할로 클러치의 용량에 맞게 설계됨은 물론이다.

그러나, 이와 같은 플라이휠(10)은 도 3에 도시된 바와 같이, 크랭크축(5)에 보울트등을 매개로 고정된 상태에서 엔진의 회전력을 변속기로 전달하기 위해 고속으로 회전하고, 또한 클러치의 조작에 따라 클러치플레이트(22)와 서로 강하게 마찰되어 엔진의 회전력을 단속하는데 이로 인해, 포트(Port)형 클러치인 경우에는 클러치플레이트(22)의 취부면과 플라이휠(10)좌면 사이의 노치(C : Notch)부위가 회전에 따른 버스트 포스(Burst Force)에 의해 균열(Crack)이 발생될 소지가 있는 문제가 있게 된다.

또한, 트럭과 버스와 같이 대형 디젤엔진을 사용하는 경우에는 플라이휠(10)의 형상도 이너시아(Inertia)값이 매우 큰 형상을 갖고 주철로 제조되는데 특히, 이와 같은 경우에는 빈번하면서 장시간동안 클러치를 조작하는 경우에는, 클러치에서 발생되는 약 250 - 300℃ 정도의 고온에 의해 플라이휠(10)의 열변형을 가져오고 이에 따른 강도 저하는 물론 균열을 발생시킬 수 있는 문제가 있게 된다.

발명이 이루고자 하는 기술적 과제

이에 본 발명은 상기와 같은 점을 감안하여 발명된 것으로, 플라이휠을 서로 결합되는 여러 부분으로 분리해 제작하면서 그 재질을 달리해 버스트포스를 자체적인 탄성을 통해 흡수하면서 클러치의 조작에 의한 마찰열의 방열성도 향상시켜 균열을 방지함에 그 목적이 있다.

상기와 같은 목적을 달성하기 위한 본 발명은, 플라이 휠이 초기 시동시 스타트 모터에 의해 회전되는 링기어를 외주면으로 압입 고정하면서 엔진의 초기 구동력 발생하는 크랭크축으로 링기어의 회전력을 전달하도록 크랭크축에 결합된 지지플레이트와,
상기 지지플레이트에 고정되면서 지지플레이트로부터 일정간격을 두도록 절곡되어 그 내부로 수용공간을 형성하는 커버플레이트,
상기 커버플레이트의 내부 수용공간인 안쪽에서 고정되는 인서트플레이트 및
상기 커버플레이트내에서 인서트플레이트에 접촉되도록 삽입·고정되어 클러치 조작 시 클러치어셈블리의 클러치플레이트에 접촉되면서 마찰력을 발생하는 마찰플레이트로 이루어진 것을 특징으로 한다.

발명의 구성 및 작용

이하 본 발명의 실시예를 첨부된 예시도면을 참조로 상세히 설명한다.

도 4는 본 발명에 따른 플라리휠의 구성 단면도를 도시한 것인바, 본 발명은 피스톤(2)의 왕복 운동을 회전운동으로 변환하는 크랭크축(5)에 결합되면서 클러치어셈블리(20)가 장착되는 플라이휠(10)이,
초기 시동시에 스타트 모터의 피니언 기어와 맞물려 회전력을 전달받는 링기어(11)가 외주 측에 열 박음으로 압입됨과 더불어 보울트등의 고정부재를 통해 크랭크축(5)에 결합되는 지지플레이트(10a)와, 이 지지플레이트(10a)에 보울트등의 고정부재를 통해 고정된 일단으로부터 서로 간격을 두도록 절곡되어 그 내부로 수용공간을 형성하는 컵 형상의 커버플레이트(10b), 이 커버플레이트(10b)의 안쪽에서 보울트등의 고정부재를 통해 고정되는 인서트플레이트(10c) 및 이 인서트플레이트(10c)에 접촉됨과 더불어 커버플레이트(10b)내에 삽입·고정되어 클러치 조작 시 클러치어셈블리(20)의 클러치플레이트(22)와 접촉되어 클램핑로드(F')가 작용되는 마찰플레이트(10d)로 이루어진다.

여기서, 상기 지지플레이트(10a)와 인서트플레이트(10c)는 주철로 이루어지는 반면, 상기 커버플레이트(10b)는 강(Steel)재질로 이루어져 플라이휠(10)에 작용하는 버스트 포스(F)를 자체적인 탄성력을 통해 흡수·완화시켜주게 된다.

또한, 상기 인서트플레이트(10c)는 클러치 조작에 따라 마찰플레이트(10d)에서 발생되는 마찰열의 전달시 열팽창에 의해 커버플레이트(10b)와의 간섭을 방지하도록 약 1.00 - 1.50mm 정도의 갭(K)을 유지하게 된다.

그리고, 상기 마찰플레이트(10d)는 클러치 조작에 따른 클러치플레이트(22)와의 마찰열을 외부로 발산하도록 그 측면 테두리를 따라 다수의 슬롯(10d')이 형성되어진다.

이하 본 발명의 작동을 첨부된 도면을 참조로 상세히 설명한다.

본 발명은 플라이휠(10)이 일체로 이루어지는 대신 여러 부품들로 이루어지는데 즉, 지지플레이트(10a)에 초기 시동시에 스타트 모터의 피니언 기어와 맞물려 회전력을 전달받는 링기어(11)를 열 박음으로 압입시킨 상태에서 커버플레이트

(10b)의 안쪽으로 보울트등의 고정부재를 이용해 인서트플레이트(10c)와 마찰플레이트(10d) 순차적으로 고정한 후, 상기 커버플레이트(10b)와 지지플레이트(10a)를 보울트등의 고정부재를 매개로 결합시킨 상태에서 크랭크축(5)에 결합하여 플라이휠(10)을 조립하게 된다.

이때, 상기 지지플레이트(10a)와 크랭크축(5)사이에는 파이롯 베어링(Pilot Bearing)이 개재됨은 물론이다.

이어, 상기 플라이휠(10)에 클러치어셈블리(20)를 결합하여 클러치 조작시 클러치플레이트(22)에 의해 플라이휠(10)의 마찰플레이트(10d)쪽으로 강하게 작용하는 클램핑로드(F')를 통해 엔진과 변속기사이의 회전력을 단속하게 된다.

이때, 본 발명의 플라이휠(10)은 클러치의 조작시 엔진의 회전에 의해 플라이휠(10)에 발생되는 버스트 포스(F)가 강재질로 이루어진 커버플레이트(10b)의 탄성력에 의해 흡수·완화되거나 또는 제거되고 이로 인해, 상기 커버플레이트(10b)의 모서리부위인 노치 부위로 집중되는 버스트 포스(F)에 의한 균열의 발생을 예방할 수 있게 된다.

또한, 본 발명의 플라이휠(10)은 클러치의 빈번한 조작에 의한 클램핑로드(F')에 의해 클러치플레이트(22)와 마찰플레이트(10d)사이에서 마찰열이 발생되면, 상기 마찰플레이트(10d)에 접촉된 인서트플레이트(10c)로 전달됨과 더불어 마찰플레이트(10d)의 측면 테두리를 따라 형성된 다수의 슬랏(10d')을 통해 보다 빠른 열의 방출이 이루어지게 된다.

이때, 상기 인서트플레이트(10c)로 전달된 마찰열이 방열되는 것보다 적층되는 것이 클 경우에는 인서트플레이트(10c)가 팽창하게 되지만, 이때 상기 인서트플레이트(10c)가 이를 수용한 커버플레이트(10b)내에서 약 1.00 - 1.50mm 정도의 갭(K)을 유지하므로 열팽창에 의한 커버플레이트(10b)와의 간섭을 방지할 수 있게 됨은 물론이다.

발명의 효과

이상 설명한 바와 같이 본 발명에 의하면, 플라이휠이 링기어가 외주 측에 압입되면서 크랭크축에 결합되는 부분과 클러치 조작에 따라 클러치플레이트로부터 클램핑 로드를 받는 부분으로 분리 제작한 후 서로 조립·결합시켜, 플라이휠이 적용되는 차종에 관계없이 플라이휠에서 발생되는 버스트포스에 의한 크랙과 클램핑로드에 따른 마찰열의 방열성을 향상시킬 수 있어 내구성을 강화할 수 있는 효과가 있게 된다.

(57) 청구의 범위

청구항 1.

초기 시동시 스타트 모터에 의해 회전되는 링기어(11)를 외주면으로 압입 고정하면서 엔진의 초기 구동력 발생하는 크랭크축(5)으로 링기어(11)의 회전력을 전달하도록 크랭크축(5)에 결합된 지지플레이트(10a)와,

상기 지지플레이트(10a)에 고정되면서 지지플레이트(10a)로부터 일정간격을 두도록 절곡되어 그 내부로 수용공간을 형성하는 커버플레이트(10b),

상기 커버플레이트(10b)의 내부 수용공간인 안쪽에서 고정되는 인서트플레이트(10c) 및

상기 커버플레이트(10b)내에서 인서트플레이트(10c)에 접촉되도록 삽입·고정되어 클러치 조작 시 클러치어셈블리(20)의 클러치플레이트(22)에 접촉되면서 마찰력을 발생하는 마찰플레이트(10d)로 이루어진 방열과 강성 강화용 플라이 휠.

청구항 2.

제 1항에 있어서, 상기 지지플레이트(10a)와 인서트플레이트(10c)는 주철로 이루어지고, 상기 커버플레이트(10b)는 탄성을 갖는 강재질로 이루진 것을 특징으로 하는 방열과 강성 강화용 플라이 휠.

청구항 3.

제 1항에 있어서, 상기 인서트플레이트(10c)는 열팽창에 의해 커버플레이트(10b)와의 간섭을 방지하도록 1.00 - 1.50mm 정도의 갭(K)을 형성하는 것을 특징으로 하는 방열과 강성 강화용 플라이 휠.

청구항 4.

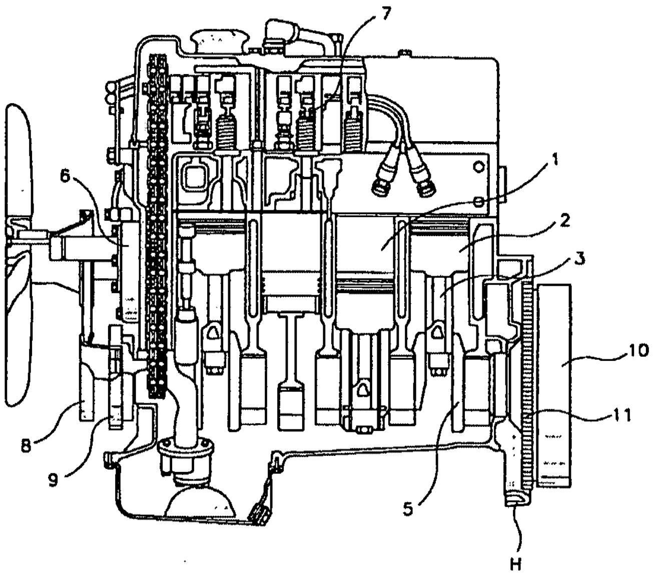
삭제

청구항 5.

제 1항에 있어서, 상기 마찰플레이트(10d)는 클러치 조작에 따른 클러치플레이트(22)와의 마찰열을 외부로 발산하도록 그 측면 테두리를 따라 다수의 슬랏(10d')이 형성되어진 것을 특징으로 하는 방열과 강성 강화용 플라이 휠.

도면

도면1



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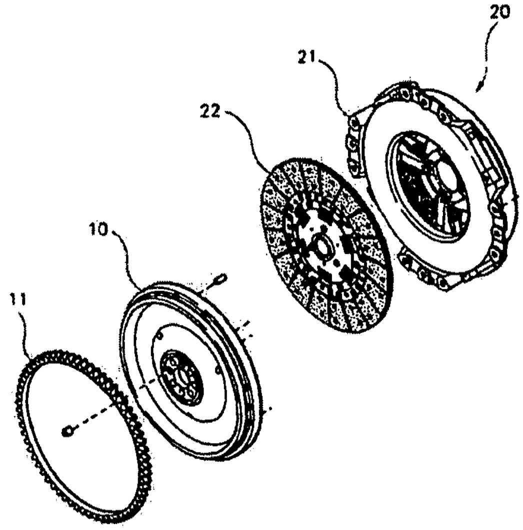

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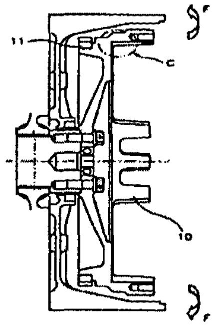

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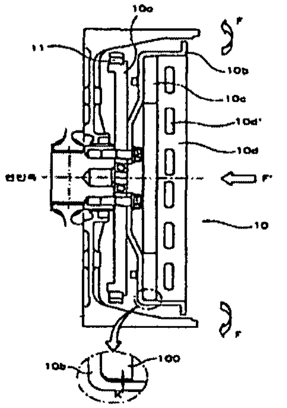

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(71) Applicant: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventor: ZHOU, Guo-Fu; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(74) Agent: DEGUELLE, Wilhelmus, H., G.; Internationaal Octrooibureau B.V., Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

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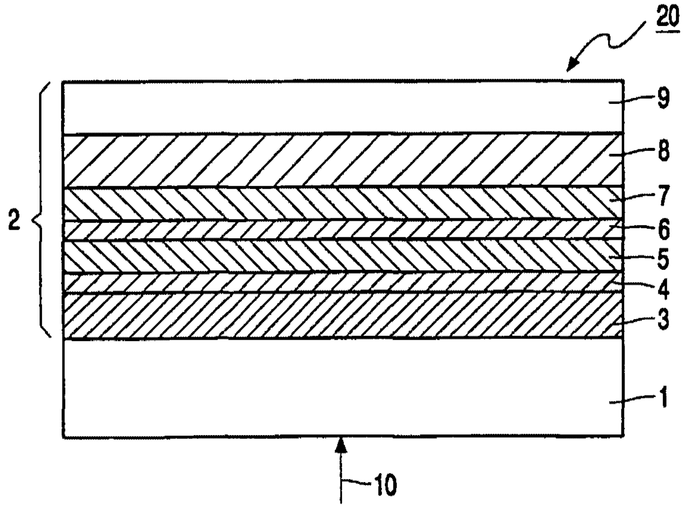
For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: OPTICAL RECORDING MEDIUM AND USE OF SUCH OPTICAL RECORDING MEDIUM



(57) Abstract: The optical recording medium (20) has a substrate (1) and a stack (2) of layers provided thereon. A phase change recording layer (5), having a melting point T_{mp} is sandwiched between a first (3) and a second (7) dielectric layer. A crystallization-accelerating layer (4, 6) is being interposed in contact with the recording layer (5). Further a reflective layer (8) is present and an optional cover layer (9). The crystallization-accelerating layer (4, 6) consists of a binary metal alloy or a semiconductor and has a melting point T_{mg} at least 250 °C higher than the melting point T_{mp} of the recording layer (5) and has a crystal structure similar to the crystalline state of the recording layer (5).

WO 01/82297 A1

Optical recording medium and use of such optical recording medium

The invention relates to an optical recording medium having a substrate and a stack of layers provided thereon, the stack comprising a recording layer, having a melting point T_{mp} and being able to change between an amorphous and a crystalline state, sandwiched between a first and a second dielectric layer, the first being adjacent to the substrate, a crystallization accelerating layer being interposed in contact with the recording layer, and a reflective layer.

The invention also relates to the use of such an optical recording medium.

An optical recording medium of the type mentioned in the opening paragraph is known from Japanese patent application JP-09161316 A. In the known medium the state of the recording layer locally changes from crystalline to amorphous when data are optically recorded.

Optical data storage based on the phase change principle is attractive, because it combines the possibilities of direct overwrite (DOW) and high storage density with easy compatibility with read-only optical data storage systems. Phase-change optical recording involves the formation of submicrometer-sized amorphous recording marks in a crystalline film using a focused relatively high power laser-light beam. During recording information, the medium is moved with respect to the focused laser-light beam that is modulated in accordance with the information to be recorded. Due to this, quenching takes place in the phase-change recording layer and causes the formation of amorphous information bits in the exposed areas of the recording layer that remains crystalline in the unexposed areas. Erasure of written amorphous marks is realized by recrystallizing through heating with the same laser at an intermediate power level, without melting the recording layer. The amorphous marks represent the data bits, which can be read, e.g. via the substrate, by a low-power focused laser-light beam. Reflection differences of the amorphous marks with respect to the crystalline recording layer bring about a modulated laser-light beam which is subsequently converted by a detector into a modulated photocurrent in accordance with the recorded digital information.

One of the most important demands in phase-change optical recording is a high data rate, which means that data can be written in and read from the medium with a rate of at least 30Mbits/s. A high data rate requires the recording layer to have a high crystallization rate, i.e. a short crystallization time. To ensure that the previously recorded amorphous marks can be crystallized during direct overwrite, the recording layer should have a proper crystallization time to match the velocity of the medium relative to the laser-light beam. If the crystallization speed is not high enough to match the velocity of the medium relative to the laser-light beam the amorphous marks from the previous recording, representing old data, cannot be completely erased, meaning recrystallized, during DOW. This causes a high noise level. A high crystallization speed is particularly required in high-density recording and high data rate applications, such as disc-shaped DVD+RW, DVR-red and blue which are abbreviations of new generation high density Digital Versatile Disc+RW, where RW refers to the rewritability of such discs, and Digital Video Recording optical storage discs, where red and blue refer to the used laser wavelength. For these new discs the complete erasure time (CET) has to be at most 60 ns. CET is defined as the minimum duration of the erasing pulse for complete crystallization of a written amorphous mark in a crystalline environment, which is measured statically. For DVD+RW, which has a 4.7 GB recording density per 120 mm disk, a user data bit rate of 33 Mbits/s is needed, and for DVR-red said rate is 35 Mbits/s. For rewritable phase change optical recording systems such as DVR-blue, a user data rate higher than 50 Mbits/s is required.

The known medium of the phase-change type comprises a disc-shaped substrate carrying a stack of layers consisting, in succession, of a first dielectric layer, a Sb_2Te_3 layer as crystallization accelerating layer, a Sb layer as a composition correcting layer, a recording layer of a phase-change $Sb_{72}Te_{28}$ alloy, a second dielectric layer and a metal reflective layer. Such a stack of layers can be referred to as an INP'PIM structure, wherein M represents a reflective or mirror layer, I represents a dielectric layer and P represents a phase-change recording layer while P' represents a composition correction layer which mixes with the recording layer at first recording. A crystallization accelerating layer N of Sb_2Te_3, has been arranged between the first dielectric layer and the correction and the recording layer to achieve a fast crystallization of the medium during erasing information in the medium by means of a laser-light beam. In the known recording medium the N layer has a melting point of 618°C, only 68°C higher than the melting point 550°C of the P layer. The melting point of the known N layer is relatively close to the melting point of the P layer causing the N layer to dissolve in the correction and recording layer P'P after one or at best a few recording/erasure cycles, whereafter the crystallization accelerating layer N is no longer present and its crystallization-accelerating action is lost.

For complete erasure of an amorphous mark, two processes occur, i.e. nucleation and grain (crystallite) growth. An investigation of the known recording medium has revealed that the known crystallization-accelerating layer N is merely a nucleation-promoting layer.

It is a disadvantage of the known medium that its crystallization accelerating layer only functions for at most a few recording and erasing cycles. This is not sufficient for modern erasable media, which require a stable performance for at least a thousand of recording and erasing cycles.

It is an object of the invention to provide an optical recording medium of the kind described in the opening paragraph, which is suitable for high speed rewritable optical recording, having a CET-value of at most 60 ns.

It is another object of the invention to provide an optical recording medium of the kind described in the opening paragraph, which is suitable for rewritable optical recording, having a stable performance for at least 10^3 recording and erasing cycles.

This object is achieved in accordance with the invention by an optical recording medium as described in the opening paragraph, which is characterized in that the crystallization accelerating layer

- comprises a material selected from the group consisting of binary metal alloys, semiconductors elements and semiconductor alloys and
- has a melting point T_{mg} at least 250°C higher than the melting point T_{mp} of the recording layer and
- has a crystal structure similar to the crystalline state of the recording layer.

The crystallization accelerating layer according to the invention, which will also be abbreviated as G, yields a high crystallization speed of the recording layer because the amorphous marks of the recording layer are in contact with the G-layer. This accelerates the crystallite growth process, leading to a higher crystallization speed. Especially because the crystal structure of the G-layer is similar to, or even the same as, the structure of the crystalline state of the recording layer the crystallization rate of amorphous marks is advantageously increased. The crystal structure of the G-layer then serves as a very good grain growth initialization or nucleation layer for crystallite growth in the recording layer.

The G-layer is always present adjacent to a thermally isolating layer, here the first or second dielectric layer, because a stack having a G-layer between the recording layer and the substrate or the reflection layer cannot realize the desired thermal properties.

An advantage of the G-layer, comprising a material selected from the group consisting of binary metal alloys, semiconductors and semiconductor alloys, is that it has a high melting point. This counteracts dissolving of the G-layer in the recording layer and maintenance of the crystalline structure for a large number of recording and erasing cycles. During recording, the maximum temperature in the recording layer is about 800°C, which is about 1.4 times T_{mp} for a recording layer with a T_{mp} of 550°C. This may be deduced from a temperature calculation based on the presented laser energy during recording and the physical properties of the stack. The melting temperature T_{mg} of the G-layer has to be above this maximum temperature so that the G-layer remains in crystalline state when the recording layer is melted.

Therefore, the melting temperature difference between recording layer and G-layer should be 250°C or larger, but preferably 300°C or larger, taking into consideration a safety margin.

Preferred materials, which may be used as G-layer, are PbTe, Ag_2Te, CrTe, Ge and Si.

In an embodiment of the recording medium the G-layer is arranged between the recording layer and the second dielectric layer. The thickness of the G-layer may be chosen between 0.1 and 10 nm. The thermal conductivity of the crystallization-accelerating layer is generally comparable to that of the recording layer, which is an alloy of metals. However this only has a small effect on the thermal behaviour of the stack because the thickness of the G-layer is generally relatively small compared to the other layers in the stack. This facilitates the thermal design of the stack.

In another embodiment the crystallization time is reduced further in that a second G-layer is arranged between the recording layer and the first dielectric layer. Thus a G-layer is arranged on both sides of the recording layer. The second G-layer may be of a material similar or identical to the material of the other G-layer. The crystallization time is reduced because now a crystalline layer, which accelerates the crystallite growth process, is present against the recorded amorphous mark on both sides. The thicknesses of the G-layers are between 0.1 and 10nm, preferably lower than 5 nm.

In a specific embodiment the two G-layers present on either side of the recording layer are substantially equal both in thickness and in composition. Equal in thickness means to within 10% of each other. The equality of the thicknesses is advantageous in the manufacturing of the medium. In general the stack is deposited by evaporation or by sputtering in a vacuum chamber, where substrates move stepwise along a series of stations having targets of different compositions. The dwell time at each station is about equal, and the thickness of the layer deposited at a station is determined in part by switching the deposition process on and off. Consequently, the deposition of a relatively thin layer may require less time than available at a station, whereas the deposition of a relatively thick layer may even require two adjacent stations having the same target. It is therefore advantageous to choose to replace a relatively thick layer and a relatively thin layer by two layers of about equal thickness and composition, thereby reducing the number of deposition stations and the manufacturing time of a stack.

In a specific embodiment the recording layer comprises an alloy of Q, In, Sb and Te, wherein Q is selected from the group consisting of Ag and Ge.

The preferred composition comprises $Q_a In_b Sb_c Te_d$ (in atomic percentages), wherein Q is selected from the group consisting of Ag and Ge;

$2 \leq a \leq 9$

$0 < b \leq 6$

$55 \leq c \leq 80$

$16 \leq d \leq 30; a + b + c + d = 100.$

In another specific embodiment the recording layer comprises a compound of Ge, Sb and Te. The preferred composition of this compound is defined by the formula

$Ge_{50x}Sb_{40-40x}Te_{60-10x}$ (in atomic percentages), wherein $0.166 \leq x \leq 0.444$;

the recording layer having a thickness of 5 to 35 nm;

This composition exists on a part of the line connecting the compounds GeTe and Sb_2Te_3 in the triangular Ge-Sb-Te composition diagram and includes the stoichiometric compounds $Ge_2Sb_2Te_5$ ($x = 4/9$), $GeSb_2Te_4$ ($x = 2/7$) and $GeSb_4Te_7$ ($x = 1/6$). Especially these ternary stoichiometric compounds are preferred, because these materials crystallize rapidly since no segregation is required during crystallization.

The first and second dielectric layers are preferably made of a mixture of ZnS and SiO_2, e.g. $(ZnS)_{80}(SiO_2)_{20}$. The layers may alternatively be made of SiO_2, TiO_2, Ta_2O_5, ZnS, AlN and/or Si_3N_4. The dielectric layer through which the laser light enters the stack preferably has a thickness of 70 to $(70+\lambda/2n)$ nm wherein n is the refractive index of the first dielectric layer and λ is the wavelength of the read/write laser-light beam. If the total thickness is smaller than 70 nm, the cyclability is reduced considerably. The cyclability is measured by the relative change of the optical contrast M_0 after a large number of DOW-cycles, e.g. 10^3. The optical contrast M_0 is defined as $|R_C-R_A|/R_C$, where R_C and R_A are the reflections of the recording material in the crystalline and amorphous state respectively. Another way to define cyclability is related to jitter increase of the medium. Jitter is a measure of the distortion of the shape of a recording mark, and is measured as a time shift of rising and falling edges in the information signal. The jitter of the medium should be at a low, constant level during at least 10^3 DOW-cycles.

As mentioned above the total thickness of the first dielectric layer is preferably smaller than $(70+\lambda/2n)$ nm. A larger total thickness does not further increase the cyclability and is more expensive to make. If for example the wavelength is equal to 630 nm and the refractive index is 1.5, the thickness range extends from 70 nm to 280 nm.

The dielectric layer, which is closest to the reflective layer, has a thickness of 10 to 40 nm. Preferably the thickness of the dielectric layer adjacent to the reflective layer is larger than or equal to 15 nm. A smaller thickness results in an increased cooling rate of the recording layer and, consequently, an undesirable increase in the write power. The thickness is preferably smaller than 40 nm. A larger thickness decreases the thermal contact between the recording layer and the reflective layer too much, resulting in too low a cooling rate of the recording layer and a worse recording performance.

The reflective layer may comprise metals such as Al, Ti, Au, Ni, Cu, Ag and Cr, and alloys of these metals. The reflective layer preferably has a thickness of 60 to 120 nm.

Both the reflective layers and the dielectric layers generally have been provided by vapour deposition or sputtering.

Optionally an outermost layer may be present on the stack as a cover layer that protects the underlying layers from the environment. The cover layer is made of, for example, an UV light-cured poly(meth)acrylate.

Another specific embodiment is characterized in that the reflective layer is present between the substrate and the first dielectric layer. Optionally a cover layer, that is transparent for laser-light and has a surface which allows optical recording of information into and reading of information from the underlying recording layer with a focused laser-light beam is present on top of the stack. Thus in this embodiment the optical recording medium is written in and read out through the cover layer. This method is used in the new DVR discs that were mentioned above. The cover layer of a DVR disc has a thickness of about 100 micrometers. This cover layer allows the use, in optical disc recorders, of a read/write lens with a high numerical aperture that is necessary for high density recording and reading. Because the laser light enters the medium through the cover layer it may be necessary to adjust the thicknesses of the layers of the stack in order to optimize for optimal optical contrast between recorded and unrecorded areas.

The term high-speed recording, which was mentioned above, is to be understood to mean in this context a linear velocity of the medium relative to the laser-light beam of at least 7.2 m/s, which is six times the speed according to the Compact Disc standard. The use of an optical recording medium according to the invention is therefore advantageous because the crystallization rate is fast enough to permit at least this recording velocity. The important parameter is the CET (in ns), which is defined above. The CET is inversely proportional to the crystallization rate.

The substrate of the information medium generally is transparent to the laser wavelength, and is made, for example, of polycarbonate, polymethyl methacrylate (PMMA), amorphous polyolefin or glass. In a typical example, the substrate is disc-shaped and has a diameter of 120 mm and a thickness of 1.2 mm, 0.6 mm or 0.1 mm for respectively low, medium and high information density applications.

Alternatively, the substrate may be in the form of a synthetic resin flexible tape, made e.g. from a polyester film. This flexible tape, with a stack of layers deposited thereon, is called an optical tape and can be suited for use in an optical tape recorder, which is for example based on a fast spinning polygon. In such a device the reflected laser-light beam scans transversely across the tape surface.

The surface of the disc-shaped substrate on the side of the recording layer is, preferably, provided with a servotrack that can be scanned optically. This servotrack is often constituted by a spiral-shaped groove and is formed in the substrate by means of a mould during injection moulding or pressing. This groove can be alternatively formed in a replication process in a synthetic resin layer, for example, of an UV light-cured layer of acrylate, which is separately provided on the substrate. In high-density recording such a groove has a pitch e.g. of 0.5 - 0.8 μm and a width of about half the pitch.

High-density recording and erasing can be achieved by using a short-wavelength laser, e.g. with a wavelength of 675 nm or shorter (red to blue).

The phase change recording layer as well as the G-layer can be applied by vapour depositing or sputtering of a suitable target. The recording layer thus deposited is amorphous and exhibits a low reflection. In order to constitute a suitable recording layer having a high reflection, this layer must first be completely crystallized, which is commonly referred to as initialization. For this purpose, the recording layer can be heated in a furnace to a temperature just above the crystallization temperature of the e.g. Ge-In-Sb-Te or Ge-Sb-Te compound, e.g. 200°C. A synthetic resin substrate, such as polycarbonate, to which a high temperature may cause damage, can alternatively be heated by a laser-light beam of sufficient power. This can be realized, e.g. in a recorder, in which case a laser beam scans the moving recording layer. The amorphous layer is then locally heated to the temperature required for crystallizing the layer, without the substrate being subjected to a disadvantageous heat load.

If desired, an additional, optically transparent, metal layer M' can be interposed in the stack, thereby forming a so called MIRIM'-structure, wherein R represents a layer stack comprising a recording layer and at least one crystallization accelerating layer according to the present invention. Although the structure becomes more complicated, the additional metal layer increases the cooling rate of the recording layer as well as the optical contrast M_0.

Embodiments of the optical recording medium of the invention will be described with reference to the drawings.

In the drawings:

Fig. 1 shows a schematic cross sectional view of a first embodiment of the optical recording medium.

Fig. 2. shows a view as shown in FIG.1 of a second embodiment.

Fig. 3 shows a view as in FIG.2 of a third embodiment.

In Fig. 1 the optical recording medium 20 has a substrate 1 and a stack 2 of layers provided thereon. The substrate 1 may be made of, for example, a sheet of plastic, e.g. polycarbonate, or glass. In Fig. 1 the stack 2 comprises a phase change recording layer 5, having a melting point T_{mp} and being able to change between an amorphous and a crystalline state, that is sandwiched between a first 3 and a second 7 dielectric layer, the first 3 being adjacent to the substrate 1. In this embodiment both the first dielectric layer 3 and the second dielectric layer 7 are made of the material $(ZnS)_{80}(SiO_2)_{20}$ and have a thickness of 125 nm and 20 nm respectively. A crystallization accelerating layer 6, abbreviated as G-layer, is interposed in contact with the recording layer 5, which comprises an alloy of Q, In, Sb and

Te, wherein Q is selected from the group consisting of Ag and Ge. A reflective layer 8 is present on top of the stack 2. Reflective layer 8 is a 100 nm layer of Al or an aluminium alloy, e.g. AlCr or AlTi. The crystallization accelerating layer 6 comprises a binary metal alloy or a semiconductor element or semiconductor alloy and has a melting point T_{mg} at least 250°C higher than the melting point T_{mp} of the recording layer 5. The crystal structure of these materials is similar to the crystalline state of the recording layer 5. In this embodiment the recording layer 5 is made of $Ge_{6.2}In_{3.2}Sb_{71.1}Te_{19.6}$, which has a thickness of 12 nm. The embodiment shown has a cover layer 9 that may be made of an organic material, e.g. a UV-cured resin. A focused laser-light beam with a wavelength λ=405 nm enters the medium through the substrate 1. This beam is diagrammatically illustrated by means of an arrow 10 in Fig. 1.

In this embodiment, when using PbTe as G-layer, which has a thickness of 3 nm, the CET has been measured to be equal to 40 ns, which is sufficiently short to allow high-speed recording. When no G-layer is present a minimal CET value of 48 ns can be obtained. Other preferred materials as G-layer are Ag_2Te, CrTe, Ge or Si. The melting points T_{mg} of bulk PbTe, Ag_2Te, CrTe, Ge and Si are 914, 960, 1292, 936 and 1414°C respectively. The write power for the medium is relatively low and is 9 mW at the entrance face of the medium at a relative speed between the radiation beam and the medium of 7.2 m/s. The R_A and R_C are measured to be 4.3% and 23% respectively.

The cyclability is measured as the number of rewrite cycles where the jitter has increased to 12% of the clock time T_C. The jitter is the standard deviation of the difference between the rising and falling edges in the information signal and the data clock recovered from the information signal. As an example, for a standard CD format written with the so-called EFM code at the CD speed of 1.2 m/s and clock time of 230 ns, the jitter should be lower than 28 ns. The number of overwrite cycles before deterioration of the medium becomes noticeable, e.g. the jitter has increased to 12% of the clock time, is larger than 10^3. The jitter of a pattern read from the medium as a function of the overwrite cycle does not show a large overshoot.

During writing, the recording layer 5 of $Ge_{6.2}In_{3.2}Sb_{71.1}Te_{19.6}$ is heated to a temperature of about 750°C, well above its melting temperature, which is about 550°C. The temperature during recording is below the melting temperature of the G-layer 6 comprising PbTe. The high melting temperature of the material used for the G-layer neighbouring the recording layer 5 therefore results in an increased cyclability of the recording medium.

In application JP-09161316 A the crystallization accelerating layer N of Sb_2Te_3, which has a melting point of 618°C, is thus heated above its melting temperature, causing the atoms in the layer to become mobile. These atoms are then able to diffuse into the recording layer. The properties of the recording layer are affected by the influx of foreign atoms, resulting in a deterioration of the recording process.

In Fig. 2 and Fig. 3 corresponding reference numerals denote the same layers as in Fig. 1.

In Fig. 2 a second crystallization accelerating layer 4 similar to the crystallization accelerating layer 6 is arranged between the recording layer 5 and the first dielectric layer 3. Now G-layers 4, 6 are present on both sides adjacent to the recording layer 5. The G-layer 6 is made of PbTe and has a thickness of 1.5 nm. The second G-layer 4 is substantially equal both in thickness and in composition to the G-layer 6. The recording layer 5 has a thickness of 10 nm. Further the characteristics of the stack 2 are the same as in Fig. 1. The CET is measured to be 36 ns. The CET in this embodiment is smaller than in the embodiment with only one G-layer. The R_A and R_C are measured to be 4.6% and 22% respectively.

In Fig. 3 the reflective layer 8 is present between the substrate 1 and the first dielectric layer 3. In this embodiment the laser light 10 is entering the stack 2 through the cover layer 9 which has a thickness of 100 μm. The cover layer 9 has a uniform thickness, thereby improving the optical read and write performance in underlying recording layers when the read or write laser beam passes through said cover layer 9. For example a 100 μm cover layer 9 is used for the new 60 mm radius Digital Video Recording (DVR) disc. This disc is recorded in and read out through this cover layer 9, which therefore has to be of good optical quality. Preferably, the cover layer 9 is 100+/-3 μm thick up to radius 58.5 mm. The cover layer 9 is made from a UV-cured resin. Dielectric layer 3 and 7 have a thickness of 20 nm and 125 nm respectively and are made of the same dielectric material as in Fig. 1. G-layer 4, 6 are made of the same material as in Fig. 2 and both have a thickness of 1.5 nm. Recording layer 5 has a thickness of 10 nm. For characteristics that are not specifically mentioned reference is made to the description of Fig. 1.

Preferably, for all embodiments, the surface of the disc-shaped substrate 1 on the side of the stack 2 is provided with a servotrack that can be scanned optically. This servotrack is often constituted by a spiral-shaped groove and is formed in the substrate by means of a mould during injection moulding or pressing. This groove can be alternatively formed in a replication process in a synthetic resin layer, for example, of an UV light-cured layer of acrylate, which is separately provided on the substrate 1. In high-density recording such a groove has a pitch e.g. of 0.5 - 0.8 μm and a width of about half the pitch.

In a modification of the recording medium of Fig. 3, the recording layer 5 comprises an alloy of Ge, Sb and Te, e.g. $Ge_2Sb_2Te_5$.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word "comprising" does not exclude the presence of elements or steps other than those listed in a claim. The word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

According to the invention an optical recording medium is provided, which is suitable for high speed recording, e.g. with a possible data rate higher than 50 Mbits/s, and which is suitable for direct overwrite for a least 10^3 times.

CLAIMS:

1. An optical recording medium (20) having a substrate (1) and a stack (2) of layers provided thereon, the stack comprising a recording layer (5), having a melting point T_{mp} and being able to change between an amorphous and a crystalline state, sandwiched between a first (3) and a second (7) dielectric layer, the first (1) being adjacent to the substrate (1), a crystallization accelerating layer (4, 6) being interposed in contact with the recording layer (5), and a reflective layer (8), characterized in that the crystallization accelerating layer (4, 6)

- comprises a material selected from the group consisting of binary metal alloys, semiconductors elements and semiconductor alloys and
- has a melting point T_{mg} at least 250°C higher than the melting point T_{mp} of the recording layer (5) and
- has a crystal structure similar to the crystalline state of the recording layer (5).

2. An optical recording medium (20) as claimed in Claim 1 characterized in that the crystallization accelerating layer (4, 6) comprises a material selected from the group consisting of PbTe, Ag_2Te, CrTe, Ge and Si.

3. An optical recording medium (20) as claimed in any of Claims 1 or 2, characterized in that the crystallization accelerating layer (6) is arranged between the recording layer (5) and the second dielectric layer (7).

4. An optical recording medium (20) as claimed in Claim 3, characterized in that a second crystallization accelerating layer (4) similar to the crystallization accelerating layer (6) is arranged between the recording layer (5) and the first dielectric layer (3).

5. An optical recording medium (20) as claimed in Claim 4, characterized in that the second crystallization accelerating layer (4) is substantially equal both in thickness and in composition to the crystallization accelerating layer (6).

6. An optical recording medium (20) as claimed in Claim 1, characterized in that the recording layer (5) comprises an alloy of Q, In, Sb and Te, wherein Q is selected from the group consisting of Ag and Ge

7. An optical recording medium (20) as claimed in Claim 1, characterized in that the recording layer (5) comprises an alloy of Ge, Sb and Te.

8. An optical recording medium (20) as claimed in Claim 1, characterized in that the reflective layer (8) is present between the substrate (1) and the first dielectric layer (3).

9. The use of an optical recording medium (20), which medium is claimed in any one of the preceding claims, characterized in that the linear velocity of the medium relative to a laser-light beam (10) is at least 7.2 m/s.

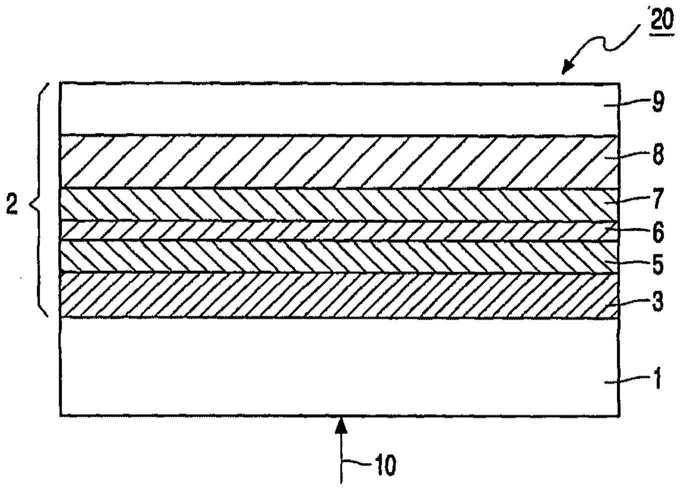


FIG. 1

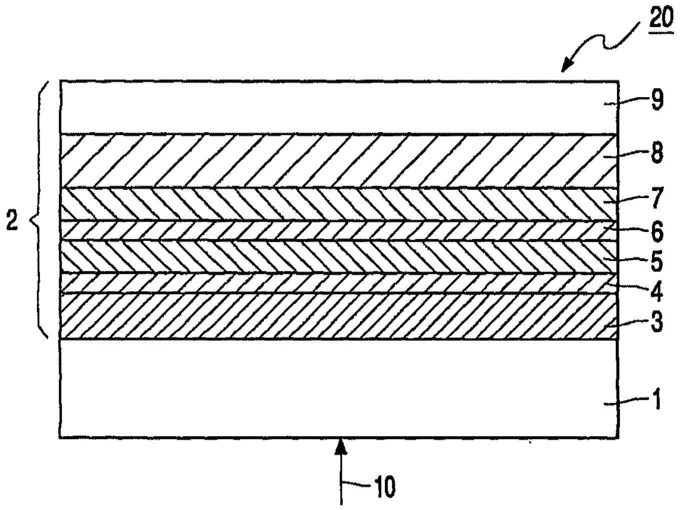


FIG. 2

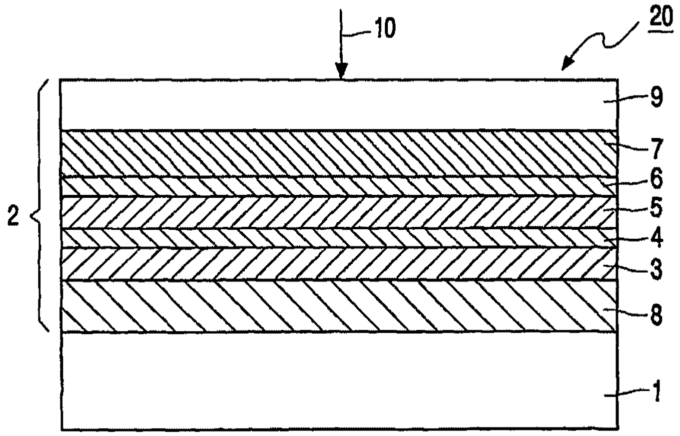


FIG. 3

INTERNATIONAL SEARCH REPORT

Ir tional Application No
PCT/EP 01/04028

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11B7/24

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G11B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 980 068 A (ASAHI CHEMICAL IND) 16 February 2000 (2000-02-16) abstract paragraph '0012! - paragraph '0019! paragraph '0038!; figure 1	1,2,7
Y		8
A		3,4,9

Y	EP 0 431 489 A (HITACHI LTD) 12 June 1991 (1991-06-12) column 16, line 28 - line 56; figure 18	8

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☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
"&" document member of the same patent family

Date of the actual completion of the international search
8 August 2001

Date of mailing of the international search report
16/08/2001

Name and mailing address of the ISA
European Patent Office, P.B. 5818 Patentlaan 2
NL – 2280 HV Rijswijk
Tel. (+31–70) 340–2040, Tx. 31 651 epo nl,
Fax: (+31–70) 340–3016

Authorized officer
Annibal, P

INTERNATIONAL SEARCH REPORT

Ii   itional Application No
PCT/EP 01/04028

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 945 860 A (MATSUSHITA ELECTRIC IND CO LTD) 29 September 1999 (1999-09-29) abstract paragraph '0017! paragraph '0018! paragraph '0034! paragraph '0035! paragraph '0050! paragraph '0084!; figures 1,2	1,3-7,9
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INTERNATIONAL SEARCH REPORT

Information on patent family members

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(71) Applicant (*for all designated States except US*): SYMMORPHIX, INC. [US/US]; 1278 Reamwood Avenue, Sunnyvale, CA 94089-2233 (US).

(72) Inventors; and
(75) Inventors/Applicants (*for US only*): DEMARAY, Richard, Ernest [US/US]; 190 Fawn Lane, Portola Valley, CA 94028 (US). NARASIMHAN, Mukundan [IN/US]; 293 Bluefield Drive, San Jose, CA 91536 (US).

(74) Agent: GARRETT, Arthur, S.; Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P., 1300 I Street N.W., Washinton, D.C. 20005-3315 (US).

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(54) Title: TRANSPARENT CONDUCTIVE OXIDES

(57) Abstract: A method of deposition of a transparent conductive film from a metallic target is presented. A method of forming a transparent conductive oxide film according to embodiments of the present invention include depositing the transparent conductive oxide film in a pulsed DC reactive ion process with substrate bias, and controlling at least one process parameter to affect at least one characteristic of the conductive oxide film. The resulting transparent oxide film, which in some embodiments can be an indium-tin oxide film, can exhibit a wide range of material properties depending on variations in process parameters. For example, varying the process parameters can result in a film with a wide range of resistive properties and surface smoothness of the film.

Transparent Conductive Oxides

Related Applications

[0001] The present application claims priority to U.S. Provisional Application 60/473,379, "Transparent Conductive Oxides from a Metallic Target," by R. Ernest Demaray and Mukundan Narasimhan, filed on May 23, 2003, herein incorporated by reference in its entirety.

Background

1. Field of the Invention

[0002] The present invention is related to deposition of oxides on a substrate and, in particular, deposition of transparent conductive oxides.

2. Discussion of Related Art

[0003] Transparent conductive oxides have a wide variety of uses, including applications to solar cells, organic light emitting diodes (OLEDs), electric field devices, current devices (i.e. touch screens), energy efficient windows, conductive anti-reflective devices, electromagnetic interference shields, heaters, transparent electrodes, coatings for cathode ray tube (CRT) displays, to name only a few. Another important application is for touch sensitive MEMS devices, such as those used, for example, in fingerprint sensors and such. In many cases, the electrical properties of the conducting film is of great importance.

[0004] Specifically, for OLED applications, films deposited with current technologies are generally rough, resulting in stress risers and field concentration issues, that can cause leakage. Further, asperities in the resulting film can induce lifetime dependent defects in nearest neighbor films that can shorten device lifetimes. Additionally, the brightness of the emergent light from the OLED can be reduced.

[0005] Transparent conductive oxides have been deposited from ceramic targets by RF magnetron sputtering. However, the surface of properties of the resulting films often include nodules or asperites which can cause arcing, defects, surface roughness, and other deleterious effects in the resulting film. Additionally, ceramic targets tend to be more expensive to produce than metallic targets.

[0006] Previous attempts at deposition of transparent conductive oxides, for example indium tin oxide (ITO), with metallic targets have presented numerous problems, including small process windows, problems in process controllability, a disappearing anode effect, and particle deposition on the film. Such attempts have been abandoned. Deposition with ceramic targets has also been difficult, including problems with particles, nodule formation, and arching during deposition. In both cases, film smoothness has presented major difficulties. Additionally, control of film parameters such as, for example, resistivity and transparency has been difficult.

[0007] Therefore, there is need for cost effective deposition of smoother layers of transparent conductive oxides with greater control over layer properties such as resistivity and transparency.

Summary

[0008] In accordance with the present invention, a method of depositing of a transparent conductive film from a metallic target is presented. A method of forming a transparent conductive oxide film according to embodiments of the present invention includes depositing the transparent conductive oxide film in a pulsed DC reactive ion process with substrate bias, and controlling at least one process parameter to provide at least one characteristic of the conductive oxide film at a particular value.

[0009] A method of depositing a transparent conductive oxide film on a substrate according to some embodiments of the invention, then, includes placing the substrate in a reaction chamber, adjusting power to a pulsed DC power supply coupled to a target in the reaction chamber, adjusting an RF bias power coupled to the substrate, adjusting gas flow into the reaction chamber, and providing a magnetic field at the target in order to direct deposition of the transparent conductive oxide film on the substrate in a pulsed-dc biased reactive-ion deposition process, wherein the transparent conductive oxide film has a particular characteristic.

[0010] The resulting transparent oxide film, which can be deposited according to some embodiments of the present invention, can be an indium-tin oxide (ITO) film. An ITO film can have a wide range of material properties depending on variations in process parameters. For example, varying the process parameters according to some embodiments of the present invention can result in a wide range of resistive properties and surface smoothness of the film.

[0011] These and other embodiments of the invention are further discussed below with reference to the following figures.

Short Description of the Figures

[0012] Figures 1A and 1B illustrate a pulsed-DC biased reactive ion deposition apparatus that can be utilized in the methods of depositing according to the present invention.

[0013] Figure 2 shows an example of a target that can be utilized in the reactor illustrated in Figures 1A and 1B

[0014] Figure 3A shows an Atomic Force Microscopy (AFM) image of an indium-tin-oxide (ITO) process according to some embodiments of the present invention.

[0015] Figure 3B shows an Atomic Force Microscopy (AFM) image of another ITO process deposited using a process according to some embodiments of the present invention.

[0016] Figure 4 shows the variation of bulk resistivity of an ITO layer according to some embodiments of the present invention as a function of the oxygen flow for two different target powers before and after a 250 °C anneal in vacuum.

[0017] Figure 5 shows the variation of the sheet resistance of an ITO layer according to some embodiments of the present invention as a function of the oxygen flow used for two different target powers before and after a 250 °C anneal in vacuum.

[0018] Figure 6 shows the target current and voltage (min and max) as a function of oxygen flow.

[0019] Figure 7 shows the thickness change in layers of ITO according to embodiments of the present invention as a function of oxygen flow.

[0020] Figure 8 illustrates the relationship between oxygen flow and oxygen partial pressure for a metallic target.

[0021] Figures 9A-9D illustrate the smoothness of transparent conductive oxides deposited with ceramic targets according to the present invention.

[0022] In the figures, elements having the same designation have the same or similar function.

Detailed Description

[0023] Deposition of materials by pulsed-DC biased reactive ion deposition is described in U.S. Patent Application Serial No. 10/101863, entitled "Biased Pulse DC Reactive Sputtering of Oxide Films," to Hongmei Zhang, et al., filed on March 16, 2002. Preparation of targets is described in U.S. Patent Application Serial No. 10/101,341, entitled "Rare-Earth Pre-Alloyed PVD Targets for Dielectric Planar Applications," to Vassiliki Milonopoulou, et al., filed on March 16, 2002. U.S. Patent Application Serial No. 10/101863 and U.S. Patent Application Serial No. 10/101,341 are each assigned to the same assignee as is the present disclosure and each is incorporated herein in their entirety. Deposition of oxide materials has also been described in U.S. Patent No. 6,506,289, which is also herein incorporated by reference in its entirety. Transparent oxide films are deposited utilizing processes similar to those specifically described in U.S. Patent No. 6,506,289 and U.S. Application Serial No. 10/101863.

[0024] Figure 1A shows a schematic of a reactor apparatus 10 for sputtering material from a target 12 according to the present invention. In some embodiments, apparatus 10 may, for example, be adapted from an AKT-1600 PVD (400 X 500 mm substrate size) system from Applied Komatsu or an AKT-4300 (600 X 720 mm substrate size) system from Applied Komatsu, Santa Clara, CA. The AKT-1600 reactor, for example, has three deposition chambers connected by a vacuum transport chamber. These Komatsu reactors can be modified such that pulsed DC power is supplied to the target and RF power is supplied to the substrate during deposition of a material film.

[0025] Apparatus 10 includes target 12 which is electrically coupled through a filter 15 to a pulsed DC power supply 14. In some embodiments, target 12 is a wide area sputter source target, which provides material to be deposited on a substrate 16. Substrate 16 is positioned parallel to and opposite target 12. Target 12 functions as a cathode when power is applied to it and is equivalently termed a cathode. Application of power to target 12 creates a plasma 53. Substrate 16 is capacitively coupled to an electrode 17 through an insulator 54. Electrode 17 can be coupled to an RF power supply 18. A magnet 20 is scanned across the top of target 12.

[0026] For pulsed reactive dc magnetron sputtering, as performed by apparatus 10, the polarity of the power supplied to target 12 by power supply 14 oscillates between negative and positive potentials. During the positive period, the insulating layer on the surface of target 12 is discharged and arcing is prevented. To obtain arc free deposition, the pulsing frequency exceeds a critical frequency that can depend on target material, cathode current and reverse time. High quality oxide films can be made using reactive pulse DC magnetron sputtering as shown in apparatus 10.

[0027] Pulsed DC power supply 14 can be any pulsed DC power supply, for example an AE Pinnacle plus 10K by Advanced Energy, Inc. With this DC power supply, up to 10 kW of pulsed DC power can be supplied at a frequency of between 0 and 350 KHz. The reverse voltage can be 10% of the negative target voltage. Utilization of other power supplies can lead to different power characteristics, frequency characteristics and reverse voltage percentages. The reverse time on this embodiment of power supply 14 can be adjusted between 0 and 5 μs.

[0028] Filter 15 prevents the bias power from power supply 18 from coupling into pulsed DC power supply 14. In some embodiments, power supply 18 can be a 2 MHz RF power supply, for example a Nova-25 power supply made by ENI, Colorado Springs, Co.

[0029] In some embodiments, filter 15 can be a 2 MHz sinusoidal band rejection filter. In some embodiments, the band width of the filter can be approximately 100 kHz. Filter 15, therefore, prevents the 2 MHz power from the bias to substrate 16 from damaging power supply 18.

[0030] However, both RF and pulsed DC deposited films are not fully dense and may have columnar structures. Columnar structures can be detrimental to thin film applications. By applying a RF bias on wafer 16 during deposition, the deposited film can be densified by energetic ion bombardment and the columnar structure can be substantially eliminated.

[0031] In the AKT-1600 based system, for example, target 12 can have an active size of about 675.70 X 582.48 by 4 mm in order to deposit films on substrate 16 that have dimension about 400 X 500 mm. The temperature of substrate 16 can be held at between -50 °C and 500 °C. The distance between target 12 and substrate 16 can be between about 3 and about 9 cm. Process gas can be inserted into the chamber of apparatus 10 at a rate up to about 200 sccm while the pressure in the chamber of apparatus 10 can be held at between about .7 and 6 millitorr. Magnet 20 provides a magnetic field of strength between about 400 and about 600 Gauss directed in the plane of target 12 and is moved across target 12 at a rate of less than about 20-30 sec/scan. In some embodiments utilizing the AKT 1600 reactor, magnet 20 can be a race-track shaped magnet with dimensions about 150 mm by 600 mm.

[0032] Figure 2 illustrates an example of target 12. A film deposited on a substrate positioned on carrier sheet 17 directly opposed to region 52 of target 12 has good thickness uniformity. Region 52 is the region shown in Figure 1B that is exposed to a uniform plasma condition. In some implementations, carrier 17 can be coextensive with region 52. Region 24 shown in Figure 2 indicates the area below which both physically and chemically uniform deposition can be achieved, for example where physical and chemical uniformity provide refractive index uniformity. Figure 2 indicates region 52 of target 12 that provides thickness uniformity is, in general, larger than region 24 of target 12 providing thickness and chemical uniformity. In optimized processes, however, regions 52 and 24 may be coextensive.

[0033] In some embodiments, magnet 20 extends beyond area 52 in one direction, for example the Y direction in Figure 2, so that scanning is necessary in only one direction, for example the X direction, to provide a time averaged uniform magnetic field. As shown in Figures 1A and 1B, magnet 20 can be scanned over the entire extent of target 12, which is larger than region 52 of uniform sputter erosion. Magnet 20 is moved in a plane parallel to the plane of target 12.

[0034] The combination of a uniform target 12 with a target area 52 larger than the area of substrate 16 can provide films of highly uniform thickness. Further, the material properties of the film deposited can be highly uniform. The conditions of sputtering at the target surface, such as the uniformity of erosion, the average temperature of the plasma at the target surface and the equilibration of the target surface with the gas phase ambient of the process are uniform over a region which is greater than or equal to the region to be coated with a uniform film thickness. In addition, the region of uniform film thickness is greater than or equal to the region of the film which is to have highly uniform optical properties such as index of refraction, density, transmission or absorptivity.

[0035] Target 12 can be formed of any materials. Typically metallic materials, for example, include combinations of In and Sn. Therefore, in some embodiments, target 12 includes a metallic target material formed from intermetallic compounds of optical elements such as Si, Al, Er and Yb. Additionally, target 12 can be formed, for example, from materials such as La, Yt, Ag, Au, and Eu. To form optically active films on substrate 16, target 12 can include rare-earth ions. In some embodiments of target 12 with rare earth ions, the rare earth ions can be pre-alloyed with the metallic host components to form intermetallics. *See* U.S. Application Serial No. 10/101,341. Typical ceramic target materials include alumina, silica, alumina silicates, and other such materials.

[0036] In some embodiments of the invention, material tiles are formed. These tiles can be mounted on a backing plate to form a target for apparatus 10. A wide area sputter cathode target can be formed from a close packed array of smaller tiles. Target 12, therefore, may include any number of tiles, for example between 2 to 20 individual tiles. Tiles can be finished to a size so as to provide a margin of non-contact, tile to tile, less than about 0.010" to about 0.020" or less than half a millimeter so as to eliminate plasma processes that may occur between adjacent ones of tiles 30. The distance between tiles of target 12 and the dark space anode or ground shield 19 in Figure 1B can be somewhat larger so as to provide non contact assembly or to provide for thermal expansion tolerance during process chamber conditioning or operation.

[0037] As shown in Figure 1B, a uniform plasma condition can be created in the region between target 12 and substrate 16 in a region overlying substrate 16. A plasma 53 can be created in region 51, which extends under the entire target 12. A central region 52 of target 12 can experience a condition of uniform sputter erosion. As discussed further below, a layer deposited on a substrate placed anywhere below central region 52 can then be uniform in thickness and other properties (i.e., dielectric, optical index, or material concentrations). In addition, region 52 in which deposition provides uniformity of deposited film can be larger than the area in which the deposition provides a film with uniform physical or optical properties such as chemical composition or index of refraction. In some embodiments, target 12 is substantially planar in order to provide uniformity in the film deposited on substrate 16. In practice, planarity of target 12 can mean that all portions of the target surface in region 52 are within a few millimeters of a planar surface, and can be typically within 0.5 mm of a planar surface.

[0038] Reactive gases that provide a constant supply of ionic oxygen to keep the target surface oxidized can be provided to expand the process window. Some examples of the gases that can be utilized for controlling surface oxidation are CO_2, water vapor, hydrogen, N_2O, fluorine, helium, and cesium. Additionally, a feedback control system can be incorporated to control the oxygen partial pressure in the reactive chamber. Therefore, a wide range of oxygen flow rates can be controlled to keep a steady oxygen partial pressure in the resulting plasma. Other types of control systems such as target voltage control and optical plasma emission control systems can also be utilized to control the surface oxidation of the target. As shown in Figure 1A, power to target 12 can be controlled in a feedback loop at supply 14. Further, oxygen partial pressure controller 20 can control either oxygen or argon partial pressures in plasma 53.

[0039] In some embodiments, transparent conductive oxides can be deposited on various substrates utilizing an inidium-tin (In/Sn) metallic target. A series of depositions on glass in accordance with the present invention is illustrated in Table I. The parameters in the process column of Table I are in the format (pulsed DC power/RF bias power/pulsing frequency/reverse time/deposition time/Ar flow (sccms)/O_2 flow (sccms)). An indium-tin (In/Sn: 90%/10% by weight) target using a reactive-pulsed DC (RPDC) process such as that described in U.S. Application Serial No. 10/101,863 was utilized. A power supply with 2MHz RF bias applied to substrate 16 was utilized in the process. Along with the process parameters for each of the separate depositions, each defined by a "Slot" number in the first column, the target voltage, and target current ranges for each of the depositions is also listed.

[0040] Table 2 shows the results obtained by using the process parameters in Table 1. The results include the sheet resistance, thickness, bulk resistivity, and refractive indices of the resulting films. Again, the first column indicates the slot number of the deposition. The process for each slot number is reiterated in column 2 of Table 2. The sheet resistance of selected ones of the films resulting from the deposition is listed in the third column and the uniformity of the sheet resistance is indicated in the fourth column. The thickness of the film and its uniformity of each of the films deposited by the indicated process is indicated in the fifth and sixth columns. The bulk resistance of selected ones of the films, ρ, is also indicated. Additionally, the refractive index taken at 632 nm is indicated along with the film uniformity of that index. The comments section of Table 2 indicates whether the resulting film is transparent, translucent, or metallic in character.

[0041] Figure 3A shows the Atomic Force Microscopy (AFM) image of an ITO film produced by the process identified in slot #5 in tables 1 and 2. That process, with particularly low oxygen flow rates (24 sccm), produced a rough film with an Ra of about 70 Å and an Rms of about 90 Å. The film also appears to be metallic with this particular oxygen flow and the film roughness is high. Such a film could be applicable to large surface area requirements, for example solar cell applications. Wile not being limited by any particular theory, it is suspected that the roughness of this film reflects the sub-stoichiometric nature of the film caused by insufficient oxygen flow in the plasma. As can be seen in Figure 3B, where the oxygen flow during deposition has been significantly increased to about 36 sccm, the film is smooth.

[0042] Figure 3B shows an Atomic Force Microscopy (AFM) image of an ITO film deposited using the process described in slot #19 of Tables 1 and 2. In that process, the oxygen flow rate is increased to 36 sccm. The film appears to be transparent and conductive and the surface roughness is ~6Å Ra and Rms of about 13 Å, which is acceptable for OLED requirements. As can be seen from Figures 3A and 3B, variation in oxygen partial pressure (as indicated by increased flow rate) has a large influence on the characteristics of the resulting deposited film.

[0043] The resistivity of the film layer and the smoothness of the film layer can be related. In general, the higher the resistivity of the film layer, the smoother the film layer. Figure 4 shows the variation of bulk resistivity of the ITO as a function of the oxygen flow rate used for two different target powers before and after a 250 °C anneal in vacuum. The bulk resistivity of the film exhibits a sudden transition downward as the oxygen flow rate is lowered. This transition occurs when the target surface becomes metallic from being poisoned with oxygen. The data utilized to form the graph shown in Figure 4 has been taken from Tables 1 and 2.

[0044] Figure 5 shows the variation of the sheet resistance of an ITO film as function of the O_2 flow used for two different target powers before and after a 250C anneal in vacuum. As shown in Figure 5, the sheet resistance follows similar trends as the bulk resistivity of the film.

[0045] Figure 6 shows the target current and voltage (min and max) as a function of the oxygen flow rate. The target voltage increases as the oxygen flow rate is lowered. It could be seen here that at a 40 sccm oxygen flow rate through repeated depositions, the target voltage is not constant. This illustrates the utility of a target voltage feedback control system that adjusts the power supplied to target 12 to hold the target voltage constant. Therefore, as shown in Figure 1A, PDC power 14 can include feedack loop to control the voltage on target 12.

[0046] Figure 7 shows the thickness change of a resulting film as a function of oxygen flow rate in sccm. The thickness of the film increases as the oxygen flow decreases but this could make opaque metallic films and so choosing the correct oxygen flow and utilizing an oxygen flow feedback control system to control material characteristics such as, for example, transparency or conductivity can be desirable.

[0047] In some embodiments, instead of oxygen flow rate, oxygen partial pressure can be controlled with a feedback system 20 (see Figure 1A). Controlling the oxygen partial pressure can provide better control over the oxygen content of the plasma, and therefore the oxygen content of the resulting films, and allows better control over the film characteristics. Figure 8 illustrates the relationship between the flow rate and partial pressure. As can be seen from Figure 8, in order to reach the saturated region (e.g., when target 12 is completely poisoned with oxygen), no increase in flow rate is required. In some embodiments, reactor 10 can include a partial pressure feedback loop controller 20 that controls the oxygen flow in order to maintain a desired partial pressure of oxygen in the plasma. Such a controller can be the IRESS system, that can be purchased from Advanced Energy, Inc., Ft. Collins, Colorado. It has been found that film parameters such as resistivity, smoothness, and transparency can be highly dependent on oxygen partial pressures, and therefore these characteristics of the resulting deposited layer can be controlled by adjusting the oxygen partial pressures.

[0048] Some embodiments of the present invention can be deposited with ceramic targets. An example target is an ITO (In/Sn 90/10) ceramic target can be utilized. Table 3 illustrates some example processes for deposition of ITO utilizing a ceramic target according to the present invention. Bulk resistivity, sheet resistance, resistance, thicknesses, deposition rates, and index of refraction of the resulting films are shown along with the process parameters utilized in the deposition. Figure 9A shows an AFM depiction of a transparent conductive oxide film corresponding to run #10 in Table 3. Figure 9B shows an AFM depiction of a transparent conductive oxide film corresponding to run #14 in Table 3. Figure 9C shows an AFM depiction of a transparent conductive oxide film corresponding to run #16 in Table 3. Figure 9D shows an AFM depiction of a transparent conductive oxide film layer corresponding to run #6 in Table 3.

[0049] Figures 9A through 9D illustrate the roughnesses of selective depositions of ITO deposited utilizing the ceramic target. In Figure 9A, the roughest surface shown, the film was deposited using 3kW RF power, 100W bias, 3 sccm O_2 and 60 sccm Ar at a temperature of 280 °C. The layer grew to a thickness of 1200 Å in 100 seconds of deposition time and exhibited a sheet resistance of 51 ohms/sq. The roughness illustrated in Figure 9A is characterized by an Ra=2.3 nm and R_{MS} of 21 nm.

[0050] The ITO film shown in Figure 9B was deposited using 3 kW RF power, 300 W bias, 3 sccm O_2 and 60 sccm Ar at a temperature of 280 °C. The layer illustrated in Figure 9B grew to a thickness of 1199 Å in 100 sec. The layer in Figure 9B exhibited a sheet resistance of 39 ohms/sq. The roughness illustrated in Figure 9B is characterized by an Ra=1.1 nm and Rmax of 13 nm.

[0051] The ITO film shown in Figure 9C was deposited using 3 kW RF power, 300 W bias, 3 sccm O_2, 30 sccm Ar at a temperature of 280 °C. The layer grew to a thickness of 1227 Å in 100 seconds of deposition time and exhibited a sheet resistance of 57 ohms/sq. The roughness illustrated in Figure 9C can be characterized by an Ra=0.88 nm and a Rmax of 19.8 nm.

[0052] Figure 9D was deposited using 1.5 kW RF power, 300 W bias, 0 sccm O_2, 30 sccm Ar at a temperature of 280 C. The layer grew to a thickness of 580 Å in 100 seconds of deposition time and exhibited a sheet resistance of 106 ohms/sq. The roughness illustrated in Figure 9C can be characterized by an Ra=0.45 nm and an Rmax of 4.6 nm.

[0053] Utilizing the example depositions described herein, the roughness and resistivity of a transparent oxide film can be tuned to particular applications. In general, particularly high resistivities can be obtained, which are useful for touch sensitive devices. As shown in Table 3, the sheet resistance ranged from about 39 Ω/sq for trial # 14 to a high of 12,284 Ω/sq for trial #1. Careful variation of the process parameters, therefore, allow control of sheet resistance over an extremely broad range. Low resistivities can be obtained by adjusting the process parameters for uses in devices such as OLEDS and MEMS display devices. As is illustrated in Table 3, the bulk resistivity can be controlled to be between about 2E-4 micro-ohms-cm to about 0.1 micro-ohms-cm. Additionally, other parameters such as refractive index and transparency of the film can be controlled.

[0054] Further, deposition of transparent conductive oxide layers, for example ITO, can be doped with rare-earth ions, for example erbium or cerium, can be utilized to form color-conversion layers and light-emission sources. In some embodiments, a rare-earth doped target can be made in a single piece to insure uniformity of doping. Co-doping can be accomplished in the target.

[0055] Similar processes for other metallic conductive oxides can also be developed. For example, deposition of zinc oxide films. Further, as can be seen in the examples shown in Table 3, low temperature depositions can be performed. For example, transparent conductive oxides according to the present invention can be deposited at temperatures as low as about 100 °C. Such low temperature depositions can be important for depositions on temperature sensitive materials such as plastics.

[0056] Other thin film layers according to the present invention include deposition of other metal oxides to form conducting and semi-conducting films. Thin films formed according to the present invention can be utilized in many devices, including, but not limited to, displays, photovoltaics, photosensors, touchscreens, and EMI shielding.

[0057] Embodiments of the invention disclosed here are examples only and are not intended to be limiting. Further, one skilled in the art will recognize variations in the embodiments of the invention described herein which are intended to be included within the scope and spirit of the present disclosure. As such, the invention is limited only by the following claims.

Table I

Slot #	Process	Target Voltage (V)		Target Current (Amps)	
		Min	Max	Mix	Max
14	1.5kw/100w/200khz/2.2μs/300s/20Ar/80O_2	244	252	5.94	6.14
15	1.5kw/100w/200khz/2.2μs/300s/20Ar/40O_2	254	263	5.7	5.9
17	1.5kw/100w/200khz/2.2μs/300s/20Ar/40O_2	252	260	5.76	5.96
19	1.5kw/100w/200khz/2.2μs/300s/20Ar/36O_2	254	263	5.72	5.92
21	1.5kw/100w/200khz/2.2μs/300s/20Ar/30O_2	255	268	5.76	5.9
1	1kw/100w/200khz/2.2μs/300s/20Ar/ 80O_2	224	233	4.32	4.5
2	1kw/100w/200khz/2.2μs/300s/20Ar/ 36O_2	231	243	4.12	4.3
3	1kw/100w/200khz/2.2μs/300s/20Ar/ 32O_2	232	242	4.12	4.28
4	1kw/100w/200khz/2.2μs/300s/20Ar/ 28O_2	237	243	4.1	4.22
5	1kw/100w/200khz/2.2μs/300s/20Ar/ 24O_2	233	243	4.1	4.34
6	1kw/100w/200khz/2.2μs/300s/20Ar/ 28O_2	231	245	4.12	4.3

Table II

Slot #	Process	Rs (Ohms/ Sq)	Rs unif %	Th (nm)	Th std 1sig	Bulk Rho (μOhm-cm)	R.I (@632nm)	R.I Unif (%)	Comments
14	1.5kw/100w/200khz/2.2μs/ 300s/20Ar/80O2			38.59	0.16		1.980758	0.000005	transparent
15	1.5kw/100w/200khz/2.2μs/ 300s/20Ar/40O2	94112	2	57.28	0.51	539073.5	1.951452	0.029342	translucent
17	1.5kw/100w/200khz/2.2μs/ 300s/20Ar/40O2	33927	60.282	58.48	1.37	198405.1	1.936166	0.040957	translucent
19	1.5kw/100w/200khz/2.2μs/ 300s/20Ar/36O2	7335.32	72.49	67.75	1.03	49696.8	1.980746	0.000018	translucent
21	1.5kw/100w/200khz/2.2μs/ 300s/20Ar/30O2	22.3507	2.995	80		178.8			metallic
1	1kw/100w/200khz/2.2μs/ 300s/20Ar/80O2			26.69	0.32		1.980326	0.00096	transparent
2	1kw/100w/200khz/2.2μs/ 300s/20Ar/36O2			36.4	0.13		1.980756	0.000003	transparent
3	1kw/100w/200khz/2.2μs/ 300s/20Ar/32O2			39.3	0.15		1.980761	0	transparent
4	1kw/100w/200khz/2.2μs/ 300s/20Ar/28O2			44.02	0.24		1.98076	0.000001	transparent
5	1kw/100w/200khz/2.2μs/ 300s/20Ar/24O2	58.1031	7.467	50		290.5			metallic
6	1kw/100w/200khz/2.2μs/ 300s/20Ar/28O2	58.0992	10.566	45		261.4			metallic

Table III

Trial	Run (sec)	Target Power (kW)	Bias/ W	O2	Ar	T (oC)	Rs (Ohms/Sq)	Rs (non-unif)	Bulk Rho (uOhmcm)	Thickness (Å)	n	DepRate (A/sec)	Target /V	Target/I
14	100	3	300	3	60	280	38.69	4.07%	4.64E-04	1200	1.864	12		
16	100	3	300	3	30	280	56.90	7.94%	6.98E-04	1227	1.888	12.27	288-308	9.86-10.42
10	100	3	100	3	60	280	50.98	11.89%	6.25E-04	1225	1.933	12.25	265-275	10.92-11.36
4	100	1.5	100	3	30	280	383.62	21.72%	2.09E-03	543.9	2.016	5.439	238-251	5.98-6.32
8	100	1.5	300	3	30	280	504.02	7.23%	2.44E-03	483.5	2.082	4.835	239-250	5.98-6.33
2	100	1.5	100	3	30	280	402.52	26.80%	2.10E-03	520.7	2.056	5.207	225-239	6.46-6.68
6	100	1.5	300	0	30	280	106.21	6.12%	6.17E-04	580.5	1.945	5.805	237-250	5.98-6.38
12	100	3	100	4	30	280	374.34	19.43%	4.18E-03	1116	1.917	11.16	285-300	9.98-10.52
15	100	3	300	4	30	100	6264.69	58.18%	6.81E-02	1087	1.897	10.87	282-304	10.00-10.62
7	100	1.5	200	4	30	100	7509.45	44.14%	2.95E-02	392.3	2.149	3.923	237-250	6.02-632
1	100	1.5	100	4	30	100	12284.82	112.55%	4.78E-02	389.1	2.236	3.891	238-250	6.04-632

Table III (Cont.)

11	100	3	100	3	60	100	631.77	49.40%	7.30E-03	1155	1.958	11.55	266-273	10.96-11.38
9	100	3	100	0	30	100	43.78	7.47%	5.55E-04	1268	1.945	12.68	288-307	9.78-10.42
5	100	1.5	200	3	60	100	1293.53	14.82%	5.88E-03	454.8	2.149	4.548	225-235	6.46-6.68
3	100	1.5	100	4	60	100	4154.43	28.25%	1.78E-02	428.8	2.211	4.288	226-235	6.44-6.64
13	100	3	200	0	60	100	49.05	7.24%	6.16E-04	1256	1.913	12.56	264-275	10.96-11.38
18	100	2.25	100	3	30	100	1476.79	21.54%	1.10E-02	744.5	2.044	7.445	263-277	8.08-8.56
17	100	1.5	150	0	60	100	157.23	8.83%	9.91E-04	630.5	1.931	6.305	225-231	6.48-6.74
19	100	2.25	150	3	60	100	526.72	13.01%	4.29E-03	814.2	2.021	8.142	247-255	8.78-9.14

Claims

We claim:

1. A method of forming a transparent conductive oxide film, comprising:

depositing the transparent conductive oxide film in a pulsed DC reactive ion process with substrate bias; and

controlling at least one process parameter to provide at least one characteristic of the conductive oxide film at a particular value.

2. The method of claim 1, wherein controlling at least one process parameter includes controlling the oxygen partial pressure.

3. The method of claim 1, wherein the transparent conductive oxide film includes indiuim-tin oxide.

4. The method of claim 1, wherein the at least one characteristic includes sheet resistance.

5. The method of claim 1, wherein the at least one characteristic includes film roughness.

6. The method of claim 5, wherein the transparent conductive oxide film includes an indium-tin oxide film and the film roughness is characterized by R_a less than about 10 nm with Rms of less than about 20 nm.

7. The method of claim 4, wherein the bulk resistance can be varied between about 2×10^{-4} micro-ohms-cm to about 0.1 micro-ohms-cm.

8. The method of claim 1, wherein the at least one process parameter includes a power supplied to a target.

9. The method of claim 1, wherein the at least one process parameter includes an oxygen partial pressure.

10. The method of claim 1, wherein the at least one process parameter includes bias power.

11. The method of claim 1, wherein the at least one process parameter includes deposition temperature.

12. The method of claim 1, wherein the at least one process parameter includes an argon partial pressure.

13. The method of claim 1, further including supplying a metallic target.

14. The method of claim 1, further including supplying a ceramic target.

15. The method of claim 1, wherein the transparent conductive oxide film is doped with at least one rare-earth ions.

16. The method of claim 15, wherein the at least one rare-earth ions includes erbium.

17. The method of claim 15, wherein the at least one rare-earth ions includes cerium.

18. A method of depositing a transparent conductive oxide film on a substrate, comprising:

placing the substrate in a reaction chamber;

adjusting power to a pulsed DC power supply coupled to a target in the reaction chamber;

adjusting an RF bias power coupled to the substrate;

adjusting gas flow into the reaction chamber; and

providing a magnetic field at the target in order to direct deposition of the transparent conductive oxide film on the substrate in a pulsed-dc biased reactive-ion deposition process, wherein the transparent conductive oxide film exhibits at least one particular property.

19. The method of claim 18, wherein at least one particular property of the transparent conductive oxide film is determined by parameters of the pulsed-dc biased reactive ion deposition process.

20. The method of claim 19, wherein the at least one particular property includes resistivity of the transparent conductive oxide film.

21. The method of claim 19, wherein the transparent conductive oxide film includes an indium-tin oxide film.

22. The method of claim 19, wherein the parameters include oxygen partial pressure.

23. The method of claim 19, wherein the parameters include bias power.

24. The method of claim 18, wherein the target can include at least one rare-earth ions.

25. The method of claim 24, wherein the at least one rare-earth ions includes erbium.

26. The method of claim 24, wherein the at least one rare-earth ion includes cerbium.

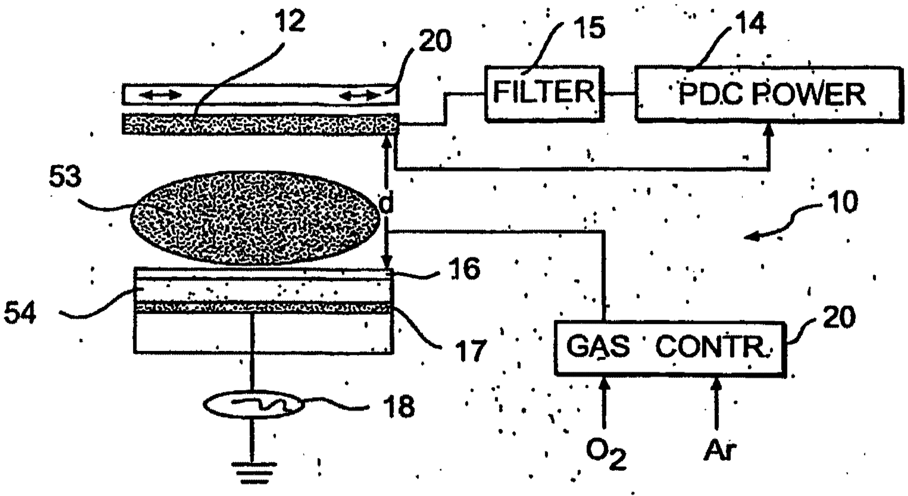
12
20
15
FILTER
14
PDC POWER
53
d
10
16
54
17
20
GAS CONTR.
18
O2
Ar

FIG. 1A

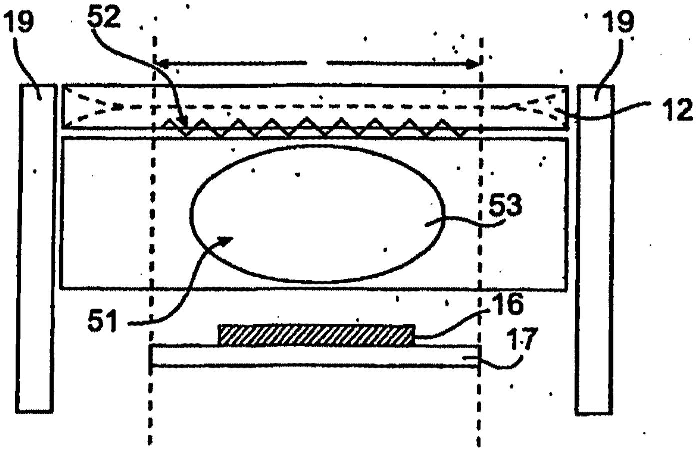
19
52
19
12
53
51
16
17

FIG. 1B

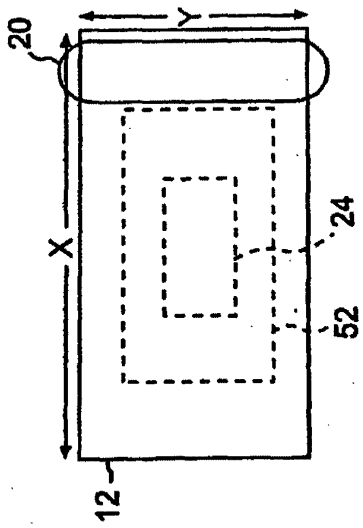

FIG. 2

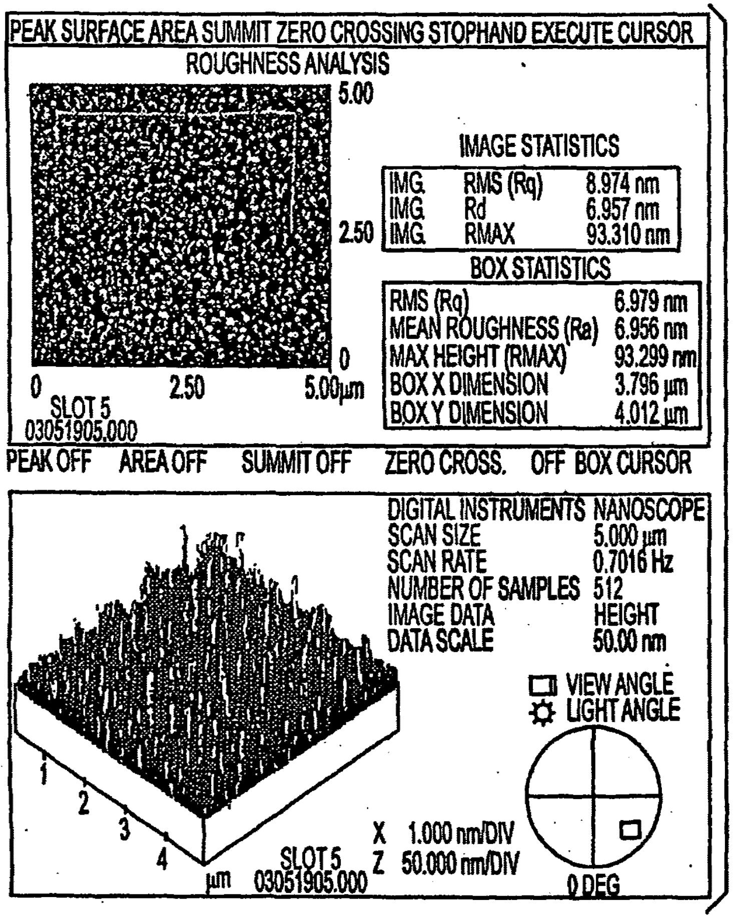

IMAGE STATISTICS

IMG.	RMS (Rq)	8.974 nm
IMG.	Rd	6.957 nm
IMG.	RMAX	93.310 nm

BOX STATISTICS

RMS (Rq)	6.979 nm
MEAN ROUGHNESS (Ra)	6.956 nm
MAX HEIGHT (RMAX)	93.299 nm
BOX X DIMENSION	3.796 µm
BOX Y DIMENSION	4.012 µm

DIGITAL INSTRUMENTS	NANOSCOPE
SCAN SIZE	5.000 µm
SCAN RATE	0.7016 Hz
NUMBER OF SAMPLES	512
IMAGE DATA	HEIGHT
DATA SCALE	50.00 nm

X 1.000 nm/DIV
Z 50.000 nm/DIV

FIG. 3A

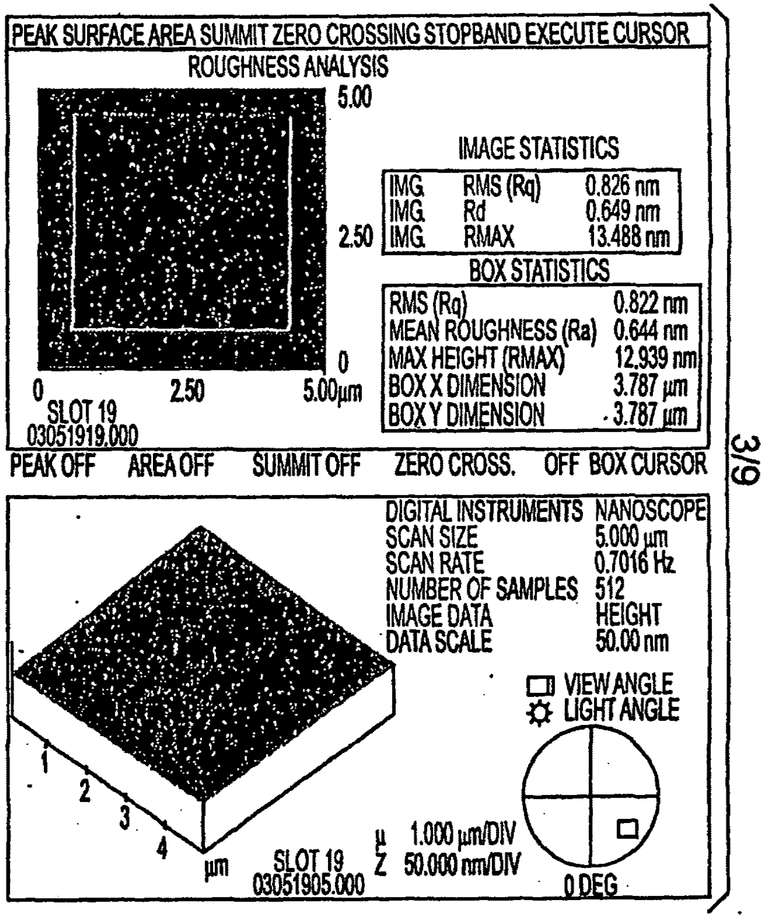

IMAGE STATISTICS

IMG.	RMS (Rq)	0.826 nm
IMG.	Rd	0.649 nm
IMG.	RMAX	13.488 nm

BOX STATISTICS

RMS (Rq)	0.822 nm
MEAN ROUGHNESS (Ra)	0.644 nm
MAX HEIGHT (RMAX)	12.939 nm
BOX X DIMENSION	3.787 µm
BOX Y DIMENSION	3.787 µm

DIGITAL INSTRUMENTS	NANOSCOPE
SCAN SIZE	5.000 µm
SCAN RATE	0.7016 Hz
NUMBER OF SAMPLES	512
IMAGE DATA	HEIGHT
DATA SCALE	50.00 nm

µ 1.000 µm/DIV
Z 50.000 nm/DIV

FIG. 3B

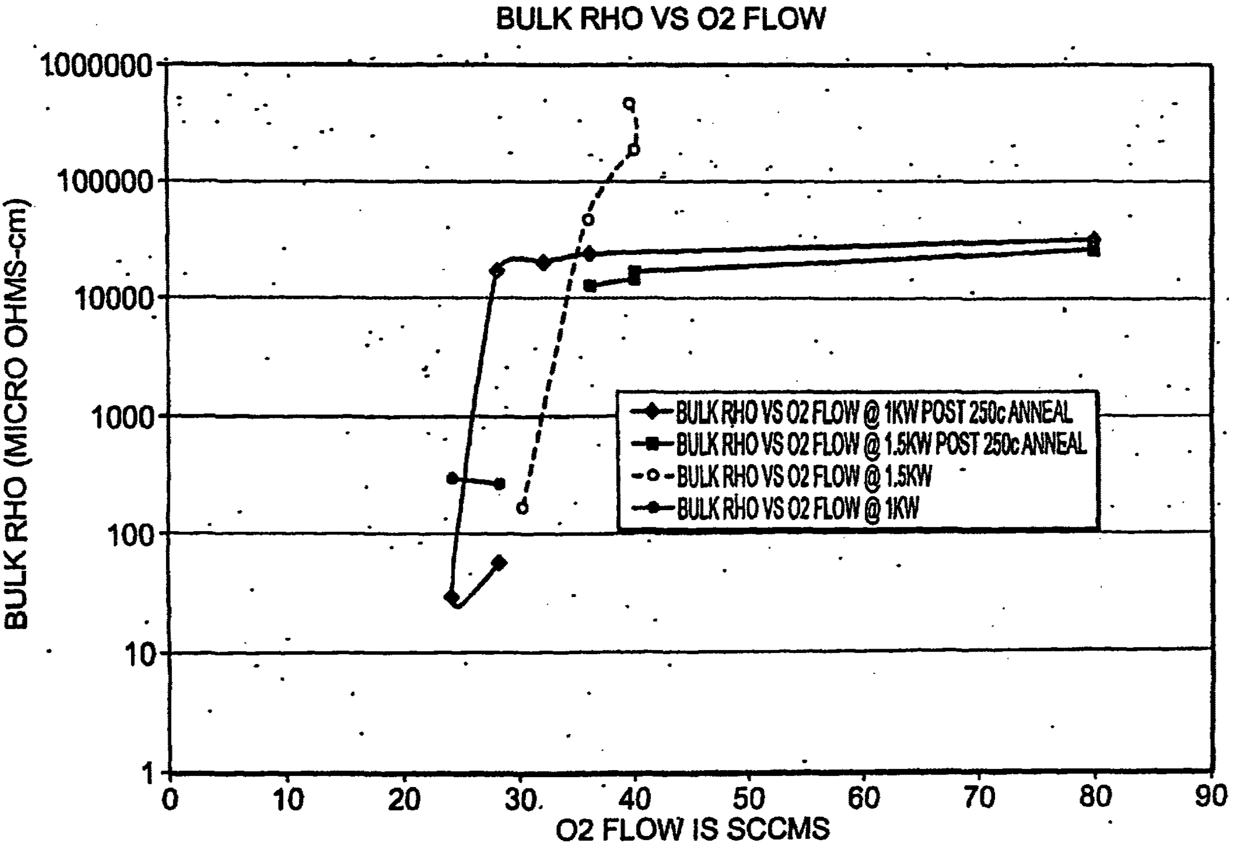
BULK RHO VS O2 FLOW
BULK RHO (MICRO OHMS-cm)
1000000
100000
10000
1000
100
10
1
0
10
20
30
40
50
60
70
80
90
O2 FLOW IS SCCMS
BULK RHO VS O2 FLOW @ 1KW POST 250c ANNEAL
BULK RHO VS O2 FLOW @ 1.5KW POST 250c ANNEAL
BULK RHO VS O2 FLOW @ 1.5KW
BULK RHO VS O2 FLOW @ 1KW

FIG. 4

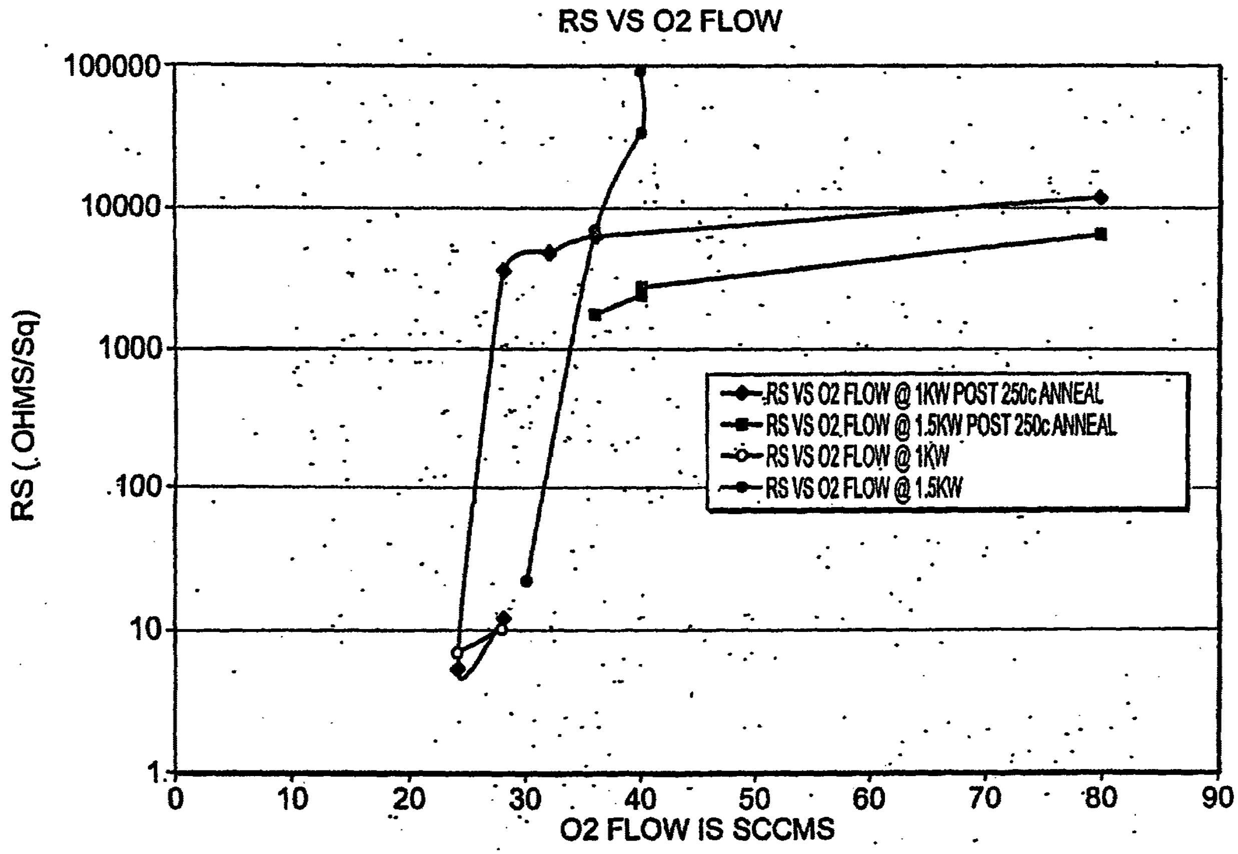
RS VS O2 FLOW
RS (OHMS/Sq)
100000
10000
1000
100
10
1
0
10
20
30
40
50
60
70
80
90
O2 FLOW IS SCCMS
RS VS O2 FLOW @ 1KW POST 250c ANNEAL
RS VS O2 FLOW @ 1.5KW POST 250c ANNEAL
RS VS O2 FLOW @ 1KW
RS VS O2 FLOW @ 1.5KW

FIG. 5

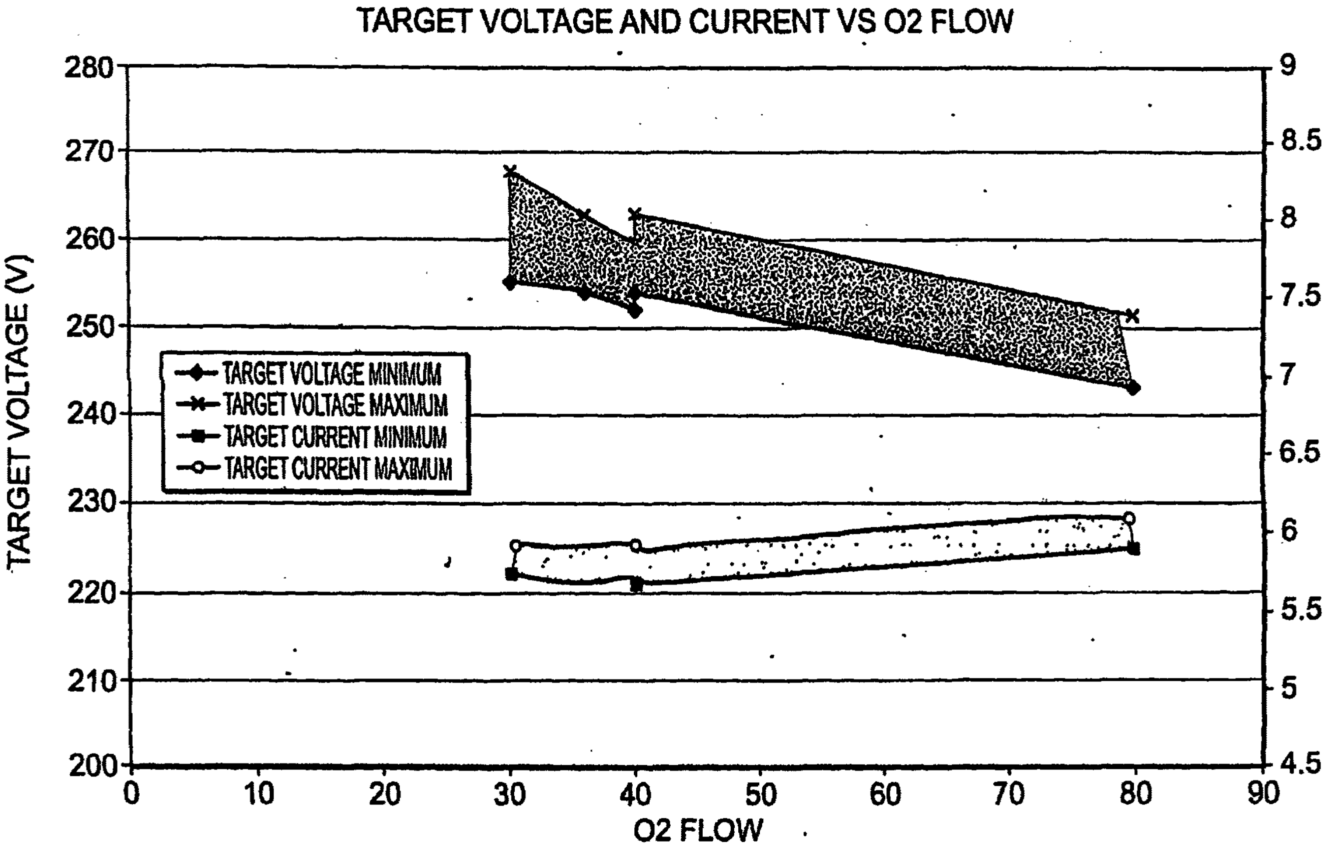
TARGET VOLTAGE AND CURRENT VS O2 FLOW
TARGET VOLTAGE (V)
280
270
260
250
240
230
220
210
200
9
8.5
8
7.5
7
6.5
6
5.5
5
4.5
0
10
20
30
40
50
60
70
80
90
O2 FLOW
TARGET VOLTAGE MINIMUM
TARGET VOLTAGE MAXIMUM
TARGET CURRENT MINIMUM
TARGET CURRENT MAXIMUM

FIG. 6

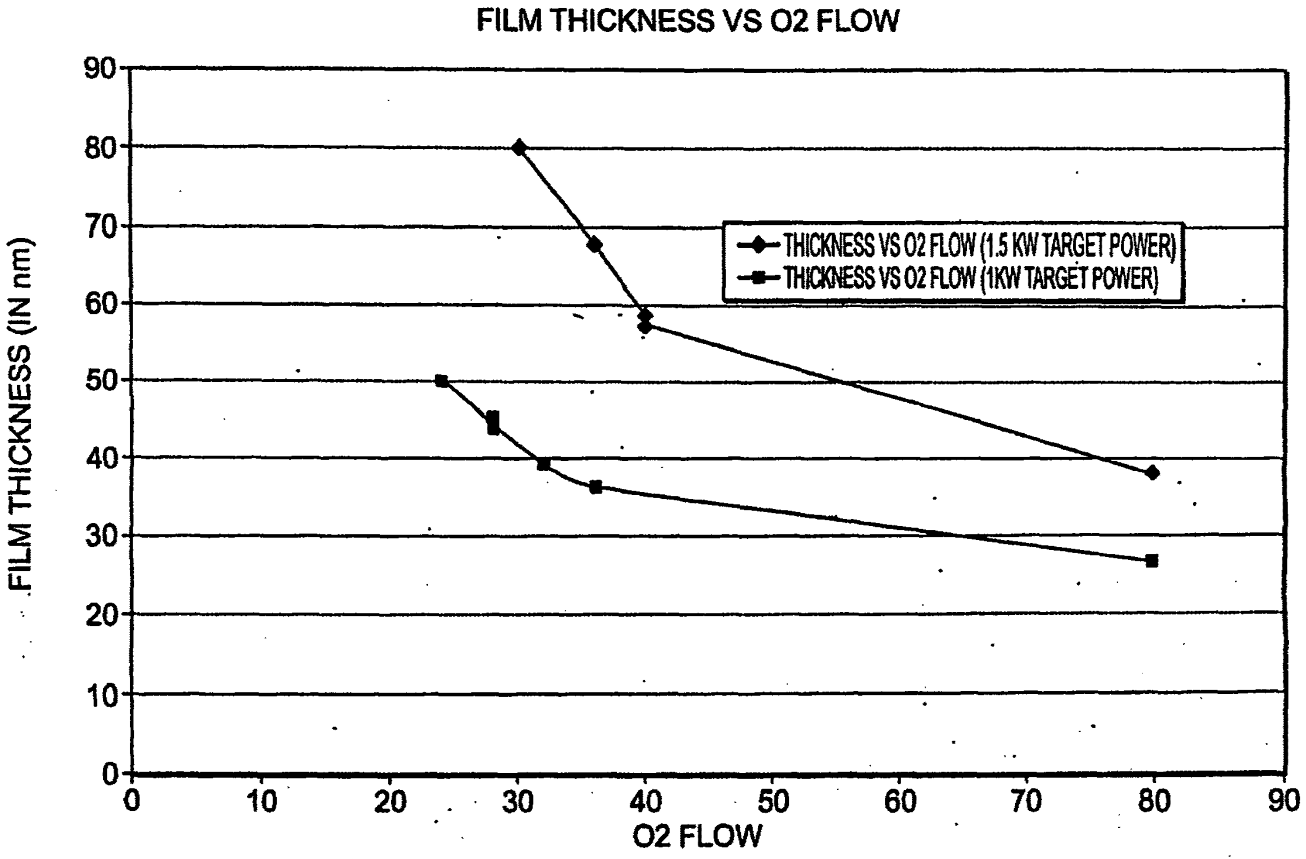
FILM THICKNESS VS O2 FLOW
FILM THICKNESS (IN nm)
90
80
70
60
50
40
30
20
10
0
0
10
20
30
40
50
60
70
80
90
O2 FLOW
THICKNESS VS O2 FLOW (1.5 KW TARGET POWER)
THICKNESS VS O2 FLOW (1KW TARGET POWER)

FIG. 7

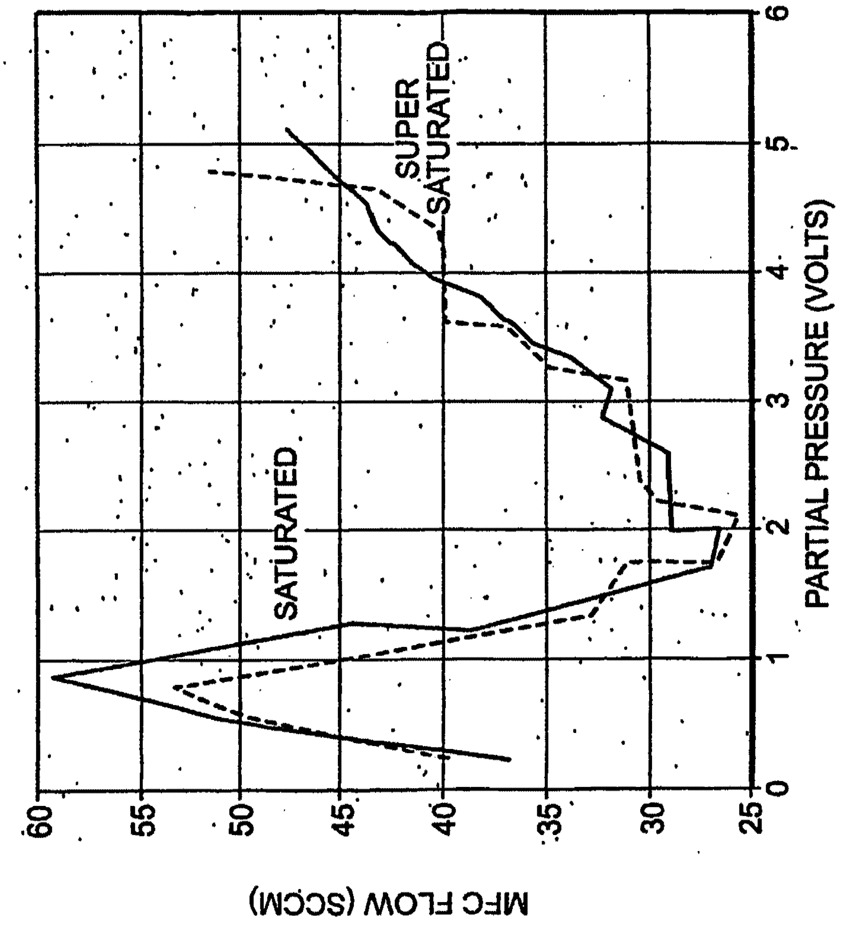
SUPER SATURATED
SATURATED
MFC FLOW (SCCM)
60
55
50
45
40
35
30
25
PARTIAL PRESSURE (VOLTS)
0
1
2
3
4
5
6

FIG. 8

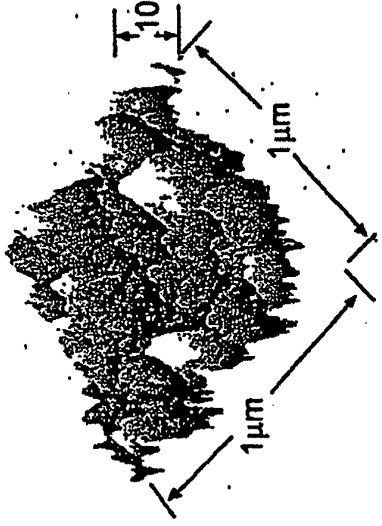

FIG. 9A

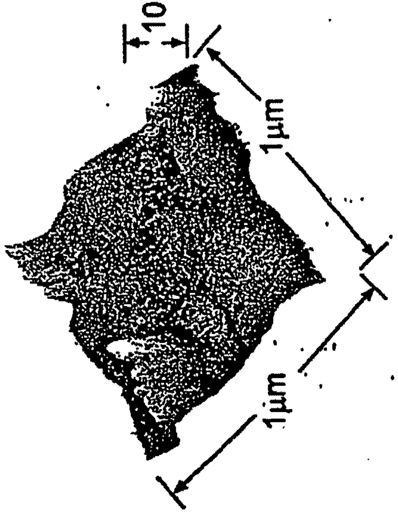

FIG. 9B

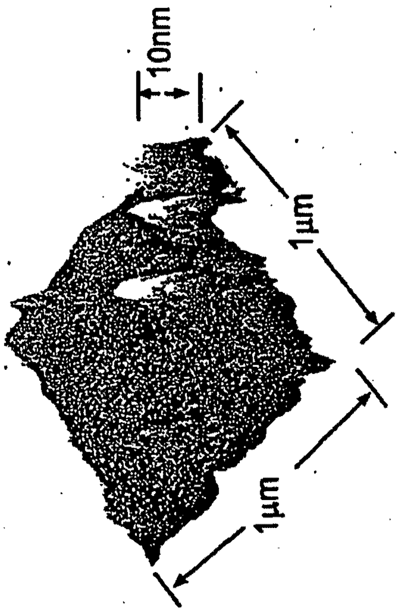

FIG. 9C

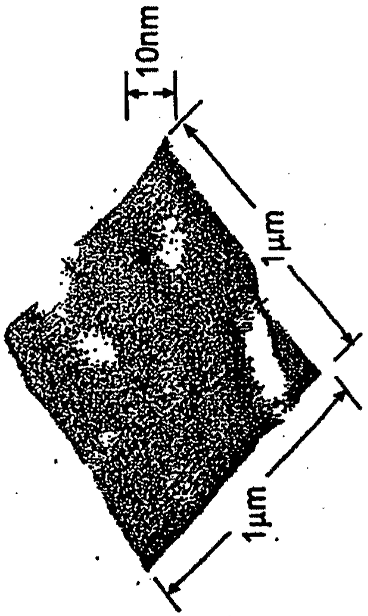

FIG. 9D

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(71) Applicant *(for all designated States except US)*: SYMMORPHIX, INC. [US/US]; 1278 Reamwood Avenue, Sunnyvale, CA 94089-2233 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **DEMARAY, Richard, Ernest** [US/US]; 190 Fawn Lane, Portola Valley, CA 94028 (US). **ZHANG, Hongmei** [US/US]; 1330 Rodney Drive, San Jose, CA 95118 (US). **NARASIMHAN, Mukundan** [IN/US]; 293 Bluefield Drive, San Jose, CA 95136 (US). **MILONOPOULOU, Vassiliki** [GR/US]; 6160 Paseo Pueblo Drive, San Jose, CA 95120 (US).

(74) Agent: **GARRETT, Arthur, S.**; Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P., 1300 I Street N.W., Washinton, D.C. 20005-3315 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

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WO 2004/106582 A2

(54) Title: ENERGY CONVERSION AND STORAGE FILMS AND DEVICES BY PHYSICAL VAPOR DEPOSITION OF TITANIUM AND TITANIUM OXIDES AND SUB-OXIDES

(57) Abstract: High density oxide films are deposited by a pulsed-DC, biased reactive sputtering process from a titanium containing target to form high quality titanium containing oxide films. A method of forming a titanium based layer or film according to the present invention includes depositing a layer of titanium containing oxide by pulsed-DC, biased reactive sputtering process on a substrate. In some embodiments, the layer is TiO_2. In some embodiments, the layer is a sub-oxide of Titanium. In some embodiments, the layer is Ti_xO_y wherein x is between about 1 and about 4 and y is between about 1 and about 7. In some embodiments, the layer can be doped with one or more rare-earth ions. Such layers are useful in energy and charge storage, and energy conversion technologies.

Energy Conversion and Storage Films and Devices by Physical Vapor Deposition of Titanium and Titanium Oxides and sub-Oxides

Related Applications

The present invention claims priority to U.S. Provisional Application Serial No. 60/473,375, "Energy Conversion and Storage Devices by Physical Vapor Deposition of Titanium Oxides and Sub-Oxides," by Richard E. Demaray and Hong Mei Zhang, filed on May 23, 2003, herein incorporated by reference in its entirety.

Background

1. Field of the Invention

[0001] The present invention is related to fabrication of thin films for planar energy and charge storage and energy conversion and, in particular, thin films deposited of titanium and titanium oxides, sub oxides, and rare earth doped titanium oxides and sub oxides for planar energy and charge storage and energy conversion.

2. Discussion of Related Art

[0002] Currently, titanium oxide layers are not utilized commercially in energy storage, charge storage, or energy conversion systems because such layers are difficult to deposit, difficult to etch, are known to have large concentrations of defects, and have poor insulation properties due to a propensity for oxygen deficiency and the diffusion of oxygen defects in the layers. Additionally, amorphous titania is difficult to deposit due to its low recrystalization temperature (about 250 °C), above which the deposited layer is often a mixture of crystalline anatase and rutile structures.

[0003] However, such amorphous titania layers, if they can be deposited in sufficient quality, have potential due to their high optical index, n~2.7, and their high dielectric constant, k less than or equal to about 100. Further, they have substantial chemical stability. There are no known volatile halides and titania is uniquely resistant to mineral acids. Amorphous titania is thought to have the further advantage that there are no grain boundary mechanisms for electrical breakdown, chemical corrosion, or optical scattering. It is also well known that the sub oxides of titanium have unique and useful properties. *See, e.g.*, Hayfield, P.C.S., "Development of a

New Material- Monolithic Ti_4O_7 Ebonix Ceramic", Royal Society Chemistry, ISBN 0-85405-984-3, 2002. Titanium monoxide, for example, is a conductor with a uniquely stable resistivity with varying temperature. Additionally, Ti_2O_3, which can be pinkish in color, is known to have semiconductor type properties. However, these materials have not found utilization because of their difficult manufacture in films and their susceptibility to oxidation. Further, Ti_4O_7 demonstrates both useful electrical conductivity and unusual resistance to oxidation. Ti_4O_7, however, is also difficult to fabricate, especially in thin film form.

[0004] Additional to the difficulty of fabricating titanium oxide or sub oxide materials in useful thin film form, it also has proven difficult to dope these materials with, for example, rare earth ions, in useful or uniform concentration.

[0005] Therefore, utilization of titanium oxide and suboxide films, with or without rare earth doping, has been significantly limited by previously available thin film processes. If such films could be deposited, their usefulness in capacitor, battery, and energy conversion and storage technologies would provide for many value-added applications.

[0006] Current practice for construction of capacitor and resistor arrays and for thin film energy storage devices is to utilize a conductive substrate or to deposit the metal conductor or electrode , the resistor layer, and the dielectric capacitor films from various material systems. Such material systems for vacuum thin films, for example, include copper, aluminum, nickel, platinum, chrome, or gold depositions, as well as conductive oxides such as ITO, doped zinc oxide, or other conducting materials.

[0007] Materials such as chrome-silicon monoxide or tantalum nitride are known to provide resistive layers with 100 parts per million or less resistivity change per degree Centigrade for operation within typical operating parameters. A wide range of dielectric materials such as silica, silicon nitride, alumina, or tantalum pentoxide can be utilized for the capacitor layer. These materials typically have dielectric constants k of less than about twenty four (24). In contrast, TiO_2 either in the pure rutile phase or in the pure amorphous state can demonstrate a dielectric constant as high as 100. *See, e.g.*, R. B. van Dover, "Amorphous Lanthanide-Doped TiO_2 Dielectric Films," Appl. Phys Lett., Vol. 74, no. 20, p. 3041-43 (May 17, 1999).

[0008] It is well known that the dielectric strength of a material decreases with increasing value of dielectric constant k for all dielectric films. A 'figure of merit' (FM) is therefore obtained by the product of the dielectric constant k and the dielectric strength measured in Volts per cm of dielectric thickness. Capacitive density of 10,000 to 12,000 pico Farads /mm^2 is very difficult to achieve with present conductors and dielectrics. Current practice for reactive deposition of titanium oxide has achieved a figure-of-merit, FM, of about 50 (k MV/cm). *See* J.-Y. Kim et al., "Frequency-Dependent Pulsed Direct Current Magnetron Sputtering of Titanium Oxide Films," J. Vac. Sci. Technol. A 19(2), Mar/Apr 2001.

[0009] Therefore, there is an ongoing need for titanium oxide and titanium sub-oxide layers, and rare-earth doped titanium oxide and titanium sub-oxide layers, for various applications.

Summary

[0010] In accordance with the present invention, high density oxide films are deposited by a pulsed-DC, biased, reactive sputtering process from a titanium containing target. A method of forming a titanium based layer or film according to the present invention includes depositing a layer of titanium containing oxide by pulsed-DC, biased reactive sputtering process on a substrate. In some embodiments, the layer is TiO_2. In some embodiments, the layer is a sub-oxide of Titanium. In some embodiments, the layer is Ti_xO_y wherein x is between about 1 and about 4 and y is between about 1 and about 7.

[0011] In some embodiments of the invention, the figure of merit of the layer is greater than 50. In some embodiments of the invention, the layer can be deposited between conducting layers to form a capacitor. In some embodiments of the invention, the layer includes at least one rare-earth ion. In some embodiments of the invention, the at least one rare-earth ion includes erbium. In some embodiments of the invention, the erbium doped layer can be deposited between conducting layers to form a light-emitting device. In some embodiments of the invention, the erbium doped layer can be an optically active layer deposited on a light-emitting device. In some embodiments of the invention, the layer can be a protective layer. In some embodiments, the protective layer can be a catalytic layer.

[0012] In some embodiments of the invention, the layer and a TiO_2 layer can be deposited between conducting layers to form a capacitor with decreased roll-off characteristics with decreasing thickness of the TiO_2 layer. In some embodiments, the TiO_2 layer can be a layer deposited according to some embodiments of the present invention.

[0013] These and other embodiments of the present invention are further discussed below with reference to the following figures.

Short Description of the Figures

[0014] Figures 1A and 1B illustrate a pulsed-DC biased reactive ion deposition apparatus that can be utilized in the deposition according to the present invention.

[0015] Figure 2 shows an example of a target that can be utilized in the reactor illustrated in Figures 1A and 1B.

[0016] Figures 3A and 3B illustrate various configurations of layers according to embodiments of the present invention.

[0017] Figures 4A and 4B illustrate further various configurations of layers according to embodiments of the present invention.

[0018] Figure 5 shows another layer structure involving one or more layers according to the present invention.

[0019] Figure 6 shows a transistor gate with a TiOy layer according to the present invention.

[0020] Figure 7 illustrates the roll-off of the dielectric constant with decreasing film thickness.

[0021] Figure 8 illustrates data points from a bottom electrode that helps reduce or eliminate the roll-off illustrated in Figure 7.

[0022] Figures 9A and 9B illustrate an SEM cross-section of a Ti_4O_7 target obtained from Ebonex™ and an SEM cross section of the $Ti_4O_{6.8}$ film deposited from the Ebonex™ target according to the present invention.

[0023] Figure 10 shows the industry standard of thin-film capacitor performance in comparison with layers according to some embodiments of the present invention.

[0024] Figure 11 shows the performance of various thin films deposited according to the present invention in a capacitor structure.

[0025] Figure 12 shows a cross-section TEM and diffraction pattern amorphous and crystalline layers of TiO_2 on n++ wafers.

[0026] Figure 13 shows a comparison of the leakage current for TiO_2 films according to embodiments of the present invention with and without erbium ion doping.

[0027] Figures 14A and 14B show a photoluminescence signal measured from a 5000 Å layer of 10% erbium containing TiO_2 deposited from a 10% erbium doped TiO conductive target and a photoluminescence signal measured from the same layer after a 30 minute 250 °C anneal.

[0028] In the figures, elements having the same designation have the same or similar functions.

Detailed Description

[0029] Miniaturization is driving the form factor of portable electronic components. Thin film dielectrics with high dielectric constants and breakdown strengths allow production of high density capacitor arrays for mobile communications devices and on-chip high-dielectric capacitors for advanced CMOS processes. Thick film dielectrics for high energy storage capacitors allow production of portable power devices.

[0030] Some embodiments of films deposited according to the present invention have a combination of high dielectric and high breakdown voltages. Newly developed electrode materials allow the production of very thin films with high capacitance density. The combination of high dielectric and high breakdown voltages produce thick films with new levels of available energy storage according to $E=1/2CV^2$.

[0031] Deposition of materials by pulsed-DC biased reactive ion deposition is described in U.S. Patent Application Serial No. 10/101863, entitled "Biased Pulse DC Reactive Sputtering of Oxide Films," to Hongmei Zhang, et al., filed on March 16, 2002. Preparation of targets is described in U.S. Patent Application Serial No. 10/101,341, entitled "Rare-Earth Pre-Alloyed PVD Targets for Dielectric Planar Applications," to Vassiliki Milonopoulou, et al., filed on March 16, 2002. U.S. Patent

Application Serial No. 10/101863 and U.S. Patent Application Serial No. 10/101,341 are each assigned to the same assignee as is the present disclosure and each is incorporated herein in their entirety. Additionally, deposition of materials is further described in U.S. Patent 6,506,289, which is also herein incorporated by reference in its entirety.

[0032] Figure 1A shows a schematic of a reactor apparatus 10 for sputtering of material from a target 12 according to the present invention. In some embodiments, apparatus 10 may, for example, be adapted from an AKT-1600 PVD (400 X 500 mm substrate size) system from Applied Komatsu or an AKT-4300 (600 X 720 mm substrate size) system from Applied Komatsu, Santa Clara, CA. The AKT-1600 reactor, for example, has three deposition chambers connected by a vacuum transport chamber. These AKT reactors can be modified such that pulsed DC (PDC) power is supplied to the target and RF power is supplied to the substrate during deposition of a material film. The PDC power supply 14 can be protected from RF bias power 18 by use of a filter 15 coupled between PDC power supply 14 and target 12.

[0033] Apparatus 10 includes a target 12 which is electrically coupled through a filter 15 to a pulsed DC power supply 14. In some embodiments, target 12 is a wide area sputter source target, which provides material to be deposited on substrate 16. Substrate 16 is positioned parallel to and opposite target 12. Target 12 functions as a cathode when power is applied to it and is equivalently termed a cathode. Application of power to target 12 creates a plasma 53. Substrate 16 is capacitively coupled to an electrode 17 through an insulator 54. Electrode 17 can be coupled to an RF power supply 18. Magnet 20 is scanned across the top of target 12.

[0034] For pulsed reactive dc magnetron sputtering, as performed by apparatus 10, the polarity of the power supplied to target 12 by power supply 14 oscillates between negative and positive potentials. During the positive period, the insulating layer on the surface of target 12 is discharged and arcing is prevented. To obtain arc free deposition, the pulsing frequency exceeds a critical frequency that depends on target material, cathode current and reverse time. High quality oxide films can be made using reactive pulsed DC magnetron sputtering in apparatus 10.

[0035] Pulsed DC power supply 14 can be any pulsed DC power supply, for example an AE Pinnacle plus 10K by Advanced Energy, Inc. With this example supply, up to 10 kW of pulsed DC power can be supplied at a frequency of between 0 and 350 KHz. In some embodiments, the reverse voltage is 10% of the negative target voltage. Utilization of other power supplies will lead to different power characteristics, frequency characteristics, and reverse voltage percentages. The reverse time on this embodiment of power supply 14 can be adjusted to between 0 and 5 µs.

[0036] Filter 15 prevents the bias power from power supply 18 from coupling into pulsed DC power supply 14. In some embodiments, power supply 18 can be a 2 MHz RF power supply, for example a Nova-25 power supply made by ENI, Colorado Springs, Co.

[0037] Therefore, filter 15 can be a 2 MHz band sinusoidal rejection filter. In some embodiments, the bandwidth of the filter can be approximately 100 kHz. Filter 15, therefore, prevents the 2 MHz power from the bias to substrate 16 from damaging power supply 18.

[0038] However, both RF sputtered and pulsed DC sputtered films are not fully dense and may typically have columnar structures. These columnar structures are detrimental to thin film applications. By applying a RF bias on wafer 16 during deposition, the deposited film can be densified by energetic ion bombardment and the columnar structure can be substantially eliminated or completely eliminated.

[0039] In the AKT-1600 based system, for example, target 12 can have an active size of about 675.70 X 582.48 by 4 mm in order to deposit films on substrate 16 that have dimension about 400 X 500 mm. The temperature of substrate 16 can be held at between –50C and 500C by introduction of back-side gas in a physical or electrostatic clamping of the substrate, thermo-electric cooling, electrical heating, or other methods of active temperature control. In Figure 1A, a temperature controller 22 is shown to control the temperature of substrate 16. The distance between target 12 and substrate 16 can be between about 3 and about 9 cm. Process gas can be inserted into the chamber of apparatus 10 at a rate up to about 200 sccm while the pressure in the chamber of apparatus 10 can be held at between about .7 and 6 millitorr. Magnet 20 provides a magnetic field of strength between about 400 and about 600 Gauss directed in the plane of target 12 and is moved across target 12 at a rate of less than about 20-30 sec/scan. In some embodiments utilizing the AKT 1600 reactor, magnet 20 can be a race-track shaped magnet with dimension about 150 mm by 600 mm.

[0040] Figure 2 illustrates an example of target 12. A film deposited on a substrate positioned on carrier sheet 17 directly opposed to region 52 of target 12 has good thickness uniformity. Region 52 is the region shown in Figure 1B that is exposed to a uniform plasma condition. In some implementations, carrier 17 can be coextensive with region 52. Region 24 shown in Figure 2 indicates the area below which both physically and chemically uniform deposition can be achieved, where physical and chemical uniformity provide refractive index uniformity, for example. Figure 2 indicates that region 52 of target 12 that provides thickness uniformity is, in general, larger than region 24 of target 12 providing thickness and chemical uniformity. In optimized processes, however, regions 52 and 24 may be coextensive.

[0041] In some embodiments, magnet 20 extends beyond area 52 in one direction, the Y direction in Figure 2, so that scanning is necessary in only one direction, the X direction, to provide a time averaged uniform magnetic field. As shown in Figures 1A and 1B, magnet 20 can be scanned over the entire extent of target 12, which is larger than region 52 of uniform sputter erosion. Magnet 20 is moved in a plane parallel to the plane of target 12.

[0042] The combination of a uniform target 12 with a target area 52 larger than the area of substrate 16 can provide films of highly uniform thickness. Further, the material properties of the film deposited can be highly uniform. The conditions of sputtering at the surface of target 12, such as the uniformity of erosion, the average temperature of the plasma at the target surface and the equilibration of the target surface with the gas phase ambient of the process are uniform over a region which is greater than or equal to the region to be coated with a uniform film thickness. In addition, the region of uniform film thickness is greater than or equal to the region of the film which is to have highly uniform optical properties such as index of refraction, density, transmission, or absorptivity.

[0043] Target 12 can be formed of any materials, but is typically metallic materials such as, for example, combinations of In and Sn. Therefore, in some embodiments, target 12 includes a metallic target material formed from intermetallic compounds of optical elements such as Si, Al, Er and Yb. Additionally, target 12 can be formed, for example, from materials such as La, Yt, Ag, Au, and Eu. To form optically active films on substrate 16, target 12 can include rare-earth ions. In some embodiments of target 12 with rare earth ions, the rare earth ions can be pre-alloyed with the metallic host components to form intermetallics. *See* U.S. Application Serial No. 10/101,341.

[0044] In several embodiments of the invention, material tiles are formed. These tiles can be mounted on a backing plate to form a target for apparatus 10. A wide area sputter cathode target can be formed from a close packed array of smaller tiles. Target 12, therefore, may include any number of tiles, for example between 2 to 20 individual tiles. Tiles are finished to a size so as to provide a margin of non-contact, tile to tile, less than about 0.010" to about 0.020" or less than half a millimeter so as to eliminate plasma processes that may occur between adjacent ones of the tiles. The distance between the tiles of target 12 and the dark space anode or ground shield 19 in Figure 1B can be somewhat larger so as to provide non contact assembly or provide for thermal expansion tolerance during processing, chamber conditioning, or operation.

[0045] As shown in Figure 1B, a uniform plasma condition can be created in the region between target 12 and substrate 16 in a region overlying substrate 16. A plasma 53 can be created in region 51, which extends under the entire target 12. A central region 52 of target 12, can experience a condition of uniform sputter erosion. As discussed further below, a layer deposited on a substrate placed anywhere below central region 52 can then be uniform in thickness and other properties (i.e., dielectric, optical index, or material concentrations). In addition, region 52 in which deposition provides uniformity of deposited film can be larger than the area in which the deposition provides a film with uniform physical or optical properties such as chemical composition or index of refraction. In some embodiments, target 12 is substantially planar in order to provide uniformity in the film deposited on substrate 16. In practice, planarity of target 12 can mean that all portions of the target surface in region 52 are within a few millimeters of a planar surface, and can be typically within 0.5 mm of a planar surface.

[0046] Figure 3A illustrates deposition of a layer 102 according to the present invention deposited on a substrate 101. In some embodiments, layer 102 can be a conducting protective layer of TiO_y. Figure 3B shows a first layer 102 according to the present invention deposited over a second layer 103, which can also be a layer according to some embodiments of the present invention. In some embodiments, first layer 102 can be a conducting protective layer and second layer 103 can be a titanium or other conducting layer. Layer 103 is deposited on substrate 101.

[0047] The fabrication of high density capacitor and resistor arrays as well as high energy storage solid state devices can be accomplished with embodiments of processes according to the present invention on a wide variety of substrates such as silicon wafers or glass or plastic sheets at low temperature and over wide area. With reference to Figure 3B, layer 102 can be an amorphous film of TiO_2, which is deposited by a process such as that described in U.S. Application Serial No. 10/101,341. Utilization or formation of a conducting layer 103 such as TiO or Ti_4O_7 between a conducting layer of titanium, which is substrate 101, and the dielectric TiO_2 layer 102 is shown in the present invention to substantially reduce or eliminate the 'roll off' of the dielectric constant k with decreasing film thickness below about 1000 Angstroms. Consequently, capacitors fabricated from titanium on low temperature substrates result in high value planar capacitors and capacitor arrays with very high capacitive density and low electrical leakage. Such electrical arrays are useful for shielding and filtering and buffering high frequency and may be used in stationary as well as in portable electronic devices.

[0048] In particular, the low temperature deposition of amorphous titania capacitors provides for the fabrication of integrated passive electronic circuits on plastic and glass. It also provides for the integration of such devices on other electronic devices and arrays at low temperature.

[0049] Similarly, a conducting layer of TiO or Ti_4O_7 as layer 103 in Figure 3B, deposited between a conducting layer of titanium as layer 101 and a layer of titania as layer 102 of Figure 3B can be deposited so as to provide an increase in the surface smoothness by planarization of the titanium in layer 101 or other metallurgical conductive substrate layer 101 of Figure 3B. Consequently, roughness or asperity based defects can be minimized or eliminated. As an example, charge injection from a metallurgical electrode can be decreased at the interface with a dielectric. The titanium based dielectric layer can be formed on a smooth conducting oxide layer, which according to some theories can prevent charge depletion of the high k dielectric layer, decrease point charge accumulation and support dipole formation at the conductor-dielectric interface, sometimes referred to as dipole coupling. These features are important to prevent the roll-off of the dielectric strength of the dielectric layer as the layer thickness is decreased below about 1000 Å. It is consequently useful in the formation of thin layers having high capacitive value.

[0050] A thick film of dielectric material may be deposited having a high dielectric strength for the storage of electrical energy. Such energy is well known to increases with the square of the applied Voltage. For example, in Figure 3B layer 102 can be a thick layer of dielectric according to the present invention. Layer 104 in Figure 3B, then, can be a conducting layer deposited on layer 102 while layer 103 is a conducting layer deposited between a substrate 101 and layer 102 to form a capacitor. As the dielectric strength of the amorphous dielectric layer of layer 102 increases in proportion to it's thickness, the energy storage also increases effectively as the square of the thickness. It is shown that both record capacitance density and electrical energy storage density result for films according to the present invention. For thick film applications, smoothing of the metallurgical electrode by a conductive sub-oxide can decrease leakage at the interface in high voltage applications.

[0051] Protective conductive sub-oxide films of titanium can also be deposited on conductive and insulating substrates to protect them from harmful chemical attack while acting as conducting layers. For example, as illustrated in Figure 3A layer 102 can be a protective conductive sub-oxide film deposited on substrate 101. These layers can be used to protect an electrode, which can be substrate 101, from oxidation in the gas phase and in the liquid phase as well as the solid phase. Examples of such applications include electrolytic energy storage or as an active electrode surface for catalytic reactions and energy conversion such as in the oxygen-hydrogen fuel cell. Transparent oxides and semi-transparent sub-oxides can be deposited sequentially so that the conducting sub-oxides are protected by the transparent non-conducting oxides for purposes of photovoltaic or electrochromic energy conversion devices. It is well known that organic based photovoltaic cells are enhanced by the presence of titania in the organic absorbing layer. Layers according to the present invention can be utilized both for the conductivity of electricity, the enhancement of the organic absorber, as well as the overall protection of the device.

[0052] TiO_2 layers, for example, can photocatylitically produce ozone in the presence of sunlight. However, in the course of such activity, the TiO_2 layer can build up a fixed charge. Absent a metallurgical conductor, as shown in Figure 3B layer 102 can be a catalytic oxide while layer 103 can be a conducting suboxide while substrate 101 is a dielectric substrate such as glass or plastic and layer 104 is absent. In such a two-layer device, where the oxide is provided on the surface of the sub-oxide, the sub-oxide can form an electrode so that electric charge can be conducted to the oxide layer for enhanced photochemical photalysis such as in an AC device, or for the purpose of charge dissipation.

[0053] Protective conductive sub-oxide films of titanium can also be deposited on conductive and insulating substrates to protect them from harmful chemical attack while acting as conducting layers for electrolytic energy storage or as an active electrode for catalytic energy conversion. Transparent and semi-transparent oxides can be deposited sequentially so that the conducting suboxides are protected by the transparent non-conducting oxide for purposes of protecting layered devices. Alternatively, it is well known that certain crystalline suboxides of titania, collectively referred to as Magnelli phases, posses unusual levels of durability to mineral acid solutions and other corrosive gassious or liquid environments. Hayfield, P.C.S., "Development of a New Material- Monolithic Ti_4O_7 Ebonix Ceramic", Royal Society Chemistry, ISBN 0-85405-984-3, 2002 describes these in detail and discusses many applications of the monolithic suboxides. Hayfield also explains that the basis of conductivity of sub-oxides is due to the presence of the Ti^{+2} cation in layers having the stoichometry TiO. Of the several compositions, Ti_4O_7 in particular is known to posses both useful conductivity and also chemical resistance to both anodization, which would decrease it's conductivity, as well as reduction, which would decrease it's chemical durability. Therefore, as shown in Figure 3A, substrate 101 can be a metallurgical substrate such as aluminum or titanium and layer 102 can be Ti_4O_7. An example is the catalytic of H_2 and O_2 to make water and electricity.

[0054] In this disclosure, an amorphous coating layer according to embodiments of the present invention, derived from a crystalline target of Ti_4O_7, can obtain a similar composition as described above, measured as $Ti_4O_{6.8}$. Similar useful levels of chemical conductivity can be obtained. The sputtered film was dense, adherent, and also displayed robust durability to immersion in concentrated mineral acid and oxidizing solution. A similar material was deposited directly from a titanium target using the subject reactive sputtering process.

[0055] The increased density of the amorphous sputtered film according to embodiments of the present invention such as film 102 shown in Figure 3A can provide high levels of impermeability. Planarization can also be achieved by layer 102 over structures on substrate 101. Layer 102 can therefore achieve 'atomic' smooth surfaces on otherwise rough substrates. The sputtering process according to the present invention also allows the formation of a continuous range of stoicheometry between what are, in their crystalline environment, 'line compounds' with whole number integer ratios of titanium cations to oxygen atoms. In the present amorphous films, as long as one Ti^{+2} has a nearest neighbor cation in the amorphous glass matrix with the Ti^{+2} valence, conductive paths will be available in the sputtered film.

[0056] The sputtered sub-oxides also have the advantage that they can be layered, without removal from the vacuum system, with metallic titanium, other sub-oxides, as well as TiO_2 for connection to electrical conduction and insulation. This feature provides the utility of multiplayer depositions by integrated processes in one vacuum chamber. Where thick films of a particular sub-oxide are desired, a target 12 (Figure 1) fabricated of the desired sub-oxide can be utilized. TiO is particularly a good conductor and possesses very stable resistivity with temperature variation. Ti_2O_3 is a semiconductor. The higher oxygen-containing Magnelli compositions obtain higher resistivity as well as increased chemical stability and robustness and can be utilized as a resistive layer or as a protective, conductive layer.

[0057] Erbium doped TiO_2 is known to display useful levels of photoluminescence. And rare earth doped titanium oxide is known to display decreased levels of electrical leakage current under conditions of high electrical field. Layer 102 of Figure 3B, deposited according to some embodiments of the present invention, then can be erbium doped TiO_2 and therefore displays very high level of breakdown and very low leakage under electrical stress. Additionally, a capacitor can be formed by deposition of conductors as layers 103 and 104 on a substrate 101. Consequently, capacitive and energy storage devices formed from rare earth doped layers formed according to the present invention are extremely useful for very high field applications such as capacitors, high voltage dielectric batteries, and electro luminescent devices and also for low-leakage devices.

[0058] A TiO or erebium-doped TiO target, target 12 of Figure 1A, can be formed by mixing of TiO powder or TiO powder and Erbium or Erbium-Oxide powder. TiO powder can be formed from the partial oxygenation in a controlled furnace. The mixed powder is then hipped under a controlled environment (for example hydrogen or CO_2) to a high density to form tiles. As discussed above, such tiles can be mounted to form target 12. Additionally, other rare-earth doped titanium containing targets can be formed in the same fashion.

[0059] As an example, a layer of erbium doped titania or titania containing alloy deposited by means of the present invention, could be coupled as a continuous oxide layer to a photo diode constructed proximate to dielectric layer 102 of Figure 3A. Such an arrangement could provide an optical means for the measurement of the applied electrical field or the leakage current.

[0060] Alternatively, such a rare earth doped dielectric layer 102 might be coupled to conducting transparent oxides so that a light wave device might be provided for the conversion of electrical energy to light energy. In another embodiment, a titanium oxide containing a rare earth ion can be deposited directly on a light emitting diode device so that the rare earth ion can absorb some or all of the light emitted by the diode and re-fluoresce that light at another wavelength. In this embodiment, layer 102 can be a rare earth containing titanium oxide or sub oxide and substrate 101 includes a light emitting diode. An example of this may be the conversion of blue light from a LED to yellow-green light by layer 102. In that case, layer 102 may be cerium doped titanium oxide or sub-oxide. Partial absorption of the blue light by layer 102 with conversion to yellow-green light by layer 102 would result in a white light source. Other colors of light can be obtained by doping the titanium oxide or sub-oxide with other rare earth ions.

[0061] Figures 4A and 4B illustrate further stackings of layers according to embodiments of the present invention. For example, layer 201 can be a TiO_2 dielectric protective deposited over a conducting layer 103 on substrate 101. Figure 4B can show dielectric protective layer 201 deposited over conducting protective layer 102 of TiO_y, which is deposited on a metal conducting layer 103 on substrate 101. The TiO_y conducting protective layer can act as a smoothing layer, resulting in a better barrier layer in dielectric 201. The end result is a better roll-off characteristic than has previously been obtained.

[0062] In general, layer 102 can be formed of any Ti_xO_y layer or rare earth doped Ti_xO_y layer according to the present invention. As illustrated here, layers of various compositions of Ti_xO_y, with or without rare-earth doping, have various properties. In some embodiments of the invention, x can be between about 1 and about 4 and y can be between about 1 and about 7.

[0063] Figure 5 shows an example of a capacitor stack according to the present invention. A metal conducting layer 103 is deposited on substrate 101. A conducting protective layer 102 is deposited over conducting layer 103 and a TiO_2 dielectric protective layer is deposited over the protective conducting layer 102. Another protective conducting layer 102 can be deposited over the TiO_2 dielectric layer and a metal layer can be deposited over the protective conducting layer 102. The resulting capacitor stack has upper and lower smoothing due to the two TiO_y layers and results in improved roll-off characteristics in the dielectric constant. Such capacitor stacks can be very useful in energy storage devices.

[0064] Figure 6 shows a transistor structure according to the present invention. A source 401, drain 402 and gate structure 404 are deposited on a semiconducting substrate 403. An intermediate dielectric 400 can then be deposited over the source, drain and gate structure. A protective conducting layer 102, which can be formed of TiO_y, can then be deposited over an opening in the intermediate dielectric layer 400 followed by a conducting layer 103. The protective conducting layer 102 prevents roll-off of the gate dielectric 404.

Example 1. Deposition of Ti_4O_7 film

[0065] In this example, Ti_4O_7 films were deposited using a Pulse DC scanning magnetron PVD process as was previously described in U.S. Application Serial No. 10/101,341. The target was a about 1mm thick, about 16.5x12.5 mm^2 tiles of titanium oxide target obtained from a sheet of Ebonex™ which compounded of bulk Ti_4O_7 was bonded onto a backing plate. Ebonex™ can be obtained from Atraverda Ltd., Oakham Business Park, Mansfield, UK. A pulsed DC generator from Advanced Energy (Pinnacle Plus) was used as the target power supply. The pulsing frequency can be varied from 0-350 KHz. Reversed duty cycle can be varied from 1.3μs to 5μs depending on the pulsing frequency. Target power was fixed at 2 KW and pulsing frequency was 200KHz during deposition, Ar flow rate is 100sccm. The deposition rate at this condition is 14Å/sec over a 40 by 50 cm substrate 101. A 100 W at 2 MHz bias was supplied to the substrate. The bias power supply can be an RF supply produced by ENI.

[0066] Utilizing the above parameters, a layer 102 of Figure 3A was deposited on a substrate 101 of 150mm p-type Si wafer. The sheet resistance was measured using 4 point probe to be 140 ohms/sq, with film thickness of 1.68μm. The resistivity of the resulting film is measured to be 0.023 ohms-cm. The composition of film was determined using EDX to be $Ti_4O_{6.8}$.

Example 2. Deposition of TiO2 on Ti-Ti4O7 film Stack

[0067] In this example, TiO_2 films were deposited using a 2MHz RF biased, Pulse DC scanning magnetron PVD process as was previously described in U.S. Application Serial No. 10/101,341. The substrate size can be up to 600x720mm^2. The target was a ~7mm thick, ~630x750 mm^2 Ti plate of 99.9% purity. A pulsed DC generator, or PDC power supply from Advanced Energy (Pinnacle Plus) was used as the target power supply. The pulsing frequency can be varied from 0-350 KHz. Reversed duty cycle can be varied from 1.3μs to 5μs depending on the pulsing frequency. An ENI RF generator and ENI Impedance matching unit were used for the substrate bias. A 100 W with a 2 MHz RF generator, which can be an EFI supply, was utilized. The chamber base pressure was kept below 2×10^{-7} Torr. The substrate temperature was below 200°C during deposition.

[0068] A systematic DOE (design of experiments) were carried out on both n++ type bare Si wafers and Al metallized wafers. All n++ wafers were HF cleaned just before loading into the chamber for deposition. A series of 150nm thick, Al films were deposited onto the bare Si wafers using the same PVD system at low temperature (<100°C).

[0069] The total PDC target power, pulsing frequency, oxygen partial pressure, and substrate bias power were variables in the DOE. Total gas flow of Ar and O_2 were kept constant at 100 sccm. The PDC target power was between 4 and 7 kW with a pulsing frequency of between 100 and 250 kHz. The oxygen flow rate ranged from 30 to 60%. The bias power ranged from 0 to 300 W at 2 Mhz. Both dielectric strength and breakdown voltage were measured using a mercury probe. Film thickness in this DOE range from 100nm to 270nm.

[0070] Therefore, with reference to Figure 3B, layer 101 is the Si wafer substrate, layer 103 is the 150 nm thick Al layer, layer 102 is the Ti_4O_7 layer, and layer 104 is TiO_2. Figure 7 shows the thickness dependence of the dielectric constant of layer 102, showing the roll off effect. The capacitance of the layer stack 101, 103, 102, and 104 was measured with a mercury electrode impressed upon layer 104 and coupled to layer 103. The precise thickness of dielectric layer 104 was measured optically. The dielectric constant of layer 104 was then calculated from the measured capacitance. As shown in Figure 7, the TiO_2 film thickness decreases, so does the dielectric constant of the TiO_2 film.

[0071] However, this roll-off effect can be greatly reduced or eliminated in certain embodiments of the present invention. Figure 8 shows two additional data points shown as circles which represent the dielectric constant of thin TiO_2 layers for layer 104 with Ti-Ti_4O_7 deposited as layer 102 of Figure 3B.

Example 3. Deposition of TiO_2 on Ti-TiO_x ($x<2$) film Stack

[0072] A layer of TiO_2 was deposited on a titanium coated substrate. About 2000 Å of Ti metal was deposited at 7KW of PDC target power, with Ar flow of 100 sccm and bias power of 200W. After Ti deposition, TiO_2 was deposited in the same chamber without oxide burn in. This process resulted in a Ti-TiO_y –TiO_2 ($y<2$) film stack. The k value of a 200Å film was as high as 60.

[0073] Figures 9A and 9B illustrate an SEM cross-section of a Ti_4O_7 Ebonex™ target (Figure 9A) and an SEM cross section of the $Ti_4O_{6.8}$ layer (Figure 9B) deposited from the Ebonex™ target according to the present invention. The deposited film shows smooth deposition of the layer. The Ebonex™ target shown in Figure 9A shows an open porousity material with high roughness. The deposited layer shown in Figure 9B, however, shows a highly dense layer with a smooth surface condition.

[0074] Table I shows the effects of the dielectric properties of TiO_2 deposited according the present invention in comparison with previously obtained values. The values for the previously obtained reactive sputtering was taken from the paper "Frequency-Dependent Pulsed Direct Current magnetron Sputtering of Titanium Oxide Films," by J. Y. Kim et al., J. Vac. Sci. Techn., A 19(2), Mar/Apr. 2001. The values for PDC PVD with bias was experimentally obtained from layers deposited as described in Example 2 above.

Table I

Process	V_{bd} (Mv/cm)	K	FM
Reactive Sputtering	0.46 ~ 1.35	34 ~ 65.9	19 ~ 50
PDC physical Vapor Deposition with Bias	3.48	83	288

[0075] As can be seen from Table I, the breakdown voltage V_{bd} is significantly improved in layers according to the present invention. Further, the dielectric constant of the resulting layer is also higher. The figure of merit (FM) then for the deposited layer was 288, very much higher than that report by Kim et al. The reference Kim et al. was the reference reporting the best quality TiO_2 films available at the time of filing of the prior application to which this disclosure claims priority.

[0076] Figure 10 shows data of capacitance made with layers according to the present invention in processes as described in Example 2 above are shown in comparison with available industry values. As is observed in Figure 10, layers of TiO_2 deposited according to the present invention have higher dielectric breakdown voltages than other dielectric films utilized in industry, which is represented by the solid line. However, due to the roll-off in dielectric constant K in films below about 1000 Å in thickness (as is indicated in the top two points in Figure 10), a capacitance density above about 5000 or 6000 pF/mm2 could not be achieved using thinner films. This is also shown in Figure 7.

[0077] However, combined with the use of a conductive sub-oxide and the higher dielectric constant of thinner films as shown in Figure 11, a capacitance density of 12000 pF/mm2 can be achieved with a 500 Å thickness film and a capacitance density of greater than 24000 pF/mm2 can be achieved with a 220 Å film, as is shown in Figure 11. These film stacks were deposited as described in Example 3 above.

[0078] Figure 12 shows a deposited layer 102 on a substrate 101 formed of n++ silicon wafer. Layer 102 is formed of TiO_2 deposited according to the present invention. As shown in the SEM cross-section, the TiO_2 layer shows several layers. A layer 1201 is formed of SiO_2 formed on substrate 101 and is formed about 20 Å thick. An amorphous layer 1202 of thickness about 250 Å is then formed above layer 1201. Finally, a crystalling TiO_2 layer 1203 is formed about 4000 Å thick. In some embodiments of the present invention, a continuous deposition on a substrate results in a first amorphous layer deposited at initially cooler temperature followed by a further crystalline layer deposited during the increased temperature of the process. A diffraction pattern inset in Figure 12 illustrates the crystalline nature of layer 1203.

[0079] Table II tabulates data taken from a number of bi-layer film such as that shown in Figure 12 and completely amorphous films formed by repeated initial deposition layers at cool deposition conditions. Films near 1000 Å of thickness are compared and display similar values for the dielectric constant. However, the amorphous film exhibits much higher dielectric breakdown strengths. Due to the similar thickness and values of the dielectric constant, the two films exhibit similar values for capacitance. However, the amorphous film illustrates superior breakdown voltage and therefore has a higher figure of merit (FM). These trends are more pronounced in the thicker films with thicknesses close to 2000 Å. In this case, the values of the dielectric constant and capacitance are nearly identical but again there is a significantly higher breakdown voltage in the amorphous film, which results in a significant improvement in the figure of merit for the amorphous films.

Table II

Film Thickness (nm)	k	V_{bd} (MV/cm)	FM	C (pF/mm2)	Breakdown Voltage (V)	Film Morphology
969	63	3.6	227	540	348	Bi-layer
1036	62	6.4	396	538	660	Amorphous
2020	98	3.5	335	429	705	Bi-Layer
2322	98	5.5	539	429	1110	Amorphous

[0080] Therefore, it is clear that amorphous TiO_2 films have much better performance. As discussed above, those layers are the result of low temperature depositions. Therefore, as was demonstrated with the data shown in Table II, one method of producing thick amorphous TiO_2 layers is to simply utilize a sequence of low temperature depositions, halting the deposition prior to thermal heating of the depositing film. However, this method can take a significant amount of production time for thick films. Another embodiment of obtaining thick TiO_2 amorphous films is to apply active cooling to the substrate in an amount sufficient to provide continuously amorphous TiO_2 films.

[0081] Figure 13 shows a comparison of the leakage current for TiO_2 films according to embodiments of the present invention with and without erbium ion doping. The lower data points in Figure 13 are from capacitors formed from films deposited from a 10 at. % Er doped TiO target. The target was electrically conductive. One example of the 10% doped film of 1000 Å thickness was formed with 60 sccm Ar, 6 sccm O_2, with a target power of 3 kW, bias power of 100 W, with a deposition time of 200 sec on a metal coated glass wafer. With the metal coating forming a copper titanium lower electrode and a titanium copper gold upper electrode patterned as 1X1 mm, discreet capacitors was then formed. The layers corresponding to the upper data points were deposited from a pure titanium target with no erbium doping on a TaN substrate with a evaporated platinum upper electrode. This structure of the bottom data is illustrated in Figure 4B where, for example, layer 101 is a glass substrate, layer 103 is a copper titanium layer, layer 102 is the erbium doped TiO_2 layer, and layer 201 is a titanium copper gold layer.

[0082] As can be seen in Figure 13, the leakage current density is reduced by many orders of magnitude by addition of erbium.

[0083] Figures 14A and 14B show a photoluminescence signal with excitation at 580 nm and measurement at 1.53 µm, measured from a 5000 Å layer of 10% erbium containing TiO_2 deposited from a 10% erbium doped TiO conductive target and a photoluminescence signal measured from the same layer after a 30 minute 250 °C anneal, respectively. Table III shows similar data for several layers deposited from the erbium-doped TiO conductive target.

Table III

Thickness	Before Anneal	Anneal (°C)	After Anneal
5000 Å	6704	150	5809
5000 Å	6493	200	4042
5000 Å	6669	250	2736
5000 Å	6493	300	3983
1 µm	6884	150	6743
1 µm	5197	200	3685
1 µm	6253	250	3612
1 µm	5324	300	3381

[0084] According to some explanations of the reduction of leakage current in layers as illustrated by Figure 13, fast electrons that have sufficient energy to excite the erbium ion would cause the rare earth ion to undergo excitation upon electron impact or passage within a distance sufficient for energy exchange. Consequently, the leakage current electrons capable of causing ionization within the dielectric oxide would be reduced by electron collisions with erbium ions. Excited state ions have at least two relaxation mechanisms for disposal of the energy: radiative and non-radiative. In radiative relaxation, the excited ion emits light. In non-radiative relaxation, the excited ion undergoes a cooperative process with vibrational modes of it's host dielectric oxide and produces a vibration which is the elemental form of heat. In the data illustrated in Figure 13, it was not possible to observe light in the leakage test, but photoluminescence was observed from optical excitation of the similar 10% Er doped TiO_2 deposited from the 10% Er doped TiO conductive target, as shown in Table III.

[0085] As can be seen from the data in Table III, an erbium doped layer of titanium oxide was shown to fluoresce strongly under optical excitation by light of a wavelength 580 nm, using a Phillips PhotoLuminescence Microscope, model no. PLM-100. The target was electrically conductive and sputtered at a higher rate and a lower oxygen partial pressure than characteristic of a metallic titanium target. One example of the 10% doped film of 2,032 angstroms was 60 sccm Ar, 6 sccm O_2, with a target power of 3 kW, bias power of 100 W, with a deposition time of 300 sec.

[0086] The level of photoluminescence observed from the layer was similar to that obtained in as-deposited and annealed films providing commercial levels of optical absorption and fluorescence for applications to planar waveguide amplifiers having at least 15 dB gain for signals as weak as -40dB at the 1.5 micron wavelength utilized for photonic C band communications.

[0087] Such a device can be illustrated with Figure 3B, where layer 103 can be a conductive layer deposited on substrate 101, layer 102 can be a rare-earth doped TiO_2 layer deposited according to embodiments of the present invention, and layer 104 can be a further conductive layer or a conductive transparent layer to form an metal-insulating-metal (MIM) capacitor structure. Such a structure could function as a light emitting layer under either DC or AC electrical excitation. In another embodiment, layer 103 can be a lift-off layer such as CaF_2 or other organic material, layer 102 is the rare-earth doped TiO_2 layer, and layer 104 is absent, then upon lift-off or upon transfer of layer 102, a free standing or applied layer having electroluminescent or photoluminescent applications can be provided over a selected device.

[0088] Thin films according to the present invention can be utilized in advanced display devices, electrical energy storage and conversion, and to form optical and electronic films with scratch resistance and barrier properties. Advanced display product applications include OLED encapsulation, barriers for flexible polymer substrates, outcoupling mirrors and anti-reflection coatings, transparent conducting oxides, and semiconducting materials for active matrix displays. Electrical energy storage and conversion applications include high density capacitor arrays for mobile communication devices, on-chip high "K" capacitors for advanced CMOS, and high voltage energy storage for portable power devices. Other applications include touch-sensitive devices and durable bar code scanners and see-through sensors as well as implantable biometric devices.

[0089] The embodiments described in this disclosure are examples only and are not intended to be limiting. Further, the present invention is not intended to be limited by any particular theory or explanation presented to explain experimental results. As such, examples of titanium oxide and titanium sub-oxide films illustrated herein and their applications are not intended to be limiting. One skilled in the art may contemplate further applications or films that are intended to be within the spirit and scope of the present invention. As such, the invention is limited only by the following claims.

Claims

We claim:

1. A method of forming a titanium based layer, comprising:

depositing a layer of titanium containing oxide by pulsed-DC, biased reactive sputtering process on a substrate.

2. The method of claim 1, wherein the layer is TiO_2.

3. The method of claim 2, wherein the figure of merit of the layer is greater than 50.

4. The method of claim 2, wherein the layer is deposited between conducting layers to form a capacitor.

5. The method of claim 2, wherein the layer includes at least one rare-earth ion.

6. The method of claim 5, wherein the layer is deposited between conducting layers to form a capacitor.

7. The method of claim 5, wherein the at least one rare-earth ion includes erbium.

8. The method of claim 5, wherein the layer is deposited between conducting layers to form a light-emitting device.

9. The method of claim 5, wherein the layer is an optically active layer deposited on a light-emitting device.

10. The method of claim 5, wherein the layer is an optically active layer applied to a light-emitting device.

11. The method of claim 1, wherein the layer is a sub-oxide of Titanium.

12. The method of claim 11, wherein the figure of merit of the layer is greater than 50.

13. The method of claim 11, wherein the layer is deposited between conducting layers to form a capacitor.

14. The method of claim 11, wherein the layer includes at least one rare-earth ion.

15. The method of claim 14, wherein the layer is deposited between conducting layers to form a capacitor.

16. The method of claim 14, wherein the at least one rare-earth ion includes erbium.

17. The method of claim 14, wherein the layer is deposited between conducting layers to form a light-emitting device.

18. The method of claim 14, wherein the layer is an optically active layer deposited on a light-emitting device.

19. The method of claim 14, wherein the layer is an optically active layer applied to a light-emitting device.

20. The method of claim 2, wherein the layer is a protective layer.

21. The method of claim 20, wherein the protective layer is a catalytic layer.

22. The method of claim 20, wherein the protective layer includes at least one rare-earth ion.

23. The method of claim 1, wherein the layer is Ti_xO_y wherein x is between about 1 and about 4 and y is between about 1 and about 7.

24. The method of claim 23, wherein the figure of merit of the layer is greater than 50.

25. The method of claim 23, further including depositing an TiO_2 layer on the layer wherein the layer and the TiO_2 layers are deposited between conducting layers to form a capacitor with decreased roll-off characteristics with decreasing thickness of the TiO_2 layer.

26. The method of claim 23, wherein the TiO_2 layer is an amorphous layer deposited by a pulsed DC, biased, reactive ion process.

27. The method of claim 23, wherein the layer includes at least one rare-earth ion.

28. The method of claim 27, wherein the at least one rare-earth ion includes erbium.

29. The method of claim 27, wherein the layer is deposited between conducting layers to form a light-emitting device.

30. The method of claim 27, wherein the layer is an optically active layer deposited on a light-emitting device.

31. The method of claim 27, wherein the layer is an optically active layer applied to a light-emitting device.

32. The method of claim 23, wherein the layer is a conducting oxide.

33. The method of claim 32, wherein the substrate is a conducting electrode and the layer is a protective layer.

34. The method of claim 33, wherein the protective layer is a catalytic layer.

35. The method of claim 33, wherein the protective layer includes at least one rare-earth ion.

36. The method of claim 32, wherein the substrate is a dielectric and the layer is a protective layer.

37. The method of claim 36, wherein the protective layer is a catalytic layer.

38. The method of claim 1, further including

controlling the temperature of the substrate during deposition.

39. The method of claim 38, wherein controlling the temperature includes active temperature control.

40. The method of claim 1, wherein the layer is an amorphous layer.

41. The method of claim 1, wherein the substrate includes a transistor structure.

42. A titanium based layer, comprising:

a layer compounded from titanium and oxygen deposited by pulsed-DC, biased reactive sputtering process on a substrate.

43. The layer of claim 42, wherein the layer is TiO_2.

44. The layer of claim 43, wherein the figure of merit of the layer is greater than 50.

45. The layer of claim 43, wherein the layer is deposited between conducting layers to form a capacitor.

46. The layer of claim 43, wherein the layer includes at least one rare-earth ion.

47. The layer of claim 46, wherein the layer is deposited between conducting layers to form a capacitor.

48. The layer of claim 46, wherein the at least one rare-earth ion includes erbium.

49. The layer of claim 46, wherein the layer is deposited between conducting layers to form a light-emitting device.

50. The layer of claim 46, wherein the layer is an optically active layer deposited on a light-emitting device.

51. The layer of claim 46, wherein the layer is an optically active layer applied to a light-emitting device.

52. The layer of claim 42, wherein the layer is sub-oxide of Titanium.

53. The layer of claim 52, wherein the figure of merit is greater than 50.

54. The layer of claim 52, wherein the layer is deposited between conducting layers to form a capacitor.

55. The layer of claim 52, wherein the layer includes at least one rare-earth ion.

56. The layer of claim 55, wherein the layer is deposited between conducting layers to form a capacitor.

57. The layer of claim 55, wherein the at least one rare-earth ion includes erbium.

58. The layer of claim 55, wherein the layer is deposited between conducting layers to form a light-emitting device.

59. The layer of claim 55, wherein the layer is an optically active layer deposited on a light-emitting device.

60. The layer of claim 55, wherein the layer is an optically active layer applied to a light-emitting device.

61. The layer of claim 43, wherein the layer is a protective layer.

62. The layer of claim 61, wherein the protective layer is a catalytic layer.

63. The layer of claim 61, wherein the protective layer includes at least one rare-earth ion.

64. The layer of claim 42, wherein the layer is Ti_xO_y wherein x is between about 1 and about 4 and y is between about 1 and about 7.

65. The layer of claim 64, wherein the figure of merit is greater than 50.

66. The layer of claim 64, further including depositing an TiO_2 layer on the layer wherein the layer and the TiO_2 layers are deposited between conducting layers to form a capacitor with decreased roll-off characteristics with decreasing thickness of the TiO_2 layer.

67. The layer of claim 64, wherein the TiO_2 layer is an amorphous layer deposited by a pulsed DC, biased, reactive ion process.

68. The layer of claim 64, wherein the layer includes at least one rare-earth ion.

69. The layer of claim 68, wherein the at least one rare-earth ion includes erbium.

70. The layer of claim 68, wherein the layer is deposited between conducting layers to form a light-emitting device.

71. The layer of claim 68, wherein the layer is an optically active layer deposited on a light-emitting device.

72. The layer of claim 68, wherein the layer is an optically active layer applied to a light-emitting device.

73. The layer of claim 64, wherein the layer is a conducting oxide.

74. The layer of claim 73, wherein the substrate is a conducting electrode and the layer is a protective layer.

75. The layer of claim 74, wherein the protective layer is a catalytic layer.

76. The layer of claim 74, wherein the protective layer includes at least one rare-earth ion.

77. The layer of claim 73, wherein the substrate is a dielectric and the layer is a protective layer.

78. The layer of claim 77, wherein the protective layer is a catalytic layer.

79. The layer of claim 42, further including

controlling the temperature of the substrate during deposition.

80. The layer of claim 79, wherein controlling the temperature includes active temperature control.

81. The layer of claim 42, wherein the substrate includes a transistor structure.

82. The layer of claim 42, wherein the layer is an amorphous layer.

83. A target, comprising:

hipped TiO having composition TiO.

84. The target of claim 83, further including at least one rare-earth dopant.

85. A method of forming a target, comprising:

forming a TiO powder;

mixing the TiO powder to form a mix;

hipping the mix under a controlled atmosphere to form tiles; and

forming a target from the tiles.

86. The method of claim 85, further including mixing at least one rare-earth oxide powder with the mix.

87. The method of claim 86, wherein the at least one rare-earth oxide includes erbium oxide.

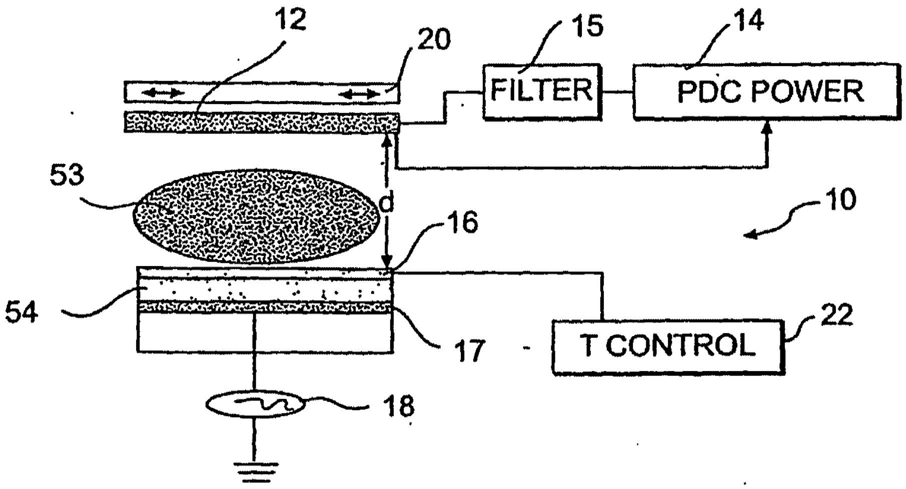
12
20
15
FILTER
14
PDC POWER
53
d
16
10
54
17
T CONTROL
22
18

FIG. 1A

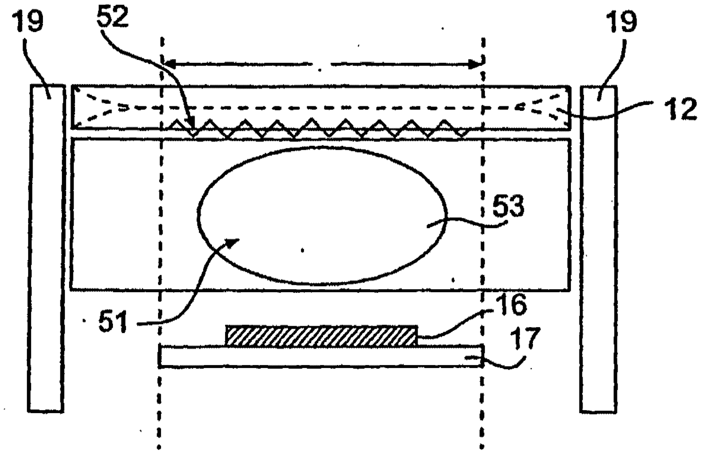
19
52
19
12
53
51
16
17

FIG. 1B

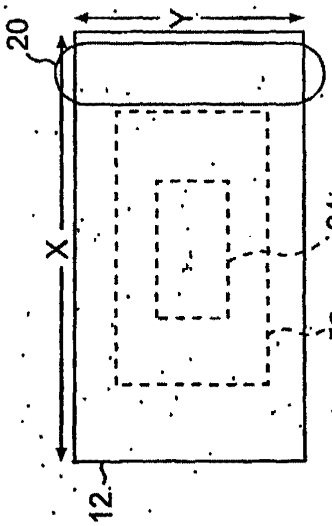

FIG. 2

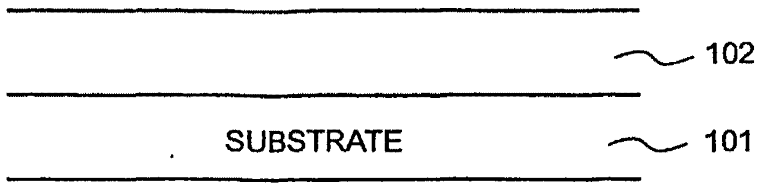

FIG. 3A

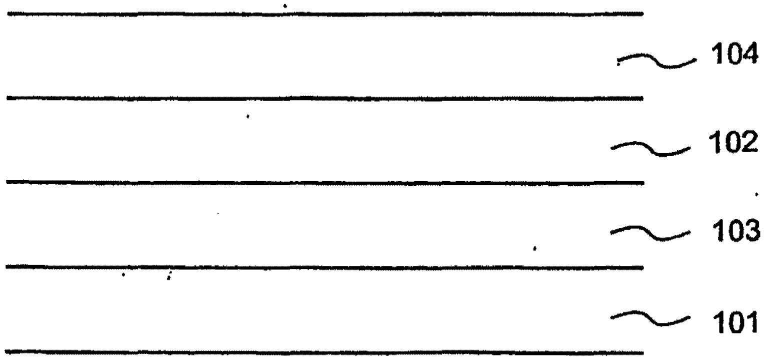

FIG. 3B

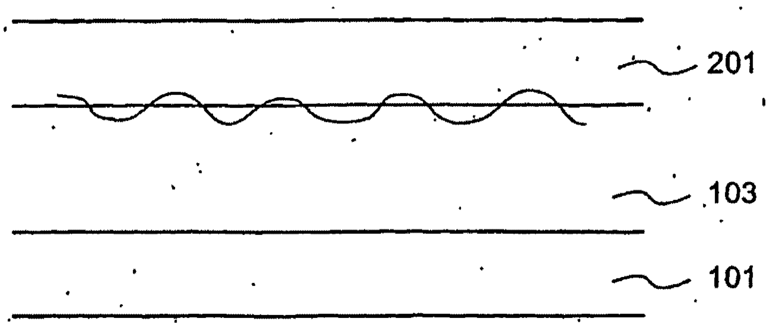

FIG. 4A

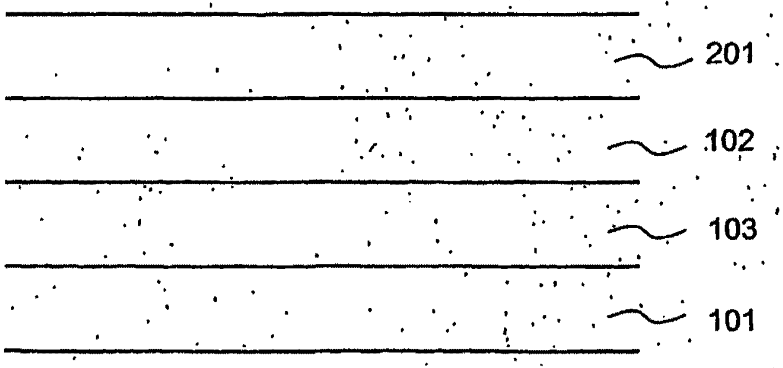

FIG. 4B

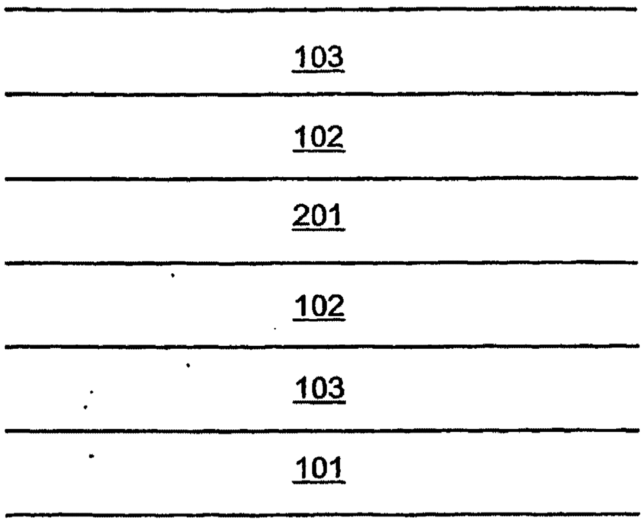

FIG. 5

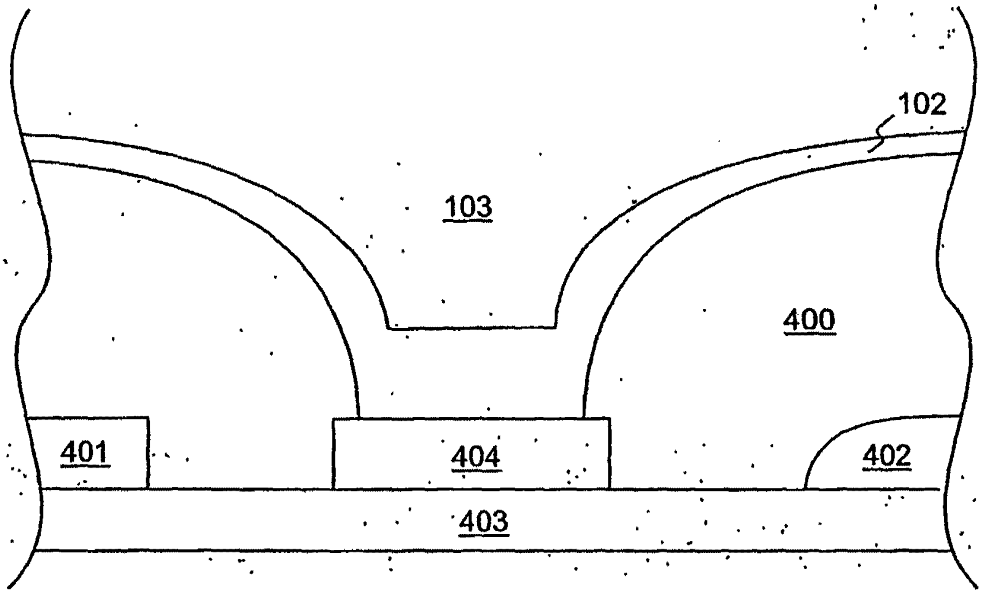

FIG. 6

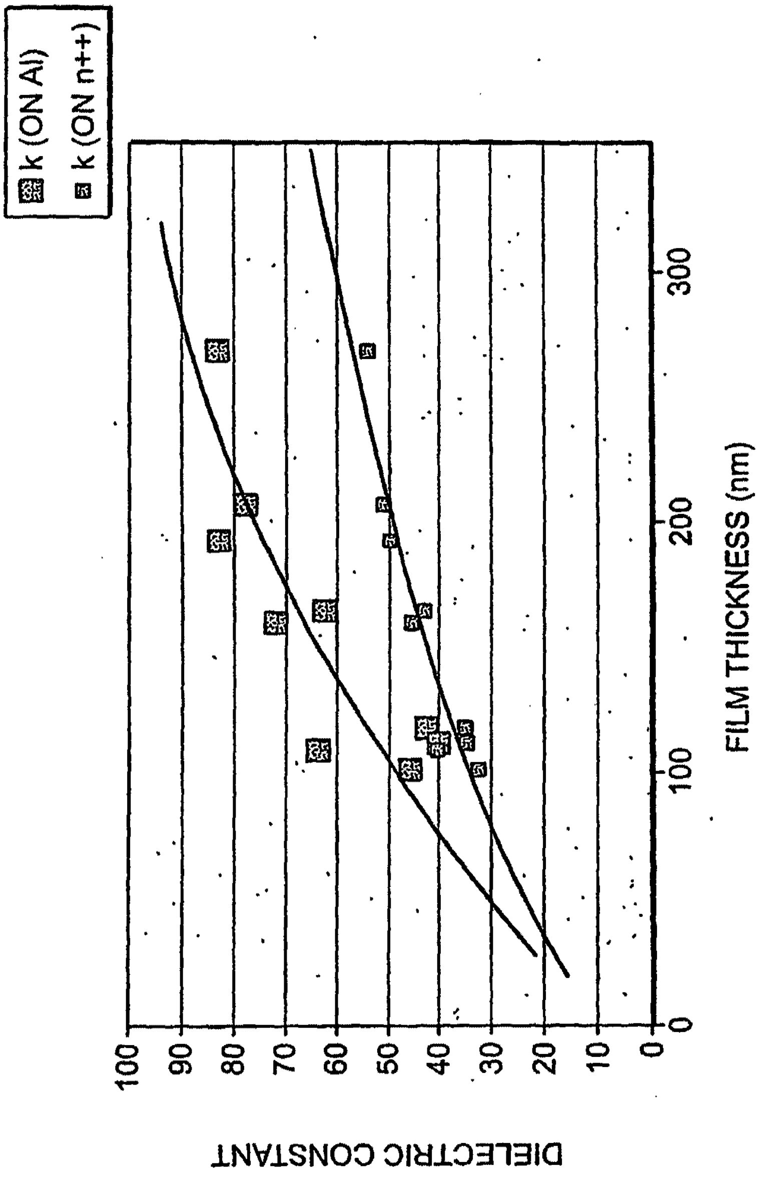
▨ k (ON Al)
▨ k (ON n++)
DIELECTRIC CONSTANT
100
90
80
70
60
50
40
30
20
10
0
FILM THICKNESS (nm)
0
100
200
300

FIG. 7

7

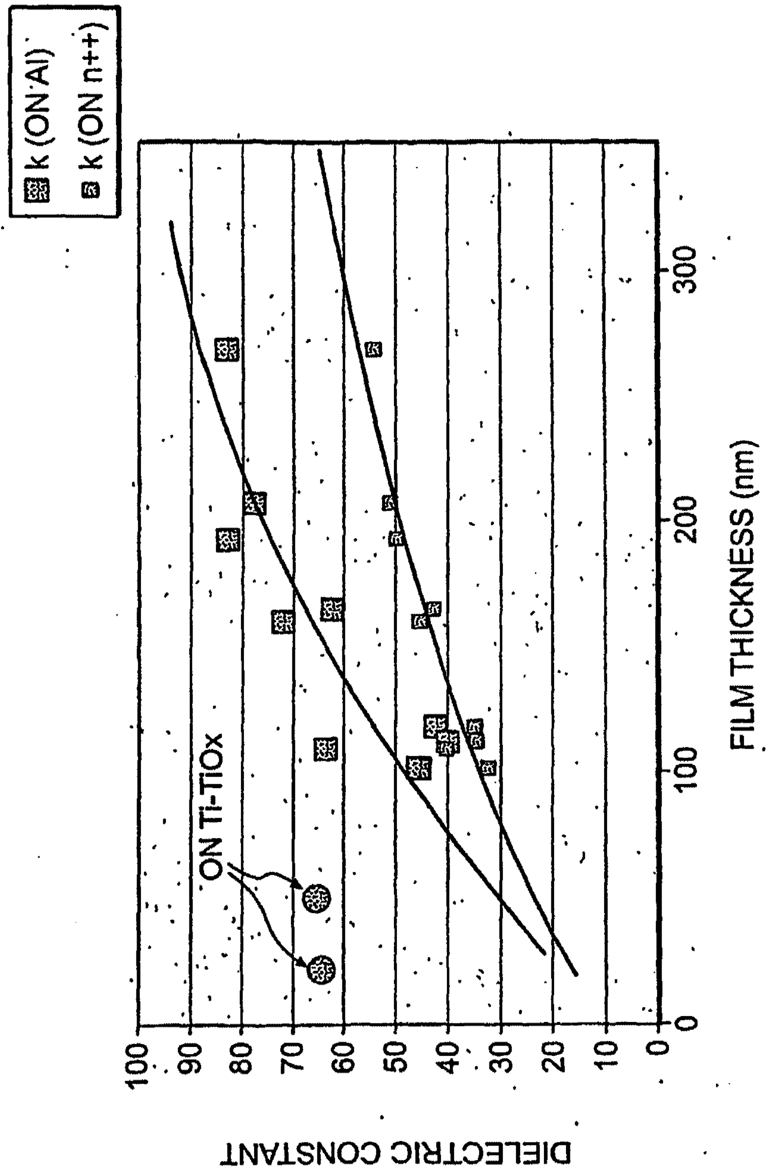
▨ k (ON Al)
▨ k (ON n++)
ON Ti-TiOx
DIELECTRIC CONSTANT
100
90
80
70
60
50
40
30
20
10
0
0
100
200
300
FILM THICKNESS (nm)

FIG. 8

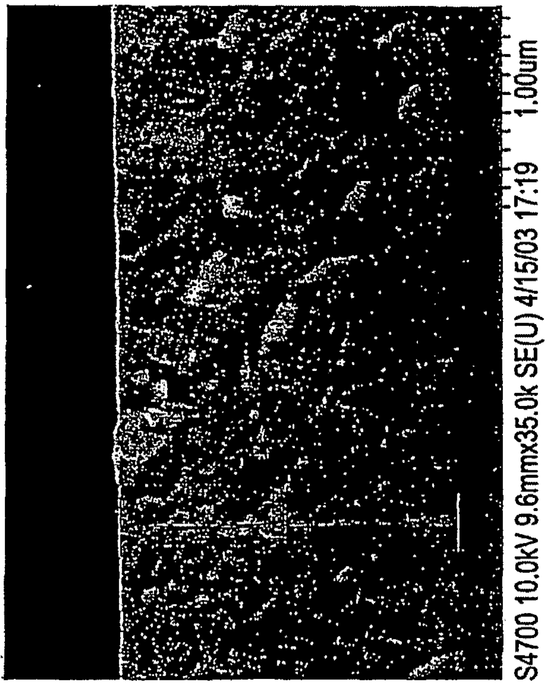
S4700 10.0KV 9.6mmx35.0k SE(U) 4/15/03 17:19 1.00um

FIG. 9B

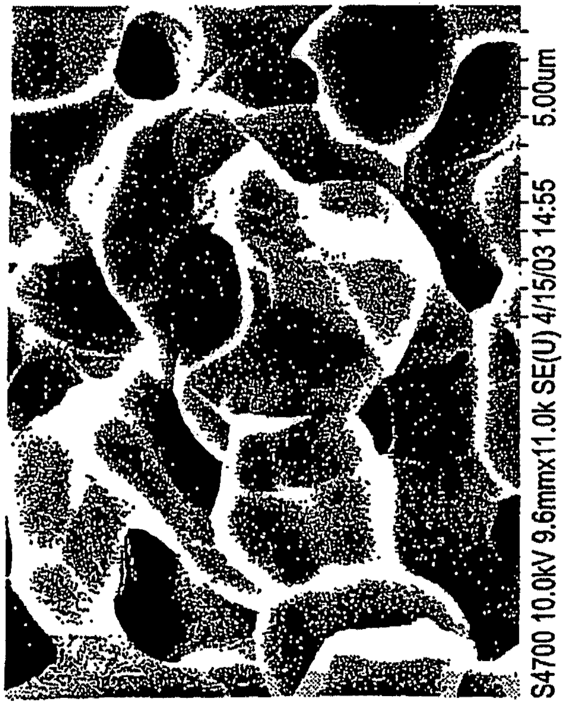
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FIG. 9A

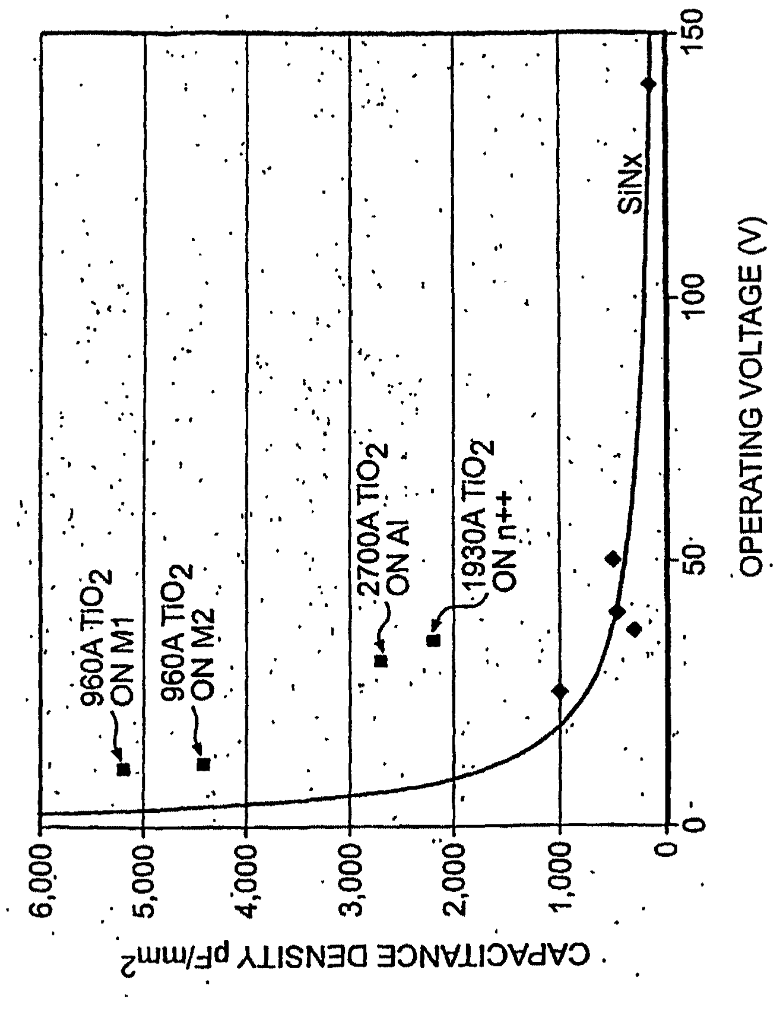

CAPACITANCE DENSITY pF/mm²
6,000
5,000
4,000
3,000
2,000
1,000
0
OPERATING VOLTAGE (V)
0
50
100
150
960A TiO2 ON M1
960A TiO2 ON M2
2700A TiO2 ON Al
1930A TiO2 ON n++
SiNx

FIG. 10

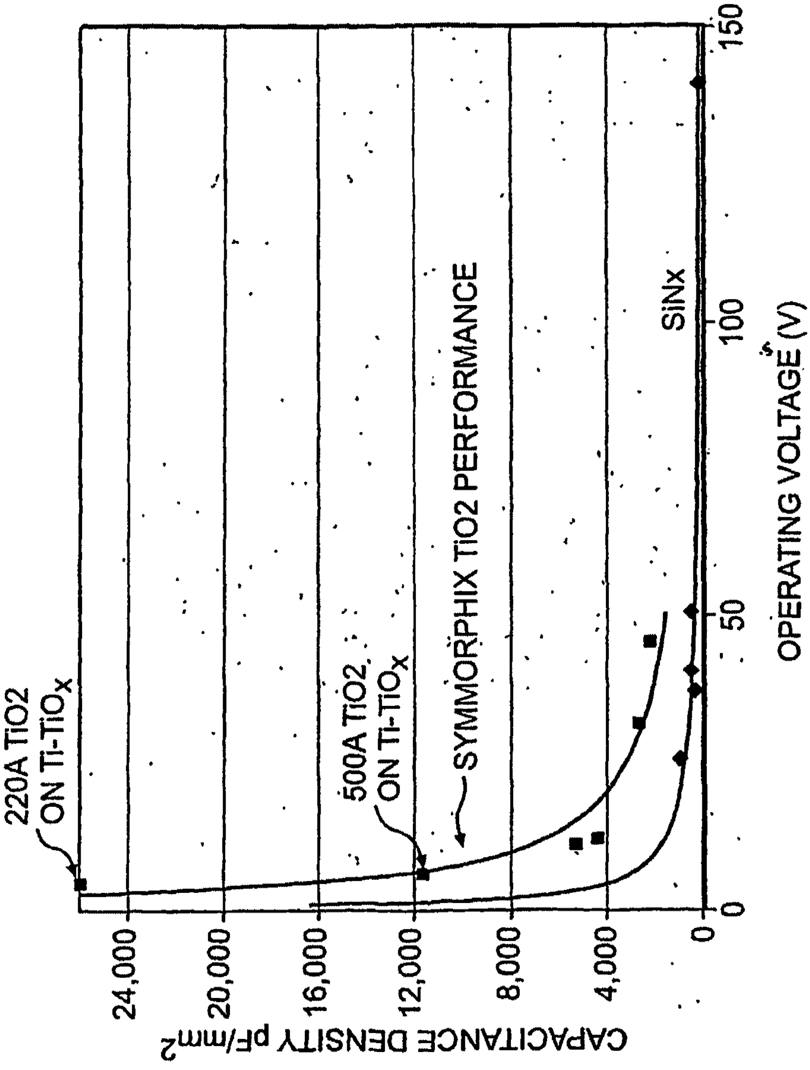

220A TiO2 ON Ti-TiO$_x$
500A TiO2 ON Ti-TiO$_x$
SYMMORPHIX TiO2 PERFORMANCE
SiNx
CAPACITANCE DENSITY pF/mm^2
24,000
20,000
16,000
12,000
8,000
4,000
0
0
50
100
150
OPERATING VOLTAGE (V)

FIG. 11

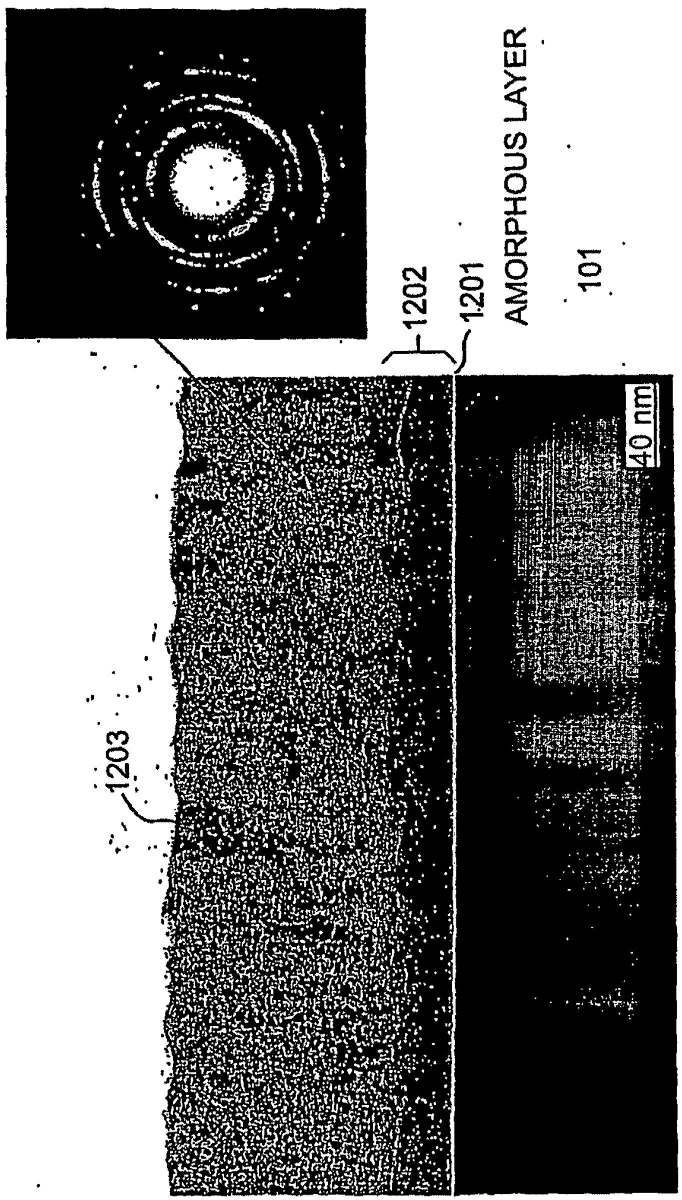


FIG. 12

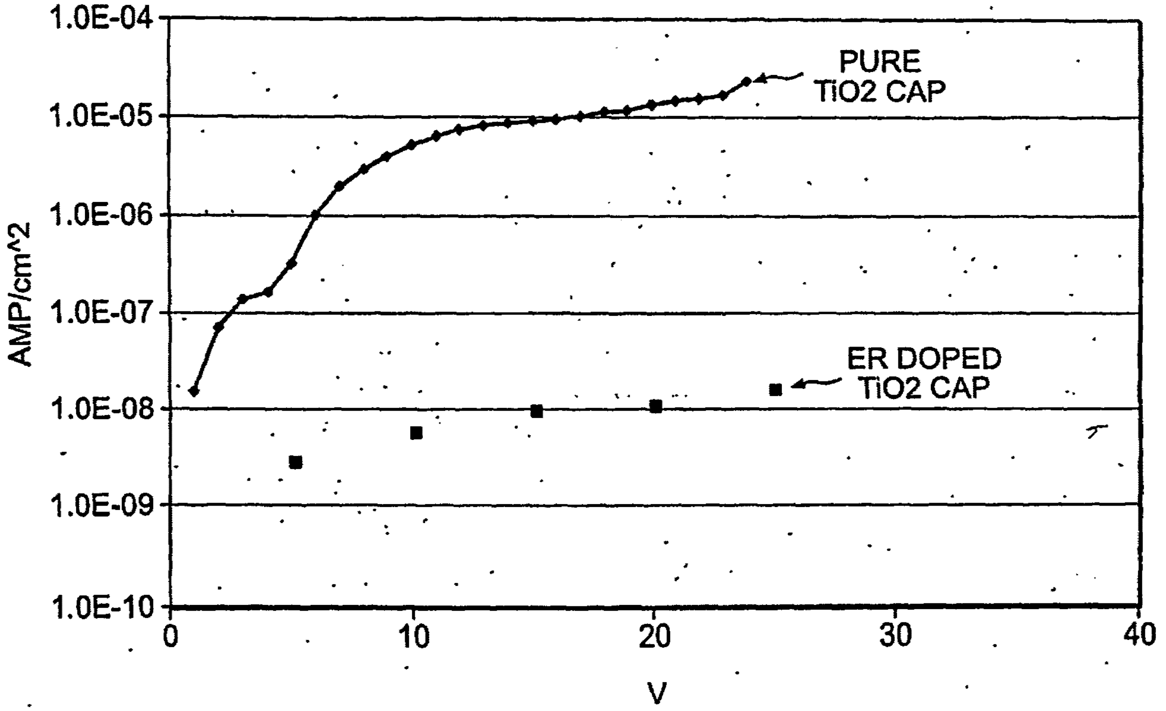
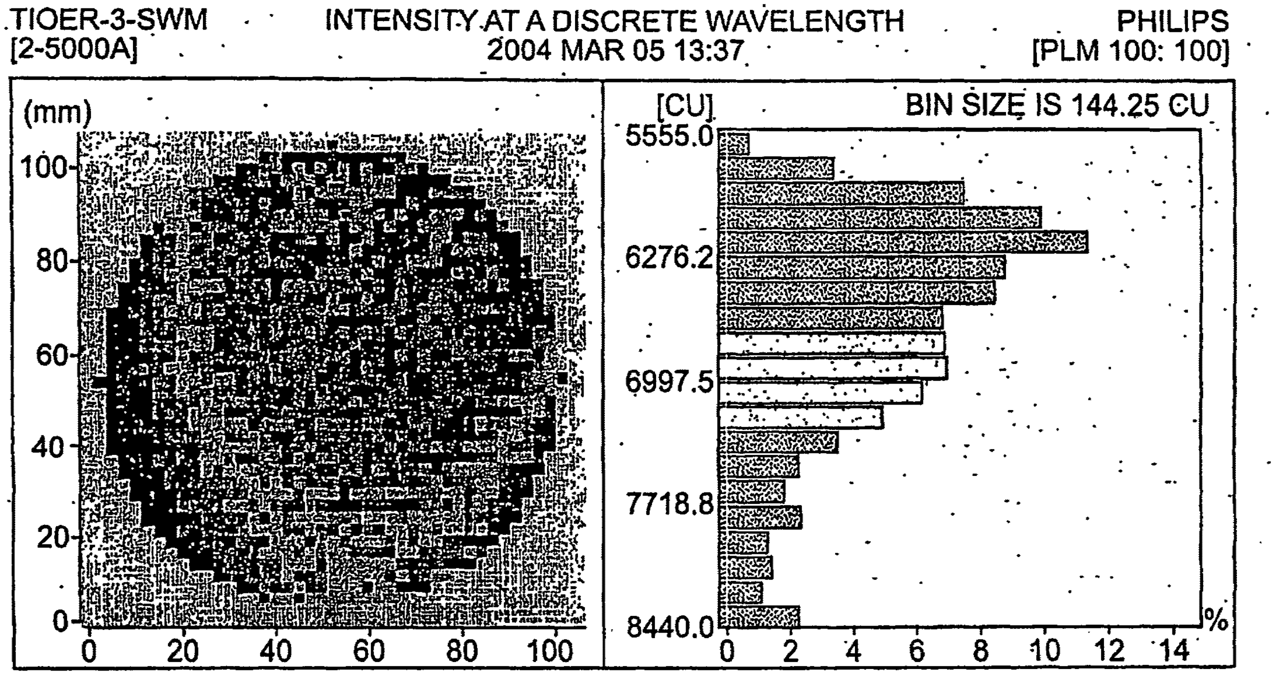

1.0E-04
1.0E-05
1.0E-06
1.0E-07
1.0E-08
1.0E-09
1.0E-10
AMP/cm^2
0
10
20
30
40
V
PURE
TiO2 CAP
ER DOPED
TiO2 CAP

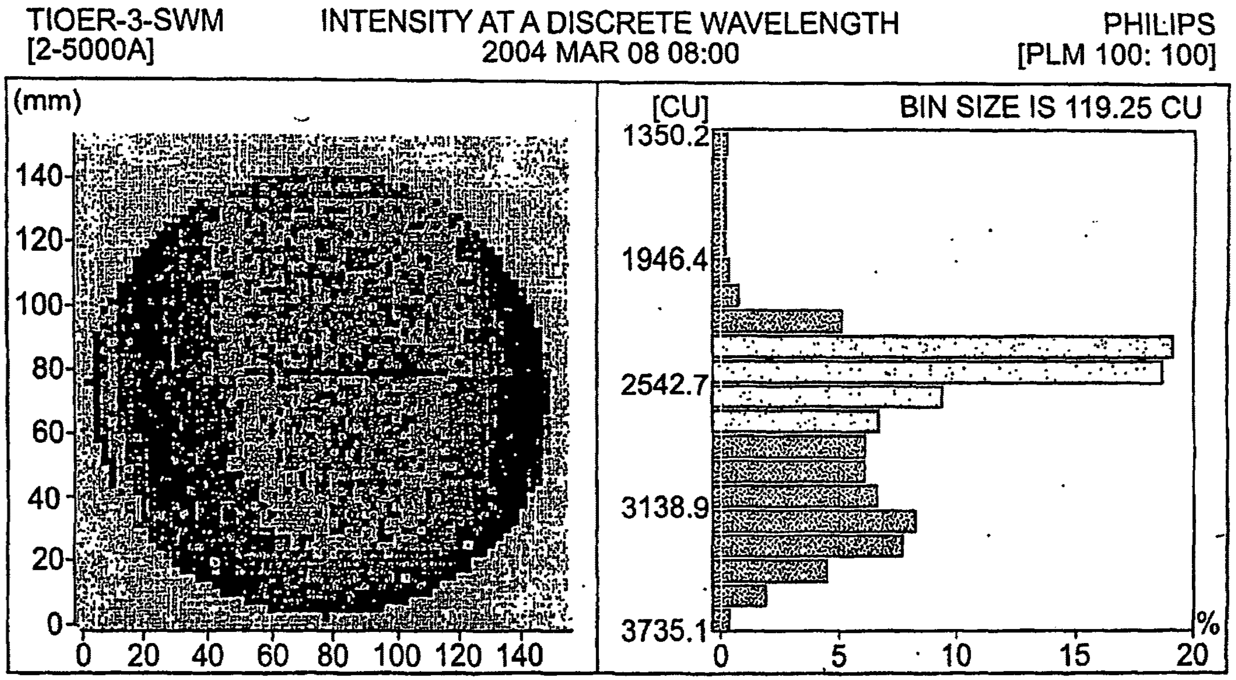
FIG. 13



INTENSITY - AVERAGE (O) : 6669.1 (643.7) CU
- UNIFORMITY : 9.7%
- MEDIAN : 6541.5 CU
- 10% : 5946.4 CU
- 90% : 7607.3 CU
SAMPLE WAVELENGTH : 1530.0 nm

INTENSITY -UNDER ▨ 32.0%
-OVER ☐ 0.0 %

FIG. 14A



INTENSITY - AVERAGE (O) : 2736.0 (382.3) CU
- UNIFORMITY : 14.0 %
- MEDIAN : 2615.1 CU
- 10% : 2330.0 CU
- 90% : 3307.5CU
SAMPLE WAVELENGTH : 1530.0 nm

INTENSITY -UNDER ☐ 34.9%
-OVER ☐ 0.0 %

FIG. 14B

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H01M 4/52 (2006.01) *C23C 14/34* (2006.01)

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(71) Applicant *(for all designated States except US)*: **SYMMORPHIX, INC.** [US/US]; 1278 Reamwood Avenue, Sunnyvale, CA 94089-2233 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **ZHANG, Hongmei** [US/US]; 1330 Rodney Drive, San Jose, CA 95118 (US). **DEMARAY, Richard, E.** [US/US]; 190 Fawn Lane, Portola Valley, CA 94028 (US). **SHAO, May** [US/US]; 5401 Nectar Circle, Elk Grove, CA 95757 (US).

(74) Agent: EDWARDS, Gary, J.; Finnegan, Henderson, Farabow, Garrett & Dunner LLP, 901 New York Avenue, Washington, D.C.,, District of Columbia 20001-4413 (US).

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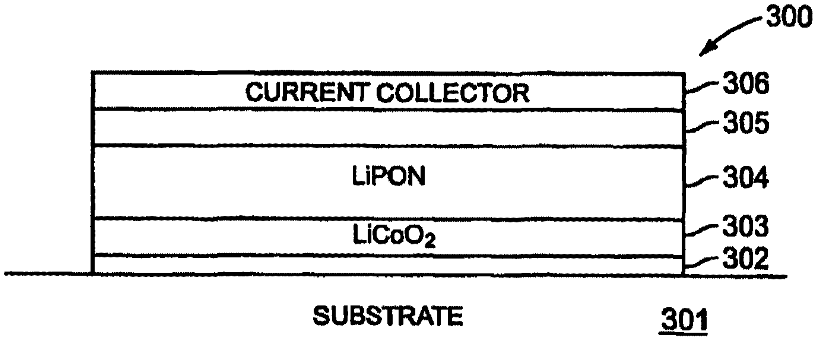
(54) Title: DEPOSITION OF LICoO2



(57) Abstract: In accordance with the present invention, deposition of $LiCoO_2$ layers in a pulsed-dc physical vapor deposition process is presented. Such a deposition can provide a low-temperature, high deposition rate deposition of a crystalline layer of $LiCoO_2$ with a desired <101> or <003> orientation. Some embodiments of the deposition addresses the need for high rate deposition of $LiCoO_2$ films, which can be utilized as the cathode layer in a solid state rechargeable Li battery. Embodiments of the process according to the present invention can eliminate the high temperature (>700°C) anneal step that is conventionally needed to crystallize the $LiCoO_2$ layer. Some embodiments of the process can improve a battery utilizing the $LiCoO_2$ layer by utilizing a rapid thermal anneal process with short ramp rates.

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DEPOSITION OF LICoO$_2$

RELATED APPLICATION

[001] The present application claims priority to Provisional Application No. 60/651,363, filed on February 8, 2005, by Hongmei Zhang and Richard E. Demaray, and to Provisional Application No. 60/634,818, filed on December 8, 2004, by the same inventors, each of which are herein incorporated by reference in their entirety.

BACKGROUND

1. Field of the Invention

[002] The present invention is related to thin-film solid-state batteries and, in particular, the deposition of LiCoO$_2$ films and layers for battery manufacture.

2. Discussion of Related Art

[003] Solid-state thin-film batteries are typically formed by stacking thin films on a substrate in such a way that the films cooperate to generate a voltage. The thin films typically include current collectors, a cathode, an anode, and an electrolyte. The thin films can be deposited utilizing a number of deposition processes, including sputtering and electroplating. Substrates suitable for this application have conventionally been high temperature materials capable of withstanding at least one high temperature anneal process to at least 700 °C for up to about 2 hours in air so as to crystallize the LiCoO$_2$ film. Such a substrate can be any suitable material with appropriate structural and material properties, for example a semiconductor wafer, metallic sheet (e.g., titanium or zirconium), ceramic such as alumina, or other material capable of withstanding subsequent high temperature processing in

the presence of the $LiCoO_2$, which can experience significant interfacial reactions with most materials utilized in a battery during these temperature cycles.

[004] Other lithium containing mixed metal oxides besides $LiCoO_2$, including Ni, Nb, Mn, V, and sometimes also Co, but including other transition metal oxides, have been evaluated as crystalline energy storage cathode materials. Typically, the cathode material is deposited in amorphous form and then the material is heated in an anneal process to form the crystalline material. In $LiCoO_2$, for example, an anneal at or above 700°C transforms the deposited amorphous film to a crystalline form. Such a high temperature anneal, however, severely limits the materials that can be utilized as the substrate, induces destructive reaction with the lithium containing cathode material and often requires the use of expensive noble metals such as gold. Such high thermal budget processes (i.e., high temperatures for extended periods of time) are incompatible with semiconductor or MEM device processing and limit the choice of substrate materials, increase the cost, and decrease the yield of such batteries. The inventors are unaware of a process disclosed in the art that allows production of cathodic lithium films for a battery structure where a post-deposition anneal process has a low enough thermal budget to allow production of functional structures on low temperature materials such as stainless steel, aluminum, or copper foil.

[005] It is known that crystallization of amorphous $LiCoO_2$ on precious metals can be achieved. An example of this crystallization is discussed in Kim et al., where a conventional furnace anneal at 700°C for 20 minutes of an amorphous layer of $LiCoO_2$ on a precious metal achieves crystallization of the $LiCoO_2$ material, as shown by x-ray diffraction data. Kim, Han-Ki and Yoon, Young Soo, "Characteristics of rapid-thermal-annealed $LiCoO_2$, cathode film for an all-solid-state thin film microbattery," J. Vac. Sci. Techn. A 22(4), Jul/Aug 2004. In Kim et al., the $LiCoO_2$ film was deposited on a platinum film that was deposited on a high-temperature MgO/Si substrate. In Kim et al, it was shown that such

a crystalline film is capable of constituting the Li+ ion containing cathode layer of a functional all solid-state Li+ ion battery. However, it is of continuing interest for the manufacture of solid state Li+ ion batteries to further reduce the thermal budget of the post deposition anneal, both in time and in temperature, so as to enable the manufacture of such batteries without the need for expensive precious metal nucleation, barrier layers, or expensive high-temperature substrates.

[006] There are many references that disclose an ion beam assisted process that can provide a $LiCoO_2$ film that demonstrates some observable crystalline composition by low angle x-ray diffraction (XRD). Some examples of these are found in U.S. Patent Applications 09/815,983 (Publication No. US 2002/001747), 09/815,621 (Publication No. US 2001/0032666), and 09/815,919 (Publication No. US 2002/0001746). These references disclose the use of a second front side ion beam or other ion source side-by-side with a deposition source so as to obtain a region of overlap of the flux of ions with the flux of $LiCoO_2$ vapor at the substrate surface. None of these references disclose film temperature data or other temperature data of the film during deposition to support an assertion of low temperature processing.

[007] It is very difficult to form a uniform deposition either by sputtering a material layer or by bombardment with an ion flux. Utilization of two uniform simultaneous distributions from two sources that do not occupy the same position and extent with respect to the substrate enormously increases the difficulties involved in achieving a uniform material deposition. These references do not disclose a uniform materials deposition, which is required for reliable production of thin-film batteries. A well understood specification for material uniformity for useful battery products is that a 5% one-sigma material uniformity is standard in thin film manufacturing. About 86% of the films with this uniformity will be found acceptable for battery production.

[008] It is even more difficult to scale a substrate to manufacturing scale, such as 200 mm or 300 mm. Indeed, in the references discussed above that utilize both a sputtering deposition and an ion beam deposition, only small area targets and small area substrates are disclosed. These references disclose a single feasibility result. No method for achieving a uniform distribution from two separate front side sources has been disclosed in these references.

[009] Further, conventional materials and production processes can limit the energy density capacity of the batteries produced, causing a need for more batteries occupying more volume. It is specifically desirable to produce batteries that have large amounts of stored energy per unit volume in order to provide batteries of low weight and low volume.

[010] Therefore, there is a need for a low temperature process for depositing crystalline material, for example $LiCoO_2$ material, onto a substrate.

SUMMARY

[011] In accordance with the present invention, deposition of $LiCoO_2$ layers in a pulsed-dc physical vapor deposition process is presented. Such a deposition can provide a low-temperature, high deposition rate deposition of a crystalline layer of $LiCoO_2$ with a desired <101> orientation. Some embodiments of the deposition address the need for high rate deposition of $LiCoO_2$ films, which can be utilized as the cathode layer in a solid state rechargeable Li battery. Embodiments of the process according to the present invention can eliminate the high temperature (>700 °C) anneal step that is conventionally needed to crystallize the $LiCoO_2$ layer.

[012] A method of depositing a $LiCoO_2$ layer according to some embodiments of the present invention includes placing a substrate in a reactor; flowing a gaseous mixture including argon and oxygen through the reactor; and applying pulsed-DC power to a target

formed of $LiCoO_2$ positioned opposite the substrate. In some embodiments, a $LiCoO_2$ layer is formed on the substrate. Further, in some embodiments the $LiCoO_2$ layer is a crystalline layer of orientation <101>.

[013] In some embodiments, a stacked battery structure can be formed. The stacked battery structure includes one or more battery stacks deposited on a thin substrate, wherein each battery stack includes: a conducting layer, a crystalline $LiCoO_2$ layer deposited over the conducting layer, a LiPON layer deposited over the $LiCoO_2$ layer; and an anode deposited over the LiPON layer. A top conducting layer can be deposited over the one or more battery stacks.

[014] In some embodiments, a battery structure can be formed in a cluster tool. A method of producing a battery in a cluster tool includes loading a substrate into a cluster tool; depositing a conducting layer over the substrate in a first chamber of the cluster tool; depositing a crystalline $LiCoO_2$ layer over the conducting layer in a second chamber of the cluster tool; depositing a LiPON layer over the $LiCoO_2$ layer in a third chamber of the cluster tool; depositing an anode layer over the $LiCoO_2$ layer in a fourth chamber; and depositing a second conducting layer over the LiPON layer in a fifth chamber of the cluster tool.

[015] A fixture for holding a thin substrate can include a top portion and a bottom portion, wherein the thin substrate is held when the top portion is attached to the bottom portion.

[016] These and other embodiments of the invention are further discussed below with reference to the following figures. It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention, as claimed. Further, specific explanations or theories regarding the deposition or performance of certain layers during deposition processes or in the performance of devices incorporating those layers are presented for explanation only and

are not to be considered limiting with respect to the scope of the present disclosure or the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[017] Figures 1A and 1B illustrate a pulsed-DC biased reactive deposition apparatus that can be utilized in the methods of depositing according to the present invention.

[018] Figure 2 shows an example of a target that can be utilized in the reactor illustrated in Figures 1A and 1B.

[019] Figure 3 illustrates a thin-film battery design according to some embodiments of the present invention.

[020] Figures 4A and 4B show an x-ray diffraction analysis of and an SEM photograph of a $LiCoO_2$ film deposited according to embodiments of the present invention.

[021] Figures 5A through 5F show SEM photographs of $LiCoO_2$ films according to some embodiments of the present invention.

[022] Figure 5G shows x-ray diffraction data corresponding to the depositions shown in Figures 5B-5F.

[023] Figure 6A illustrates a layer of $LiCoO_2$ deposited according to some embodiments of the present invention on a thin substrate.

[024] Figure 6B illustrates a layer of $LiCoO_2$ deposited according to some embodiments of the present invention over a conducting layer on a thin substrate.

[025] Figures 7A, 7B, 7C, and 7D illustrate a thin substrate mount and mask arrangement that can be utilized in the deposition of $LiCoO_2$ layers deposited according to some embodiments of the present invention.

[026] Figure 8 illustrates a cluster tool that can be utilized to form batteries with $LiCoO_2$ layers deposited according to some embodiments of the present invention.

[027] Figures 9A and 9B illustrate examples of stacked batter structures with $LiCoO_2$ layers deposited according to some embodiments of the present invention.

[028] Figures 10A through 10D illustrate deposition and anneal steps for $LiCoO_2$ deposited over an iridium layer on a silicon wafer.

[029] Figures 11A through 11D illustrate a single layer battery formed over an iridium layer according to some embodiments of the present invention.

[030] Figures 12A through 12L illustrate deposition of a crystalline LiCoO2 layer on a silicon or alumina substrate.

[031] Figures 13A through 13F illustrate rapid thermal anneal processes for $LiCoO_2$ layers deposited according to the present invention.

[032] Figures 14A through 14D illustrate several anneal processes utilized with a $LiCoO_2$ film deposited according to embodiments of the present invention.

[033] Figures 15A and 15B illustrate the effects of ramp-time in a rapid thermal anneal of $LiCoO_2$ films deposited according to the present invention.

[034] Figure 16 illustrates thickness uniformity of a LiCoO2 film deposited according to some embodiments of the present invention.

[035] Figure 17 illustrates battery charge and discharge profiles of a battery formed utilizing a $LiCoO_2$ film according to some embodiments of the present invention.

[036] In the figures, elements having the same designation have the same or similar functions.

DETAILED DESCRIPTION

[037] In accordance with embodiments of the present invention, $LiCoO_2$ films are deposited on a substrate by a pulsed-dc physical vapor deposition (PVD) process. In contrast to, for example, Kim et al., $LiCoO_2$ films according to some embodiments of the present

invention provide a crystalline $LiCoO_2$ film as deposited on a substrate at a substrate temperature as low as about 220 °C during deposition, without the use of a metallic nucleation or barrier underlying film. The as-deposited crystalline $LiCoO_2$ films can be easily ripened to very high crystalline condition by anneal at about 700 °C for as little as 5 minutes without the use of an underlying precious metal film. In addition, the as deposited crystalline films, when positioned on a noble metal film can be annealed at much further reduced temperatures, for example as low as 400 to 500 °C, providing for deposition, annealing, and production of solid state batteries on lower temperature substrates.

[038] In the present application, a single, extended source is described which has been scaled to 400mm X 500mm for production achieving a $LiCoO_2$ uniformity of 3% one-sigma measured at 25 points at a deposition rate of 1.2 microns thickness an hour over an area of 2000 cm^2, without the need for secondary front side ion source or ion assistance.

[039] In one example process, a $LiCoO_2$ film was deposited utilizing a conductive ceramic $LiCoO_2$ target as described herein, with pulsed-dc power of 4 kW, no bias, with 60 sccm Ar and 20 sccm O_2 gas flows. A 3000 Angstrom layer of crystalline $LiCoO_2$ was deposited on a substrate area of 400 X 500 mm. As demonstrated in Figure 16, film thickness uniformity was located at about 25 locations spaced uniformly across the substrate using a felt marker pen to lift off a portion of the film in each location. High precision white-light interferometry was utilized to measure the film thickness in each location by measuring the step height from the substrate to film surface. All 25 thickness measurements demonstrated a 3% one-sigma uniformity in the film thickness over 400 X 500 mm substrate area. As shown in Figure 16, a film was deposited with average thickness of about 2.96 μm with a maximum of 3.09 μm and a minimum of 2.70 μm and standard deviation of 0.093. Thickness data was taken at points spaced 0.65 mm apart on the surface of the film. The film thickness therefore showed 3% one-sigma uniformity over the shown surface area.

[040] On other depositions utilizing this process, a temperature measurement of the substrate during deposition showed that the substrate remained at less than 224 °C. Temperature measurements were performed utilizing a temperature sticker purchased from Omega Engineering, Stamford, Ct (Model no. TL-F-390, active from 199-224 °C).

[041] Moreover, in some embodiments, films deposited according to the present invention can have a deposition rate of from about 10 to about 30 times higher than processes in conventional films. Deposition thicknesses and times of deposition for films deposited according to the present invention are illustrated in Table I. Furthermore, films according to the present invention can be deposited on wide area substrates having a surface area from 10 to 50 times the surface area of prior sputtering processes, resulting in much higher productivity and much lower cost of manufacture, thereby providing high-volume, low-cost batteries.

[042] Further, conventional deposition processes without ion sources are capable of depositing amorphous $LiCoO_2$ layers, but do not deposit crystalline $LiCoO_2$ layers. Surprisingly, depositions according to some embodiment of the present invention, deposit a $LiCoO_2$ layer with substantial crystallinity readily measured by x-ray diffraction techniques. In some embodiments, the crystallinity of the as-deposited $LiCoO_2$ layers is sufficient to be utilized in a battery structure with no further thermal processing. In some embodiments, crystallinity of the as-deposited $LiCoO_2$ layers are improved by thermal processes with low thermal budgets, which can be compatible with films deposited on low-temperature substrates.

[043] Further, as-deposited the stoichiometry of some $LiCoO_2$ layers deposited according to some embodiments of the present invention shows that this layer is sufficient for utilization in a battery. With the demonstrated ability to deposit a $LiCoO_2$ film with crystallinity and with sufficient stoichiometry, a battery utilizing as-deposited $LiCoO_2$ films

can be produced. Heat treating the $LiCoO_2$ layers may improve the crystallinity and lower the impedance.

[044] In some embodiments, a crystalline layer of $LiCoO_2$ with a <101> or a <003> crystalline orientation is deposited directly on the substrate. Deposition of crystalline material can eliminate or lessen the need of a subsequent high temperature anneal or precious-metal layers to crystallize and orient the film. Removing the high temperature anneal allows for formation of battery structures on light-weight and low temperature substrates such as stainless steel foil, copper foil, aluminum foil, and plastic sheet, reducing both the weight and the cost of batteries while retaining the energy density storage capabilities of Li-based batteries. In some embodiments, a crystalline $LiCoO_2$ layer can be deposited on a precious metal layer, such as platinum or iridium, resulting in a further significant lowering of the ripening thermal budget required to improve crystallinity.

[045] Deposition of materials by pulsed-DC biased reactive ion deposition is described in U.S. Patent Application Serial No. 10/101863, entitled "Biased Pulse DC Reactive Sputtering of Oxide Films," to Hongmei Zhang, et al., filed on March 16, 2002. Preparation of targets is described in U.S. Patent Application Serial No. 10/101,341, entitled "Rare-Earth Pre-Alloyed PVD Targets for Dielectric Planar Applications," to Vassiliki Milonopoulou, et al., filed on March 16, 2002. U.S. Patent Application Serial No. 10/101863 and U.S. Patent Application Serial No. 10/101,341 are each assigned to the same assignee as is the present disclosure and each is incorporated herein in their entirety. Deposition of oxide materials has also been described in U.S. Patent No. 6,506,289, which is also herein incorporated by reference in its entirety. Transparent oxide films can be deposited utilizing processes similar to those specifically described in U.S. Patent No. 6,506,289 and U.S. Application Serial No. 10/101863.

[046] Figure 1A shows a schematic of a reactor apparatus 10 for sputtering material from a target 12 according to the present invention. In some embodiments, apparatus 10 may, for example, be adapted from an AKT-1600 PVD (400 X 500 mm substrate size) system from Applied Komatsu or an AKT-4300 (600 X 720 mm substrate size) system from Applied Komatsu, Santa Clara, CA. The AKT-1600 reactor, for example, has three deposition chambers connected by a vacuum transport chamber. These AKT reactors can be modified such that pulsed DC power is supplied to the target and RF power is supplied to the substrate during deposition of a material film. Apparatus 10 can also be a Phoenix Gen III PVD cluster tool made by Symmorphix, which is specifically designed for pulsed-dc processes such as is described herein.

[047] Apparatus 10 includes target 12 which is electrically coupled through a filter 15 to a pulsed DC power supply 14. In some embodiments, target 12 is a wide area sputter source target, which provides material to be deposited on a substrate 16. Substrate 16 is positioned parallel to and opposite target 12. Target 12 functions as a cathode when power is applied to it from the pulsed DC power supply 14 and is equivalently termed a cathode. Application of power to target 12 creates a plasma 53. Substrate 16 is capacitively coupled to an electrode 17 through an insulator 54. Electrode 17 can be coupled to an RF power supply 18. A magnet 20 is scanned across the top of target 12.

[048] For pulsed reactive dc magnetron sputtering, as performed by apparatus 10, the polarity of the power supplied to target 12 by power supply 14 oscillates between negative and positive potentials. During the positive period, the insulating layer on the surface of target 12 is discharged and arcing is prevented. To obtain arc free deposition, the pulsing frequency exceeds a critical frequency that can depend on target material, cathode current and reverse time. High quality oxide films can be made using reactive pulse DC magnetron sputtering as shown in apparatus 10.

[049] Pulsed DC power supply 14 can be any pulsed DC power supply, for example an AE Pinnacle plus 10K by Advanced Energy, Inc. With this DC power supply, up to 10 kW of pulsed DC power can be supplied at a frequency of between 0 and 350 kHz. The reverse voltage can be 10% of the negative target voltage. Utilization of other power supplies can lead to different power characteristics, frequency characteristics, and reverse voltage percentages. The reverse time on this embodiment of power supply 14 can be adjusted between 0 and 5 μs.

[050] Filter 15 prevents the bias power from power supply 18 from coupling into pulsed DC power supply 14. In some embodiments, power supply 18 can be a 2 MHz RF power supply, for example a Nova-25 power supply made by ENI, Colorado Springs, Co.

[051] In some embodiments, filter 15 can be a 2 MHz sinusoidal band rejection filter. In some embodiments, the band width of the filter can be approximately 100 kHz. Filter 15, therefore, prevents the 2 MHz power from the bias to substrate 16 from damaging power supply 14 and allow passage of the pulsed-dc power and frequency.

[052] Pulsed DC deposited films are not fully dense and may have columnar structures. Columnar structures can be detrimental to thin film applications such as barrier films and dielectric films, where high density is important, due to the boundaries between the columns. The columns act to lower the dielectric strength of the material, but may provide diffusion paths for transport or diffusion of electrical current, ionic current, gas, or other chemical agents such as water. In the case of a solid state battery, a columnar structure containing crystallinity as derived from processes according to the present invention is beneficial for battery performance because it allows better Li transport through the boundaries of the material.

[053] In the Phoenix system, for example, target 12 can have an active size of about 800.00 X 920.00 mm by 4 to 8 mm in order to deposit films on substrate 16 that have

dimension about 600 X 720 mm. The temperature of substrate 16 can be adjusted to between –50 °C and 500 °C. The distance between target 12 and substrate 16 can be between about 3 and about 9 cm (in some embodiments, between 4.8 and 6 cm are used). Process gas can be inserted into the chamber of apparatus 10 at a rate up to about 200 sccm while the pressure in the chamber of apparatus 10 can be held at between about .7 and 6 milliTorr. Magnet 20 provides a magnetic field of strength between about 400 and about 600 Gauss directed in the plane of target 12 and is moved across target 12 at a rate of less than about 20-30 sec/scan. In some embodiments utilizing the Phoenix reactor, magnet 20 can be a race-track shaped magnet with dimensions about 150 mm by 800 mm.

[054] Figure 2 illustrates an example of target 12. A film deposited on a substrate positioned on carrier sheet 17 directly opposed to region 52 of target 12 has good thickness uniformity. Region 52 is the region shown in Figure 1B that is exposed to a uniform plasma condition. In some implementations, carrier 17 can be coextensive with region 52. Region 24 shown in Figure 2 indicates the area below which both physically and chemically uniform deposition can be achieved, for example where physical and chemical uniformity provide refractive index uniformity, oxide film uniformity, or metallic film uniformity. Figure 2 indicates region 52 of target 12 that provides thickness uniformity, which is, in general, larger than region 24 of target 12 providing thickness and chemical uniformity to the deposited film. In optimized processes, however, regions 52 and 24 may be coextensive.

[055] In some embodiments, magnet 20 extends beyond area 52 in one direction, for example the Y direction in Figure 2, so that scanning is necessary in only one direction, for example the X direction, to provide a time averaged uniform magnetic field. As shown in Figures 1A and 1B, magnet 20 can be scanned over the entire extent of target 12, which is larger than region 52 of uniform sputter erosion. Magnet 20 is moved in a plane parallel to the plane of target 12.

[056] The combination of a uniform target 12 with a target area 52 larger than the area of substrate 16 can provide films of highly uniform thickness. Further, the material properties of the film deposited can be highly uniform. The conditions of sputtering at the target surface, such as the uniformity of erosion, the average temperature of the plasma at the target surface, and the equilibration of the target surface with the gas phase ambient of the process are uniform over a region which is greater than or equal to the region to be coated with a uniform film thickness. In addition, the region of uniform film thickness is greater than or equal to the region of the film which is to have highly uniform electrical, mechanical, or optical properties such as index of refraction, stoichiometry, density, transmission, or absorptivity.

[057] Target 12 can be formed of any materials that provide the correct stoichiometry for $LiCoO_2$ deposition. Typical ceramic target materials include oxides of Li and Co as well as metallic Li and Co additions and dopants such as Ni, Si, Nb, or other suitable metal oxide additions. In the present disclosure, target 12 can be formed from $LiCoO_2$ for deposition of $LiCoO_2$ film.

[058] In some embodiments of the invention, material tiles are formed. These tiles can be mounted on a backing plate to form a target for apparatus 10. A wide area sputter cathode target can be formed from a close packed array of smaller tiles. Target 12, therefore, may include any number of tiles, for example between 2 and 60 individual tiles. Tiles can be finished to a size so as to provide a margin of edge-wise non-contact, tile to tile, less than about 0.010" to about 0.020" or less than half a millimeter so as to eliminate plasma processes that may occur between adjacent ones of tiles 30. The distance between tiles of target 12 and the dark space anode or ground shield 19 in Figure 1B can be somewhat larger so as to provide non contact assembly or to provide for thermal expansion tolerance during process chamber conditioning or operation.

[059] As shown in Figure 1B, a uniform plasma condition can be created in the region between target 12 and substrate 16 in a region overlying substrate 16. A plasma 53 can be created in region 51, which extends under the entire target 12. A central region 52 of target 12 can experience a condition of uniform sputter erosion. As discussed further herein, a layer deposited on a substrate placed anywhere below central region 52 can then be uniform in thickness and other properties (i.e., dielectric, optical index, or material concentrations). In some embodiments, target 12 is substantially planar in order to provide uniformity in the film deposited on substrate 16. In practice, planarity of target 12 can mean that all portions of the target surface in region 52 are within a few millimeters of a planar surface, and can be typically within 0.5 mm of a planar surface.

[060] Figure 3 shows a battery structure with a $LiCoO_2$ layer deposited according to some embodiments of the present invention. As shown in Figure 3, a metallic current collection layer 302 is deposited on a substrate 301. In some embodiments, current collection layer 302 can be patterned in various ways before deposition of a $LiCoO_2$ layer 303. Also according to some embodiments, $LiCoO_2$ layer 303 can be a deposited crystalline layer. In some embodiments of the invention, layer 303 is crystalline without the necessity of a crystallizing heat treatment. Therefore, substrate 301 can be a silicon wafer, titanium metal, alumina, or other conventional high temperature substrate, but may also be a low temperature material such as plastic, glass, or other material which could be susceptible to damage from the high temperature crystallizing heat treatment. This feature can have the great advantage of decreasing the expense and weight of battery structures formed by the present invention. The low temperature deposition of the $LiCoO_2$ allows for successive depositions of battery layers, one upon another. Such a process would have the advantage that successive layers of battery structure would be obtained in a stacked condition without the inclusion of a substrate

layer. The stacked layered battery would provide higher specific energy density as well as low impedance operation for charging and discharging.

[061] In some embodiments, an oxide layer can be deposited on substrate 301. For example, a silicon oxide layer can be deposited on a silicon wafer. Other layers can be formed between conducting layer 302 and substrate 301.

[062] As further shown in Figure 3, a LiPON layer 304 ($Li_xPO_yN_z$) is deposited over $LiCoO_2$ layer 303. LiPON layer 304 is the electrolyte for battery 300 while $LiCoO_2$ layer 303 acts as the cathode. A metallic conducting layer 305 can be deposited over the LiPON layer 304 in order to complete the battery. Metallic conducting layer 305 can include lithium adjacent to LiPON layer 304.

[063] An anode 305 is deposited over LiPON layer 304. Anode 305 can be, for example an evaporated lithium metal. Other materials such as, for example, nickel can also be utilized. A current collector 306, which is a conducting material, is then deposited over at least a portion of anode 305.

[064] A Li based thin film battery operates by transport of Li ions in the direction from current collector 306 to current collector 302 in order to hold the voltage between current collector 306 and current collector 302 at a constant voltage. The ability for battery structure 300 to supply steady current, then, depends on the ability of Li ions to diffuse through LiPON layer 304 and $LiCoO_2$ layer 303. Li transport through bulk cathode $LiCoO_2$ layer 303 in a thin film battery occurs by the way of grains or grain boundaries. Without being restricted in this disclosure to any particular theory of transport, it is believed that the grains with their planes parallel to substrate 302 will block the flow of Li ions while grains oriented with planes perpendicular to substrate 301 (i.e., oriented parallel to the direction of Li ion flow) facilitate the Li diffusion. Therefore, in order to provide a high-current battery

structure, $LiCoO_2$ layer 303 should include crystals oriented in the <101> direction or <003> direction.

[065] In accordance with the present invention, $LiCoO_2$ films can be deposited on substrate 302 with a pulsed-DC biased PVD system as was described above. In addition, an AKT 1600 PVD system can be modified to provide an RF bias, which is available in the Phoenix system, and an Advanced Energy Pinnacle plus 10K pulsed DC power supply can be utilized to provide power to a target. The pulsing frequency of the power supply can vary from about 0 to about 350 KHz. The power output of the power supply is between 0 and about 10 kW. A target of densified $LiCoO_2$ tiles having a resistivity in the range of about 3 to about 10 kΩ can be utilized with dc-sputtering.

[066] In some embodiments, $LiCoO_2$ films are deposited on Si wafers. Gas flows containing Oxygen and Argon can be utilized. In some embodiments, the Oxygen to Argon ratio ranges from 0 to about 50% with a total gas flow of about 80 sccm. The pulsing frequency ranges from about 200 kHz to about 300 kHz during deposition. RF bias can also be applied to the substrate. In many trials, the deposition rates vary from about 2 Angstrom/(kW sec) to about 1 Angstrom/(kW sec) depending on the O_2/Ar ratio as well as substrate bias.

[067] Table I illustrates some example depositions of $LiCoO_2$ according to the present invention. XRD (x-Ray Diffraction) results taken on the resulting thin films illustrate that films deposited according to the present invention are crystalline films, often with highly textured grain sizes as large as about 150 nm. The dominant crystal orientation appears to be sensitive to the O_2/Ar ratio. For certain O_2/Ar ratios (~10%), as-deposited films exhibit a preferred orientation in the <101> direction or the <003> direction with poorly developed <003> planes.

[068] Figures 4A and 4B illustrate an XRD Analysis and SEM cross section, respectively, of the $LiCoO_2$ film deposited as Example 15 in Table I. Such a $LiCoO_2$ film was deposited on Si wafer with 2kW of target power, a frequency of 300 kHz, with 60 sccm Ar and 20 sccm of O_2 for a substrate with an initial temperature of about 30°C. As shown in the XRD analysis of Figure 4A, a strong <101> peak is indicated showing a strong orientation of $LiCoO_2$ crystals in the desired <101> crystallographic direction. The SEM cross section shown in Figure 4B further shows the columnar structure of the film having the <101> direction and the grain boundaries of the resulting $LiCoO_2$ crystals.

[069] Figures 5A through 5F show SEM cross sections of further example depositions of $LiCoO_2$ crystals according to the present invention. In each of the examples, deposition of the $LiCoO_2$ film was performed on a Si wafer with target power of about 2 kW and frequency of about 250 kHz. The $LiCoO_2$ film shown in Figure 5A corresponds to the example deposition Example 1 in Table I. In the deposition of the $LiCoO_2$ film shown in Figure 5A, no bias power was utilized with an argon flow rate of about 80 sccm and an oxygen flow rate of about 0 sccm. A deposition rate of about 1.45 μm/hr was achieved over the full substrate area of 400 X 500 mm. Further, as is indicated in the cross section shown in Figure 5A, a <101> orientation of the $LiCoO_2$ was achieved.

[070] The rate of deposition of the $LiCoO_2$ layer shown in Figure 5A is very high, likely due to the relatively high conductivity or low resistivity of the ceramic $LiCoO_2$ oxide sputter target. A target resistance of 10 kOhms was measured by means of an Ohm meter over a distance of about 4 cm on the surface of target 12. This high rate allows the manufacture of the 3 micron or thicker $LiCoO_2$ layer required for the battery at high rate over a wide area in short times, resulting in very high productivity and very low cost. Target resistance on the order of about 500 kΩ over the same distance by the same measurement technique or higher would not allow for such a high sputter efficiency or high rate of

deposition at such a low target power. The resistance of conventional target materials can be unmeasurably high. A resistance of 100 kΩ over about 4 cm of surface will result in high sputter efficiency and high rate of deposition. Further, because deposition rates typically scale nearly linearly with target power, a deposition at 6 kW will yield a deposition rate of approximately 3 μm/hr, which is a very desirable rate of deposition for manufacturability of Li-based thin-film solid-state batteries on a surface area of 400 X 500 mm^2.

[071] The $LiCoO_2$ layer shown in Figure 5B is deposited under the conditions listed as Example 7 in Table I. Again, no bias was utilized in the deposition. An argon flow rate of about 72 sccm and an oxygen flow rate of about 8 sccm was utilized. The deposition rate was significantly reduced to about 0.85 μm/hr. Further, although a <101> crystallinity can be discerned, that <101> crystallinity is not as pronounced as that exhibited in the deposition of the film shown in Figure 5A.

[072] The $LiCoO_2$ film shown in Figure 5C was deposited according to Example 3 in Table I. In this deposition, 100 W of bias power is applied to the substrate. Further, an argon flow rate of 72 sccm, and an oxygen flow rate of 8 sccm was utilized. The deposition rate was about 0.67 μm/hr. Therefore, the application of bias in comparison with the $LiCoO_2$ film shown in Figure 5B further reduced the deposition rate (from 0.85 μm/hr of the example shown in Figure 5B to 0.67 μm/hr of the example shown in Figure 5C). Further, the desired <101> directionality of formed crystals appears to be further degraded.

[073] The $LiCoO_2$ film shown in Figure 5D corresponds to Example 4 in Table I. In this deposition, the Ar/O_2 ratio was increased. As is shown in Figure 5D, increasing the Ar/O_2 ratio improves crystallinity. With respect to the example illustrated in Figure 5C, the deposition illustrated in Figure 5D was performed with an argon flow of about 76 sccm and an oxygen flow of about 4 sccm as well as retaining the 100 W bias to the substrate. The

$LiCoO_2$ deposition rate was improved to 0.79 μm/hr from a rate of 0.67 μm/hr illustrated in Figure 5C.

[074] In the example deposition illustrated in Figure 5E corresponding to Example 5 in Table I. The substrate temperature was set at about 200°C while the bias power remained at about 100 W. The argon flow rate was set at about 76 sccm and the oxygen flow rate was set at about 4 sccm. The resulting deposition rate for the $LiCoO_2$ layer was about 0.74 μm/hr.

[075] In the example deposition illustrated in Figure 5F, which corresponds with Example 6 of Table I, the argon flow rate was set at about 74 sccm and the oxygen flow rate was set at about 6 sccm, resulting in a $LiCoO_2$ deposition rate of about 0.67 μm/hr. Therefore, increasing both argon and oxygen flow rate over the deposition illustrated in Figure 5E resulted in a lower deposition rate.

[076] Figure 5G illustrates XRD data corresponding to Figures 5F, 5D, 5C, 5E, and 5B, respectively. As illustrated in Figure 5G, as-deposited crystalline $LiCoO_2$ is deposited in these processes.

[077] The data show clearly that an as-deposited crystalline film of $LiCoO_2$ can be obtained under several of the process conditions, as shown in Table II. In particular, very high rates of deposition with low power are obtained along with the oriented crystalline structure for the process conditions according to embodiments of the present invention.

[078] Figure 6A illustrates a layer of $LiCoO_2$ 602 deposited on a thin substrate 601 according to some embodiments of the present invention. Higher lithium-ion mobilities can be achieved utilizing crystalline $LiCoO_2$ cathode films 602 deposited on a thin substrate 601 that has thickness comparable to that of the battery stack itself, rather than a thickness many or tens of times that of the battery stack. Such a film can lead to faster charging and discharging rates. Substrate 601 can be formed of a thin metallic sheet (e.g., aluminum,

titanium, stainless steel, or other suitable thin metallic sheet), can be formed of a polymer or plastic material, or may be formed of a ceramic or glass material. As shown in Figure 6B, if substrate 601 is an insulating material, a conducting layer 603 can be deposited between substrate 601 and $LiCoO_2$ layer 602.

[079] Depositing materials on a thin substrate involves holding and positioning the substrate during deposition. Figures 7A, 7B, 7C, and 7D illustrate a reusable fixture 700 for holding a thin film substrate. As shown in Figure 7A, reusable fixture 700 includes a top portion 701 and a bottom portion 702 that snap together. Thin substrate 601 is positioned between top portion 701 and bottom portion 702. As shown in Figure 7B, top portion 701 and bottom portion 702 are such that substrate 601 is brought into tension and subsequently clamped as top portion 701 is closed into bottom portion 702. Substrate 601 can be easily held by fixture 700 so that substrate 601 can be handled and positioned. In some embodiments, the corners of substrate 601, areas 703, are removed so that substrate 601 is more easily stretched by avoiding "wrap-around" corner clamping effects when top portion 701 is closed into bottom portion 702.

[080] As shown in Figure 7C, a mask 712 can be attached to fixture 700. In some embodiments, fixture 700 includes guides in order to align fixture 700 with respect to mask 712. In some embodiments, mask 712 may be attached to fixture 700 and travel with fixture 700. Mask 712 can be positioned at any desired height above substrate 601 in fixture 700. Therefore, mask 712 can function as either a contact or proximity mask. In some embodiments, mask 712 is formed of another thin substrate mounted in a fixture similar to fixture 700.

[081] As shown in Figure 7C and 7D, fixture 700 and mask 712 can be positioned relative to mount 710. Mount 710, for example, can be a susceptor, mount, or an electrostatic chuck of a processing chamber such as that shown in Figures 1A and 1B. Fixture 700 and

mask 712 can have features that allow for ready alignment with respect to each other and with respect to mount 710. In some embodiments, mask 712 is resident in the processing chamber and aligned with fixture 700 during positioning of fixture 700 on mount 710, as shown in Figure 7D.

[082] Utilizing fixture 700 as shown in Figures 7A, 7B, 7C, and 7D allows processing of a thin film substrate in a processing chamber. In some embodiments, thin film substrates can be about 10 µm or more. Further, thin film substrate 601, once mounted within fixture 700, can be handled and moved from process chamber to process chamber. Therefore, a multiprocessor chamber system can be utilized to form stacks of layers, including one or more layers of $LiCoO_2$ deposited according to embodiments of the present invention.

[083] Figure 8 illustrates a cluster tool 800 for processing thin film substrates. Cluster tool 800 can, for example, include load lock 802 and load lock 803, through which mounted thin film substrate 601 is loaded and a resultant device is removed from cluster tool 800. Chambers 804, 805, 806, 807, and 808 are processing chambers for depositions of materials, heat treatments, etching, or other processes. One or more of chambers 804, 805, 806, 807, and 808 can be a pulsed-DC PVD chamber such as that discussed above with respect to Figures 1A and 1B and within which a $LiCoO_2$ film deposited according to embodiments of the present invention may be deposited.

[084] Processing chambers 804, 805, 806, 807, and 808 as well as load locks 802 and 803 are coupled by transfer chamber 801. Transfer chamber 801 includes substrate transfer robotics to shuttle individual wafers between processing chambers 804, 805, 806, 807, and 808 and load locks 802 and 803.

[085] In production of a conventional thin-film battery, ceramic substrates are loaded into load lock 803. A thin metallic layer can be deposited in chamber 804, followed

by a $LiCoO_2$ deposition performed in chamber 805. The substrate is then removed through load lock 803 for an in-air heat treatment external to cluster tool 800. The treated wafer is then reloaded into cluster tool 800 through load lock 802. A LiPON layer can be deposited in chamber 806. The wafer is then again removed from cluster tool 800 for deposition of the lithium anode layer, or sometimes chamber 807 can be adapted to deposition of the lithium anode layer. A second metallic layer is deposited in chamber 808 to form a charge collector and anode collector. The finished battery structure is then off-loaded from cluster tool 800 in load lock 802. Wafers are shuttled from chamber to chamber by robotics in transfer chamber 801.

[086] A battery structure produced according to the present invention could utilize thin film substrates loaded in a fixture such as fixture 700. Fixture 700 is then loaded into load lock 803. Chamber 804 may still include deposition of a conducting layer. Chamber 805 then includes deposition of a $LiCoO_2$ layer according to embodiments of the present invention. A LiPON layer can then be deposited in chamber 806. Chamber 807 may still be adapted to deposition of a lithium rich material such as lithium metal and chamber 808 can be utilized for deposition of the conducting layer of the current collector. In this process, no heat treatment is utilized to crystallize the $LiCoO_2$ layer.

[087] Another advantage of a thin film battery process is the ability to stack battery structures. In other words, substrates loaded into cluster tool 800 may traverse process chambers 804, 805, 806, 807, and 808 multiple times in order to produce multiply stacked battery structures. Figures 9A and 9B illustrate such battery structures.

[088] Figure 9A illustrates a parallel coupled stacking. As shown in Figure 9A, a substrate 601, which for example can be a plastic substrate, is loaded into load lock 803. A conducting layer 603, for example about 2 μm of aluminum, copper, iridium or other material, acts as a bottom current collector. Conducting layer 603, for example, can be

deposited in chamber 804. A $LiCoO_2$ layer 602 is then deposited on conducting layer 603. $LiCoO_2$ layer 602 can be about 3-10 μm and can be deposited in chamber 805 according to embodiments of the present invention. The wafer can then be moved to chamber 806 where a LiPON layer 901 of thickness of about .5 to about 2 μm can be deposited. In chamber 807, an anode layer 902, for example a lithium metal layer of up to about 10 μm, can then be deposited in chamber 807. A second conducting layer 903 can then be deposited over anode layer 902. A second battery stack can then be deposited over the first battery stack formed by metal layer 603, LiCoO2 layer 602, LiPON layer 901, lithium layer 902, and current collection conduction layer 903. Over current collection conducting layer 903, another lithium layer 902 is formed. Another LiPON layer 901 is formed over lithium layer 902. Another LiCoO2 layer 602 is formed over LiPON layer 901 and finally another metal layer 603 is formed over LiCoO2 layer 602. In some embodiments, further stackings can be formed. In some embodiments, metal layers 603 and 903 differ in the mask utilized in deposition so that tabs are formed for electrical coupling of layers.

[089] As discussed above, any number of individual battery stacks can be formed such that parallel battery formations are formed. Such a parallel arrangment of battery stacking structure can be indicated as Current collector/LiCoO2/LiPON/Anode/current collector/Anode/LiPON/LiCoO2/current collector/LiCoO2 . . . /current collector. Figure 9B illustrates an alternative stacking corresponding to the battery structure current collector/LiCoO2/LiPON/anode/current collector/LiCoO2/LiPON/anode/current collector . . . /current collector. In this case, a series arrangement battery stacking structure is formed because the individual battery stacks share anodes.

[090] To form the structures shown in Figures 9A and 9B, substrates are rotated again through the chambers of cluster tool 800 in order to deposit the multiple sets of batteries. In general, a stack of any number of batteries can be deposited in this fashion.

[091] In some embodiments, stoichiometric $LiCoO_2$ can be deposited on iridium. Figures 10A through 10D illustrate an anneal procedure for Li-Co deposition over an iridium layer that has been deposited on a Si wafer. The $LiCoO_2$ deposition was accomplished as discussed above with a target power of 2 kW, no bias power, reverse time of 1.6 μs, a pulsing frequency of 300 kHz, with 60 sccm Ar flow and 20 sccm of O_2 flow, with no pre-heat for 7200 sec. As a result, a layer of $LiCoO_2$ of about 1.51 μm was deposited.

[092] Figures 10A through 10D show XRD analysis of both as-deposited and annealed layers of $LiCoO_2$ deposited as discussed above. The XRD analysis of the as-deposited layer demonstrates a shallow peak at $2\theta = 18.85°$ denoting a <003> orientation of crystalline $LiCoO_2$, a sharper peak at about $2\theta = 38.07°$ corresponding with the desired <101> crystallographic direction, and a peak at $2\theta = 40.57°$ corresponding to the <111> direction of iridium. However, the position of the <101> $LiCoO_2$ peak indicates that the <101> $LiCoO_2$ peak is nonstoichiometric $LiCoO_2$. In order to be useful as a battery layer, stoichiometric $LiCoO_2$ provides for the best Li transport. One of ordinary skill in the art will notice that careful adjustment of deposition parameters can provide stoichiometric $LiCoO_2$ of desired orientation.

[093] Figure 10B shows an XRD analysis of the sample shown in figure 10A after a 300°C anneal in air for 2 hours. As shown in Figure 10B, the XRD peak corresponding to <003> $LiCoO_2$ grows, indicating crystallization of $LiCoO_2$ into the <003> direction. Further, the <101> peak of $LiCoO_2$ shifts slightly to $2\theta = 38.53°$, indicating a more stoichiometric crystallization of the <101> $LiCoO_2$. However, the crystalline $LiCoO_2$ is still not stoichiometric after this anneal. One of ordinary skill in the art will notice that longer anneals and/or further adjustment of the deposited stoichiometry may result in usefully oriented stoichiometric $LiCoO_2$ layers with anneal temperatures at 300 °C or less. Consequently, low temperature materials such as polymers, glass, or metal may be utilized as the substrate.

[094] Figure 10C illustrates an XRD analysis from the sample after a subsequent 500°C anneal in air for 2 hours. As shown in Figure 10C, more of the $LiCoO_2$ crystalizes into the <003> layer. Further, the <101> $LiCoO_2$ peak shifts again to $2\theta = 39.08°$, indicating crystallization of a <012> layer of $LiCoO_2$. In this case, the <012> $LiCoO_2$ cyrstal is stoichiometric and therefore allows for efficient Li transport. One of ordinary skill in the art will notice that longer anneals and/or further adjustment of the deposited stoichiometry may result in usefully oriented stoichiometric $LiCoO_2$ layers with anneal temperatures at 500°C or less. Consequently, low temperature materials such as polymers, glass, or metal may be utilized as the substrate.

[095] Figure 10D illustrates an XRD analsysis of the sample after a subsequent anneal of 700°C in air for 2 hours. As shown in Figure 10D, the <003> $LiCoO_2$ peak disappears, but the <012> $LiCoO_2$ peak remains relatively the same as that shown in the 500° anneal illustrated in Figure 10C.

[096] Figures 10A through 10D demonstrate deposition of <101> $LiCoO_2$ at low temperature over an iridium layer. Subsequent anneals to 500°C may be desired to change the stoichiometry of the <101> $LiCoO_2$ layer, but anneals to 700 °C do not appear to be necessary. With anneal temperatures less than 500°C, depositions of a $LiCoO_2$ layer over a conducting iridium layer can be accomplished on glass, aluminum foil, plastic, or other low temperature substrate material. Anneal temperatures of less than 500°C but greater than 300°C or lengthening the time of lower temperature anneals may also result in desired orientations of stoichiometric crystalline $LiCoO_2$.

[097] Figures 11A through 11D illustrate formation of a single-layer battery according to some embodiments of the present invention. As shown in Figure 11A, a lift-off layer 1102 can be deposited on a substrate 1101. Further, an iridium layer 1103 can be

deposited over lift-off layer 1102. In some embodiments, substrate 1101 can be plastic, glass, Al foil, Si wafer, or any other material. Lift-off layer 1102 can be any lift off layer and can be a polymer layer such as polyimide, an inorganic layer such as CaF_2 or carbon, or an adhesive layer that loses its adhesion as a result of, for example, oxidation, heat, or light. Lift-off layers are well known. Iridium layer 1103 can be from about 500 Å or more.

[098] As shown in Figure 11B, a $LiCoO_2$ layer is deposited over iridium layer 1103 as was discussed above. In some embodiments, an anneal can be performed at this step. In some embodiments, further layers of the battery may be deposited before an anneal step is performed. In some embodiments, a stoichiometric $LiCoO_2$ layer of a useful crystalline orientation may result in the as-deposited $LiCoO_2$ with no further anneals necessary.

[099] Figure 11C illustrates deposition of a LiPON layer 1105 over the $LiCoO_2$ layer, deposition of a Li layer 1106 over LiPON layer 1105, and deposition of an electrode layer 1107 over Li layer 1106. In some embodiments, an anneal step of up to 500°C as discussed above may be performed here.

[0100] As shown in Figure 11D, the resulting single-layer battery formed from iridium layer 1103, $LiCoO_2$ layer 1104, LiPON layer 1105, Li layer 1106, and electrode layer 1107 can be "lifted off" from substrate 1101. Such a single-layer battery can be a free-standing battery of thickness about 5 μm or greater. Such a battery, without the requirement of a substrate 1101, is well known to have the potential of energy storage of greater than about 1 kW-hr/liter.

[0101] As an alternative to a lift-off process as described in Figures 11A through 11D, a substrate may be removed during anneal leaving a single-layer battery. Further, in some embodiments, substrate 1101 can be removed by a solvent, etching, or a photo process. Further, single-layer batteries may be combined or stacked in any fashion to provide a device of greater energy storage at a particular voltage.

[0102] Figures 12A through 12L illustrate the crystallinity of as-grown and post anneal $LiCoO_2$ layers according to samples 31 and 32 illustrated in Table I. Samples 31 and 32 were formed in the same deposition, utilizing a silicon substrate and an alumina substrate, respectively.

[0103] Figure 12A illustrates an XRD analysis of the as-deposited $LiCoO_2$ film on Al_2O_3 substrate (Example 32 in Table I). A broad <003> crystalline $LiCoO_2$ peak is observed. The remaining peaks in the analysis, which are not labeled in Figure 12A, result from the Al_2O_3 substrate. The <003> peak is characteristic of the layered structure in the as-deposited crystalline $LiCoO_2$ film according to embodiments of the present invention.

[0104] Figure 12B illustrates the crystallinity of the LiCoO2 film shown in Figure 12A after a 2 hr 700 °C anneal. As shown in Figure 12B, the <003> peak becomes sharper and higher, indicating better crystallinity. As shown in Figures 12G through 12J, in comparison with figures 12C through 12F, the columnar structure ripens with the anneal and the grain size becomes larger with anneal. Figure 12B also shows <012> and <006> crystallinity peaks.

[0105] Figure 12C through 12F show SEM photos of the granularity of the as-deposited film corresponding to Example 32 in Figure I. Figures 12G through 12J show SEM photos of the granularity of the annealed film, as illustrated in Figure 12B. A comparison of Figures 12C through 12F with 12G through 12J illustrate the increased granularity resulting from the anneal process.

[0106] Figure 12K illustrates a fracture cross-section SEM that illustrates the morphology of the as-deposited crystalline film corresponding to Example 31 in Table I. Figure 12L illustrate a similar cross-section SEM corresponding to the film grown according to Example 32 in Table I.

[0107] Figures 13A through 13J illustrate rapid thermal anneal processes applied to a $LiCoO_2$ layer as in Example 49 of Table I. In that example, $LiCoO_2$ is deposited on alumina with a 2 kW pulsed DC power with no bias. Argon flow as set to 60 sccm and oxygen flow was set to 20 sccm. The deposition parameters are nearly identical with those of Example 32 in Table I, therefore XRD data for the as-deposited films are shown in Figure 12A. Figure 13A shows XRD data after a 15 minute 700 °C anneal in an argon atmosphere. Ramp-up time (room temperature to 700 °C) is 45 sec and ramp-down time (700 °C to about 300 °C) occurred over 10 min. At 300 °C, the sample is removed from the rapid-thermal-anneal (RTA) oven and cooled in air to room temperature. As shown in Figure 13A, substantial crystallinity is obtained. Figure 13B shows XRD data after a RTA as described with Figure 13A in an argon/oxygen atmosphere. The argon/oxygen ratio was 3:1.

[0108] As shown in a comparison of Figures 13A and 13B, more crystallinity is observed in an argon only RTA than with a RTA performed in the presence of oxygen. This is further illustrated in a comparison of Figures 13C and 13D with Figures 13E and 13F. Figures 13C and 13D show the granularity of the $LiCoO_2$ film after the RTA illustrated in Figure 13A. Figures 13E and 13F show the granularity of the $LiCoO_2$ film after the RTA illustrated in Figure 13B. As is observed, the granularity shown in Figures 13C and 13D (which differ in magnification) is better than that shown in Figures 13E and 13F (which also differ in magnification).

[0109] Figures 14A through 14D illustrate several anneal processes with the Example 37 of Table I. In that example, LiCoO2 was deposited on alumina utilizing a pulsed-dc process with 2kW of power and 100 W of bias with an argon flow of 60 sccm and an oxygen flow of 20 sccm.

[0110] Figure 14A shows an SEM photo of an as-deposited $LiCoO_2$ film according to the process illustrated in Example 37 of Table I. Figure 14B shows an SEM photo of

$LiCoO_2$ film according to the process illustrated in Example 37 of Table I, annealed conventionally with a two-hour 700 °C anneal. Figures 14C and 14D show SEM photos of a $LiCoO_2$ film according to the process illustrated in Example 37 of Table I, annealed in an RTA process at 700 °C. The ramp-up and ramp-down times in the RTA process is illustrated above. Figure 14C shows an SEM photo of a $LiCoO_2$ film after an RTA process at 700 °C for five minutes whereas Figure 14D shows an SEM photo of a $LiCoO_2$ film after an RTA process at 700 °C for fifteen minutes. It is clear from a comparison of Figures 14C and 14D with Figure 14B, that much better granularity is achieved with the low thermal-budget RTA process rather than the conventional furnace anneal. A low thermal-budget RTA process allows for deposition of such films on low temperature substrates.

[0111] Figures 15A and 15B show SEM photos of a $LiCoO_2$ film that was annealed in an RTA process utilizing two different ramp-up times, illustrating the effects of the ramp time in the RTA process. A $LiCoO_2$ film was deposited on an alumina substrate according to the process described as Example 51 in Table I. The film shown in Figure 15A was annealed with a 45 sec ramp-up time (i.e., room temperature to 700 °C in 45 sec). The film shown in Figure 15B was annealed with a 240 sec ramp-up time. Both films were held at 700 °C for five minutes. As shown in a comparison between Figures 15A and 15B, it is clear that a short anneal ramp-up times yield better granularity than longer ramp-up times.

[0112] Figure 17 illustrates battery charge and discharge profiles of a battery structure formed utilizing $LiCoO_2$ films according to embodiments of the present invention. The $LiCoO_2$ film in the battery profiled in Figure 17 was deposited according to Example 54 in Table I. The $LiCoO_2$ film was deposited on an alumina substrate with a gold current collector. The $LiCoO_2$ film was annealed utilizing a fast-ramp (45 sec) RTA process as was described above. A 1.5 μm LiPON layer was then deposited with a standard RF deposition process without bias in a modified AKT reactor. A lithium anode and a nickel current collector were then deposited. Data was taken at 0.33 mA, 1.65 mA, 3.3 mA, 16.5 mA, 33 mA, and 66 mA. As observed, the battery was capable of storing an exceptional 25 mA/cm^2 at voltages greater than 2.0 V.

[0113] One skilled in the art will recognize variations and modifications of the examples specifically discussed in this disclosure. These variations and modifications are intended to be within the scope and spirit of this disclosure. As such, the scope is limited only by the following claims.

TABLE I

Example #	Target Power (kW)	Bias Power (W)	Reverse Time (µs)	Frequency (kHz)	Ar (sccm)	O_2 (sccm)	Initial Substrate Temperature (temperature during deposit) (°C)	Deposition Time (sec)	Film Thickness (µm)
1	2	0	1,6	250	80	0	30	10000	3.9
2	2	0		250	72	8	30	7200	1.7
3	2	100		250	72	8	30	7200	1.34
4	2	100		250	76	4	30	7200	1.57
5	2	100		250	76	4	200	7200	1.3
6	2	100		250	74	6	200	7200	1.3
7	2	0		300	72	8	30	7200	1.58
8	2	0		300	74	6	30	7200	
9	2	100		300	74	6	30	7200	
10	2	100		300	72	8	30	7200	
11	2	100		300	70	10	30	7200	
12	2	0		300	70	10	30	7200	
13	2	0		300	72	8	30	7200	1.58
14	2	0		300	74	6	30	7200	
15	2	0		300	60	20	30	7200	
16	2	0		300	50	30	30	7200	
17	2	200		300	60	20	30	7200	
18	2	50		300	60	20	30	7200	
19	2	0		300	70	10	30	7200	
20	2	0		300	65	15	30	7200	
21	3	0		300	65	15	30	7200	
22	2	0	1.6	250	60	20	30	7200	
23	3	0	1.6	250	60	20	30	7200	
24	2	0	1.6	250	60	20	30 (NPH)	7200	

25	2	0	1.6	250	60	20	10min heat 30min coc	7200	
26	2	0	1.6	250	60	20	no preheat	9000	
27	2	0		300	60	20	no preheat	7200	
28	2	0		300	60	20	15min heat, 10min	7200	
29	2	0		250	60	20	no preheat		
30	2	0		250	60	20	10min, 10min		
31	2	0	1.3	300	60	20	30 (220)	7200	4.81
32	2	0	1.3	300	60	20	30 (220)	7200	4.74
33	2	0	1.3	300	22.5	7.5	30 (220)	7200	3.99
34	2	0	1.3	300	22.5	7.5	30 (220)	7200	3.93
35	2	0	1.3	300	37.5	12.5	30 (220)	7200	3.64
36	2	0	1.3	300	37.5	12.5	30 (220)	7200	3.54
37	2	100	1.3	300	60	20	30 (220)	7200	4.54
38	2	200	1.3	300	60	20	30 (220)	7200	4.84
39	2	100	1.3	300	37.5	12.5	30 (220)	7200	4.30
40	2	100	1.3	300	22.5	7.5	30 (220)	7200	3.77
41	2	200	1.3	300	37.5	12.5	30 (220)	7200	3.92
42	2	200	1.3	300	60	20	400	7200	3.77
43	2	0	1.3	300	22.5	7.5	30(220)	7200	3.24
44	2	0	1.3	300	60	20	30(220)	7200	3.88
45	2	0	1.3	300	60	20	30(220)	3600	1.78
46	2	200	1.3	300	60	20	30(220)	3600	1.87
47	2	200	1.3	300	22.5	7.5	30(220)	3600	1.52
48	2	0	1.3	300	60	20	30(220)	6000	1.12
49	2	0	1.3	300	60	20	30(220)	10800	1.89
50	2	0	1.3	300	60	20	30(220)	14400	2.52
51	2	100	1.3	300	60	20	30(220)	10000	1.57
52	2	100	1.3	300	60	20	30(220)	10000	2.11
53	2	100	1.3	300	60	20	30(220)	6000	2.70

54	2	100	1.3	300	60	20	30(220)	6000	2.70

TABLE II

Example #	Phase	Lattice	Texture	d_{101} [Å]	2θ [°]	crystallite size [Å]
15	$LiCoO_2$	rhombohedral	strong [101]	2.376(1)	37.83	~1300
16	$LiCoO_2$	Rhombohedral	strong [101]	2.375(1)	37.85	~750
17	Co	cubic	random	--	—	<50
18	Co	cubic	random	—	—	<50
19	$LiCoO_2$	rhombohedral	strong [101]	2.370(1)	37.93	~1400
20	$LiCoO_2$	rhombohedral	strong [101]	2.372(1)	37.90	~1500
21	$LiCoO_2$	rhombohedral	strong [101]	2.370(1)	37.92	~1700
PDF	$LiCoO_2$	Rhombohedral	random	2.408(1)	37.31	—

WHAT IS CLAIMED IS:

1. A method of depositing a $LiCoO_2$ layer, comprising:

placing a substrate in a reactor;

flowing a gaseous mixture including argon and oxygen through the reactor; and

applying pulsed DC power to a target formed of $LiCoO_2$ positioned opposite the substrate,

wherein a crystalline layer of $LiCoO_2$ is deposited over the substrate.

2. The method of claim 1, further including applying an RF bias to the substrate.

3. The method of claim 1, wherein the crystalline layer is <101> oriented.

4. The method of claim 1, wherein the crystalline layer is <003> oriented.

5. The method of claim 1, wherein a grain size of the crystalline layer is between about 750 Å and about 1700 Å.

6. The method of claim 1 wherein the substrate is a material chosen from a set comprised of silicon, polymers, glasses, ceramics, and metals.

7. The method of claim 1, further including preheating the substrate to a temperature of about 200 °C.

8. The method of claim 1, wherein the substrate is a low temperature substrate.

9. The method of claim 8, wherein the low temperature substrate is one of a set of substrates including glass, plastic, and metal foil.

10. The method of claim 1, further including depositing an oxide layer on the substrate.

11. The method of claim 10, wherein the oxide layer is a silicon dioxide layer.

12. The method of claim 3, wherein the crystalline layer is deposited at a rate of greater than 1 μm per hour.

13. The method of claim 1 wherein the target is a ceramic $LiCoO_2$ sputter target with a resistance measured across about 4 cm of surface of less than about 500 kΩ.

14. The method of claim 1, further including depositing a metal layer on the substrate.

15. The method of claim 14, wherein the metal layer is iridium.

16. The method of claim 14, wherein the metal layer is platinum.

17. The method of claim 1, further including annealing the crystalline layer with a low thermal budget.

18. The method of claim 17, wherein annealing the crystalline layer includes annealing to 700°C in a rapid thermal anneal process for a period of time less than about 10 minutes.

19. The method of claim 14, further including annealing the $LiCoO_2$ layer at a temperature of less than or equal to about 500°C.

20. The method of claim 14, further including annealing the $LiCoO_2$ layer at a temperature of less than or equal to about 400°C.

21. A battery structure, comprising:

a crystalline $LiCoO_2$ layer deposited over a low-temperature substrate.

22. The structure of claim 21, further including a conducting layer deposited between the crystalline $LiCoO_2$ layer and the low-temperature substrate.

23. The structure of claim 22, wherein the conducting layer is an iridium layer.

24. The structure of claim 22, wherein the conducting layer is a platinum layer.

25. The structure of claim 21, further including a LiPON layer deposited over the $LiCoO_2$ layer.

26. The structure of claim 21, further including a second conducting layer deposited over the $LiCoO_2$ layer.

27. A stacked battery structure, comprising:

one or more battery stacks deposited on a thin substrate, wherein each battery stack comprises:

a conducting layer,

a $LiCoO_2$ layer deposited as a crystalline layer over the conducting layer,

a LiPON layer deposited over the crystalline $LiCoO_2$ layer,

an anode layer deposited over the LiPON layer; and

a top conducting layer deposited over the one or more battery stacks.

28. The stacked battery structure of claim 27, wherein the battery stacks form a parallel stacked battery structure.

29. The stacked battery structure of claim 27, wherein the battery stacks form a series stacked battery structure.

30. The stacked battery structure of claim 27, wherein the conducting layer is a metal layer deposited on a substrate.

31. The stacked battery structure of claim 30, wherein the metal layer is an iridium layer.

32. The stacked battery structure of claim 30, wherein the metal layer is a platinum layer.

33. The stacked battery structure of claim 30, wherein the substrate is a low temperature substrate.

34. The stacked battery structure of claim 27, wherein the conducting layer is a metallic foil.

35. The stacked battery structure of claim 34, wherein the metallic foil is formed of a metal from a group consisting of copper, gold, platinum, aluminum, stainless steel and other nickel or cobalt based super alloy.

36. A method of producing a battery, comprising:

loading a substrate into a cluster tool;

depositing a crystalline $LiCoO_2$ layer over a conducting layer in a chamber of the cluster tool with a pulsed-dc PVD process.

37. The method of claim 36, wherein depositing a crystalline $LiCoO_2$ layer includes depositing crystalline $LiCoO_2$ through a mask.

38. The method of claim 36, further including

depositing a conducting layer on the substrate.

39. The method of claim 36, further including depositing a LiPON layer over the $LiCoO_2$ layer.

40. The method of claim 39, further including deposition an anode over the LiPON layer.

41. The method of claim 40, further including depositing a conducting layer over the anode.

42. The method of claim 36, wherein the conducting layer is an iridium layer.

43. A fixture for holding a thin substrate, comprising:

a top portion; and

a bottom portion, wherein

the thin substrate is held when the top portion is attached to the bottom portion.

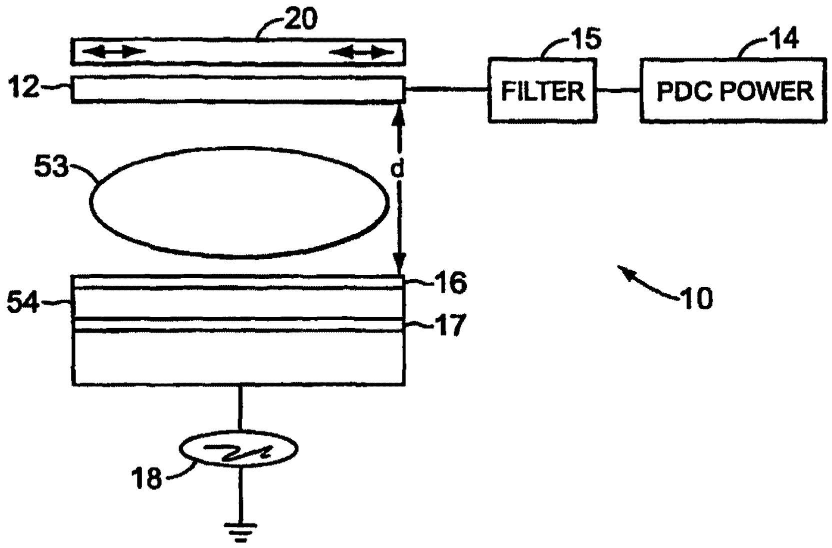

20
15
14
12
FILTER
PDC POWER
53
d
16
54
17
10
18

FIG. 1A

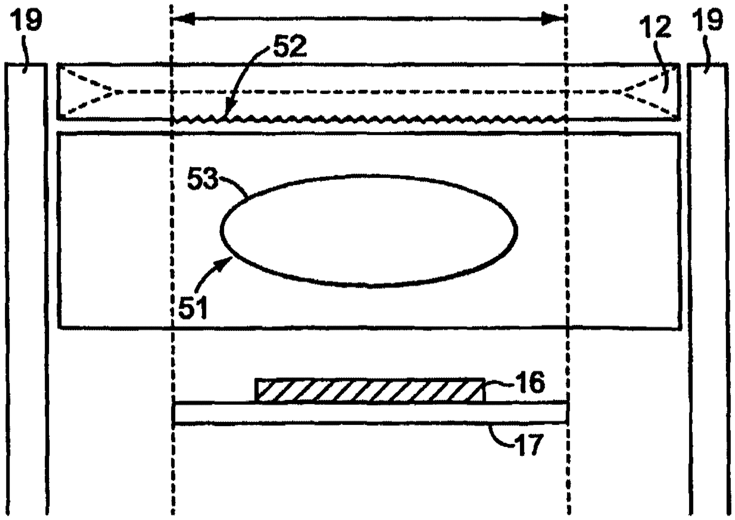

19
12
19
52
53
51
16
17

FIG. 1B

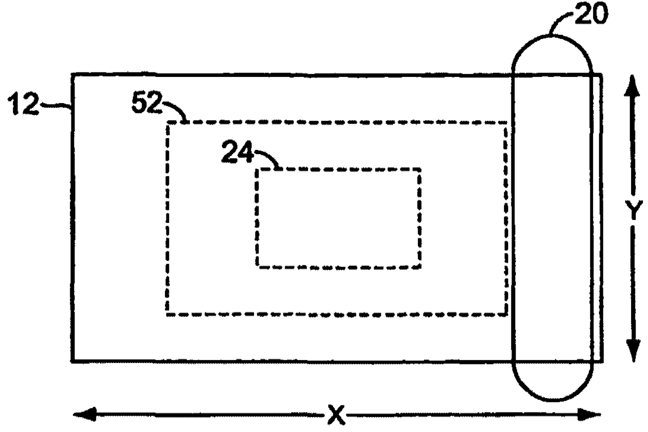


FIG. 2

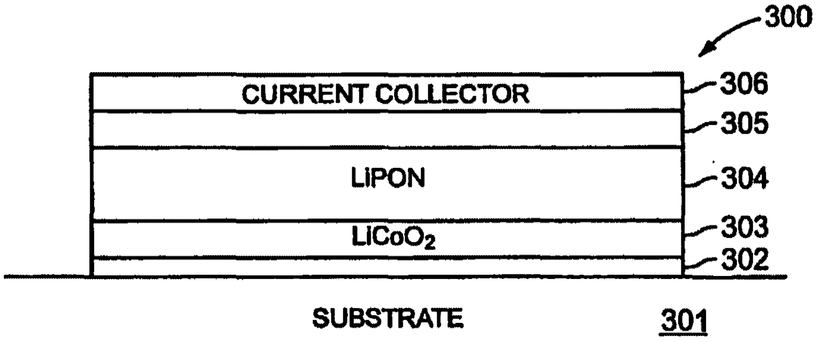


FIG. 3

FIG. 6A

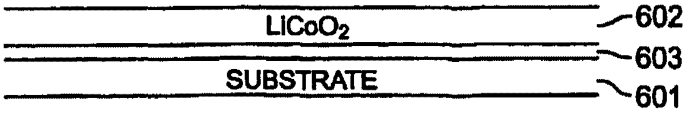


FIG. 6B

SUBSTITUTE SHEET (RULE 26)

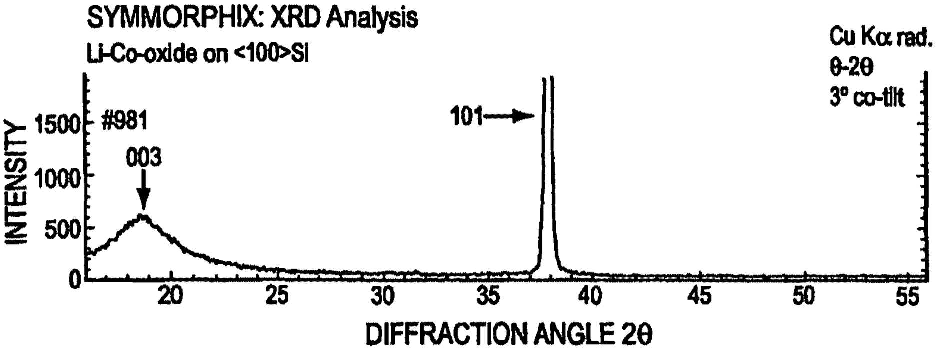

SYMMORPHIX: XRD Analysis
Li-Co-oxide on <100>Si
Cu Kα rad.
θ-2θ
3° co-tilt
#981
003
101
INTENSITY
1500
1000
500
0
20
25
30
35
40
45
50
55
DIFFRACTION ANGLE 2θ

FIG. 4A

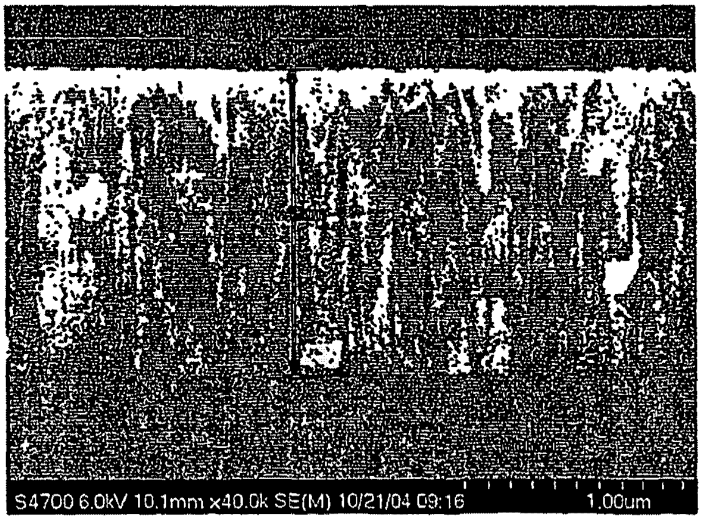

S4700 6.0kV 10.1mm x40.0k SE(M) 10/21/04 09:16
1.00um

FIG. 4B

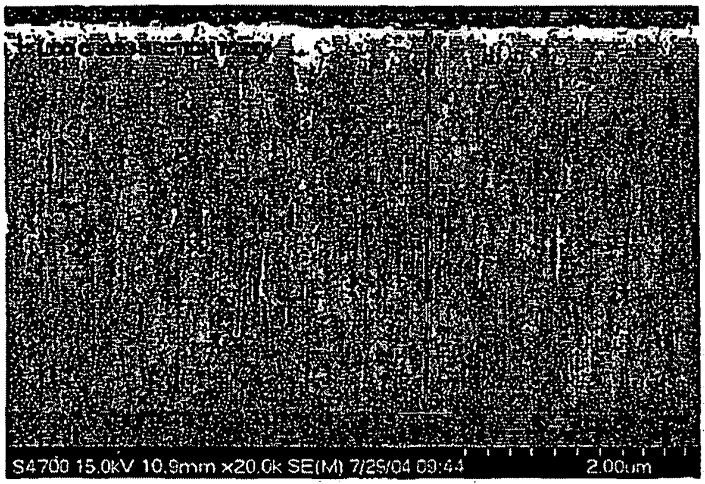

LDO CROSS SECTION
S4700 15.0kV 10.9mm x20.0k SE(M) 7/29/04 09:44
2.00um

FIG. 5A

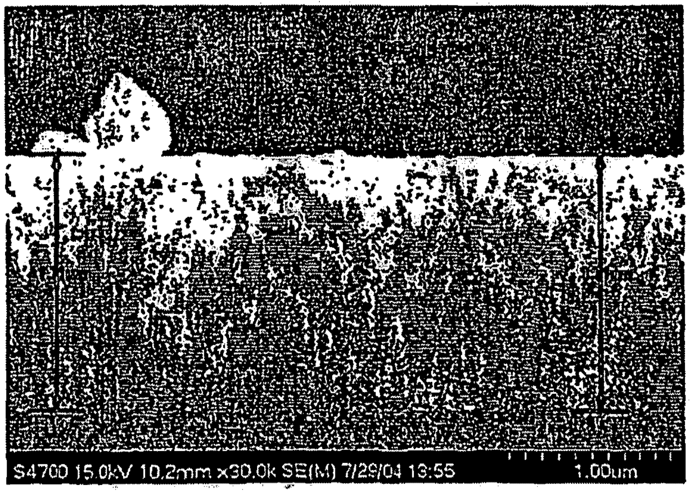

S4700 15.0kV 10.2mm x30.0k SE(M) 7/29/04 13:55
1.00um

FIG. 5B

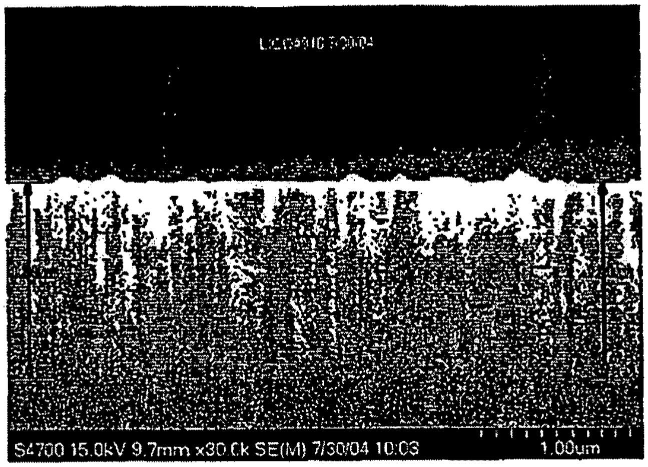

S4700 15.0kV 9.7mm x30.0k SE(M) 7/30/04 10:03
1.00um

FIG. 5C

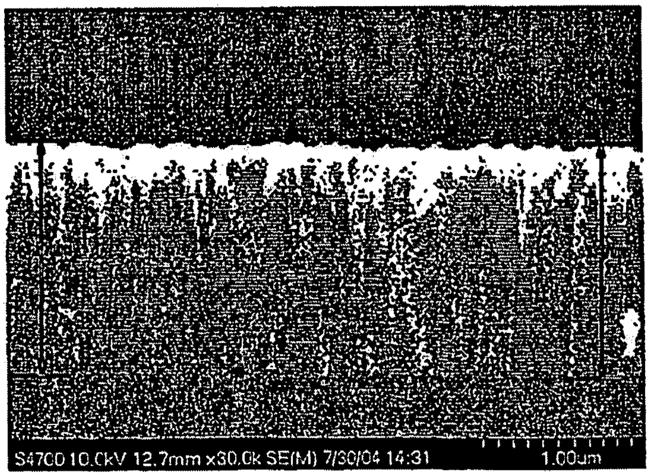

S4700 10.0kV 12.7mm x30.0k SE(M) 7/30/04 14:31
1.00um

FIG. 5D

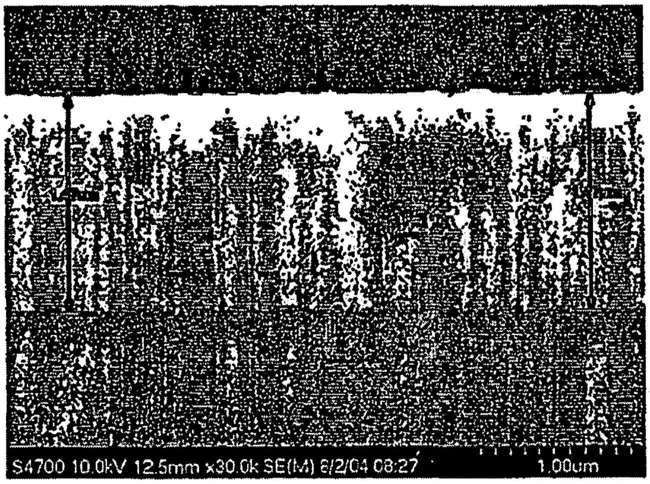

S4700 10.0kV 12.5mm x30.0k SE(M) 8/2/04 08:27
1.00um

FIG. 5E

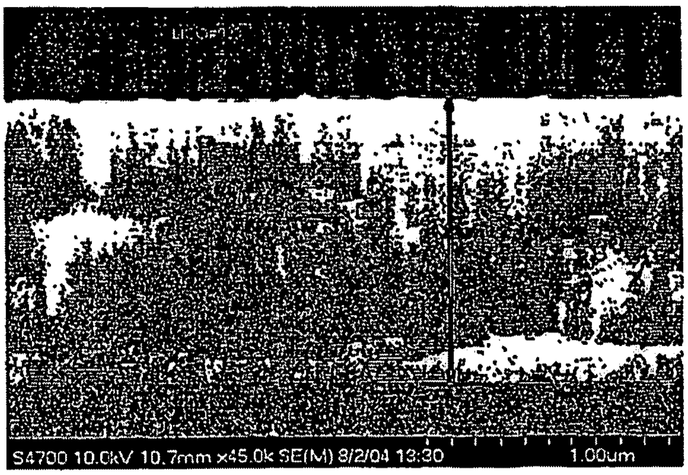

S4700 10.0kV 10.7mm x45.0k SE(M) 8/2/04 13:30
1.00um

FIG. 5F

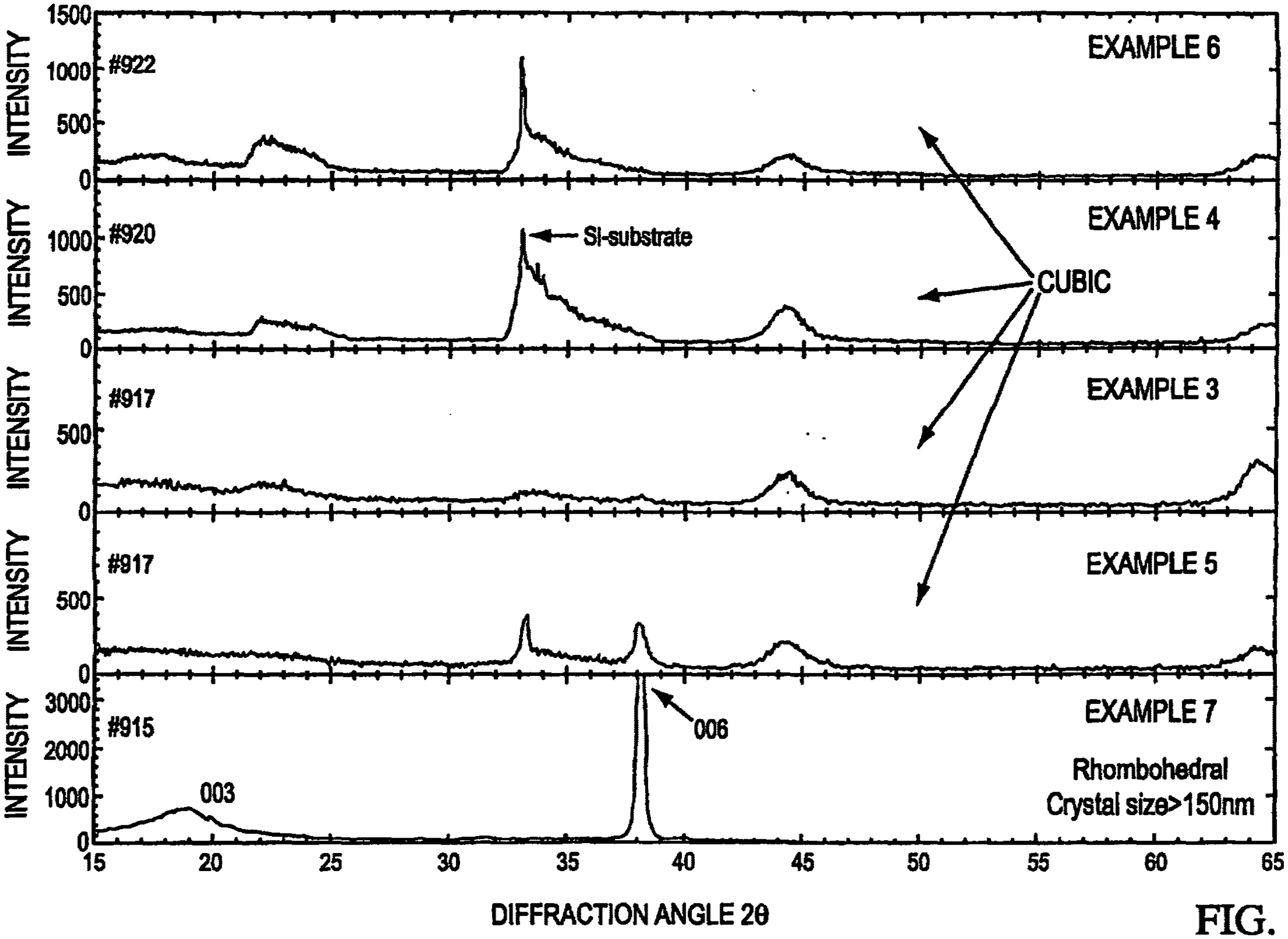

1500
1000
500
0
INTENSITY
#922
EXAMPLE 6
1000
500
0
INTENSITY
#920
Si-substrate
EXAMPLE 4
CUBIC
500
0
INTENSITY
#917
EXAMPLE 3
500
0
INTENSITY
#917
EXAMPLE 5
3000
2000
1000
0
INTENSITY
#915
003
006
EXAMPLE 7
Rhombohedral
Crystal size>150nm
15
20
25
30
35
40
45
50
55
60
65
DIFFRACTION ANGLE 2θ

FIG. 5G

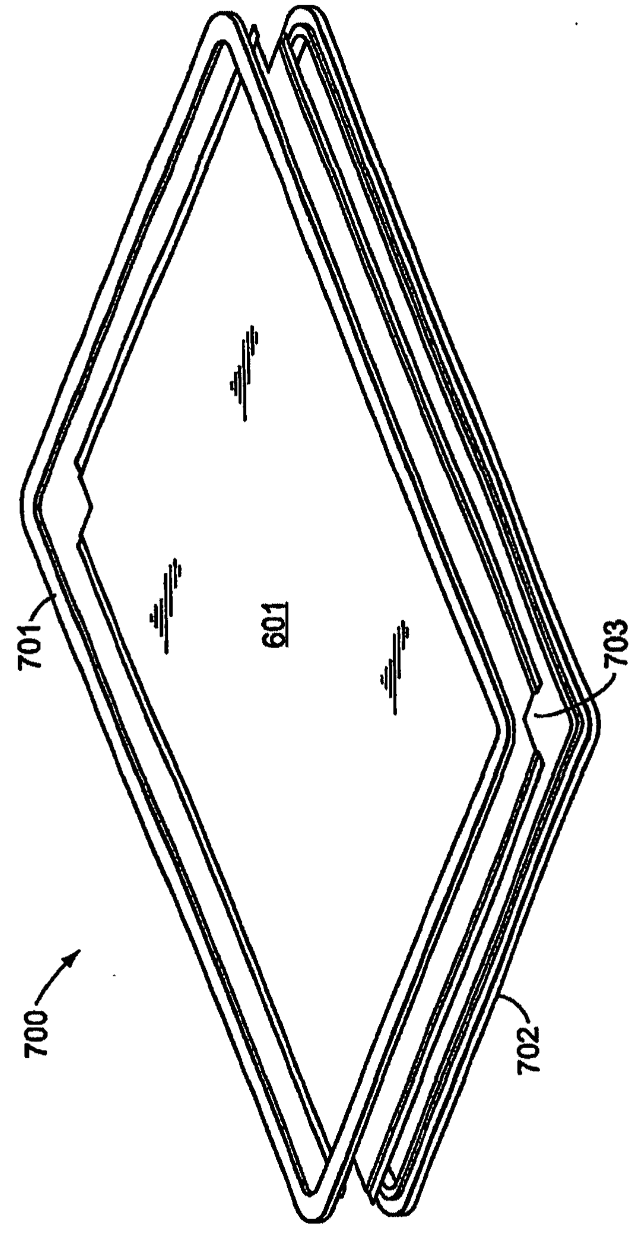


FIG. 7A

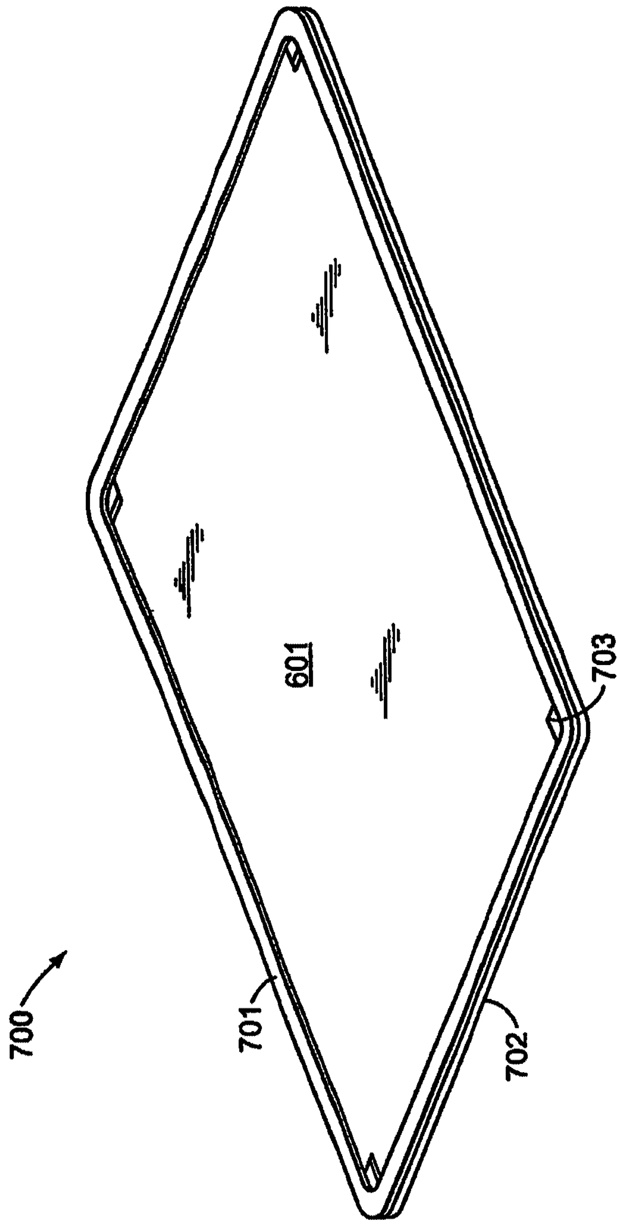


FIG. 7B

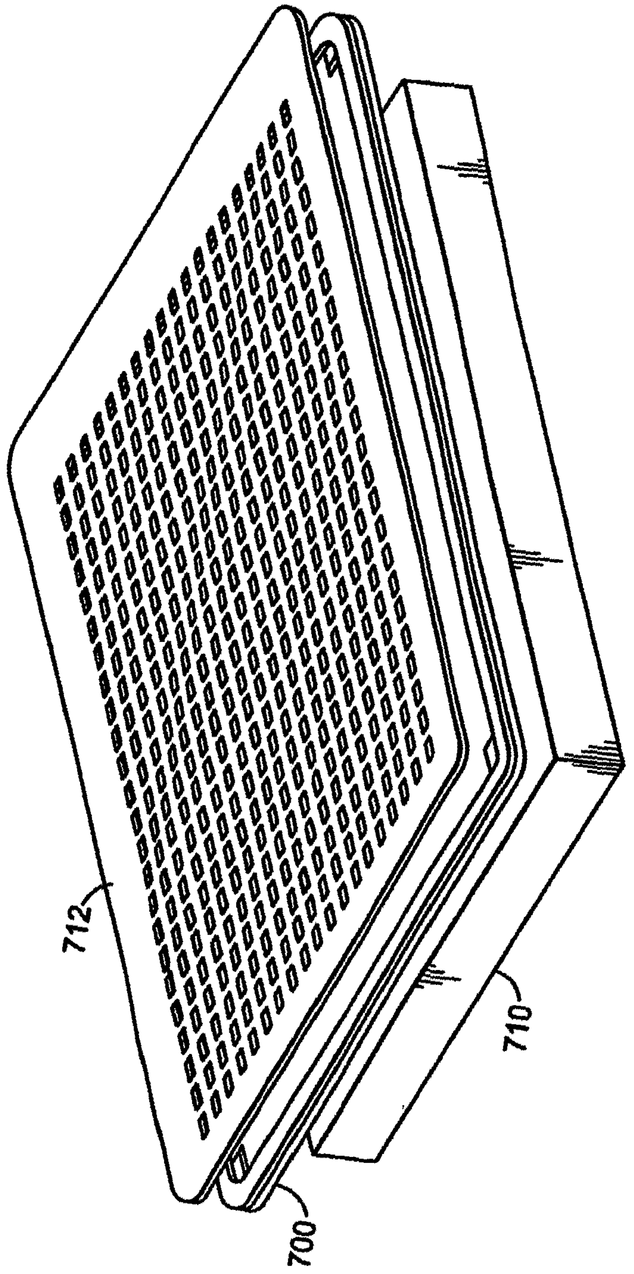


FIG. 7C

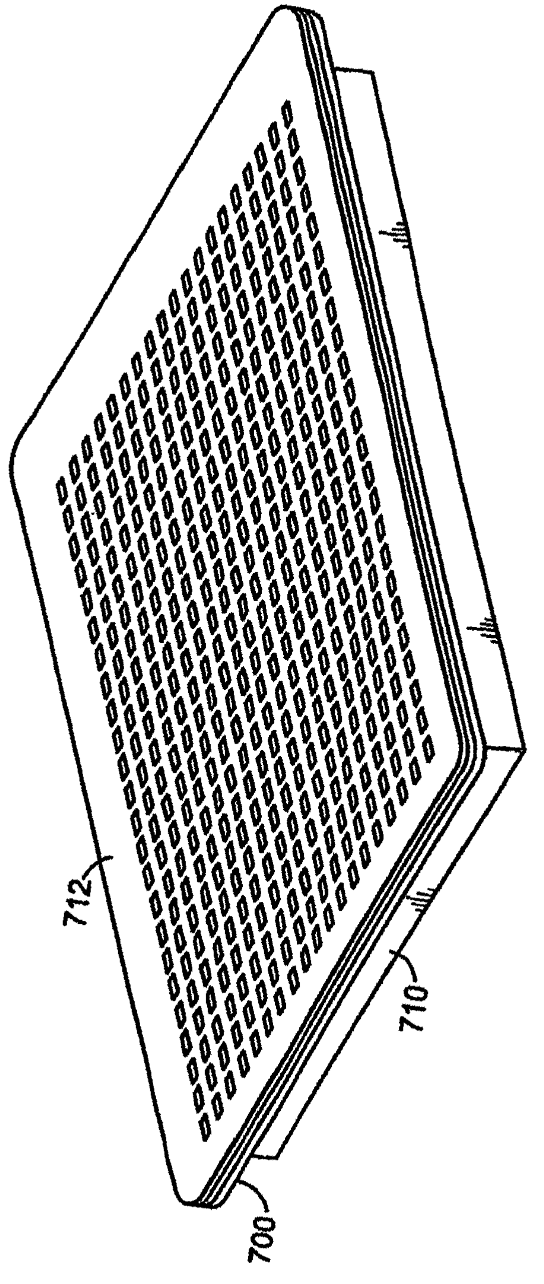


FIG. 7D

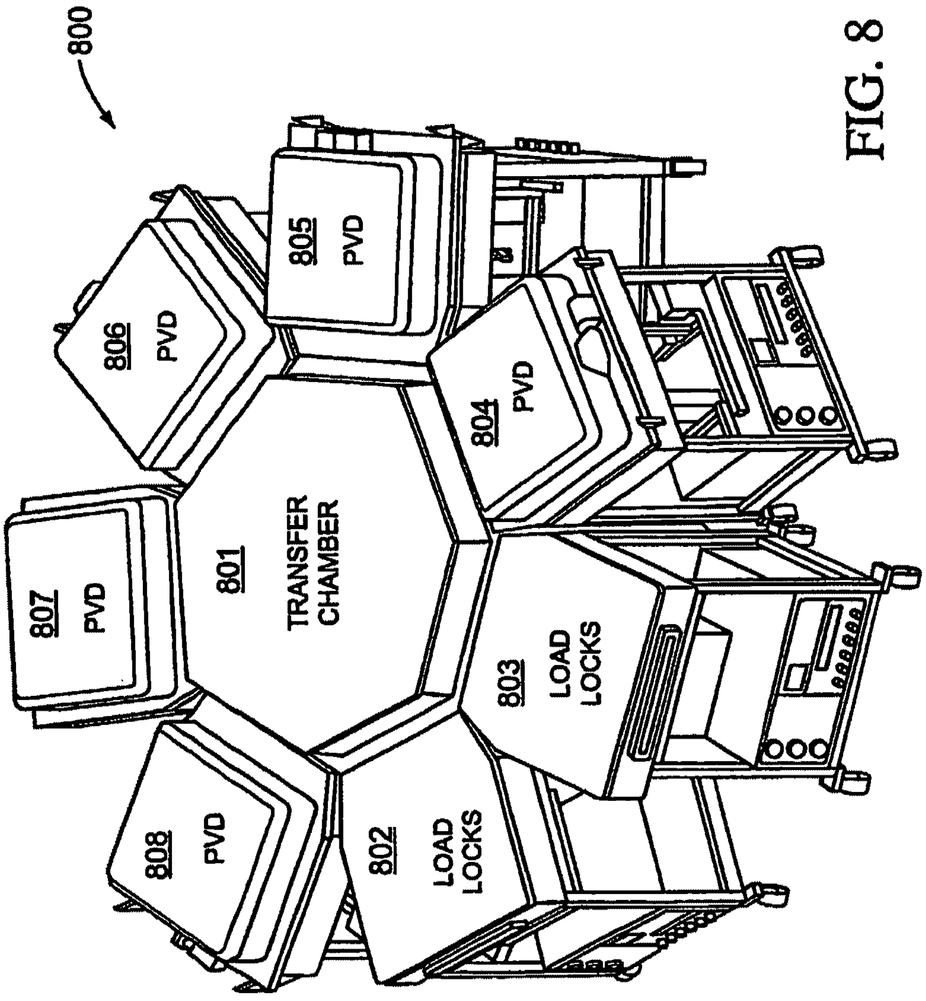

800
801
TRANSFER CHAMBER
802
LOAD LOCKS
803
LOAD LOCKS
804
PVD
805
PVD
806
PVD
807
PVD
808
PVD

FIG. 8

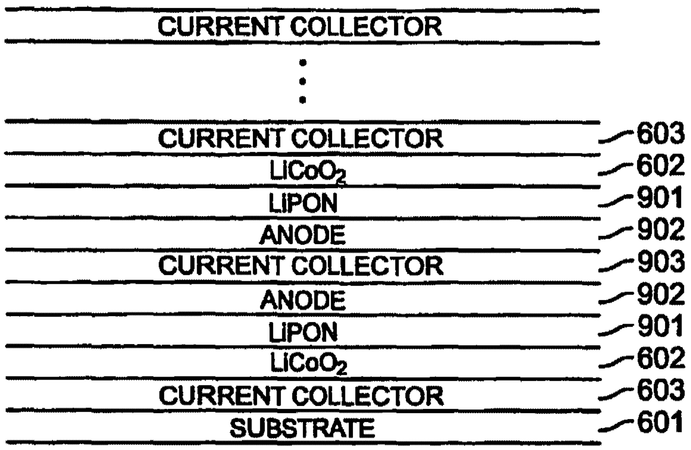

CURRENT COLLECTOR
CURRENT COLLECTOR 603
$LiCoO_2$ 602
LiPON 901
ANODE 902
CURRENT COLLECTOR 903
ANODE 902
LiPON 901
$LiCoO_2$ 602
CURRENT COLLECTOR 603
SUBSTRATE 601

FIG. 9A

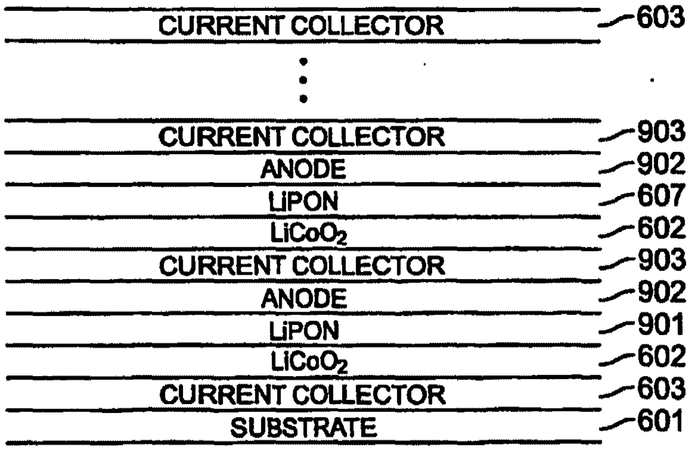

CURRENT COLLECTOR 603
CURRENT COLLECTOR 903
ANODE 902
LiPON 607
$LiCoO_2$ 602
CURRENT COLLECTOR 903
ANODE 902
LiPON 901
$LiCoO_2$ 602
CURRENT COLLECTOR 603
SUBSTRATE 601

FIG. 9B

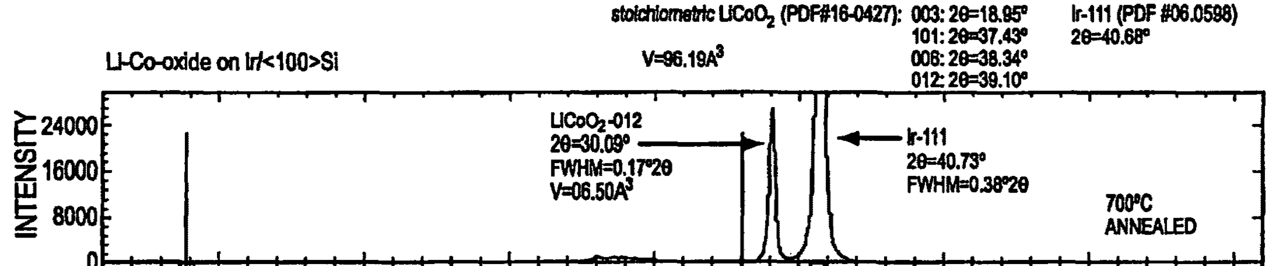


FIG. 10D

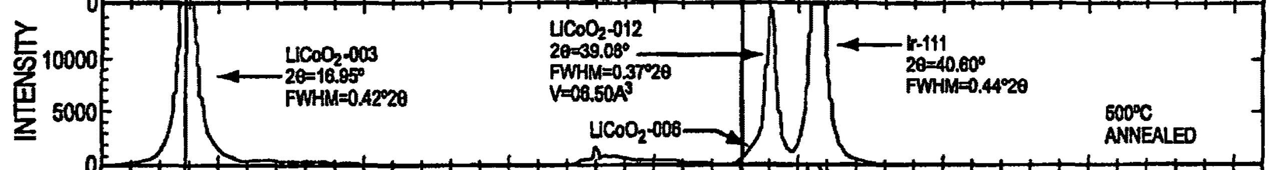


FIG. 10C

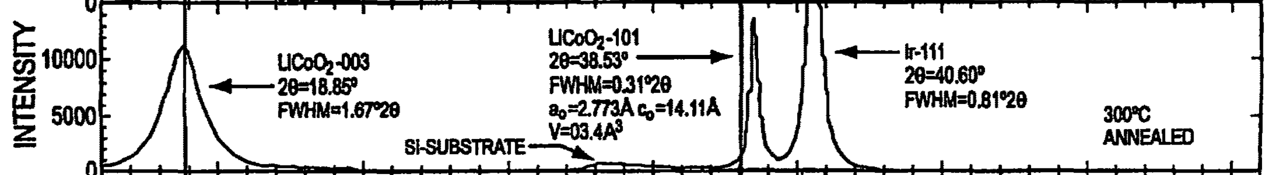


FIG. 10B

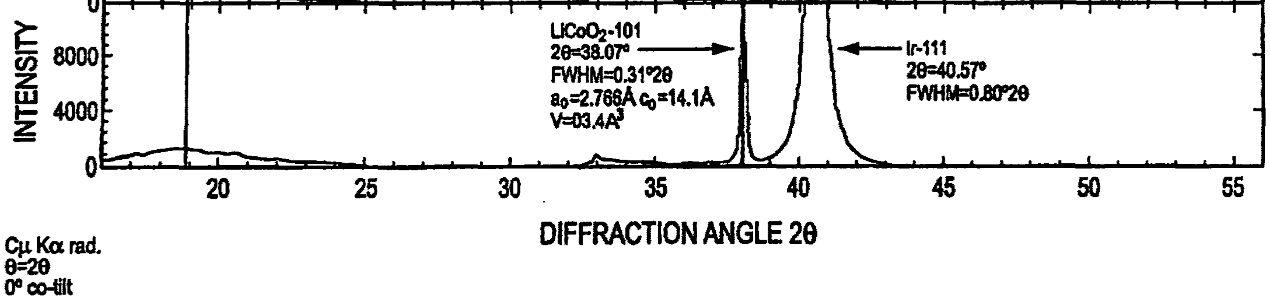


FIG. 10A

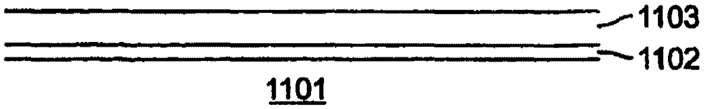


FIG. 11A

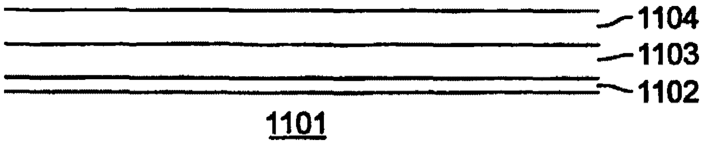


FIG. 11B

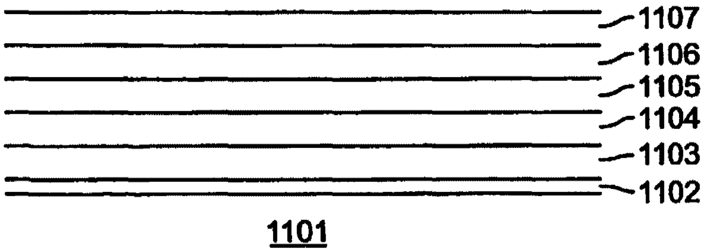


FIG. 11C

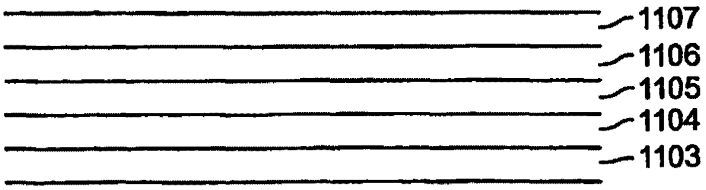


FIG. 11D

16/27

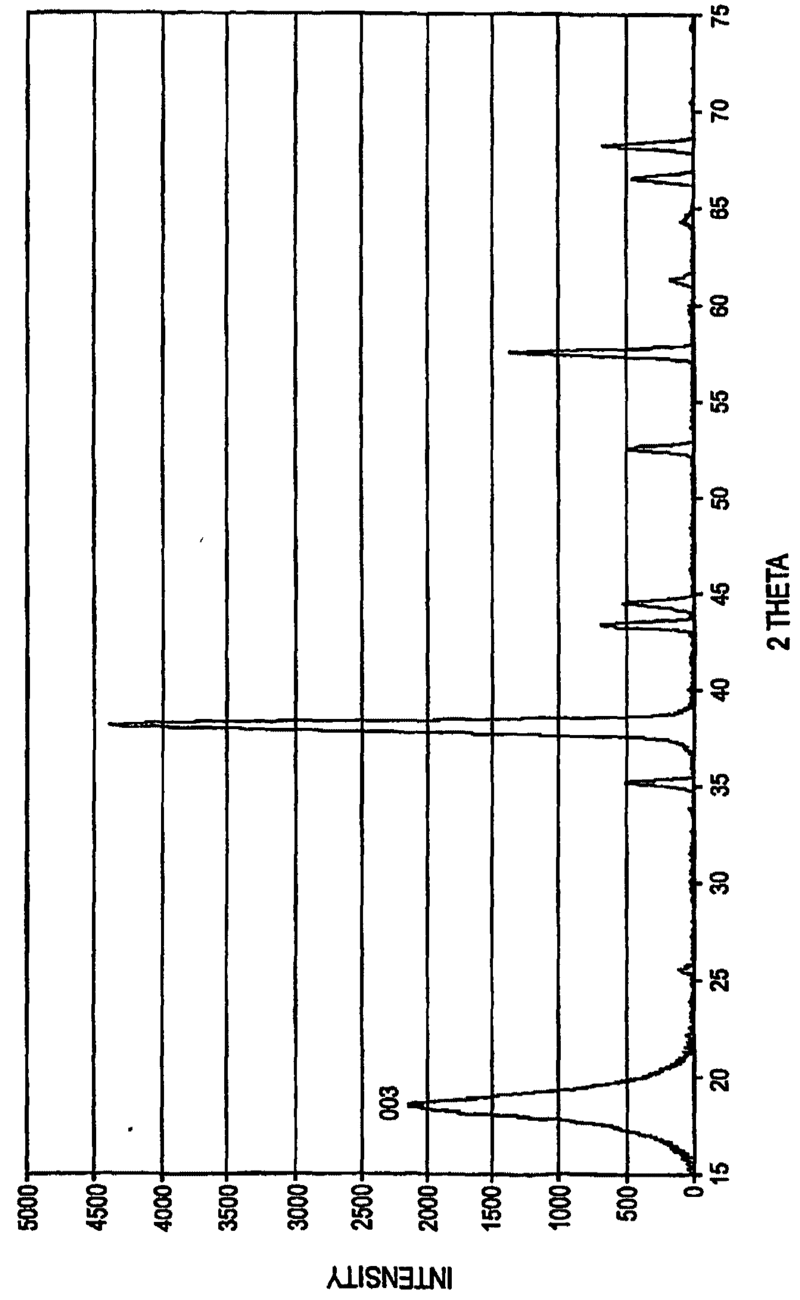

003
INTENSITY
5000
4500
4000
3500
3000
2500
2000
1500
1000
500
0
15
20
25
30
35
40
45
50
55
60
65
70
75
2 THETA

FIG. 12A

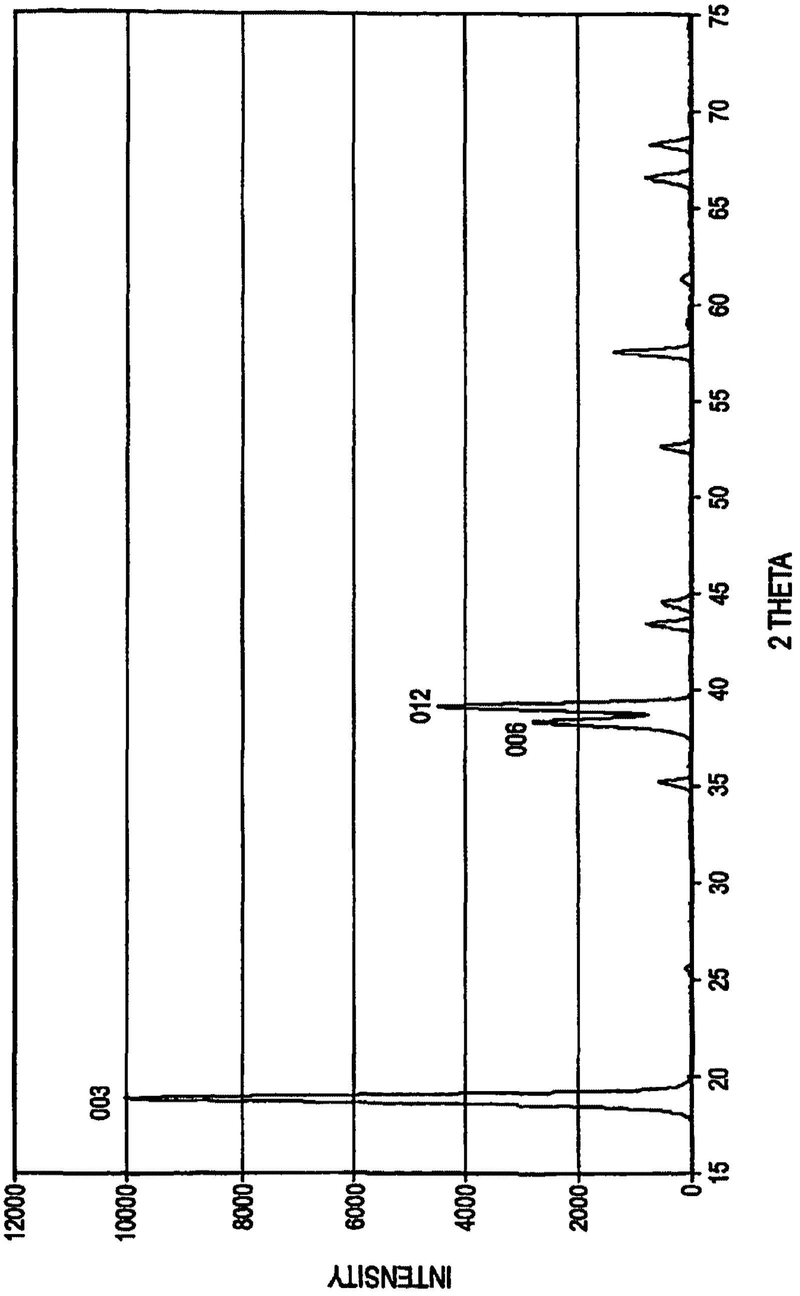

003
006
012
INTENSITY
0
2000
4000
6000
8000
10000
12000
2 THETA
15
20
25
30
35
40
45
50
55
60
65
70
75

FIG. 12B

18/27

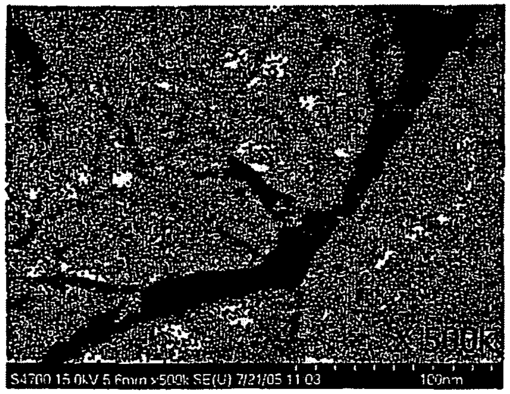


FIG. 12C

FIG. 12D

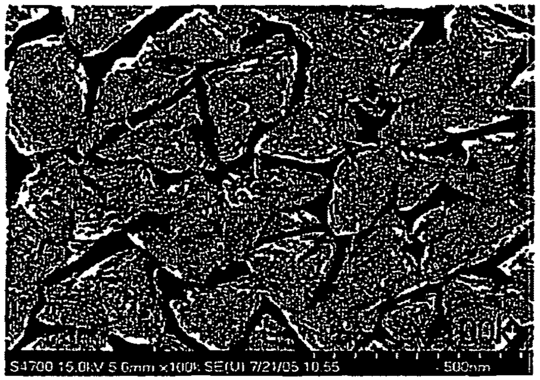


FIG. 12E

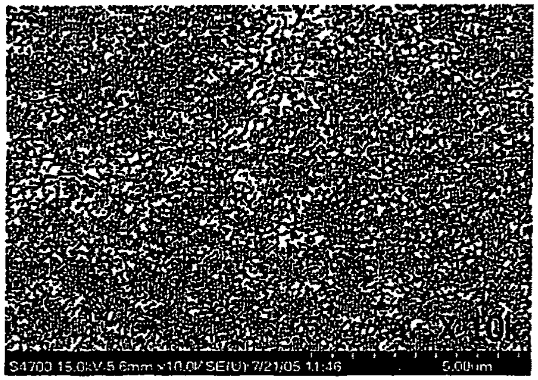


FIG. 12F

SUBSTITUTE SHEET (RULE 26)

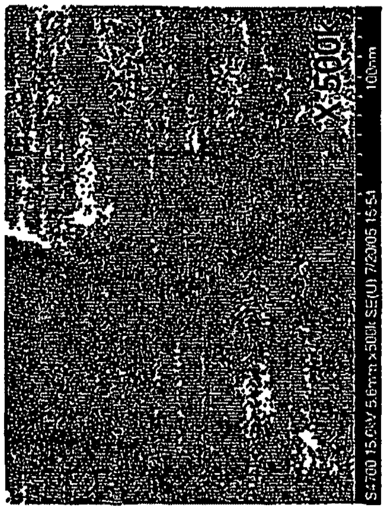


FIG. 12G

FIG. 12H

FIG. 12I

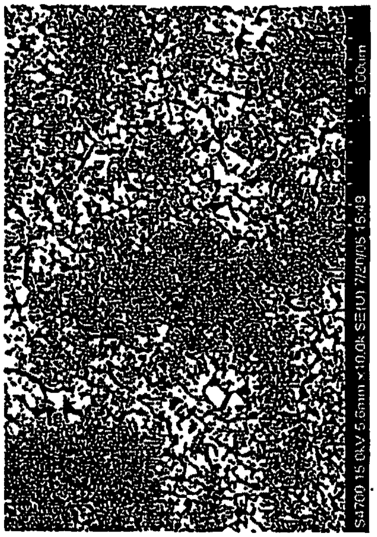
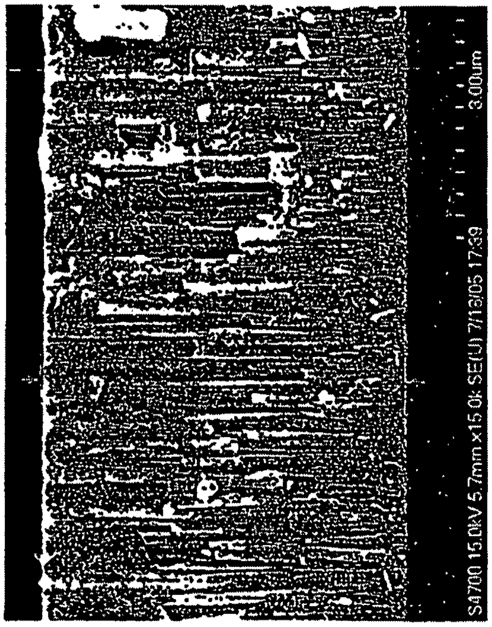


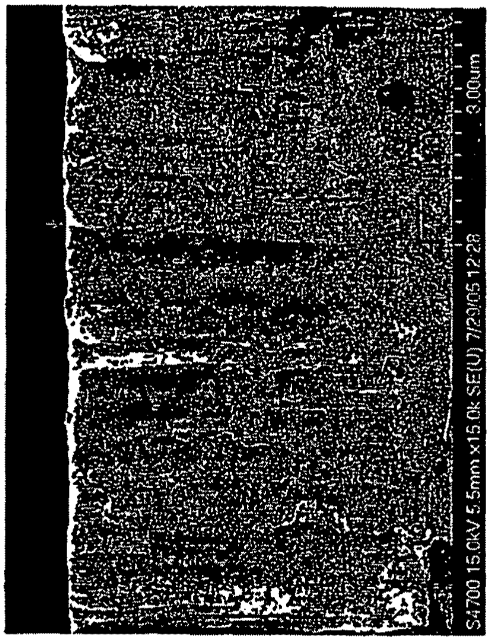
FIG. 12J

FIG. 12K



On Si

FIG. 12L



On alumina

SUBSTITUTE SHEET (RULE 26)

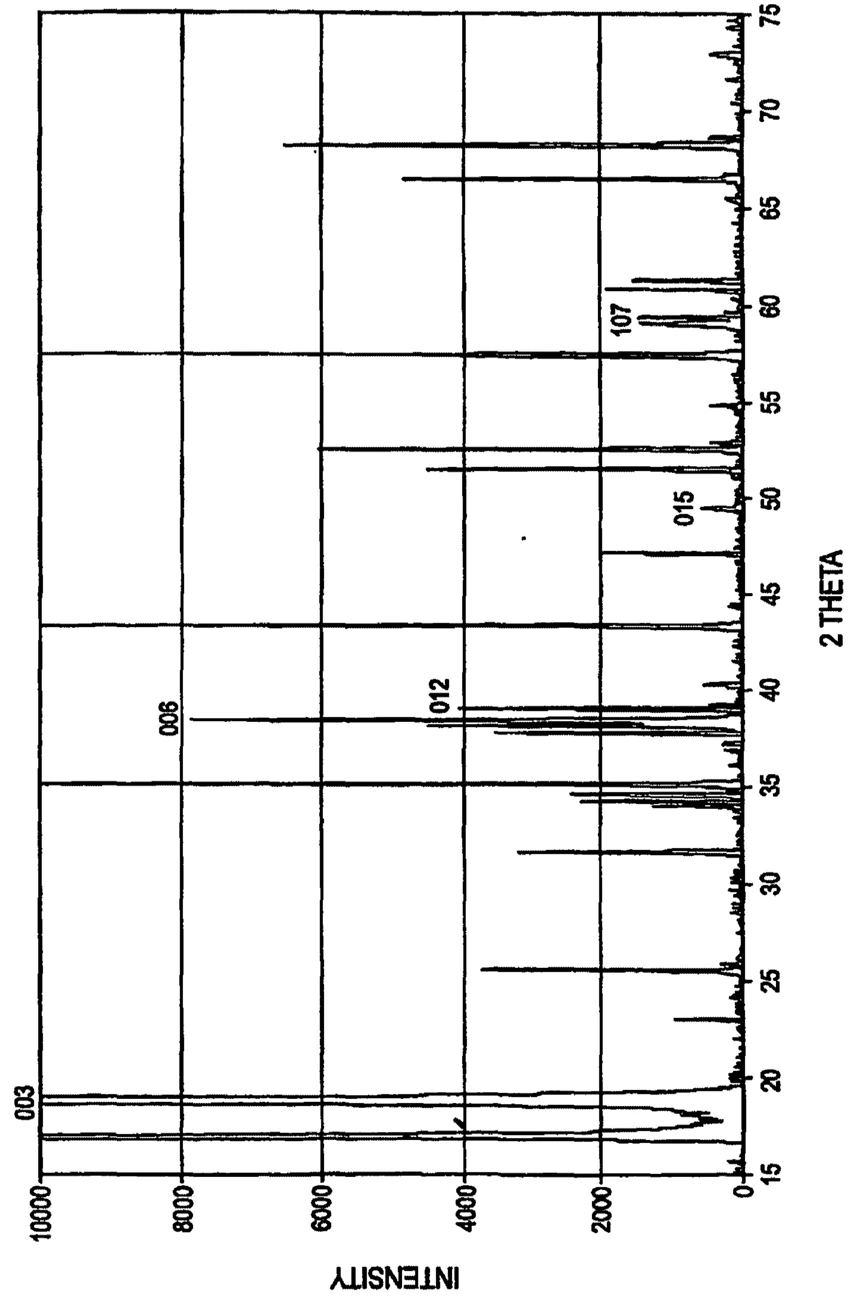

003
006
012
015
107
INTENSITY
10000
8000
6000
4000
2000
0
15
20
25
30
35
40
45
50
55
60
65
70
75
2 THETA

FIG. 13A

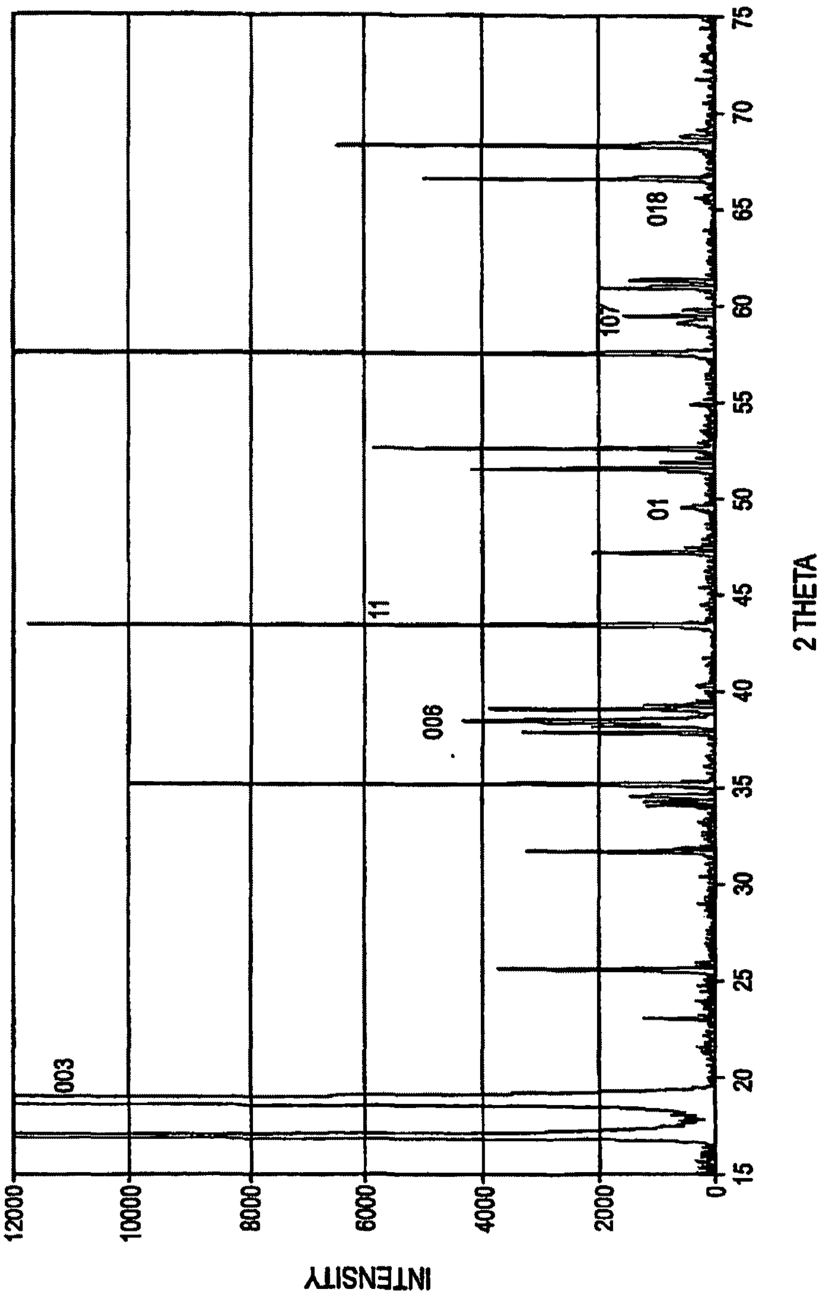

INTENSITY
12000
10000
8000
6000
4000
2000
0
2 THETA
15
20
25
30
35
40
45
50
55
60
65
70
75
003
006
11
01
107
018

FIG. 13B

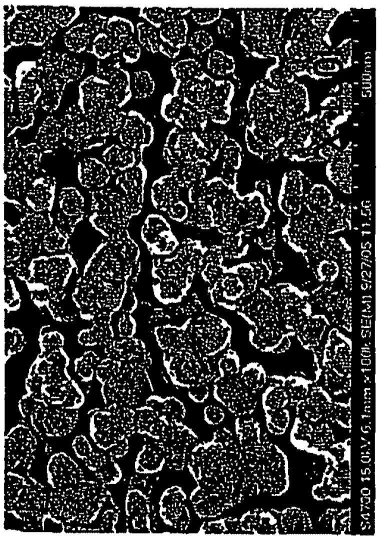
FIG. 13C

FIG. 13D

In Ar

FIG. 13E

FIG. 13F



In Ar/O_2 (3/1)

SUBSTITUTE SHEET (RULE 26)

FIG. 14A

As deposited

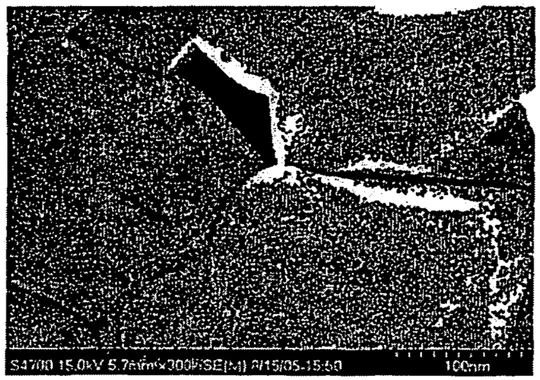
FIG. 14B

700CX2h

FIG. 14C

RTA-5m

FIG. 14D



RTA-700C15m

FIG. 15A

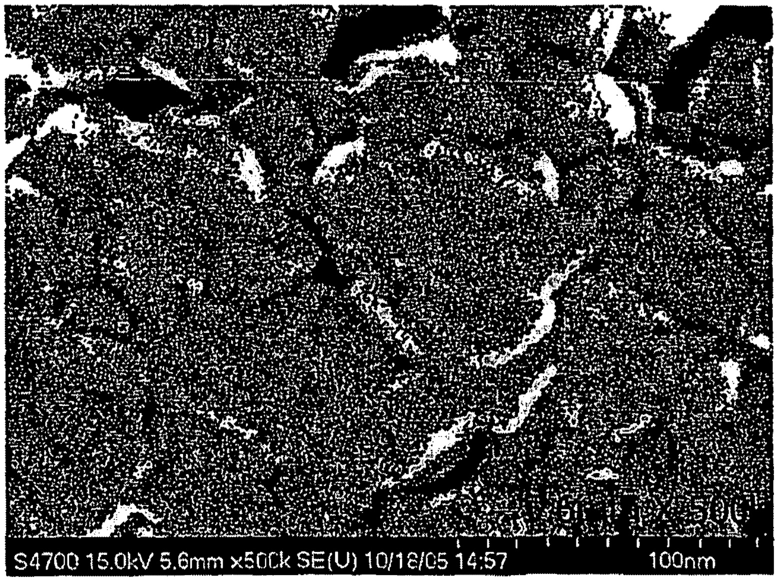
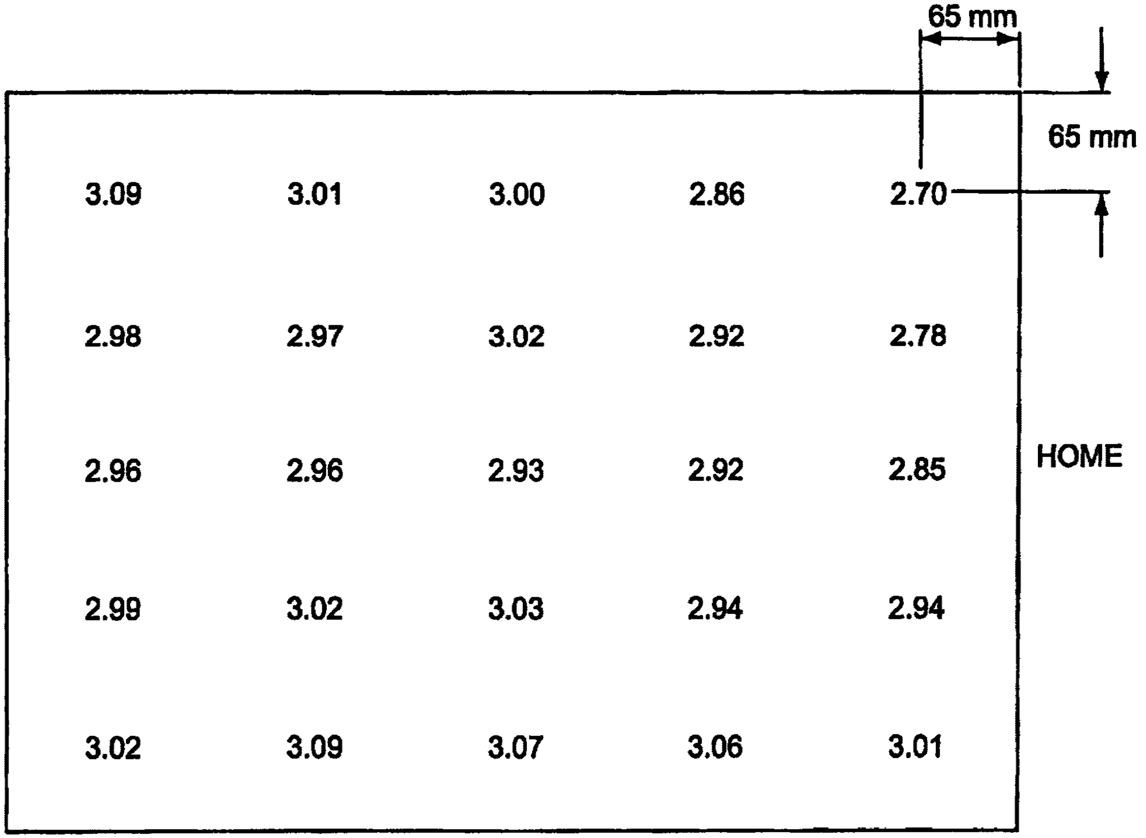


FIG. 15B

SUBSTITUTE SHEET (RULE 26)



3.09	3.01	3.00	2.86	2.70
2.98	2.97	3.02	2.92	2.78
2.96	2.96	2.93	2.92	2.85
2.99	3.02	3.03	2.94	2.94
3.02	3.09	3.07	3.06	3.01

FIG. 16

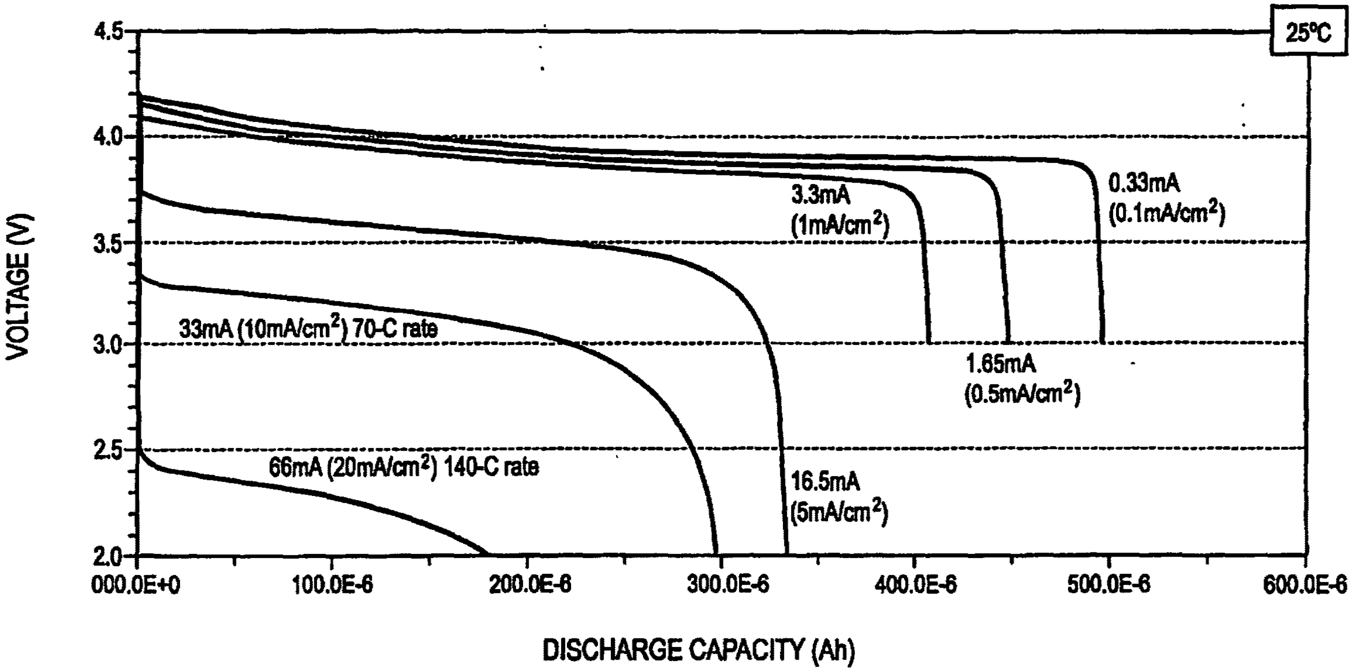

25°C
4.5
4.0
3.5
3.0
2.5
2.0
VOLTAGE (V)
0.33mA
(0.1mA/cm²)
3.3mA
(1mA/cm²)
1.65mA
(0.5mA/cm²)
33mA (10mA/cm²) 70-C rate
66mA (20mA/cm²) 140-C rate
16.5mA
(5mA/cm²)
000.0E+0
100.0E-6
200.0E-6
300.0E-6
400.0E-6
500.0E-6
600.0E-6
DISCHARGE CAPACITY (Ah)

FIG. 17

02-08-07

IFW

OIPE IAP2
FEB 06 2007
PATENT & TRADEMARK OFFICE

PATENT
Customer No. 22,852
Attorney Docket No. 9140.0016-02

IN THE UNITED PATENT AND TRADEMARK OFFICE

In re Application of:)
)
ZHANG, Hongmei et al.) Group Art Unit: 1753
)
Application No.: 11/228,834) Examiner: MCDONALD, Rodney Glenn
)
Filed: September 16, 2005)
) Confirmation No.: 9006
For: BIASED PULSE DC REACTIVE)
SPUTTERING OF OXIDE FILMS)

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

SUPPLEMENTAL PRELIMINARY AMENDMENT

Please amend the above-identified patent application as follows:

Amendments to the Claims are reflected in the listing of claims in this paper beginning on page 2.

Remarks follow the amendment sections of this paper beginning on page 6.

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

1.-14. (Canceled)

15. (Currently amended) A reactor according to the present invention, comprising:

a target area for receiving a target;

a substrate area opposite the target area for receiving a substrate;

a pulsed DC power supply coupled to the target area, the pulsed DC power supply providing alternating negative and positive voltages to the target; ~~and~~

[[a]] an RF bias power supply coupled to the substrate; and

a narrow band-rejection filter that rejects at a frequency of the RF bias power supply coupled between the pulsed DC power supply and the target area.

16. (Previously presented) The reactor of claim 15, wherein the target has a surface area greater than the surface area of the substrate.

17. (Currently amended) The reactor of claim 15, further including a ~~scanning~~ magnet which provides ~~uniform~~ erosion of the target.

18. (Currently amended) The reactor of claim 17, wherein the ~~scanning~~ magnet scans across the target in a first direction and extends in a second direction perpendicular to the first direction.

19. (Currently amended) The reactor of claim 18, wherein the magnet extends beyond the target in the second direction.

20.-37. (Canceled).

38. (Previously presented) A sputtering apparatus, comprising:

means for providing pulsed DC power to a target; and

means for providing bias power to a substrate.

39. (Previously presented) The apparatus of claim 38, further including means for providing process gas between the target and the substrate.

40. (New) A reactor according to the present invention, comprising:

a target area for receiving a target;

a magnetic field generator supplying a magnetic field to the target;

a substrate area opposite the target area for receiving a substrate;

a pulsed DC power supply coupled to the target to provide alternating positive and negative voltages to the target;

an RF bias power supply coupled to provide an RF bias to the substrate; and

a narrow band rejection filter operating at a frequency of the RF bias power supply coupled between the pulsed DC power supply and the target,

wherein a material is deposited on the substrate by exposure of the substrate to a plasma generated when pulsed DC power from the pulsed DC power supply is applied to the target in the presence of a process gas.

41. (New) The reactor of claim 40, wherein the target is a metallic target.

42. (New) The reactor of claim 40, wherein the process gas includes one or more of a set consisting of Ar, O_2, N_2, NH_3, CO, NO, CO_2, C_2F_6, and halide containing gasses.

43. (New) The reactor of claim 40, wherein the target is a ceramic target.

44. (New) The reactor of claim 40, further including a temperature controller for holding the temperature of the substrate substantially constant.

45. (New) The reactor of claim 40, wherein the target is an alloyed target.

46. (New) The reactor of claim 45 wherein the alloyed target includes one or more rare-earth ions.

47. (New) The reactor of claim 45 wherein the alloyed target includes one or more elements taken from a set consisting of Si, Al, Er, Yb, Zn, Ga, Ge, P, As, Sn, Sb, Pb, Ag, Au, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy Ho, Tm, and Lu.

48. (New) A reactor, comprising:

a pulsed DC power supply;

a narrow band rejection filter coupled to the pulsed DC power supply, wherein an oscillating negative and positive voltage can be supplied to from the pulsed DC power supply to the target;

a substrate mount positioned opposite a target mount that holds the target; and

a process gas system that allows process gas into an area between the substrate mount and the target mount.

REMARKS

Applicant has amended claims 15 and 17-19, and have added new claims 40-48 to further describe the invention. Applicants request that the Examiner examine the amended claims presented.

The new claims and the additional limitations added to the previous claims are well supported in the specification. Claim 15 has been amended to recite that "the pulsed DC power supply providing alternating negative and positive voltages to the target," which is disclosed, for example, in paragraph [0053] of the specification. Claim 15 has also been amended to recite "a narrow band-rejection filter that rejects at a frequency of the RF bias power supply coupled between the pulsed DC power supply and the target area," which is disclosed, for example, in paragraph [0056] of the specification.

New claim 40 recites similar limitations to those disclosed in claim 15. Claim 15 further recites "a magnetic field generator," which is disclosed, for example, in paragraphs [0058]-[0059] of the specification. Claim 41 recites that "the target is a metallic target," which is disclosed, for example, in paragraph [0062]. Claim 42 recites that "the process gas includes one or more of a set . . . ," which is disclosed, for example, in paragraphs [0015] and [0073]. Claim 43 recites that "the target is a ceramic target," which is disclosed, for example, in paragraphs [0062] and [114]. Claim 44 recites "a temperature controller . . . ," which is disclosed, for example, in paragraph [0058]. Claims 45-47 recite that "the target is an alloyed target," which is disclosed, for example, in paragraphs [0062] and [0064]. Claim 48 includes limitations to those previously discussed.

Please grant any extensions of time required to enter this paper and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: February 6, 2007

By:
Gary J. Edwards
Reg. No. 41,008

**EXPRESS MAIL LABEL NO.
EV 955594475 US**

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IAP2
FEB 06 2007
PATENT & TRADEMARK OFFICE

PATENT
Customer No. 22,852
Attorney Docket No. 9140.0016-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
ZHANG, Hongmei et al.	Group Art Unit: 1753
Application No.: 11/228,834	Examiner: MCDONALD, Rodney Glenn
Filed: September 16, 2005	Confirmation No.: 9006
For: BIASED PULSE DC REACTIVE SPUTTERING OF OXIDE FILMS	

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

FOURTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§ 1.56 and 1.97(b), Applicant brings to the attention of the Examiner the documents on the attached listing. This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits for the above-referenced application.

Copies of the listed non-patent literature documents are attached. Copies of the U.S. patent and patent publications are not enclosed.

Applicant respectfully requests that the Examiner consider the listed documents and indicate that they were considered by making appropriate notations on the attached form.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or

constitute "prior art." If the Examiner applies any of the documents as prior art against any claim in the application and Applicant determines that the cited documents do not constitute "prior art" under United States law, Applicant reserves the right to present to the office the relevant facts and law regarding the appropriate status of such documents.

Applicant further reserves the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: February 6, 2007

By:
Gary J. Edwards
Reg. No. 41,008

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IDS Form PTO/SB/08: Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	11/228,834
Filing Date	September 16, 2005
First Named Inventor	ZHANG, Hongmei
Art Unit	1753
Examiner Name	MCDONALD, Rodney Glenn
Attorney Docket Number	9140.0016-02

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Issue or Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-6,154,582	11-28-2000	Bazylenko et al.	
		US-2002/0191916 A1	12-19-2002	Frish et al.	
		US-2005/0175287 A1	08-11-2005	Pan et al.	

Note: Submission of copies of U.S. Patents and published U.S. Patent Applications is not required.

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation[6]
		BELKIND, A. et al., "Pulsed-DC Reactive Sputtering of Dielectrics: Pulsing Parameter Effects," 43rd Annual Technical Conference Proceedings-Denver: 86-90 (April 15-20, 2000).	
		SCHOLL, R., "Power Supplies for Pulsed Plasma Technologies: State-Of-The-Art And Outlook," Advances Energy Industries, Inc., pages 1-8 (1999).	
		SCHOLLI, R., "Power Systems for Reactive Sputtering of Insulating Films," Advances Energy Industries, Inc., pages 1-8 (August 2001).	
		Office Action dated December 1, 2006, in U.S. Application No. 10,291,179 (Attorney Docket No. 9140.0001-00).	
		Office Action dated December 18, 2006, in U.S. Application No. 09/903,081 (Attorney Docket No. 9140.0014-00).	
		Office Action dated December 1, 2006, in U.S. Application No. 11/100,856 (Attorney Docket No. 9140.0015-01).	
		Response dated February 6, 2007, in U.S. Application No. 10/101,863 (Attorney Docket No. 9140.0016-00).	
		Response to Office Action dated December 6, 2006, in Application No. 10/954,182 (Attorney Docket No. 9140.0016-01).	
		Supplemental Preliminary Amendment dated February 6, 2007, in U.S. Application No. 11/191,643 (Attorney Docket No. 9140.0016-04).	
		Response to Office Action dated December 21, 2006, in U.S. Application No. 11/228,805 (Attorney Docket No. 9140.0030-01).	
		Response to Office Action dated November 8, 2006, to the Korean Patent Office in Application No. 10-2005-7016055 (Attorney Docket No. 9140.0030-	

Examiner Signature		Date Considered	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

EXPRESS MAIL LABEL NO.
EV 955594475 US

IDS Form PTO/SB/08: Substitute for form 1449A/PTO **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** *(Use as many sheets as necessary)*				***Complete if Known***	
				Application Number	11/228,834
				Filing Date	September 16, 2005
				First Named Inventor	ZHANG, Hongmei
				Art Unit	1753
				Examiner Name	MCDONALD, Rodney Glenn
Sheet	2	of	2	*Attorney Docket Number*	9140.0016-02

NON PATENT LITERATURE DOCUMENTS			
		00202).	
		Response to Office Action dated January 26, 2007, in U.S. Application No. 10/851,542 (Attorney Docket No. 9140.0033-00).	
		Preliminary Amendment dated July 21, 2006, in U.S. Application No. 11/297,057 (Attorney Docket No. 9140.0042-00).	
		Supplemental Preliminary Amendment, Substitute Specification with Markings, Substitute Specification without Markings, and Replacement Drawing Sheets dated December 6, 2006 in U.S. Application No. 11/297,057 (Attorney Docket No. 9140.0042-00)	
		Continuation application and Preliminary Amendment dated December 13, 2006 (Attorney Docket No. 9140.0042-01).	
		Voluntary Amendment dated August 15, 2006 in TW Appl. No. 94143175 (Attorney Docket No. 9140.0042-00270).	
		PCT International Search Report and Written Opinion for Application No. PCT/US05/44781 dated October 3, 2006 (Attorney Docket No. 9140.0042-00304).	
		Specification dated September 2, 2005, for U.S. Appl. No. 11/218,652 (Attorney Docket No. 9140.0052-00).	

Examiner Signature		Date Considered	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875 Effective December 8, 2004

Application or Docket Number: 11228834

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	150.00		N/A	300.00
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	$250		N/A	$500
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	$100		N/A	$200
TOTAL CLAIMS (37 CFR 1.16(i))	7 minus 20 =	* 0	X$ 25 =		OR	X$50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	* 0	X100 =			X200 =	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			+180=			+360=	
			TOTAL			TOTAL	1000

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

AMENDMENT A	(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
2/6/07	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 16	Minus	** 20	= /	X$ 25 =		OR	X$50 =	
Independent (37 CFR 1.16(h))	* 4	Minus	*** 3	= 1	X100 =		OR	X200 =	200
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					+180=		OR	+360=	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	$200.00

AMENDMENT B	(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X$ 25 =		OR	X$50 =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X100 =		OR	X200 =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					+180=		OR	+360=	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

10-26-07

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OCT 2 5 2007
PATENT & TRADEMARK OFFICE

PATENT
Customer No. 22,852
Attorney Docket No. 10655.0016-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
ZHANG, Hongmei et al.	)	Group Art Unit: 1795
	)	
Application No.: 11/228,834	)	Examiner: MCDONALD, Rodney Glenn
	)	
Filed: September 16, 2005	)	
	)	
For: BIASED PULSE DC REACTIVE SPUTTERING OF OXIDE FILMS	)	Confirmation No.: 9006

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

FIFTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§ 1.56 and 1.97(b), Applicants bring to the attention of the Examiner the listed documents on the attached PTO SB/08 Form. This Supplemental Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits for the above-referenced application.

Copies of the listed foreign and non-patent literature documents are attached. Copies of the U.S. patents and patent publications are not enclosed.

Applicants respectfully request that the Examiner consider the listed documents and indicate that they were considered by making appropriate notations on the attached form.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or constitute "prior art." If the Examiner applies any of the documents as prior art against any claim in the application and Applicants determine that the cited documents do not constitute "prior art" under United States law, Applicants reserve the right to present to the U.S. Patent and Trademark Office the relevant facts and law regarding the appropriate status of such documents.

Applicants further reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to Deposit Account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: October 24, 2007

By:
Gary J. Edwards
Reg. No. 41,008

**EXPRESS MAIL LABEL NO.
EM 100825629 US**

OIPE
OCT 15 2007

IDS Form PTO/SB/08: Substitute for form 1449A/PTO			
INFORMATION DISCLOSURE STATEMENT BY APPLICANT			
(Use as many sheets as necessary)			
Sheet	1	of	2

Complete if Known	
Application Number	11/228,834
Filing Date	September 16, 2005
First Named Inventor	ZHANG, Hongmei
Art Unit	1795
Examiner Name	MCDONALD, Rodney Glenn
Attorney Docket Number	10655.0016-02

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Issue or Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-6,391,166 B1	05-21-2002	Wang	
		US-7,262,131 B2	08-28-2007	Narasimhan et al.	
		US-2001/0034106 A1	10-25-2001	Moise et al.	
		US-2007/0053139 A1	03-08-2007	Zhang et al.	

Note: Submission of copies of U.S. Patents and published U.S. Patent Applications is not required.

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	Translation[6]
		WO 2007/027535 A2	03-08-2007	Symmorphix, Inc.		

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation[6]
		Response to Office Action dated March 1, 2007, in U.S. Application No. 10/291,179 (Attorney Docket No. 9140.0001-00).	
		Office Action dated May 21, 2007, in U.S. Application No. 10/291,179 (Attorney Docket No. 9140.0001-00).	
		Response to Office Action filed March 19, 2007, in U.S. Application No. 09/903,081 (Attorney Docket No. 9140.0014-00).	
		Final Office Action dated April 13, 2007, in U.S. Application No. 09/903,081 (Attorney Docket No. 9140.0014-00).	
		Amendment/RCE filed August 9, 2007, in U.S. Application No. 09/903,081 (Attorney Docket No. 9140.0014-00).	
		Office Action dated September 5, 2007, in U.S. Application No. 09/903,081 (Attorney Docket No. 9140.0014-00).	
		Response to Office Action filed March 1, 2007, in U.S. Application No. 11/100,856 (Attorney Docket No. 9140.0015-01).	
		Final Office Action dated September 7, 2007, in U.S. Application No. 11/100,856 (Attorney Docket No. 9140.0015-01).	
		Response to Office Action filed February 6, 2007, in U.S. Application No. 10/101,863 (Attorney Docket No. 9140.0016-00).	
		Final Office Action dated May 2, 2007, in U.S. Application No. 10/101,863 (Attorney Docket No. 9140.0016-00).	
		Response to Final Office Action filed October 2, 2007, in U.S. Application No. 10/101,863 (Attorney Docket No. 9140.0016-00).	
		Office Action dated March 14, 2007, in U.S. Application No. 10/954,182 (Attorney Docket No. 9140.0016-01).	

Examiner Signature		Date Considered	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

IDS Form PTO/SB/08: Substitute for form 1449A/PTO **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** *(Use as many sheets as necessary)*				***Complete if Known***	
				Application Number	11/228,834
				Filing Date	September 16, 2005
				First Named Inventor	ZHANG, Hongmei
				Art Unit	1795
				Examiner Name	MCDONALD, Rodney Glenn
Sheet	2	of	2	*Attorney Docket Number*	10655.0016-02

		Response to Office Action filed March 30, 2007, in U.S. Application No. 10/954,182 (Attorney Docket No. 9140.0016-01).	
		Notice of Non-Compliant Amendment dated April 12, 2007, in U.S. Application No. 10/954,182 (Attorney Docket No. 9140.0016-01).	
		Response to Notice of Non-Compliant Amendment filed April 23, 2007, in U.S. Application No. 10/954,182 (Attorney Docket No. 9140.0016-01).	
		Final Office Action dated July 24, 2007, in U.S. Application No. 10/954,182 (Attorney Docket No. 9140.0016-01).	
		Preliminary Amendment filed July 27, 2005, in U.S. Application No. 11/191,643 (Attorney Docket No. 9140.0016-04).	
		Corrected Preliminary Amendment filed September 19, 2005, in U.S. Application No. 11/191,643 (Attorney Docket No. 9140.0016-04).	
		Response to Office Action filed February 20, 2007, in U.S. Application No. 10/650,461 (Attorney Docket No. 9140.0025-00).	
		Office Action dated March 6, 2007, in U.S. Application No. 10/650,461 (Attorney Docket No. 9140.0025-00).	
		Response to Office Action filed July 9, 2007, in U.S. Application No. 10/650,461 (Attorney Docket No. 9140.0025-00).	
		Final Office Action dated October 10, 2007, in U.S. Application No. 10/650,461 (Attorney Docket No. 9140.0025-00).	
		Notice of Allowance dated February 21, 2007, in U.S. Application No. 10/789,953 (Attorney Docket No. 9140.0030-00).	
		Notice of Allowance dated March 26, 2007, in U.S. Application No. 11/228,805 (Attorney Docket No. 9140.0030-01).	
		Corrected Notice of Allowance dated June 7, 2007, in U.S. Application No. 11/228,805 (Attorney Docket No. 9140.0030-01).	
		Supplemental Notice of Allowance dated July 5, 2007, in U.S. Application No. 11/228,805 (Attorney Docket No. 9140.0030-01).	
		Notice of Allowance dated February 22, 2007, in U.S. Application No. 10/851,542 (Attorney Docket No. 9140.0033-00).	
		Supplemental Notice of Allowance dated March 15, 2007, in U.S. Application No. 10/851,542 (Attorney Docket No. 9140.0033-00).	
		Preliminary Amendment filed March 22, 2007, in U.S. Application No. 11/726,972 (Attorney Docket No. 9140.0033-01).	
		Voluntary Amendment filed March 8, 2007, in Taiwan Application No. 93114518 (Attorney Docket No. 9140.0033-270).	
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(71) Applicant *(for all designated States except US)*: **SYMMORPHIX, INC.** [US/US]; 1278 Reamwood Avenue, Sunnyvale, California 94089-2233 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **ZHANG, Hongmei** [US/US]; 1330 Rodney Drive, San Jose, California 95118 (US). **DEMARAY, Richard, E.** [US/US]; 190 Fawn Lane, Portola Valley, California 94028 (US).

(74) Agent: EDWARDS, Gary J.; Finnegan, Henderson, Farabow, Garrett & Dunner LLP, 901 New York Avenue, N.W., Washington, D.C., District Of Columbia 20001-4413 (US).

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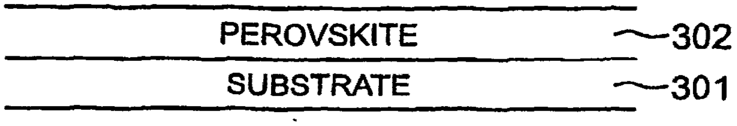
(54) Title: DEPOSITION OF PEROVSKITE AND OTHER COMPOUND CERAMIC FILMS FOR DIELECTRIC APPLICATIONS



(57) Abstract: In accordance with the present invention, deposition of perovskite material, for example barium strontium titanite (BST) film, by a pulsed-dc physical vapor deposition process or by an RF sputtering process is presented. Such a deposition can provide a high deposition rate deposition of a layer of perovskite. Some embodiments of the deposition address the need for high rate deposition of perovskite films, which can be utilized as a dielectric layer in capacitors, other energy storing devices and micro-electronic applications. Embodiments of the process according to the present invention can eliminate the high temperature (>700 °C) anneal step that is conventionally needed to crystallize the BST layer.

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Deposition of Perovskite and Other Compound Ceramic Films for Dielectric Applications

FIELD OF THE INVENTION

[001] The present invention is related to production and application of dielectric thin-films and, in particular, the deposition of perovskites such as Barium Strontium Titanate (BST) films and other ceramic oxides for dielectric applications.

DISCUSSION OF RELATED ART

[002] Perovskite films, for example Barium Strontium Titanate (BST) films, are one of the attractive materials to use in capacitors for high density device applications because of its relatively high dielectric constant, low leakage current density, high dielectric breakdown strength, and ferroelectric perovskite phase that does not exhibit fatigue. However, electric properties of the perovskite films are greatly dependent on the deposition process, the substrate, the post-processing, and the related film structure. For all of the potential, thin film perovskites have rarely been utilized in manufacture primarily because of difficulties in controlling physical and chemical properties of the crystalline and amorphous phases of perovskite thin-film materials and their interactions with metallic and conductive electrodes.

[003] Solid-state thin-film devices are typically formed by stacking thin films of metal and dielectric on a substrate. The thin films typically include two metallic electrodes with a dielectric layer in between. The thin films can be deposited utilizing a number of deposition processes, including sputtering, electroplating, chemical vapor deposition, sol gel, or oxidation. Substrates suitable for these applications have conventionally been high temperature materials capable of withstanding at least one high temperature anneal process to at least 650-750 °C so as to crystallize the perovskite dielectric film in order to increase its

dielectric constant. Such a substrate can be any suitable material with appropriate structural and material properties, for example a semiconductor wafer, refractory metallic sheet (e.g., titanium, zirconium, or stainless steel), ceramic such as alumina, or other material capable of withstanding subsequent high temperature processing.

[004] However, conventional materials and production processes can limit the types of materials that can be used in device manufacture. Typically, the dielectric material is deposited in amorphous form and then the material is heated in an anneal process to form the crystalline material. Conventional formation of perovskite layers, for example, require an anneal at or above 650°C to transform the deposited amorphous film to a crystalline form. Such a high temperature anneal, however, severely limits the materials that can be utilized as the substrate, and often requires the use of expensive noble metals such as platinum to protect the substrate from reaction with the electrode material. Such high heat-treat temperatures are incompatible with standard semiconductor or MEM device processing, and limit the choice of substrate materials on which the layers can be formed, increasing the cost, and decreasing the yield of such devices formed with the layers.

[005] Therefore, there is a need for a low temperature process for depositing crystalline material, for example perovskite material and other ceramic oxides, onto a substrate.

SUMMARY

[006] In accordance with the present invention, deposition of layers in a pulsed-DC physical vapor deposition process from a conductive ceramic target is presented. In some embodiments, the deposition can provide a low-temperature, high deposition-rate deposition of a dense amorphous layer of BST from a conductive BST target, which can be annealed at much lower temperature to yield crystalline BST. Some embodiments of the deposition address the need for low temperature, high rate deposition of perovskite films, for example

BST films, which can be utilized as the dielectric layer in high specific capacitance devices as, for example, de-coupling capacitors, energy storage devices, voltage tunable capacitors, or other micro-electronic devices.

[007] A method of depositing a perovskite or ceramic oxide layer according to some embodiments of the present invention includes placing a substrate in a reactor; flowing a gaseous mixture, for example argon and oxygen, through the reactor; and applying pulsed-DC power to a target formed of conductive perovskite or ceramic oxide material, such as BST, positioned opposite the substrate.

[008] In some embodiments the perovskite layer can be formed utilizing radio frequency (RF) sputtering. The perovskite is deposited by RF sputtering of a wide area target in the presence of a sputtering gas under a condition of uniform target erosion. The substrate is positioned opposite a planar target formed of perovskite, for example BST, the area of the target being larger than the area of the substrate. A central area of the target of the same size as the substrate and overlying the substrate is exposed to a uniform plasma condition, which provides a condition of uniform target erosion. A uniform plasma condition can be created without magnetic enhancement, termed diode sputtering, or by providing a time-averaged uniform magnetic field by scanning a magnet across the target in a plane parallel to the plane of the target.

[009] A film produced utilizing a pulsed dc, bias PVD process with a conductive ceramic target can be deposited at much higher rates than an insulating ceramic process, which requires an RF sputtering process. Further, deposition occurs with much less oxygen present in the gas flow to provide a fully oxidized film as opposed to a metallic target. The resulting film is much higher density than the low rate films. The films can be stoichiometric, uniform, highly dense, with low sintering temperatures and resulting high dielectric properties.

[010] In some embodiments, the substrate is preheated. The substrate can be heated to a temperature of about 400°C or below during deposition for low temperature perovskite deposition, or to higher temperatures for perovskite deposition on substrates capable of withstanding such temperature regime. Substrates suitable for low temperature perovskite deposition include glass, plastic, metal foil, stainless steel, and copper. A perovskite layer of thickness up to several microns thick can be deposited, although layers of any thickness can be formed.

[011] In some embodiments the perovskite layer formed on the substrate is later annealed. The anneal temperature can be as low as 400°C for low temperature anneal, and higher for perovskite deposition on substrates capable of withstanding such higher temperature regime. In some embodiments the perovskite target can be doped with transition metal dopants, for example manganese, transition elements, lanthanides (including the rare earth ions) and/or amphoteric elements.

[012] In some embodiments, a stacked capacitor structure can be formed. The stacked capacitor structure includes one or more capacitor stacks deposited on a thin substrate, wherein each capacitor stack includes: a bottom electrode layer, a perovskite, for example BST, dielectric layer deposited over the bottom electrode layer; and a top electrode layer deposited over the dielectric layer. A top conducting layer can be deposited over the capacitor stacks.

[013] In some embodiments, a capacitor structure can be formed in a cluster tool. An exemplary method of producing a capacitor in a cluster tool includes loading a substrate into the cluster tool; depositing an electrode layer over the substrate in a first chamber of the cluster tool; depositing a perovskite dielectric layer over the electrode layer in a second chamber of the cluster tool; depositing a second electrode layer over the dielectric layer in a

third chamber. In some embodiments the first and the second electrode layers can be deposited in the same chamber.

[014] A fixture for holding a thin substrate can include a top portion; and a bottom portion, wherein the thin substrate is held when the top portion is attached to the bottom portion.

[015] In some embodiments, the ceramic layer can be deposited on a substrate coated with iridium or other refractory conductive material to provide a low temperature anneal processed capacitive structure.

[016] These and other embodiments of the invention are further discussed below with reference to the following figures. It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention, as claimed. Further, specific explanations or theories regarding the deposition or performance of materials according to the present invention are presented for explanation only and are not to be considered limiting with respect to the scope of the present disclosure or the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[017] Figures 1A and 1B illustrate a pulsed-DC biased reactive deposition apparatus that can be utilized in the methods of depositing according to the present invention.

[018] Figure 1C illustrates an RF sputtering deposition apparatus.

[019] Figure 2 shows an example of a target that can be utilized in the reactor illustrated in Figures 1A, 1B, and 1C.

[020] Figures 3A and 3B illustrate a thin-film capacitor design according to some embodiments of the present invention.

[021] Figures 4A, 4B, 4C, and 4D illustrate a thin substrate mount and mask arrangement that can be utilized in the deposition of dielectric perovskite layers, for example BST films, deposited according to some embodiments of the present invention.

[022] Figure 5 illustrates a cluster tool that can be utilized to form batteries with dielectric perovskite layers deposited according to some embodiments of the present invention.

[023] Figure 6 illustrates an example of stacked capacitor structure with dielectric perovskite layers deposited according to some embodiments of the present invention.

[024] In the figures, elements having the same designation have the same or similar functions.

DETAILED DESCRIPTION

[025] In accordance with embodiments of the present invention, dielectric perovskite films or other ceramic oxide films are deposited on a substrate by a pulsed-DC physical vapor deposition (PVD) process utilizing a conductive ceramic target. In some embodiments, the film can be deposited by RF sputtering.

[026] In some embodiments, a dielectric perovskite layer, for example BST material, is deposited directly on the substrate with only low temperature anneal, eliminating the need of a subsequent high temperature anneal to crystallize the film. Removing the high temperature anneal allows for formation of capacitor structures on light-weight, low temperature, and low cost substrates such as copper foil and plastic sheet, reducing both the weight and the cost of capacitors while maintaining the high dielectric constant of the perovskite, for example BST, high-density dielectric film.

[027] Deposition of materials by pulsed-DC, RF biased reactive ion deposition is described in U.S. Patent Application Serial No. 10/101,863, entitled "Biased Pulse DC Reactive Sputtering of Oxide Films," to Hongmei Zhang, et al., filed on March 16, 2002.

Preparation of targets is described in U.S. Patent Application Serial No. 10/101,341, entitled "Rare-Earth Pre-Alloyed PVD Targets for Dielectric Planar Applications," to Vassiliki Milonopoulou, et al., filed on March 16, 2002. U.S. Patent Application Serial No. 10/101,863 and U.S. Patent Application Serial No. 10/101,341 are each assigned to the same assignee as is the present disclosure and each is incorporated herein in their entirety. Deposition of oxide materials by RF sputtering has also been described in U.S. Patent No. 6,506,289, which is also herein incorporated by reference in its entirety. Transparent oxide films can be deposited utilizing processes similar to those specifically described in U.S. Patent No. 6,506,289 and U.S. Application Serial No. 10/101,863.

[028] Figure 1A shows a schematic of a reactor apparatus 10 for sputtering material from a target 12 according to the present invention. In some embodiments, apparatus 10 may, for example, be adapted from an AKT-1600 PVD (400 X 500 mm substrate size) system from Applied Komatsu or an AKT-4300 (600 X 720 mm substrate size) system from Applied Komatsu, Santa Clara, CA. The AKT-1600 reactor, for example, has three deposition chambers connected by a vacuum transport chamber. These AKT reactors can be modified such that pulsed DC power is supplied to the target and RF power is supplied to the substrate during deposition of a material film.

[029] Apparatus 10 includes target 12, which is electrically coupled through a filter 15 to a pulsed DC power supply 14. In some embodiments, target 12 is a wide area sputter source target, which provides material to be deposited on a substrate 16. Substrate 16 is positioned parallel to and opposite target 12. Target 12 functions as a cathode when power is applied to it from the pulsed DC power supply 14 and is equivalently termed a cathode. Application of power to target 12 creates a plasma 53. Substrate 16 is capacitively coupled to an electrode 17 through an insulator 54. Electrode 17 can be coupled to an RF power supply 18. A magnet 20 is scanned across the top of target 12.

[030] For pulsed reactive DC magnetron sputtering, as performed by apparatus 10, the polarity of the power supplied to target 12 by power supply 14 oscillates between negative and positive potentials. During the positive period, the insulating layer on the surface of target 12 is discharged. To obtain arc free deposition, the pulsing frequency exceeds a critical frequency that can depend on target material, cathode current and reverse time. High quality films can be made using reactive pulse DC magnetron sputtering as shown in apparatus 10.

[031] Pulsed DC power supply 14 can be any pulsed DC power supply, for example an AE Pinnacle plus 10K by Advanced Energy, Inc. With this DC power supply, up to 10 kW of pulsed DC power can be supplied at a frequency of between 0 and 350 kHz. The reverse voltage can be 10% of the negative target voltage. Utilization of other power supplies can lead to different power characteristics, frequency characteristics and reverse voltage percentages. The reverse time on this embodiment of power supply 14 can be adjusted between 0 and 5 μs.

[032] Filter 15 prevents the RF bias power from power supply 18 from coupling into pulsed DC power supply 14. In some embodiments, power supply 18 can be a 2 MHz RF power supply, for example a Nova-25 power supply made by ENI, Colorado Springs, Co.

[033] In some embodiments, filter 15 can be a 2 MHz sinusoidal band rejection filter. In some embodiments, the band width of the filter can be approximately 100 kHz. Filter 15, therefore, prevents the 2 MHz power from the bias to substrate 16 from damaging power supply 14 while allowing the full bandwidth of the pulsed DC power supply to pass filter 15.

[034] Pulsed DC deposited films are not fully dense and may have columnar structures. Columnar structures can be detrimental to thin film applications such as barrier films and dielectric films, where high density is important, due to the boundaries between the

columns. The columns act to lower the dielectric strength of the material, but may provide diffusion paths for transport or diffusion of electrical current, ionic current, gas, or other chemical agents such as water.

[035] In the AKT-1600 based system, for example, target 12 can have an active size of about 675.70 X 582.48 by 4 mm in order to deposit films on substrate 16 that have dimension about 400 X 500 mm. The temperature of substrate 16 can be adjusted to between –50 °C and 500 °C. The distance between target 12 and substrate 16 can be between about 3 and about 9 cm. Process gas can be inserted into the chamber of apparatus 10 at a rate up to about 200 sccm while the pressure in the chamber of apparatus 10 can be held at between about .7 and 6 milliTorr. Magnet 20 provides a magnetic field of strength between about 400 and about 600 Gauss directed in the plane of target 12 and is moved across target 12 at a rate of less than about 20-30 sec/scan. In some embodiments utilizing the AKT 1600 reactor, magnet 20 can be a race-track shaped magnet with dimensions about 150 mm by 600 mm.

[036] In some embodiments of the present invention a perovskite layer is deposited by RF sputtering with a wide area target and a condition of uniform target erosion. An example apparatus 30 for RF sputtering is illustrated schematically in FIG. 1C. Apparatus 30 includes an RF power supply 60 coupled to wide area sputter source target 12 which provides material to be deposited on substrate 16. Substrate 16 is positioned parallel to and opposite target 12. Target 12 functions as a cathode when RF power is applied to it and is equivalently termed the cathode. In the present disclosure, target 12 can be formed from a perovskite material, for example BST, for deposition of dielectric perovskite film. Substrate 16 is a solid, smooth surface. Substrate 16 typically is supported on a holder or carrier sheet 17 that may be larger than substrate 16.

[037] In some embodiments, a feature of the RF sputtering method is that the area of wide area target 12 is greater than the area on the carrier sheet on which physically and

chemically uniform deposition is accomplished. Secondly, a central region on target 12, overlying the substrate 16, can be provided with a very uniform condition of sputter erosion of the target material. Uniform target erosion is a consequence of a uniform plasma condition. In the following discussion, all mention of uniform condition of target erosion is taken to be equivalent to uniform plasma condition. Uniform target erosion is evidenced by the persistence of film uniformity throughout an extended target life. A uniform deposited film is defined as a film having a nonuniformity in thickness, when measured at representative points on the entire surface of a substrate wafer, of less than about 5%. Thickness nonuniformity is defined, by convention, as the difference between the minimum and maximum thickness divided by twice the average thickness. If films deposited from a target from which more than about 20% of the weight of the target has been removed under constant process conditions continue to exhibit thickness uniformity, then the sputtering process is judged to be in a condition of uniform target erosion for all films deposited during the target life.

[038] Thus, a uniform plasma condition can be created in the region between the target and the substrate overlying the substrate. The region of uniform plasma condition is indicated in the exploded view of FIG. 1B. A plasma is created in the region denoted 51, which extends under the entire target 12. The central region of the target 52 experiences the condition of uniform sputter erosion. As discussed further below, a layer deposited on a substrate placed anywhere below central region 52 will have uniform film thickness.

[039] In addition, the region in which deposition provides uniform film thickness is larger than the area in which deposition provides a film with uniform physical or optical properties such as chemical composition or index of refraction. In the present invention the target can be planar or approximately planar for the formation of a film on a planar substrate which is to be coated with the material of the target. In practice, planarity of the target means

that all portions of the target surface in region 52 are within a few millimeters of an ideal planar surface, typically within 0.5 mm.

[040] Figure 2 illustrates an example of target 12. A film deposited on a substrate positioned on carrier sheet 17 directly opposed to region 52 of target 12 has good thickness uniformity. Region 52 is the region shown in Figure 1B that is exposed to a uniform plasma condition. In some implementations, carrier 17 can be coextensive with region 52. Region 24 shown in Figure 2 indicates the area below which both physically and chemically uniform deposition can be achieved, for example where physical and chemical uniformity provide refractive index uniformity. Figure 2 indicates region 52 of target 12 that provides thickness uniformity, which is, in general, larger than region 24 of target 12 providing thickness and chemical uniformity to the deposited film. In optimized processes, however, regions 52 and 24 may be coextensive.

[041] In some embodiments, magnet 20 extends beyond area 52 in one direction, for example the Y direction in Figure 2, so that scanning is necessary in only one direction, for example the X direction, to provide a time averaged uniform magnetic field. As shown in Figures 1A and 1B, magnet 20 can be scanned over the entire extent of target 12, which is larger than region 52 of uniform sputter erosion. Magnet 20 is moved in a plane parallel to the plane of target 12.

[042] The combination of a uniform target 12 with a target area 52 larger than the area of substrate 16 can provide films of highly uniform thickness. Further, the material properties of the film deposited can be highly uniform. The conditions of sputtering at the target surface, such as the uniformity of erosion, the average temperature of the plasma at the target surface and the equilibration of the target surface with the gas phase ambient of the process are uniform over a region which is greater than or equal to the region to be coated with a uniform film thickness. In addition, the region of uniform film thickness is greater

than or equal to the region of the film which is to have highly uniform optical properties such as index of refraction, density, transmission, or absorption.

[043] In the present disclosure, target 12 can be formed from perovskite material, such as BST, for deposition of dielectric perovskite film. In some embodiments of the present invention the perovskite target is doped with transition metal dopants, for example Manganese, transition elements, lanthanides (including the rare earth ions) and/or amphotaric elements. In some embodiments of the present invention the percentage of the dopant in the perovskite target is from 0.1 to several percent.

[044] In some embodiments of the invention, material tiles are formed. These tiles can be mounted on a backing plate to form a target for apparatus 10. A wide area sputter cathode target can be formed from a close packed array of smaller tiles. Target 12, therefore, may include any number of tiles, for example between 2 and 20 individual tiles. Tiles can be finished to a size so as to provide a margin of non-contact, tile to tile, less than about 0.010" to about 0.020" or less than half a millimeter so as to eliminate plasma processes that may occur between adjacent ones of tiles 30. The distance between tiles of target 12 and the dark space anode or ground shield 19 in Figure 1B can be somewhat larger so as to provide non contact assembly or to provide for thermal expansion tolerance during process chamber conditioning or operation.

[045] As shown in Figure 1B, a uniform plasma condition can be created in the region between target 12 and substrate 16 in a region overlying substrate 16. A plasma 53 can be created in region 51, which extends under the entire target 12. A central region 52 of target 12 can experience a condition of uniform sputter erosion. As discussed further below, a layer deposited on a substrate placed anywhere below central region 52 can then be uniform in thickness and other properties (i.e., dielectric, optical index, or material concentrations). In addition, in region 52 the deposition provides uniformity of deposited film that can be larger

than the area in which the deposition provides a film with uniform physical or optical properties such as chemical composition or index of refraction. In some embodiments, target 12 is substantially planar in order to provide uniformity in the film deposited on substrate 16. In practice, planarity of target 12 can mean that all portions of the target surface in region 52 are within a few millimeters of a planar surface, and can be typically within 0.5 mm of a planar surface.

[046] Reactive gases that provide a constant supply of oxygen to keep the target surface oxidized can be provided to expand the process window. Some examples of the gases that can be utilized for controlling surface oxidation are O_2, water vapor, hydrogen, N_2O, fluorine, helium, and cesium. Additionally, a feedback control system can be incorporated to control the oxygen partial pressure in the reactive chamber. Therefore, a wide range of oxygen flow rates can be controlled to keep a steady oxygen partial pressure in the resulting plasma. Other types of control systems such as target voltage control and optical plasma emission control systems can also be utilized to control the surface oxidation of the target. In some embodiments, power to target 12 can be controlled in a feedback loop at supply 14. Further, oxygen partial pressure controller 20 can control either oxygen or argon partial pressures in plasma 53. In some embodiments of the present invention, oxygen flow or partial pressure can be utilized to maintain a constant voltage of discharge from target 12.

[047] Figures 3A and 3B show a capacitor structure with a dielectric perovskite layer deposited according to some embodiments of the present invention. As shown in Figure 3A, a dielectric perovskite layer 302 is deposited on a substrate 301. In some embodiments, the dielectric layer 302 can be patterned in various ways before deposition of a substrate 301. In some embodiments, a first electrode layer 303 can be deposited on the substrate and the dielectric layer 302 is deposited over the first electrode layer. The second electrode layer 304 is then deposited over the dielectric layer 302. In some embodiments of

the invention, the dielectric perovskite layer 302 is crystalline and has sufficiently high dielectric constant without the necessity of a high temperature anneal. Therefore, substrate 301 can be a silicon wafer, titanium metal, alumina, or other conventional high temperature substrate, but may also be a low temperature material such as plastic, glass, or other material that may be susceptible to damage from the high temperature anneal. This feature can have the great advantage of decreasing the expense and weight of capacitor structures formed by the present invention. The low temperature deposition of perovskite material allows for successive depositions of perovskite and electrode layers, one upon another. Such a process would have the advantage that successive layers of capacitor structure would be obtained in a stacked condition without the inclusion of a substrate layer. The stacked layered capacitor would provide higher capacitance and higher energy storage than single layer devices with a smaller surface area. Additionally, a capacitor with a lower inductance can be obtained.

[048] In accordance with the present invention, perovskite films can be deposited on substrate 302 with a pulsed-DC biased PVD system as was described above. In particular, an AKT 1600 PVD system can be modified to provide an RF bias and an Advanced Energy Pinnacle plus 10K pulsed DC power supply can be utilized to provide power to a target. The pulsing frequency of the power supply can vary from about 0 to about 350 KHz. The power output of the power supply is between 0 and about 10 kW.

[049] A target of Barium Strontium Titanate with resistivity in the range of less than about megaohms can be utilized with high rate pulsed-dc sputtering. As discussed above, the target can be mounted on a monolithic backing plate as described in U.S. Provisional Application **{Attorney Docket No. 09140.6013}**, filed on August 26, 2005, which is also herein incorporated by reference in its entirety.

[050] In general, target 12 can be a dielectric material having a resistivity of less than about a megaohm, and therefore can be described as a conducting ceramic target. Target

12, which is formed of a dielectric perovskite material that may not be inherently conducting, is made conducting by formulation so as to contain an excess of metallic composition or by addition of a dopant that provides sufficient conductivity. Examples of suitable dopants include boron, antimony, arsenic, phosphorous, or other dopants. In the example of a BST target, the sintering process can be conducted in the presence of a reducing ambient to achieve a sufficiently conductive target material. Utilization of a conducting ceramic target material can be sputtered at high rates utilizing reactive pulsed-DC techniques so as to form dense stoichiometric dielectric films.

[051] Gas flows containing Oxygen and Argon can be utilized. In some embodiments, the Oxygen to Argon ratio ranges from 0 to about 50% with a total gas flow of between about 60 to about 80 sccm. The pulsing frequency ranges from about 200 kHz to about 350 kHz during deposition. RF bias can also be applied to the substrate. In many trials, the deposition rates varied from about 2 Angstrom/(kW sec) to about 1 Angstrom/(kW sec) depending on the O_2/Ar ratio as well as substrate bias.

[052] Figure 3A illustrates a layer of perovskite material 302 deposited on a thin substrate 301 according to some embodiments of the present invention. Substrate 301 can be formed of a thin metallic sheet (e.g., copper, titanium, stainless steel, or other suitable thin metallic sheet), can be formed of a high temperature plastic material, or may be formed of a ceramic, glass, or polymer material.

[053] Depositing materials on a thin substrate involves holding and positioning the substrate during deposition. Figures 4A, 4B, 4C, and 4D illustrate a reusable fixture 400 for holding a thin film substrate. As shown in Figure 4A, reusable fixture 400 includes a top portion 401 and a bottom portion 402 that are fastened together to secure the substrate. Thin substrate 301 is positioned between top portion 401 and bottom portion 402. As shown in Figure 7B, top portion 701 and bottom portion 702 are such that substrate 301 is brought into

a planar condition and subsequently clamped as top portion 401 is closed into bottom portion 402. Substrate 301 can be easily held by fixture 400 so that substrate 301 can be handled and positioned. In some embodiments, the corners of substrate 301, areas 403, are removed so that substrate 301 is more easily stretched by avoiding "wrap-around" corner clamping effects when top portion 401 is closed into bottom portion 402.

[054] As shown in Figure 4C, a mask 412 can be attached to fixture 400. In some embodiments, fixture 400 includes guides in order to align fixture 400 with respect to mask 412. In some embodiments, mask 412 may be attached to fixture 400 and travel with fixture 400. Mask 412 can be positioned at any desired height above substrate 301 in fixture 400. Therefore, mask 412 can function as either a contact or proximity mask. In some embodiments, mask 412 is formed of another thin substrate mounted in a fixture similar to fixture 400.

[055] As shown in Figure 4C and 4D, fixture 400 and mask 412 can be positioned relative to mount 410. Mount 410, for example, can be a susceptor, mount, or an electrostatic chuck of a processing chamber such as that shown in Figures 1A and 1B. Fixture 400 and mask 412 can have features that allow for ready alignment with respect to each other and with respect to mount 410. In some embodiments, mask 412 is resident in the processing chamber and aligned with fixture 400 during positioning of fixture 400 on mount 410, as shown in Figure 4D.

[056] Utilizing fixture 400 as shown in Figures 4A, 4B, 4C, and 4D allows processing of a thin film substrate in a processing chamber. In some embodiments, thin film substrates can be about 1 μm or more. Further, thin film substrate 301, once mounted within fixture 400, can be handled and moved from process chamber to process chamber. Therefore, a multiprocessor chamber system can be utilized to form stacks of layers,

including one or more layers of perovskite film deposited according to embodiments of the present invention.

[057] Figure 5 illustrates a cluster tool 500 for processing thin film substrates. Cluster tool 500 can, for example, include load lock 502 and load lock 503, through which mounted thin film substrate 301 is loaded and a resultant device is removed from cluster tool 500. Chambers 504, 505, 506, 507, and 508 are processing chambers for depositions of materials, heat treatments, etching, or other processes. One or more of chambers 504, 505, 506, 507, and 508 can be a pulsed-DC or RF PVD chamber such as discussed above with respect to Figures 1A, 1B, and 1C and within which a dielectric perovskite film may be deposited according to embodiments of the present invention.

[058] Processing chambers 504, 505, 506, 507, and 508 as well as load locks 502 and 503 are coupled by transfer chamber 501. Transfer chamber 501 includes substrate transfer robotics to shuttle individual wafers between processing chambers 504, 505, 506, 507, and 508 and load locks 502 and 503.

[059] In production of a thin-film capacitor, substrates are loaded into load lock 503. An electrode layer can be deposited in chamber 504, followed by a perovskite deposition performed in chamber 505. The substrate can then be removed through load lock 503 for an in-air heat treatment external to cluster tool 500. The treated wafer can then be reloaded into cluster tool 500 through load lock 502. The wafer can then again be removed from cluster tool 500 for deposition of a second electrode layer, or sometimes chamber 506 can be adapted to deposition of the second electrode layer. The process can be repeated to form a capacitor stack. The finished capacitor structure is then off-loaded from cluster tool 500 in load lock 502. Wafers are shuttled from chamber to chamber by robotics in transfer chamber 501.

[060] A capacitor structure produced according to the present invention could utilize thin film substrates loaded in a fixture such as fixture 400. Fixture 400 is then loaded into

load lock 503. Chamber 504 may still include deposition of the electrode layer. Chamber 505 then includes deposition of a perovskite layer according to embodiments of the present invention. A second electrode layer can then be deposited in chamber 506. In this process, only low temperature anneal is utilized to increase crystallinity and the dielectric constant of the perovskite layer.

[061] Another advantage of a thin film capacitor process is the ability to stack capacitor structures. In other words, substrates loaded into cluster tool 500 may traverse process chambers 504, 505, 506, 507, and 508 multiple times in order to produce multiply stacked capacitor structures. Figures 6A and 6B illustrate such structures.

[062] Figure 6A illustrates a parallel coupled stacking. As shown in Figure 6A, a substrate 301, which for example can be a high temperature plastic substrate, such as polyimide, is loaded into load lock 503. Electrode layer 303, for example, can be deposited in chamber 504. A dielectric perovskite layer 302 is then deposited on electrode layer 303. Perovskite layer 302 can be about 0.1 to 1 μm and can be deposited in chamber 505 according to embodiments of the present invention.. The wafer can then be moved to chamber 506 where the next electrode layer 304 of thickness of about 0.1 μm or more is deposited. A second capacitor stack can then be deposited over the first capacitor stack formed by first electrode layer 303, perovskite layer 302, and second electrode layer 304. This capacitor stack includes second perovskite layer 305 and third electrode layer 306. In some embodiments, further stacks can be formed. In some embodiments, metal layers 303, 304, and 306 differ in the mask utilized in deposition so that tabs are formed for electrical coupling of layers.

[063] As discussed above, any number of individual capacitor stacks can be formed such that parallel capacitor formations are formed. Such a parallel arrangement of capacitor

stacking structure can be formed of alternating layers of electrode and perovskite dielectric layers and can have any number of dielectric layers.

[064] To form the structures shown in Figure 6, substrates are rotated again through the chambers of cluster tool 500 in order to deposit the multiple sets of capacitors. In general, a stack of any number of capacitors can be deposited in this fashion.

[065] Tables I and II illustrate some examples depositions of perovskite material, for example BST, according to the present invention. In these examples, the BST film is deposited using an AKT-1600 PVD (400 X 500 mm substrate size) system from Applied Komatsu. The power supply is an ENI 13.56 MHz RF power supply with a ENI matchbox. The target material is BST with resistivity in the range of kΩs or less. The target material can, for example, be sintered. Silicon wafers are used for initial experiments. 0.1-1 microns of BST films are deposited on Si wafers with various bottom electrode materials such as: n++ Si, Ir, Pt, IrO_2 and also Ti_4O_7, Ti_3O_5, Nb, Os. The Oxygen to Argon ratio ranges from 0 to 50%. Process pressure ranges from 3-10 mT. RF bias is applied to substrates for some of the examples. The dielectric constant of as deposited film range from 13 to 123 and increases after post-deposition anneal to more than 1000.

[066] One skilled in the art will recognize variations and modifications of the examples specifically discussed in this disclosure. These variations and modifications are intended to be within the scope and spirit of this disclosure. As such, the scope is limited only by the following claims.

TABLE 1

Example #	Film Thickness (nm)	Target Power (W)r	Bias Power (W)	Ar/O_2 Ratio	Vbd	Ebd	C (PF)	Dielectric Constant
BST 2	3679	1500	100	50/50	157	4.267464	167	13.35
BST 3	3736	1500	100	50/50	150	4.014989	168	13.64
BST3-N++ 550c	3736	1500	100		40	1.070664	1670	135.57
BST-Pt-1	2282	1500	100	50/25	47	2.059597	299.5	14.85
BST Pt-1 550C	2282	1500	100		16	0.701139	5722	283.74
BST-n++-4	2282	1500	100	50/25	120	5.258545	274	13.59
BST-n++550c	2282	1500	100		30	1.314636	1970	97.69
BST-IrO2-1	2310	1500	100	50/25	100	4.329004	296.2	14.87
BST-IrO2-1 750C	2310			50/25	2.4	0.103896	17700	888.46
BST-Pt-2	2310	1500	100	50/25	100	4.329004	319	16.01
BST-Pt-2 650C	2310				9.4	0.406926	9750	489.41
BST-Pt-3	2199	1500	100	75/25	7	0.318327	2580	123.28
BST-Pt-3 550	2199	1500	100	75/25	11.2	0.509322	10740	513.20
BST IrO2-2	2199	1500	100	75/25	16.7	0.759436	378	18.06
BST IrO2-2 550	2199	1500	100	75/25	1.4	0.063665	10400	496.95
BST IrO2-2 650	2199	1500	100	75/25	6.9	0.313779	11000	525.62
BST IrO2-2 750	2199			75/25	1.4	0.063665	21950	1048.85
BST Pt 1 step	2918	2000	0	50/50			1239	78.56
BST Ir 1 step	2918	2000	0	50/50			1180	74.82
BST IrO2 1 step	2918	2000	0	50/50			567	35.95
BST Pt 2 steps	1689	2000	0	100/0-50/50			1220	44.78
BST Ir 2 steps	1689	2000	0	100/0-50/50			1230	45.14
BST IrO2 2 steps	1689	2000	0	100/0-50/50			684	25.10

Table II

Sample#	thickness	target power	bias power	Ar/O2	dep time (sec)	Vbd	Ebd	C(PF)	Dielectric Constant, k	Vbd (V)		C(PF)	Dielectric Constant, k (after 500C° anneal)
ALDOEN++-1	840.4					70	8.329367	380	6.939418				
	840.4							377	6.884633				
ALDOEN++-2	5767.2							60.5	7.581825				
								1200	0				
experiment 109	1000							1200	26.07562				
	840					75	8.928571	405	7.392438				
ebonex,BST (A)	1140	900	100		3600		0		0				
Ir Coated #2	2220	900	0	50/50	5400		0	508	24.50587			16800	810.4302
												5000	
	2220											21530	1038.605
IrO2 Coated #2	2220	900	0	50/50	5400		0	365	17.60756	9	0.405	22000	1061.278
	2220						0					20000	964.7979
												19000	
												9000	
N++(1)	2220	900	0		5400	12	0.540541	290	13.98957	12		2512	121.1786
N++(2)	840	900	100	50/50	5400	10	1.190476	982	17.92438	10		2675	48.8266
N++(3)	can't meas	900	200		5400			377					
N++(4)	1490	900	100	50/25	5400		0	242	7.835289			537	17.38657
Ti4O7 (A)	910	900		50/50			0	3030	59.91525			450	8.898305
	910							2962	58.57062				
	910							2860	56.55367				
Ti4O7 (B)	1490			50/25			0	1988	64.36593			314	10.16645
	1490							2048	66.30856				
Ir # 3	650	900	1000 sec no bias/ 4400sec bias 80W	50/50	5400			very leaky					

Ir #4	870	900	500 sec no bias/ 4900 sec 50w bias	50/50	5400			very leaky					
Ir #5	2000	900	1500sec no bias/5700 sec 50W bias	50/50	7200			very leaky					
IrO2 (Tsub=450c)	2000	900	no bias	50/50	5400	10	0.5	1390	60.40852	10		5972	259.5393
	2000											6021	261.6688
n++ (6)(Tsub=450c)	934	900	75 w bias	50/50	7200	12	1.284797	870	17.65711	12		2857	57.98431
n++ (7) (room)	2541	900	no bias	50/50	5400			219		13	0.512	2210	122.0254
n++(8) (room)	2504	900	75 w bias	50/50	7200			224	12.18809	22	0.879	2218	120.6839
n++ (9) (room)	10000		75 w bias	50/50	28800			58	12.60322	55	0.55	954.7	207.4533
n++ (10) (room)	5000		75w bias	50/50	14400								

WHAT IS CLAIMED IS:

1. A method of depositing a perovskite layer on a substrate, comprising:

placing the substrate into a reactor;

flowing a gaseous mixture through the reactor; and

providing power to a target formed of a perovskite material positioned opposite the substrate.

2. The method of claim 1, wherein providing power to the conducting target includes applying pulsed-DC power to the conducting target.

3. The method of claim 2 further including filtering the pulsed-DC power to protect a pulsed DC power supply from a bias power while allowing passage of the pulsed DC power through the filter.

4. The method of claim 2, further including supplying an RF bias power to the substrate.

5. The method of claim 1, wherein providing power to the conducting target includes applying RF power to the conducting target.

6. The method of claim 1, wherein a perovskite layer is formed on the substrate.

7. The method of claim 6, wherein the perovskite layer is a barium strontium titanite (BST) layer.

8. The method of claim 6, wherein the formed perovskite layer is more than about 0.1 micron thick.

9. The method of claim 6 wherein the formed perovskite layer is less than about 1 micron thick.

10. The method of claim 6, further comprising annealing the perovskite layer formed on the substrate.

11. The method of claim 10 wherein annealing the perovskite layer includes heating the perovskite layer to an anneal temperature of between about 500°C and about 800°C.

12. The method of claim 1, further comprising preheating the substrate before applying power to the conducting target.

13. The method of claim 12, wherein preheating the substrate including heating the substrate to a temperature of about 400 °C for low temperature perovskite deposition.

14. The method of claim 1, wherein the substrate is a low temperature substrate.

15. The method of claim 14, wherein the low temperature substrate is one of a set of substrates including glass, plastic, metal foil, copper, and stainless steel.

16. The method of claim 1 wherein the conducting target is doped with a transition metal dopant, transition element, lanthanide, and/or amphotaric elements.

17. The method of claim 16 wherein the target is doped with Manganese.

18. The method of claim 17 wherein a level of Manganese in the target is at least 0.1%.

19. The method of claim 1, wherein the perovskite target is a conductive target.

20. A capacitor structure, comprising:

a first conducting electrode layer;

a dielectric perovskite layer deposited over the first conducting electrode layer; and

a second conducting electrode layer deposited over the dielectric perovskite layer.

21. The capacitor of claim 20, wherein the first conducting layer is a copper sheet.

22. A stacked capacitor structure, comprising:

one or more capacitor stacks deposited on a substrate, wherein each capacitor stack comprises:

a bottom electrode layer,

a dielectric perovskite layer deposited over the electrode layer, and

a top electrode layer deposited over the one or more capacitor stacks.

23. The stacked capacitor structure of claim 22, wherein the capacitor stacks form a parallel stacked capacitor structure.

24. The stacked capacitor structure of claim 22, wherein the capacitor stacks form a series stacked capacitor structure.

25. A method of producing a capacitor, comprising:

loading a substrate into a cluster tool;

depositing a dielectric perovskite layer over a substrate in a chamber of the cluster tool.

26. The method of claim 25, wherein depositing the dielectric perovskite layer includes depositing perovskite film with a pulsed-DC PVD process.

27. The method of claim 25, wherein depositing the dielectric perovskite layer includes depositing perovskite film with an RF sputtering PVD process.

28. The method of claim 25, wherein depositing the dielectric perovskite layer includes depositing the perovskite material through a mask.

29. The method of claim 25, further including

depositing a bottom electrode layer on the substrate wherein the dielectric perovskite layer is .deposited over the bottom electrode layer.

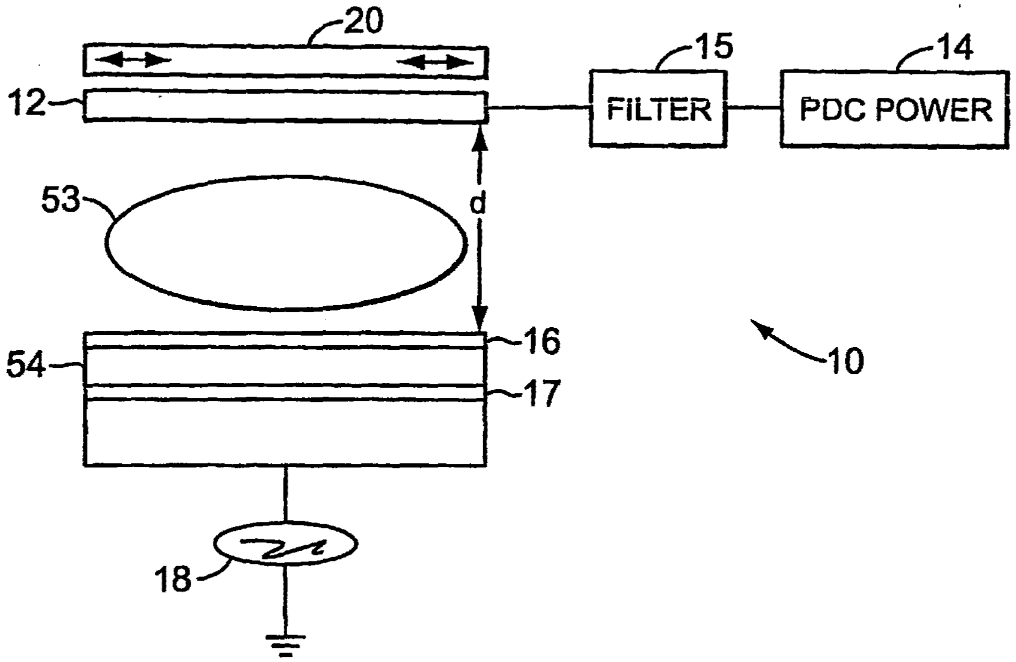
31. The method of claim 25, further including depositing a top electrode layer over the dielectric perovskite layer.

32. A fixture for holding a thin substrate, comprising:

a top portion; and

a bottom portion, wherein

the thin substrate is held when the top portion is attached to the bottom portion.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FILTER
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PDC POWER
53
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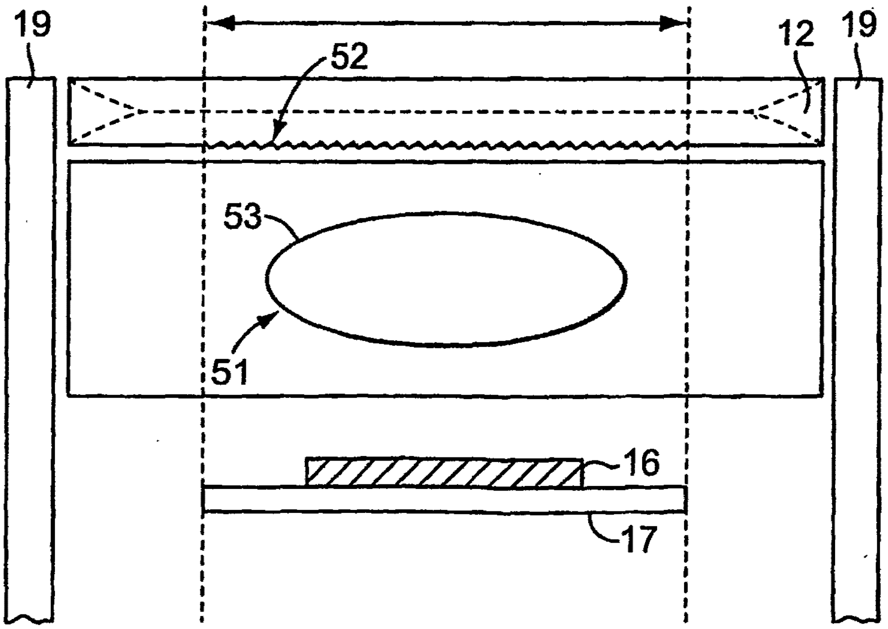
54
17
10
18

FIG. 1A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52
12
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53
51
16
17

FIG. 1B

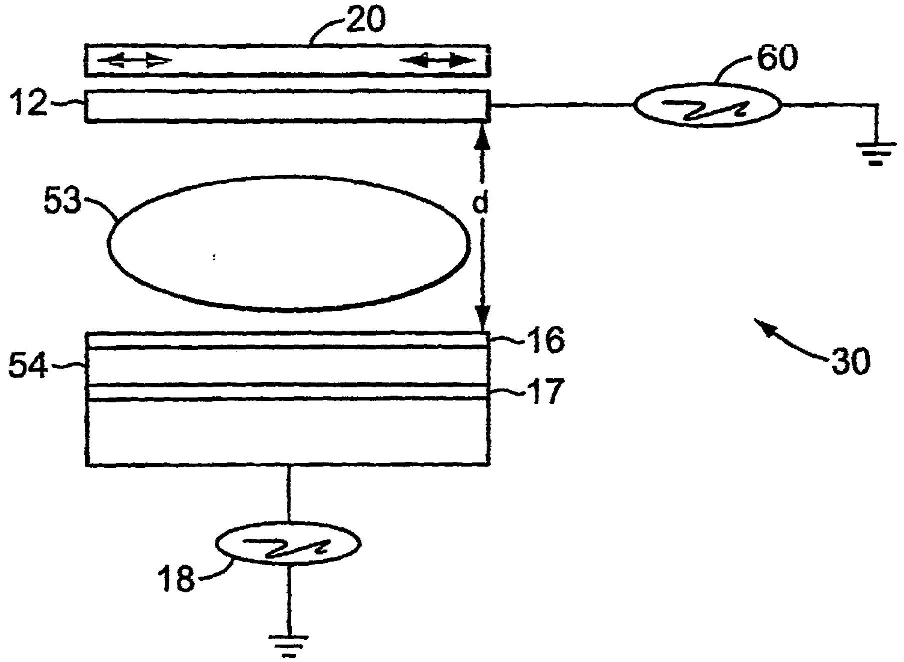

FIG. 1C

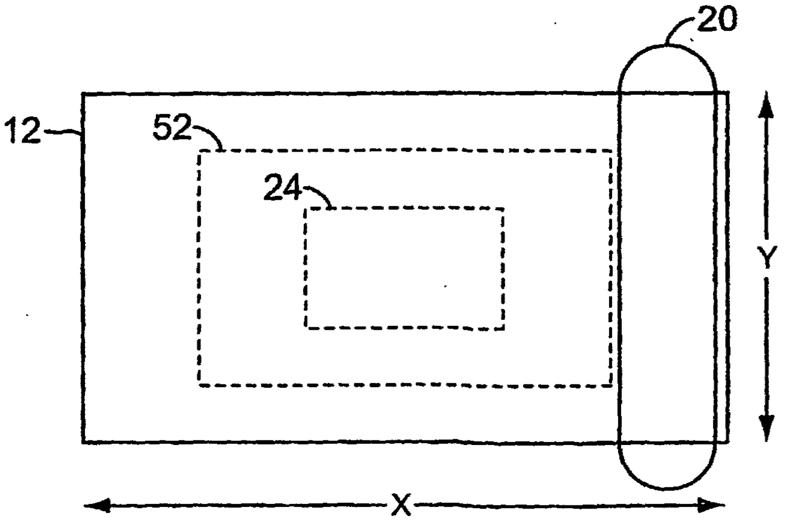

FIG. 2

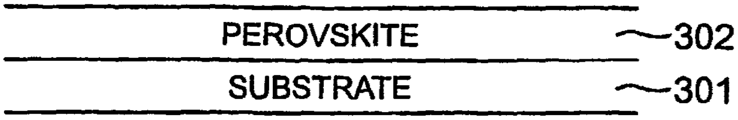

FIG. 3A

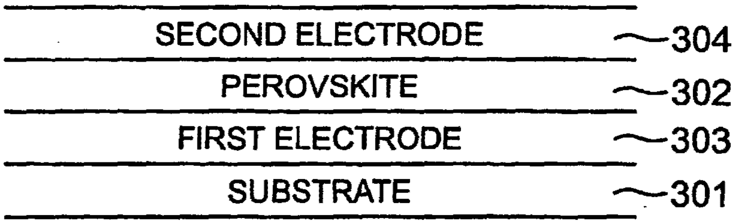

FIG. 3B

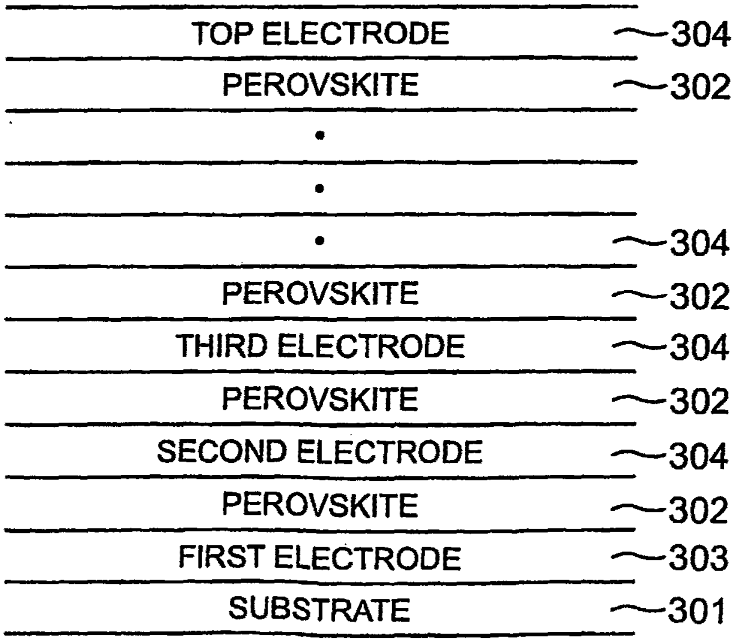

FIG. 6

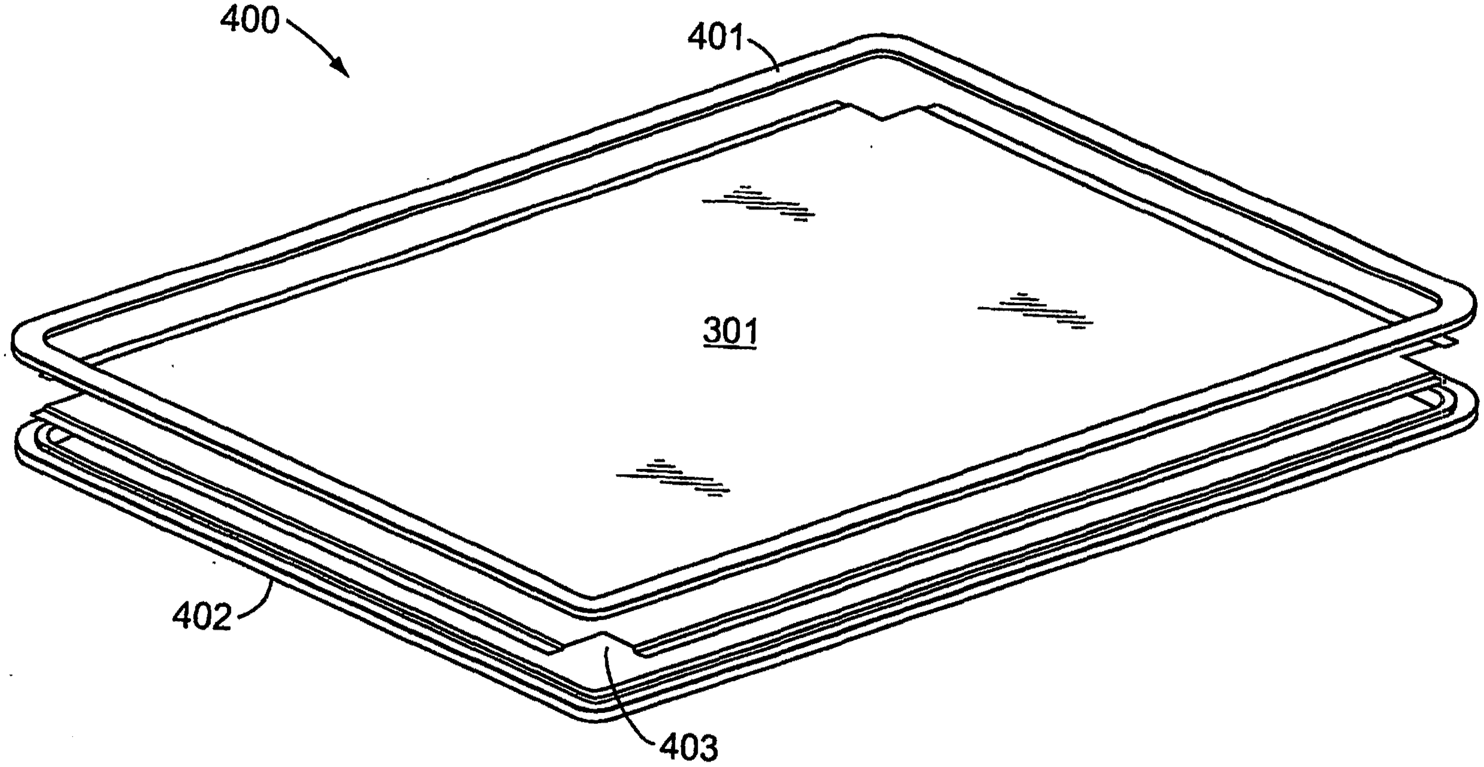

FIG. 4A

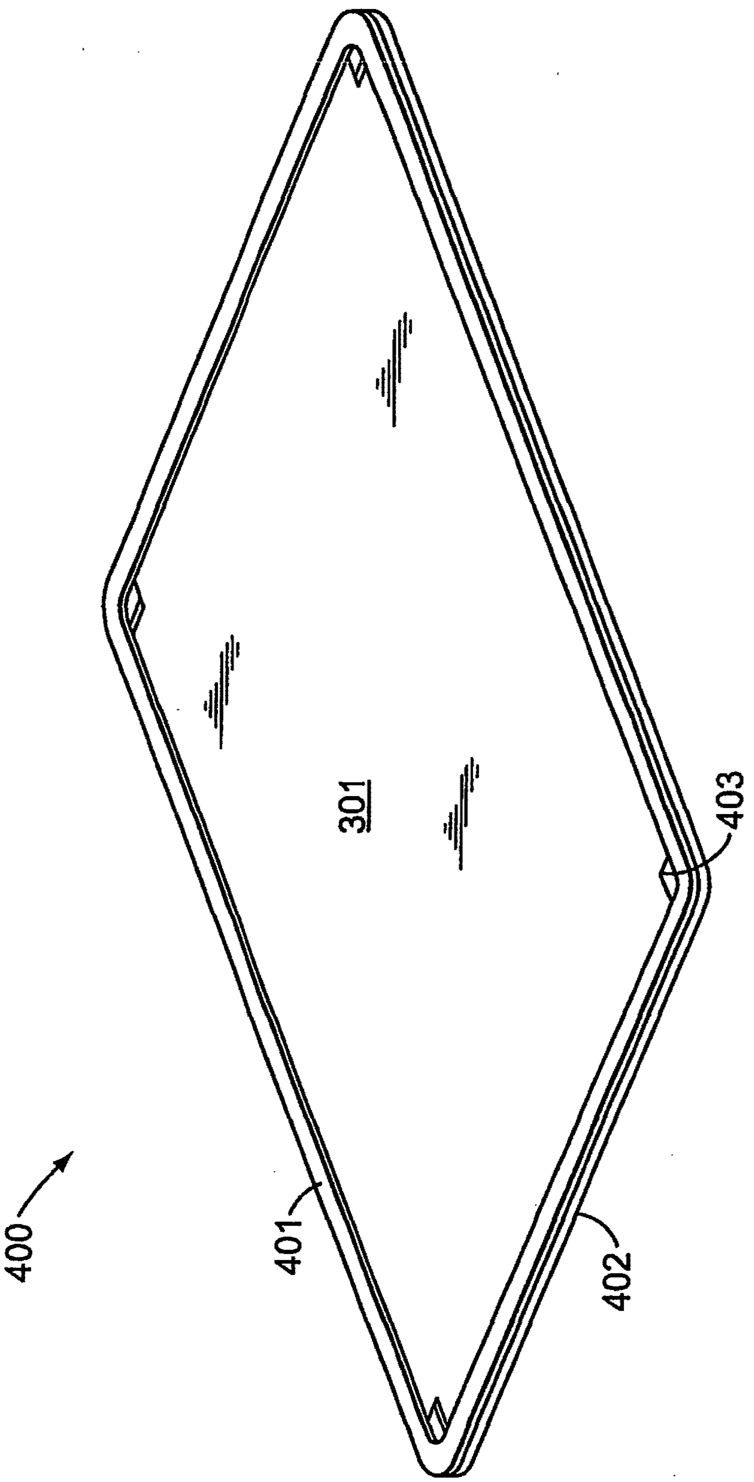

FIG. 4B

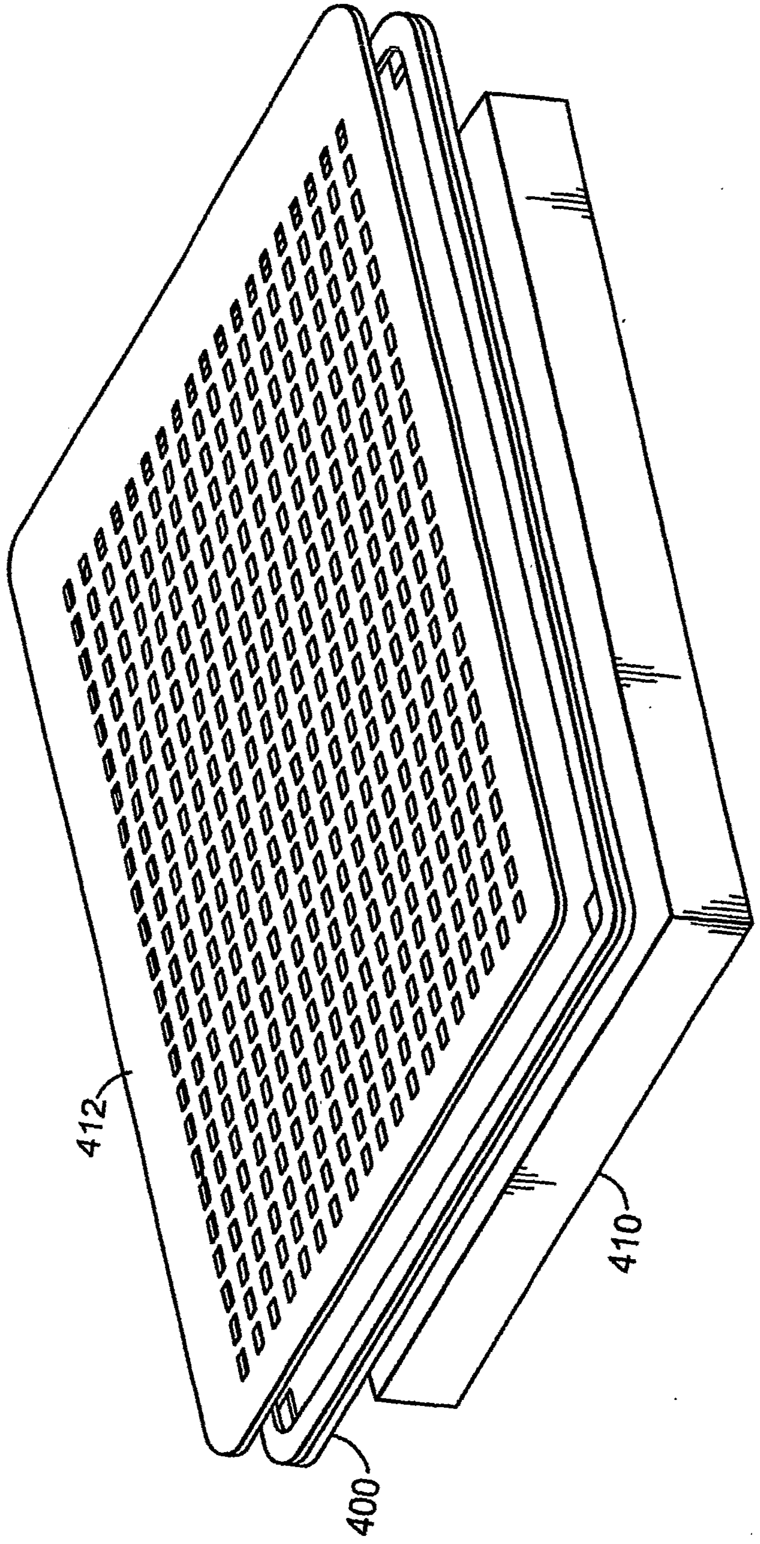

FIG. 4C

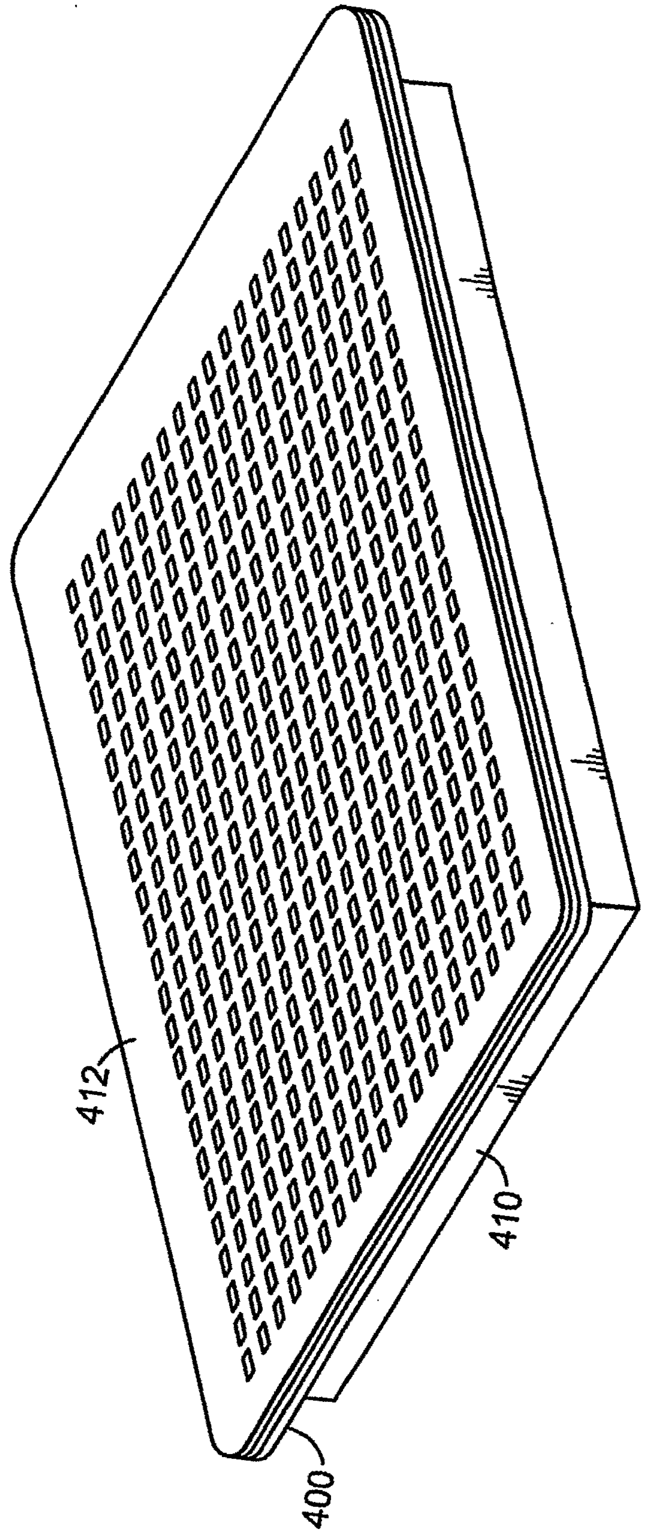

FIG. 4D

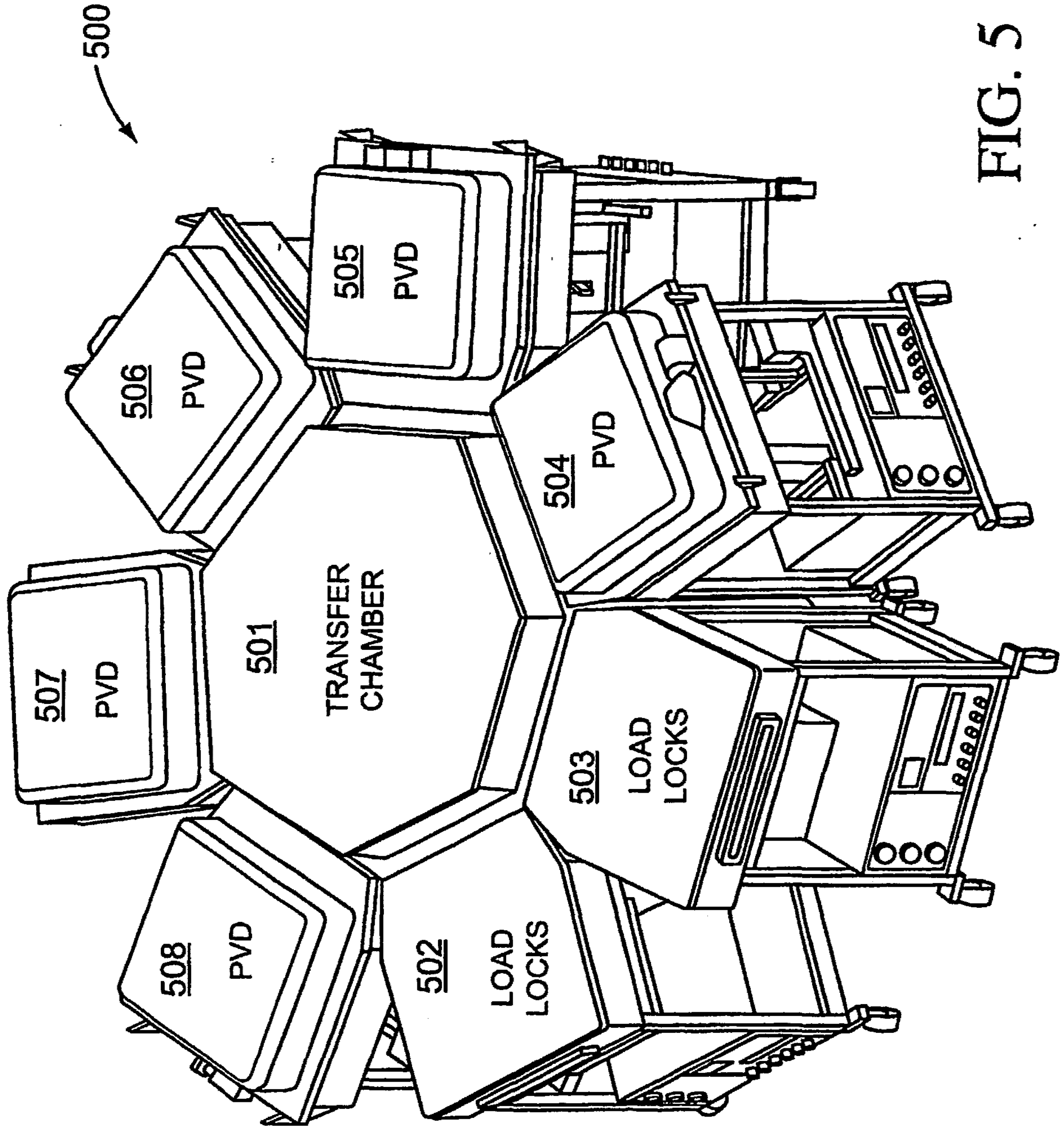
500
501
TRANSFER CHAMBER
502
LOAD LOCKS
503
LOAD LOCKS
504
PVD
505
PVD
506
PVD
507
PVD
508
PVD

FIG. 5

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/228,834	09/16/2005	Hongmei Zhang	10655.0016-02	9006

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FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413

EXAMINER	
MCDONALD, RODNEY GLENN	
ART UNIT	**PAPER NUMBER**
1795	
MAIL DATE	**DELIVERY MODE**
05/29/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

Office Action Summary	Application No. 11/228,834	Applicant(s) ZHANG ET AL.	
	Examiner Rodney G. McDonald	**Art Unit** 1795	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-19 and 38-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15-19 and 40-47* is/are allowed.

6)☒ Claim(s) *38,39 and 48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :9/16/05, 9/30/05, 11/28/05, 11/07/06, 2/06/07, 10/25/07.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 38 and 39 are rejected under 35 U.S.C. 102(b) as being anticipated by Sproul et al. (U.S. Pat. 5,942,089).

Regarding claim 38, Sproul et al. teach a sputtering apparatus comprising means for providing pulsed DC power to a target. (Column 3 lines 66-67; Column 4 lines 1-3) Means for providing a bias power to a substrate. (Column 5 lines 9-21)

Regarding claim 39, Sproul et al. teach means for providing process gas between the target and the substrate. (Column 4 lines 4-11)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sproul et al. (U.S. Pat. 5,942,089) in view of Wang et al. (U.S. Pat. 6,413,382) or Lantsman (U.S. Pat. 5,830,330).

Regarding claim 48, Sproul et al. teach a reactor comprising a pulsed DC power supply. The DC power having oscillating negative and positive voltages supplied form the pulsed DC power supply to the target. (Column 3 lines 66-67; Column 4 lines 1-3) A substrate mount positioned opposite a target mount that holds the target. (Column 3 lines 56-58) A process gas system that allows process gas into an area between the substrate mount and the target mount. (Column 4 lines 4-7)

The difference between Sproul et al. and the present claims is that using a filter is not discussed (Claim 48).

Regarding the filter of claim 48, Wang et al. teach utilizing a filter connected to a pulsed DC power source. (Column 7 lines 61-67)

The motivation for utilizing the features of Wang et al. is that it allows controlling the time constant of the pulse. (Column 7 lines 61-67)

Regarding the filter of claim 48, Lantsman teach utilizing a filter 22 connected to a pulsed DC source. (Column 4 lines 27-30)

The motivation for utilizing the features of Lantsman is that it allows for filtering out RF energy. (Column 4 lines 27-30)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Sproul et al. by utilizing the features of Wang et al. or Lantsman because it allows for controlling the time constant of the pulse or filtering RF energy.

Allowable Subject Matter

Claims 15-19 and 40-47 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Claims 15-19 are allowable over the prior art of record because the prior art of record does not teach the claimed reactor combined with the narrow band rejection filter that rejects at a frequency of the RF bias power supply coupled between the pulsed DC power supply and the target area.

Claims 40-47 are allowable over the prior art of record because the prior art of record does not teach the claimed reactor combined with a narrow band rejection filter operating at a frequency of the RF bias power supply coupled between the pulsed DC power supply and the target.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rodney G. McDonald whose telephone number is 571-272-1340. The examiner can normally be reached on M-Th with every Friday off..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam X. Nguyen can be reached on 571-272-1342. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Rodney G. McDonald/
Primary Examiner, Art Unit 1795

Rodney G. McDonald
Primary Examiner
Art Unit 1795

RM
May 20, 2008

Search Notes	**Application/Control No.** 11228834	**Applicant(s)/Patent Under Reexamination** ZHANG ET AL.
	Examiner Rodney G McDonald	**Art Unit** 1795

SEARCHED

Class	Subclass	Date	Examiner
204	298.2	5/20/07	/RM/
204	298.06	5/20/07	/RM/
204	298.08	5/20/07	/RM/

SEARCH NOTES

Search Notes	Date	Examiner
See East Search	5/20/08	/RM/

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	17	((DC or (direct adj current)) same (pulsed or pulsing or pulse)) and sputter$5 and filter and bias$5 and (204/298.06.ccls.)	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/20 10:46
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BIB DATA SHEET

CONFIRMATION NO. 9006

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/228,834	09/16/2005 **RULE**	204	1795	10655.0016-02

APPLICANTS

Hongmei Zhang, San Jose, CA;
Mukundan Narasimhan, San Jose, CA;
Ravi B. Mullapudi, San Jose, CA;
Richard E. Demaray, Portola Valley, CA;

** **CONTINUING DATA** *************************

This application is a DIV of 10/101,863 03/16/2002 PAT 7,378,356

** **FOREIGN APPLICATIONS** *************************

** **IF REQUIRED, FOREIGN FILING LICENSE GRANTED** **

10/07/2005

		STATE OR COUNTRY	**SHEETS DRAWINGS**	**TOTAL CLAIMS**	**INDEPENDENT CLAIMS**
Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /RODNEY GLENN MCDONALD/ Examiner's Signature	☐ Met after Allowance Initials	CA	27	7	2

ADDRESS

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413
UNITED STATES

TITLE

Biased pulse DC reactive sputtering of oxide films

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PATENT
Customer No. 22,852
Attorney Docket No. 9140.0016-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

ZHANG, Hongmei et al.

Application No.: 11/228,834

Filed: September 16, 2005

For: BIASED PULSE DC REACTIVE SPUTTERING OF OXIDE FILMS

Group Art Unit: Not Yet Assigned

Examiner: Not Yet Assigned

Confirmation No.: Not Yet Assigned

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§ 1.56 and 1.97(b), Applicants bring to the attention of the Examiner the documents on the attached listing. This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits for the above-referenced application. Applicants respectfully request that the Examiner consider the listed documents and indicate that they were considered by making appropriate notations on the attached form.

Copies of the listed non-patent literature documents are attached.

Applicants respectfully request that the Examiner consider the listed documents and indicate that they were considered by making appropriate notations on the attached form.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or

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constitute "prior art." If the Examiner applies any of the documents as prior art against any claims in the application and Applicants determine that the cited documents do not constitute "prior art" under United States law, Applicants reserve the right to present to the office the relevant facts and law regarding the appropriate status of such documents.

Applicants further reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: September 30, 2005

By: Gary J. Edwards
Gary J. Edwards
Reg. No. 41,008

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	14

Complete if Known	
Application Number	
Filing Date	September 16, 2005
First Named Inventor	ZHANG, Hongmei
Art Unit	
Examiner Name	
Attorney Docket Number	9140.0016-02

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

Examiner Initials*	Cite No.¹	Document Number Number-Kind Code² *(if known)*	Issue or Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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/RM/		US 6,605,228 B1	08-12-2003	Kawaguchi et al.	

Examiner Signature	/Rodney Mcdonald/	Date Considered	05/20/2008

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				*Application Number*	
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(Use as many sheets as necessary)				*Examiner Name*	
Sheet	2	of	14	*Attorney Docket Number*	9140.0016-02

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/RM/		US 6,210,544 B1	04-03-2001	Sasaki	

Examiner Signature	/Rodney Mcdonald/	Date Considered	05/20/2008

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				Examiner Name	
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Examiner Signature	/Rodney Mcdonald/	Date Considered	05/20/2008

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT		*Application Number*	
		Filing Date	September 16, 2005
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		Art Unit	
(Use as many sheets as necessary)		*Examiner Name*	
Sheet 4	of 14	*Attorney Docket Number*	9140.0016-02

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Examiner Signature	/Rodney Mcdonald/	Date Considered	05/20/2008

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet	5	of	14

Complete if Known	
Application Number	
Filing Date	September 16, 2005
First Named Inventor	ZHANG, Hongmei
Art Unit	
Examiner Name	
Attorney Docket Number	9140.0016-02

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

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IDS Form PTO/SB/08: Substitute for form 1449A/PTO				***Complete if Known***
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				*Application Number*	
				Filing Date	September 16, 2005
				First Named Inventor	ZHANG, Hongmei
				Art Unit	
(Use as many sheets as necessary)				*Examiner Name*	
Sheet	13	of	14	*Attorney Docket Number*	9140.0016-02

NON PATENT LITERATURE DOCUMENTS			
/RM/		ZHANG, Hongmei et al. "High Dielectric Strength, High k TiO_2 Films by Pulsed DC, Reactive Sputter Deposition," (2001).	
		Office Action issued on September 27, 2004 in U.S. Serial No. 10/291,179 (Attorney Docket No. 09140-0001-00).	
		Response to Office Action filed on March 14, 2005 in U.S. Serial No. 10/291,179 (Attorney Docket No. 09140-0001-00).	
		Office Action issued on June 15, 2005 in U.S. Serial No. 10/291,179 (Attorney Docket No. 09140-0001-00).	
		Office Action issued on May 2, 2002 in U.S. Patent No. 6,533,907 (Attorney Docket No. 09140-0004-00).	
		Response to Office Action filed on September 3, 2002 in U.S. Patent No. 6,533,907 (Attorney Docket No. 09140-0004-00).	
		Office Action issued on February 12, 2004 in U.S. Serial No. 09/903,081 (Attorney Docket No. 09140-0014-00).	
		Response to Office Action filed on August 10, 2004 in U.S. Serial No. 09/903,081 (Attorney Docket No. 09140-0014-00).	
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		Office Action issued on February 12, 2004 in U.S. Serial No. 09/903,081 (Attorney Docket No. 09140-0014-00).	
		Amendment/RCE filed on August 10, 2004 in U.S. Serial No. 09/903,081 (Attorney Docket No. 09140-0014-00).	
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		Office Action issued on September 3, 2003 in U.S. Serial No. 10/101,492 (Attorney Docket No. 09140.0015-00).	
		Response to Office Action filed on March 3, 2004 in U.S. Serial No. 10/101,492 (Attorney Docket No. 09140-0015-00).	
		Office Action issued on February 24, 2004 in U.S. Serial No. 10/101,863 (Attorney Docket No. 09140-0016-00).	
/RM/		Response to Office Action filed on July 23, 2004 in U.S. Serial No. 10/101,863 (Attorney Docket No. 09140-0016-00).	

Examiner Signature	/Rodney Mcdonald/	Date Considered	05/20/2008

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				Application Number	
				Filing Date	September 16, 2005
				First Named Inventor	ZHANG, Hongmei
				Art Unit	
				Examiner Name	
Sheet	14	of	14	*Attorney Docket Number*	9140.0016-02

NON PATENT LITERATURE DOCUMENTS			
/RM/		Office Action issued on October 6, 2004 in U.S. Serial No. 10/101,863 (Attorney Docket No. 09140.0016-00).	
↓		Office Action dated January 13, 2005, received in Application No. 10/101,863 (Attorney Docket No. 09140.0016-00).	
↓		Response to office Action filed on June 10, 2005 in U.S. Serial No. 10/101,863 (Attorney Docket No. 09140.0016-00).	
↓		Office Action issued on August 4, 2005, in U.S. Serial No. 10/101,863 (Attorney Docket No. 09140.0016-00).	
↓		Office Action dated March 25, 2005, received in Application No. 10/954,182 (Attorney Docket No. 09140.0016-01).	
↓		Office Action issued on October 22, 2003 in U.S. Serial No. 10/101,341 (Attorney Docket No. 09140-0017-00).	
↓		Response to Office Action filed on February 23, 2004 in U.S. Serial No. 10/101,341 (Attorney Docket No. 09140-0017-00).	
↓		Office Action issued on June 10, 2004 in U.S. Serial No. 10/101,341 (Attorney Docket No. 09140-0017-00).	
↓		Response to Office Action filed on December 08, 2004 in U.S. Serial No. 10/101,341 (Attorney Docket No. 09140-0017-00).	
↓		Office Action issued on May 4, 2004 in U.S. Application No. 10/101,493 (Attorney Docket No. 09140.0021-00).	
↓		International Search Report issued on November 21, 2003 in PCT/US03/24809 (Attorney Docket No. 09140-0025-00304).	
↓		Office Action issued on March 14, 2005 in U.S. Serial No. 10/789,953 (Attorney Docket No. 09140-0030-00).	
↓		International Search Report issued on October 11, 2004 in PCT/US2004/005531 (Attorney Docket No. 09140-0030-00304)	
↓		Written Opinion issued on October 11, 2004 in PCT/US2004/005531 (Attorney Docket No. 09140-0030-00304)	
↓		Office Action issued March 24, 2005 in U.S. Application No. 10/851,542 (Attorney Docket No. 09140.0033-00).	
↓		Pct international Search Report of Application No. PCT/US2004/014524 dated March 2, 2005 (Attorney Docket No. 09140.0033-00304).	
/RM/		PCT International Search Report of Application No. PCT/US2004/014523 dated January 17, 2005 (Attorney Docket No. 09140.0034-00304).	

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IDS Form PTO/SB/08: Substitute for form 1449A/PTO **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** *(Use as many sheets as necessary)*				***Complete if Known***	
				Application Number	11/228,834
				Filing Date	September 16, 2005
				First Named Inventor	ZHANG, Hongmei
				Art Unit	1753
				Examiner Name	MCDONALD, Rodney Glenn
Sheet	1	of	2	*Attorney Docket Number*	9140.0016-02

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Issue or Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/RM/		US-6,154,582	11-28-2000	Bazylenko et al.	
/RM/		US-2002/0191916 A1	12-19-2002	Frish et al.	
/RM/		US-2005/0175287 A1	08-11-2005	Pan et al.	

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation[6]
/RM/		BELKIND, A. et al., "Pulsed-DC Reactive Sputtering of Dielectrics: Pulsing Parameter Effects," 43rd Annual Technical Conference Proceedings-Denver: 86-90 (April 15-20, 2000).	
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		Office Action dated December 1, 2006, in U.S. Application No. 10,291,179 (Attorney Docket No. 9140.0001-00).	
		Office Action dated December 18, 2006, in U.S. Application No. 09/903,081 (Attorney Docket No. 9140.0014-00).	
		Office Action dated December 1, 2006, in U.S. Application No. 11/100,856 (Attorney Docket No. 9140.0015-01).	
		Response dated February 6, 2007, in U.S. Application No. 10/101,863 (Attorney Docket No. 9140.0016-00).	
		Response to Office Action dated December 6, 2006, in Application No. 10/954,182 (Attorney Docket No. 9140.0016-01).	
		Supplemental Preliminary Amendment dated February 6, 2007, in U.S. Application No. 11/191,643 (Attorney Docket No. 9140.0016-04).	
		Response to Office Action dated December 21, 2006, in U.S. Application No. 11/228,805 (Attorney Docket No. 9140.0030-01).	
/RM/		Response to Office Action dated November 8, 2006, to the Korean Patent Office in Application No. 10-2005-7016055 (Attorney Docket No. 9140.0030-	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet	2	of	2

Complete if Known	
Application Number	11/228,834
Filing Date	September 16, 2005
First Named Inventor	ZHANG, Hongmei
Art Unit	1753
Examiner Name	MCDONALD, Rodney Glenn
Attorney Docket Number	9140.0016-02

NON PATENT LITERATURE DOCUMENTS

		00202).	
/RM/		Response to Office Action dated January 26, 2007, in U.S. Application No. 10/851,542 (Attorney Docket No. 9140.0033-00).	
		Preliminary Amendment dated July 21, 2006, in U.S. Application No. 11/297,057 (Attorney Docket No. 9140.0042-00).	
		Supplemental Preliminary Amendment, Substitute Specification with Markings, Substitute Specification without Markings, and Replacement Drawing Sheets dated December 6, 2006 in U.S. Application No. 11/297,057 (Attorney Docket No. 9140.0042-00)	
		Continuation application and Preliminary Amendment dated December 13, 2006 (Attorney Docket No. 9140.0042-01).	
		Voluntary Amendment dated August 15, 2006 in TW Appl. No. 94143175 (Attorney Docket No. 9140.0042-00270).	
		PCT International Search Report and Written Opinion for Application No. PCT/US05/44781 dated October 3, 2006 (Attorney Docket No. 9140.0042-00304).	
/RM/		Specification dated September 2, 2005, for U.S. Appl. No. 11/218,652 (Attorney Docket No. 9140.0052-00).	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet	1	of	1

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Application Number	11/228,834
Filing Date	September 16, 2005
First Named Inventor	ZHANG, Hongmei
Art Unit	1753
Examiner Name	Not Yet Assigned
Attorney Docket Number	9140.0016-02

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	Translation[6]

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/RM/		Office Action issued September 21, 2005 in U.S. Application No. 11/100,856 (Attorney Docket No. 09140.0015-01).	
/RM/		Office Action issued on October 25, 2005, in U.S. Appl. No. 10/954,182 (Attorney Docket No. 09140-0016-01000).	
/RM/		Office Action issued on October 3, 2005 in U.S. Application No. 10/650,461 (Attorney Docket No. 09140-0025-00).	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet	1	of	6

Complete if Known	
Application Number	11/228,834
Filing Date	September 16, 2005
First Named Inventor	ZHANG, Hongmei
Art Unit	1753
Examiner Name	MCDONALD, Rodney Glenn
Attorney Docket Number	9140.0016-02

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

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/RM/		US-3,309,302	03-14-1967	Heil	
		US-4,710,940	12-01-1987	Sipes, Jr.	
		US-4,785,459	11-15-1988	Baer	
		US-5,338,625	08-16-1994	Bates et al.	
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		US-2002/0076133 A1	06-20-2002	Li et al.	
		US-2003/0044118 A1	03-06-2003	Zhou et al.	
		US-2003/0143853 A1	07-31-2003	Celii et al.	
		US-2003/0185266 A1	10-02-2003	Henrichs	
/RM/		US-2005/0048802 A1	03-02-2005	Zhang et al.	

Examiner Signature	/Rodney Mcdonald/	Date Considered	05/20/2008

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IDS Form PTO/SB/08: Substitute for form 1449A/PTO				***Complete if Known***	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				*Application Number*	11/228,834
				Filing Date	September 16, 2005
				First Named Inventor	ZHANG, Hongmei
				Art Unit	1753
(Use as many sheets as necessary)				*Examiner Name*	MCDONALD, Rodney Glenn
Sheet	2	of	6	*Attorney Docket Number*	9140.0016-02

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

/RM/		US-2005/0183946 A1	08-25-2005	Pan et al.	
↓		US-2006/0057283 A1	03-16-2006	Zhang et al.	
↓		US-2006/0057304 A1	03-16-2006	Zhang et al.	
↓		US-2006/0071592 A1	04-06-2006	Narasimhan et al.	
/RM/		US-2006/0134522 A1	06-22-2006	Zhang et al.	

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FOREIGN PATENT DOCUMENTS

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/RM/		JP 7-224379 A	08-22-1995	Ulvac Japan Ltd		
↓		KR 2002-26187	04-06-2002	Hyundai Motor Co Ltd		Abstract
↓		WO 01/82297 A1	11-01-2001	Koninklijke Philips Electronics N.V.		
↓		WO 2004/106581 A2	12-09-2004	Symmorphix, Inc.		
↓		WO 2004/106582 A2	12-09-2004	Symmorphix, Inc.		
/RM/		WO 2006/063308 A2	06-15-2006	Symmorphix, Inc.		

NON PATENT LITERATURE DOCUMENTS

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/RM/		AGRAWAL, G.P., in: Fiber-Optic Communication Systems, 2nd Edition, John Wiley & Sons, New York, pp. 361-399 and 415 (1997).	
/RM/		COCORULLO, G. et al., "Amorphous silicon waveguides and light modulators for integrated photonics realized by low-temperature plasma-enhanced chemical-vapor deposition," Optics Lett. 21(24):2002-2004 (1996).	
/RM/		MASUDA, H. & KAWAI, S., "Wide-band and gain-flattened hybrid fiber amplifier consisting of an EDFA and a multiwavelength pumped raman amplifier," IEEE Photonics Technology Lett. 11(6):647-649 (1999).	
/RM/		SNOEKS, E. et al., "Cooperative upconversion in erbium-implanted soda-lime silicate glass optical waveguides," J. Opt. Soc. Am. B 12(8):1468-1474 (1995).	

Examiner Signature	/Rodney Mcdonald/	Date Considered	05/20/2008

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Sheet	3	of	6

Complete if Known	
Application Number	11/228,834
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First Named Inventor	ZHANG, Hongmei
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/RM/		Response to Office Action filed on October 17, 2005 in U.S. Application No. 10/291,179 (Atty. Docket No. 09140.0001-00).	
		Final Office Action issued on December 14, 2005 in U.S. Application No. 10/291,179 (Atty. Docket No. 09140.0001-00).	
		Response to Final Office Action filed April 14, 2006, in U.S. Appl. No. 10/291,179 (Atty. Docket No. 9140.0001-00).	
		Office Action mailed April 27, 2006, in U.S. Appl. No. 10/291,179 (Atty. Docket No. 9140.0001-00).	
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		Final Office Action dated October 12, 2006, in U.S. Application No. 10,291,179 (Attorney Docket No. 9140.0001-00).	
		Response to Final Office Action mailed November 3, 2006, in U.S. Application No. 10,291,179 (Attorney Docket No. 9140.0001-00).	
		Office Action issued November 28, 2001, for US Patent No. 6,506,289 (Atty. Docket No. 09140.0002-01).	
		Response to Office Action filed February 20, 2002, for US Patent No. 6,506,289 (Atty. Docket No. 09140.0002-01).	
		Office Action issued April 17, 2002, for US Patent No. 6,506,289 (Atty. Docket No. 09140.0002-01).	
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		Notice of Allowance mailed August 6, 2002, for US Patent No. 6,506,289 (Atty. Docket No. 09140.0002-01).	
		Ex parte Quayle Action mailed November 10, 2003 for US Patent No. 6,827,826 (Atty. Docket No. 09140.0002-02).	
		Notice of Allowance mailed March 25, 2004 for US Patent No. 6,827,826 (Atty. Docket No. 09140.0002-02).	
		PCT Invitation to Pay Additional Fees for PCT/US01/22750, dated March 13, 2002 (Atty. Docket No. 09140.0002-00304).	
		PCT International Search Report for PCT/US01/22750, dated July 19, 2002 (Atty. Docket No. 09140.0002-00304).	
		PCT Written Opinion for PCT/US01/22750, dated July 23, 2002 (Atty. Docket No. 09140.0002-00304).	
/RM/		PCT International Preliminary Examination Report for PCT/US01/22750, dated	

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Application Number	11/228,834
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First Named Inventor	ZHANG, Hongmei
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Attorney Docket Number	9140.0016-02

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/RM/		October 8, 2002 (Atty. Docket No. 09140.0002-00304).	
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		Office Action issued on November 28, 2005 in U.S. Application No. 09/903,081 (Atty. Docket No. 09140-0014-00).	
		Response to Office Action filed February 28, 2006 in U.S. Application No. 09/903,081 (Atty. Docket No. 09140-0014-00).	
		Final Office Action mailed May 8, 2006 in U.S. Application No. 09/903,081 (Atty. Docket No. 09140-0014-00).	
		Amendment dated October 19, 2006, in U.S. Application No. 09/903,081 (Atty. Docket No. 09140.0014-00).	
		Notice of Allowance issued on October 21, 2004, in U.S. Application No. 10/101,492 (Atty. Docket No. 09140-0015-00).	
		Response to Office Action filed February 17, 2006 in U.S. Application No. 11/100,856 (Atty. Docket No. 09140.0015-01).	
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		Response to Office Action filed September 11, 2006 in U.S. Application No. 11/100,856 (Atty. Docket No. 09140.0015-01.)	
		Response to Office Action filed December 5, 2005, in U.S. Application No. 10/101,863 (Atty. Docket No. 09140.0016-00).	
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		Office Action mailed March 22, 2006, in U.S. Appl. No. 10/101,863 (Atty. Docket No. 09140.0016-00).	
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/RM/		Response to Office Action filed on July 25, 2005 in Application No. 10/954,182 (Atty. Docket No. 09140.0016-01).	

Examiner Signature	/Rodney Mcdonald/	Date Considered	05/20/2008

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

EXPRESS MAIL LABEL NO.
EV 746095967 US

IDS Form PTO/SB/08: Substitute for form 1449A/PTO		**Complete if Known**	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		*Application Number*	11/228,834
		Filing Date	September 16, 2005
		First Named Inventor	ZHANG, Hongmei
		Art Unit	1753
(Use as many sheets as necessary)		*Examiner Name*	MCDONALD, Rodney Glenn
Sheet 5	of 6	*Attorney Docket Number*	9140.0016-02

NON PATENT LITERATURE DOCUMENTS			
/RM/		Response to Office Action filed on December 21, 2005 in Application No. 10/954,182 (Atty. Docket No. 09140.0016-01).	
		Office Action issued on March 9, 2006, in U.S. Appl. No. 10/954,182 (Atty. Docket No. 09140-0016-01000).	
		Response to Office Action filed on August 9, 2006 in Application No. 10/954,182 (Atty. Docket No. 09140.0016-01).	
		Office Action dated October 31, 2006, in Application No. 10/954,182 (Atty. Docket No. 09140.0016-01).	
		Response to Office Action filed on January 3, 2006 in U.S. Application No. 10/650,461 (Atty. Docket No. 09140-0025-00).	
		Office Action issued on March 23, 2006, in U.S. Application No. 10/650,461 (Atty. Docket No. 09140-0025-00).	
		Response to Office Action filed on July 24, 2006, in U.S. Application No. 10/650,461 (Atty. Docket No. 09140-0025-00).	
		Final Office Action mailed October 19, 2006, in U.S. Application No. 10/650,461 (Attorney Docket No. 09140.0025-00).	
		Voluntary Amendment filed July 26, 2006 in TW Appl. No. 92123625 (Atty. Docket No. 09140.0025-00270).	
		International Preliminary Examination Report mailed on April 15, 2004 in PCT/US03/24809 (Atty. Docket No. 09140-0025-00304).	
		Office Action issued on December 2, 2005 in U.S. Application No. 10/789,953 (Atty. Docket No. 09140.0030-00).	
		Response to Office Action filed March 2, 2006 in U.S. Application No. 10/789,953 (Atty. Docket No. 09140.0030-00).	
		Final Office Action issued on May 19, 2006 in U.S. Application No. 10/789,953 (Atty. Docket No. 09140.0030-00).	
		Response to Final Office Action filed August 3, 2006, in U.S. Application No. 10/789,953 (Atty. Docket No. 09140.0030-00).	
		Notice of Allowance mailed October 23, 2006, in U.S. Application No. 10/789,953 (Atty. Docket No. 09140.0030-00).	
		Office Action dated October 12, 2006, for U.S. Application No. 11/228,805 (Attorney Docket No. 09140.0030-01000).	
		Office Action dated September 22, 2006 from Korean Patent Office in Appl. No. 10-2005-7016055 (Atty. Docket No. 09140.0030-00202)	
/RM/		Office Action from Singapore Patent Office in Appl. No. 200505388-9, dated	

Examiner Signature	/Rodney Mcdonald/	Date Considered	05/20/2008

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

EXPRESS MAIL LABEL NO.
EV 746095967 US

IDS Form PTO/SB/08: Substitute for form 1449A/PTO **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** *(Use as many sheets as necessary)*	***Complete if Known***	
	Application Number	11/228,834
	Filing Date	September 16, 2005
	First Named Inventor	ZHANG, Hongmei
	Art Unit	1753
	Examiner Name	MCDONALD, Rodney Glenn
Sheet 6 of 6	*Attorney Docket Number*	9140.0016-02

NON PATENT LITERATURE DOCUMENTS

/RM/		March 20, 2006 (Atty. Docket No. 9140.0030-00256).	
		Response to Office Action from Singapore Patent Office in Appl. No. 200505388-9, dated August 11, 2006 (Atty. Docket No. 9140.0030-00256).	
		Response to Office Action dated July 25, 2005 in U.S. Application No. 10/851,542 (Atty. Docket No. 09140-0033-00).	
		Office Action issued on October 19, 2005 in U.S. Application No. 10/851,542 (Atty. Docket No. 09140.0033-00).	
		Response to Office Action filed January 19, 2006 in U.S. Application No. 10/851,542 (Atty. Docket No. 09140.0033-00).	
		Office Action mailed April 19, 2006 in U.S. Application No. 10/851,542 (Atty. Docket No. 09140.0033-00).	
		Response to Office Action filed July 26, 2006 in U.S. Application No. 10/851,542 (Atty. Docket No. 09140.0033-00).	
		Final Office Action dated October 26, 2006, in U.S. Application No. 10/851,542 (Atty. Docket No. 09140.0033-00).	
		PCT International Search Report and Written Opinion for Application No. PCT/US2004/014524 dated March 2, 2005 (Atty. Docket No. 09140.0033-00304).	
		PCT International Preliminary Report on Patentability for Application No. PCT/US2004/014524, dated December 8, 2005 (Atty. Docket No. 09140.0033-00304).	
		PCT International Search Report and Written Opinion for Application No. PCT/US2004/014523 dated January 17, 2005 (Atty. Docket No. 09140.0034-00304).	
/RM/		PCT International Preliminary Report on Patentability for Application No. PCT/US2004/014523, dated December 8, 2005 (Atty. Docket No. 09140.0034-00304).	

Examiner Signature	/Rodney Mcdonald/	Date Considered	05/20/2008

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

EXPRESS MAIL LABEL NO.
EV 746095967 US

Index of Claims	**Application/Control No.** 11228834	**Applicant(s)/Patent Under Reexamination** ZHANG ET AL.
	Examiner Rodney G McDonald	**Art Unit** 1795

✓	**Rejected**	-	**Cancelled**	N	**Non-Elected**	A	**Appeal**
=	**Allowed**	÷	**Restricted**	I	**Interference**	O	**Objected**

☐ **Claims renumbered in the same order as presented by applicant** ☐ **CPA** ☐ **T.D.** ☐ **R.1.47**

CLAIM		**DATE**								
Final	Original	05/20/2008								
	1	-								
	2	-								
	3	-								
	4	-								
	5	-								
	6	-								
	7	-								
	8	-								
	9	-								
	10	-								
	11	-								
	12	-								
	13	-								
	14	-								
	15	=								
	16	=								
	17	=								
	18	=								
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	21	-								
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	26	-								
	27	-								
	28	-								
	29	-								
	30	-								
	31	-								
	32	-								
	33	-								
	34	-								
	35	-								
	36	-								

Index of Claims	**Application/Control No.** 11228834	**Applicant(s)/Patent Under Reexamination** ZHANG ET AL.
	Examiner Rodney G McDonald	**Art Unit** 1795

✓	**Rejected**		**-**	**Cancelled**		**N**	**Non-Elected**		**A**	**Appeal**
=	**Allowed**		**÷**	**Restricted**		**I**	**Interference**		**O**	**Objected**

☐ **Claims renumbered in the same order as presented by applicant** ☐ **CPA** ☐ **T.D.** ☐ **R.1.47**

CLAIM		**DATE**								
Final	Original	05/20/2008								
	37	-								
	38	✓								
	39	✓								
	40	=								
	41	=								
	42	=								
	43	=								
	44	=								
	45	=								
	46	=								
	47	=								
	48	✓								

OIPE OCT 1 5 2007 PATENT & TRADEMARK OFFICE

IDS Form PTO/SB/08: Substitute for form 1449A/PTO		**Complete if Known**	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		*Application Number*	11/228,834
		Filing Date	September 16, 2005
		First Named Inventor	ZHANG, Hongmei
		Art Unit	1795
(Use as many sheets as necessary)		*Examiner Name*	MCDONALD, Rodney Glenn
Sheet 1	of 2	*Attorney Docket Number*	10655.0016-02

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Issue or Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/RM/		US-6,391,166 B1	05-21-2002	Wang	
/RM/		US-7,262,131 B2	08-28-2007	Narasimhan et al.	
/RM/		US-2001/0034106 A1	10-25-2001	Moise et al.	
/RM/		US-2007/0053139 A1	03-08-2007	Zhang et al.	

Note: Submission of copies of U.S. Patents and published U.S. Patent Applications is not required.

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	Translation[6]
/RM/		WO 2007/027535 A2	03-08-2007	Symmorphix, Inc.		

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation[6]
/RM/		Response to Office Action dated March 1, 2007, in U.S. Application No. 10/291,179 (Attorney Docket No. 9140.0001-00).	
↓		Office Action dated May 21, 2007, in U.S. Application No. 10/291,179 (Attorney Docket No. 9140.0001-00).	
↓		Response to Office Action filed March 19, 2007, in U.S. Application No. 09/903,081 (Attorney Docket No. 9140.0014-00).	
↓		Final Office Action dated April 13, 2007, in U.S. Application No. 09/903,081 (Attorney Docket No. 9140.0014-00).	
↓		Amendment/RCE filed August 9, 2007, in U.S. Application No. 09/903,081 (Attorney Docket No. 9140.0014-00).	
↓		Office Action dated September 5, 2007, in U.S. Application No. 09/903,081 (Attorney Docket No. 9140.0014-00).	
↓		Response to Office Action filed March 1, 2007, in U.S. Application No. 11/100,856 (Attorney Docket No. 9140.0015-01).	
↓		Final Office Action dated September 7, 2007, in U.S. Application No. 11/100,856 (Attorney Docket No. 9140.0015-01).	
↓		Response to Office Action filed February 6, 2007, in U.S. Application No. 10/101,863 (Attorney Docket No. 9140.0016-00).	
↓		Final Office Action dated May 2, 2007, in U.S. Application No. 10/101,863 (Attorney Docket No. 9140.0016-00).	
↓		Response to Final Office Action filed October 2, 2007, in U.S. Application No. 10/101,863 (Attorney Docket No. 9140.0016-00).	
/RM/		Office Action dated March 14, 2007, in U.S. Application No. 10/954,182 (Attorney Docket No. 9140.0016-01).	

Examiner Signature	/Rodney Mcdonald/	Date Considered	05/20/2008

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

IDS Form PTO/SB/08: Substitute for form 1449A/PTO **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** *(Use as many sheets as necessary)*				***Complete if Known***	
				Application Number	11/228,834
				Filing Date	September 16, 2005
				First Named Inventor	ZHANG, Hongmei
				Art Unit	1795
				Examiner Name	MCDONALD, Rodney Glenn
Sheet	2	of	2	*Attorney Docket Number*	10655.0016-02

/RM/		Response to Office Action filed March 30, 2007, in U.S. Application No. 10/954,182 (Attorney Docket No. 9140.0016-01).	
		Notice of Non-Compliant Amendment dated April 12, 2007, in U.S. Application No. 10/954,182 (Attorney Docket No. 9140.0016-01).	
		Response to Notice of Non-Compliant Amendment filed April 23, 2007, in U.S. Application No. 10/954,182 (Attorney Docket No. 9140.0016-01).	
		Final Office Action dated July 24, 2007, in U.S. Application No. 10/954,182 (Attorney Docket No. 9140.0016-01).	
		Preliminary Amendment filed July 27, 2005, in U.S. Application No. 11/191,643 (Attorney Docket No. 9140.0016-04).	
		Corrected Preliminary Amendment filed September 19, 2005, in U.S. Application No. 11/191,643 (Attorney Docket No. 9140.0016-04).	
		Response to Office Action filed February 20, 2007, in U.S. Application No. 10/650,461 (Attorney Docket No. 9140.0025-00).	
		Office Action dated March 6, 2007, in U.S. Application No. 10/650,461 (Attorney Docket No. 9140.0025-00).	
		Response to Office Action filed July 9, 2007, in U.S. Application No. 10/650,461 (Attorney Docket No. 9140.0025-00).	
		Final Office Action dated October 10, 2007, in U.S. Application No. 10/650,461 (Attorney Docket No. 9140.0025-00).	
		Notice of Allowance dated February 21, 2007, in U.S. Application No. 10/789,953 (Attorney Docket No. 9140.0030-00).	
		Notice of Allowance dated March 26, 2007, in U.S. Application No. 11/228,805 (Attorney Docket No. 9140.0030-01).	
		Corrected Notice of Allowance dated June 7, 2007, in U.S. Application No. 11/228,805 (Attorney Docket No. 9140.0030-01).	
		Supplemental Notice of Allowance dated July 5, 2007, in U.S. Application No. 11/228,805 (Attorney Docket No. 9140.0030-01).	
		Notice of Allowance dated February 22, 2007, in U.S. Application No. 10/851,542 (Attorney Docket No. 9140.0033-00).	
		Supplemental Notice of Allowance dated March 15, 2007, in U.S. Application No. 10/851,542 (Attorney Docket No. 9140.0033-00).	
		Preliminary Amendment filed March 22, 2007, in U.S. Application No. 11/726,972 (Attorney Docket No. 9140.0033-01).	
		Voluntary Amendment filed March 8, 2007, in Taiwan Application No. 93114518 (Attorney Docket No. 9140.0033-270).	
		Second Supplemental Preliminary Amendment filed May 31, 2007, in U.S. Application No. 11/297,057 (Attorney Docket No. 9140.0042-00).	
/RM/		PCT International Preliminary Report on Patentability dated June 21, 2007, in International Application No. PCT/US2005/044781 (Attorney Docket No. 9140.0042-304).	

Examiner Signature	/Rodney Mcdonald/	Date Considered	05/20/2008

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

EXPRESS MAIL LABEL NO.
EM 100825629 US

PATENT
Customer No. 22,852
Attorney Docket No. 10655.0016-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)
	)
Hongmei ZHANG et al.	) Group Art Unit: 1795
	)
Application No.: 11/228,834	) Examiner: Rodney Glenn MCDONALD
	)
Filed: September 16, 2005	)
	) Confirmation No.: 9006
For: BIASED PULSE DC REACTIVE SPUTTERING OF OXIDE FILMS	)
	)

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

AMENDMENT AND RESPONSE TO OFFICE ACTION

In reply to the Office Action mailed May 29, 2008, the period for response having been extended to September 29, 2008 by a request for extension of one month and fee payment filed concurrently herewith, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims in this paper beginning on page 2.

Remarks/Arguments follow the amendment sections of this paper beginning on page 5.

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1.-14. (Canceled).

15. (Previously presented) A reactor according to the present invention, comprising:

a target area for receiving a target;

a substrate area opposite the target area for receiving a substrate;

a pulsed DC power supply coupled to the target area, the pulsed DC power supply providing alternating negative and positive voltages to the target;

an RF bias power supply coupled to the substrate; and

a narrow band-rejection filter that rejects at a frequency of the RF bias power supply coupled between the pulsed DC power supply and the target area.

16. (Previously presented) The reactor of claim 15, wherein the target has a surface area greater than the surface area of the substrate.

17. (Previously presented) The reactor of claim 15, further including a magnet which provides erosion of the target.

18. (Previously presented) The reactor of claim 17, wherein the magnet scans across the target in a first direction and extends in a second direction perpendicular to the first direction.

19. (Previously presented) The reactor of claim 18, wherein the magnet extends beyond the target in the second direction.

20.-39. (Canceled).

40. (Previously presented) A reactor according to the present invention, comprising:

a target area for receiving a target;

a magnetic field generator supplying a magnetic field to the target;

a substrate area opposite the target area for receiving a substrate;

a pulsed DC power supply coupled to the target to provide alternating positive and negative voltages to the target;

an RF bias power supply coupled to provide an RF bias to the substrate; and

a narrow band rejection filter operating at a frequency of the RF bias power supply coupled between the pulsed DC power supply and the target,

wherein a material is deposited on the substrate by exposure of the substrate to a plasma generated when pulsed DC power from the pulsed DC power supply is applied to the target in the presence of a process gas.

41. (Previously presented) The reactor of claim 40, wherein the target is a metallic target.

42. (Previously presented) The reactor of claim 40, wherein the process gas includes one or more of a set consisting of Ar, O_2, N_2, NH_3, CO, NO, CO_2, C_2F_6, and halide containing gasses.

43. (Previously presented) The reactor of claim 40, wherein the target is a ceramic target.

44. (Previously presented) The reactor of claim 40, further including a temperature controller for holding the temperature of the substrate substantially constant.

45. (Previously presented) The reactor of claim 40, wherein the target is an alloyed target.

46. (Previously presented) The reactor of claim 45 wherein the alloyed target includes one or more rare-earth ions.

47. (Previously presented) The reactor of claim 45 wherein the alloyed target includes one or more elements taken from a set consisting of Si, Al, Er, Yb, Zn, Ga, Ge, P, As, Sn, Sb, Pb, Ag, Au, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy Ho, Tm, and Lu.

48. (Canceled)

REMARKS

Claims 15-19, and 38-48 are pending in the above identified application. The Examiner has rejected claims 38, 39, and 48. In this amendment, Applicants have canceled claims 38, 39, and 48. Therefore, the both the rejection of claims 38 and 39 under 35 U.S.C. § 102(b) and the rejection of claim 48 under 35 U.S.C. § 103(a) are moot. Applicants reserve the right to pursue claims 38, 39, and 48 in a subsequently filed application.

Applicants thank the Examiner for indicating that claims 15-19 and 40-47 are allowable over the prior art. In view of the foregoing amendments and remarks, Applicants respectfully request reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: September 29, 2008

By:
Gary J. Edwards
Reg. No. 41,008
(650) 849-6622

PATENT
Customer No. 22,852
Attorney Docket No. 10655.0016-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Hongmei ZHANG et al.	)	Group Art Unit: 1795
	)	
Application No.: 11/228,834	)	Examiner: Rodney Glenn MCDONALD
	)	
Filed: September 16, 2005	)	
	)	
For: BIASED PULSE DC REACTIVE SPUTTERING OF OXIDE FILMS	)	Confirmation No.: 9006

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

PETITION FOR EXTENSION OF TIME

Applicant petitions for a one month extension of time to file a reply to the Office Action of May 29, 2008. A fee of $120.00 is enclosed.

Please grant any additional extensions of time required to enter the attached reply and charge any additional required fees to Deposit Account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: September 29, 2008

By: Gary J. Edwards
Gary J. Edwards
Reg. No. 41,008
(650) 849-6622

Electronic Patent Application Fee Transmittal

Application Number:	11228834
Filing Date:	16-Sep-2005
Title of Invention:	Biased pulse DC reactive sputtering of oxide films
First Named Inventor/Applicant Name:	Hongmei Zhang
Filer:	Aaron James Capron/Drew Herndon
Attorney Docket Number:	10655.0016-02

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 1 month with $0 paid	1251	1	120	120

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
	Total in USD ($)			**120**

Electronic Acknowledgement Receipt

EFS ID:	4026686
Application Number:	11228834
International Application Number:	
Confirmation Number:	9006
Title of Invention:	Biased pulse DC reactive sputtering of oxide films
First Named Inventor/Applicant Name:	Hongmei Zhang
Customer Number:	22852
Filer:	Aaron James Capron/Drew Herndon
Filer Authorized By:	Aaron James Capron
Attorney Docket Number:	10655.0016-02
Receipt Date:	29-SEP-2008
Filing Date:	16-SEP-2005
Time Stamp:	18:07:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$120
RAM confirmation Number	4247
Deposit Account	060916
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	10655-0016-02_Response_to_OA_dtd_5-29-08.pdf	45588 d2ce853b91ef41d65553ef08a9f77b187758358b	no	5
Warnings:					
Information:					
2	Extension of Time	10655-0016-02_EOT_1MO.pdf	11872 7eda55149f8718c79009e9e594063299bd8aa477	no	1
Warnings:					
Information:					
3	Fee Worksheet (PTO-06)	fee-info.pdf	29953 c736f7f9dd5b452db0774f4a0c8580066094d02e	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	87413	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 11/228,834	Filing Date 09/16/2005	☐ To be Mailed

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT		(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
	09/29/2008	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 13	Minus	** 20	= 0	X $ =		OR	X $50=	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***4	= 0	X $ =		OR	X $210=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	**0**

AMENDMENT		(Column 1)		(Column 2)	(Column 3)					
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/BRENDA MURPHY/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

22852 7590 12/30/2008

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER
LLP
901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413

EXAMINER	
MCDONALD, RODNEY GLENN	
ART UNIT	PAPER NUMBER
1795	

DATE MAILED: 12/30/2008

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/228,834	09/16/2005	Hongmei Zhang	10655.0016-02	9006

TITLE OF INVENTION: BIASED PULSE DC REACTIVE SPUTTERING OF OXIDE FILMS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	03/30/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail
Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

22852 7590 12/30/2008

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER
LLP
901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/228,834	09/16/2005	Hongmei Zhang	10655.0016-02	9006

TITLE OF INVENTION: BIASED PULSE DC REACTIVE SPUTTERING OF OXIDE FILMS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	03/30/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
MCDONALD, RODNEY GLENN	1795	204-298080

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
   - ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
   - ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 ____________________
2 ____________________
3 ____________________

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies ____________________

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number ____________ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature ______________________________ Date ______________________________

Typed or printed name ______________________________ Registration No. ______________________________

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/228,834	09/16/2005	Hongmei Zhang	10655.0016-02	9006

22852 7590 12/30/2008

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WASHINGTON, DC 20001-4413

EXAMINER	
MCDONALD, RODNEY GLENN	
ART UNIT	PAPER NUMBER
1795	

DATE MAILED: 12/30/2008

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 529 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 529 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	**Application No.** 11/228,834	**Applicant(s)** ZHANG ET AL.	
	Examiner Rodney G. McDonald	**Art Unit** 1795	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *September 29, 2008*.

2. ☒ The allowed claim(s) is/are *15-19 and 40-47*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE “MAILING DATE” of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE**.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER’S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as “replacement sheets”) must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson’s Patent Drawing Review (PTO-948) attached
   1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner’s Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner’s comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Rodney G. McDonald/
Primary Examiner, Art Unit 1795

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

Claims 15-19 are allowable over the prior art of record because the prior art of record does not teach the claimed reactor combined with the narrow band rejection filter that rejects at a frequency of the RF bias power supply coupled between the pulsed DC power supply and the target area.

Claims 40-47 are allowable over the prior art of record because the prior art of record does not teach the claimed reactor combined with a narrow band rejection filter operating at a frequency of the RF bias power supply could between the pulsed DC power supply and the target.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rodney G. McDonald whose telephone number is 571-272-1340. The examiner can normally be reached on M-Th with every Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam X. Nguyen can be reached on 571-272-1342. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Rodney G. McDonald/
Primary Examiner, Art Unit 1795

Rodney G. McDonald
Primary Examiner
Art Unit 1795

RM
December 22, 2008

Index of Claims	**Application/Control No.** 11228834	**Applicant(s)/Patent Under Reexamination** ZHANG ET AL.
	Examiner Rodney G McDonald	**Art Unit** 1795

✓	**Rejected**	**-**	**Cancelled**	**N**	**Non-Elected**	**A**	**Appeal**
=	**Allowed**	**÷**	**Restricted**	**I**	**Interference**	**O**	**Objected**

☐ **Claims renumbered in the same order as presented by applicant** ☐ **CPA** ☐ **T.D.** ☐ **R.1.47**

CLAIM		**DATE**								
Final	Original	05/20/2008	12/22/2008							
	1	-	-							
	2	-	-							
	3	-	-							
	4	-	-							
	5	-	-							
	6	-	-							
	7	-	-							
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	9	-	-							
	10	-	-							
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	14	-	-							
1	15	=	=							
2	16	=	=							
3	17	=	=							
4	18	=	=							
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	32	-	-							
	33	-	-							
	34	-	-							
	35	-	-							
	36	-	-							

Index of Claims	**Application/Control No.** 11228834	**Applicant(s)/Patent Under Reexamination** ZHANG ET AL.
	Examiner Rodney G McDonald	**Art Unit** 1795

✓	**Rejected**		**-**	**Cancelled**		**N**	**Non-Elected**		**A**	**Appeal**
=	**Allowed**		**÷**	**Restricted**		**I**	**Interference**		**O**	**Objected**

☐ **Claims renumbered in the same order as presented by applicant** ☐ **CPA** ☐ **T.D.** ☐ **R.1.47**

CLAIM		**DATE**								
Final	Original	05/20/2008	12/22/2008							
	37	-	-							
	38	✓	-							
	39	✓	-							
6	40	=	=							
7	41	=	=							
8	42	=	=							
8	43	=	=							
10	44	=	=							
11	45	=	=							
12	46	=	=							
13	47	=	=							
	48	✓	-							

Search Notes	**Application/Control No.** 11228834	**Applicant(s)/Patent Under Reexamination** ZHANG ET AL.
	Examiner Rodney G McDonald	**Art Unit** 1795

SEARCHED

Class	Subclass	Date	Examiner
204	298.2	12/22/08	/RM/
204	298.06	12/22/08	/RM/
204	298.08	12/22/08	/RM/

SEARCH NOTES

Search Notes	Date	Examiner
See East Search	12/22/08	/RM/

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner
EAST PGPUB		12/22/08	/RM/

	/Rodney G McDonald/ Primary Examiner.Art Unit 1795

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S63	12	((narrow adj band adj rejection adj filter) or (narrow-band adj rejection adj filter)).clm.	US-PGPUB; USPAT	OR	OFF	2008/12/22 10:32
S64	244499	filter.clm.	US-PGPUB; USPAT	OR	OFF	2008/12/22 10:33
S65	218	filter.clm. and (204/192.1-192.28.ccls. or 204/298.01-298.41.ccls.)	US-PGPUB; USPAT	OR	OFF	2008/12/22 10:34

12/22/08 11:58:24 AM
C:\ Documents and Settings\ RMcDonald\ My Documents\ EAST\ Workspaces \ 11339964.wsp

Issue Classification	**Application/Control No.** 11228834	**Applicant(s)/Patent Under Reexamination** ZHANG ET AL.
	Examiner Rodney G McDonald	**Art Unit** 1795

ORIGINAL	
CLASS	**SUBCLASS**
204	298.08

INTERNATIONAL CLASSIFICATION					
CLAIMED					**NON-CLAIMED**
C	2	3	C	14 / 34 (2006.01.01)	

CROSS REFERENCE(S)					
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**				
204	298.2	298.06			

☐ **Claims renumbered in the same order as presented by applicant** ☐ **CPA** ☐ **T.D.** ☐ **R.1.47**

Final	Original	Final	Original	Final	Original
-	1	3	17	-	33
-	2	4	18	-	34
-	3	5	19	-	35
-	4	-	20	-	36
-	5	-	21	-	37
-	6	-	22	-	38
-	7	-	23	-	39
-	8	-	24	6	40
-	9	-	25	7	41
-	10	-	26	8	42
-	11	-	27	9	43
-	12	-	28	10	44
-	13	-	29	11	45
-	14	-	30	12	46
1	15	-	31	13	47
2	16	-	32	-	48

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 13	
/Rodney G McDonald/ Primary Examiner.Art Unit 1795 (Primary Examiner)	12/22/2008 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1A

U.S. Patent and Trademark Office

Part of Paper No. 20081222

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	311	204/298.2.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/12/22 11:50
L2	569	204/298.06.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/12/22 11:50
L3	476	204/298.08.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/12/22 11:50
L4	18	((HONGMEI) near2 (ZHANG)).INV.	US-PGPUB; USPAT	OR	OFF	2008/12/22 11:53
S55	18	((HONGMEI) near2 (ZHANG)).INV.	US-PGPUB; USPAT	OR	OFF	2008/12/22 08:25
S56	56	(narrow adj band adj rejection adj filter)	US-PGPUB; USPAT; USOCR	OR	OFF	2008/12/22 08:43
S57	56	(narrow adj band adj rejection adj filter) or (narrow-band adj rejection adj filter)	US-PGPUB; USPAT; USOCR	OR	OFF	2008/12/22 08:45
S59	30	(rejection adj filter) and ("204"/$.ccls. or "118"/$.ccls. or "427"/$.ccls.)	US-PGPUB; USPAT; USOCR	OR	OFF	2008/12/22 08:52
S60	55	((RICHARD) near2 (DEMARAY)).INV.	US-PGPUB; USPAT	OR	OFF	2008/12/22 09:01
S61	18	((MUKUNDAN) near2 (NARASIMHAN)).INV.	US-PGPUB; USPAT	OR	OFF	2008/12/22 09:09
S62	27	((RAVI) near2 (MULLAPUDI)).INV.	US-PGPUB; USPAT	OR	OFF	2008/12/22 09:11

12/22/08 11:54:09 AM
C:\ Documents and Settings\ RMcDonald\ My Documents\ EAST\ Workspaces\ 11339964.wsp

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

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901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/228,834	09/16/2005	Hongmei Zhang	10655.0016-02	9006

TITLE OF INVENTION: BIASED PULSE DC REACTIVE SPUTTERING OF OXIDE FILMS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	03/30/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
MCDONALD, RODNEY GLENN	1795	204-298080

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Finnegan, Henderson,
2 Farabow, Garrett &
3 Dunner, LLP

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE
SpringWorks, LLC

(B) RESIDENCE: (CITY and STATE OR COUNTRY)
Minnetonka, Minnesota

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies ____________

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, ~~or~~ and credit any overpayment, to Deposit Account Number 06-0916 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature Gary J. Edwards
Date February 20, 2009

Typed or printed name Gary J. Edwards
Registration No. 41,008

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Electronic Patent Application Fee Transmittal

Application Number:	11228834
Filing Date:	16-Sep-2005
Title of Invention:	BIASED PULSE DC REACTIVE SPUTTERING OF OXIDE FILMS
First Named Inventor/Applicant Name:	Hongmei Zhang
Filer:	Gary James Edwards/Annie Wong
Attorney Docket Number:	10655.0016-02

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1810**

Electronic Acknowledgement Receipt

EFS ID:	4830133
Application Number:	11228834
International Application Number:	
Confirmation Number:	9006
Title of Invention:	BIASED PULSE DC REACTIVE SPUTTERING OF OXIDE FILMS
First Named Inventor/Applicant Name:	Hongmei Zhang
Customer Number:	22852
Filer:	Gary James Edwards/Annie Wong
Filer Authorized By:	Gary James Edwards
Attorney Docket Number:	10655.0016-02
Receipt Date:	20-FEB-2009
Filing Date:	16-SEP-2005
Time Stamp:	14:55:58
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1810
RAM confirmation Number	170
Deposit Account	060916
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	Issue_Fee_Transmittal_20Feb2009_11228834.pdf	42782 45b1037d84bf585103aa1f09214195b1c6fb5fcb	no	1
Warnings:					
Information:					
2	Fee Worksheet (PTO-06)	fee-info.pdf	32268 5fd4296af24fc4ecded997090fd532a2f44406ff	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	75050		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/228,834	09/16/2005	Hongmei Zhang	10655.0016-02	9006

22852 7590 04/23/2009
FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER
LLP
901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413

EXAMINER	
MCDONALD, RODNEY GLENN	
ART UNIT	PAPER NUMBER
1795	
MAIL DATE	DELIVERY MODE
04/23/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

Supplemental Notice of Allowability	**Application No.** 11/228,834	**Applicant(s)** ZHANG ET AL.	
	Examiner Rodney G. McDonald	**Art Unit** 1795	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *September 29, 2008*.

2. ☒ The allowed claim(s) is/are *15-19 and 40-47*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
   1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

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P.O. Box 1450
Alexandria, Virginia 22313-1450

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
11228834	9/16/05	ZHANG ET AL.	10655.0016-02

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER
LLP
901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413

EXAMINER	
Rodney G.. McDonald	
ART UNIT	**PAPER**
1795	20090421

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

The attached IDS document is being supplied to indicate that all the references were considered by the examiner. The application remains allowed for reasons of record.

/Rodney G. McDonald/
Primary Examiner, Art Unit 1795

PTO-90C (Rev.04-03)

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

Claims 15-19 are allowable over the prior art of record because the prior art of record does not teach the claimed reactor combined with the narrow band rejection filter that rejects at a frequency of the RF bias power supply coupled between the pulsed DC power supply and the target area.

Claims 40-47 are allowable over the prior art of record because the prior art of record does not teach the claimed reactor combined with a narrow band rejection filter operating at a frequency of the RF bias power supply could between the pulsed DC power supply and the target.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rodney G. McDonald whose telephone number is 571-272-1340. The examiner can normally be reached on M-Th with every Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam X. Nguyen can be reached on 571-272-1342. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Rodney G. McDonald/
Primary Examiner, Art Unit 1795

Rodney G. McDonald
Primary Examiner
Art Unit 1795

RM
April 21, 2009

OIPE
SEP 30 2005
PATENT & TRADEMARK OFFICE

IDS Form PTO/SB/08: Substitute for form 1449A/PTO		**Complete if Known**	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		*Application Number*	11/228,834
		Filing Date	September 16, 2005
		First Named Inventor	ZHANG, Hongmei
		Art Unit	Not Yet Assigned
(Use as many sheets as necessary)		*Examiner Name*	Not Yet Assigned
Sheet 1	of 1	*Attorney Docket Number*	9140.0016-02

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Issue or Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/RM/		5,478,456	12-26-1995	Humpal et al.	
/RM/		6,846,765 B2	01-25-2005	Imamura et al.	

Note: Submission of copies of U.S. Patents and published U.S. Patent Applications is not required.

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	Translation[6]

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation[6]
/RM/		DOREY, R.A., "Low temperature micromoulding of functional ceramic devices," Grant summary for GR/S84156/01 for the UK Engineering and Physical Sciences Research Council, 2 pages (2004).	
/RM/		HOWSON, R.P., "The reactive sputtering of oxides and nitrides," *Pure & Appl. Chem.* *66*(6):1311-1318 (1994).	
/RM/		Office Action issued on August 4, 2005, in U.S. Serial No. 10/101,863 (Attorney Docket No. 09140-0016-00).	
/RM/		Office Action issued on August 8, 2005 in U.S. Serial No. 10/101,341 (Attorney Docket No. 09140-0017-00).	

EXPRESS MAIL LABEL NO.
EV 708642472 US

Examiner Signature	/Rodney Mcdonald/	Date Considered	04/21/2009

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/228,834	06/09/2009	7544276	10655.0016-02	9006

22852 7590 05/20/2009

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER
LLP
901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 529 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Hongmei Zhang, San Jose, CA;
Mukundan Narasimhan, San Jose, CA;
Ravi B. Mullapudi, San Jose, CA;
Richard E. Demaray, Portola Valley, CA;

IR103 (Rev. 11/05)

PATENT
Attorney Docket No. 10655.0016-02000

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Hongmei ZHANG et al.

Application No.: 11/228,834

Filed: September 16, 2005

For: BIASED PULSE DC REACTIVE SPUTTERING OF OXIDE FILMS

Group Art Unit: 1795

Examiner: Rodney G. MCDONALD

Confirmation No.: 9006

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

REQUEST FOR WITHDRAWAL AS ATTORNEY OR AGENT AND CHANGE OF CORRESPONDENCE ADDRESS

I hereby apply to withdraw myself and the practitioners associated with Customer Number 22,852 as attorney or agent for the above-identified patent application.

The reasons for this request are: The Assignee of Record has requested that this application be transferred to another law firm for further prosecution, therefore this request is made under the provision of 37 CFR 10.40(b)(4).

Please change the correspondence address and direct all future correspondence to: Haynes & Boone, LLP, **USPTO Customer Number 27,683**.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: July 28, 2009

By: ____________________
C. Larry O'Rourke
Reg. No. 26,014
(650) 849-6600

Electronic Acknowledgement Receipt

EFS ID:	5782216
Application Number:	11228834
International Application Number:	
Confirmation Number:	9006
Title of Invention:	BIASED PULSE DC REACTIVE SPUTTERING OF OXIDE FILMS
First Named Inventor/Applicant Name:	Hongmei Zhang
Customer Number:	22852
Filer:	Aaron James Capron/Drew Herndon
Filer Authorized By:	Aaron James Capron
Attorney Docket Number:	10655.0016-02
Receipt Date:	28-JUL-2009
Filing Date:	16-SEP-2005
Time Stamp:	13:49:10
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Petition to withdraw attorney or agent (SB83)	Request_for_Withdrawal_10655-0016-02.PDF	12275 8725e234525bb8b540e4990c3566fcdb83162450	no	1

Warnings:

Information:

Total Files Size (in bytes):	12275

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Via EFS-Web
COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

POWER OF ATTORNEY TO PROSECUTE APPLIATIONS BEFORE THE USPTO

Dear Sir:

I hereby appoint practitioners associated with Haynes and Boone Customer Number **27683,** as my/our attorney(s) or agent(s) to prosecute the applications identified in Attachment A, and to transact all business in the United States Patent and Trademark Office connected therewith.

Please recognize or change the correspondence address for the applications listed in Attachment A to Customer Number **27683**.

SpringWorks, LLC, is the Assignee of record of the entire interest in the applications identified in Attachment A by virtue of the assignment recorded in the Reel and Frame numbers listed, or for which a copy therefore is attached, in Attachment A.

SPRINGWORKS, LLC

By: ____________________
Name: Douglas A. Kelley
Title: Receiver

Attachment A
Power of Attorney to Prosecute Applications Before the USPTO

Applicant/Patent Owner: **SpringWorks LLC** hereby states that they are the assignee of the entire right, title and interest as listed below by virtue of an assignment from the inventor(s) of the patent application/patent. The assignment was recorded in the United States Patent and Trademark Office at the Reel and Frame number listed below or for which a copy therefore is attached.

Attorney Docket No.	Application Number / Patent Number	Appl. Date/ Issued Date	Inventors	Title	Current Owner	Chain of Title	Assigment Reel/Frame	Recorded Date
43668.3	11/191,643	7/27/2005	H. Zhang M. Narasimhan R. Mullapudi R. Demaray	Biased Pulse DC Reactive Sputtering Of Oxide Films	SpringWorks LLC	From Inventors to Symmorphix	014766 / 0601	12/2/2003
						From Symmorphix to SpringWorks LLC	20134 / 0102	11/19/2007
43668.4	11/100,856	4/6/2005	T. Pan R. Demaray Y. Chen Y. Xie R. Pethe	Mode Size Converter For A Planar Waveguide	SpringWorks LLC	From Inventors to Symmorphix	020035 / 0110	10/30/2007
						From Symmorphix to SpringWorks LLC	20134 / 0102	11/19/2007
43668.5	10/850,968	5/20/2004	R. Demaray M. Narasimhan	Transparent Conductive Oxides	SpringWorks LLC	From Inventors to Symmorphix	014945 / 0661	8/4/2004
						From Symmorphix to SpringWorks LLC	20134 / 0102	11/19/2007
43668.22	10/650,461	8/27/2003	D. Dawes	Optically Coupling Into Highly Uniform Waveguides	SpringWorks LLC	From Inventors to Symmorphix	014897 / 0768	1/16/2007
						From Symmorphix to SpringWorks LLC	20134 / 0102	11/19/2007
43668.39	11/726,972	3/22/2007	R. Demaray H. Zhang M. Narasimhan V. Milonopoulou	Energy Conversion And Storage Devices By Physical Vapor Deposition Of Titanium And Titanium Oxides And Sub-Oxides	SpringWorks LLC	From Inventors to Symmorphix	014948 / 0097	8/5/2004
						From Symmorphix to SpringWorks LLC	20134 / 0102	11/19/2007
43668.44	11/297,057	12/7/2005	H. Zhang R. Demaray M. Shao	Deposition Of LiCoO2	SpringWorks LLC	From Inventors to Symmorphix	017196 / 0699	12/21/2006
						From Symmorphix to SpringWorks LLC	20134 / 0102	11/19/2007
43668.53	11/218,652	9/2/2005	H. Zhang R. Demaray	Deposition Of Perovskite And Other Compound Ceramic Films From Dielectric Applications	SpringWorks LLC	From Inventors to Symmorphix	016821 / 0220	11/28/2005
						From Symmorphix to SpringWorks LLC	20134 / 0102	11/19/2007
43668.6	10/291,179 US Pat No. 7,404,877	ISSUED - 7/29/08	R. Demaray, V. Milonopoulou	Low temperature zirconia based thermal barrier layer by PVD	SpringWorks LLC	From Inventors to Symmorphix	014756 / 0416	12/2/2003
						From Symmorphix to SpringWorks LLC	20134 / 0102	11/19/2007

Initial: TAK

Attachment A
Power of Attorney to Prosecute Applications Before the USPTO

Applicant/Patent Owner: **SpringWorks LLC** hereby states that they are the assignee of the entire right, title and interest as listed below by virtue of an assignment from the inventor(s) of the patent application/patent. The assignment was recorded in the United States Patent and Trademark Office at the Reel and Frame number listed below or for which a copy therefore is attached.

Attorney Docket No.	Application Number / Patent Number	Appl. Date/ Issued Date	Inventors	Title	Current Owner	Chain of Title	Assigment Reel/Frame	Recorded Date
43668.8	09/903,050 US Pat No. 6,506,289	ISSUED - 1/14/03	R. Demaray, K. Wang, R. Mullapudi, D. Stadtler, H Zhang, R. Peth	Planar optical devices and methods for their manufacture	SpringWorks LLC	From Inventors to Symmorphix	012010 / 0318	07/10/2001
						From Symmorphix to SpringWorks LLC	20134 / 0102	11/19/2007
43668.9	10/288,278 US Pat No. 6,827,826	ISSUED - 12/7/04	R. Demaray, K. Wang, R. Mullapudi, D. Stadtler, H Zhang, R. Pethe	Planar optical devices and methods for their manufacture	SpringWorks LLC	From Inventors to Symmorphix	012010 / 0318	07/10/2001
						From Symmorphix to SpringWorks LLC	20134 / 0102	11/19/2007
43668.13	09/766,463 U.S. Pat No. 6,533,907	ISSUED - 3/18/03	R. Demaray, J. Shan, K. Wang, R. Mullapudi	Method of Producing amorphous silicon for hard mask and waveguide applications	SpringWorks LLC	From Inventors to Symmorphix	011504 / 0738	01/19/2001
						From Symmorphix to SpringWorks LLC	20134 / 0102	11/19/2007
43668.14	09/903,081 US Pat No. 7,469,558	ISSUED - 12/30/08	R. Demaray, K. Wang, R. Mullapudi, Q. Zhu, H. Zhang, H. Ackler, J. Egermeier, R. Pethe	As-deposited planar optical waveguides with low scattering loss and methods for their manufacture	SpringWorks LLC	From Inventors to Symmorphix	012010 / 0752	07/10/2001
						From Symmorphix to SpringWorks LLC	20134 / 0102	11/19/2007
43668.15	10/101,492 US Pat No. 6,884,327	ISSUED - 4/26/05	T. Pan, R. Demaray, Y. Chen, Y. Xie, R. Pethe	Mode size converter for a planar waveguide	SpringWorks LLC	From Inventors to Symmorphix	020035 / 0110	10/30/2007
						From Symmorphix to SpringWorks LLC	20134 / 0102	11/19/2007
43668.17	10/101,863 US Pat No. 7,378,356	ISSUED - 5/27/08	H. Zhang, M. Narasimhan, R. Mullapudi, R. Demaray	Biased pulse DC reactive sputtering of oxide films	SpringWorks LLC	From Inventors to Symmorphix	014766 / 0601	12/2/2003
						From Symmorphix to SpringWorks LLC	20134 / 0102	11/19/2007
43668.21	10/954,182 US Pat No. 7,381,657	ISSUED - 6/30/08	H. Zhang, M. Narasimhan, R. Mullapudi, R. Demaray	Biased pulse DC reactive sputtering of oxide films	SpringWorks LLC	From Inventors to Symmorphix	014766 / 0601	12/2/2003
						From Symmorphix to SpringWorks LLC	20134 / 0102	11/19/2007
43668.19	11/228,834 US Pat No. 7,544,276	ISSUED - 6/9/09	H. Zhang, M. Narasimhan, R. Mullapudi, R. Demaray	Biased pulse DC reactive sputtering of oxide films	SpringWorks LLC	From Inventors to Symmorphix	014766 / 0601	12/2/2003
						From Symmorphix to SpringWorks LLC	20134 / 0102	11/19/2007

Initial:

Attachment A
Power of Attorney to Prosecute Applications Before the USPTO

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Attorney Docket No.	Application Number / Patent Number	Appl. Date/ Issued Date	Inventors	Title	Current Owner	Chain of Title	Assigment Reel/Frame	Recorded Date
43668.20	11/228,717 U.S. Pat No. 7,413,998	ISSUED - 8/19/08	H. Zhang, M. Narasimhan, R. Mullapudi, R. Demaray	Biased pulse DC reactive sputtering of oxide films	SpringWorks LLC	From Inventors to Symmorphix	014766 / 0601	12/2/2003
						From Symmorphix to SpringWorks LLC	20134 / 0102	11/19/2007
43668.25	10/789,953 US Pat No. 7,205,662	ISSUED - 4/17/07	M. Narasimhan, P. Brooks, R. Demaray	Dielectric Barrier Layer Films	SpringWorks LLC	From Inventors to Symmorphix	014948 / 0111	08/05/2004
						From Symmorphix to SpringWorks LLC	20134 / 0102	11/19/2007
43668.32	11/228,805 US Pat No. 7,262,131	ISSUED - 8/28/07	M. Narasimhan, P. Brooks, R. Demaray	Dielectric Barrier Layer Films	SpringWorks LLC	From Inventors to Symmorphix	014948 / 0111	08/05/2004
						From Symmorphix to SpringWorks LLC	20134 / 0102	11/19/2007
43668.34	10/851,542 US Pat No. 7,238,628	ISSUED - 7/3/07	R. Demaray, H. Zhang, M. Narasimhan, V. Milonopoulou	Energy Conversion and Storage Devices by Physical Vapor Deposition of Titanium and Titanium Oxides and Sub-Oxides	SpringWorks LLC	From Inventors to Symmorphix	014948 / 0097	8/5/2004
						From Symmorphix to SpringWorks LLC	20134 / 0102	11/19/2007

SpringWorks LLC

By: Douglas A. Kelley

Name: Douglas A. Kelley

Title: Receiver

Initial: DAK

PTO/SB/122 (11-08)
Approved for use through 11/30/2011. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

CHANGE OF CORRESPONDENCE ADDRESS
Application

Address to:
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	11/228,834
Filing Date	9-16-2005
First Named Inventor	H. Zhang
Art Unit	1795
Examiner Name	Rodney Glenn McDonald
Attorney Docket Number	43668.19

Please change the Correspondence Address for the above-identified patent application to:

☑ The address associated with Customer Number: 27683

OR

☐ Firm or Individual Name

Address

City
State
Zip

Country

Telephone
Email

This form cannot be used to change the data associated with a Customer Number. To change the data associated with an existing Customer Number use “Request for Customer Number Data Change” (PTO/SB/124).

I am the:

☐ Applicant/Inventor

☐ Assignee of record of the entire interest.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

☑ Attorney or agent of record. Registration Number 41008.

☐ Registered practitioner named in the application transmittal letter in an application without an executed oath or declaration. See 37 CFR 1.33(a)(1). Registration Number______________________.

Signature /gary j. edwards/

Typed or Printed Name Gary J. Edwards

Date December 2, 2009
Telephone 408-660-4120

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of ____________forms are submitted.

This collection of information is required by 37 CFR 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	6555152
Application Number:	11228834
International Application Number:	
Confirmation Number:	9006
Title of Invention:	BIASED PULSE DC REACTIVE SPUTTERING OF OXIDE FILMS
First Named Inventor/Applicant Name:	Hongmei Zhang
Customer Number:	22852
Filer:	Gary James Edwards/Sheila Badon
Filer Authorized By:	Gary James Edwards
Attorney Docket Number:	43668.19
Receipt Date:	02-DEC-2009
Filing Date:	16-SEP-2005
Time Stamp:	12:36:01
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		43668_POA.pdf	482094 50be7508dee6f2cb790d6ae139f6af2655b53fda	yes	4

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<tr><td colspan="3">Document Description</td><td>Start</td><td>End</td></tr>
<tr><td colspan="3">Power of Attorney</td><td>1</td><td>1</td></tr>
<tr><td colspan="3">Assignee showing of ownership per 37 CFR 3.73(b).</td><td>2</td><td>4</td></tr>
<tr><td colspan="6">Warnings:</td></tr>
<tr><td colspan="6">Information:</td></tr>
<tr><td>2</td><td>Change of Address</td><td>43668_19_COA.pdf</td><td>298836
63d4b23d35241513314b0ddaf24228702c3fc133</td><td>no</td><td>2</td></tr>
<tr><td colspan="6">Warnings:</td></tr>
<tr><td colspan="6">Information:</td></tr>
<tr><td colspan="3">Total Files Size (in bytes):</td><td colspan="3">780930</td></tr>
</table>

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/228,834	09/16/2005	Hongmei Zhang	43668.19

CONFIRMATION NO. 9006

POWER OF ATTORNEY NOTICE

OC000000039122317

22852
FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER
LLP
901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413

Date Mailed: 12/11/2009

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/02/2009.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/mnguyen/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/228,834	09/16/2005	Hongmei Zhang	43668.19

CONFIRMATION NO. 9006

POA ACCEPTANCE LETTER

OC000000039122358

27683
HAYNES AND BOONE, LLP
IP Section
2323 Victory Avenue
Suite 700
Dallas, TX 75219

Date Mailed: 12/11/2009

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/02/2009.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/mnguyen/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

page 1 of 1

Attorney Docket No. 48604.20

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Assignee	: DEMARAY, LLC	Conf. No.	: 9006
Inventor:	: Hongmei Zhang et al.	Examiner	: Rodney Glenn McDonald
Serial No.	: 11/228,834	Art Unit	: 1795
Title	: BIASED PULSE DC REACTIVE SPUTTERING OF OXIDE FILMS	Filed	: September 16, 2005

VIA EFS-WEB
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Palo Alto, California
November 7, 2019

REQUEST FOR CERTIFICATE OF CORRECTION PTO'S ERROR

Dear Commissioner:

The Patentees submit herewith PTO Form PTO/SB/44 Certificate of Correction. This submission corrects errors by the U.S. Patent and Trademark Office (PTO). Accordingly, the Applicant/Assignee requests a Certificate of Correction or an otherwise corrected patent at the expense of the PTO to correct this error.

We believe that no fee is due. However, if a fee is required, please charge Deposit Account No. 08-1394. If any questions remain or anything additional is required to correct this patent copy, please contact the undersigned at (650) 687-8800.

Respectfully submitted,

Dated: November 7, 2019

By: /Gary J. Edwards/
Gary J. Edwards
Attorney for Applicant
Reg. No. 41,008

Haynes and Boone, LLP
IP Section
2323 Victory Avenue, Suite 700
Dallas, Texas 75219
Telephone: 650.687.8800
Facsimile: 214.200.0853
E-mail: ipdocketing@haynesboone.com

FILED VIA EFS
CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being transmitted to the United States Patent and Trademark Office (USPTO) via the USPTO's EFS-Web electronic filing system on November 7, 2019.

/Ryan Bordon/
Ryan Bordon

PTO/SB/44 (09-07)
Approved for use through 01/31/2020. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

Page 1 of 1

PATENT NO. : 7,544,276

APPLICATION NO.: 11/228,834

ISSUE DATE : June 9, 2009

INVENTOR(S) : Hongmei Zhang, Mukundan Narasimhan, Ravi B. Mullapudi, and Richard E. Demaray

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims:

In Claim 1 Column 22, Line 49, change "RE" to --RF--.

MAILING ADDRESS OF SENDER (Please do not use Customer Number below):

Haynes and Boone LLP
2323 Victory Avenue #700
Dallas, TX 75219

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	37691395
Application Number:	11228834
International Application Number:	
Confirmation Number:	9006
Title of Invention:	BIASED PULSE DC REACTIVE SPUTTERING OF OXIDE FILMS
First Named Inventor/Applicant Name:	Hongmei Zhang
Customer Number:	27683
Filer:	Gary James Edwards/Ryan Bordon
Filer Authorized By:	Gary James Edwards
Attorney Docket Number:	48604.20
Receipt Date:	07-NOV-2019
Filing Date:	16-SEP-2005
Time Stamp:	19:00:49
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Certificate of Correction	48604_20US01_Request_for_Certificate_of_Correction.pdf	177051 353f75494ab680d5a519b965e9685369a5a50fd1	no	3

Warnings:

Information:	
Total Files Size (in bytes):	177051

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,544,276 B2
APPLICATION NO. : 11/228834
DATED : June 9, 2009
INVENTOR(S) : Hongmei Zhang et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims

In Claim 1 Column 22, Line 49, change “RE” to --RF--.

Signed and Sealed this
Third Day of December, 2019

Andrei Iancu

Andrei Iancu
Director of the United States Patent and Trademark Office