Vivek Subramanian

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Education

3 / 96 - 6 / 98

Ph.D. in Electrical Engineering, Stanford University
Stanford, California
Honors earned: Graduate Fellowship, Eastman Kodak Company

9 / 94 - 3 / 96

MS in Electrical Engineering, Stanford University
Stanford, California

8 / 90 - 5 / 94

BS in Electrical Engineering, Louisiana State University
Baton Rouge, Louisiana
Honors earned: Summa cum laude, College Honors, Outstanding Senior, Junior and Sophomore, Honors College

Professional Experience

2018 - present

École polytechnique fédérale de Lausanne
Switzerland

8/18 – present: Professor of Microengineering

2000 - present

Department of Electrical Engineering & Computer Sciences, University of California
Berkeley, CA

7/20 to date: Adjunct Professor
7/18 – 6/20: Chancellor's Professor
7/11 – 6/20: Professor
7/05 – 7/11: Associate Professor
7/00-7/05: Assistant Professor
Research, teaching and service in EECS Department
Honors Earned:

2015 IEEE Kiyo Tomiyasu Award
Best in session and best in track awards, 2013 IMAPS Microelectronics Conference
Outstanding paper award, 2012 IMAPS Microelectronics Conference
2008 Printed Electronics Champion, Printed Electronics USA Conference, November 2008
Outstanding Teaching Award, EECS Department, UC Berkeley, 2005
Best paper award, 2004 IEEE Device Research Conference
Nominated to MIT's Technology Review top 100 young innovators list (TR100), 2002
National Science Foundation Young Investigator (CAREER) Award, FY2002,
Nominated to National Academy of Engineering's *Frontiers of Engineering*, 2002
Winner of 2002 Paul Rappaport Award for best paper in an IEEE EDS Journal

2009 - present

Adjunct Professor, Sunchon National University
Sunchon, Korea
2013 to date: Adjunct Professor, BK21 Program
2009-2013: Adjunct Professor and Principal Investigator, WCU Program
Initiated, managed, and contributed to large multinational research program focused on printed electronics, including displays, energy devices, and RFID

2000 - present

Independent Consultant
Orinda, CA
Consultant to the semiconductor industry and its associated fields in the following areas:

Memory technology and design, Silicon Process Technology
Display / Imager and Flexible Electronics Technology, RFID Technology
Intellectual Property Consulting
Technology Evaluation / Venture Capital due diligence

Founder and CTO, Locix Inc.
San Bruno, CA
Senior leadership role in venture-funded startup company working on wireless networking

2004 – 2013 **Founding Scientific Advisor, Kovio, Inc.**
Sunnyvale, CA
Scientific advising to printed electronics startup company

2008 - 2011 **Chief Technical Advisor, QuSwami, Inc.**
San Francisco, CA
Scientific advising to energy conversion device startup company
Served as CTO from July 2010-June 2011

1998 - 2000 **Consulting Assistant Professor, Electrical Engineering Department, Stanford University.**
Stanford, CA
Advisory role for research group of Prof. Krishna C. Saraswat

1998-2000 **Visiting Research Engineer, Electrical Engineering Department, University of California.**
Berkeley, CA
Research into 25nm MOSFET technologies for giga-scale integration

1998 - 2000 **Founder, Matrix Semiconductor, Inc.**
Santa Clara, CA
Co-founder and technical advisor of startup company working on high-density memory technology
Honors Earned:
Nominated to Scientific American's SA50 List for Visionary Technology
Finalist for 2003 World Technology Award for Information Technology Hardware
Winner, 2005 EDN Innovation Award

1998 **Co-instructor, Electrical Engineering Department, Stanford University.**
Stanford, CA
Co-teaching of EE311, Advanced Integrated Circuit Fabrication Processes

1997 **Intern, Advanced Product Research and Development Laboratory, Motorola Inc.**
Austin, TX
Research into process development issues affecting SiGe SEMFET devices

1996 **Head Teaching Assistant EE410: IC Fabrication Laboratory, Stanford University**
Stanford, CA
Coordination and instruction of EE410, graduate level laboratory course.

1994-1998 **Research Assistant, Electrical Engineering, Stanford University**
Stanford, CA
Research into crystallization of amorphous Si and SiGe films using low thermal budget processes.

Professional Affiliations and Activities

Technical Program Committee, IEEE Electronic Components and Technology Conference, 2014 to 2016
Chair, Scientific Advisory Board, iPACK, Royal Institute of Technology (KTH), Sweden, 2011 to 2016
Tampere Institute of Technology Faculty Search Committee, Finland, 2013
University of Oulu Faculty Search Committee, Finland, 2013
Served as external thesis committee member for several universities world-wide, including University of Cape Town (South Africa), Tampere Institute of Technology (Finland), Technical University of Eindhoven (Netherlands), Indian Institute of Science (India), Indian Institute of Technology (India), 2009 to date
Associate Editor, IEEE Journal of Display Technology, 2008 to date
Technical Program Chair, Large Area, Organic, and Printed Electronics Conference, 2012-2013
Scientific Committee, Large Area, Organic, and Printed Electronics Conference, 2009-2011
Scientific Committee, International Conference on Printed and Flexible Elecronics, 2009-2013
IEEE Electron Devices Society Organic Electronics Committee, 2003 - 2005
Executive Committee, International Electron Device Meeting, 2003 to 2009
Technical Program Committee, International Electron Device Meeting, 2001-2002
Technical Program Committee member, Device Research Conference, 2000-2002
Technical Program Committee member, VLSI-TSA Conference, 2005

List of Patents, Publications and Presentations

Patents

1. "Systems and methods for using ranging to determine locations of wireless sensor nodes based on radio frequency communications between the nodes and various RF-enabled devices", T. Ylamurto, M. Seth, L. Kong, V. Subramanian, US Patent 10,551,479
2. "Systems and methods for providing communications within wireless sensor networks based on a periodic beacon signal", T. Ylamurto, V, Pavate, E. Alon, V. Subramanian, US Patent 10,536,901
3. "Systems and methods for using radio frequency signals and sensors to monitor environments", T. Bakhishev, V. Subramanian, V. Pavate T. Ylamurto, US Patent 10,514,704.
4. "Systems and methods for using radio frequency signals and sensors to monitor environments", T. Bakhishev, V. Subramanian, V. Pavate T. Ylamurto, US Patent 10,504,364
5. "Systems and methods for coarse and fine time of flight estimates for precise radio frequency localization in the presence of multiple communication paths", M. Seth, L. Kong, T. Ylamurto, V. Subramanian, US Patent 10,470,156
6. "Methods and apparatus for monitoring wound healing using impedance spectroscopy", M. Maharbiz, V. Subramanian, A. C. Arias, S. Swisher, A. Liao, M. Lin, F. Pavinatto, Y. Khan, D. Cohen, E. Leeflang, S. Roy, M. Harrison, D. Young, US Patent 10,463,293
7. "Systems and methods for using radio frequency signals and sensors to monitor environments", T. Bakhishev, V. Subramanian, V. Pavate T. Ylamurto, US Patent 10,156,852.
8. "Systems and methods for determining locations of wireless sensor nodes in a tree network architecture having mesh-based features", L. Kong, T. Bakhishev, T. Ylamurto, V. Subramanian, M. Seth, US Patent 10,104,508.
9. "Systems and methods for providing wireless asymmetric network architectures of wireless devices with power management features", V. Subramanian, E. Alon, V. Pavate, US Patent 10,028,220.
10. "Random delay generation for thin-film transistor based circuits", V Subramanian, M Mao, Z Wang, US Patent 9,985,664
11. "Systems and methods for determining locations of wireless sensor nodes in a network architecture having mesh-based features for localization", L. Kong, T. Bakhishev, T. Ylamurto, V. Subramanian, M. Seth, US Patent 9,846,220
12. "Systems and methods for determining locations of wireless sensor nodes in a tree network architecture having mesh-based features", L. Kong, T. Bakhishev, T. Ylamurto, V. Subramanian, M. Seth, US Patent 9,763,054
13. "Through silicon vias and thermocompression bonding using inkjet-printed nanoparticles", V. Subramanian and J. Sadie, US Patent 9,717,145
14. "Systems and methods for providing wireless asymmetric network architectures of wireless devices with anti-collision features", V. Subramanian, E. Alon, V. Pavate, US Patent 9,706,489
15. "Systems and methods for determining locations of wireless sensor nodes in an asymmetric network architecture", V. Subramanian, E. Alon, V. Pavate, US Patent 9,529,076
16. "Systems and methods for providing wireless sensor networks with an asymmetric network architecture", V. Subramanian, E. Alon, V. Pavate, US Patent 9,380,531
17. "Transparent metal oxide nanoparticle compositions, methods of manufacture thereof and articles comprising the same", V. Subramanian, S. K. Volkman, US Patent 9,343,202
18. "Three-dimensional nonvolatile memory and method of fabrication", M. G. Johnson, T. H. Lee, V. Subramanian, P. M. Farmwald, J. M. Cleeves, US Patent 9,214,243
19. "Dense arrays and charge storage devices", T. H. Lee, V. Subramanian, J. M. Cleeves, I. G. Kouznetsov, M. G. Johnson, P. M. Farmwald, US Patent 9,171,857
20. "Print compatible designs and layout schemes for printed electronics", Z. Wang, V. Subramanian, L. Cleveland, US Patent 9,155,202
21. "Wireless devices including printed integrated circuitry and methods for manufacturing and using the same", P. Smith, C. Choi, V. Pavate, J. M. Cleeves, V. Subramanian, R. Young, V. Biviano, US Patent 9,004,366.

22. “Dense arrays and charge storage devices “, T. H. Lee, V. Subramanian, J. M. Cleeves, M. G. Johnson, P. M. Farmwald, I. Kouznetzov, US Patent, 8,981,457.
23. “High reliability surveillance and/or identification tag/devices and methods of making and using the same”, V. Subramanian, P. Smith, V. Pavate, A. Kamath, C. Choi, A. Chandra, J. M. Cleeves, US Patent, 8,933,806.
24. “Surveillance devices with multiple capacitors”, P. Smith, C. Choi, J. M. Cleeves, V. Subramanian, A. Kamath, S. Molesa, US Patent, 8,912,890.
25. “Pillar-shaped nonvolatile memory and method of fabrication”, M. G. Johnson, T. H. Lee, V. Subramanian, P. M. Farmwald, J. M. Cleeeves, US Patent 8,897,056
26. “Dense arrays and charge storage devices”, T. H. Lee, V. Subramanian, J. M. Cleeves, I. G. Kouznetsov, M. G. Johnson, P. M. Farmwald, US Patent 8,853,765
27. “Dense arrays and charge storage devices”, T. H. Lee, V. Subramanian, J. M. Cleeves, I. G. Kouznetsov, M. G. Johnson, P. M. Farmwald, US Patent 8,823,076
28. “Random delay generation for thin-film transistor based circuits”, V. Subramanian, M. Mao, Z. Wang, US Patent 8,810,298
29. “Vertically stacked field programmable nonvolatile memory and method of fabrication”, M. Johnson, T. Lee, V. Subramanian, M. Farmwald, and J. M. Cleeves, US Patent 8,503,215
30. “Process-variation tolerant series-connected NMOS and PMOS diodes, and standard cells, tags, and sensors containing the same”, V. Subramanian, P. Smith, US Patent 8,471,308
31. “Printed compatible designs and layout schemes for printed electronics”, Z. Wang, V. Subramanian, L. Cleveland, US Patent 8,383,952
32. “Method for making surveillance devices with multiple capacitors”, P. Smith, C. Choi, J. M. Cleeves, V. Subramanian, A. Kamath, S. Molesa, US Patent 8,296,943
33. “High reliability surveillance and/or identification tag/devices and methods of making and using the same”, V. Subramanian, P. Smith, V. Pavate, A. Kamath, C. Choi, A. Chandra, and J. M. Cleeves, US Patent 8,264,359
34. “High reliability surveillance and/or identification tag/devices and methods of making and using the same”, V. Subramanian, P. Smith, V. Pavate, A. Kamath, C. Choi, A. Chandra, and J. M. Cleeves, US Patent 8,227,320
35. “Vertically stacked field programmable nonvolatile memory and method of fabrication”, M. Johnson, T. Lee, V. Subramanian, M. Farmwald, and J. M. Cleeves, US Patent 8208282
36. “Reliable tag deactivation”,J. M. Cleeves, V. Subramanian, US Patent 8138921
37. “Combined static and dynamic frequency divider chains using thin film transistors”, V. Subramanian, US Patent 8085068
38. “Process-variation tolerant diode, standard cells including the same, tags and sensors containing the same, and methods for manufacturing the same”, V. Subramanian, P. Smith, US Patent 7932537
39. “Three terminal nonvolatile memory Device with vertical gated diode”, T. H. Lee, V. Subramanian, J. M. Cleeves, M. G. Johnson, P. M. Farmwald, I. G. Kouznetsov, US Patent 7825455
40. “Vertically stacked field programmable nonvolatile memory and method of fabrication”, V. Subramanian, J. M. Cleeves, US Patent 7816189
41. “Multi-mode tags and methods of making and using the same”, P. Smith, J. M. Cleeves, V. Pavate, V. Subramanian, US Patent 7750792
42. “Method of manufacturing complementary diodes”, V. Subramanian, P. Smith, US Patent 7528017
43. “Vertically stacked field programmable nonvolatile memory and method of fabrication”, V. Subramanian, J. M. Cleeves, US Patent 7319053
44. “Vertically stacked field programmable nonvolatile memory and method of fabrication”, V. Subramanian, J. M. Cleeves, US Patent 7265000
45. “Vertically stacked field programmable nonvolatile memory and method of fabrication”, V. Subramanian, J. M. Cleeves, US Patent 7160761
46. “Vertically stacked field programmable nonvolatile memory and method of fabrication”, V. Subramanian, J. M. Cleeves, US Patent 7157314

47. “Dense arrays and charge storage devices”, T. H. Lee, V. Subramanian, J. M. Cleeves, A. J. Walker, C. Petti, I. Kouznetzov, M. G. Johnson, P. M. Farmwald. B. Herner, US Patent 7129538

48. “Patterning three dimensional structures”, C. K. Li, J. N. Knall, M. A. Vyvoda, J. M. Cleeves, V. Subramanian, US Patent 7071565

49. “Monolithic three dimensional array of charge storage devices containing a planarized layer”, T. H. Lee, V. Subramanian, J. M. Cleeves, A. J. Walker, C. J. Petti, I. G. Kouznetzov, M. G. Johnson, P. M. Farmwald, and B. Herner, US Patent 6881994

50. “Thermal processing for three dimensional circuits”, V. Subramanian, J. M. Cleeves, J. N. Knall, C. K. Li, and M. A. Vyvoda, US Patent 6,770,939

51. “Vertically stacked field programmable nonvolatile memory and method of fabrication”, M. G. Johnson, T. H. Lee, V. Subramanian, and P. M. Farmwald, US Patent 6780711

52. “Multigate semiconductor device with vertical channel current and method of fabrication”, J. M. Cleeves and V. Subramanian, US Patent 6677204

53. “Thermal processing for three dimensional circuits”, V. Subramanian, J. M. Cleeves, J. N. Knall, C. K. Li, and M. A. Vyvoda, US Patent 6624011

54. “Multigate semiconductor device with vertical channel current and method of fabrication”, J. M. Cleeves and V. Subramanian, US Patent 6580124

55. “Patterning three dimensional structures”, C. K. Li, J. N. Knall, M. A. Vyvoda, J. M. Cleeves, and V. Subramanian, US Patent 6627530

56. “Low cost three-dimensional memory array”, M. Johnson, T. Lee, V. Subramanian, P. Farmwald, J. Knall, US Patent 6515888

57. “Integrated circuit structure including three-dimensional memory array”, M. Johnson, T. Lee, V. Subramanian, P. M. Farmwald, J. M. Cleeves, US Patent 6385074.

58. “FINFET transistor structures having double gate channel extending vertically from a substrate and methods of manufacture”, C. Hu, T-J. King, V. Subramanian, L. Chang, X. Huang, Y-K. Choi, J. T. Kedzierski, N. Lindert, J. Bokor, W-C. Lee, US Patent 6413802

59. “Vertically stacked field programmable nonvolatile memory and method of fabrication”, M. Johnson, T. Lee, V. Subramanian, M. Farmwald, and J. M. Cleeves, US Patent 6185122.

60. “Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication”, M. Johnson, T. Lee, V. Subramanian, M. Farmwald, and J. M. Cleeves, US Patent 6034882.

61. “Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication”, M. Johnson, T. Lee, V. Subramanian, M. Farmwald, and J. M. Cleeves, US Patent 6351406.

62. “Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication”, M. Johnson, T. Lee, V. Subramanian, M. Farmwald, and J. M. Cleeves, US Patent 6483736.

Invited Magazine Articles, Books, Chapters, and Monographs

1. Chapter in “Inkjet Technology for Digital Fabrication”, Editors: Ian M. Hutchings, Graham D. Martin, Wiley, ISBN: 978-0470681985

2. Chapter in “Applications of Organic and Printed Electronics: A Technology-Enabled Revolution (Integrated Circuits and Systems), Editor: E. Cantatore, ISB: 978-1-461-43159-6

3. Chapter in “Inkjet-based Micromanufacturing”, Editors: Korvink, Smith, Shin, Wiley, ISBN: 978-3-527-31904-6

4. Chapter in “Organic Electronics II. More Materials and Applications", Editor: H. Klauk, Wiley, ISBN: 978-3-527-32647-1

5. Chapter in “Transparent Electronics: From Synthesis to Applications”, Editors: A. Facchetti and T. Marks, Wiley, ISBN: 978-0-470-99077-3, 2010.

6. Chapter in “The chemistry of inkjet inks”, Editor: S. Magdassi, World Scientific Publishing Company, ISBN: 978-9812818218, 2009

7. Chapter in “Organic Field-Effect Transistors”, Editors: Z. Bao, and J. Locklin, CRC Press, ISBN: 978-0849380808, 2007

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