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United States Patent [19]

Thompson

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[54] **POWER CONSUMPTION REDUCTION IN MEDICAL DEVICES BY EMPLOYING PIPELINE ARCHITECTURE**

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[73] Assignee: **Medtronic, Inc.**, Minneapolis, Minn.

[21] Appl. No.: **09/289,502**

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Related U.S. Application Data

[63] Continuation-in-part of application No. 09/067,881, Apr. 29, 1998, abandoned, and a continuation-in-part of application No. 09/181,460, Oct. 28, 1998, and a continuation-in-part of application No. 09/181,459, Oct. 28, 1998, and a continuation-in-part of application No. 09/181,517, Oct. 28, 1998, and a continuation-in-part of application No. 09/181,523, Oct. 28, 1998.

[51] **Int. Cl.**[7] **A61N 1/36**

[52] **U.S. Cl.** **607/2**

[58] **Field of Search** 607/2, 9, 5; 395/750.03, 395/750.04, 750.07, 800.32, 800.33, 800.34, 556, 555, 557

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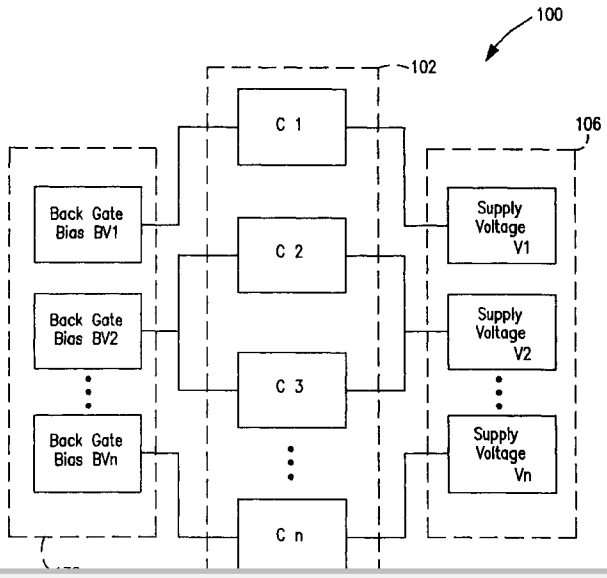
[57] **ABSTRACT**

Power consumption in medical and battery powered devices is reduced through the use and operation of pipeline architecture in a digital signal processor, microcontroller or microprocessor by operating such devices at clock frequencies tailored to conserve power while preserving computational and executional performance. The digital signal processor, microcontroller or microprocessor can be operated at lower clock frequencies relative to those that would be required by one of such processors to complete the multiple functions within a predetermined time period but having no pipeline architecture. With reduced clock frequency, power consumption is reduced. Further, with reduced clock speed, supply voltages applied to such processors may also be reduced.

63 Claims, 20 Drawing Sheets



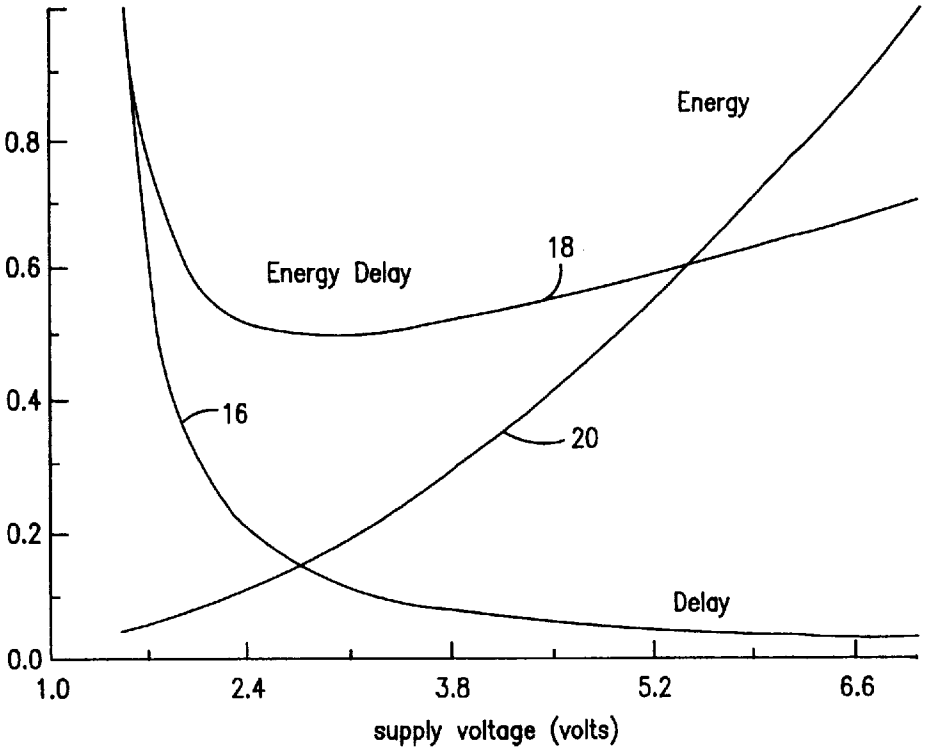


FIG. 1

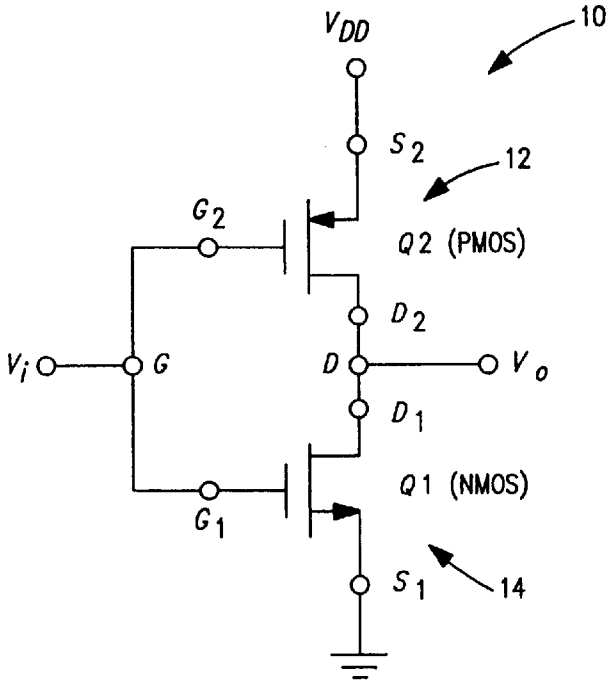


FIG. 2

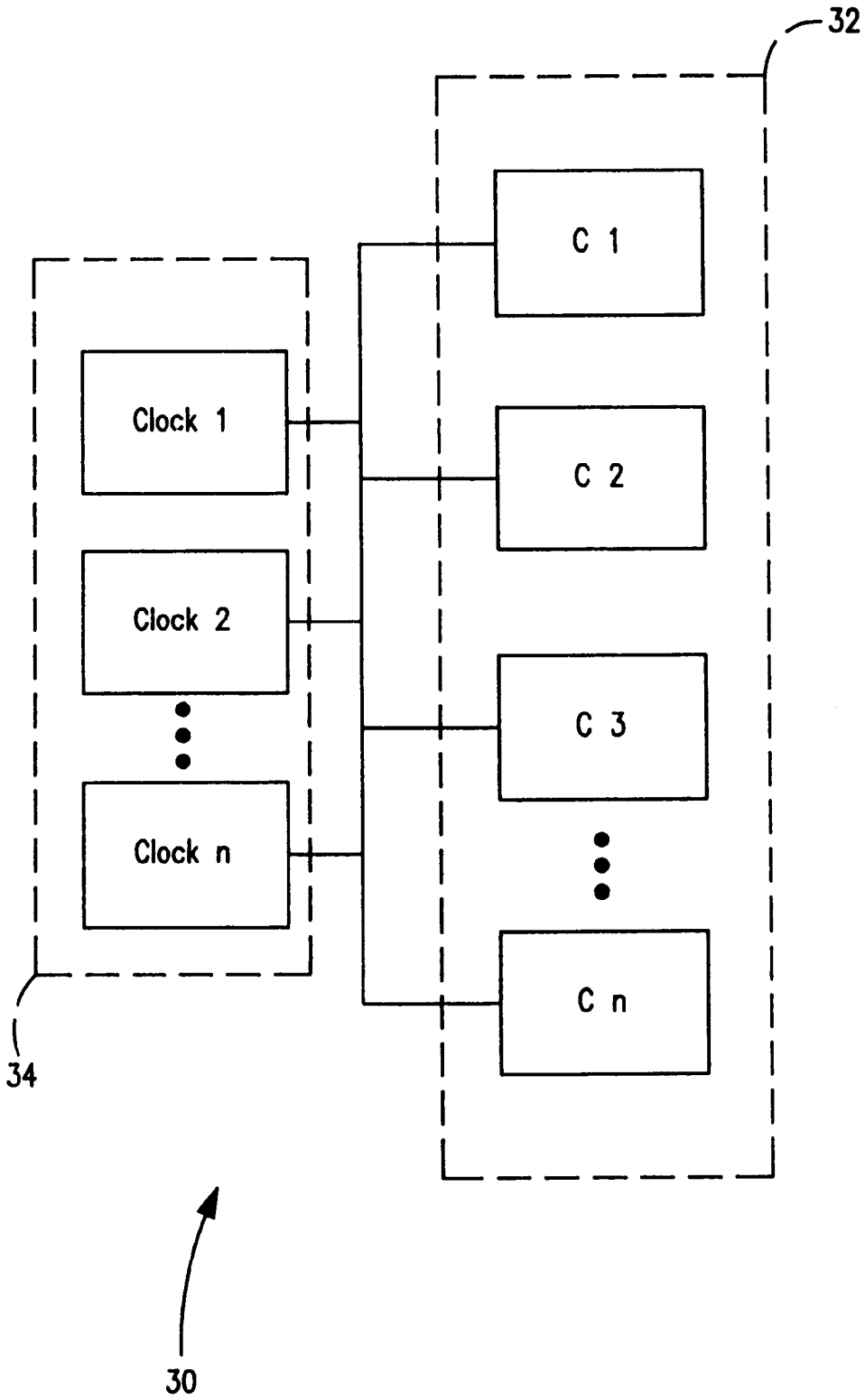


FIG. 3

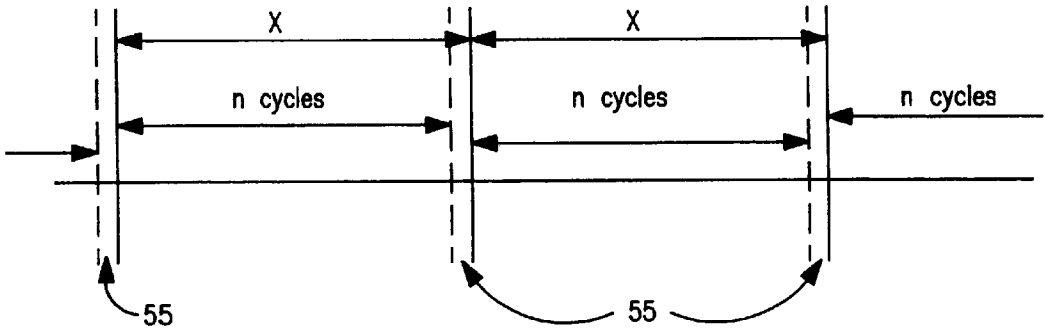


FIG. 4A

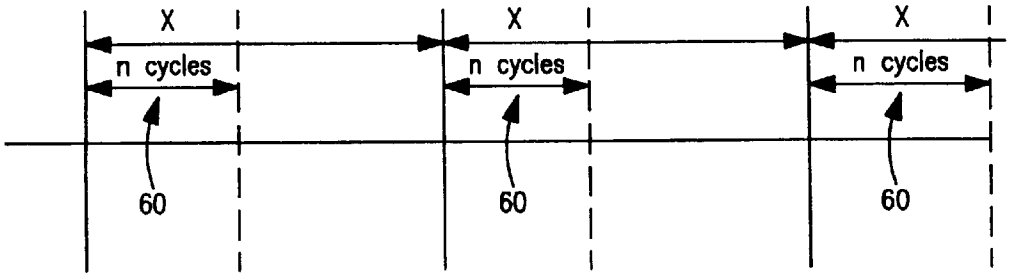


FIG. 4B

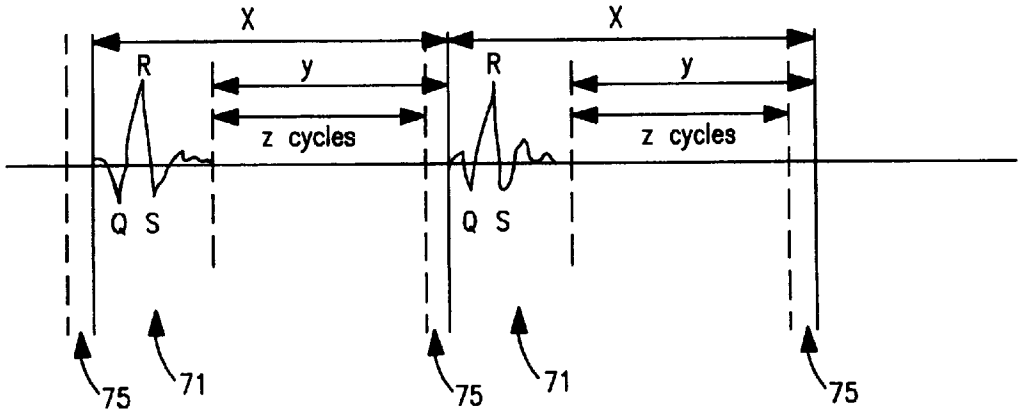


FIG. 4C

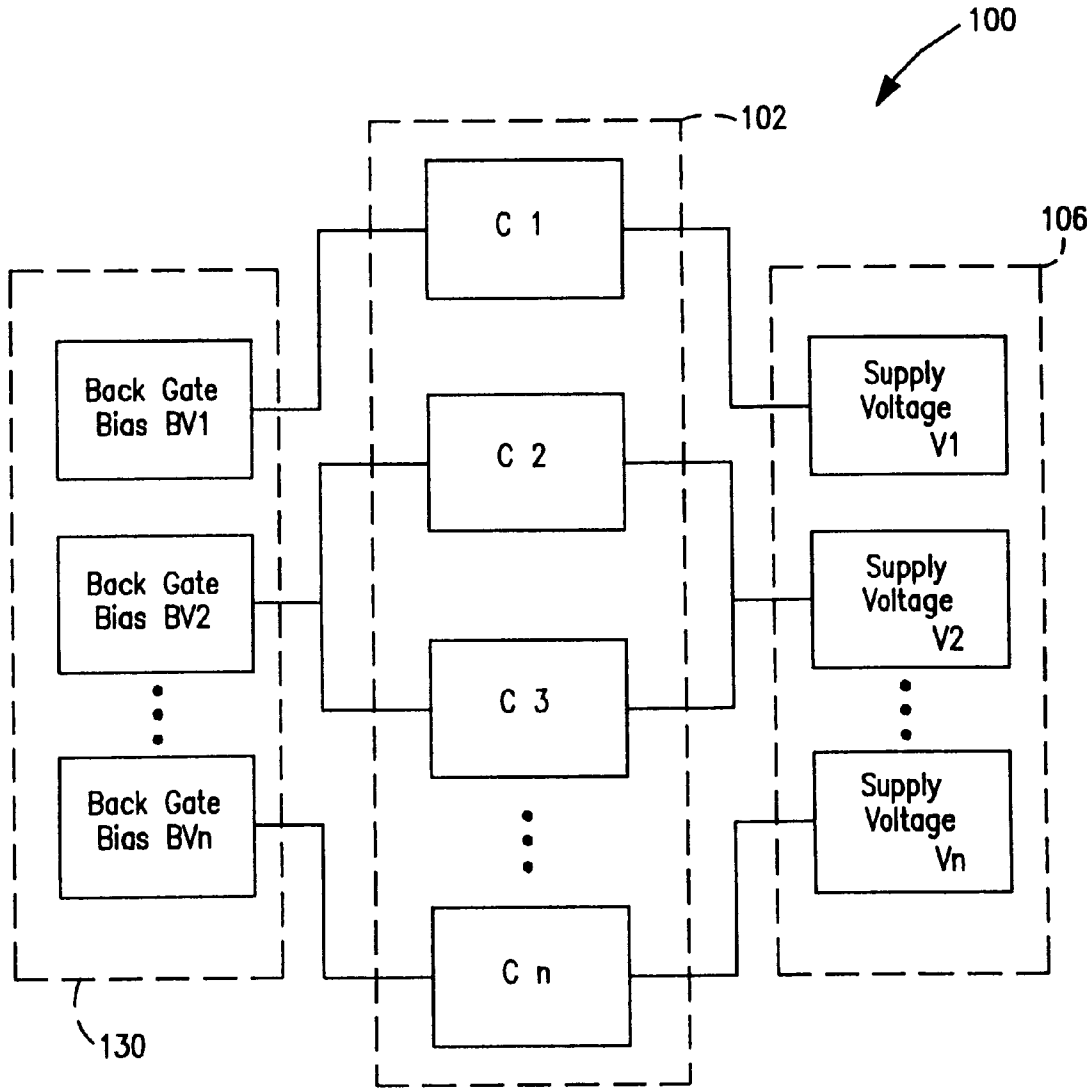


FIG. 5

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