UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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QUALCOMM INCORPORATED

PETITIONER

v.

MONTEREY RESEARCH, LLC,

PATENT OWNER

_____

INTER PARTES REVIEW NO. IPR2020-01492
PATENT 6,651,134

_____

PETITIONER'S DEMONSTRATIVES

Qualcomm

Petitioner's Hearing Demor
IPR2020-01492

# U.S. Patent No. 6,651,

December 7, 2021

'134 Patent

— **Purports to have developed "non-interruptible" bu**

Schaefer

— Schaefer discloses "non-interruptible" burst operations

— A user command is issued at T2 before the precharge is i

— PO's Expert concedes that the only user command is issu

— Petitioner's Expert confirms Schaefer's disclosure

— PO's Expert reliance on "termination" commands is not a

— Schaefer's purported goals do not negate anticipation
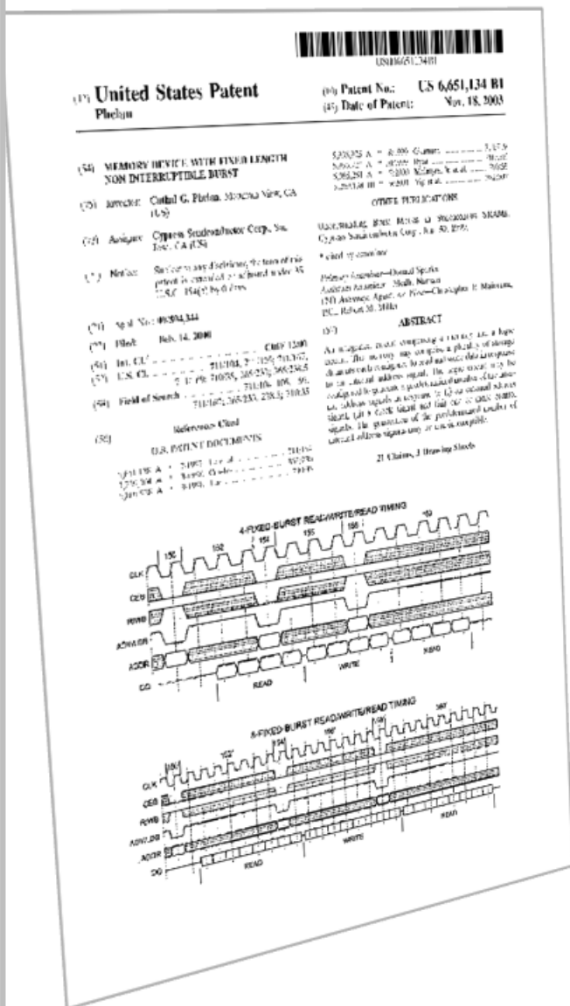
(12) **United States Patent**
Phelan

(10)

(45)

(54) **MEMORY DEVICE WITH FIXED LENGTH NON INTERRUPTIBLE BURST**

(75) Inventor: **Cathal G. Phelan**, Mountain View, CA (US)

(73) Assignee: **Cypress Semiconductor Corp.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/504,344**

(22) Filed: **Feb. 14, 2000**

SUMMARY OF THE I

The present invention concern
comprising a memory and a logi
may comprise a plurality of S
configured to read and write data i
address Signal. The logic circuit
generate a predetermined number
Signals in response to (i) an exter
clock signal and (iii) one or mo
generation of the predetermine
address signals may be non-interru
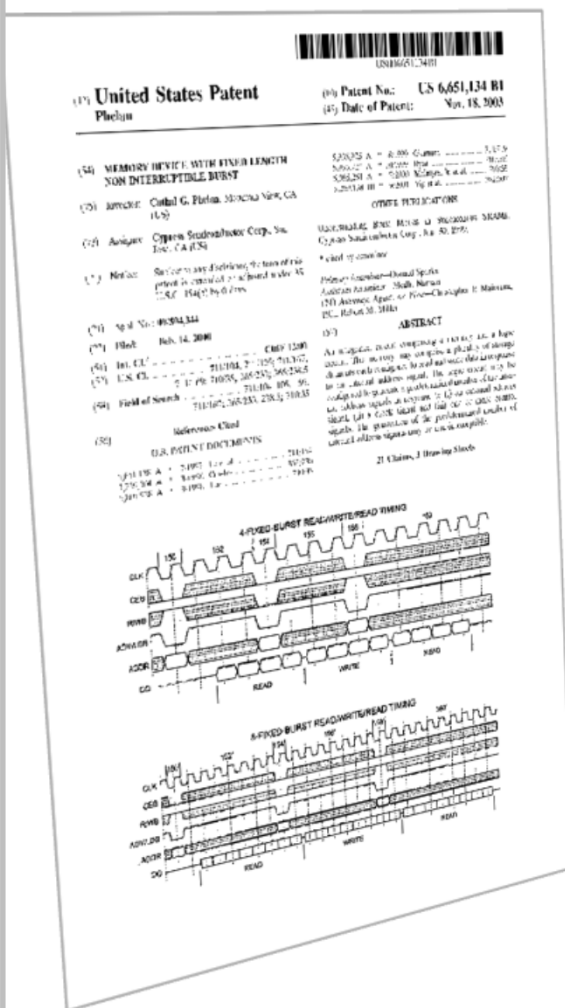
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