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Attorneys for Defendant
GSI TECHNOLOGY, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

CYPRESS SEMICONDUCTOR CORPORATION,

Plaintiff,

v.

GSI TECHNOLOGY, INC.,

Defendant.

CASE NOS. 3:13-cv-02013-JST (JCS)
4:13-cv-03757-JST (JCS)

DECLARATION OF ROBERT MURPHY IN SUPPORT OF DEFENDANT GSI TECHNOLOGY, INC.'S RESPONSIVE CLAIM CONSTRUCTION BRIEF

DATE: May 20, 2014
TIME: 2:00 P.M.
PLACE: Courtroom 9, 19th floor
JUDGE: Hon. Jon S. Tigar

I, Robert Murphy, do hereby declare:

1. I am making this declaration at the request of GSI Technology Inc. in support of its responsive claim construction brief. I am being compensated for my work in this matter at the rate of $450 per hour. My compensation in no way depends upon the outcome of this proceeding.

2. In preparing this declaration and forming the opinions expressed below, I have considered:

a. U.S. Patent No. 6,651,134 (the "'134 patent");

b. The file history of the '134 patent;

c. U.S. Patent No. 6,069,839 (the "'839 patent");

d. The file history of the '839 patent;

e. U.S. Patent No. 6,292,403 (the "'403 patent");

f. The file history of the '403 patent;

g. The various pieces of evidence listed in the Joint Claim Construction and Prehearing Statement under Patent Local Rule 4-3 and the exhibits thereto dated January 27, 2014;

h. Plaintiff Cypress's Opening Claim Construction Brief dated February 26, 2014 and the exhibits thereto;

i. My knowledge and experience based upon my work in this area as described below.

I. Qualifications and Professional Experience

3. As indicated in my Curriculum Vitae, attached as Exhibit A, I received a B.S. in Electrical Engineering from Drexel University in 1974, and a M.S. in Electrical Engineering from University of California, Los Angeles (UCLA) in 1976.

4. While at Hughes Aircraft Co. from 1974-1978, in addition to other circuit designs, I designed charged coupled device (CCD) based memories that included control circuitry, addressing scheme and circuitry, data input and data output paths. The CCD based memories used a CCD device as a memory cell to store data in a different manner than is done with a DRAM

memory. In memories that use either a CCD memory cell or a single transistor based memory cell such as is used in a DRAM memory, the memories must be addressed to either read or write data into the memory, must have the other usual control circuitry and must have read data paths and write data paths to get the data into or out from the memory. As a result, the control circuitry, addressing scheme and circuitry, data input and data output paths for the CCD based memories are very similar to the control circuitry, addressing scheme and circuitry, data input and data output paths used in other semiconductor memories.

5. In 1978, I was hired at National Semiconductor Corp. to design a pseudostatic dynamic random access memory (DRAM). As part of the design of the pseudostatic DRAM, I designed the sense amplifiers for the device. The pseudo-static DRAM used CCD devices for the memory cells, but used the same manufacturing processes and circuitry as typical DRAM.

6. About a year after my hire at National Semiconductor Corp., I transferred over to the static random access memory (SRAM) group and then learned about various SRAM operations including addressing, data outputting and controlling of the SRAM. As part of the work, I designed a four transistor (4T) cell 4K SRAM product. After the 4T cell 4K SRAM product was built, I was promoted to SRAM design manager. As the SRAM design manager, I was responsible for all SRAM designs. As part of my role as SRAM design manager, I resolved an SRAM yield crash in 62 days. I was responsible for the SRAM designs in production in the amount of 30,000 4 inch wafers per month.

7. From 1982 to 1983, I was a program manager at RCA and led the development of a 64K SRAM including the design, layout, process development and manufacturing of the SRAM part. As part of that development of the 64K SRAM, the team that I led also created a 4K SRAM test chip.

8. At Silicon Graphics, I was in charge of all circuit designers including cache designers for a major microprocessor. I was also responsible for the circuit design of a floating point processor for a microprocessor system.

9. In 1998, I founded a company, Firenza, LLC., that develops and licenses high performance building blocks for semi-custom and ASIC designs. A part of those designs that I

have built are memory blocks. For example, I was hired to build memory blocks for a DVD controller chip that included a MIPs processor core. The memories included i-cache, d-cache; i-tag, d-tag and 22 dual port register files.

II. Overview of the '134 Patent

10. The '134 patent is generally directed to a computer memory that is used for volatile storage of data. The '134 patent more specifically relates to burst read and write operations ("burst operations") using a circuit, such as a volatile memory. '134 patent at Title and col. 2, lines 25-38. In burst operations, two or more pieces of data are read from the volatile memory or written to the volatile memory. The '134 patent relates to burst operations in which the generation of internal address signals is non-interruptible. '134 patent at col. 3: 5-29 and col. 4: 15-48. A fixed length non-interruptible burst generally frees up the address bus and control bus for a known number of cycles. '134 patent at col. 3: 56-58.

11. The specification of the '134 patent describes the circuits used within the volatile memory.

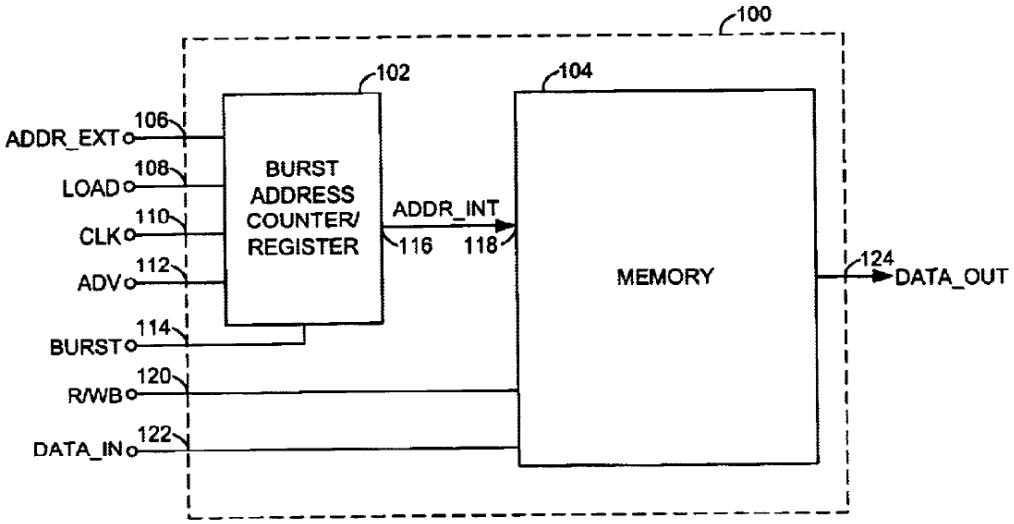

FIG. 1

12. As shown in Figure 1 of the '134 patent reproduced above, the circuit 100 has a logic circuit 102 that generates multiple internal address signals (ADDR_INT) that are fed into a

memory 104 to write/read burst data to/from the memory 104. The logic circuit uses a number of signals in order to generate the multiple internal address signals, such as an external address signal (ADDR_EXT) that is generated external to the circuit 100 as shown in Figure 1, a clock signal (CLK) that is generated external to the circuit 100 and one or more control signals (LOAD, ADV and BURST).

13. The logic circuit may be a burst address counter/register as shown in Figure 1. The other embodiments of the logic circuit shown have an address counter register and a burst counter (Figure 2) or a latch, counter and multiplexer (Figure 3).

14. To perform the addressing for the burst operation, the external address is a starting address of the burst. '134 patent at col. 4: 4-14. The logic circuit then generates a fixed number of internal addresses based on the starting address.

II. Claim Construction

15. It is my understanding that in order to properly evaluate a patent, the terms of the claims must first be interpreted. It is also my understanding that the claims should be construed in light of their ordinary and customary meaning, which is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention. It is my further understanding that claim terms are given their ordinary and accustomed meaning as would be understood by one of ordinary skill in the art, unless the inventor, as a lexicographer, has set forth a special meaning for a term.

16. In order to construe the claims, I have reviewed the entirety of the '134, '839 and '403 patents, as well as their prosecution histories.

A. Level of Ordinary Skill in the Art

17. In my opinion, a person of ordinary skill in the art as of the time of the '134 patent would have had a BS in Electrical Engineering and 5 years of experience with direct SRAM design experience.

18. In my opinion, a person of ordinary skill in the art as of the time of the '403 and '839 patents would have needed to have the capability of understanding the scientific and engineering principles applicable to the '839 patent and '403 patent, which would have required a

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