UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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QUALCOMM INC.,
Petitioner,

v.

MONTEREY RESEARCH, LLC,
Patent Owner.

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IPR2020-01492
Patent 6,651,134 B1

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Before KRISTEN L. DROESCH, JOHN F. HORVATH, and
JASON W. MELVIN, *Administrative Patent Judges*.

MELVIN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I.   INTRODUCTION

Qualcomm Inc., ("Petitioner") filed a Petition (Paper 1, "Pet.") requesting institution of *inter partes* review of claims 1–7 and 9–21 ("the challenged claims") of U.S. Patent No. 6,651,134 B1 (Ex. 1001, "the '134 patent"). Pet. 6. Monterey Research, LLC, ("Patent Owner") filed a Preliminary Response. Paper 6 ("Prelim. Resp."). After our email authorization, Petitioner filed a Preliminary Reply (Paper 7) and Patent Owner filed a Preliminary Sur-Reply (Paper 8). Pursuant to 35 U.S.C. § 314 and 37 C.F.R. § 42.4(a), we have authority to determine whether to institute review.

An *inter partes* review may not be instituted unless "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a). For the reasons set forth below, we conclude that Petitioner has shown a reasonable likelihood it will prevail in establishing the unpatentability of at least one challenged claim, and we therefore institute *inter partes* review.

A.   REAL PARTIES IN INTEREST

Petitioner identifies itself, Qualcomm Technologies, Inc., and Qualcomm CDMA Technologies Asia-Pacific Pte Ltd. as real parties in interest. Pet. 2. Patent Owner identifies itself and IPValue Management as real parties in interest. Paper 3, 1.

B.   RELATED MATTERS

As required by regulation, the parties identify matters related to the '134 patent. Pet. 2–3; Paper 3, 1–2. Of note is *Advanced Micro Devices, Inc.*

v. Monterey Research, LLC, IPR2020-00985, in which AMD challenges all claims of the '134 patent. We instituted review in that proceeding on December 2, 2020. IPR2020-00985, Paper 13. Additionally, the district-court case involving Qualcomm is identified as *Monterey Research, LLC v. Qualcomm Inc. et al.*, No. 1:19-cv-02083 (D. Del. 2019), whereas the case involving AMD is identified as *Monterey Research, LLC v. Advanced Micro Devices Inc.*, No. 1:19-cv-02149 (D. Del. 2019). Paper 3, 1; Pet. 3.

C.   THE '134 PATENT

The '134 patent is titled Memory Device with Fixed Length Non Interruptible Burst. Ex. 1001, code (54). The patent discloses that "the data burst transfers of conventional memories can be interrupted and single access made," and proposes a memory device "that has a fixed burst length." *Id.* at 1:37–45.
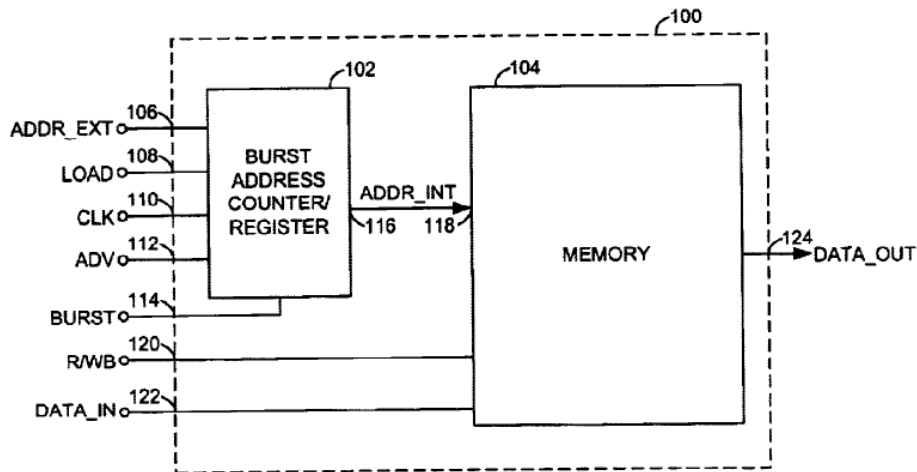
Figure 1 is reproduced below:

FIG. 1

Ex. 1001, Fig. 1. Figure 1 depicts circuit 100 configured as a fixed burst memory, in which circuit 102 accepts external signals including external

address signal ADDR_EXT, and "generate[s] the signal ADDR_INT as a fixed number of addresses in response to the signal CLK." *Id.* at 3:21–22. The '134 patent states that "[o]nce the circuit 102 has started generating the fixed number of addresses, the circuit 102 will generally not stop until the fixed number of addresses has been generated (e.g., a non-interruptible burst)." *Id.* at 3:25–28.

The '134 patent depicts two embodiments for circuit 102, in Figures 2 and 3. Figure 2 is reproduced below:
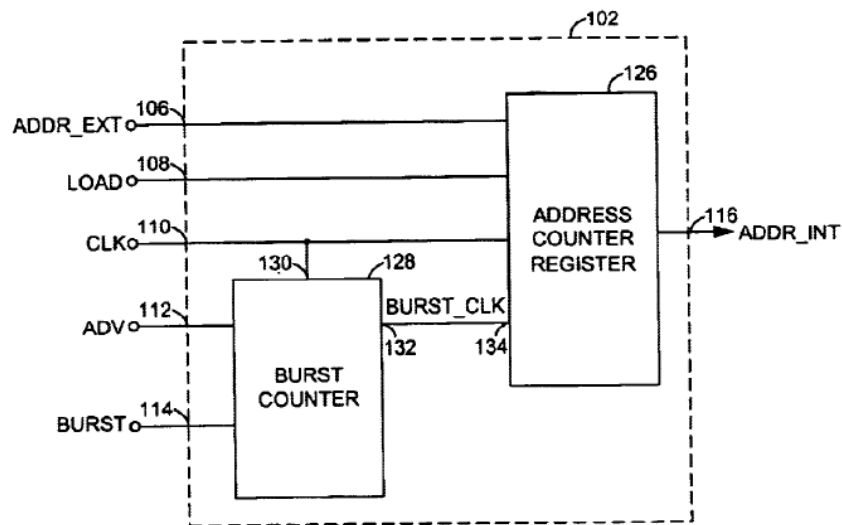

FIG. 2

Id. Fig. 2. Figure 2 shows burst counter 128 receiving signal CLK (a clock signal), signal ADV, and signal BURST, and providing signal BURST_CLK. "When the signal ADV is asserted, the burst counter 128 will generally present the signal BURST_CLK in response to the signal CLK. The signal BURST_CLK generally contains a number of pulses that has been programmed by the signal BURST." *Id.* at 4:10–14. Figure 3 and the associated description disclose an alternative circuit, in which "counter 138 may be configured to generate a number of addresses in response to the

signals CLK, BURST[,] and ADV" and where "[t]he number of addresses generated by the counter 138 may be programmed by the signal BURST." *Id.* at 4:29–34. The '134 patent describes more generally that, "[w]hen the signal ADV is asserted, the circuit 100 will generally generate a number of address signals" and that "[t]he address signals will generally continue to be generated until the Nth address signal is generated." *Id.* at 4:42–48.

D.   CHALLENGED CLAIMS

Challenged claim 1 is reproduced below:

1.   A circuit comprising:

a memory comprising a plurality of storage elements each configured to read and write data in response to an internal address signal; and

a logic circuit configured to generate a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

Ex. 1001, 5:22–32. Independent claim 16 recites limitations similar to those of claim 1, expressed as means-plus-function elements. *Id.* at 6:20–30. Independent claim 17 recites limitations similar to those of claim 1, expressed as a "method of providing a fixed burst length data transfer." *Id.* at 6:31–39. Claims 2–7 and 9–15 depend, directly or indirectly, from claim 1. *Id.* at 5:33–6:19. Claims 18–21 depend, directly or indirectly, from claim 17. *Id.* at 6:40–48.

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