

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

QUALCOMM INCORPORATED

PETITIONER

v.

MONTEREY RESEARCH, LLC

PATENT OWNER

***INTER PARTES* REVIEW NO. IPR2020-01492
PATENT 6,651,134**

PETITION FOR *INTER PARTES* REVIEW UNDER 35 U.S.C. § 312

TABLE OF CONTENTS

PETITIONER’S EXHIBIT LISTiv

I. INTRODUCTION1

II. MANDATORY NOTICES2

 A. Real Party in Interest (37 C.F.R. § 42.8(b)(1))2

 B. Related Matters (37 C.F.R. § 42.8(b)(2)).....2

 C. Lead and Back-Up Counsel (37 C.F.R. § 42.8(b)(3)).....3

 D. Service Information (37 C.F.R. § 42.8(b)(4)).....4

III. THE GROUNDS IN THIS PETITION ARE NOT CUMULATIVE
OVER THE GROUNDS IN IPR2020-009854

IV. GROUNDS FOR STANDING.....5

V. STATEMENT OF PRECISE RELIEF REQUESTED FOR EACH
CLAIM CHALLENGED6

 A. Claims for Which Review Is Requested (37 C.F.R. §
42.104(b)(1))6

 B. Statutory Grounds of Challenge (37 C.F.R. § 42.104(b)(2))6

VI. FIELD OF TECHNOLOGY7

 A. DRAM Memory and Architecture7

 B. DRAM Operations9

 C. External Commands vs. Internal Procedures11

 D. Burst Termination.....13

VII. LEVEL OF ORDINARY SKILL IN THE ART14

VIII. THE ’134 PATENT14

 A. Admitted Prior Art.....15

 B. The ’134 Patent’s Asserted Improvement to the Prior Art15

 C. Prosecution History18

 D. Claim Construction (37 C.F.R. § 42.104(b)(3)).....21

 1. “non-interruptible” (claims 1, 16, 17)21

 2. “internal address signal” (claims 1-4, 10-12, 15-17).....21

3.	<i>“predetermined number of [said] internal address signals” (claims 1-4, 10-12, 15-18, 21) / “fixed burst length” (claims 2, 5-7, 17)</i>	22
4.	<i>“means for reading data ... / means for generating a predetermined number of said internal address signals” (claim 16)”</i>	24
IX.	REASONS FOR THE RELIEF REQUESTED UNDER 37 C.F.R. §§ 42.22(a)(2) and 42.104(b)(4)	27
A.	Ground 1A – Claims 1-5, 7, 9-10, 12-18, 20, and 21 are anticipated by US 5,600,605 (“Schaeffer”).....	27
1.	<i>Overview of Schaefer</i>	27
2.	<i>Element-by-element analysis</i>	36
B.	Ground 1B – Claims 1-7, 9-10, and 12-21 are Obvious Over Schaefer in View of Fujioka.....	64
1.	<i>Fujioka</i>	65
2.	<i>Motivation to combine Schaefer and Fujioka</i>	66
3.	<i>Modification of Schaefer in view of Fujioka</i>	68
4.	<i>Element-by-element analysis</i>	69
C.	Ground 2A – Claim 11 is Obvious Over Schaefer and Lysinger	77
1.	<i>Lysinger</i>	77
2.	<i>Motivation to combine Schaefer and Lysinger</i>	79
3.	<i>Modification of Schaefer in view of Lysinger</i>	81
4.	<i>Element-by-element analysis</i>	82
D.	Ground 2B – Claim 11 is Obvious Over Schaefer in View of Lysinger and Fujioka.....	82
1.	<i>Motivation to combine Schaefer with Lysinger and Fujioka</i>	82
2.	<i>Modification of Schaefer with Lysinger and Fujoka</i>	82
3.	<i>Element-by-element analysis</i>	83
X.	CONCLUSION.....	83

PETITIONER'S EXHIBIT LIST

Exhibit	Shorthand	Description
1001	'134 Patent	U.S. Patent No. 6,651,134
1002		Omitted
1003		Omitted
1004	'134 File History	Prosecution History of U.S. Patent No. 6,651,134
1005		Omitted
1006	Fujioka	U.S. Patent No. 6,185,149
1007	Tiede	U.S. Patent No. 5,900,021
1008		Omitted
1009	Lysinger	U.S. Patent No. 5,784,331
1010		Omitted
1011	U.S.I.T.C Claim Construction Order	Order 29 Construing Claims, Inv. No. 337-TA-792, U.S.I.T.C (February 9, 2012)
1012	N.D. Cal Claim Construction Order	Order Construing Claims, Cypress Semiconductor Corp. v. GSU Tech., Inc., 13-cv-02013-JST (N.D. Cal.) (July 29, 2014)
1013	Commission Opinion	Commission Opinion, Inv. No. 337-TA-792, U.S.I.T.C. (June 28, 2013)
1014	Lowrey	U.S. Patent No. 5,360,992
1015	Murphy	Declaration of Robert Murphy
1016	Murphy CV	Curriculum Vitae of Robert Murphy
1017	Schaefer	U.S. Patent No. 5,600,605
1018	Cypress Whitepaper	Cypress Semiconductor, Understanding Burst Modes in Synchronous SRAMs (June 30, 1999)
1019	Cypress Response	Complainant Cypress Semiconductor Corporation's Response to Respondents' Petition for Review of the Remand Initial Determination on Validity and Enforceability (April 3, 2013)
1020	Cowles	U.S. Patent No. 5,729,504
1021	CMOS Circuit Design	Baker et al, CMOS Circuit Design, Layout, and Simulation (First Ed. 1998)
1022	Monterey FAC	First Amended Complaint in <i>Monterey Research, LLC v. Qualcomm Incorporated, et. al</i> , No. 19-cv-2083-CFC (D. Del. Feb. 14, 2020)
1023	IPR2020-00985	Petition for <i>Inter Partes</i> Review, IPR2020-00985, Paper 1, filed May 26, 2020.

I. INTRODUCTION

The '134 Patent is directed to well-known “burst” functionality in which a memory device generates a number of internal addresses in response to a single external address. EX1001, Abstract, 1:57-58. In the claimed burst functionality: (1) the generation of the internal address signals is “non-interruptible,” and (2) the number of internal address signals is “predetermined” / “fixed” (yet “programmable”). Both are disclosed by the prior art cited in this Petition.

First, Schaefer discloses read-and-write burst operations “with auto-precharge” in which “[t]he user is not allowed to issue another command until the precharged time (t_{RP})” at the end of the operation “is completed.” EX1017, 7:42-44.¹ Thus, Schaefer discloses a “non-interruptible” burst.

Second, Schaefer discloses a burst length / number of internal address signals is “predetermined” / “fixed” through programming of a mode register. *Id.*, 6:1-2 (“Burst lengths of 2, 4, 8, or full page (1,024) cycles are programmable into mode register 40”); *see also* EX1022, ¶94 (asserting Claim 1 is met by technical standard in which burst length is set by programming mode register). And, to the extent PO may contradict its own infringement mapping here, and assert that burst length must be “predetermined” / “fixed” during fabrication, Fujioka discloses the

¹ All emphasis added unless otherwise indicated.

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts



Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research



With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips



Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.