Paper No. 1

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

QUALCOMM INCORPORATED

PETITIONER

v.

MONTEREY RESEARCH, LLC

PATENT OWNER

***INTER PARTES* REVIEW NO. IPR2020-01492**
PATENT 6,651,134

PETITION FOR *INTER PARTES* REVIEW UNDER 35 U.S.C. § 312

TABLE OF CONTENTS

PETITIONER'S EXHIBIT LIST

Exhibit	Shorthand	Description
1001	'134 Patent	U.S. Patent No. 6,651,134
1002		Omitted
1003		Omitted
1004	'134 File History	Prosecution History of U.S. Patent No. 6,651,134
1005		Omitted
1006	Fujioka	U.S. Patent No. 6,185,149
1007	Tiede	U.S. Patent No. 5,900,021
1008		Omitted
1009	Lysinger	U.S. Patent No. 5,784,331
1010		Omitted
1011	U.S.I.T.C Claim Construction Order	Order 29 Construing Claims, Inv. No. 337-TA-792, U.S.I.T.C (February 9, 2012)
1012	N.D. Cal Claim Construction Order	Order Construing Claims, Cypress Semiconductor Corp. v. GSU Tech., Inc., 13-cv-02013-JST (N.D. Cal.) (July 29, 2014)
1013	Commission Opinion	Commission Opinion, Inv. No. 337-TA-792, U.S.I.T.C. (June 28, 2013)
1014	Lowrey	U.S. Patent No. 5,360,992
1015	Murphy	Declaration of Robert Murphy
1016	Murphy CV	Curriculum Vitae of Robert Murphy
1017	Schaefer	U.S. Patent No. 5,600,605
1018	Cypress Whitepaper	Cypress Semiconductor, Understanding Burst Modes in Synchronous SRAMs (June 30, 1999)
1019	Cypress Response	Complainant Cypress Semiconductor Corporation's Response to Respondents' Petition for Review of the Remand Initial Determination on Validity and Enforceability (April 3, 2013)
1020	Cowles	U.S. Patent No. 5,729,504
1021	CMOS Circuit Design	Baker et al, CMOS Circuit Design, Layout, and Simulation (First Ed. 1998)
1022	Monterey FAC	First Amended Complaint in *Monterey Research, LLC v. Qualcomm Incorporated, et. al*, No. 19-cv-2083-CFC (D. Del. Feb. 14, 2020)
1023	IPR2020-00985	Petition for *Inter Partes* Review, IPR2020-00985, Paper 1, filed May 26, 2020.

I. INTRODUCTION

The '134 Patent is directed to well-known "burst" functionality in which a memory device generates a number of internal addresses in response to a single external address. EX1001, Abstract, 1:57-58. In the claimed burst functionality: (1) the generation of the internal address signals is "non-interruptible," and (2) the number of internal address signals is "predetermined" / "fixed" (yet "programmable"). Both are disclosed by the prior art cited in this Petition.

First, Schaefer discloses read-and-write burst operations "with auto-precharge" in which "***[t]he user is not allowed to issue another command*** until the precharged time (t_{RP})" at the end of the operation "is completed." EX1017, 7:42-44.[1] Thus, Schaefer discloses a "non-interruptible" burst.

Second, Schaefer discloses a burst length / number of internal address signals is "predetermined" / "fixed" through programming of a mode register. *Id.*, 6:1-2 ("Burst lengths of 2, 4, 8, or full page (1,024) cycles are programmable into mode register 40"); *see also* EX1022, ¶94 (asserting Claim 1 is met by technical standard in which burst length is set by programming mode register). And, to the extent PO may contradict its own infringement mapping here, and assert that burst length must be "predetermined" / "fixed" during fabrication, Fujioka discloses the

[1] All emphasis added unless otherwise indicated.

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