Understanding Burst Modes in Synchronous SRAMs

Introduction

With the addition of the clock, synchronous SRAMs are able to provide several features that are not possible with asynchronous SRAMs. These include:

- Controlled timings on outputs
- Different write modes ($\overline{ADSP}$/$\overline{ADSC}$)
- Reading multiple locations using a single address using Burst modes

One of the more useful features of synchronous SRAMs is the burst mode. This application note discusses the different burst modes on synchronous SRAMs.

What is a Burst Mode?

Synchronous SRAMs are able to provide data from multiple address locations with the association of a single address. The advantage of this operation is that, by providing a single address, data from four locations can be obtained, thereby reducing the activity on the address bus.

Figure 1 shows the signals associated with the burst feature.

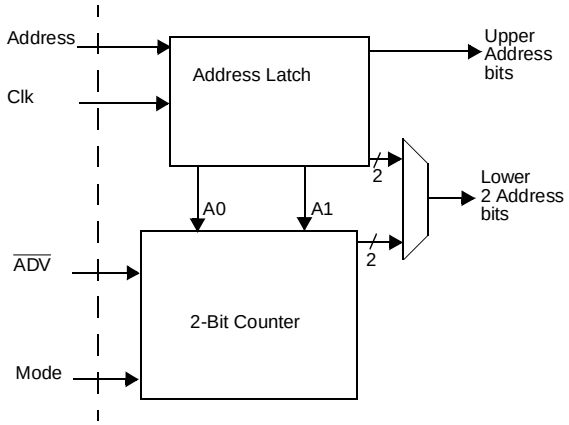

Figure 1. Key Signals for Burst Feature on Typical SRAMs

Table 1 provides the definitions for the signals shown in *Figure 1*.

Function

On the rising edge of the clock, the address and control pins are latched into the SRAM. All accesses for standard synchronous SRAMs are initiated the same way. Depending on the control signals, a read or write transaction is initiated. On the next rising edge of the clock, the $\overline{ADV}$ pin is sampled. If $\overline{ADV}$ is sampled active LOW, a burst access is initiated and the SRAM continues the present operation with an address obtained from the internal counter. The burst continues until

Table 1. Definition of Signals

Pin	Definition
Address	Address Inputs used to select one of the address locations in the SRAM. Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and CE is sampled active. A[1:0] feed the 2-bit counter.
CLK	Clock Input. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW, during a burst operation.
$\overline{ADV}$	Advance Input signal, sampled on the rising edge of CLK. When asserted, it automatically increments the address in a burst cycle.
Mode	Selects burst order. When tied to GND selects linear burst sequence.When tied HIGH or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation.

the advance pin is HIGH, or a new cycle is started. If the $\overline{ADV}$ is asserted sufficiently, the SRAM will wrap around to the originally accessed address location. This is a result of a 2-bit burst counter that can access four address locations.

The Mode pin controls the order or sequence of the burst. Currently, two popular different burst sequences are available. Both of them are described below.

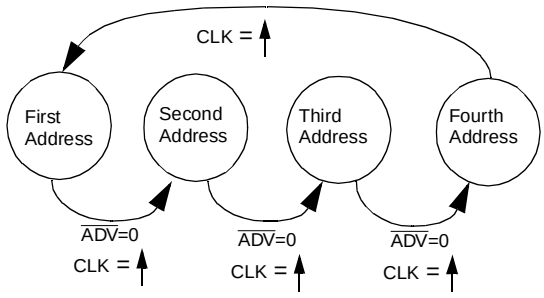

Figure 2. Burst Mode Address Update

Linear Burst

If the Mode pin is tied LOW, the device operates in the linear method of operation. In the Linear Burst mode of operation, the internal counter counts in a linear fashion up from the present value with A1 and A0 being the LSBs. This is shown in the table below.

	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address	1	1	0	0	0	1	1	0

From an implementation standpoint, this is a simple 2-bit counter.

Interleaved Burst

If the Mode pin is tied HIGH, the device operates in the interleaved method of operation.

In the Interleaved Burst mode of operation, the internal counter behaves a bit differently. The sequence in the interleaved burst is determined by the first address. The sequence is shown below.

	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0

From an implementation stand point, this is a 2-bit counter with some added logic as shown in *Figure 3*. The 2-bit counter is reset on every new address cycle and A0/A1 are the bits latched from the start of the cycle. The Interleaved Burst order is especially popular with Intel-based systems.

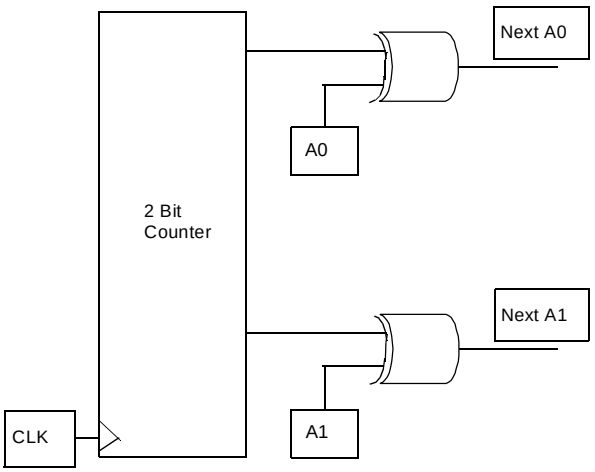

Figure 3. Implementation to Generate the Interleaved Burst Sequence.

Conclusion

In terms of general operation, one method of burst does not have any significant advantages over the other. Different processors support different kinds of bursts. Intel processors support the interleaved burst scheme, while the Power PC microprocessors support the linear burst mode of operation.

Burst Modes in Synchronous SRAMs can be very useful. The advantages are:

- Reduced activity on the address bus (four memory locations accessed with a single address)
- Address generation to the SRAM allowing the controller to perform other functions
- More reliable since the address location is generated inside the SRAM.